RRA78640

Low Voltage, 10MHz, RRIO, CMOS Operational Amplifier

Description

The RRA78640 is a quad operational amplifier (op amp) featuring low power consumption and rail-to-rail input and output capabilities. It operates on supply voltages ranging from 1.8V to 5.5V, making it suitable for a wide range of general-purpose applications. The device is unity-gain stable, ensuring reliable performance across various use cases.

The input common-mode voltage range extends 100mV above and below the power supply voltage rails, enabling compatibility with virtually any single-supply application. The rail-to-rail input and output swing enhances signal dynamic range and signal-to-noise ratio, a critical advantage in low-supply applications. With high signal bandwidth and a high slew rate, the RRA78640 is ideal for driving the sample-and-hold circuitry of analog-to-digital converters (ADCs). Additionally, the output stage can swing to within 20mV of the supply rails with a 10kΩ load, ensuring efficient and precise operation.

Part	Package	Body Size (nom)
RRA78640	NSOIC-14	3.91mm×8.65mm
	TSSOP-14	4.40mm×5.00mm

Features

- Single-Supply Operation: 1.8V to 5.5V
- Rail-To-Rail Input and Output
- Low Input Offset Voltage: ±0.45mV
- Low Noise: 15nV/√Hz at 10kHz
- Gain Bandwidth Product: 10MHz
- Slew Rate: 7.5V/µs
- Low Supply Current: 520µA/Ch
- Unity-Gain Stable
- No Phase Reversal
- Temperature Range: -40°C to 125°C
- Internal RFI and EMI filter

Applications

- Washing Machines
- Refrigerators
- HVAC
- Smoke Detectors
- Scanners
- Filters
- Signal Conditioning
- Current Sensing
- Motor Control

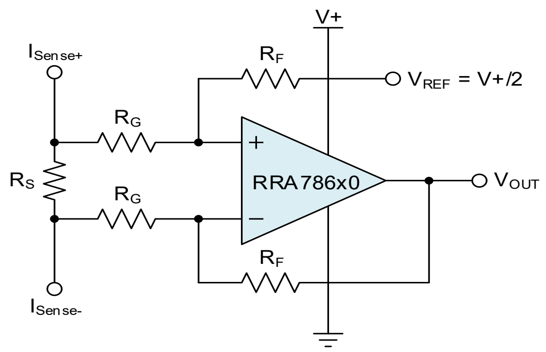


Figure 1. Typical Application - Bidirectional Current Sense Amplifier

Contents

1. Pin Information

1.1 Pin Assignment

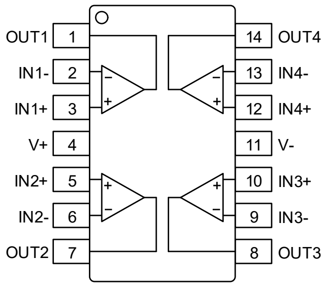


Figure 2. Pin Assignments - Top View

1.2 Pin Description

Pin Name	RRA78640 NSOIC, TSSOP	Function
IN+	–	Non-inverting Signal Input
IN1+	3	
IN2+	5	
IN3+	10	
IN4+	12	
IN-	–	Inverting Signal Input
IN1-	2	
IN2-	6	
IN3-	9	
IN4-	13	
OUT	–	Signal Output
OUT1	1	
OUT2	7	
OUT3	8	
OUT4	14	
V+	4	Positive Supply Voltage
V-	11	Negative Supply Voltage

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, V+ to V-	-	6.0	V
Input Voltage, IN± to GND	(V-) – 0.5	(V+) + 0.5	V
Input Voltage, IN+ to IN-	-	6.0	V
Input Current	-	±10	mA
Output Short-Circuit	Continuous		mA
Ambient Temperature, T_A	-40	125	°C
Junction Temperature, T_J	-	150	°C
Storage Temperature, T_{stg}	-65	150	°C
ESD Ratings			
Human Body Model (Tested per JS-001-2023)	-	±2	kV
Charged Device Model (Tested per JS-002-2022)	-	±1.5	kV
Latch-Up (Tested per JESD78B), T_A = 125°C	-	±100	mA

2.2 Thermal Specifications

Parameter	Package	Symbol[1][2]	Conditions	Typical Value	Unit
Thermal Resistance	14 Ld NSOIC Package	θ_{JA}	Junction to ambient	95	°C/W
		θ_{JC}	Junction to case	60	°C/W
Thermal Resistance	14 Ld TSSOP Package	θ_{JA}	Junction to ambient	122	°C/W
		θ_{JC}	Junction to case	57	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

2.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage [(V+) – (V-)]	V_S	1.8	5.5	V
Input Voltage Range	V_I	(V-) – 0.1	(V+) + 0.1	V
Output Voltage Range	V_O	V-	V+	V
Ambient Temperature	T_A	-40	125	°C

2.4 Electrical Specifications

V_S = (V+) – (V-) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
DC Parameters						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V	-	±0.45	±1.9	mV
		T_A = -40°C to 125°C	-	-	±2.15	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	T_A = -40°C to 125°C	-	±0.6	-	µV/°C

V_S = (V+) – (V-) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted) (Cont.)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Input Bias Current	I_B	-	-	±6.6	-	pA
Input Offset Current	I_{OS}	-	-	±0.2	-	pA
Common-Mode Input Range	V_{ICM}	V_S = 1.8V to 5.5V	(V-) - 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = 5.5V, (V-)-0.1V < V_{CM} < (V+)-1.4V T_A = -40°C to 125°C	89	109	-	dB
		V_S = 5.5V, V_{CM} = -0.1V to 5.6V T_A = -40°C to 125°C	70	92	-	dB
		V_S = 1.8V, (V-)-0.1V < V_{CM} < (V+)-1.4V T_A = -40°C to 125°C	-	97	-	dB
		V_S = 1.8V, V_{CM} = -0.1V to 1.9V T_A = -40°C to 125°C	-	83	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 1.8V - 5.5V, V_{CM} = (V-)	90	117	-	dB
Open Loop Gain	A_{OL}	V_S = 5V, V_O = 1V, R_L = 10k Ω	-	100	-	dB
Output Voltage Swing from Rails	V_{OFR+}	V_S = 5.5V	-	10	15	mV
	V_{OFR-}	V_S = 5.5V	-	10	15	mV
Sourcing Short-Circuit Current	I_{SC-}	V_S = 5V, R_L = 0Ω to V_-	-	40	-	mA
Sinking Short-Circuit Current	I_{SC+}	V_S = 5V, R_L = 0Ω to V_+	-	40	-	mA
Supply Current per Amplifier	I_Q	R_L = ∞	-	0.52	-	mA
AC Parameters						
Gain Bandwidth Product	GBW	VS = 5V, G = 1	-	10	-	MHz
Phase Margin	Φm	VS = 5V, G = 1	-	55	-	deg
Input Noise Voltage	E_n	V_S = 5V, f = 0.1-10Hz	-	4.2	-	$μV_{pp}$
Voltage Noise Density	e_n	V_S = 5V, f = 10kHz	-	15	-	nV/√Hz
Current Noise Density (at 1kHz)	i_n	V_S = 5V, f = 1kHz	-	25	-	fA/√Hz
Total Harmonic Distortion + Noise[2]	THD + N	V_S = 5.5V, V_{CM} = 2.5V, V_O = $1V_{RMS}$, G = 1, f = 1kHz	-	0.0008	-	%
Transient Response						
Slew Rate	SR	V_S = 5V, G = 1, 3V-Step	-	7.5	-	V/μs
Settling Time to 0.1% V_O	t_S	V_S = 5V, G =1, 2V-Step, C_L = 100pF	-	0.4	-	μs
Overload Recovery Time	t_{OR}	V_S = 5V, V_{IN} x G > V_S	-	0.3	-	μs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Third-order filter; bandwidth = 80kHz at –3dB.

3. Typical Performance Graphs

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, VCM = V_S/2 (unless otherwise noted)

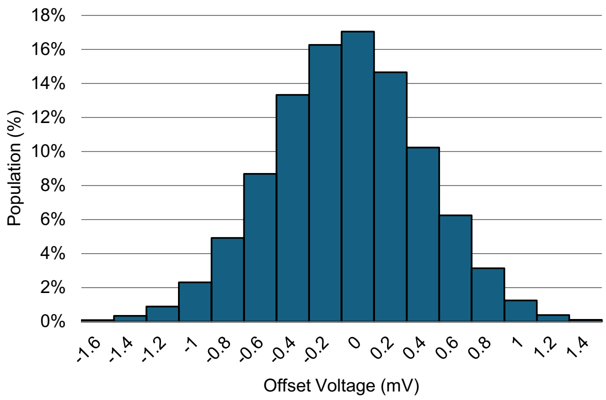


Figure 3. Offset Voltage Population % Distribution

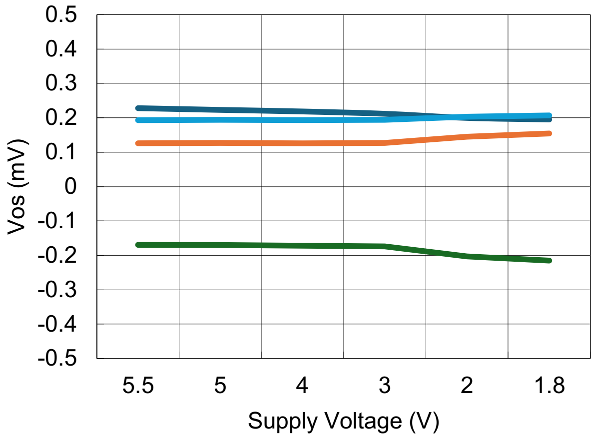


Figure 4. Offset Voltage vs Supply Voltage

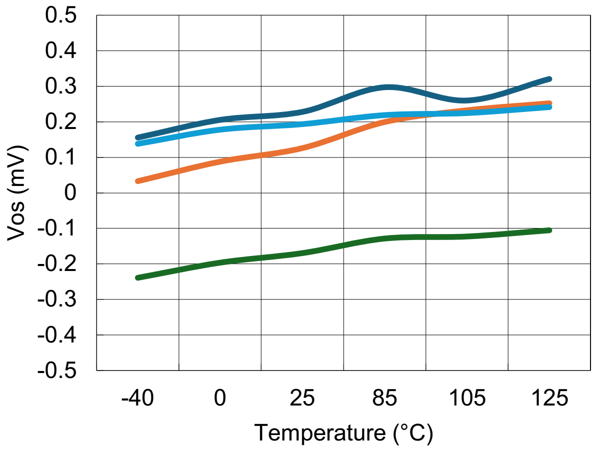


Figure 5. Offset Voltage vs Temperature

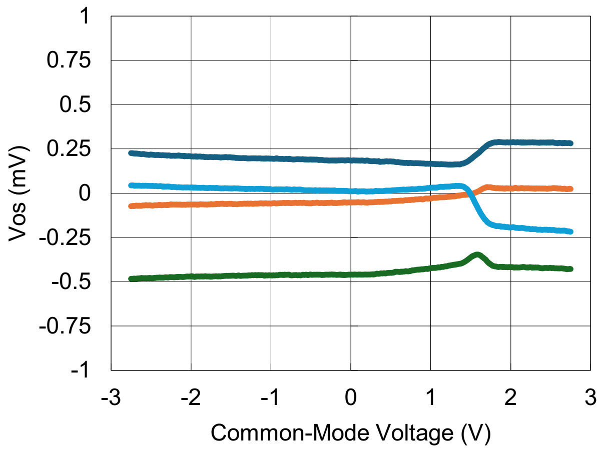


Figure 6. Offset Voltage vs Common-Mode Voltage

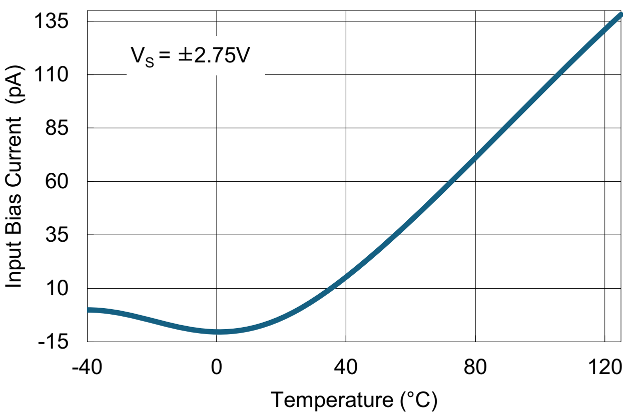


Figure 7. Input Bias Current vs Temperature

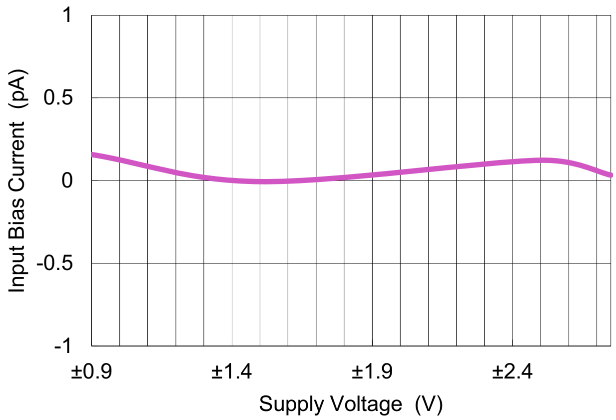


Figure 8. Input Bias Current vs Supply Voltage

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, VCM = V_S/2 (unless otherwise noted) (Cont.)

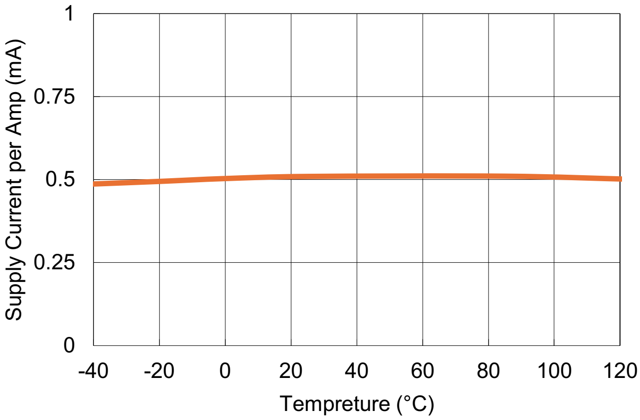


Figure 9. Supply Current vs Temperature

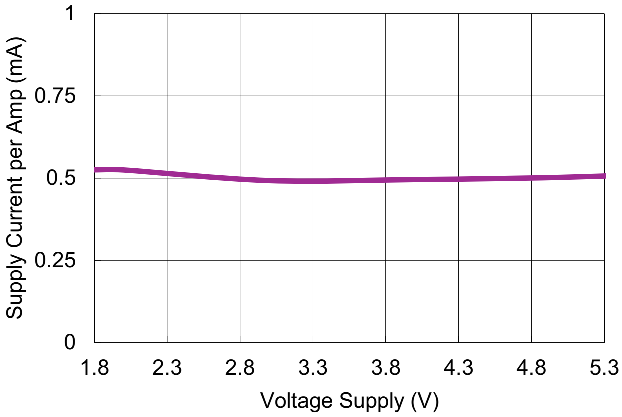


Figure 10. Supply Current vs Supply Voltage

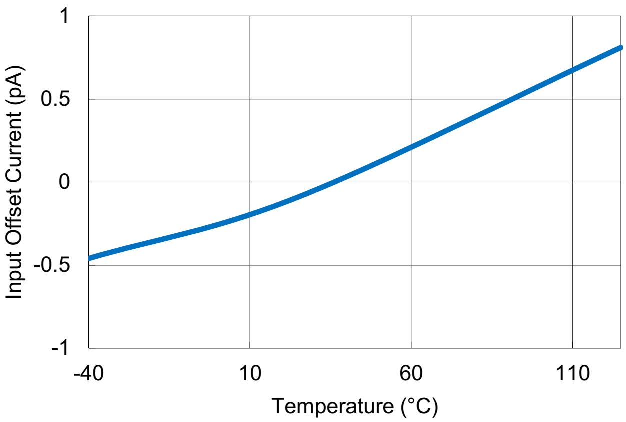


Figure 11. Input Offset Current vs Temperature

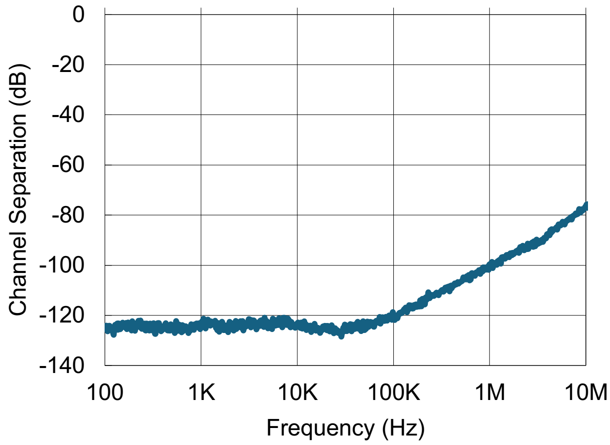


Figure 12. Channel Separation vs Frequency

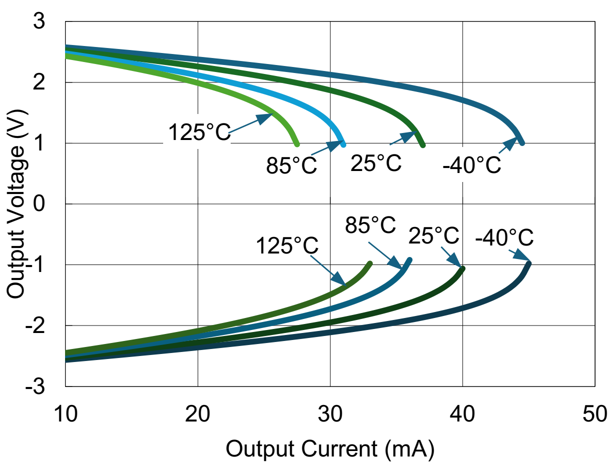


Figure 13. Output Voltage vs Output Current

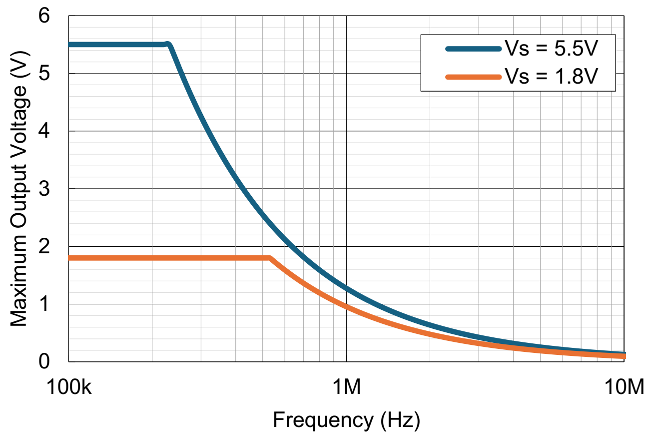


Figure 14. Maximum Output Voltage vs Frequency

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, VCM = V_S/2 (unless otherwise noted) (Cont.)

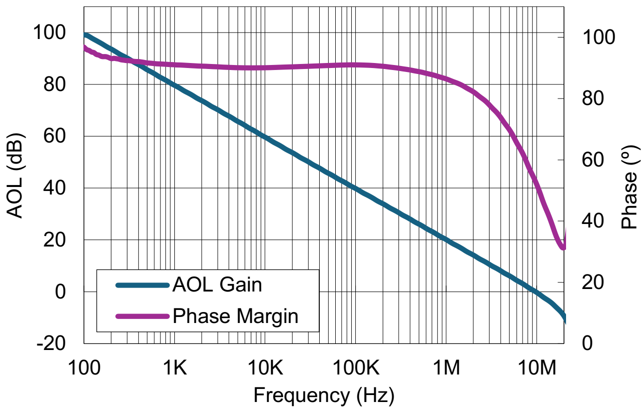


Figure 15. Open Loop Gain & Phase vs Frequency

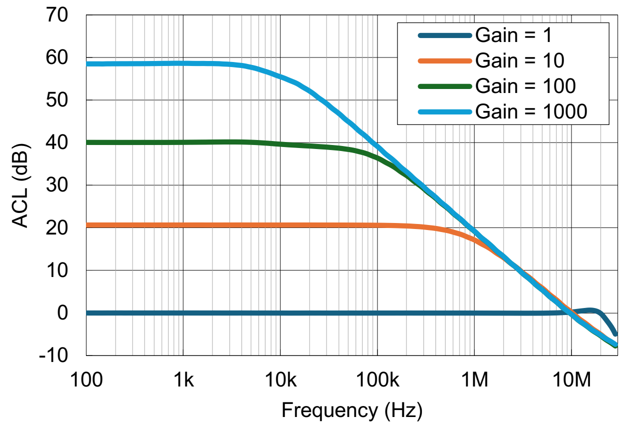


Figure 16. Closed Loop Gain vs Frequency

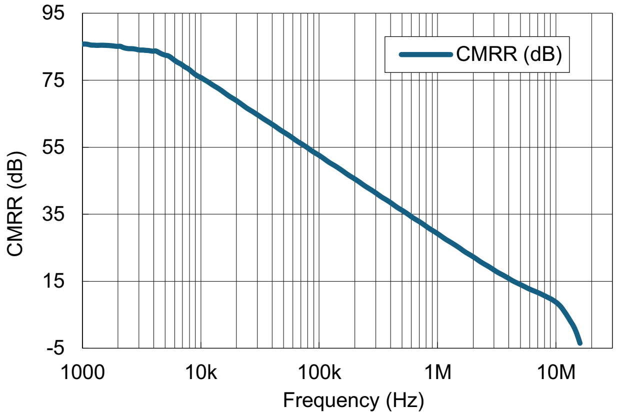


Figure 17. CMRR vs Frequency

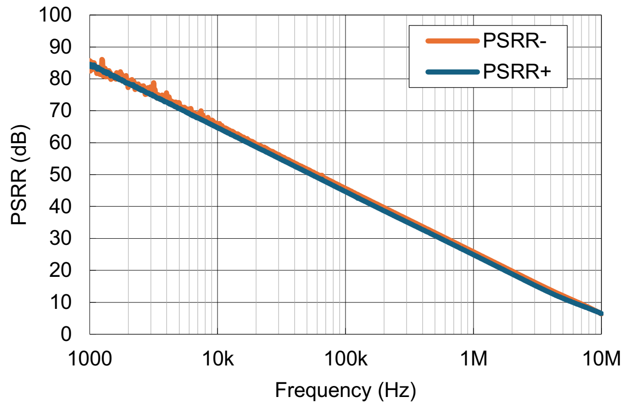


Figure 18. PSRR vs Frequency

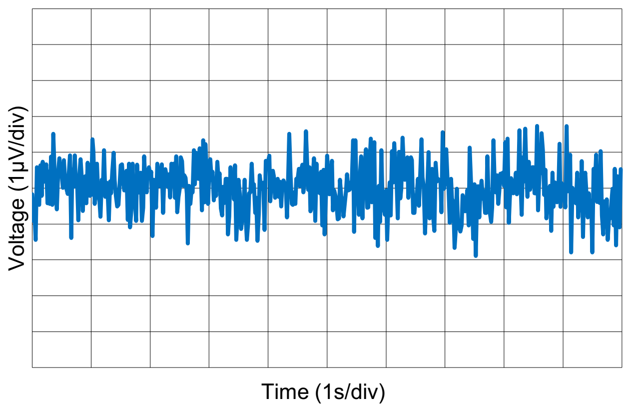


Figure 19. 0.1-Hz to 10-Hz Input Voltage Noise

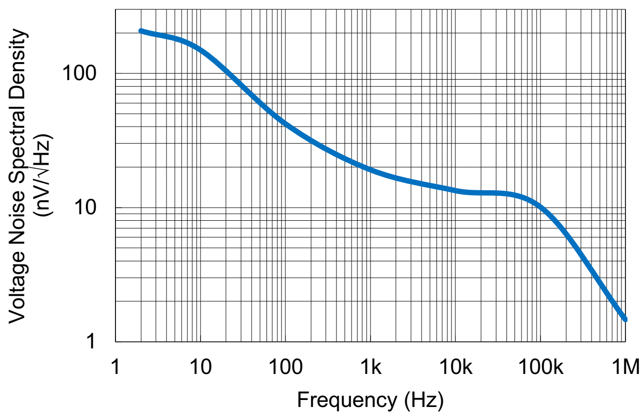


Figure 20. Voltage Noise Spectral Density vs Frequency

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, VCM = V_S/2 (unless otherwise noted) (Cont.)

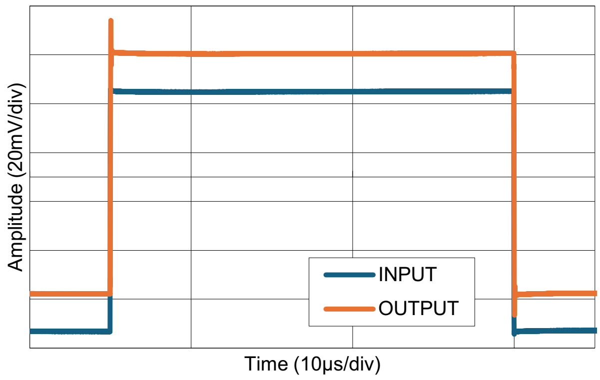


Figure 21. Small-Signal Step Response

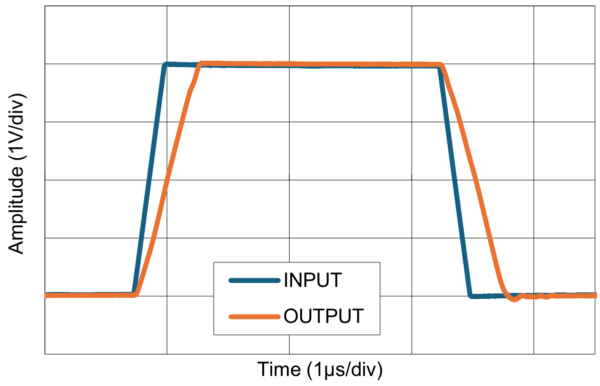


Figure 22. Large-Signal Step Response

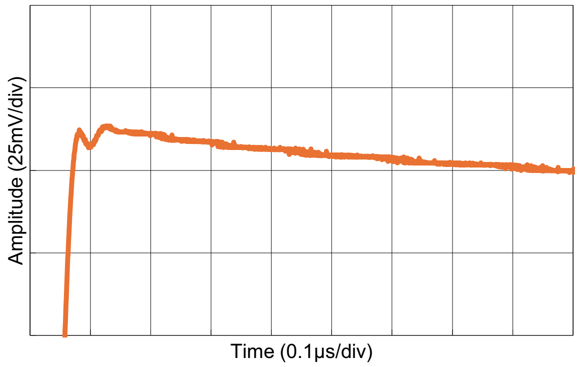


Figure 23. Large-Signal Settling Time (Positive)

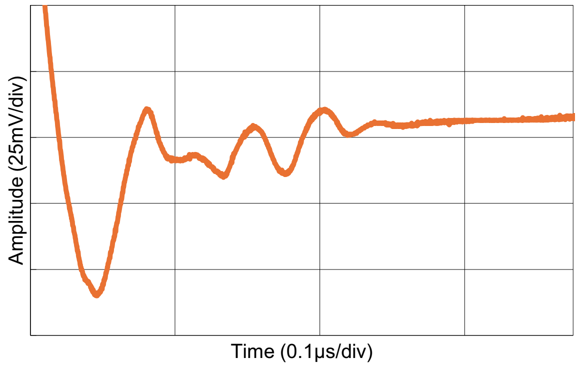


Figure 24. Large-Signal Settling Time (Negative)

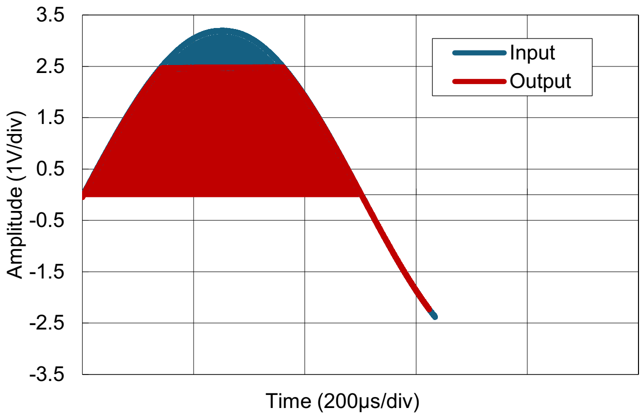


Figure 25. No Phase Reversal

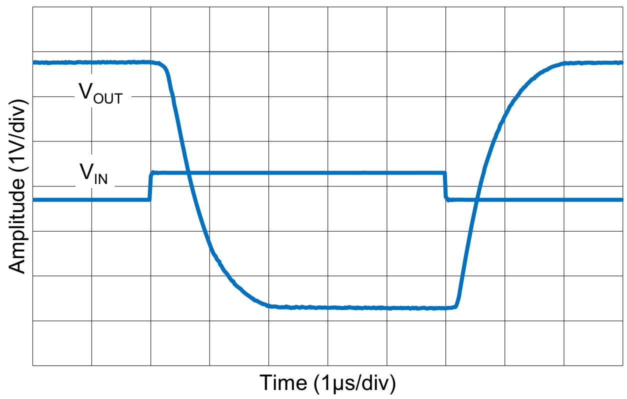


Figure 26. Overload Recovery Time

4. Detailed Description

4.1 Overview

The RRA78640 is a low-power device with rail-to-rail input and outputs. The op amp operates from supply voltages as low as 1.8V up to 5.5V. The device is unity-gain stable and designed for a wide range of general-purpose applications.

The input common-mode voltage range extends 100mV above and below the power supply voltage rails, which allows this op amp to be used in virtually any single-supply application. The rail-to-rail input and output swing capability increases the signal dynamic range and therefore, signal-to-noise ratio, a performance feature highly necessary in low-supply applications. The combination of high signal bandwidth and high slew rate enables the device to drive the sample-hold circuitry of analog-to-digital converters (ADCs). The output stage can swing to within 20mV of the supply rails with a 10kΩ load.

4.2 Functional Block Diagram

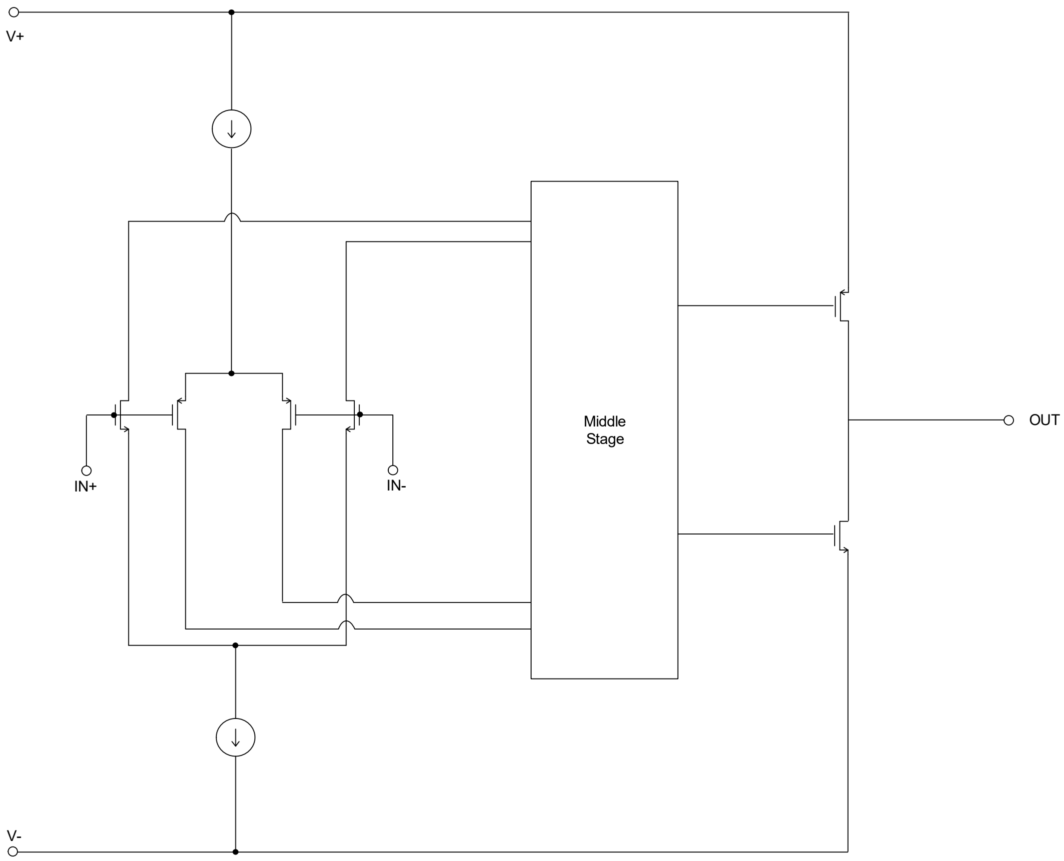


Figure 27. Block Diagram of a Single Amplifier Stage

4.3 Feature Description

4.3.1 Rail-To-Rail Input

The input common-mode voltage range of the RRA78640 extends 100mV beyond both supply rails for the full supply voltage range of 1.8V to 5.5V. This performance is accomplished with complementary input stages, consisting of an N-channel input differential pair in parallel with a P-channel differential input pair.

The N-channel pair being active for input voltages close to the positive rail, typically (V+) – 1.2 V to (V+) + 0.1V, while the P-channel pair is active for inputs from (V-) - 0.1V to about (V+) – 1.0V. Within the small transition region of 0.2V, where both pairs are active, PSRR, CMRR, V_{OS}, and THD can slightly degrade from their values outside this region.

4.3.2 Rail-To-Rail Output

The RRA78640 delivers robust output drive capability. A class AB output stage with common-source transistors provides full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 20mV of either supply rail, regardless of the applied supply voltage. Heavier load conditions, however, cause the amplifier to swing less close to the supply rails.

4.3.3 EMI Filter

The RRA78640 possesses internal electromagnetic interference (EMI) filters that reduce the effects of EMI from external sources such as wireless communications and densely populated circuit boards with a mix of analog and digital components.

4.3.4 Overload Recovery

Overload recovery is defined as the time required for the op amp output to return from a saturated state to the linear state. The op amp output saturates when the output voltage exceeds the applied supply voltage, because of a high input voltage or a high gain setting. After entering saturation, charge carriers in the output stage require time to return to the linear operating region. Only then, the device begins to slew at the specified slew rate.

Therefore, the propagation delay during an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the RRA78640 is about 500ns.

4.3.5 Input and Output ESD Protection

The RRA78640 incorporates internal ESD protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes that are connected between the input and output pins and the power-supply pins. If the input voltage is expected to exceed the specified value in the absolute maximum ratings, insert a series resistor, R_S, that limits the input current to about 10mA (Figure 28).

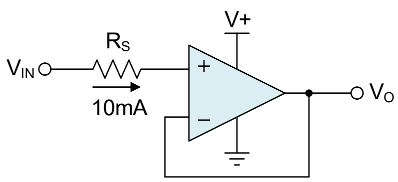


Figure 28. Input Overvoltage Protection

5. Application Information

The RRA78640 features 10MHz bandwidth and 7.5V/µs slew rate with only 520µA of supply current per channel, providing good AC-performance at very low power consumption. DC applications are well served with a low input noise voltage of 15nV/√Hz at 10kHz, low input bias current, and a typical input offset voltage of 0.45mV.

5.1 Typical Applications

5.1.1 Bidirectional Low-Side Current Sensing

Figure 29 shows RRA78640 in a bidirectional low-side current-sensing application.

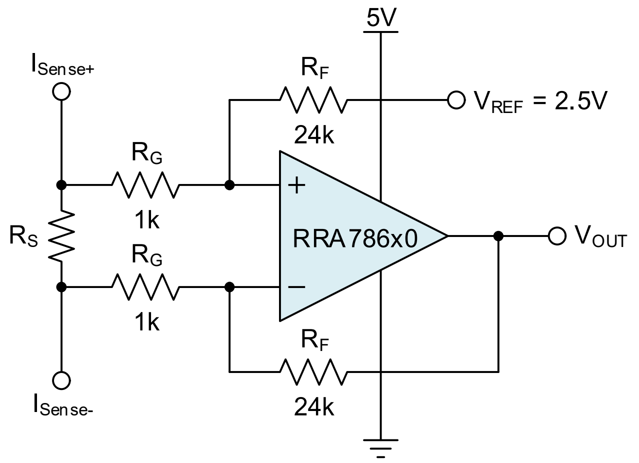


Figure 29. RRA786x0 in a Low-Side, Current-Sensing Application

5.1.2 Design Procedure

The design requirements for this design are:

- Measurable load current range: I_L = ±1A
- Measurable output voltage range: V_O = 4.9V to 0.1V
- Maximum sense resistor power dissipation: P_D = 100mW

To distinguish between positive and negative current flows or sense voltages, split the output voltage range into two equal ranges using the difference amplifier configuration in Figure 30. The output voltage is:

(EQ. 1) $$V_{OUT} = V_S \times \frac{R_F}{R_G} + V_{REF}$$

Positive sense voltages or currents produce a positive output voltage, $V_{OUT+} = V_{REF} + V_S \times R_F/R_G$, while negative sense voltages result in $V_{OUT-} = V_{REF} - V_S \times R_F/R_G$. Making V_{REF} = 2.5V and limiting the V_{OUT} limits to 100mV off the supply rails, yields a positive output range of V_{OUT+} = 2.5V to 4.9V and a negative output range of V_{OUT-} = 2.5V to 0.1V.

The maximum sense resistor value for a given power dissipation at a given load current is calculated with Equation 2.

(EQ. 2) $$R_S = \frac{P_{D\text{-}max}}{I_{L\text{-}max}^2} = \frac{0.1W}{1A^2} = 0.1\Omega$$

The maximum load current of I_L = ±1A produces a sense voltage of V_S = ±0.1V across the sense resistor, R_S, following $V_S = I_L \times R_S$. This voltage is amplified by the gain factor R_F/R_G. This gain factor is also the ratio of output voltage range to the input voltage range (Equation 2).

(EQ. 3) $$G_{max} = \frac{V_{O\text{-}max} - V_{REF}}{V_{S+}} = \frac{4.9V - 2.5V}{0.1V} = 24$$

Next, selecting the gain resistor with R_G = 10kΩ makes the feedback resistor, $R_F = R_G \times G_{max}$ = 240kΩ.

Figure 30 shows the resulting V_{OUT} versus I_{LOAD} characteristic.

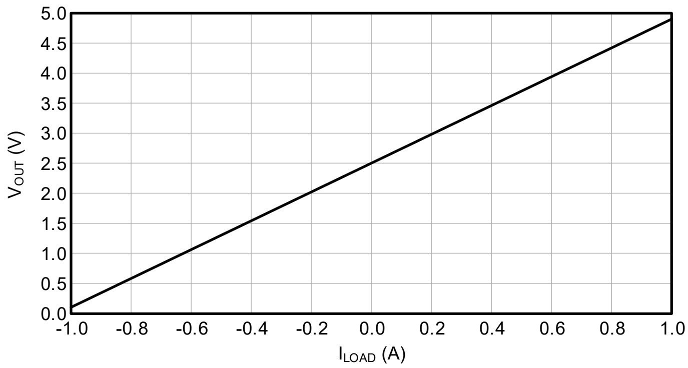


Figure 30. Bidirectional Current-Sense, V-I Characteristic

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

Part Number[1]	# Channels	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	MSL Rating[2]	Carrier Type[3]	Temp. Range
RRA78640-SLH	4	78640 SL	14 Ld NSOIC	M14.15	3	Reel, 2.5k	-40 to 125°C
RRA78640-SLA	4	78640 SL	14 Ld NSOIC	M14.15	3	Tube	-40 to 125°C
RRA78640-SKH	4	78640 SK	14 Ld TSSOP	M14.173	1	Reel, 2.5k	-40 to 125°C
RRA78640-SKA	4	78640 SK	14 Ld TSSOP	M14.173	1	Tube	-40 to 125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For more information about Moisture Sensitivity Level (MSL), see TB363.
3. See TB347 for details about reel specifications.

8. Revision History

Revision	Date	Description
1.01	Jul 10, 2025	Updated Page 1 description. Updated Figures 16 and 17. Updated Ordering information table. Added ECAD Information. Updated PODs to the latest template.
1.00	Jun 17, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRA78640-SLH	14	NSOIC	M14.15
RRA78640-SLA	14	NSOIC	M14.15
RRA78640-SKH	14	TSSOP	M14.173
RRA78640-SKA	14	TSSOP	M14.173

A.2 Symbol Pin Information

A.2.1 14-NSOIC/TSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V+	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	OUT3	Output	-
9	IN3-	Input	-
10	IN3+	Input	-
11	V-	Power	-
12	IN4+	Input	-
13	IN4-	Input	-
14	OUT4	Output	-

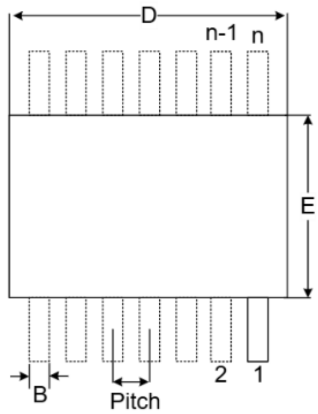
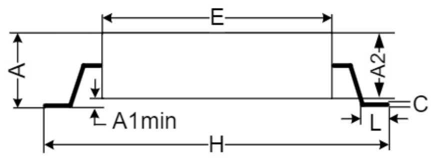
A.3 Symbol Parameters

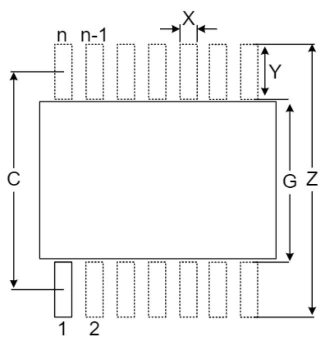
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Number of Channels	Slew Rate	Operating Supply Current	Input Offset Voltage (V_{OS})
RRA78640-SLH	Commercial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	4	7.5 V/µs	520 µA	±0.45 mV
RRA78640-SLA	Commercial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	4	7.5 V/µs	520 µA	±0.45 mV
RRA78640-SKH	Commercial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	4	7.5 V/µs	520 µA	±0.45 mV
RRA78640-SKA	Commercial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	4	7.5 V/µs	520 µA	±0.45 mV

A.4 Footprint Design Information

A.4.1 14-NSOIC

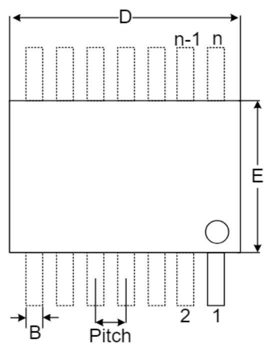
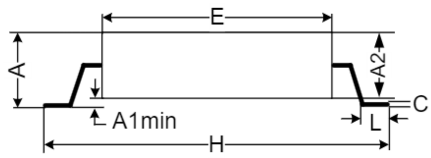
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOIC	M14.15	14

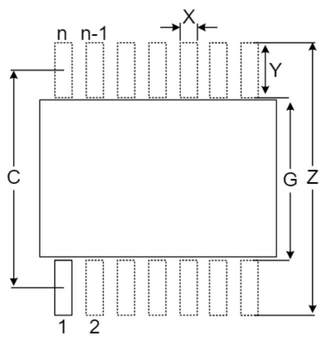
Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	5.95	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.05	
Minimum body span (pin1 side)	Dmin	8.55	
Maximum body span (pin1 side)	Dmax	8.75	
Minimum body span	Emin	3.80	
Maximum body span	Emax	4.00	
Minimum Lead Width	Bmin	0.31	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	 Side View
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	1.27	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	6.60	 PCB Top View
Distance between left pad heel to right pad heel.	G	4.20	
Row spacing. Distance between pad centers	C	5.40	
Pad Width	X	0.41	
Pad Length	Y	1.20	

A.4.2 14-TSSOP

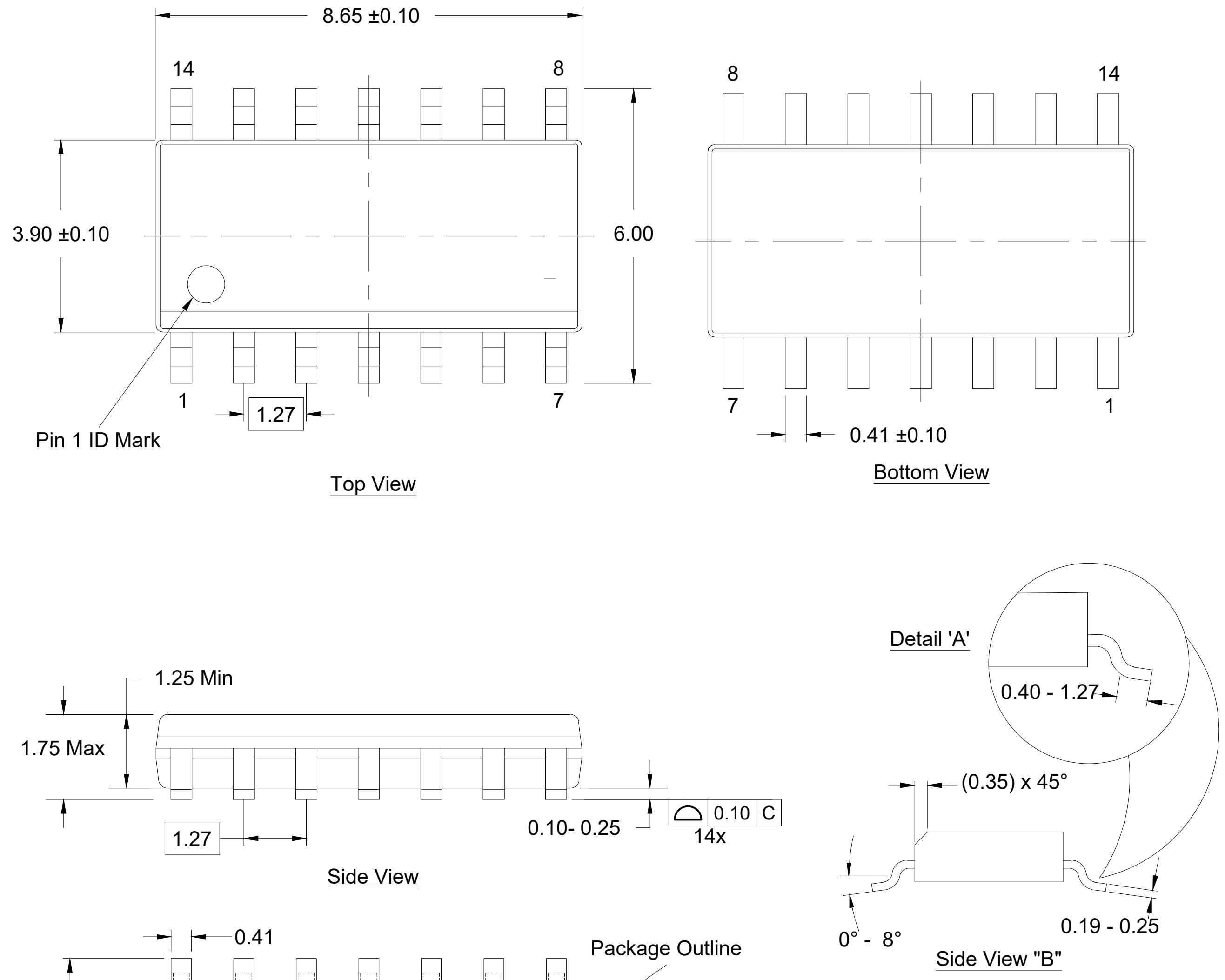
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M14.173	14

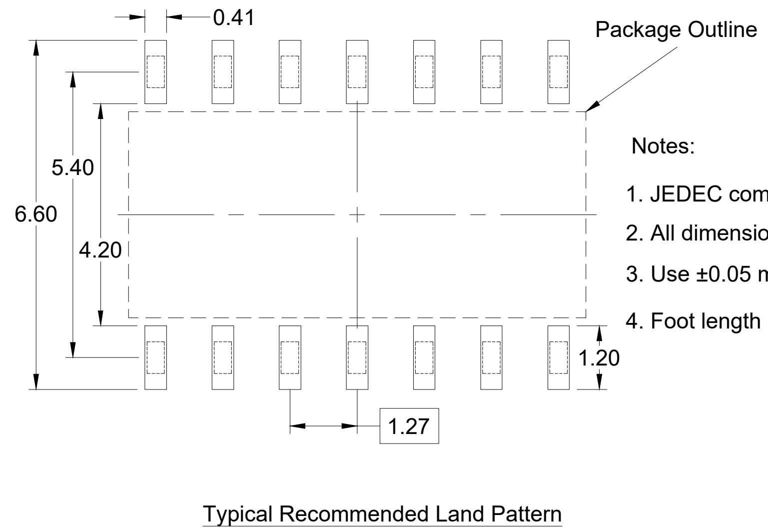
Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	6.30	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.50	
Minimum body span (horizontal side)	Dmin	4.90	
Maximum body span (horizontal side)	Dmax	5.10	
Minimum body span (vertical side)	Emin	4.30	
Maximum body span (vertical side)	Emax	4.50	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	 Side View
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	0.65	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.0	 PCB Top View
Distance between left pad heel to right pad heel.	G	4.60	
Row spacing. Distance between pad centers	C	5.80	
Pad Width	X	0.25	
Pad Length	Y	1.20	

Package Outline Drawing

M14.15
GS0014AB
14-SOICN 8.65 x 3.90 x 1.75 mm Body, 1.27 mm Pitch
Rev03, Jun 26, 2025



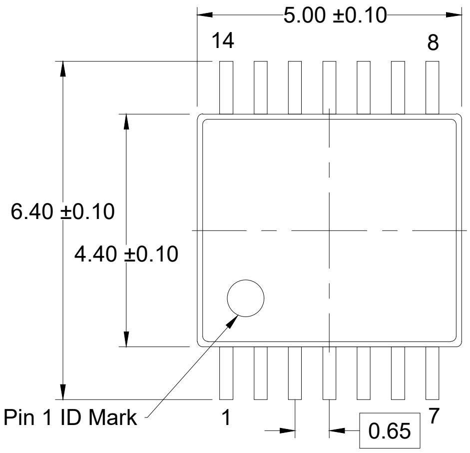


Notes:

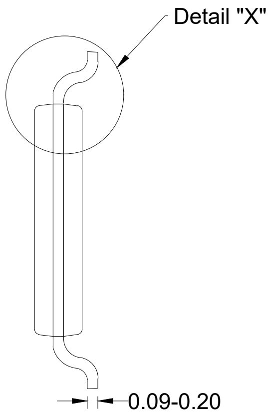
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

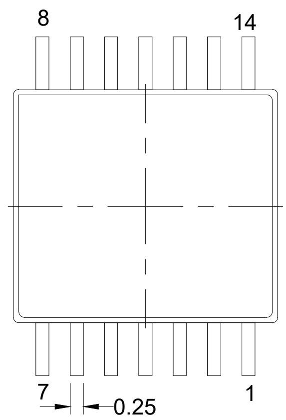
M14.173
HV0014AA
14-Lead Thin Shrink Small Outline package (TSSOP) 5.00 x 4.40 x 1.20 mm Body, 0.65 mm Pitch
Rev04, Jun 26, 2025



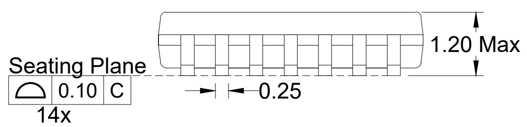
Top View



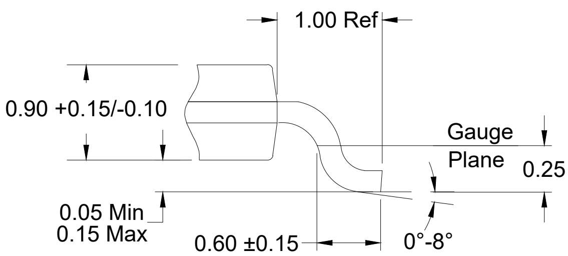
Side View



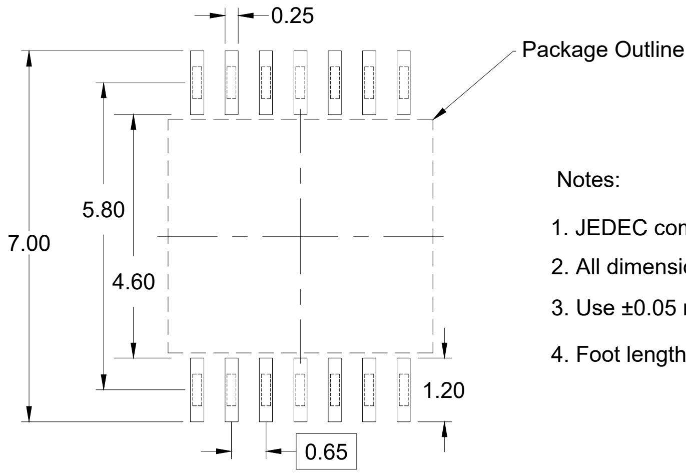
Bottom View



Side View



Detail "X"



Typical Recommended Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

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