RRA79041, RRA79042

Ultra-Low Power, RRIO, Operational Amplifiers

Description

The RRA7904x family (RRA79041, RRA79042) of ultra-low voltage operational amplifiers deliver exceptional performance and efficiency for a variety of demanding applications. Available in a single (RRA79041) and dual (RRA79042) configurations, these op-amps operate seamlessly within a wide voltage range from 1.2V to 5.5V, featuring rail-to-rail input and output capabilities.

Engineered specifically for power-sensitive applications, the RRA7904x series significantly reduces power consumption through a very low quiescent current of just 10µA (typical). Its ability to function reliably at supply voltages as low as 1.2V positions it as one of the industry's leading solutions for power-sensitive applications.

All devices operate across the temperature range of -40°C to +125°C and are available in a wide variety of packages.

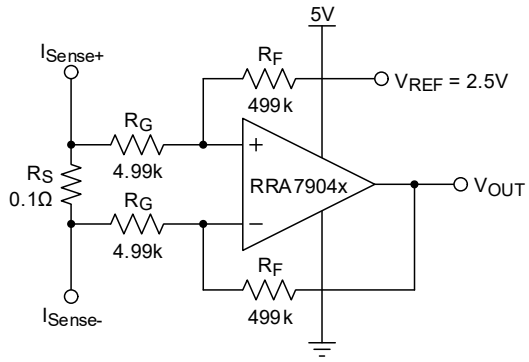
Part	Package	Body Size (nom)
RRA79041	SC70-5	1.25mm×2.00mm
	SOT-23-5	1.60mm×2.90mm
RRA79042	MSOP-8	3.00mm×3.00mm
	SOICN-8	3.90mm×4.90mm
	DFN-8	2.00mm×2.00mm

Features

- Wide supply voltage range: Down to 1.2V
- Ultra-low input bias current: 1pA typical
- Low quiescent current: 10µA/Ch
- Low integrated noise: 5.5µV_{P-P} (0.1Hz to 10Hz)
- Rail-to-rail input/output capability
- Gain bandwidth product: 350kHz
- Low input offset voltage: ±0.5mV
- Integrated RFI and EMI input filtering
- Unity-gain stable with no phase reversal
- Operating temperature range: -40°C to 125°C

Applications

- Smart and connected IoT devices
- Advanced wearable technologies
- Portable and personal electronics
- Building automation
- Environmental sensors



Bidirectional Current-Sense Amplifier

Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Functional Block Diagram

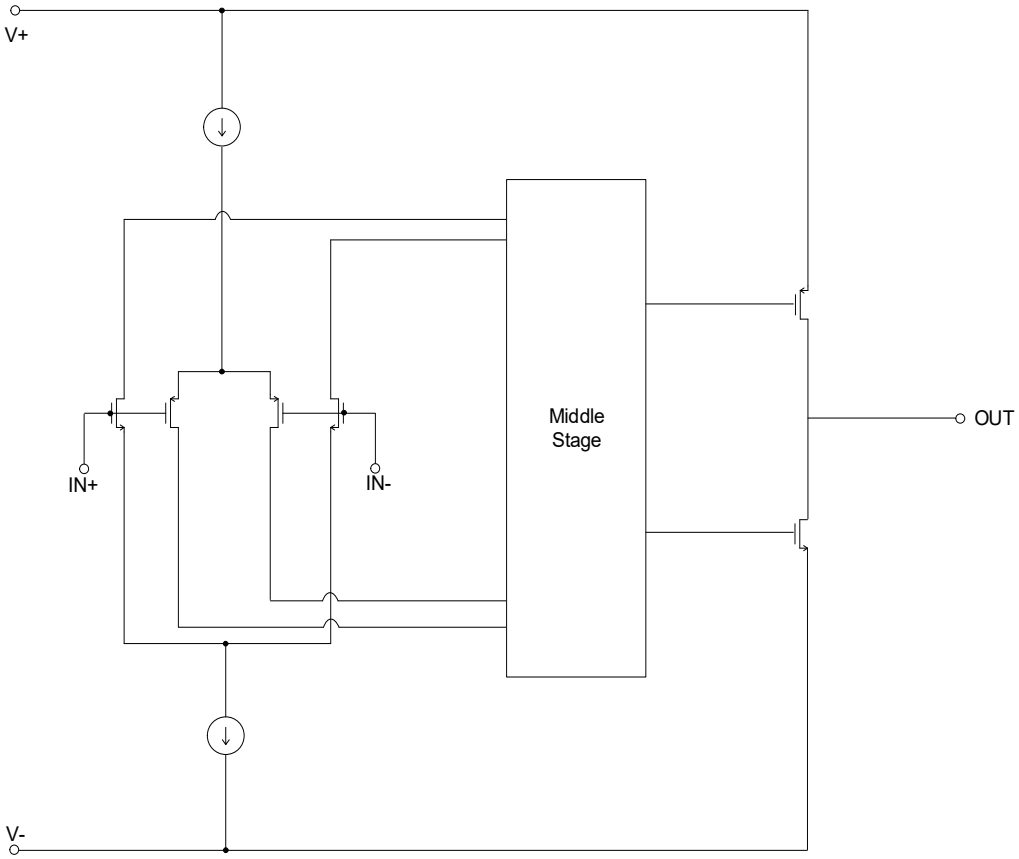


Figure 2. Block Diagram of a Single Amplifier Stage

2. Pin Information

2.1 5-Pin SC70

2.1.1 Pin Assignments

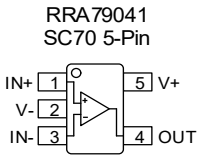


Figure 3. Pin Assignments – Top View

2.1.2 Pin Descriptions

Pin Number	Pin Name	Function
1	IN+	Non-inverting Signal Input
2	V-	Negative Supply Voltage
3	IN-	Inverting Signal Input
4	OUT	Signal Output
5	V+	Positive Supply Voltage

2.2 5-Pin SOT23

2.2.1 Pin Assignments

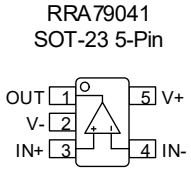


Figure 4. Pin Assignments – Top View

2.2.2 Pin Descriptions

Pin Number	Pin Name	Function
1	OUT	Signal Output
2	V-	Negative Supply Voltage
3	IN+	Non-inverting Signal Input
4	IN-	Inverting Signal Input
5	V+	Positive Supply Voltage

2.3 8-Pin DFN, MSOP, SOICN

2.3.1 Pin Assignments

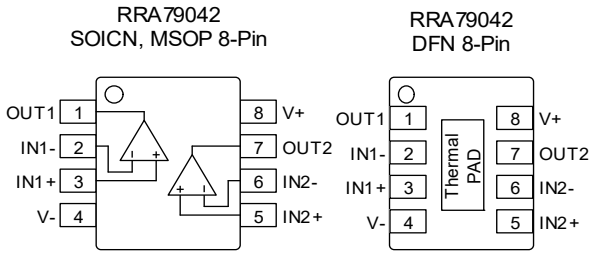


Figure 5. Pin Assignments – Top View

2.3.2 Pin Descriptions

Pin Number	Pin Name	Function
3	IN1+	Non-inverting Signal Input
5	IN2+	
2	IN1-	Inverting Signal Input
6	IN2-	
1	OUT1	Signal Output
7	OUT2	
8	V+	Positive Supply Voltage
4	V-	Negative Supply Voltage
-	EPAD	Connect the EPAD to ground for temperature dissipation. (DFN Package Only)

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by the warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, V+ to V-	-	6.0	V
Input Voltage, IN to GND	(V-) – 0.5	(V+) + 0.5	V
Input Voltage, IN+ to IN-	-	6.0	V
Input Current	-	±10	mA
Output Short-Circuit	Continuous		mA
Ambient Temperature, T_A	-55	150	°C
Junction Temperature, T_J	-	150	°C
Storage Temperature, T_{stg}	-65	150	°C
Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	-	6	kV
Charged-Device Model (CDM), per JEDEC specification JESD22-C101	-	1.5	kV
Latch-Up (Tested per JESD78B), T_A = 125°C	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage [(V+) – (V-)]	V_S	1.2	5.5	V
Input Voltage Range	V_I	(V-)	(V+)	V
Ambient Temperature	T_A	-40	125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	5 Ld SOT-23 Package	θ_{JA}[1]	Junction to ambient	202	°C/W
		θ_{JC}[2]	Junction to case	152	°C/W
Thermal Resistance	5 Ld SC-70 Package	θ_{JA}[1]	Junction to ambient	235	°C/W
		θ_{JC}[2]	Junction to case	150	°C/W
Thermal Resistance	8 Ld SOICN Package	θ_{JA}[1]	Junction to ambient	137	°C/W
		θ_{JC}[2]	Junction to case	80	°C/W
Thermal Resistance	8 Ld DFN 2x2 Package	θ_{JA}[3]	Junction to ambient	84	°C/W
		θ_{JC}[4]	Junction to case	24	°C/W
Thermal Resistance	8 Ld MSOP Package	θ_{JA}[1]	Junction to ambient	167	°C/W
		θ_{JC}[2]	Junction to case	91	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature is measured at the package top center.
3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
4. For θ_{JC}, the case temperature is measured at the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

V_S = (V+) – (V-) = 1.2V to 5.5V at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted).

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
DC Parameters						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V	-	±0.5	±1.9	mV
		T_A = -40°C to 125°C	-	-	±2.15	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	T_A = -40°C to 125°C	-	±0.8	-	µV/°C
Input Bias Current	I_B		-	±1	-	pA
Input Offset Current	I_{OS}		-	±0.5	-	pA
Common-Mode Input Range	V_{ICM}	V_S = 1.2V to 5.5V	V-	-	V+	V
Common-Mode Rejection Ratio	CMRR	V_S = 1.2V, T_A = -40°C to 125°C, (V-) < V_{CM} < (V+) – 0.7V	60	77	-	dB
		V_S = 5.5V, T_A = -40°C to 125°C, (V-) < V_{CM} < (V+) – 0.7V	75	89	-	dB
		V_S = 1.2V, T_A = -40°C to 125°C, (V-) < V_{CM} < (V+)	-	60	-	dB
		V_S = 5.5V, T_A = -40°C to 125°C, (V-) < V_{CM} < (V+)	57	72	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 1.2V to 5.5V, T_A = -40°C to 125°C, V_{CM} = V-	80	94	-	dB
Open Loop Gain	A_{OL}	V_S = 1.2V, T_A = -40°C to 125°C (V-) + 0.2V < V_O < (V+) – 0.2V, R_L = 10kΩ	-	99	-	dB
		V_S = 5.5V, T_A = -40°C to 125°C (V-) + 0.2V < V_O < (V+) – 0.2V, R_L = 10kΩ	-	125	-	dB
		V_S = 1.2V, T_A = -40°C to 125°C (V-) + 0.2V < V_O < (V+) – 0.2V, R_L = 100kΩ	-	105	-	dB
		V_S = 5.5V, T_A = -40°C to 125°C (V-) + 0.2V < V_O < (V+) – 0.2V, R_L = 100kΩ	107	130	-	dB
Output Voltage Swing from Rails	V_{OFR+}	R_L = 10kΩ	-	10	21	mV
	V_{OFR-}		-	10	21	mV
Sourcing Short Circuit Current	I_{SC+}	V_{OUT} connected to V-	-	40		mA
Sinking Short Circuit Current	I_{SC-}	V_{OUT} connected to V+	-	40		mA
Supply Current per Amplifier	I_Q	R_L = ∞	-	10	13	µA
AC Parameters						
Input Noise Voltage	E_n	f = 0.1 to 10Hz	-	5.5	-	$µV_{P-P}$
Voltage Noise Density	e_n	f = 10kHz	-	70	-	nV/√Hz
Current Noise Density	i_n	f = 1Hz	-	10	-	fA/√Hz
Gain Bandwidth	GBW	G = 1, R_L = 1MΩ	-	350	-	kHz
Phase Margin	$Φ_m$	G = +1, R_L = 10kΩ connected to V_S/2, C_L = 10pF	-	68	-	deg
Positive Slew Rate	SR+	V_S = 5.5V, C_L = 10pF, G = ±1	-	0.2	-	V/µs
Negative Slew Rate	SR-	V_S = 5.5V, C_L = 10pF, G = ±1	-	0.2	-	V/µs
Total Harmonic Distortion + Noise	THD+N	V_S = 5.5V, V_{CM} = 2.75V, V_O = $1V_{RMS}$, G=±1, f=1kHz, R_L = 100kΩ	-	0.013	-	%
Settling Time to 0.1% V_O	t_S	V_S = 5.5V, G =1, 2V-Step, C_L = 1pF	-	14	-	µs
Overload Recovery Time	T_{OR}	V_{IN} x G > V_S	-	8	-	µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Performance Curves

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted).

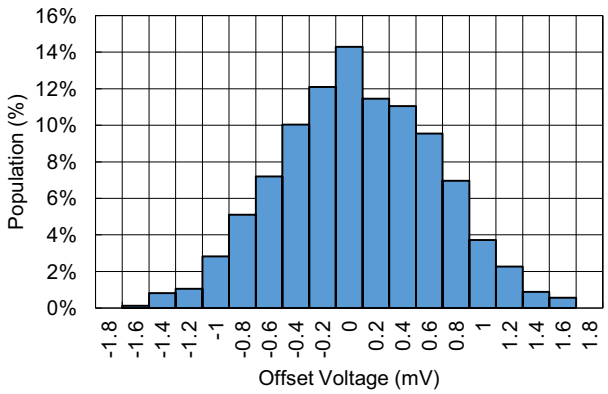


Figure 6. Offset Voltage Distribution

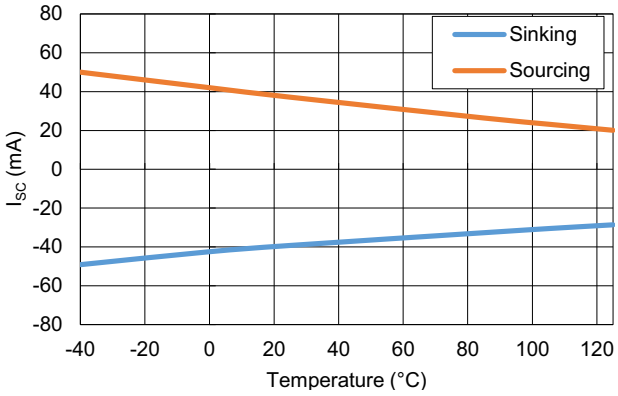


Figure 7. Short-Circuit Current vs Temperature

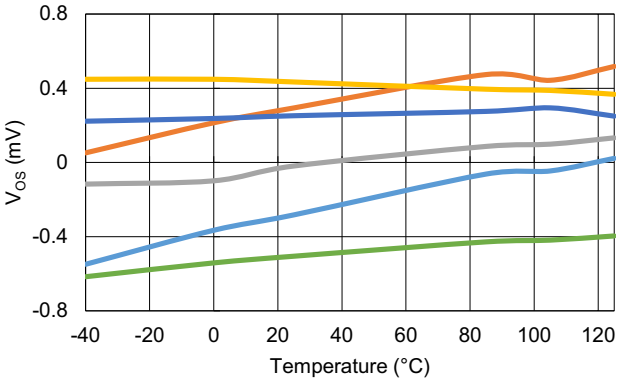


Figure 8. Offset Voltage vs Temperature
V_S = 5.5V, V_{CM} = V-

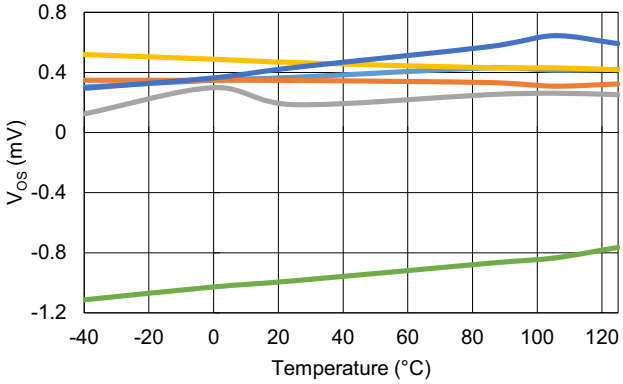


Figure 9. Offset Voltage vs Temperature
V_S = 5.5V, V_{CM} = V+

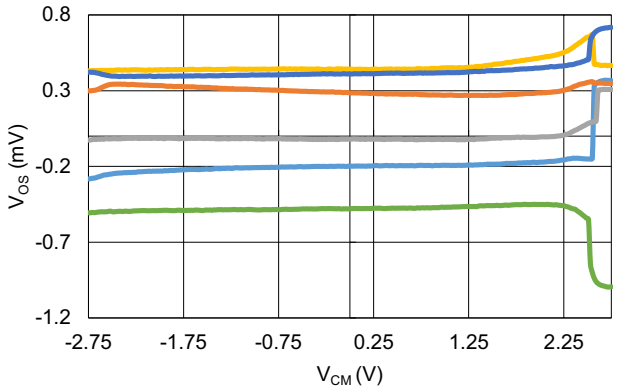


Figure 10. Offset Voltage vs Common-Mode Voltage

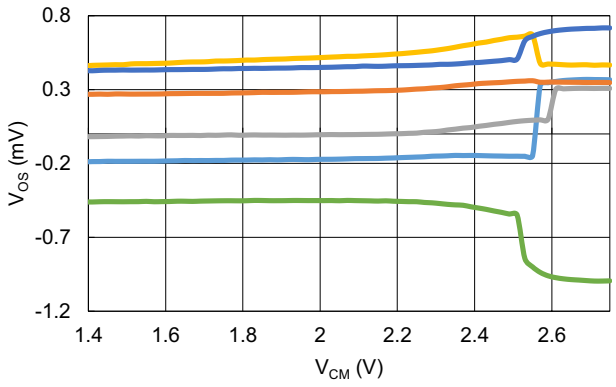


Figure 11. Offset Voltage vs Common-Mode Voltage
V_{CM} > (V+) - 1.4V

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted). (Cont.)

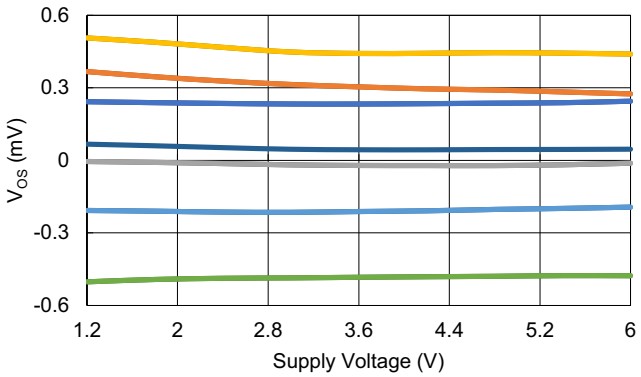


Figure 12. Offset Voltage vs Supply Voltage
V_{CM} = (V-)

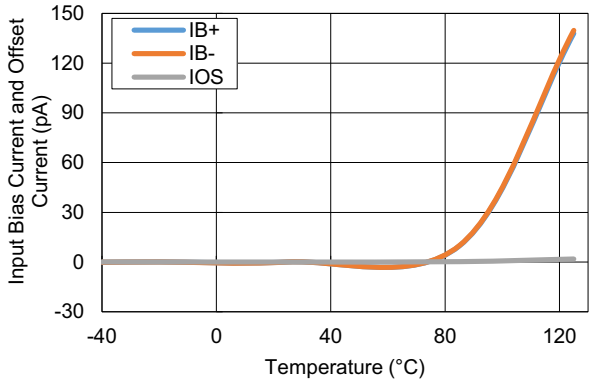


Figure 13. Input Bias and Offset Current vs Temperature

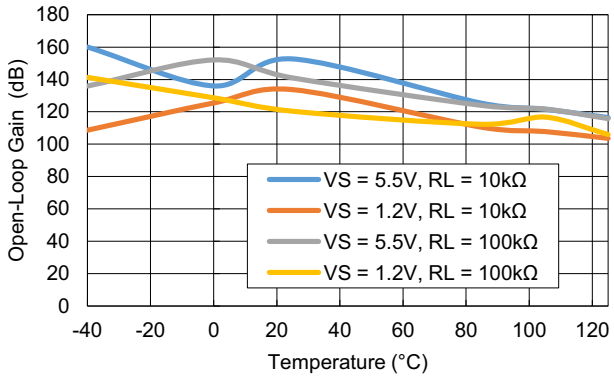


Figure 14. Open-Loop Gain vs Temperature

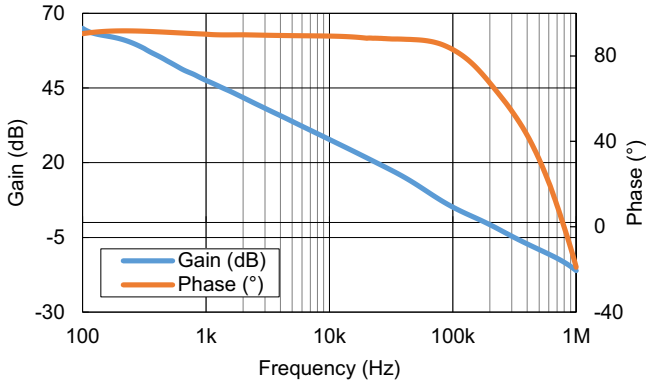


Figure 15. Open-Loop Gain and Phase vs Frequency

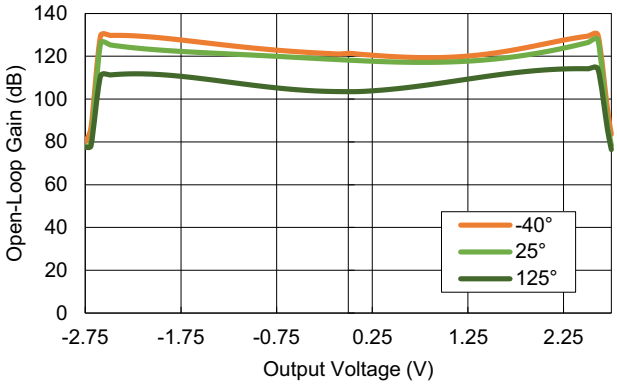


Figure 16. Open-Loop Gain vs Output Voltage

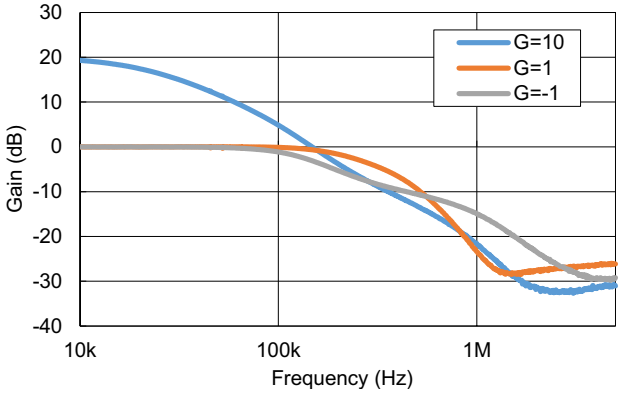


Figure 17. Closed-Loop Gain vs Frequency

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted). (Cont.)

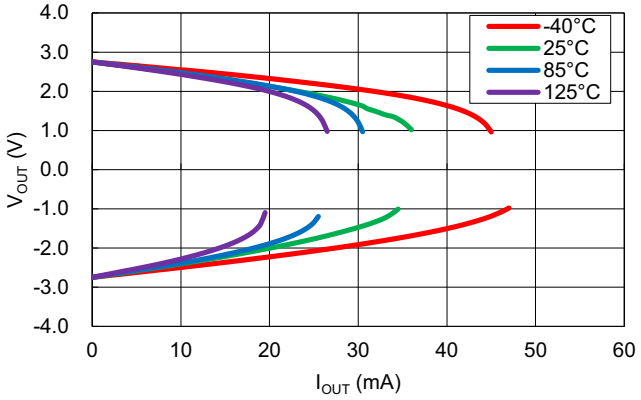


Figure 18. Output Voltage vs Output Current
V+ = 2.75V, V- = -2.75V

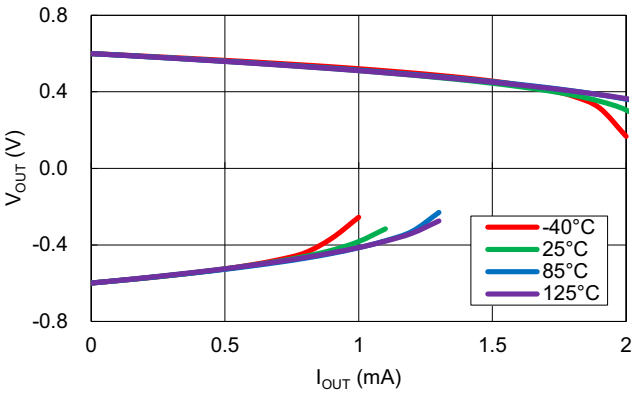


Figure 19. Output Voltage vs Output Current
V+ = 0.6V, V- = -0.6V

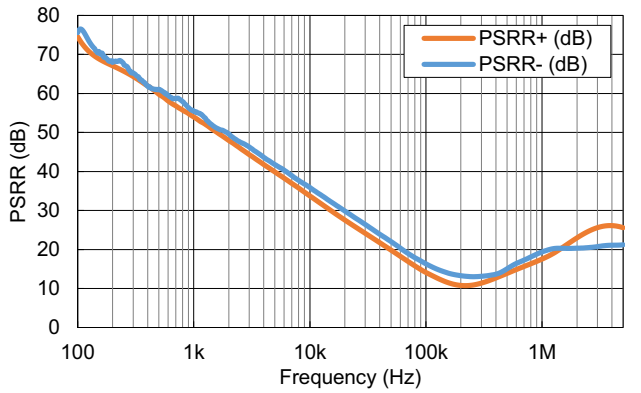


Figure 20. PSRR vs Frequency

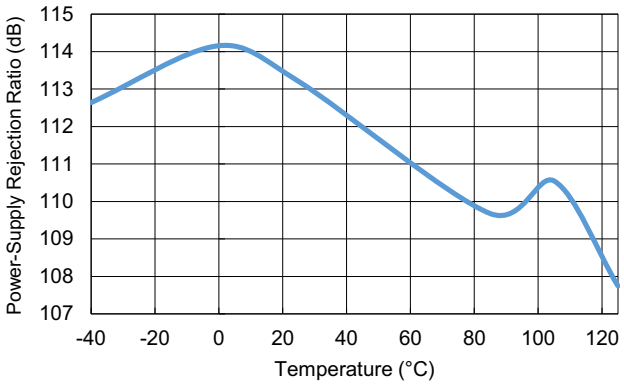


Figure 21. DC PSRR vs Temperature

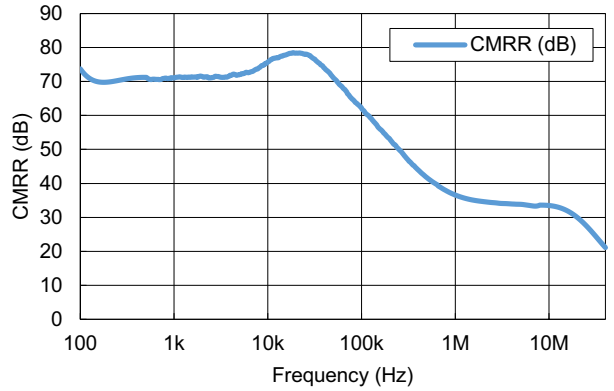


Figure 22. CMRR vs Frequency

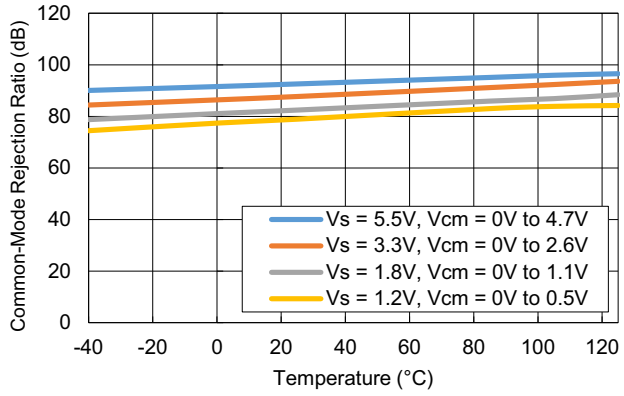


Figure 23. DC CMRR vs Temperature

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted). (Cont.)

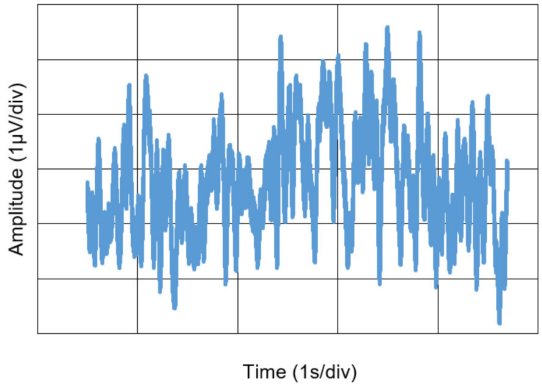


Figure 24. 0.1Hz to 10Hz Voltage Noise in Time Domain

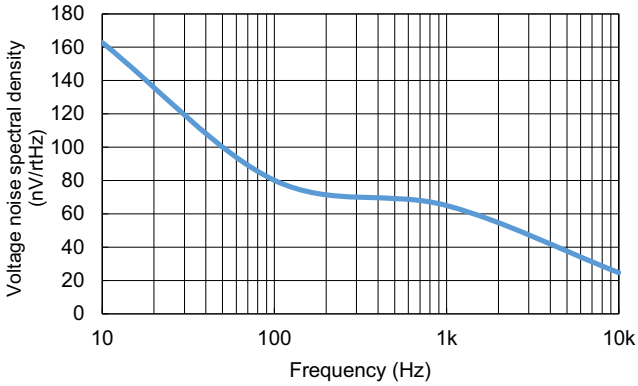


Figure 25. Voltage Noise Spectral Density

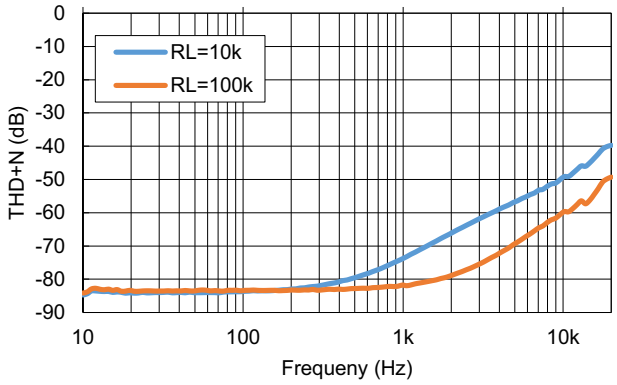


Figure 26. THD+N vs Frequency
V_S = 5.5V, V_{CM} = 2.5V, G = 1, BW = 80kHz,
V_{OUT} = 0.5VRMS

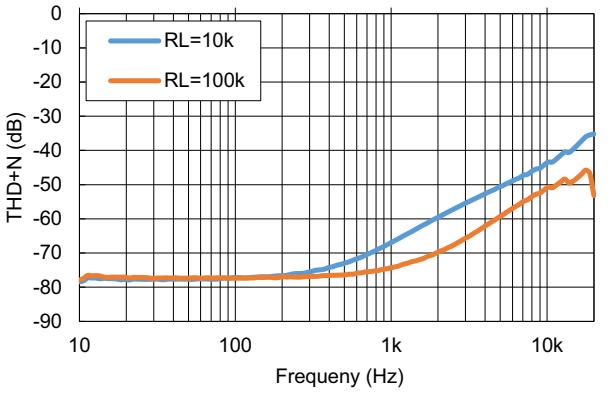


Figure 27. THD+N vs Frequency
V_S = 5.5V, V_{CM} = 2.5V, G = -1, BW = 80kHz,
V_{OUT} = 0.5VRMS

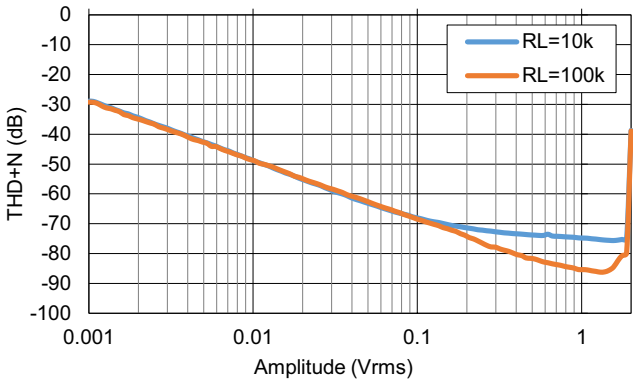


Figure 28. THD+N vs Amplitude
V_S = 5.5V, V_{CM} = 2.5V, f = 1kHz, G = 1, BW = 80kHz

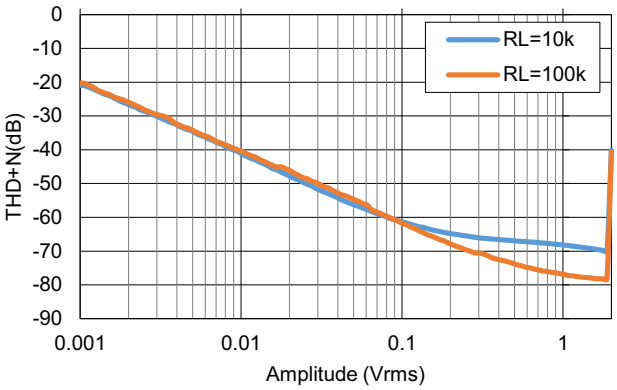


Figure 29. THD+N vs Amplitude
V_S = 5.5V, V_{CM} = 2.5V, f = 1kHz, G = -1, BW = 80kHz

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted). (Cont.)

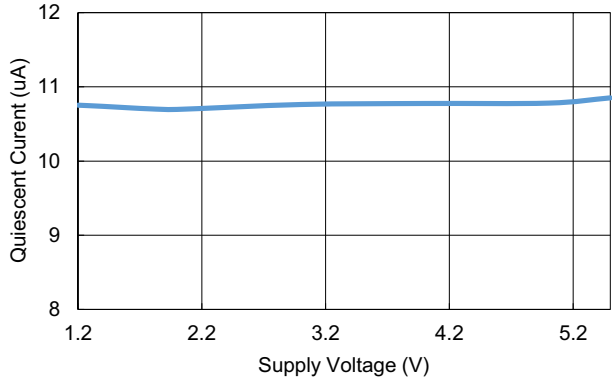


Figure 30. Quiescent Current vs Supply Voltage

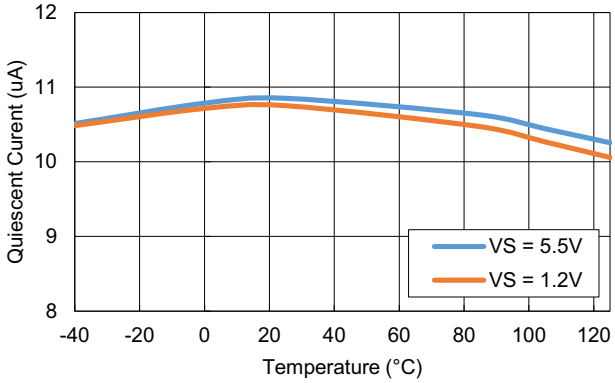


Figure 31. Quiescent Current vs Temperature

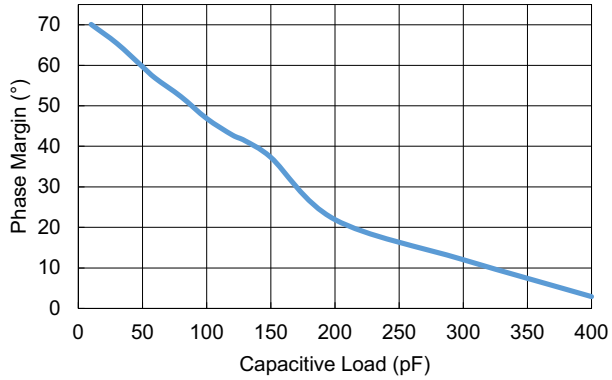


Figure 32. Phase Margin vs Capacitive Load

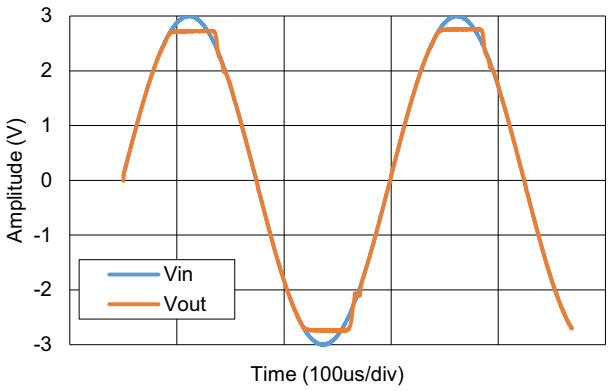


Figure 33. No Phase Reversal
G = 1, V_{IN} = 6 V_{P-P}

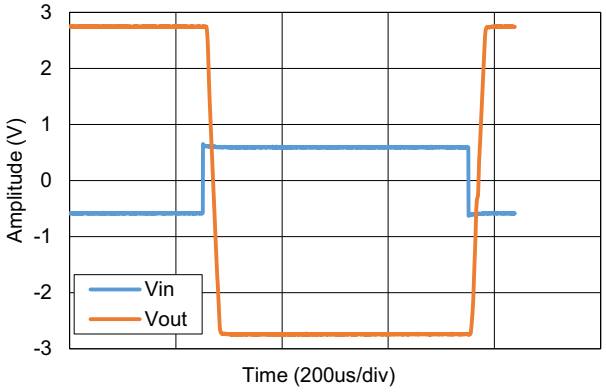


Figure 34. Overload Recovery
G = -10, V_{IN} = 600mV_{P-P}

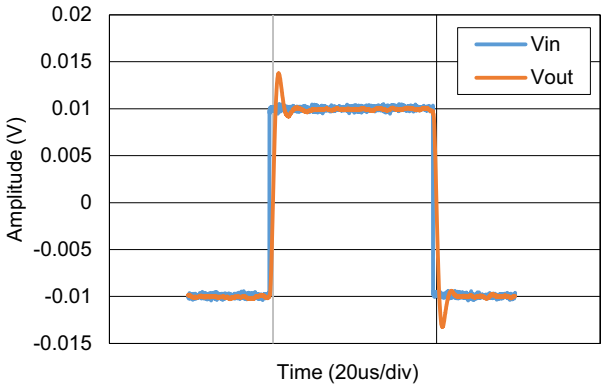


Figure 35. Small Signal Step Response
G = 1, V_{IN} = 20mV_{P-P}, C_L = 10pF

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted). (Cont.)

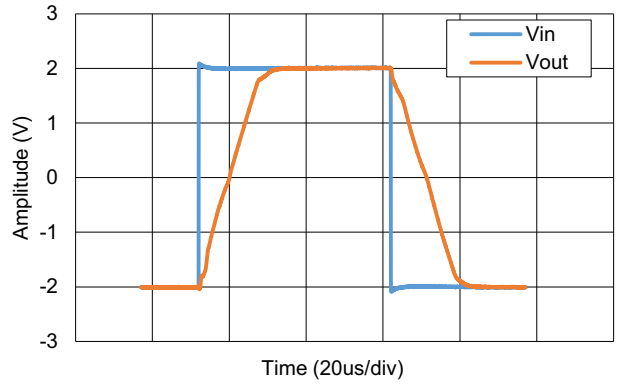


Figure 36. Large Signal Step Response
G = 1, V_{IN} = 4V_{P-P}, C_L = 10pF

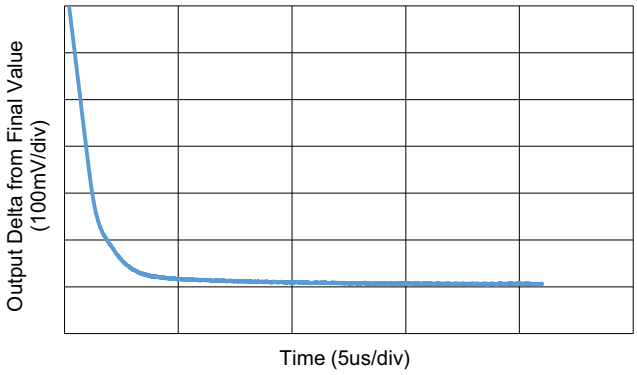


Figure 37. Large Signal Settling Time (Negative)
G = 1, V_{IN} = 4V_{P-P}, C_L = 10pF

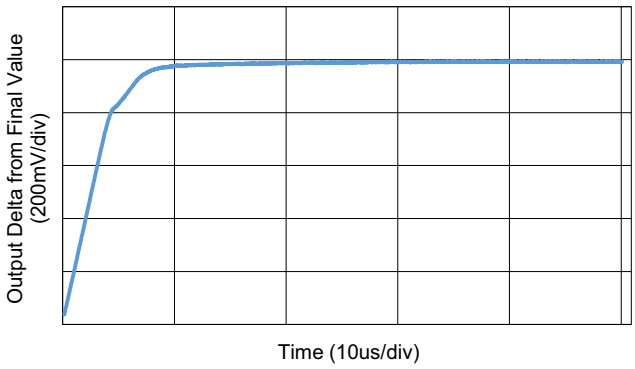


Figure 38. Large Signal Settling-Time (Positive)
G = 1, V_{IN} = 4V_{P-P}, C_L = 10pF

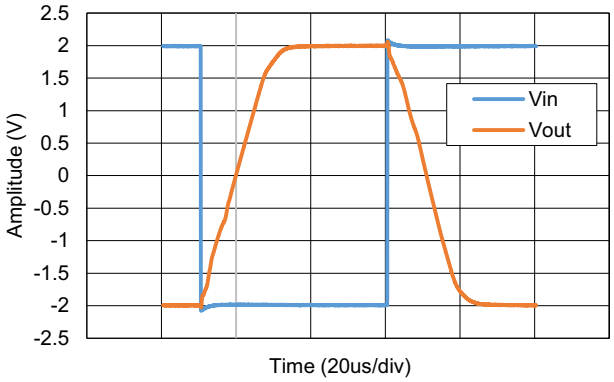


Figure 39. Large Signal Step Response
G = -1, V_{IN} = 4V_{P-P}, C_L = 10pF

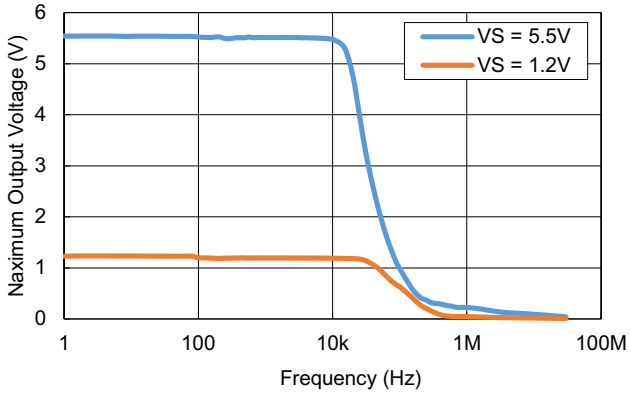


Figure 40. Maximum Output Voltage vs Frequency

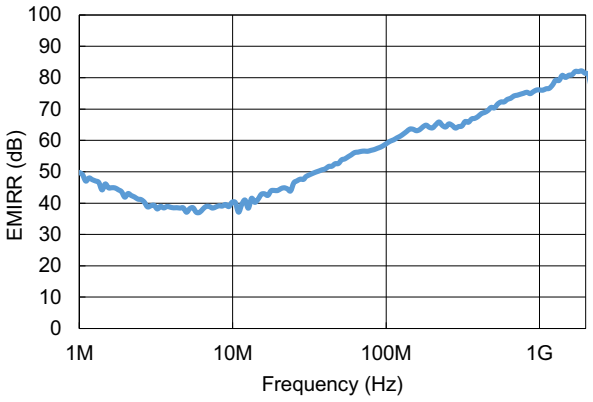


Figure 41. Electromagnetic Interference Rejection Ratio Referred to Non-Inverting Input (EMIRR+) vs Frequency

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted). (Cont.)

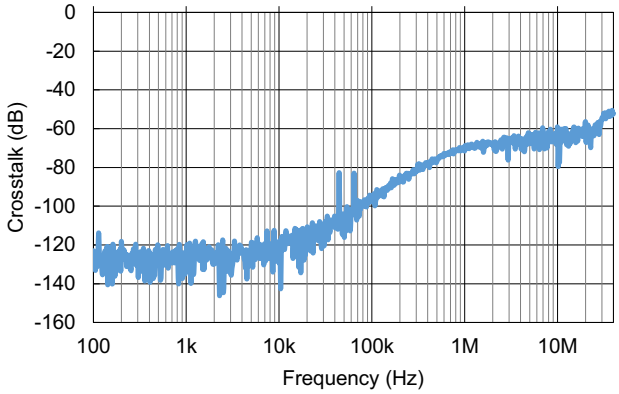


Figure 42. Channel Separation

5. Functional Description

5.1 Overview

The RRA7904x family comprises advanced low-power operational amplifiers featuring rail-to-rail input and output capabilities, specifically engineered for battery-powered and portable applications. Using innovative transistor technology, these amplifiers efficiently operate within an extensive supply voltage range, from an ultra-low 1.2V up to a standard 5.5V, making them versatile solutions across various system designs.

With a minimal quiescent current consumption of just 10μA per channel, the RRA79041, RRA79042 offers exceptional power efficiency while providing a high gain-bandwidth product of 350kHz. Its robust design includes a short-circuit current capability of 40mA at 5.5V, setting it apart in the industry for applications requiring higher output current in low-voltage environments.

The input common-mode voltage range of the RRA79041, RRA79042 encompasses both supply rails, allowing it to be seamlessly integrated into single or dual-supply configurations. The rail-to-rail input and output swings enhance the amplifier's dynamic range, making it an ideal choice for driving low-speed, precision analog-to-digital converters (ADCs).

Moreover, the class AB output stage provides reliable performance, capable of effectively driving resistive loads greater than 2kΩ between V+ and ground. The RRA79041, RRA79042 also maintains stability when driving capacitive loads up to 100pF, achieving a typical phase margin of 45°. Additional notable features include a moderate slew rate of 0.2V/μs and exceptionally low integrated noise (5.5μV_{P-P}, 0.1 to 10Hz bandwidth).

Designed with precision in mind, the RRA7904x family exhibits remarkably low input bias current of 1pA (typical), minimal input offset voltage of 0.6 mV (typical), and excellent power-supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and open-loop gain (AOL). These attributes make the RRA7904x series ideal for a wide variety of precision analog applications requiring low power consumption, high accuracy, and reliable performance.

5.2 Feature Description

5.2.1 Operating Voltage

The RRA7904x family of operational amplifiers is fully characterized and guaranteed to operate reliably across a wide supply voltage range from 1.2 V to 5.5 V. Critical performance parameters are specified across an extended temperature range from -40°C to 125°C, ensuring consistent operation in diverse environmental conditions. To ensure optimal performance and maintain stability, it is strongly recommended to bypass power supply pins with ceramic capacitors of at least 0.01μF.

5.2.2 Rail-To-Rail Input and Output (RRIO)

The RRA7904x series delivers advanced rail-to-rail input and output performance, uniquely engineered to enhance dynamic signal handling across the complete operating voltage range of 1.2V to 5.5V. At the heart of this capability is a sophisticated complementary input stage architecture, composed of both N-channel and P-channel differential transistor pairs operating in parallel. This innovative design allows each transistor pair to optimally handle specific segments of the common-mode input voltage, thereby maximizing linearity and precision.

The majority of the input common-mode voltage range is effectively managed by the P-channel differential pair, which is active from the negative supply rail up to approximately (V+) – 0.3V. Near the positive rail, the N-channel pair takes over, handling inputs from roughly (V+) – 0.5V up to the positive supply rail. The transition between these two transistor pairs occurs within a clearly defined yet narrow voltage region (typically from (V+) – 0.5V to (V+) – 0.3V) where both transistor pairs are briefly active simultaneously. Although this transitional region can slightly affect key parameters such as offset voltage, common-mode rejection, and distortion, the RRA7904x's advanced design substantially reduces this effect by maintaining a broader and more favorable P-channel operation region, especially beneficial at lower supply voltages.

Complementing its input stage, the RRA7904x incorporates a robust Class AB output stage featuring common-source transistor topology. This allows the amplifier's output to reliably swing within 20mV of either supply rail under typical conditions when driving resistive loads of up to 10kΩ. This robust output swing capability ensures maximum available dynamic range and exceptional compatibility with a broad spectrum of analog-to-digital converters (ADCs) and sensitive analog circuits, further solidifying the RRA79041, RRA79042 as an ideal solution for low-voltage precision applications.

5.2.3 EMI Filter

The RRA79041, RRA79042 possesses internal electromagnetic interference (EMI) filters that reduce the effects of EMI from external sources such as wireless communications and densely populated circuit boards with a mix of analog and digital components.

5.2.4 Overload Recovery

Overload recovery is defined as the time required for the op-amp output to return from a saturated state to the linear state. The op-amp output saturates when the output voltage exceeds the applied supply voltage, because of a high input voltage or a high gain setting. After entering saturation, charge carriers in the output stage require time to return to the linear operating region. Only then, does the device begins to slew at the specified slew rate.

Therefore, the propagation delay during an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the RRA7904x family is about 8µs.

5.2.5 Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the RRA7904x amplifiers, care should be taken in the circuit board layout. The surface of the printed circuit board must remain clean and free of moisture to avoid leakage-currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

5.2.6 Input and Output ESD Protection

The RRA7904x incorporates internal ESD protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes that are connected between the input and output pins and

the power-supply pins. If the input voltage is expected to exceed the specified value in the Absolute Maximum Ratings, insert a series resistor, R_S, that limits the input current to about 1mA (Figure 43).

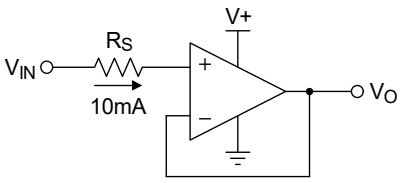


Figure 43. Input Current Protection

6. Application Information

6.1 Typical Applications

6.1.1 Low-Side Current Sensing

The RRA7904x operational amplifiers offer ultra-efficient, rail-to-rail input and output performance, specifically tailored for energy-conscious and compact electronic designs. Engineered to operate reliably from supply voltages as low as 1.2V and up to 5.5V, these amplifiers ensure excellent versatility across numerous analog applications. Featuring inherent unity-gain stability, the RRA7904x amplifiers integrate seamlessly into diverse circuit configurations. The integrated Class AB output stage robustly handles resistive loads above 2kΩ between the supply rails, enhancing overall design flexibility. The extensive input common-mode voltage range, which includes both supply rails, further supports a variety of design approaches—whether implemented in single-supply or dual-supply setups.

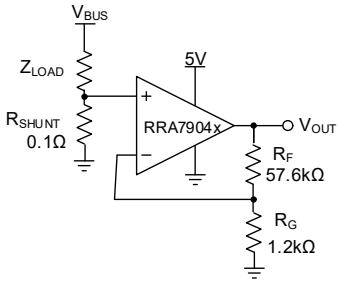


Figure 44. Low-Side Current Sensing Application

6.1.2 Design Procedure

The design aims to accommodate a load current from 0A to 1A with a maximum output voltage of 4.9V and a maximum shunt voltage of 100mV. To ensure that the shunt voltage does not exceed 100mV at the maximum load current, the shunt resistor is determined using:

(EQ. 1) $$R_{SHUNT} = \frac{V_{SHUNT_{MAX}}}{V_{LOAD_{MAX}}} = \frac{100mV}{1A} = 100mV$$

To achieve the required output voltage range from 0V to 4.9V, use Equation 2 to calculate the amplifier gain.

(EQ. 2) $$= \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{IN\_MAX} - V_{IN\_MIN}} = \frac{4.90V - 0V}{100mV - 0V} = 49V/V$$

This gain is set using feedback resistors, R_F and R_G, using Equation 3.

(EQ. 3) $$G = 1 + \frac{R_F}{R_G}$$

Selecting R_F = 57.6kΩ and R_G = 1.2kΩ precisely achieves the required gain of 49V/V. Adjusting these resistor values can optimize impedance levels, minimize parasitic effects, and tailor the circuit to specific system performance requirements. Ensure to adhere strictly to the recommended voltage limits (1.2V to 5.5V) for the RRA79041, RRA79042 to avoid permanent device damage and place the bypass capacitors (0.1µF) close to the supply pins.

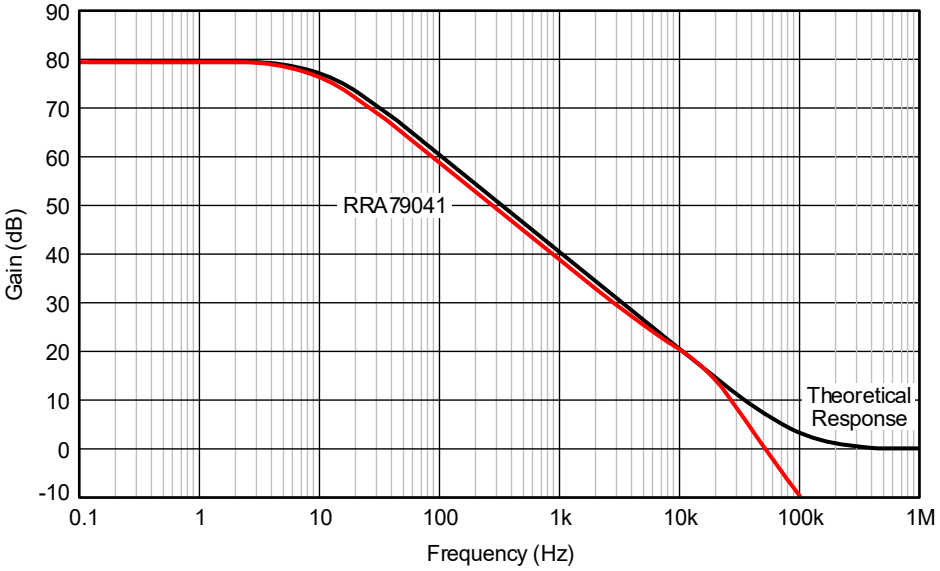


Figure 45. High-Gain Amplifier Frequency Response

6.2 Layout Considerations

To ensure optimal operational performance of the device, adhere to the following recommended PCB layout practices:

- Minimize noise propagation by employing bypass capacitors, providing a low-impedance path to ground. Connect low-ESR, 0.1-µF ceramic capacitors close to each power supply pin and ground. In single-supply designs, one capacitor from V+ to ground is sufficient.
- Establish separate grounding for analog and digital circuits to effectively suppress noise. Use dedicated ground planes on multilayer PCBs to distribute heat efficiently and reduce electromagnetic interference (EMI). Ensure careful physical separation between analog and digital grounds to manage ground current flow effectively.
- Keep input traces distant from supply and output traces to minimize parasitic coupling. If traces must intersect, cross them at 90-degree angles rather than running parallel.
- Position external components, such as RF and RG, close to the device inputs to minimize parasitic capacitance.
- Maintain short input traces since they are particularly susceptible to noise interference.
- Implement a low-impedance guard ring around critical traces to reduce leakage currents from adjacent traces at differing potentials.
- Clean the PCB thoroughly after assembly to achieve the best device performance.
- Due to potential performance shifts from moisture ingress into precision integrated circuits, it is advisable to perform a low temperature bake at 85°C for 30 minutes following aqueous PCB cleaning processes. This procedure effectively removes residual moisture from device packaging.

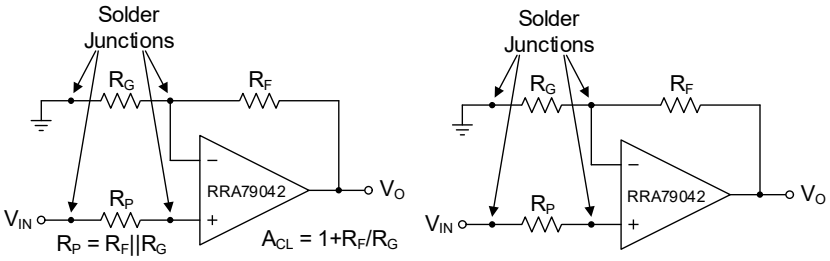


Figure 46. Schematic Representation

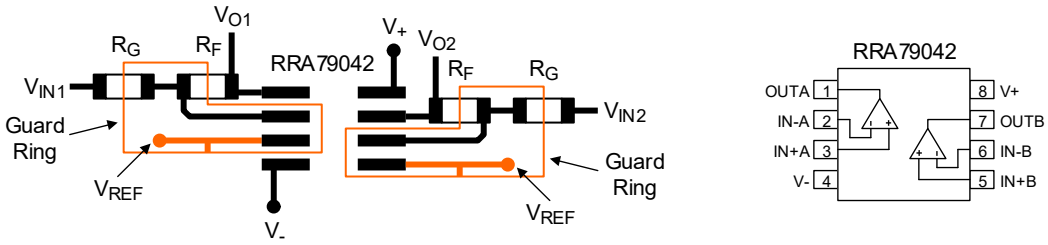


Figure 47. Layout Example

7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1]	# Channels	Part Marking	Package Description	Pkg. Dwg. #	MSL Rating[2]	Carrier Type[3]	Temp. Range
RRA79041-P3J	1	041P[4]	5 Ld SOT-23	P5.064	1	Reel, 3k units	-40 to 125°C
RRA79041-QAJ		041[4]	5 Ld SC70	P5.049	1	Reel, 3k units	
RRA79042-SNH	2	79042	8 Ld MSOP	M8.118D	1	Reel, 2.5k units	-40 to 125°C
RRA79042-SPH		79042 SP	8 Ld SOICN	M8.15	3	Reel, 2.5k units	
RRA79042-NSH		042	8 Ld DFN	L8.2x2F	1	Reel, 1k units	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For more information about Moisture Sensitivity Level (MSL), see TB363.
3. See TB347 for details about reel specifications.
4. The part marking is located on the bottom of the part.

9. Revision History

Revision	Date	Description
1.02	Dec 19, 2025	Added the Dual Op Amp (RRA79042) information throughout.
1.01	Dec 15, 2025	Updated Input Offset Voltage maximum specs from ±1.8mV to ±1.9mV and from ±2.05mV to ±2.15mV.
1.00	Nov 20, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRA79041-P3J	5	SOT-23	P5.064
RRA79041-QAJ	5	SC70	P5.049
RRA79042-SNH	8	MSOP	M8.118D
RRA79042-SPH	8	SOICN	M8.15
RRA79042-NSH	8	DFN	L8.2x2F

A.2 Symbol Pin Information

A.2.1 5-SC70

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	IN+	Input	-
2	V-	Power	-
3	IN-	Input	-
4	OUT	Output	-
5	V+	Power	-

A.2.2 5-SOT-23

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT	Output	-
2	V-	Power	-
3	IN+	Input	-
4	IN-	Input	-
5	V+	Power	-

A.2.3 8-SOICN/MSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	V+	Power	-

A.2.4 8-DFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	V+	Power	-
EPAD9	TBD	TBD	-

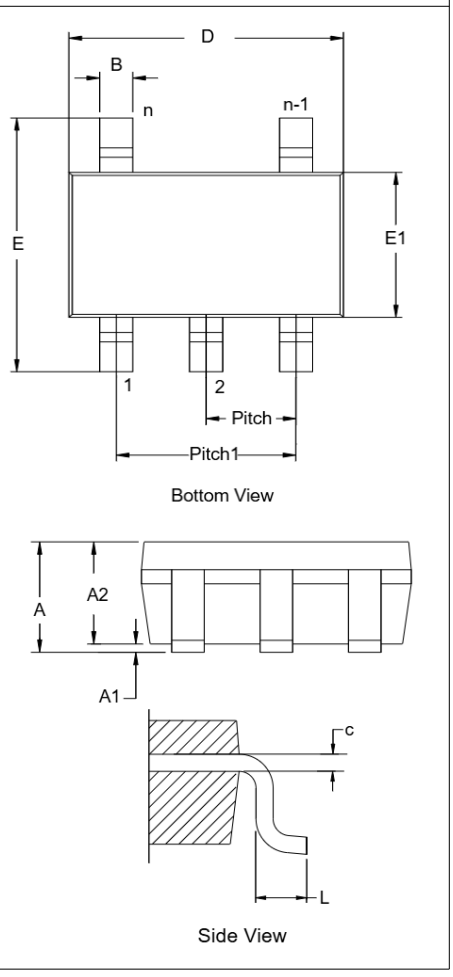
A.3 Symbol Parameters

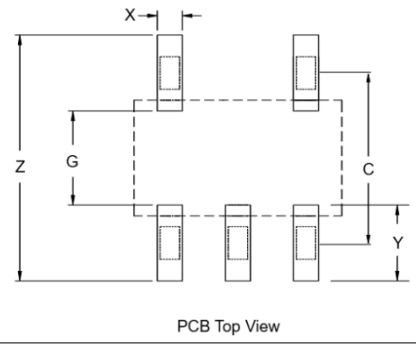
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Number of Channels	Slew Rate	Operating Supply Current	Input Offset Voltage (V_{OS})
RRA79041-P3J	Industrial	SMD	Compliant	-40 °C	125 °C	1.2 V	5.5 V	1	0.2 V/µs	10 µA	±0.5 mV
RRA79041-QAJ	Industrial	SMD	Compliant	-40 °C	125 °C	1.2 V	5.5 V	1	0.2 V/µs	10 µA	±0.5 mV
RRA79042-SNH	Industrial	SMD	Compliant	-40 °C	125 °C	1.2 V	5.5 V	2	0.2 V/µs	10 µA	±0.5 mV
RRA79042-SPH	Industrial	SMD	Compliant	-40 °C	125 °C	1.2 V	5.5 V	2	0.2 V/µs	10 µA	±0.5 mV
RRA79042-NSH	Industrial	SMD	Compliant	-40 °C	125 °C	1.2 V	5.5 V	2	0.2 V/µs	10 µA	±0.5 mV

A.4 Footprint Design Information

A.4.1 5-SC70

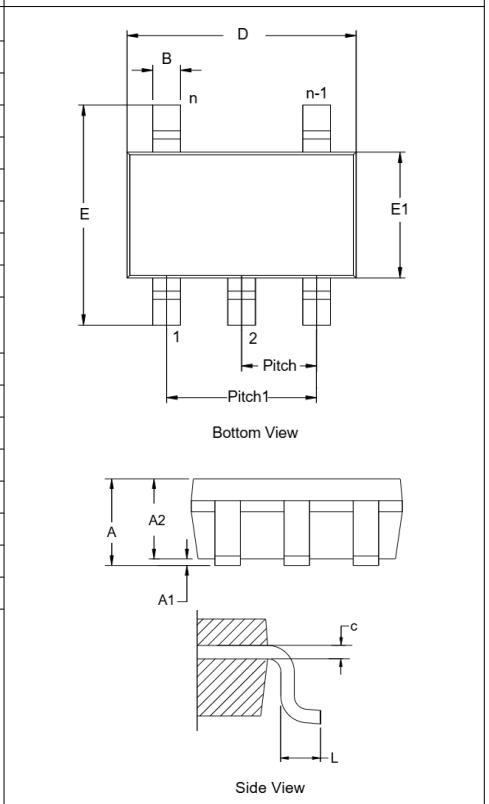
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SC70	P5.049/KA0005AA	5

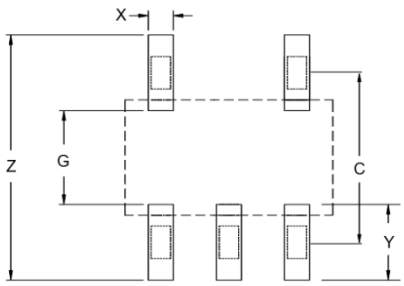
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	1.85	
Maximum body span (vertical side)	Dmax	2.15	
Minimum lead span (horizontal side)	Emin	1.80	
Maximum lead span (horizontal side)	Emax	2.40	
Minimum lead width	Bmin	0.15	
Maximum lead width	Bmax	0.30	
Minimum body width (horizontal side)	E1min	1.15	
Maximum body width (horizontal side)	E1max	1.35	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.65	
Overall pitch (e1)	Pitch1	1.30	
Maximum Height	Amax	1.10	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.22	
Minimum Lead Length	Lmin	0.26	
Maximum Lead Length	Lmax	0.46	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between pads. Measured from outside edges	Z	2.85	
Distance between pads. Measured from inside edges	G	1.35	
Pad width	X	0.40	
Pad length	Y	0.75	
Row spacing. Distance between pad centers	C	2.10	

A.4.2 5-SOT23

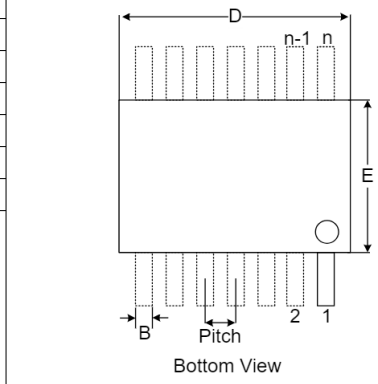
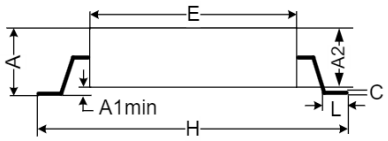
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOT23	P5.064/KA0005AB	5

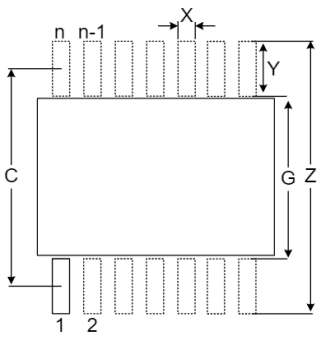
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.80	
Maximum body span (vertical side)	Dmax	3.00	
Minimum lead span (horizontal side)	Emin	2.60	
Maximum lead span (horizontal side)	Emax	3.00	
Minimum lead width	Bmin	0.30	
Maximum lead width	Bmax	0.50	
Minimum body width (horizontal side)	E1min	1.50	
Maximum body width (horizontal side)	E1max	1.70	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.95	
Overall pitch (e1)	Pitch1	1.90	
Maximum Height	Amax	1.45	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.30	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	022	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.55	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between pads. Measured from outside edges	Z	3.60	
Distance between pads. Measured from inside edges	G	1.20	
Pad width	X	0.60	
Pad length	Y	1.20	
Row spacing. Distance between pad centers	C	2.40	

A.4.3 8-SOICN

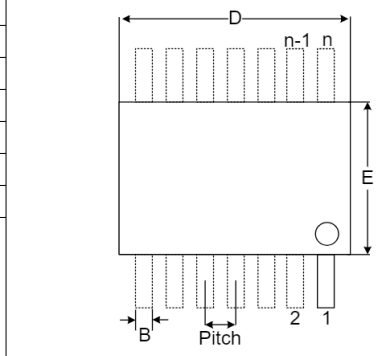
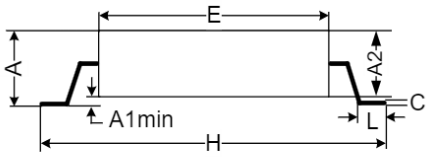
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOIC	M8.15/GS0008AC	8

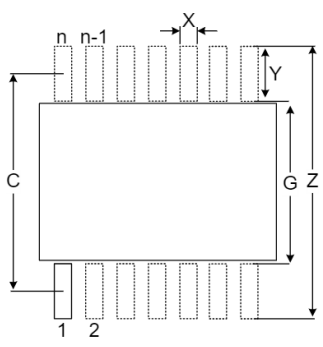
Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	5.80	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.20	
Minimum body span (horizontal side)	Dmin	4.80	
Maximum body span (horizontal side)	Dmax	5.00	
Minimum body span (vertical side)	Emin	3.80	
Maximum body span (vertical side)	Emax	4.00	
Minimum Lead Width	Bmin	0.33	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	1.27	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.40	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.00	
Row spacing. Distance between pad centers	C	5.20	
Pad Width	X	0.60	
Pad Length	Y	2.20	

A.4.4 8-MSOP

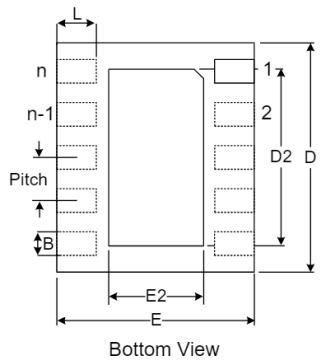
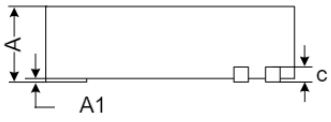
IPC Footprint Type	Package Code/ POD number	Number of Pins
SOP	M8.118D/HV0008AC	8

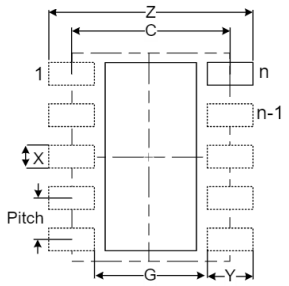
Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	4.70	 Bottom View
Maximum lead span (horizontal side)	Hmax	5.10	
Minimum body span (horizontal side)	Dmin	2.90	
Maximum body span (horizontal side)	Dmax	3.10	
Minimum body span (vertical side)	Emin	2.90	
Maximum body span (vertical side)	Emax	3.10	
Minimum Lead Width	Bmin	0.22	
Maximum Lead Width	Bmax	0.40	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	0.80	
Maximum Height	Amax	1.10	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.23	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.65	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	5.50	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.10	
Row spacing. Distance between pad centers	C	4.30	
Pad Width	X	0.32	
Pad Length	Y	1.20	

A.4.5 8-DFN

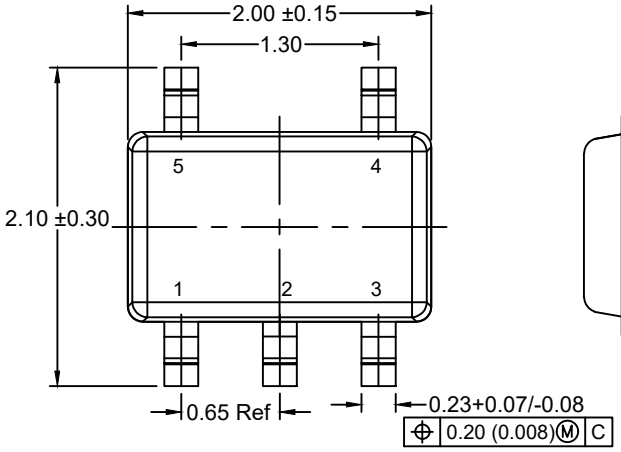
IPC Footprint Type	Package Code/ POD Number	Number of Pins
DFN	L8.2x2F	8

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	1.90	 Bottom View
Maximum body span (vertical side)	Dmax	2.10	
Minimum body span (horizontal side)	Emin	1.90	
Maximum body span (horizontal side)	Emax	2.10	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Maximum Height	Amax	0.80	
Minimum Standoff Height	A1min	0.00	 Side View
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	
Number of pins	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.50	
Minimum thermal pad size (vertical side)	D2min	1.50	
Maximum thermal pad size (vertical side)	D2max	1.70	
Minimum thermal pad size (horizontal side)	E2min	0.80	
Maximum thermal pad size (horizontal side)	E2max	1.00	

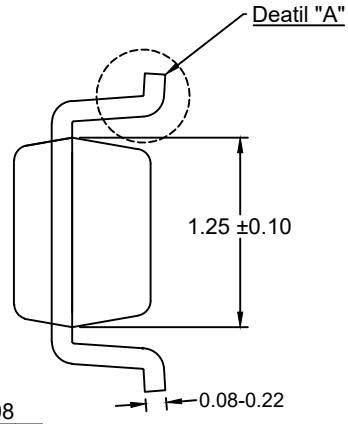
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Row spacing. Distance between pad centres	C	1.85	 PCB Top View
Distance between pads. Measured from outside edges	Z	2.30	
Distance between pads. Measured from inside edges	G	1.40	
Pad Width	X	0.25	
Pad Length	Y	0.45	

Package Outline Drawing

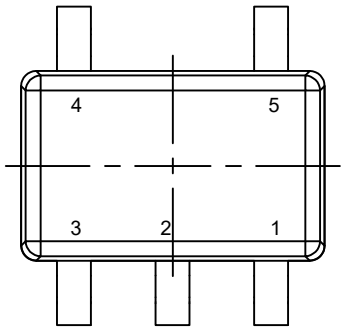
P5.049
KA0005AA
5-SC70 2.0 x 1.25 x 0.95 mm Body, 0.65mm Pitch Lead Small Outlibe Transistor Plastic Package
Rev04, Jul 16, 2025



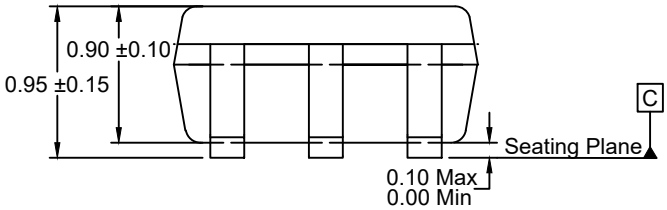
Top View



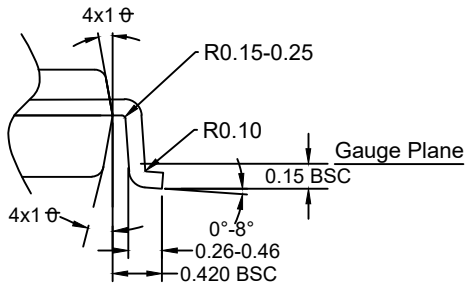
Side View



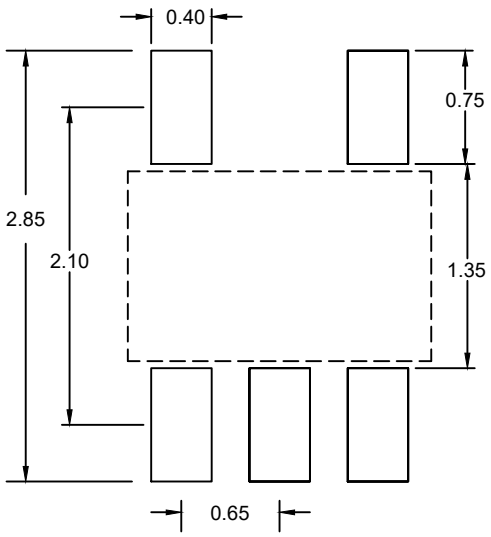
Bottom View



Side View



Detail"A"

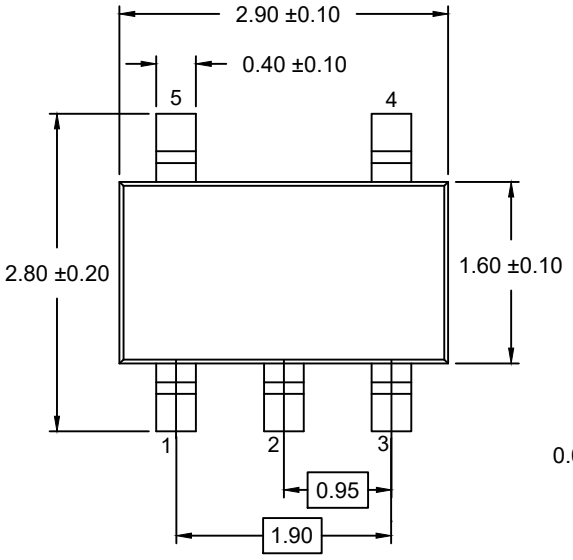


Recommended Land Pattern

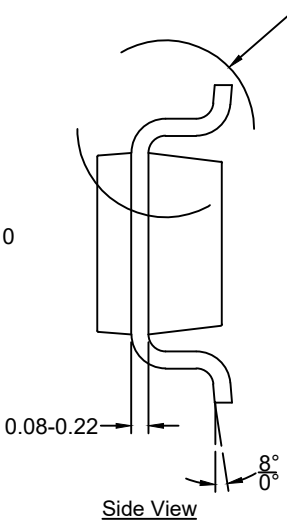
Notes:
1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions body x and y are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Converted inch dimen

Package Outline Drawing

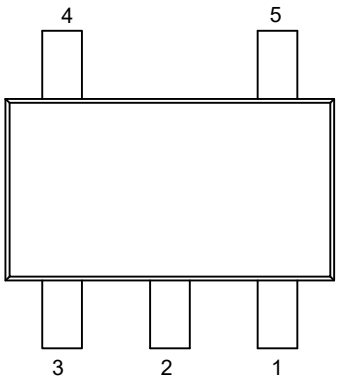
P5.064
KA0005AB
5-SOT 2.90 x 1.60 x 1.45 mm Body, 0.95mm Pitch Lead Small Outline Transistor Plastic Package
Rev04, Jul 22, 2025



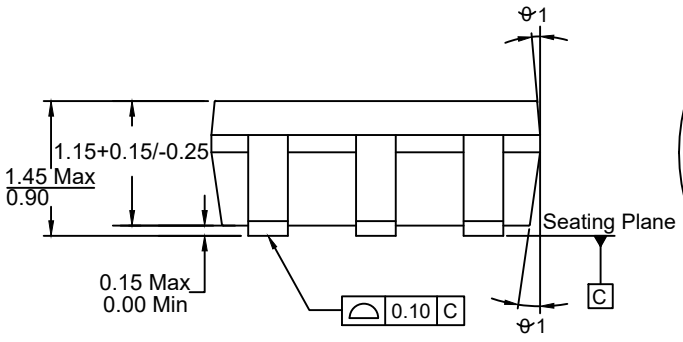
Top View



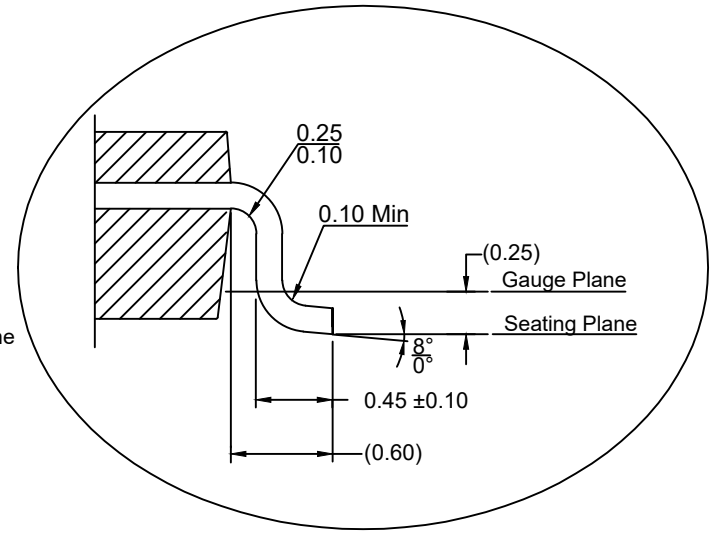
Side View



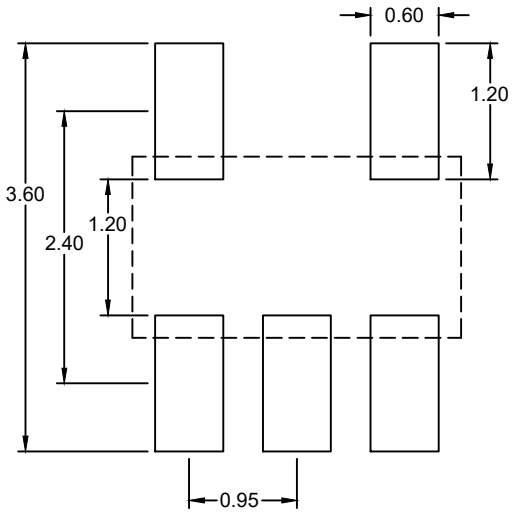
Bottom View



Side View



Detail "A"



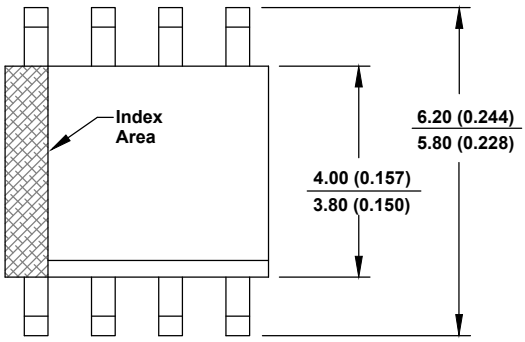
Recommended Land Pattern

Notes:

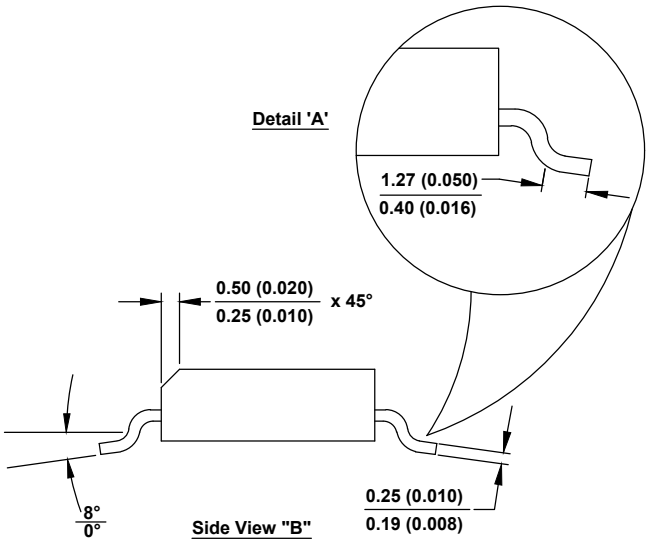
1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA
3. Package length and width are exclusive of mold flash, protrusions or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: Millimeter.

Package Outline Drawing

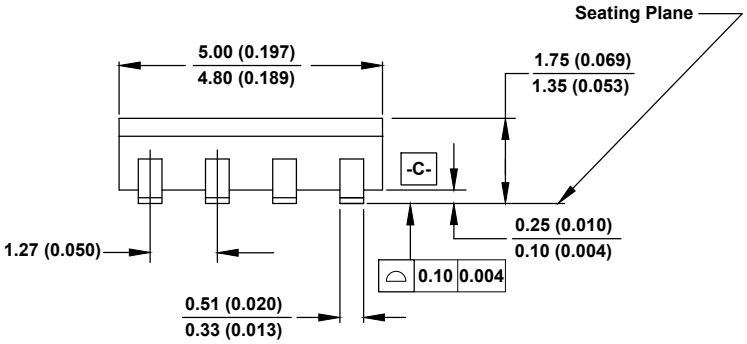
M8.15
GS0008AC
8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch
Rev08, Jul 7, 2025



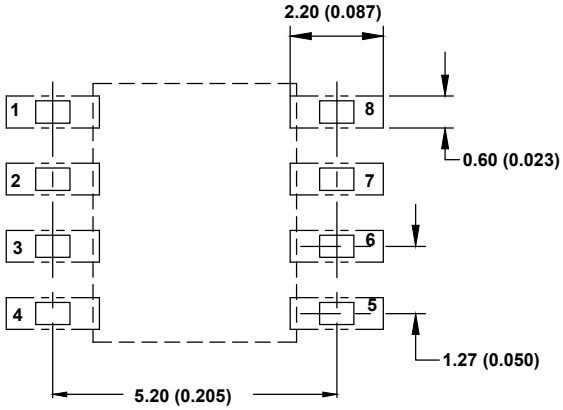
Top View



Side View "B"



Side View "A"



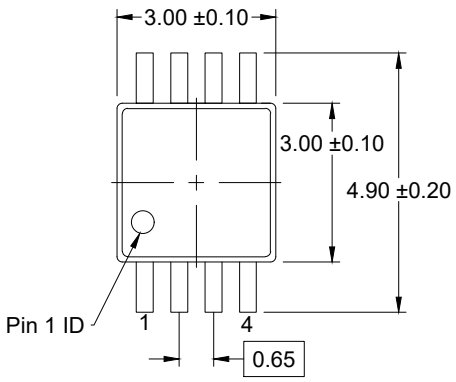
Typical Recommended Land Pattern

Notes:

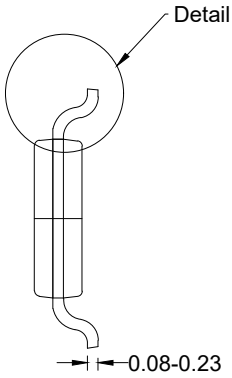
1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

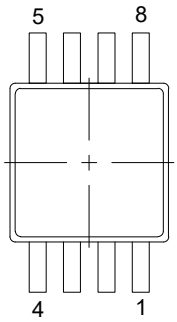
M8.118D
HV0008AC
8-MSOP 3.00 x4.90 x 1.10 mm Body, 0.65 mm Pitch
Rev03, Jul 11, 2025



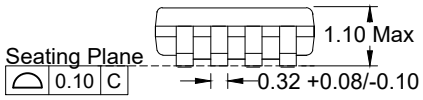
Top View



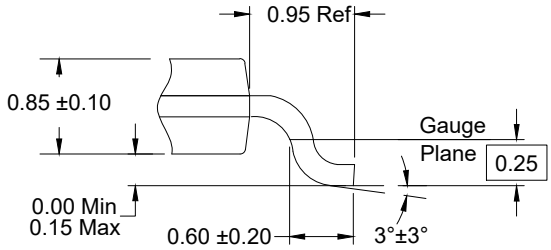
Side View



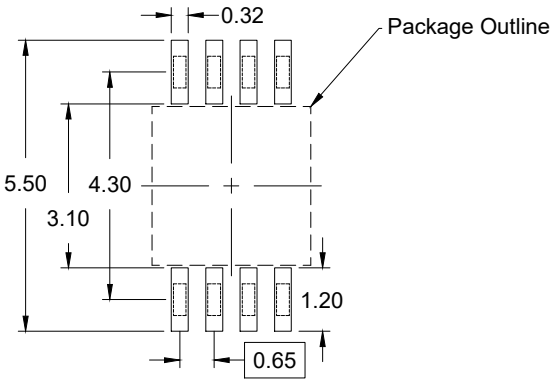
Bottom View



Side View



Detail "X"



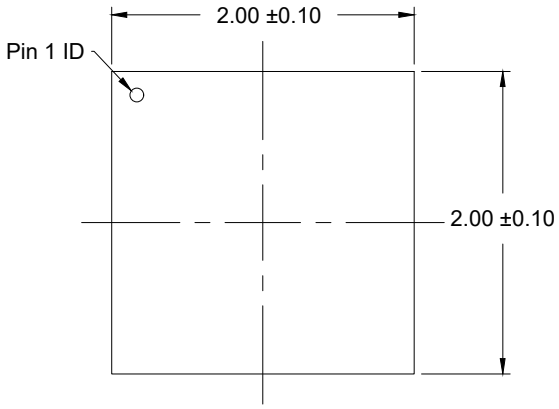
Typical Recommended Land Pattern

Notes:

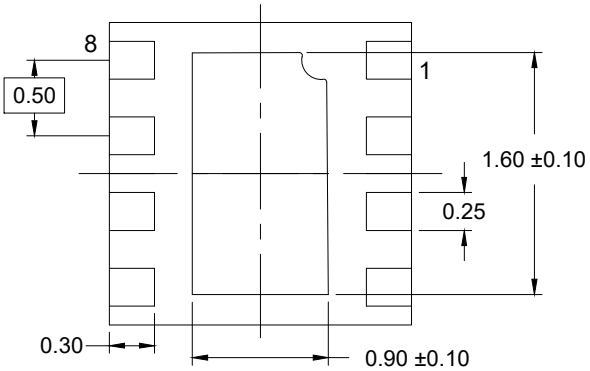
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

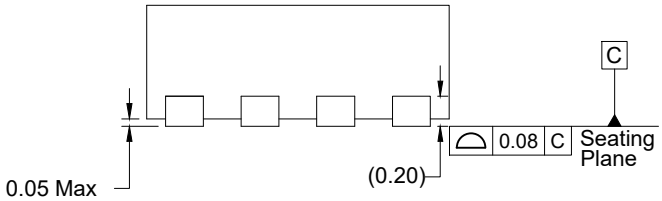
L8.2x2F
DW0008AA
8-DFN 2.0 x2.0 x 0.8 mm Body, 0.50mm Pitch
Rev 00, Jan 21, 2025



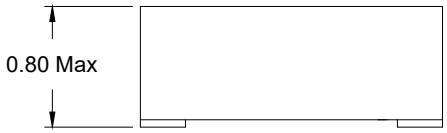
Top View



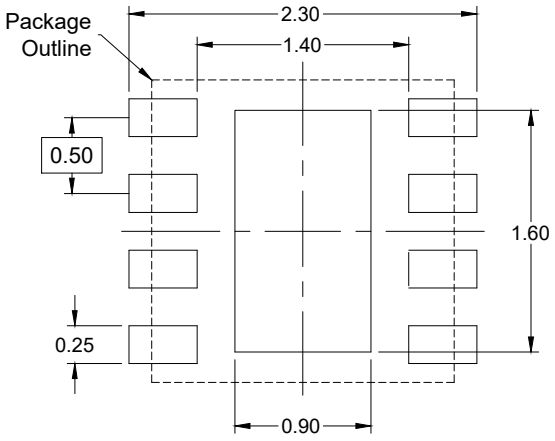
Bottom View



Side View (Rotated 90°)



Side View



Recommende Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.