RRB86848

Bidirectional Buck-Boost Voltage Regulator with SMBus Interface for General 48V and USB PD

Description

The RRB86848 is a bidirectional, buck-boost voltage regulator for power tools, portable vacuums, lawn mowers, and additional system bus regulation for notebooks. This regulator provides protection features and supports any USB-C interface platform including USB PD EPR. The advanced Renesas R3™ technology provides highly efficient light-load operation and fast transient response.

RRB86848 takes input power from a wide range of DC power sources (such as conventional AC/DC adapters (ADP), USB PD ports, travel ADP) and safely converts it to a regulated voltage.

RRB86848 also operates in the reverse direction, converting a wide-range DC power source connected at its output side to a regulated voltage at its input (ADP side). The bidirectional buck-boost regulation feature provides flexibility in developing applications with the RRB86848.

RRB86848 provides programming resistor options for setting the output voltage, the adapter current limit, and the output current limit. Additionally, it provides serial communication that enables programming of many critical parameters to deliver a customized solution.

Features

- Bidirectional buck, boost, and buck-boost operation
- Input voltage range: 3.9V to 55V (no dead zone)
- Output voltage: 2.4V to 55V
- Pass-Through mode in forward direction
- Adapter current and output current monitor (AMON/BMON)
- Battery charging support
- Forward and reverse sleep modes
- 4×4 32 Ld TQFN package compatible with the ISL9238, RAA489108, and RAA489118 family of parts

Applications

- Voltage regulation for docking stations and other applications using USB-C EPR inputs or outputs
- Battery charging for lawnmowers and other lawn tools, eBikes, power tools, power banks

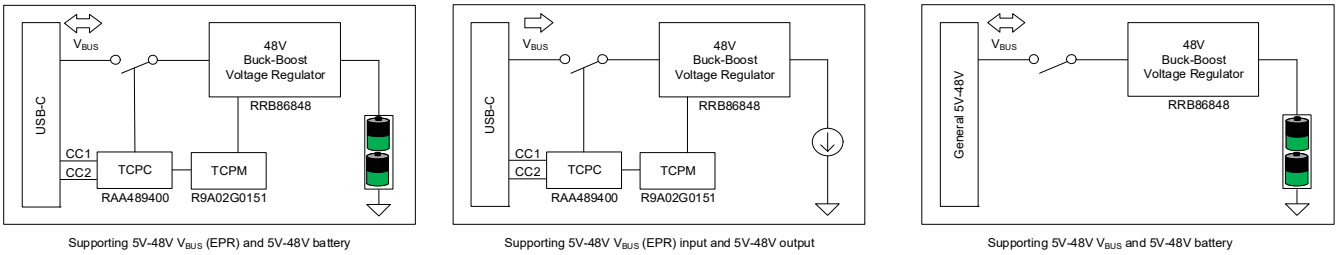


Figure 1. Full-Featured Architecture Solutions Enabled by RRB86848

Contents

1. Overview

1.1 Typical Application Diagram

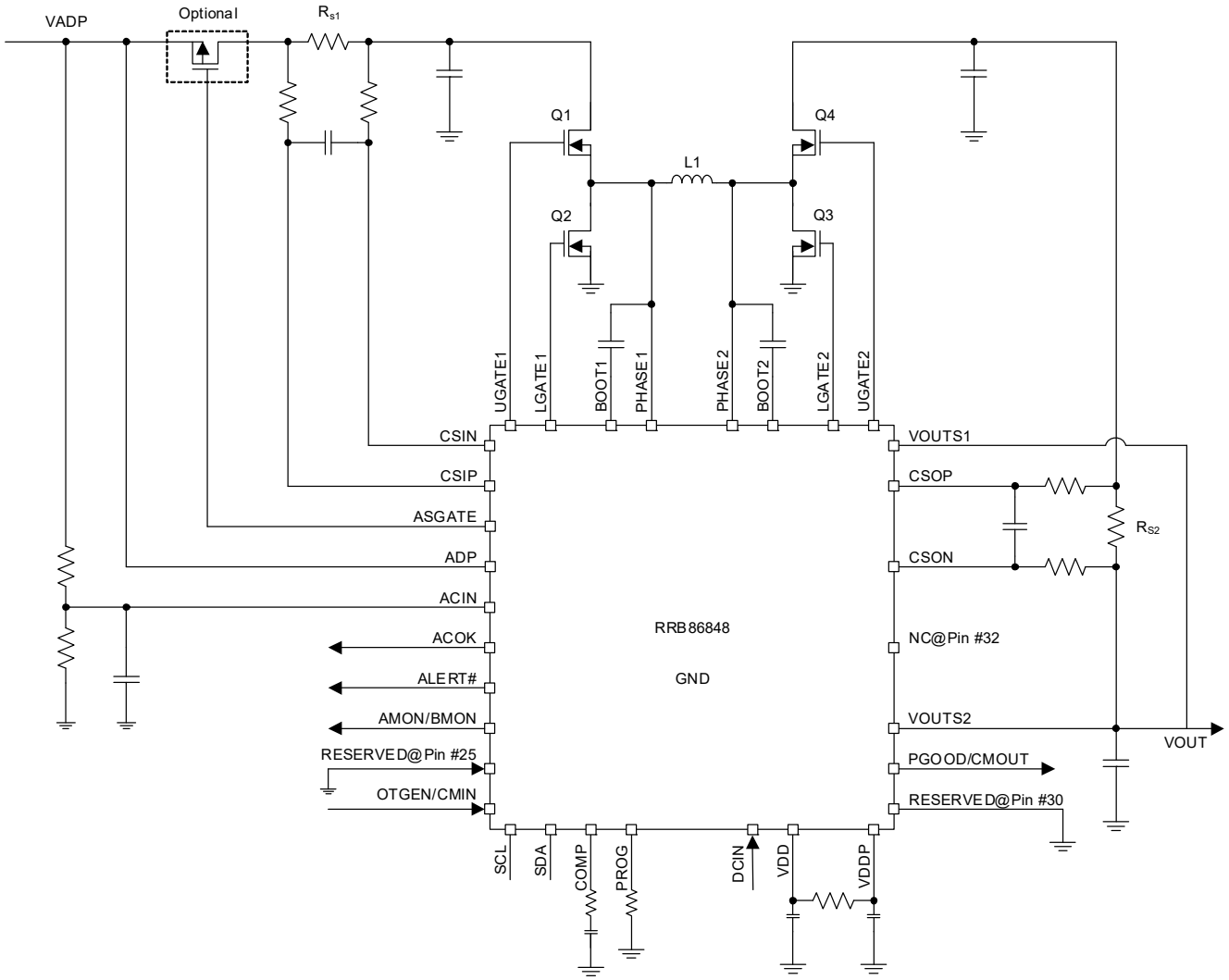


Figure 2. Typical Application Circuit

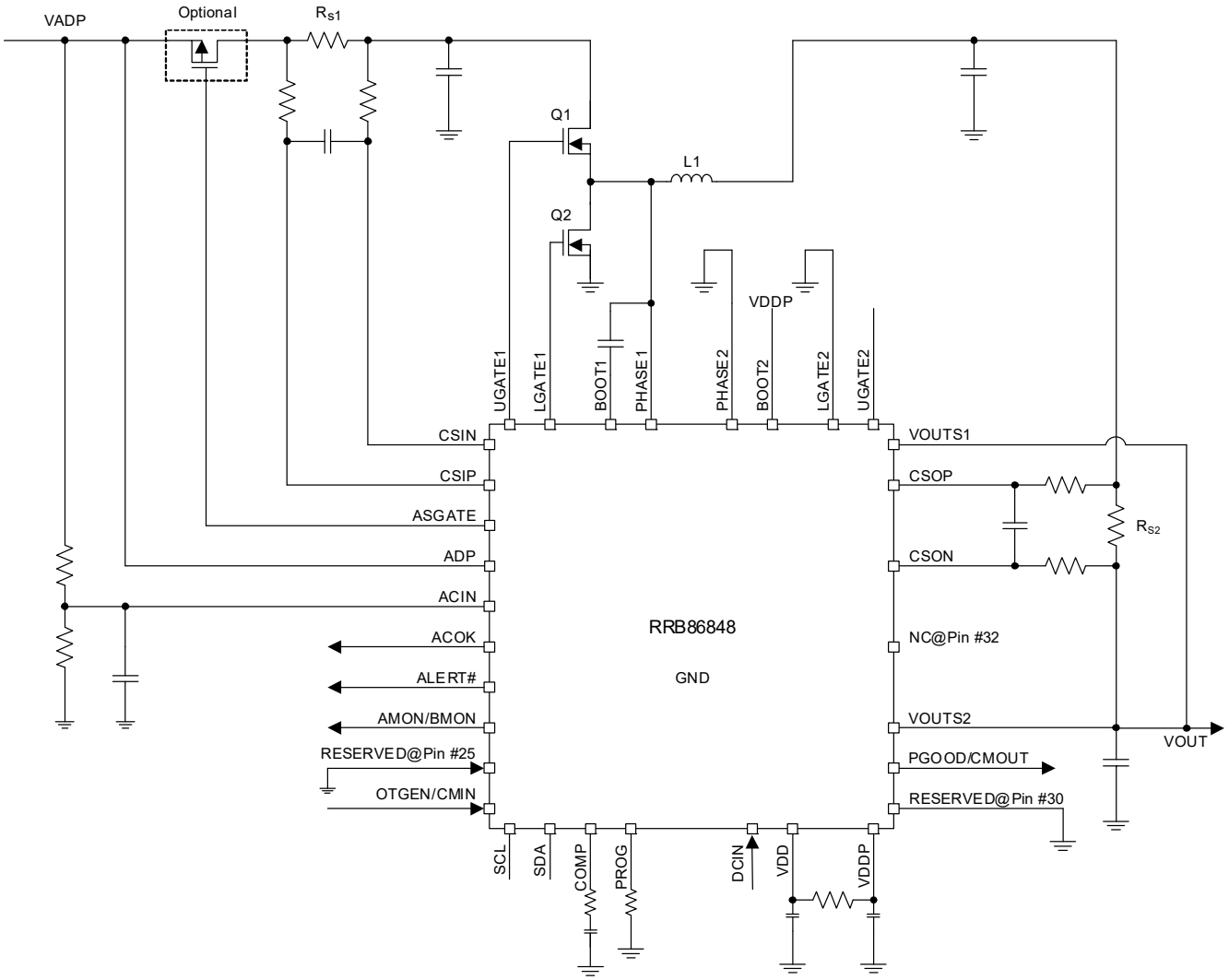


Figure 3. Application Circuit for 2-FET Mode

1.2 Block Diagram

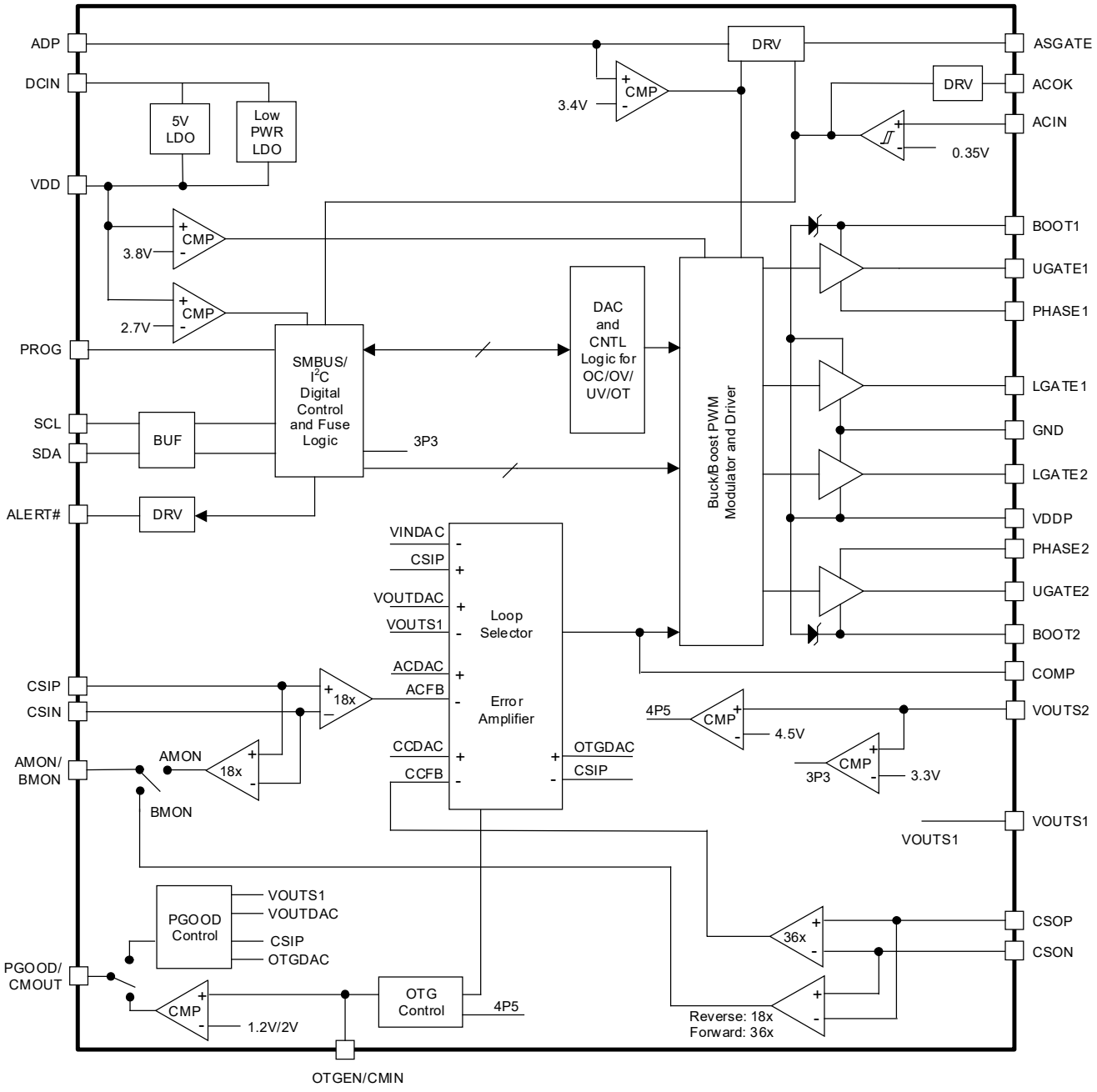


Figure 4. Block Diagram

2. Pin Information

2.1 Pin Assignments

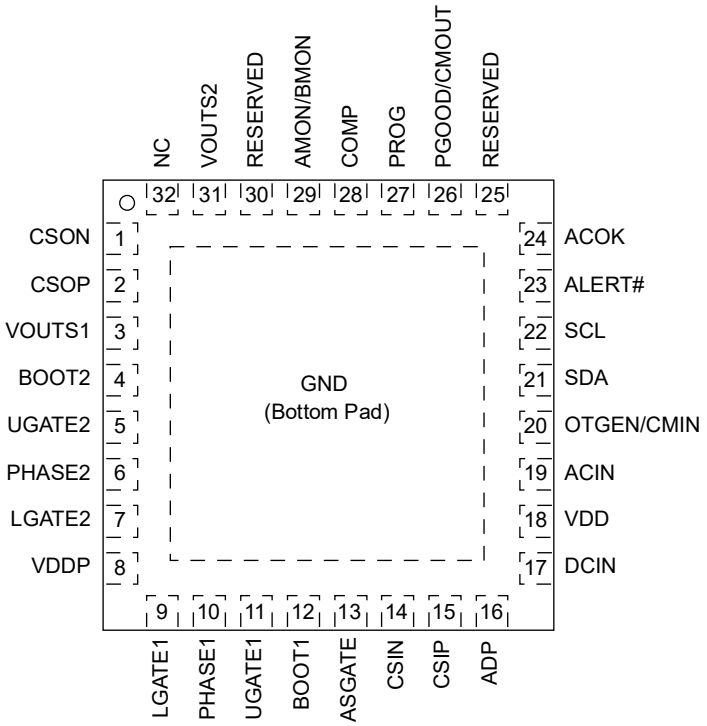


Figure 5. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat dissipation.
1	CSON	Forward mode output current sense negative input. Connect to the forward output current sense resistor negative input. Place a ceramic capacitor between CSOP and CSON to provide differential mode filtering.
2	CSOP	Forward mode output current sense positive input. Connect to the forward output current sense resistor positive input. Place a ceramic capacitor between CSOP and CSON to provide differential mode filtering.
3	VOUTS1	Provides feedback voltage for OutputVoltage regulation.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins. Connect a 0.47µF bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain, and one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and one terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.

Pin Number	Pin Name	Description
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins. Connect a 0.47µF bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional. If they are not used, leave the ASGATE pin floating.
14	CSIN	Forward mode input current sense negative input. Connect to the forward input current sense resistor negative input. Place a ceramic capacitor between CSIP and CSIN to provide differential mode filtering.
15	CSIP	Forward mode input current sense positive input. Connect to the forward input current sense resistor positive input. Place a ceramic capacitor between CSIP and CSIN to provide differential mode filtering. The modulator also uses the CSIP pin for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Forward mode input used to sense adapter voltage. ASGATE is turned on when the adapter voltage is higher than 3.2V.
17	DCIN	Internal LDO input that provides power to the IC. Connect a diode OR from the adapter and output. Bypass DCIN with an MLCC capacitor. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VOUT diodes, and connect a 4.7µF DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 30V.
18	VDD	Internal LDO output, which provides the bias power for the internal analog and digital circuit. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V. If VDD is pulled below 2V for more than 1ms, the RRB86848 resets all the SMBus register values to their defaults. An external source can provide VDD power by overdriving the LDO output.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.35V.
20	OTGEN/ CMIN	Input pin. OTG/reverse mode enable pin, general-purpose comparator input pin. When the reverse mode is enabled and the general-purpose comparator is disabled, pulling this pin high can activate the reverse mode. When the general-purpose comparator is enabled, this pin is the general-purpose comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
23	ALERT#	Open-drain output. Provides an active-low alert signal if ACOK goes low and/or the general-purpose comparator activates. The ALERT# triggers are enabled using SMBus commands (see Table 7).
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	RESERVED	Must be connected to GND.
26	PGOOD/ CMOUT	Open-drain output. This pin provides either a power-good indication or the general-purpose comparator output.
27	PROG	A resistor from the PROG pin to GND sets the following configurations: ▪ Default output voltage ▪ Default adapter current limit ▪ Default output current limit See Table 15 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Forward input current, reverse output current, forward output current, or reverse input current monitor output. ▪ AMON_FORWARD = 18x (V_{CSIP} - V_{CSIN}) for forward input current monitor ▪ AMON_REVERSE = 18x (V_{CSIN} - V_{CSIP}) for reverse output current monitor ▪ BMON_FORWARD= 36x (V_{CSOP} - V_{CSON}) for forward output current monitor ▪ BMON_REVERSE = 18x (V_{CSON} - V_{CSOP}) for reverse input current monitor
30	RESERVED	This pin should not float. Connect to either VDD or GND.
31	VOUTS2	Voltage sense pin for reverse mode. Connect VOUTS1 pin to VOUTS2 pin for Voltage regulator configuration. Connect an optional ceramic capacitor >1µF from VOUTS2 to GND.
32	Unused	-

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Units
CSIP, CSIN, DCIN, ADP, ASGATE	-0.3	+63	V
PHASE1	GND - 0.3	+63	V
PHASE1	GND - 2 (<20ns)	+63	V
BOOT1, UGATE1	GND - 0.3	VDDP+63	V
PHASE2	GND - 0.3	63	V
PHASE2	GND - 2 (<20ns)	63	V
BOOT2, UGATE2	GND - 0.3	VDDP+63	V
LGATE1, LGATE2	GND - 0.3	+6.5	V
LGATE1, LGATE2	GND - 2 (<20ns)	+6.5	V
VOUTS2, VOUTS1, CSOP, CSON	-0.3	+63	V
VDD, VDDP	-0.3	+6.5	V
COMP	-0.3	+6.5	V
AMON/BMON, RESERVED@Pin30	-0.3	+6.5	V
OTGEN, RESERVED@Pin25	-0.3	+6.5	V
ACIN, ALERT#, PGOOD, ACOK	-0.3	+6.5	V
SCL, SDA	-0.3	+6.5	V
BOOT1 - PHASE1, BOOT2 - PHASE2	-0.3	+6.5	V
CSIP - CSIN, CSOP - CSON	-0.3	+0.3	V
PGOOD, ACOK	-	2	mA
Junction Temperature Range (T_J)	-10	+125	°C
Maximum Storage Temperature Range (T_S)	-65	+175	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter		Minimum	Maximum	Unit
Ambient Temperature	RRB86848-AT7/AU7	-10	+100	°C
	RRB86848-AT8/AU8	-40	+100	°C
Junction Temperature	RRB86848-AT7/AU7	-10	+125	°C
	RRB86848-AT8/AU8	-40	+125	°C
Adapter Voltage	-	+4	+55	V

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	32 Ld TQFN Package	θ_{JA}[1]	Junction to ambient.	37	°C/W
		θ_{JC}[2]	Junction to case.	2	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r	-	**3.05**	3.36	**3.7**	V
VADP UVLO Hysteresis	VADP_UVLO_h	-	-	730	-	mV
VOUTS2 UVLO Rising	VOUTS2_UVLO_r	-	**3.05**	3.27	**3.54**	V
VOUTS2 UVLO Hysteresis	VOUTS2_UVLO_h	-	-	270	-	mV
VOUTS2 4P5V Rising	VOUTS2_4P5_r	-	**4.2**	4.5	**4.9**	V
VOUTS2 4P5V Hysteresis	VOUTS2_4P5_h	-	-	345	-	mV
VDD 2P7 POR Falling, SMBus and BMON Active Threshold	VDD_2P7_f	-	**2.45**	2.7	**2.9**	V
VDD 2P7 POR Hysteresis[2]	VDD_2P7_h	-	-	150	-	mV
VDD 3P8 POR Rising, Modulator and Gate Driver Active	VDD_3P8_r	-	**3.6**	3.8	**3.9**	V
VDD 3P8 POR Hysteresis	VDD_3P8_h	-	-	135	-	mV
ACIN Rising	ACIN_r	-	**0.33**	0.35	**0.37**	V
ACIN Hysteresis	ACIN_h	-	-	22	-	mV
Linear Regulator						
VDD Output Voltage (VDD = 5V setting)	VDD	6V < V_{DCIN} < 54V	4.5	5.0	5.5	V
VDD Output Voltage (VDD = 4.5V setting)	VDD	6V < V_{DCIN} < 54V	4.05	4.5	4.95	V
VDD Dropout Voltage	VDD_dp	<22mA, V_{DCIN} = 4V	-	-	**210**	mV
VDD Overcurrent Threshold	VDD_OC	AT7/AU7 Junction Temperature: -10 to +125°C	90	120	145	mA
		AT8/AU8 Junction Temperature: -40 to +125°C	85	120	155	mA
Bias Current						
Forward Supply Current	I_{FWD_SLP}	GPC OFF, AMON/BMON OFF ADP=CSIN=CSIP=DCIN=VDDP=5V, VOUTS2 tied to VOUTS1, Control5[3] = High	-	7	30	µA
		GPC OFF, AMON/BMON OFF ADP=CSIN=CSIP=DCIN=48V, VDDP=5V, VOUTS2 tied to VOUTS1, Control5[3] = High	-	12	35	µA

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Reverse Supply Current	I_{REV_SLP1}	No Adapter, GPC OFF, AMON/BMON OFF, V_{OUT} = 50.4V, DCIN current comes from V_{OUT}, RSLP = I_{VOUTS2} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VOUTS1}	-	18	**50**	µA
	I_{REV_SLP2}	No Adapter, GPC OFF, AMON/BMON ON, V_{OUT} = 50.4V, DCIN current comes from V_{OUT}, RSLP = I_{VOUTS2} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VOUTS1}	-	84	**135**	µA
Adapter Current Regulation, R_{S1} = 10mΩ						
Adapter Current Accuracy	-	CSIP - CSIN = 50mV	-	5	-	A
			-2.7	-	**2.7**	%
		CSIP - CSIN = 40mV	-	4	-	A
			-3	-	**3**	%
		CSIP - CSIN = 30mV	-	3	-	A
			-3.5	-	**3.5**	%
		CSIP - CSIN = 25mV	-	2.5	-	A
			-4.2	-	**4.2**	%
		CSIP - CSIN = 20mV	-	2	-	A
			-5		**5**	%
		CSIP - CSIN = 15mV	-	1.5	-	A
			-6.9	-	**6.9**	%
		CSIP - CSIN = 10mV	-	1	-	A
			-10	-	**10**	%
		CSIP - CSIN = 5mV	-	0.5	-	A
			-20	-	**20**	%
		CSIP - CSIN = 2.5mV		0.25		A
			-40		**40**	%

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage Regulation						
Output Voltage Accuracy	-	OutputVoltage for 48V and 50.4V, AT7/AU7 Junction Temperature: -10 to +125°C	**-0.7**	-	**0.7**	%
		OutputVoltage for 42V and 46.2V, AT7/AU7 Junction Temperature: -10 to +125°C	**-0.7**	-	**0.7**	%
		OutputVoltage for 33.6V and 37.8V, AT7/AU7 Junction Temperature: -10 to +125°C	**-0.8**	-	**0.8**	%
		OutputVoltage for 25.2V and 29.4V, AT7/AU7 Junction Temperature: -10 to +125°C	**-0.8**	-	**0.8**	%
		OutputVoltage for 16.8V and 21V, AT7/AU7 Junction Temperature: -10 to +125°C	**-1.3**	-	**1.3**	%
		OutputVoltage for 8.4V and 12.6V, AT7/AU7 Junction Temperature: -10 to +125°C	**-1.5**	-	**1.5**	%
		OutputVoltage for 48V and 50.4V AT8/AU8 Junction Temperature: -40 to +125°C	**-0.8**	-	**0.8**	%
		OutputVoltage for 42V and 46.2V AT8/AU8 Junction Temperature: -40 to +125°C	**-0.8**	-	**0.8**	%
		OutputVoltage for 33.6V and 37.8V AT8/AU8 Junction Temperature: -40 to +125°C	**-0.9**	-	**0.9**	%
		OutputVoltage for 25.2V and 29.4V AT8/AU8 Junction Temperature: -40 to +125°C	**-0.9**	-	**0.9**	%
		OutputVoltage for 16.8V and 21V AT8/AU8 Junction Temperature: -40 to +125°C	**-1.4**	-	**1.4**	%
		OutputVoltage for 8.4V and 12.6V AT8/AU8 Junction Temperature: -40 to +125°C	**-1.6**	-	**1.6**	%
Input Voltage Regulation Accuracy	-	Input Voltage Register = 4.096V	**3.85**	-	**4.3**	V
Output Current Regulation, R_{s2} = 5mΩ (Limits apply across temperature range of 0°C to +85°C)						
Output Current Accuracy	-	V_{CSOP} - V_{CSON} = 30mV	-	6	-	A
			-3.5	-	**3.5**	%
		V_{CSOP} - V_{CSON} = 25mV	-	5	-	A
			-3.85	-	**3.85**	%
		V_{CSOP} - V_{CSON} = 20mV	-	4	-	A
			-4	-	**4**	%
		V_{CSOP} - V_{CSON} = 15mV	-	3	-	A
			-5.2	-	**5.2**	%
		V_{CSOP} - V_{CSON} = 10mV	-	2	-	A
			-6	-	**6**	%
		V_{CSOP} - V_{CSON} = 5mV	-	1	-	A
			-12	-	**12**	%
		V_{CSOP} - V_{CSON} = 2.5mV	-	0.5	-	A
			-27	-	**27**	%
		V_{CSOP} - V_{CSON} = 1.28mV	-	0.256	-	A
			-52	-	**52**	%
ASGATE Clamp						
VADP - VASGATE ON	-	-	-	10	-	V
VADP - VASGATE OFF	-	-	-	0	-	V

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
AMON/BMON						
Input Current Sense Amplifier, R_{s1} = 10mΩ						
CSIP/CSIN Input Voltage Range	-	-	**4**	-	**54**	V
Forward AMON Gain	-	-	-	17.97	-	V/V
Forward AMON Accuracy V_{AMON} = 17.97 x (V_{CSIP} - V_{CSIN})	-	V_{CSIP} - V_{CSIN} = 50mV (5A), CSIP = 5V, 28V, 48V	**-2.8**	-	**2.8**	%
		V_{CSIP} - V_{CSIN} = 30mV (3A), V_{CSIP} = 5V, 28V, 48V	**-5**	-	**5**	%
		V_{CSIP} - V_{CSIN} = 10mV (1A), V_{CSIP} = 5V, 28V, 48V	**-10**	-	**10**	%
		V_{CSIP} - V_{CSIN} = 5mV (0.5A), V_{CSIP} = 5V, 28V, 48V	**-16.8**		**16.8**	%
		V_{CSIP} - V_{CSIN} = 1mV (0.1A), V_{CSIP} = 5V, 28V, 48V	**-78.8**	-	**78.8**	%
Reverse AMON Gain	-	-	-	17.9	-	V/V
Reverse AMON Accuracy V_{AMON} = 17.9 x (V_{CSIP} - V_{CSIN})	-	V_{CSIN} - V_{CSIP} = 50mV (5A), V_{CSIP} = 5V, 28V, 48V	**-5**	-	**5**	%
		V_{CSIN} - V_{CSIP} = 40mV (4A), V_{CSIP} = 5V, 28V, 48V	**-6**	-	**6**	%
		V_{CSIN} - V_{CSIP} = 30mV (3A), V_{CSIP} = 5V, 28V, 48V	**-7**	-	**7**	%
		V_{CSIN} - V_{CSIP} = 10mV (1A), V_{CSIP} = 5V, 28V, 48V	**-18**	-	**18**	%
		V_{CSIN} - V_{CSIP} = 5mV (0.5A), V_{CSIP} = 5V, 28V, 48V	**-35**	-	**35**	%
		V_{CSIN} - V_{CSIP} = 2.56mV (0.256A), CSIP = 5V, 28V, 48V	**-70**	-	**70**	%
AMON Minimum Output Voltage	-	V_{CSIP} - V_{CSIN} = 0V	-	-	**30**	mV
Output Current Sense Amplifier, R_{s2} = 5mΩ						
Reverse BMON Gain	-	-	-	17.97	-	V/V
BMON Accuracy V_{BMON} = 17.97× (V_{CSON} - V_{CSOP})	-	V_{CSON} - V_{CSOP} = 50mV (10A), V_{CSON} = 8V, 29.4V, 50.4V	**-3.5**	-	**5**	%
		V_{CSON} - V_{CSOP} = 25mV (5A), V_{CSON} = 8V, 29.4V, 50.4V	**-5**	-	**8**	%
		V_{CSON} - V_{CSOP} = 15mV (3A), V_{CSON} = 8V, 29.4V, 50.4V	**-8**	-	**12**	%
		V_{CSON} - V_{CSOP} = 10mV (2A), V_{CSON} = 8V, 29.4V, 50.4V	**-11.5**	-	**17**	%
		V_{CSON} - V_{CSOP} = 5mV (1A), V_{CSON} = 8V, 29.4V, 50.4V	**-23**	-	**34**	%
		V_{CSON} - V_{CSOP} = 3mV (0.6A), V_{CSON} = 8V, 29.4V, 50.4V	**-39**	-	**55**	%

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Current Sense Amplifier, R_{S2} = 5mΩ (Limits apply across the temperature range of 0°C to +85°C)						
Forward BMON Gain	-	-	-	35.78	-	V/V
BMON Accuracy V_{BMON} = 35.78 x (V_{CSOP} - V_{CSON})	-	V_{CSOP} - V_{CSON} = 30mV (6A), V_{CSON} = 8V, 29.4V, 50.4V	**-3.75**	-	**3.75**	%
		V_{CSOP} - V_{CSON} = 25mV (5A), V_{CSON} = 8V, 29.4V, 50.4V	**-4.25**	-	**4.25**	%
		V_{CSOP} - V_{CSON} = 20mV (4A), V_{CSON} = 8V, 29.4V, 50.4V	**-5**	-	**5**	%
		V_{CSOP} - V_{CSON} = 15mV (3A), V_{CSON} = 8V, 29.4V, 50.4V	**-6.5**	-	**6.5**	%
		V_{CSOP} - V_{CSON} = 5mV (1A), V_{CSON} = 8V, 29.4V, 50.4V	**-16**	-	**16**	%
		V_{CSOP} - V_{CSON} = 2.5mV (0.5A), V_{CSON} = 8V, 29.4V, 50.4V	**-30**	-	**30**	%
		V_{CSOP} - V_{CSON} = 1.28mV (0.256A), V_{CSON} = 8V, 29.4V, 50.4V	**-60**	-	**60**	%
BMON Minimum Output Voltage	-	V_{CSOP} - V_{CSON} = 0V	-	-	**31**	mV
AMON/BMON Source Resistance[2]	-	-	-	-	**5**	Ω
AMON/BMON Sink Resistance[2]	-	-	-	-	**5**	Ω
OTGEN						
High-Level Input Voltage	-	-	**0.9**	-	-	V
Low-Level Input Voltage	-	-	-	-	**0.4**	V
Pull-Down Current	-	OTGEN = 5V	-	5	-	µA
OTG						
OTG Voltage	-	OTGVoltage register = 5.004V	**4.9**	5.03	**5.15**	V
OTG Current	-	OTGCurrent register = 512mA, (OTGVoltage = 5.004V, 28.008V, 48.024V)	**350**	512	**690**	mA
		OTGCurrent register = 1024mA, (OTGVoltage = 5.004V, 28.008V, 48.024V)	**870**	1024	**1200**	mA
		OTGCurrent register = 1536mA, (OTGVoltage = 5.004V, 28.008V, 48.024V)	**1370**	1536	**1726**	mA
		OTGCurrent register = 3072mA, (OTGVoltage = 5.004V, 28.008V, 48.024V)	**2841**	3072	**3314**	mA
		OTGCurrent register = 4096mA, (OTGVoltage = 5.004V, 28.008V, 48.024V)	**3858**	4096	**4350**	mA
		OTGCurrent register = 5024mA, (OTGVoltage = 5.004V, 28.008V, 48.024V)	**4750**	5024	**5300**	mA
General Purpose Comparator						
General Purpose Comparator Rising Threshold	-	Reference = 1.2V	**1.15**	1.24	**1.33**	V
		Reference = 2V	**1.93**	2	**2.05**	V
General Purpose Comparator Hysteresis	-	Reference = 1.2V	-	55	-	mV
		Reference = 2V	-	55	-	mV

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Protection						
VOUT Absolute Overvoltage	-	Control3 Register bit [10:9] = 00, rising	56.9	57.6	58.3	V
		Control3 Register bit [10:9] = 00, hysteresis	-	525	-	mV
		Control3 Register bit [10:9] = 01, rising	44.9	45.6	46.3	V
		Control3 Register bit [10:9] = 01, hysteresis	-	510	-	mV
		Control3 Register bit [10:9] = 10, rising	32.9	33.6	34.3	V
		Control3 Register bit [10:9] = 10, hysteresis	-	500	-	mV
		Control3 Register bit [10:9] = 11, rising	23.3	24	24.7	V
		Control3 Register bit [10:9] = 11, hysteresis	-	490	-	mV
VOUT Relative Overvoltage Rising Threshold	-	OutputVoltage register value = 8.4V	**9.4**	10	**10.5**	V
		OutputVoltage register value = 29.4V	**30.2**	31	**31.7**	V
		OutputVoltage register value = 50.4V	**51.2**	52	**52.9**	V
VOUT Relative Overvoltage Hysteresis	-	OutputVoltage register value = 8.4V	**550**	800	**1045**	mV
		OutputVoltage register value = 29.4V	**600**	800	**1000**	mV
		OutputVoltage register value = 50.4V	**550**	800	**1050**	mV
VR PGOOD UV	-	OutputVoltage register value = 8.4V, falling	-	6.8	-	V
		OutputVoltage register value = 8.4V, hysteresis	-	780	-	mV
		OutputVoltage register value = 29.4V, falling	-	27.8	-	V
		OutputVoltage register value = 29.4V, hysteresis	-	800	-	mV
		OutputVoltage register value = 50.4V, falling	-	48.8	-	V
		OutputVoltage register value = 50.4V, hysteresis	-	830	-	mV
VOUT UV Falling Threshold	-	Control6 register Bit[2:0] = 001	-	3	-	V
		Control6 register Bit[2:0] = 010	-	3.9	-	V
		Control6 register Bit[2:0] = 011	-	4.8	-	V
		Control6 register Bit[2:0] = 100	-	5.7	-	V
		Control6 register Bit[2:0] = 101	-	6.6	-	V
		Control6 register Bit[2:0] = 110	-	7.5	-	V
		Control6 register Bit[2:0] = 111	-	8.4	-	V
VOUT OK Threshold	-	-	**0.45**	0.6	**0.75**	V
VOUT OK Source Current	-	-	-	10	-	mA
Over-Temperature Threshold[2]	-	-	**140**	150	**160**	°C
Adapter Overvoltage Rising Threshold	-	-	**56.6**	57.6	**58.8**	V
Adapter Overvoltage Hysteresis	-	-	**390**	550	**760**	mV
OTG Undervoltage Falling Threshold	-	OTG voltage = 5.004V, 28.008V, 48.024V	**1.3**	1.8	**2.3**	V
OTG Undervoltage Rising Hysteresis	-	OTG voltage = 5.004V, 28.008V, 48.024V	-	0.9	-	V
OTG Overvoltage Rising Threshold	-	OTG voltage = 5.004V, 28.008V, 48.024V	**1.3**	1.8	**2.3**	V

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
OTG Overvoltage Falling Hysteresis	-	OTG voltage = 5.004V, 28.008V, 48.024V	-	0.9	-	V
Adapter Way Overcurrent Rising Threshold	-	Rs1 = 10mΩ	22.3	23.1	23.9	V
Oscillator						
Oscillator Frequency, Digital Core Only	-	-	**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy[2]	-	-	**-15**	-	**15**	%
Miscellaneous						
Switching Frequency Accuracy	-	COMP > 1.7V and not in period stretching	**-15**	-	**15**	%
ADP Discharge Current	-	ADP = 5V to 54V	-	10	-	mA
VOUT Discharge Current	-	VOUT = 5V to 54V	-	10	-	mA
SMBus						
SDA/SCL Input Low Voltage	-	-	-	-	**0.6**	V
SDA/SCL Input High Voltage	-	-	**1.3**	-	-	V
SDA/SCL Input Bias Current	-	-	-	-	**1**	µA
SDA, Output Sink Current	-	SDA = 0.4V	**4**	-	-	mA
SMBus Frequency	f_{SMB}	-	**10**	-	**400**	kHz
Gate Driver[2]						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current	-	800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2	-	A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current	-	350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8	-	A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current	-	800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2	-	A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current	-	300	**475**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5	-	A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current	-	800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2	-	A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current	-	300	**475**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5	-	A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current	-	800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2	-	A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current	-	350	**475**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**1.9**	2.8	-	A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$	-	**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$	-	**10**	20	**40**	ns

Operating conditions: ADP = CSIP = CSIN = 5V, 28V, and 48V, VOUTS1 = VOUTS2 = CSOP = CSON = 8V, 29.4V, and 50.4V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$	-	**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$	-	**10**	20	**40**	ns

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Values or limits established by characterization and are not production tested.

3.5 SMBus Timing Specification

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
SMBus Frequency	F_{SMB}	-	10	-	400	kHz
Bus Free Time	t_{BUF}	-	4.7	-	-	µs
Start Condition Hold Time from SCL	$t_{HD:STA}$	-	4	-	-	µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$	-	4.7	-	-	µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$	-	4	-	-	µs
SDA Hold Time from SCL	$t_{HD:DAT}$	-	300	-	-	ns
SDA Set-Up Time from SCL	$t_{SU:DAT}$	-	250	-	-	ns
SCL Low Period	t_{LOW}	-	4.7	-	-	µs
SCL High Period	t_{HIGH}	-	4	-	-	µs

1. Limits established by characterization and are not production tested.

3.6 Gate Driver Timing Diagrams

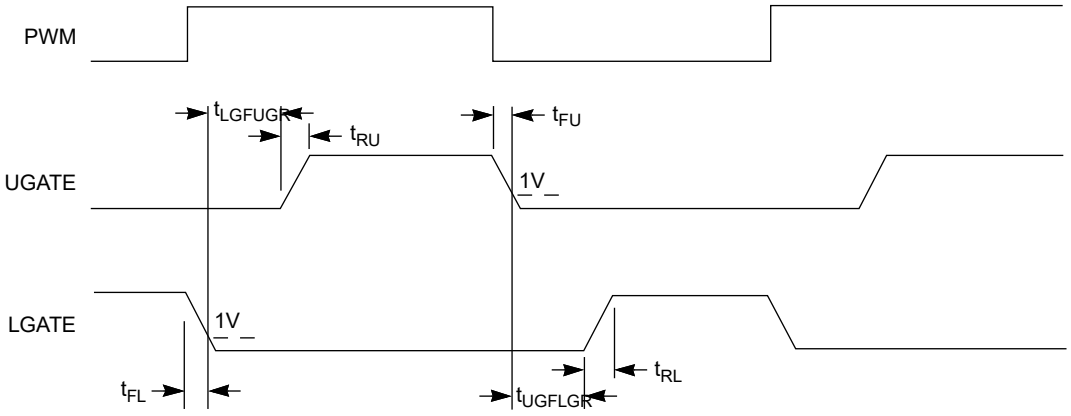


Figure 6. Gate Driver Timing Diagram

4. Typical Performance

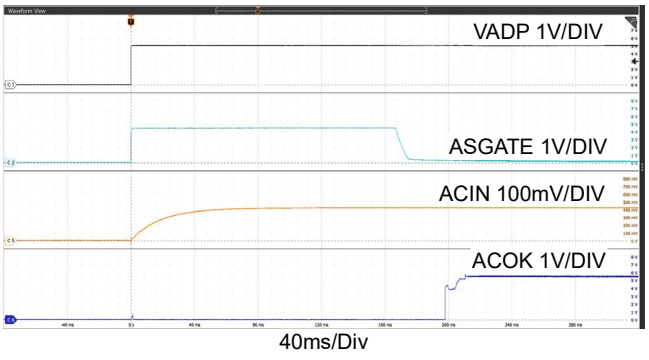


Figure 7. Adapter Insertion, V_{ADP}: 0V → 5V, V_{OUT} = 48V

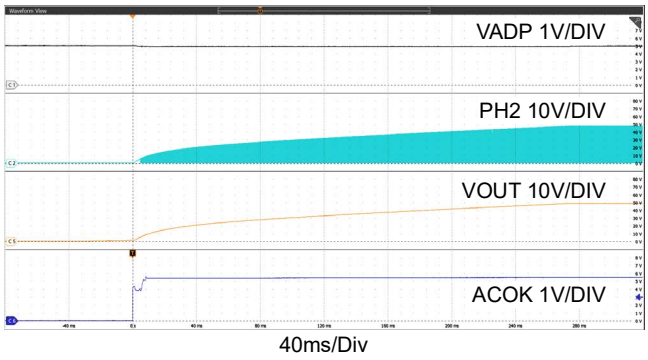


Figure 8. Adapter Insertion, V_{ADP}: 0V → 5V, V_{OUT} = 48V, (Continuation of Figure 7)

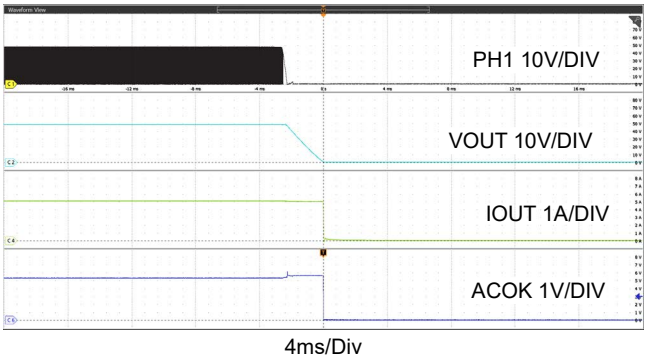


Figure 9. Adapter Removal, V_{ADP}: 48V → 0V, V_{OUT} = 48V, Load = 5A

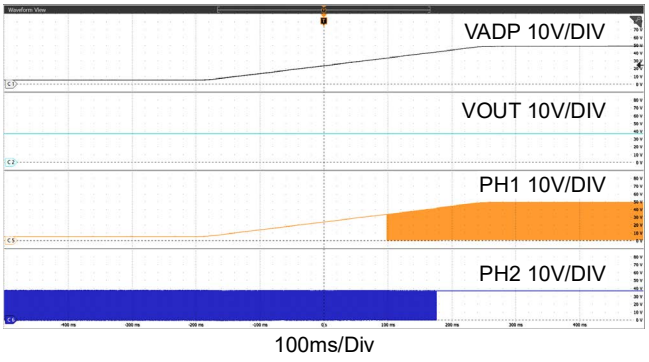


Figure 10. Adapter Voltage Ramp Up, Boost → Buck-Boost → Buck Operation Mode Transitions

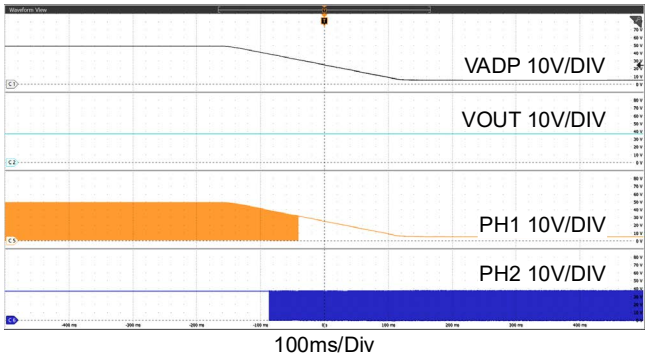


Figure 11. Adapter Voltage Ramp Down, Buck → Buck-Boost → Boost Operation Mode Transitions

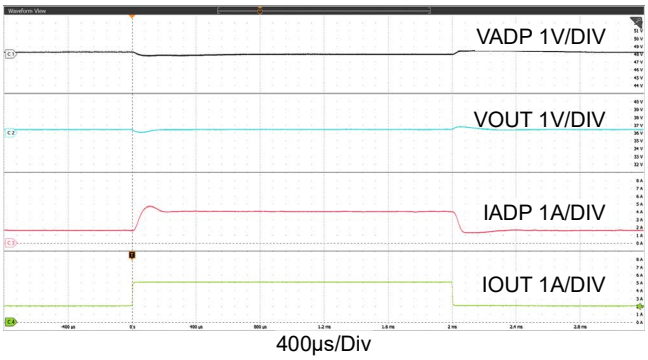


Figure 12. Buck Mode: Output Voltage Loop Load Transient, V_{ADP} = 48V, V_{OUT} = 36V, Load: 2A ↔ 5A

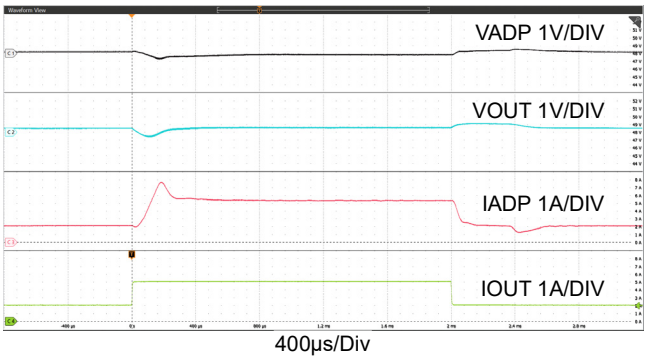


Figure 13. Buck-Boost Mode: Output Voltage Loop Load Transient, V_{ADP} = 48V, V_{OUT} = 48V, Load: 2A ↔ 5A

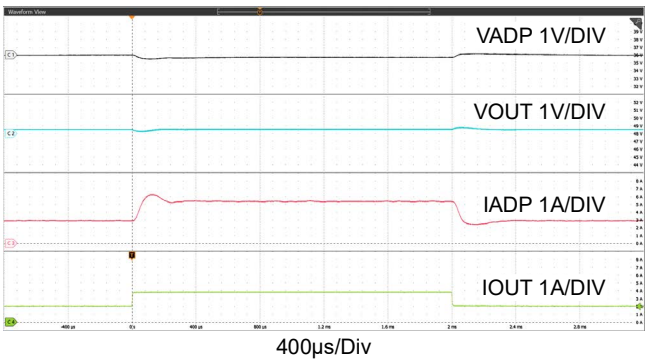


Figure 14. Boost Mode: Output Voltage Loop Load Transient, V_{ADP} = 36V, V_{OUT} = 48V, Load: 2A ↔ 3.75A

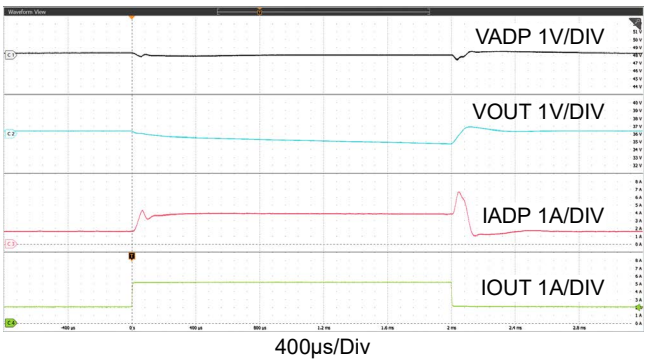


Figure 15. Buck Mode: Output Voltage Loop ↔ Output Current Loop, V_{ADP} = 48V, V_{OUT} = 36V, OutputCurrentLimit = 5A, Load: 2A ↔ 5.1A

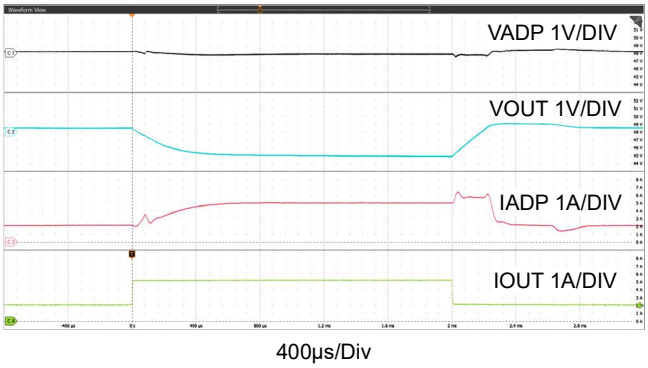


Figure 16. Buck-Boost Mode: Output Voltage Loop ↔ Output Current Loop, V_{ADP} = 48V, V_{OUT} = 48V, OutputCurrentLimit = 5A, Load: 2A ↔ 5.1A

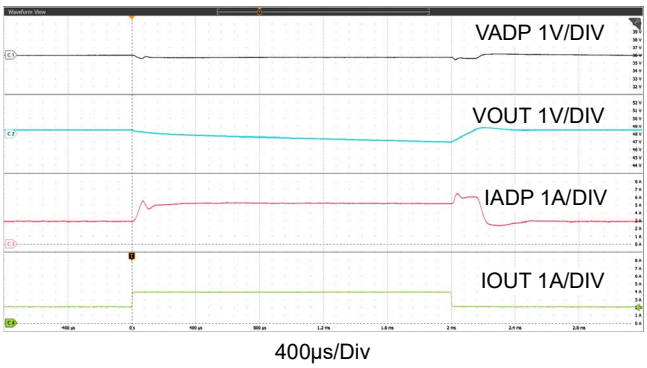


Figure 17. Boost Mode: Output Voltage Loop ↔ Output Current Loop, V_{ADP} = 36V, V_{OUT} = 48V, OutputCurrentLimit = 3.75A, Load: 2A ↔ 3.85A

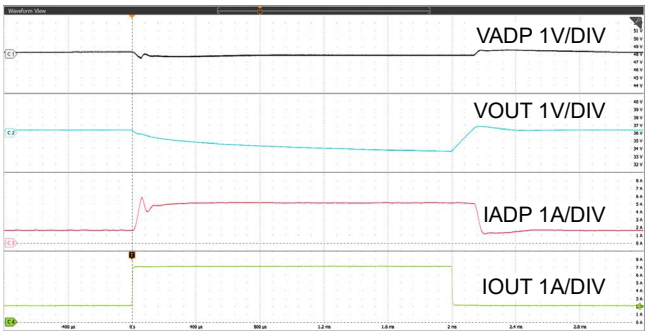


Figure 18. Buck Mode: Output Voltage Loop ↔ Input Current Loop, V_{ADP} = 48V, V_{OUT} = 36V, AdapterCurrentLimit = 5A, Load: 2A ↔ 7A

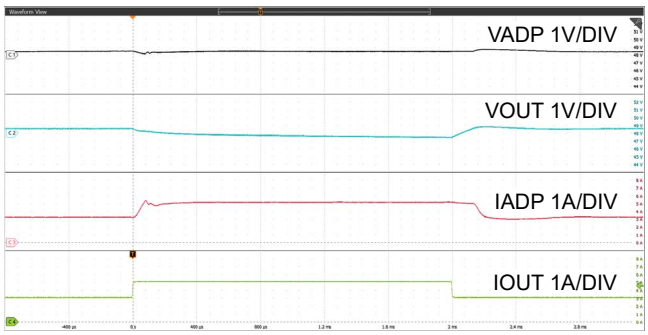


Figure 19. Buck-Boost Mode: Output Voltage Loop ↔ Input Current Loop, V_{ADP} = 48V, V_{OUT} = 48V, AdapterCurrentLimit = 5A, Load: 3A ↔ 5A

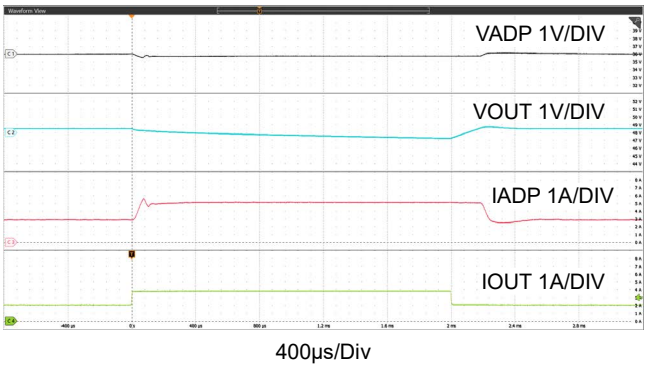


Figure 20. Boost Mode: Output Voltage Loop ↔ Input Current Loop, V_{ADP} = 36V, V_{OUT} = 48V, AdapterCurrentLimit = 5A, Load: 2A ↔ 3.75A

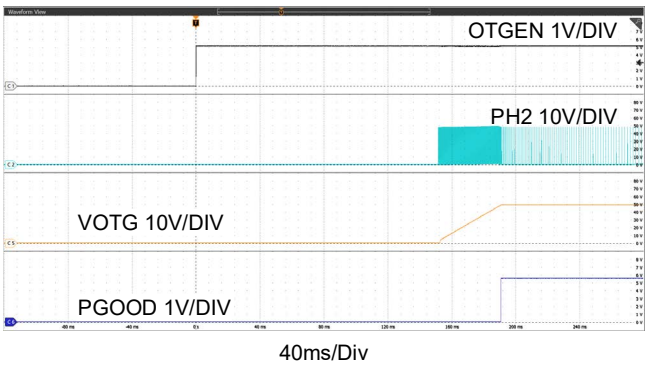


Figure 21. OTG Mode Enable, OTG_Debounce = 150ms, V_{OUT} = 48V, V_{OTG} = 48V

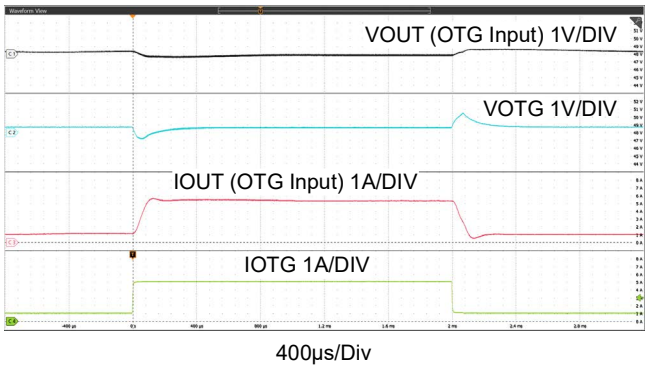


Figure 22. OTG Mode Transients, V_{OUT} = 48V, V_{OTG} = 48V, OTG Load: 1A ↔ 5A

Note: The performance waveforms were captured using the default switching frequency of 723kHz.

5. General SMBus Architecture

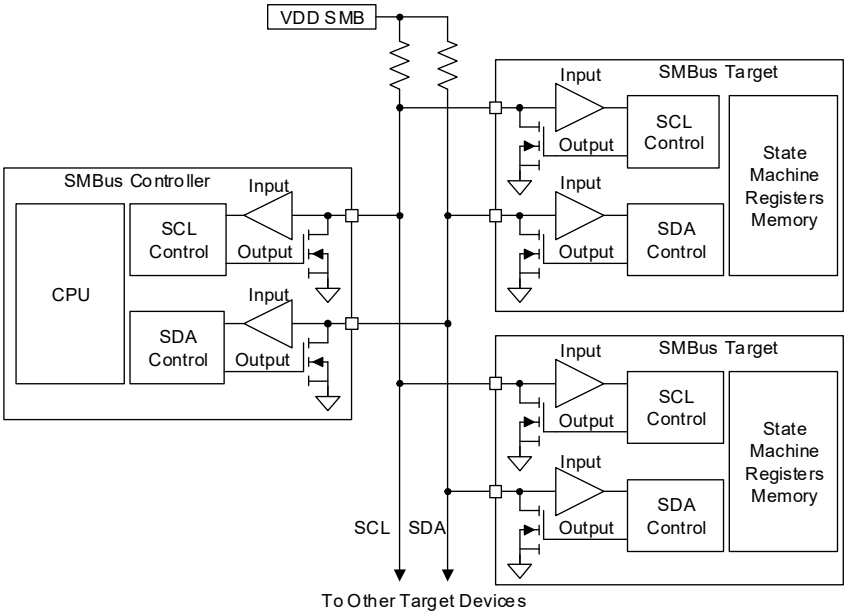


Figure 23. General SMBus

5.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 24.

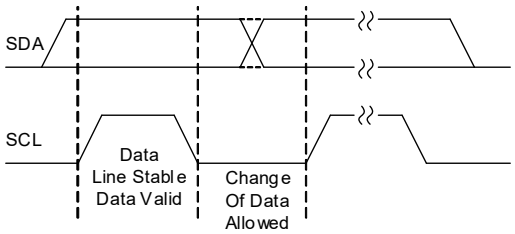


Figure 24. Data Validity

5.2 START and STOP Conditions

In Figure 25, the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

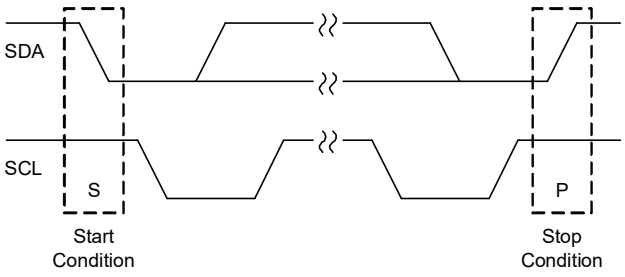


Figure 25. Start and Stop Waveforms

5.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the SMBus controller sends seven target address bits and a R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line LOW to acknowledge (see Figure 26). Both the SMBus controller and the target use the ACK bit to acknowledge receipt of register addresses and data.

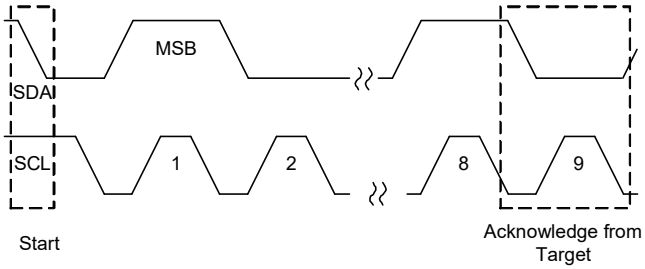


Figure 26. Acknowledge On The SMBus

5.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus controller device. The control byte begins with a Start condition followed by seven bits of target address (0001001) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any target device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line LOW for the last clock cycle in the control byte. If no target exists at that address or the target is not ready to communicate, the data line remains high indicating a not acknowledged condition.

When the control byte is sent and the RRB86848 acknowledges it, the second byte sent by the SMBus controller must be a register address byte such as 0x14 for the OutputCurrent register. The register address byte tells the RRB86848 which register the SMBus controller writes or reads. See Table 1 for register details. When the RRB86848 receives a register address byte, it responds with an acknowledge.

5.5 Byte Format

Every byte on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO Byte data is transferred before the HI Byte data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

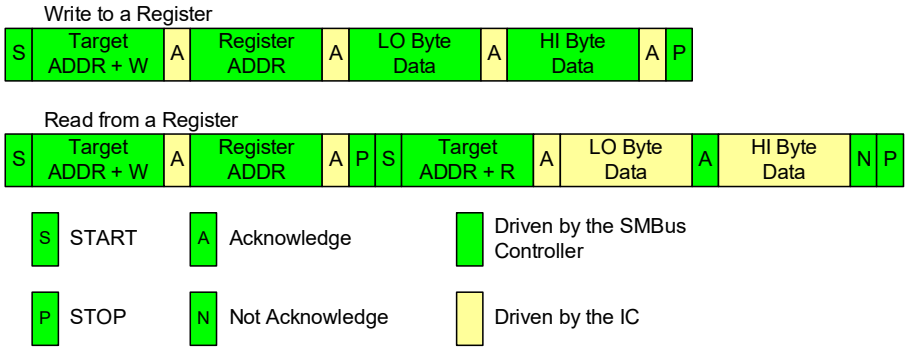


Figure 27. SMBus Read and Write Protocol

5.6 SMBus and I²C Compatibility

The RRB86848 SMBus minimum input logic high voltage is 1.3V, so it is compatible with I²C with pull-up power supplies higher than 1.3V.

The RRB86848 SMBus registers are 16 bits, so it is compatible with 16-bit I²C or 8-bit I²C with auto-increment capability.

5.7 SMBus Commands

The RRB86848 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification. The RRB86848 uses the SMBus Read-word and Write-word protocols (see Figure 27) to communicate with the host system or a smart battery. RRB86848 is an SMBus target device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ as follows:

The Read and Write address for RRB86848 is:

- Read address = 0b00010011 (0X13H)
- Write address = 0b00010010 (0X12H)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Select pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

6. Registers

The following register descriptions are based on current-sensing resistors R_{s1} = 10mΩ and R_{s2} = 5mΩ, unless otherwise specified.

6.1 Register Summary

Table 1. Register Summary

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
OutputCurrentLimit	0x14	R/W	11	[12:2], LSB size 8mA	0.48A, 2.848A, or 4.752A (Set by PROG pin)
OutputVoltage	0x15	R/W	12	[14:3], LSB size 16mV (values ≤ 24.576V) 32mV (values ≥ 24.608V)	5.008V 28V 9.008V 36V 15.008V 48V 20V (Set by PROG pin)
Control7	0x36	R/W	4	[15], [3:2], [0], configures various converter options	0x0000
Control6	0x37	R/W	7	[6:0], configures various converter options	0x0040 or 0x0043[1]
Control5	0x38	R/W	14	[15:14], [11:0], configures various converter options	0x0000
Control0	0x39	R/W	14	[15:5], [2:0], configures various converter options	0x0080
Information1	0x3A	R	3	[15:13], indicates various converter statuses	0x0000
AdapterCurrentLimit2	0x3B	R/W	11	[12:2], LSB size 8mA	1.504A
Control1	0x3C	R/W	9	[15:14], [11:8], [5:4], [2], configures various converter options	0x0200
Control2	0x3D	R/W	12	[13:11], [8:0], configures various converter options	0x0000
AdapterCurrentLimit1	0x3F	R/W	11	[12:2], LSB size 8mA	0.48A, 2.848A, or 4.752A (Set by PROG pin)
Revision ID	0x44	R	8	Revision ID register - Read only	0x00
OTG Voltage	0x49	R/W	12	[14:3], LSB size 18mV (values ≤ 27.504V) 36mV (values ≥ 27.540V), OTG mode voltage reference	5.004V
OTG Current	0x4A	R/W	9	[12:4], LSB size 32mA, OTG mode maximum current limit	0.48A
V_{IN} Voltage	0x4B	R/W	7	[14:8] LSB size 512mV (values ≤ 16.384V) 1024mV (values ≥ 16.896V), V_{IN} loop voltage reference	4.096V
Control3	0x4C	R/W	11	[15], [12:9], [6:5], [3:0] configures various converter options	0x0080
Information2	0x4D	R	15	[15:13], [11:0], indicates various converter status	0x0000
Control4	0x4E	R/W	14	[15:8], [5:0], configures various converter options	0x0000
Information3	0x90	R	1	[1], indicates pass-through mode status	0x0000
Manufacturer ID	0xFE	R	8	Manufacturer ID register – 0x49 - Read only	0x0049
Device ID	0xFF	R	8	Device ID register - Read only	0x001A

1. The default value for the VOUT UV depends on whether powering up from the adapter side or from the VOUT side.

6.2 DAC Register Summary

Table 2. DAC Summary Table[1]

ADDR Bit	Output Current Limit (R_{S2} = 5mΩ)	Output Voltage		Adapter Current Limit1 (R_{S1} = 10mΩ)	Adapter Current Limit2 (R_{S1} = 10mΩ)	V_{IN} Voltage (FWD VADP Min or OTG Input Voltage Min)		OTG Voltage		OTG Current (R_{S1} = 10mΩ)
		Value ≤ 24.576V	Value ≥ 24.608V			Value ≤ 16.384V	Value ≥ 16.896V	Value ≤ 27.504V	Value ≥ 27.540V	
	0x14	0x15		0x3F	0x3B	0x4B		0x49		0x4A
[0]	-	-	-	-	-	-	-	-	-	-
[1]	-	-	-	-	-	-	-	-	-	-
[2]	8mA	-	-	8mA	8mA	-	-	-	-	-
[3]	16mA	16mV	-	16mA	16mA	-	-	18mV	-	-
[4]	32mA	32mV	32mV	32mA	32mA	-	-	36mV	36mV	32mA
[5]	64mA	64mV	64mV	64mA	64mA	-	-	72mV	72mV	64mA
[6]	128mA	128mV	128mV	128mA	128mA	-	-	144mV	144mV	128mA
[7]	256mA	256mV	256mV	256mA	256mA	-	-	288mV	288mV	256mA
[8]	512mA	512mV	512mV	512mA	512mA	512mV	-	576mV	576mV	512mA
[9]	1024mA	1024mV	1024mV	1024mA	1024mA	1024mV	1024mV	1152mV	1152mV	1024mA
[10]	2048mA	2048mV	2048mV	2048mA	2048mA	2048mV	2048mV	2304mV	2304mV	2048mA
[11]	4096mA	4096mV	4096mV	4096mA	4096mA	4096mV	4096mV	4608mV	4608mV	4096mA
[12]	8192mA	8192mV	8192mV	8192mA	8192mA	8192mV	8192mV	9216mV	9216mV	8192mA
[13]	-	16384mV	16384mV	-	-	16384mV	16384mV	18432mV	18432mV	-
[14]	-	-	32768mV	-	-	-	32768mV	-	36864mV	-
[15]	-	-	-	-	-	-	-	-	-	-
Max	12.16A (0x17C0)	54.912V (0x6B40)		12.16A (0x17C0)	12.16A (0x17C0)	47.104mV (0x5C00)		55.26V (0x5FF0)		8.192A (0x1000)
Default	Set by PROG pin	Set by PROG pin		Set by PROG pin	1.504A (0x02F0)	4.096V (0x0800)		5.004V (0x08B0)		0.48A (0x00F0)

1. Each of the DAC registers accepts any value, but only the valid register bits are written to the register, and the voltage or current value is clamped at the indicated maximum. The RRB86848 accepts a 0V command for the OutputVoltage register, but the register value does not change.

6.3 Control Registers

The Control registers configure the operation of RRB86848. To change the configuration after a POR, write to the appropriate control registers using the Write-word protocol shown in Figure 27.

Table 3. Control0 Register 0x39H

Bit	Bit Name	Description
[15:13]	Forward Buck Phase Comparator Threshold Offset	Bits[15:13] adjust the phase comparator threshold offset for the forward buck mode. 000 = 0mV (default) 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[12:10]	Forward Buck-boost, Forward Boost, and Reverse Boost Phase Comparator Threshold Offset	Bits[12:10] adjust the phase comparator threshold offset for the forward buck-boost, forward boost, and reverse boost modes. 000 = 0mV (default) 001 = 0.5mV 010 = 1mV 011 = 1.5mV 100 = -2mV 101 = -1.5mV 110 = -1mV 111 = -0.5mV
[9,8,0]	Reverse Buck and Reverse Buck-boost Phase Comparator Threshold Offset	Bits[9,8,0] adjust the phase comparator threshold offset for the reverse buck and reverse buck-boost modes. 000 = 0mV (default) 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[7]	SMBus Timeout	Bit[7] enables or disables the output current limit timeout function. If the timeout expires, output current limiting is disabled. Renesas recommends leaving the timeout function in its default (disabled) state. 0 = Enable the SMBus timeout function 1 = Disable the SMBus timeout function (default)
[6:5]	High-Side FET Short Detection Threshold	Bits[6:5] configure the high-side FET short detection phase node voltage threshold while the low-side FET turns on. 00 = 800mV (default) 01 = 500mV 10 = 600mV 11 = 400mV
[4:3]	Unused	-
[2]	Input Voltage Regulation Loop	Bit[2] enables or disables the input voltage regulation loop. 0 = Enable the input voltage regulation loop (default) 1 = Disable the input voltage regulation loop
[1]	Force Buck Mode	Bit[1] enables or disables Force Buck mode. If the Force Buck mode bit is enabled, the Buck-Boost window narrows. 0 = Disable Force Buck mode (default) 1 = Enable Force Buck mode

Table 4. Control1 Register 0x3CH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[15:14]</td><td>General Purpose Comparator Assertion Debounce Time</td><td>Bits[15:14] configure the general-purpose comparator assertion debounce time.
00 = 2µs (default)
01 = 12µs
10 = 2ms
11 = 5s</td></tr>
<tr><td>[13]</td><td>Unused</td><td>-</td></tr>
<tr><td>[12]</td><td>Reserved</td><td>Must remain in default state of 0. If Control1 register is written, ensure this bit is written as a 0.</td></tr>
<tr><td>[11]</td><td>OTG Function</td><td>Bit[11] enables or disables the OTG function.
0 = Disable the OTG function (default)
1 = Enable the OTG function</td></tr>
<tr><td>[10]</td><td>Audio Filter</td><td>Bit[10] enables or disables the audio filter function.
0 = Disable the audio filter function (default)
1 = Enable the audio filter function</td></tr>
<tr><td>[9:8]</td><td>Switching Frequency</td><td>Control1 Bits[9:8] and Control4 Bit[11] configure the switching frequency.
<table>
<tr><th>Control4[11]</th><th>Control1[9:8]</th><th>Switching Frequency</th></tr>
<tr><td>0</td><td>00</td><td>948kHz</td></tr>
<tr><td>0</td><td>01</td><td>817kHz</td></tr>
<tr><td>0</td><td>10</td><td>723kHz (default)</td></tr>
<tr><td>0</td><td>11</td><td>646kHz</td></tr>
<tr><td>1</td><td>00</td><td>592kHz</td></tr>
<tr><td>1</td><td>01</td><td>495kHz</td></tr>
<tr><td>1</td><td>10</td><td>429kHz</td></tr>
<tr><td>1</td><td>11</td><td>377kHz (recommended)</td></tr>
</table></td></tr>
<tr><td>[7:6]</td><td>Unused</td><td>-</td></tr>
<tr><td>[5]</td><td>AMON/BMON Function</td><td>Bit[5] enables or disables the current monitor function AMON and BMON.
0 = Enable AMON/BMON (default)
1 = Disable AMON/BMON
Bit[5] is only relevant when no adapter is attached, power is applied at VOUT, and OTG is disabled, or when an adapter is attached, and Forward Sleep mode is enabled. In active switching modes (Forward or Reverse), AMON/BMON is automatically enabled, regardless of the state of Bit[5].</td></tr>
<tr><td>[4]</td><td>AMON or BMON</td><td>Bit[4] selects AMON or BMON as the AMON/BMON pin output.
0 = AMON (default)
1 = BMON</td></tr>
<tr><td>[3]</td><td>Unused</td><td>-</td></tr>
<tr><td>[2]</td><td>VOUT</td><td>Bit[2] enables or disables the buck-boost converter switching VOUT output. When disabled, the RRB86848 stops switching.
0 = Enables VOUT output (default)
1 = Disables VOUT output</td></tr>
<tr><td>[1:0]</td><td>Unused</td><td>-</td></tr>
</table>

Table 5. Control2 Register 0x3DH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[15:14]</td><td>Unused</td><td>-</td></tr>
<tr><td>[13]</td><td>OTG Function Enable Debounce Time</td><td>Control2 Bit[13] and Control 3 Bit[0] configure the OTG function debounce time from when the RRB86848 receives the OTG enable command until OTG switching begins.
<table>
<tr><th>Control2[13]</th><th>Control3[0]</th><th>OTG Start-Up Delay</th></tr>
<tr><td>0 (default)</td><td>0 (default)</td><td rowspan="2">1.3s</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>150ms</td></tr>
<tr><td>1</td><td>1</td><td>7.5ms</td></tr>
</table></td></tr>
<tr><td>[12]</td><td>Two-Level Adapter Current Limit Function</td><td>Bit[12] enables or disables the two-level adapter current limit function.
0 = Disables the two-level current limit function (default)
1 = Enables the two-level current limit function</td></tr>
<tr><td>[11]</td><td>Adapter Insertion to Switching Debounce</td><td>Bit[11] configures the debounce time from adapter insertion to when ACOK is asserted high.
0 = 1.3s (default)
1 = 150ms
After VDD POR, for the first time the adapter is plugged in, the ASGATE turn-on delay is always 150ms, regardless of the Bit[11] setting. This bit sets the ASGATE turn-on delay only after ASGATE turns off at least one time when VDD is above its POR value. The Bit[11] default is 0, corresponding to 1.3s.</td></tr>
<tr><td>[10:9]</td><td>Unused</td><td>-</td></tr>
<tr><td>[8:6]</td><td>ALERT# Duration</td><td>Bits[8:6] configure the minimum duration of the ALERT# signal when asserted.
000 = 10ms (default)
001 = 20ms
010 = 15ms
011 = 5ms
100 = 1ms
101 = 500µs
110 = 100µs
111 = 0s</td></tr>
<tr><td>[5]</td><td>ASGATE in OTG Mode</td><td>Bit[5] turns the ASGATE FET on or off in OTG mode.
0 = Turn on ASGATE in OTG mode (default)
1 = Turn off ASGATE in OTG mode</td></tr>
<tr><td>[4]</td><td>CMIN Reference</td><td>Bit[4] configures the general-purpose comparator reference voltage.
0 = 1.2V (default)
1 = 2V
Note: The 2V CMIN reference is not available in forward or reverse sleep modes.</td></tr>
<tr><td>[3]</td><td>General Purpose Comparator</td><td>Bit[3] enables or disables the general-purpose comparator.
0 = Enable the general-purpose comparator (default)
1 = Disable the general-purpose comparator</td></tr>
<tr><td>[2]</td><td>CMOUT Polarity</td><td>Bit[2] configures the general-purpose comparator output polarity when asserted. The comparator reference voltage is connected to the inverting input node.
0 = CMOUT is High when CMIN is higher than reference (default)
1 = CMOUT is Low when CMIN is higher than reference</td></tr>
<tr><td>[1:0]</td><td>Pass-Through Mode</td><td>Bit[1:0] configures the Pass-Through Mode (PTM).
00 = Disable normal PTM and forced PTM (default)
01 = Enable normal PTM
10 = Unused
11 = Enable forced PTM</td></tr>
</table>

Table 6. Control3 Register 0x4CH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[15]</td><td>Reread PROG Pin Resistor</td><td>Bit[15] specifies whether to reread the PROG pin resistor.
0 = Reread PROG pin resistor (default)
1 = Do not reread PROG pin resistor</td></tr>
<tr><td>[14]</td><td>Reserved</td><td>Must remain in default state of 0. If Control3 register is written, ensure this bit is written as a 0.</td></tr>
<tr><td>[13]</td><td>Unused</td><td>-</td></tr>
<tr><td>[12:11]</td><td>Output Current Limit Timeout</td><td>Bits[12:11] configure the SMBus output current limit timeout time.
00 = 175s (default)
01 = 87.5s
10 = 43.75s
11 = 5s
Note: This parameter is only relevant if the SMBus timeout function, as described in Control 0 Bit[7], is enabled.</td></tr>
<tr><td>[10:9]</td><td>VOUT Absolute Overvoltage</td><td>Bits[10:9] set the VOUT absolute overvoltage threshold:
00: 57.6V (default)
01: 45.6V
10: 33.6V
11: 24V</td></tr>
<tr><td>[8]</td><td>Unused</td><td>-</td></tr>
<tr><td>[7]</td><td>Reserved</td><td>Important: Must remain in default state of 1. If Control3 register is written, ensure this bit is written as a 1.</td></tr>
<tr><td>[6]</td><td>AC and CC Feedback Gain</td><td>Bit[6] configures AC and CC feedback gain for high current.
0 = x1 (default)
1 = x0.5</td></tr>
<tr><td>[5]</td><td>Adapter-Side Current Limit Loop</td><td>Bit[5] enables or disables the adapter-side current limit loops for forward and reverse/OTG modes.
0 = Enable adapter-side current limit loops (default)
1 = Disable adapter-side current limit loops</td></tr>
<tr><td>[4]</td><td>Unused</td><td>-</td></tr>
<tr><td>[3]</td><td>AMON/BMON Direction</td><td>Bit[3] configures the AMON/BMON direction.
0 = Adapter current monitor/forward output current monitor (default)
1 = OTG output current monitor/OTG input current monitor</td></tr>
<tr><td>[2]</td><td>Digital Reset</td><td>Bit[2] resets all SMBus registers to their POR default values.
0 = Idle (default)
1 = Reset</td></tr>
<tr><td>[1]</td><td>Buck-Boost Stretch CCM Period</td><td>Control3 Bit[1] and Control4 Bit[8] configure the Buck-Boost stretch CCM period (T2 time).
<table>
<tr><th>Control3[1]</th><th>Control4[8]</th><th>T2 Time</th></tr>
<tr><td>0</td><td>0</td><td>0.6x (default)</td></tr>
<tr><td>0</td><td>1</td><td>1x</td></tr>
<tr><td>1</td><td>0</td><td>3x</td></tr>
<tr><td>1</td><td>1</td><td>2x</td></tr>
</table></td></tr>
<tr><td>[0]</td><td>OTG Start-Up Delay</td><td>Refer to the description of Control2[13] in Table 5.</td></tr>
</table>

Table 7. Control4 Register 0x4EH

Bit	Bit Name	Description
[15:14]	Dither Enable	Bits[15:14] disable or select the switching frequency dithering function. 00 = Disable dither (default) 01 = Dither 100 - 102% 10 = Dither 100 - 104% 11 = Dither 100 - 106%
[13]	ADP Discharge	Bit[13] enables or disables the ADP discharge function. Typical 10mA. 0 = Disable ADP discharge function (default) 1 = Enable ADP discharge function
[12]	VOUT Sink	Bit[12] enables or disables the VOUT discharge function. Typical 10mA. 0 = Disable VOUT discharge function (default) 1 = Enable VOUT discharge function
[11]	Switching Frequency	Refer to the description of Control1 Bits[9:8] in Table 4.
[10]	Buck-Boost Min T3 Time	Bit[10] selects the minimum T3 time when in the buck-boost mode. 0 = Long (default) 1 = Short
[9]	Buck-Boost T2 time in DCM	Bit[9] selects the buck-boost T2 time in the discontinuous-conduction mode (DCM). 0 = Reduced T2 time (increases switching frequency in DCM) (default) 1 = Normal T2 time
[8]	Buck-Boost Stretch CCM Period	Refer to the description of Control3 Bit[1] in Table 6.
[7:6]	Unused	-
[5]	ACOK ALERT#	Bit[5] enables or disables ALERT# trigger with ACOK. 0 = Disable ALERT# trigger with ACOK (default) 1 = Enable ALERT# trigger with ACOK
[4]	Comparator ALERT#	Bit[4] enables or disables ALERT# trigger with General Purpose Comparator rising. 0 = Disable ALERT# trigger with General Purpose Comparator rising (default) 1 = Enable ALERT# trigger with General Purpose Comparator rising
[3:2]	ACOK ALERT# Falling Debounce	Bits[3:2] configure the debounce time from ACOK falling to ALERT# activation. 00 = 2µs (default) 01 = 25µs 10 = 125µs 11 = 250µs
[1]	ALERT# Clear	Bit[1] clears ALERT#. 0 = Idle (default) 1 = Clear ALERT#
[0]	ALERT# Latch	Bit[0] manually resets ALERT#. 0 = ALERT# signal auto-clear (default) 1 = Latch ALERT# low when tripped

Table 8. Control5 Register 0x38H

Bit	Bit Name	Descriptions
[15:14]	Internal Compensation Resistance	Bits[15:14] set the internal compensation resistance 00 = 1.26 KΩ (default) 01 = 773Ω 10 = 3.6 KΩ 11 = 1.88 KΩ
[13:12]	Unused	-
[11]	VOUT Regulation Loop in OTG Mode	Bit[11] enables or disables the VOUT (serving as the input) voltage regulation during OTG (reverse) mode. 0 = Disable (default) 1 = Enable

Table 8. Control5 Register 0x38H

Bit	Bit Name	Descriptions
[10:8]	Two-Level ACLIM T2 Time	Bits[10:8] set the T2 time corresponding to AdapterCurrentLimit2 when two-level adapter current limit function is enabled. 000 = 10μs (default) 001 = 100μs 010 = 500μs 011 = 1ms 100 = 300μs 101 = 750μs 110 = 2ms 111 = 10ms
[7]	VOUTOK 0.6V Comparator	Bit[7] enables or disables the 0.6V comparator. 0 = Enable (default) 1 = Disable
[6]	VOUTOK 10mA Current Source	Bit[6] enables or disables the 10mA current source. 0 = Enable (default) 1 = Disable
[5]	PGOOD/CMOUT Selection	Bit[5] selects the signal routed to the PGOOD/CMOUT pin. 0 = PGOOD (default) 1 = CMOUT
[4]	VOUTOV/OTGOV Control	Bit[4] enables or disables VOUT and OTG overvoltage protections. 0 = Enable (default) 1 = Disable
[3]	Forward Sleep Mode	Bit[3] disables or enables Forward Sleep Mode 0 = Disable (default) 1 = Enable
[2:0]	Two-Level ACLIM T1 Time	Bits[2:0] set the T1 time corresponding to AdapterCurrentLimit1 when two-level adapter current limit function is enabled. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms

Table 9. Control6 Register 0x37H

Bit	Bit Name	Description
[15:7]	Unused	-
[6]	Slew Rate Control for Output Current Limit, Output Voltage, and OTG Voltage	Bit[6] enables or disables the slew rate control for output current, output voltage, and OTG voltage. 0 = Disable the slew rate control 1 = Enable the slew rate control (default) Slew is limited to 1 DAC LSB per 16 clock cycles (1μs each). Nominal slew rates: 1mV/μs for output voltage, 0.5mA/μs for output current with R_{s2} = 5mΩ, and 1.125mV/μs for OTG voltage.
[5]	OTG Undervoltage Protection	Bit[5] enables or disables the OTG undervoltage protection 0 = Enable OTG undervoltage protection (default) 1 = Disable OTG undervoltage protection
[4]	Clear CMOUT Latch Data	Bit[4] clears the current CMOUT data when written to 1. The CMOUT latch data can be read from Bit[4] when Control6[3] = 0 (CMOUT Latch is enabled). 0 = Do not clear CMOUT latch data (default) 1 = Clear CMOUT latch data

Table 9. Control6 Register 0x37H

Bit	Bit Name	Description
[3]	CMOUT Latch	Bit[3] enables or disables the CMOUT latch function. 0 = Enable the CMOUT latch function (default) 1 = Disable the CMOUT latch function
[2:0]	VOUT Undervoltage Threshold	Bits[2:0] set VOUT under voltage threshold. 000: Disable (default when powering up from VOUT) 001: 3.0V (default after adapter insertion or VOUT undervoltage fault) 010: 3.9V 011: 4.8V 100: 5.7V 101: 6.6V 110: 7.5V 111: 8.4V *Note*: To prevent a VOUT UV fault from resetting the VOUT UV threshold to its default, disable PROG re-reading by setting Control register 3 Bit[15].

Table 10. Control7 Register 0x36H

Bit	Bit Name	Description
[15]	Force ASGATE OFF in Forward Mode	Bit[15] forces the ASGATE driver to turn off the ASFETs when in Forward Mode. 0 = Disable (default) 1 = Enable
[14:4]	Unused	-
[3]	High-Power LDO Output	Bit[3] sets the voltage level of the High-Power LDO 0 = 5V (default) 1 = 4.5V If an external regulator is used, the internal LDO should be set to the 4.5V level, so that the external regulator provides the power.
[2]	High-Power LDO disabled by OTP	Bit[2] disables the High-Power LDO when an over-temperature event is detected. 0 = Disable LDO on OTP (default) 1 = Do not disable LDO on OTP
[1]	Unused	-
[0]	VOUT ABS OV	VOUT absolute overvoltage protection 0 = Enable (default) 1 = Disable

6.4 Information Registers

The Information registers contain SMBus readable information about manufacturing and Operating modes. The following tables identify the bit locations of the available information.

Table 11. Information1 Register 0x3AH

Bit	Description
[15]	Bit[15] indicates whether the internal reference circuit is active. Bit[15] = 0 indicates that the RRB86848 is in a Low Power mode. 0 = Reference is not active 1 = Reference is active
[14:13]	Bits[14:13] indicate the active control loop. 00 = Output voltage control loop is active 01 = Output current loop is active 10 = Adapter current limit loop is active 11 = Input voltage loop is active
[12:0]	Unused

Table 12. Information2 Register 0x4DH

Bit	Description
[15]	Bit[15] indicates the state of pin 30 at POR. 0 = Pin30 detected as low at POR 1 = Pin30 detected as high at POR
[14]	Bit[14] indicates the ACOK pin status. 0 = No adapter 1 = Adapter is present
[13]	Bit[13] indicates the general-purpose comparator output after debounce time. 0 = Comparator output is low 1 = Comparator output is high
[12]	Unused
[11:8]	Bits[11:8] indicate the RRB86848 state machine status. 0000 = OFF 0001 = REV_SLP 0010 = ADAPTER 0011 = ACOK 0100 = VOUT 0101 = IOUT_LIM 0110 = ENOTG 0111 = OTG 1000 = ENLDO5 1001 = Not Applicable 1010 = TRIM/ENCHREF 1100 = CAL 1101 = AGON/AGONTG 1110 = WAIT
[7:5]	Bits[7:5] indicate the RRB86848 operation mode. 001 = Boost Mode 010 = Buck Mode 011 = Buck-Boost Mode 101 = OTG Boost Mode 110 = OTG Buck Mode 111 = OTG Buck-Boost Mode
[4:0]	Program Resister read out Output voltage Adapter current limit Output current limit

Table 13. Information3 Register 0x90H

Bit	Description
[15:2]	Unused
[1]	Bit[1] indicates the Pass-Through Mode (PTM) status. 0 = PTM is inactive 1 = PTM is active
[0]	Unused

7. Modulator Information

7.1 RRB86848 Buck-Boost Converter Modes of Operation

The RRB86848 buck-boost converter drives an external N-channel MOSFET bridge made of two transistor pairs as shown in Figure 28. The first pair, Q1 and Q2, is a buck arrangement with the transistor center tap connected to an inductor input as is the case with a buck converter. The second transistor pair, Q3 and Q4, is a boost arrangement with the transistor center tap connected to the output of the inductor as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the output voltage and boosting from a voltage input lower than the output voltage.

Table 14. Operation Mode

Mode	Q1	Q2	Q3	Q4
Buck	Control FET	Sync. FET	OFF	ON
Boost	ON	OFF	Control FET	Sync. FET
Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
OTG Buck	ON	OFF	Sync. FET	Control FET
OTG Boost	Sync. FET	Control FET	OFF	ON
OTG Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET
Pass-Through	ON	OFF	OFF	ON

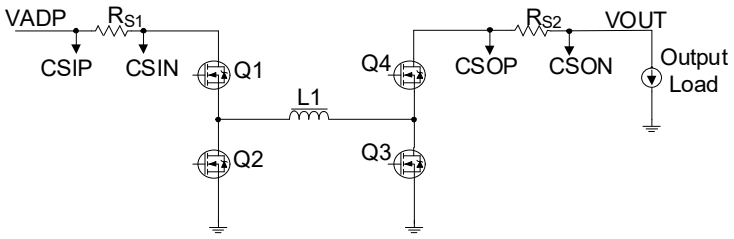


Figure 28. Buck-Boost Converter Topology

The RRB86848 optimizes the operation mode transition algorithm by comparing the input and output voltage ratio and the load condition. When the adapter voltage V_{ADP} is rising and is higher than 93% of the output voltage V_{OUT}, the RRB86848 transitions from Boost mode to Buck-Boost mode. If V_{ADP} is higher than 114% of V_{OUT}, the RRB86848 forcedly transitions from Buck-Boost mode to Buck mode. At heavier loads, the mode transition point changes accordingly to accommodate the duty cycle change because of the power loss on the charger circuit.

When the adapter voltage V_{ADP} is falling and is lower than 105% of the output voltage V_{OUT}, the RRB86848 transitions from Buck mode to Buck-Boost mode. If V_{ADP} is lower than 86% of V_{OUT}, the RRB86848 transitions from Buck-Boost mode to Boost mode.

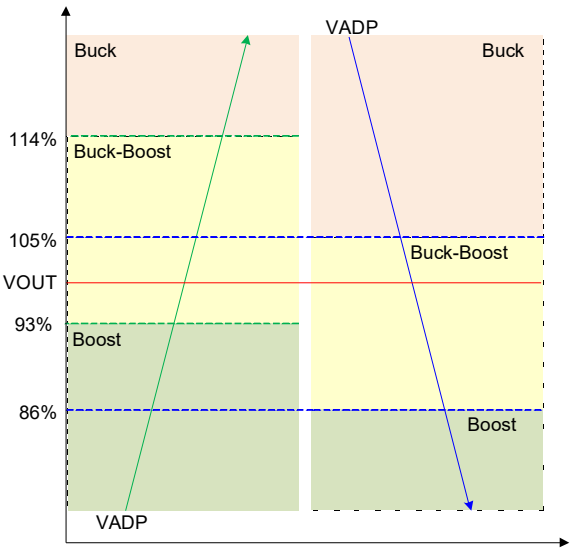


Figure 29. Operation Mode

When the Force Buck Mode is enabled by setting the Control0 Bit[1] to 1, the RRB86848 operates in Buck mode instead of Buck-Boost mode when VADP is 480mV higher than VOUT. Force Buck mode has a 240mV hysteresis window, so the RRB86848 operates in Buck-Boost mode when VADP is lower than VOUT + 240mV.

When operating as a voltage regulator in Forward mode and when no power source or battery is connected to VOUT, RRB86848 can be configured to support a 2-FET Buck topology as shown in Figure 3. To configure 2-FET Buck mode, connect LGATE2 to GND, PHASE2 to GND, BOOT2 to VDDP, and leave UGATE2 floating, as shown in Figure 3. The boost and buck-boost control loops are disabled in 2-FET mode. PTM operation is not recommended in 2-FET Buck mode.

7.2 USB On-the-Go (USB OTG)

When the On-the-Go (OTG) function is enabled with the SMBus command and OTGEN pin, and if the output-side voltage sensed at VOUTS2 is higher than 4.5V, the RRB86848 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode, and Control2 Bit[5] controls ASGATE.

When the RRB86848 receives the command to enable the OTG function, switching starts after the debounce time set by Control2 register Bit[13] and Control3 register Bit[0]. When the OTG output voltage at V_{ADP} reaches the reference set by the DAC OTG Voltage register 0x49, OTG power-good PGOOD asserts high. Control2 register Bit[5] can also turn the ASGATE FET off to cut off the OTG output.

Before OTG mode starts switching, the CSIP pin voltage must be less than the OTG output overvoltage protection threshold (OTG Voltage DAC(0x49h) + 1.8V). The CSIP pin is the output sensing point in OTG mode.

The OTG Voltage register 0x49 configures the OTG output voltage, which defaults to 5.004V. The OTG Current register 0x4A sets the OTG output current limit, and defaults to 480mA with an Rs1 of 10mΩ.

The RRB86848 includes OTG output undervoltage and overvoltage protection functions. The UVP threshold is the OTG output voltage -1.8V and the OVP threshold is the OTG output voltage +1.8V.

When OTG undervoltage is detected, the RRB86848 de-asserts PGOOD. After 32ms, switching stops and ASGATE is turned off. Switching resumes after the debounce time set by Control2 register Bit[13] and Control3 register Bit[0].

When OTG overvoltage (OV) is detected, the RRB86848 de-asserts PGOOD and turns off ASGATE. After 5ms, ASGATE begins turning back on to detect when the OTG OV condition is removed. When the OTG OV condition is no longer detected, PGOOD is asserted, and normal operation continues. If the OTG OV is not resolved within 32ms of ASGATE turning on, the RRB86848 turns ASGATE off for another 5ms. This sequence repeats until the OTG OV is removed.

The OTG Voltage DAC (0x49) is reset to its default value when an OTG UV or OV fault occurs, unless rereading of the PROG pin is disabled. To prevent the OTG DAC value from resetting when an OTG OV/UV fault occurs, disable PROG pin rereading by setting Control3 register Bit[15].

7.3 Pass-Through Mode

Pass-Through Mode (PTM) is configured by Control2 register Bits[1:0]. When PTM (normal or forced) is enabled, the internal reference for the output voltage ramps to the input voltage and switching continues until the output voltage is within ±150mV of the input (adapter) voltage. Once the output voltage falls within this 300mV window, switching stops, Q1 and Q4 are set on, and Q2 and Q3 are turned off. When PTM is enabled, all protections are still active. *Note*: The PGOOD signal is not applicable in PTM.

To disable PTM, set Control2 register Bits[1:0] = 00. On exiting PTM, the internal reference for the output voltage ramps to the OutputVoltage DAC value, and switching resumes. Normal PTM is also exited if any of the following criteria are encountered:

- Adapter OV triggers
- Adapter ACLIM triggers.
  Note: The adapter current comparator is disabled for 1ms after Q1 and Q4 latch on to enter PTM.
- VOUT absolute OV triggers

Forced PTM can only be exited by disabling PTM using Control2 Bits[1:0].

Before entering Pass-Through mode, the following is recommended:

- Ensure CV mode operation.
- Enable slew rate limiting by setting Control6 Bit[6] = 1.
- Set the OutputVoltage DAC to a value as close to the V_{ADP} voltage as possible.

7.4 Modulator Control Loops

Figure 30 shows the modulator's four main control loops in Forward mode. Each loop has a DAC register to provide settings as required for each system.

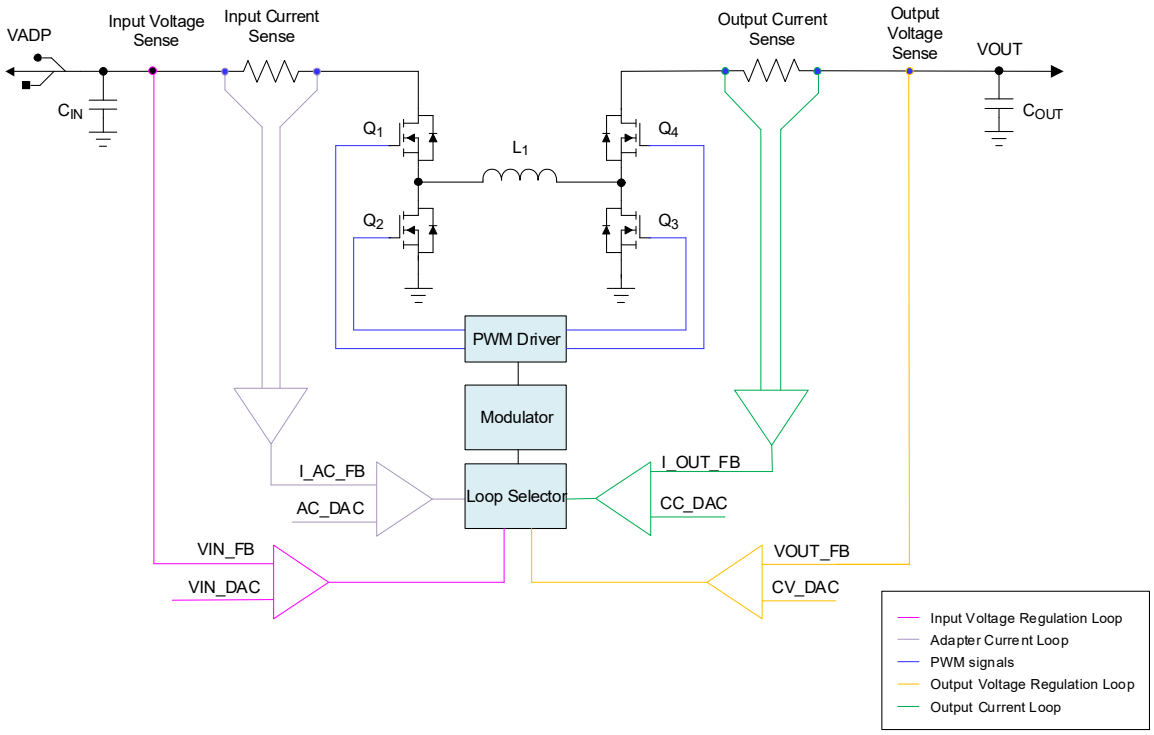


Figure 30. Converter Control Loops

7.4.1 Adapter Current Loop and Two-Level Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command to register address 0x3FH and, optionally, an AdapterCurrentLimit2 command to register address 0x3BH using the Write-word protocol. See Table 2 for the DAC summary of values.

The RRB86848 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended R_{S1} current sense resistor of 10mΩ, the DAC LSB translates to 8mA of adapter current.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.504A. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content. By default, the two-level adapter current limit is disabled.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit[12] and the t1, t2 settings are configured by the Control5 register. When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used as the adapter current limit and the AdapterCurrentLimit2 value is ignored.

In a real system, a transient load usually does not last long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The RRB86848 uses a two-level adapter current limit to fully take advantage of the surge capability of the adapter and avoid an output voltage collapse for brief load transients.

Figure 31 shows the two SMBus programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current is within 100mA of the AdapterCurrentLimit1 register setting. The adapter current limit is set at AdapterCurrentLimit2 for duration t2, then changes to AdapterCurrentLimit1 for duration t1 before repeating the pattern. These parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current.

The AdapterCurrentLimit1 register value can be higher or lower than the AdapterCurrentLimit2 value.

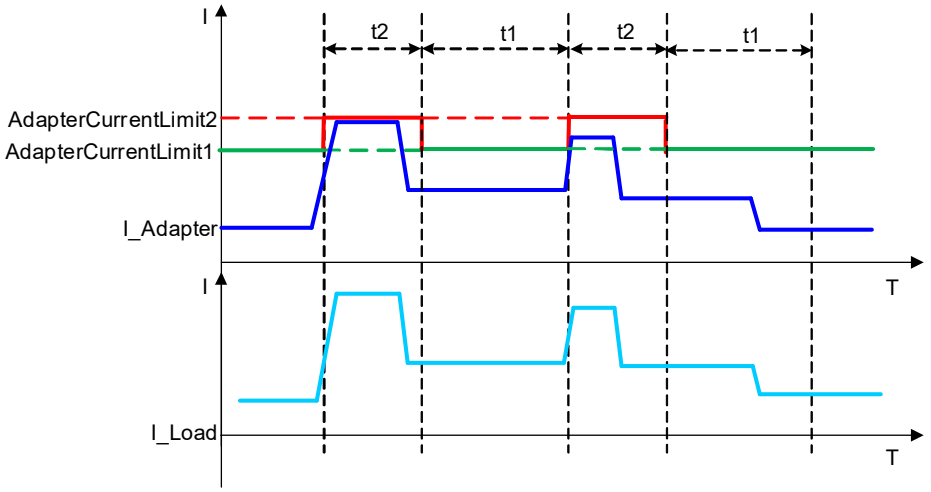


Figure 31. Two-Level Adapter Current Limit

7.4.2 Input Voltage Regulation Loop

7.4.2.1 Adapter Minimum Voltage

The input voltage regulation register DAC (Table 2) contains the SMBus readable and writable input voltage reference at which the input voltage loop tries to regulate when the input voltage is dropping. When the ADP is browning out or weak, the input voltage can droop. The input voltage loop regulates to the minimum input voltage register setting by reducing the output current. The output voltage might start to drop if the input power is not high enough to support the load.

7.4.2.2 USB-PD On-the-Go Minimum VOUT Voltage

The input voltage regulation register DAC (Table 2) sets a minimum voltage for VOUT when operating in OTG mode. Control5 register Bit[11] enables and disables the VOUT regulation loop. This regulation loop can be used to prevent exceeding the power rating of a source connected to VOUT when operating in OTG mode. The VOUTS2 pin serves as the sensing point for the OTG input voltage regulation loop.

7.4.3 USB-PD On-the-Go Output Voltage

The OTG output voltage regulation register DAC (Table 2) contains the SMBus readable and writable voltage reference for the OTG voltage loop. This loop reuses the input voltage sense amp.

This register accepts any voltage value, but only the valid register bits are written to the register. The maximum value is clamped.

7.4.4 USB-PD On-the-Go Output Current

The OTG output current regulation register DAC (Table 2) contains the SMBus readable and writable current reference for the OTG current sense loop. This loop uses the same input current sense amplifier as used in forward mode. The USB-PD Programmable Power Supply (PPS) uses the OTG current sense loop to set the OTG PPS current. *Note*: Renesas recommends disabling OTG undervoltage protection when OTG current limiting mode is anticipated as part of normal operation.

7.4.5 Output Voltage Regulation

The OutputVoltage DAC sets the regulation target for the output voltage in forward mode. Write a 16-bit OutputVoltage command to register 0x15, using the Write-word protocol shown in Figure 27, to configure the output voltage.

The VOUTS1 pin is the output voltage regulation sense point. The OutputVoltage DAC accepts any value, but only the valid register bits are written, and the voltage value is clamped at the maximum described in Table 2.

7.4.6 Output Current Loop

This loop uses the output current DAC (see Table 2) to set the output current limit. To set it, write a 16-bit OutputCurrentLimit command to register address 0x14H (Table 1).

RRB86848 limits the output current by limiting the CSOP - CSON voltage. Therefore, the output current depends on the R_{s2} resistor value. For example, if the current sense resistor R_{s2} is halved, the regulated output current doubles. By using the current sense resistor R_{s2} = 5mΩ, the DAC LSB translates to 8mA of output current. The OutputCurrentLimit register accepts any output current value, but only the valid register bits are written to the register.

7.4.6.1 Reverse Mode Input Current

When the converter operates in reverse mode (OTG), there is a reverse-mode input current limit loop that is set to 2x the forward OutputCurrentLimit register (0x14). This reverse-mode input current limit loop is in addition to the voltage regulation loop set by the OTG Voltage register, the current limit loop set by the OTG Current register, and the optional OTG input voltage regulation loop set by the Input Voltage register. The reverse-mode input current limit loop is disabled when OutputCurrentLimit (0x14) is zero. When the output current setting is a non-zero value,

the converter limits the reverse-mode input current to be less than the reverse input current limit (2x the Forward output current limit).

7.5 R3 Modulator

The RRB86848 uses the patented Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 32 conceptually shows the R3 modulator circuit.

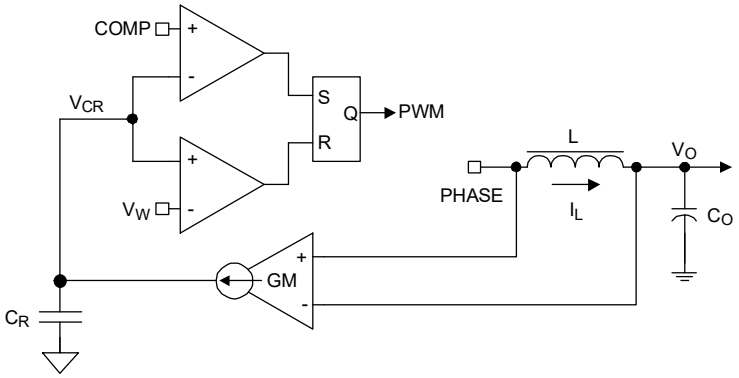


Figure 32. R3 Modulator

Figure 33 shows the operation principles in a steady state.

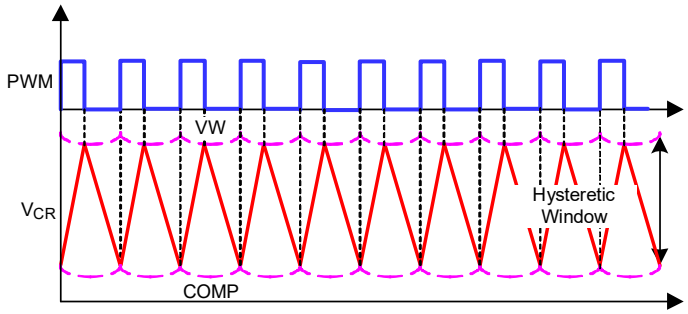


Figure 33. R3 Modulator Operation Principles in Steady State

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor C_R with a current source equal to $g_m(V_{IN}-V_O)$ during PWM on-time and discharges the ripple capacitor C_R with a current source equal to $g_m V_O$ during PWM off-time, where g_m is a gain factor. The C_R voltage V_{CR} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{CR}, which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulator.

Figure 34 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

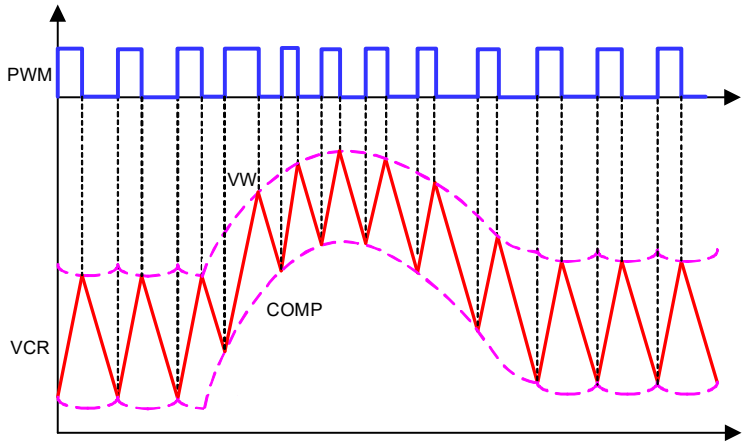


Figure 34. R3 Modulator Operation Principles in Dynamic Response

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, which emulates a diode. As shown in Figure 35, when LGATE is on, the low-side MOSFET carries current and creates negative voltage on the phase node because of the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

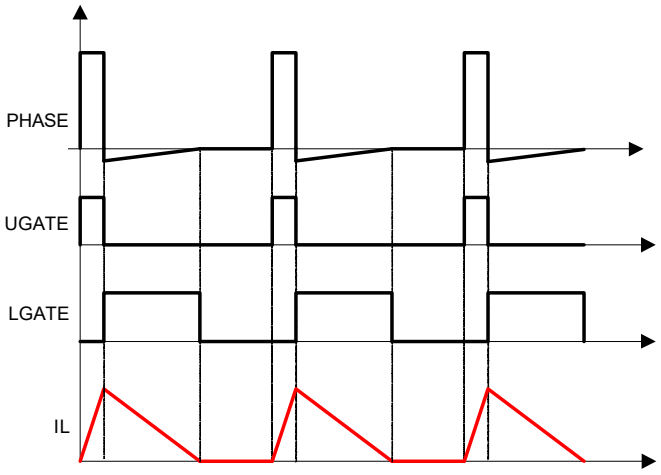


Figure 35. Diode Emulation

If the load current is light enough, as Figure 35 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A, and the regulator is in Continuous Conduction Mode (CCM) although the controller is in DE mode.

Figure 36 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on time is determined by the VW window size and therefore is the same, so the inductor current triangle is the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, which naturally stretches the switching period. The inductor current triangles move farther apart from each other

so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

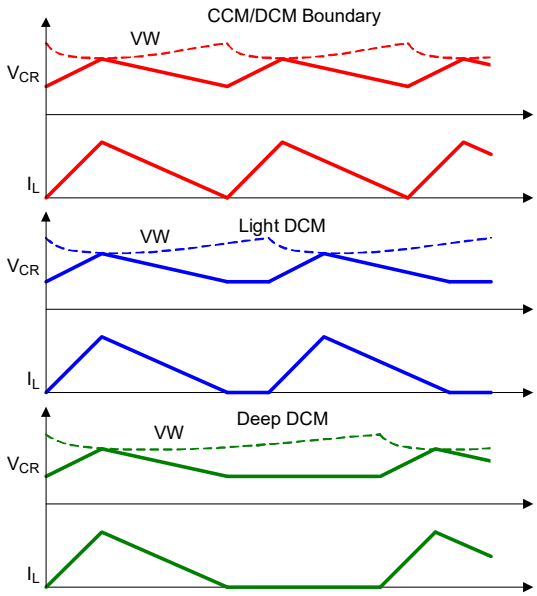


Figure 36. Period Stretching

8. Application Information

8.1 Soft-Start

The RRB86848 can use an external DC/DC or the internal LDO for supplying the VDD bias voltage. See VDD Voltage Supply for guidelines regarding bias supply options. Use of the internal LDO, applicable with low VADP and VOUT voltages, is described in this section.

The RRB96848 includes a low-power LDO with a 4.5V nominal output, and a high-power LDO with a 5V nominal output. These LDOs are powered from the DCIN pin, which is typically connected to the adapter (ADP) and the output bus (VOUT) through an external OR-ing diode circuit. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for the RRB86848. The VDDP pin is the RRB86848 gate drive power supply input. Use an R-C filter to generate the VDDP pin voltage from the VDD pin voltage.

When V_{DD} > 2.7V, the digital block is activated and the SMBus register is ready to communicate with the SMBus controller.

With VADP >3.4V and after the 1.3s or 150ms debounce time, the RRB86848 uses a patented Renesas technique to check whether the input bus is shorted. If CSIP <2V or ACIN <0.35V, ASGATE does not turn on. The input bus short protection adds an additional few milliseconds of delay, wherein the delay depends on the input capacitance. For adapter insertions after the initial one, the debounce time of 1.3s or 150ms is set by Control2 register Bit[11]. The debounce time for an initial adapter insertion is always 150ms. After the debounce time and the input bus short check, ASGATE starts turning on with 10µA of sink current.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The RRB86848 monitors the ACIN pin voltage to determine the presence of the adapter. When V_{DD} > 3.8V, the ACIN pin voltage exceeds 0.35V, and ASGATE is fully turned on, RRB86848 allows the external circuit to pull up the ACOK pin. When ACOK is asserted, RRB86848 starts switching.

The ACOK is an open-drain output pin that indicates the presence and readiness of the adapter to supply power to the output bus. The RRB86848 actively pulls ACOK low in the absence of the adapter.

Before ASGATE turns ON, the RRB86848 sources 10µA of current out of the PROG pin and reads the pin voltage to determine the PROG resistor value. The PROG resistor programs the configurations of the RRB86848.

8.2 Programming Options

The resistor from the PROG pin to GND programs default values for the OutputVoltage, the AdapterCurrentLimit1 value, and the OutputCurrentLimit. Table 15 shows the programming options.

Table 15. PROG Pin Programming Options

PROG-GND Resistance (kΩ)			Info2 [4:0]	Output Voltage (V)	Adapter Current Limit1 (A)	Output Current Limit (A)
Min	Typ. 1%	Max				
42.7	43.2	43.7	00110	5	0.48	0.48
51.7	52.3	52.9	00111		2.848	2.848
61.2	61.9	62.6	01000	9	0.48	0.48
70.6	71.5	72.4	01001		2.848	2.848
81.5	82.5	83.5	01010	15	0.48	0.48
92	93.1	94.2	01011		2.848	2.848
104	105	106	01100	20	0.48	0.48
116	118	120	01101		2.848	2.848
131	133	135	01110		4.752	4.752
145	147	149	01111	28	0.48	0.48
160	162	164	10000		2.848	2.848
176	178	180	10001		4.752	4.752
194	196	198	10010	36	0.48	0.48
212	215	218	10011		2.848	2.848
234	237	240	10100		4.752	4.752
258	261	264	10101	48	0.48	0.48
284	287	290	10110		2.848	2.848
312	316	320	10111		4.752	4.752

The default switching frequency is 723kHz. After POR, the switching frequency can be modified using SMBus Control1 register Bits[9:8] and Control4 register Bit[11]. See the SMBus Control 1 and Control 4 register programming tables (Table 4 and Table 7) for a detailed description. Note: Renesas recommends reducing the switching frequency to 377kHz, which decreases the MOSFET gate drive current from VDDP.

After an adapter insertion and before ASGATE turns on, the RRB86848 sources 10µA of current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise can pollute the PROG pin voltage and cause incorrect readings. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs so the PROG pin voltage can rise to steady state before the RRB86848 reads it.

By default, the adapter current sensing resistor R_{s1} is 10mΩ and the output current sensing resistor R_{s2} is 5mΩ. Using this R_1 = 10mΩ and R_{s2} = 5mΩ option results in an 8mA/LSB correlation in the SMBus current commands. If the R_{s1} and R_{s2} differ from these default options, the SMBus command must be scaled accordingly to obtain the correct current. Smaller current sense resistor values reduce power loss while larger current sense resistor values give better accuracy.

8.3 PGOOD

The RRB86848 provides a PGOOD/CMOUT pin which, by default, indicates whether the output voltage is outside a power-good (PGOOD) window, based on the DAC value of the Output Voltage (forward mode) or the OTG Voltage (reverse mode) register. To disable the PGOOD indication and use the PGOOD/CMOUT pin as the comparator output, set Control5 register Bit[5] to 1.

When the output voltage goes outside the PGOOD window, the PGOOD pin is pulled low. When the output voltage returns within the PGOOD hysteresis window, the PGOOD pin is pulled high. Table 37 illustrates how the PGOOD pin is asserted depending on the output voltage, the PGOOD window, and the PGOOD hysteresis window. In forward mode, the PGOOD window is ±1.6V with a hysteresis of ±0.8V. In reverse mode, the PGOOD window is ±1.8V with a hysteresis of ±0.9V. The PGOOD window is independent of Overvoltage (OV) and Undervoltage (UV) events.

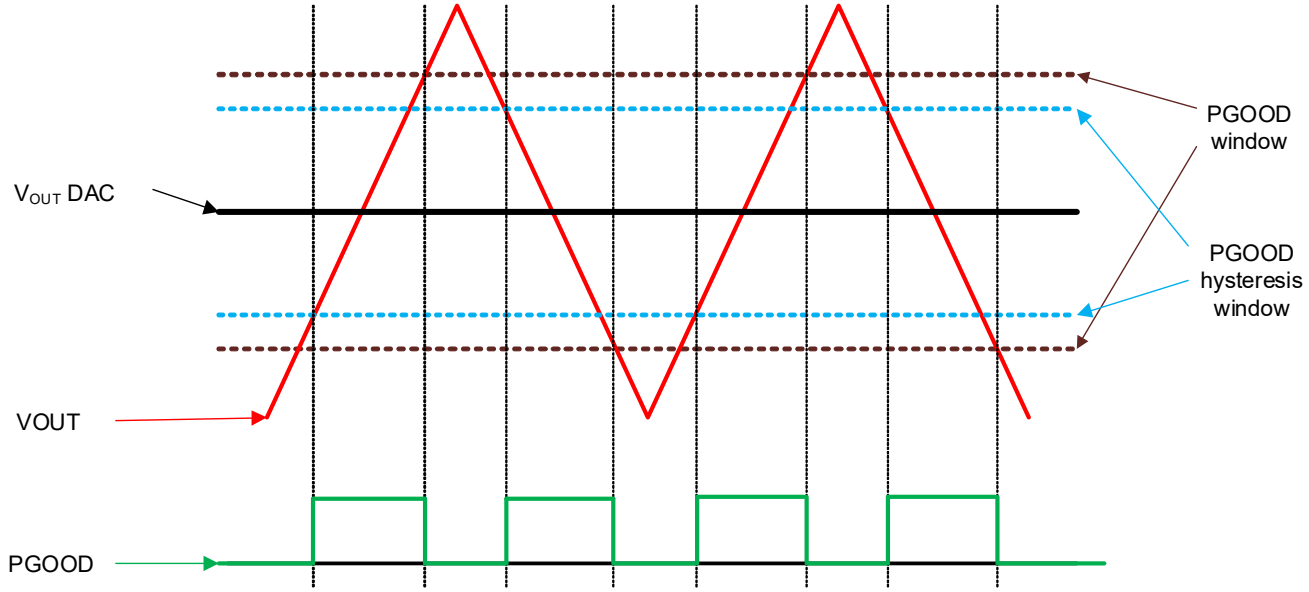


Figure 37. PGOOD Window Behavior

When the DAC sets a new output voltage reference, the PGOOD window is shifted accordingly with the DAC transition. If V_{OUT} is outside the PGOOD window during the transition, the PGOOD signal goes low and returns high when V_{OUT} is back inside the hysteresis window. Figure 38 explains this transition behavior in detail.

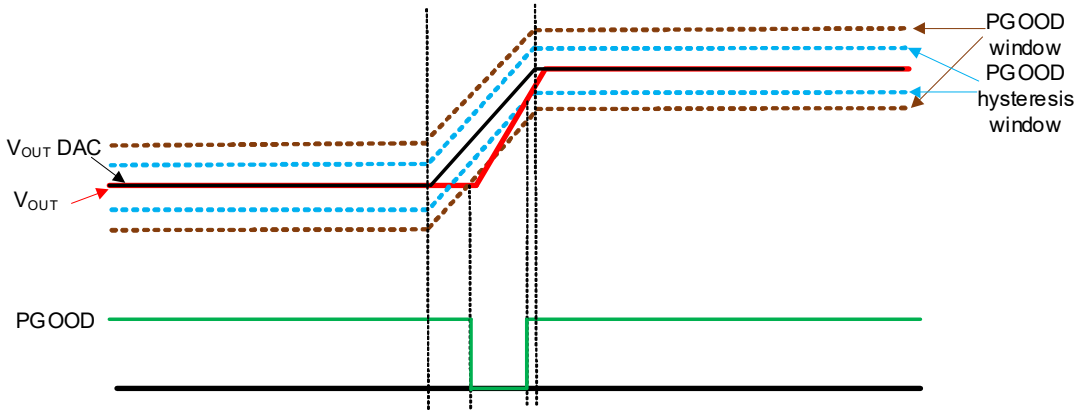


Figure 38. PGOOD VOUT DAC Transition

8.4 Low Power Modes

8.4.1 Forward Sleep Mode

To achieve low quiescent current when an adapter is attached, enable Forward Sleep Mode by setting Control5 register Bit[3]. This disables switching, the high-power LDO, and many of the internal circuits.

To achieve the lowest quiescent current in this state, disable the current monitor and general-purpose comparator as follows:

- Disable AMON/BMON – Control1 register (0x3C) Bit[5] = 1
- Disable GP comparator – Control2 register (0x3D) Bit[3] = 1

8.4.2 Reverse Sleep Mode

When no adapter is attached but power is applied at VOUT, switching is disabled by default and many of the internal circuits are not powered. In this Reverse Sleep Mode configuration, the high-power LDO is disabled and the low-power LDO supplies a VDD of 4.5V.

To achieve the lowest quiescent current in this state, disable the current monitor and general-purpose comparator as follows:

- Disable AMON/BMON – Control1 register (0x3C) Bit[5] = 1
- Disable GP comparator – Control2 register (0x3D) Bit[3] = 1

8.5 Diode Emulation Operation

In Diode Emulation (DE) mode, RRB86848 uses a phase comparator to monitor the PHASE node voltage during the low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator requires a minimum on-time of the low-side switching FET to recognize inductor current zero crossing. If the low-side switching FET on time is too short for the phase comparator to successfully recognize the inductor zero crossing, RRB86848 can lose DE ability. To prevent this, RRB86848 uses a minimum low-side switching FET on time. When the intended low-side switching FET on-time is shorter than the minimum value, RRB86848 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

8.6 Monitoring

8.6.1 Current Monitor

RRB86848 provides an adapter current monitor/OTG output current monitor, or a forward output current monitor/OTG input current monitor through the AMON/BMON pin. The AMON output voltage is 18x (CSIP - CSIN) and 18x (CSIN - CSIP) voltage. The BMON output voltage is 36x (CSOP - CSON) and 18x (CSON - CSOP) voltage.

The AMON and BMON functions can be enabled or disabled through SMBus Control1 register Bit[5]. AMON or BMON can be selected through SMBus Control1 register Bit[4] and the AMON/BMON direction can be configured through SMBus Control3 register Bit[3] as Table 4 describes.

8.6.2 ALERT#

RRB86848 provides an open-drain ALERT# signal to indicate adapter removal or general-purpose comparator triggering. The ALERT# feature is disabled by default.

To enable the adapter removal ALERT#, set Control4 register Bit[5]. With this ALERT# input enabled, the ALERT# signal is asserted (driven low) when ACOK goes low, which indicates no adapter.

To enable the general-purpose comparator ALERT#, set Control4 register Bit[4]. With this ALERT# input enabled, the ALERT# signal is asserted (driven low) when the comparator is triggered.

The debounce time for the ACOK ALERT# trigger is set by Control4 register Bits[3:2]. While the general-purpose comparator ALERT# signal has no dedicated debounce setting, the comparator itself has a debounce time that

can be set by Control1 register Bits[15:14]. The minimum duration of an ALERT# assertion is set by Control2 Bits[8:6].

Control4 Bit[0] can configure ALERT# to latch and hold its state. A latched ALERT# assertion can be cleared using Control4 Bit[1].

8.7 General-Purpose Comparator

RRB86848 includes a general-purpose comparator. The OTGEN/CMIN pin is the comparator input. The internal comparator reference is connected to the inverting input of the comparator and can be configured as 1.2V or 2V through SMBus Control2 register Bit[4]. The comparator output is the PGOOD/CMOUT pin. Control5 register Bit[5] must be set to 1 for the comparator output to route to the PGOOD/CMOUT pin. The output polarity can be configured through the SMBus register bit.

- When Control2 register Bit[2] = 0 for normal comparator output polarity, CMOUT = High if CMIN > Reference; CMOUT = Low if CMIN < Reference.
- When Control2 register Bit[2] = 1 for inversed comparator output polarity, CMOUT = Low if CMIN > Reference; CMOUT = High if CMIN < Reference.

The general-purpose comparator is enabled by default and can be disabled using Control2 Bit[3]. The general-purpose comparator must be disabled if OTG is to be enabled using the OTGEN/CMIN pin.

In forward sleep mode and reverse source mode (no adapter attached, power supplied at VOUT, OTG disabled), the 2V comparator reference is not available and should not be configured.

Table 16 shows the OTG mode and the general-purpose comparator truth table.

Table 16. OTG and Comparator Truth Table

Control1 Bit[11] OTG Function Enable/Disable	Control2 Bit[3] GP Comparator Enable/Disable	PIN-20 OTGEN/CMIN	PIN-26 PGOOD/CMOUT	Description
0	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	OTG function is disabled. Comparator is enabled.
0	1	X	X	Both the OTG function and comparator are disabled.
1	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT (Control1 register Bit[5] must be 1 to route CMOUT to the pin.)	Both the OTG function and comparator are enabled. OTG function is enabled when VOUTS2 >4.5V and Control1 register Bit[11] = 1 without OTG power-good pin indication. The device is in OTG mode while Information1 register 0x3A Bit[6:5] = 11.
1	1	OTG Enable Input Pin OTGEN	Power-Good Indication Pin PGOOD (Control1 register Bit[5] must be 0 to route PGOOD to the pin.)	Comparator is disabled. OTG function is enabled when VOUTS2 >4.5V and ENOTG pin = High and Control1 register Bit[11] = 1.

8.8 Protections[1]

8.8.1 Adapter Overvoltage Protection

If the ADP pin voltage exceeds 57.6V for more than 10µs, an adapter overvoltage condition occurs. RRB86848 turns off the ASGATE MOSFETs to isolate the adapter from the system, de-asserts the ACOK signal by pulling it low, and stops switching. When the ADP voltage drops below 57.05V from more than 100µs, it starts to turn on ASGATE and start switching.

8.8.2 Output Overvoltage Protection

RRB86848 provides VOUT relative overvoltage protection. If the sensed output voltage VOUTS1 is 1.6V higher than the OutputVoltage register set value, it declares the output overvoltage and stops switching. It resumes switching, with no debounce time, when VOUTS1 drops 800mV below the output overvoltage threshold.

RRB86848 also provides VOUT absolute overvoltage protection. The default absolute overvoltage rising threshold is 57.6V. If the sensed output voltage VOUTS1 is higher than 57.6V, switching stops. When VOUTS1 drops to lower than 57.08V, switching restarts. The absolute overvoltage protection threshold can be modified using Control3 register Bits[10:9] to support USB-C voltages of 36V, 28V, or 20V.

8.8.3 Output Voltage Rail Short Protection

The RRB86848 has an output rail short protection (VOUTOK) to prevent powering on the output rail into a short-circuit before switching starts. When the VOUTS1 voltage is below 0.6V, the RRB86848 sources 10mA current (by default) from VDDP to charge VOUT before switching can start. Renesas recommends ensuring that there is no load on VOUT at startup.

From the beginning of VOUTOK (VOUT rail short protection) to the start of switching in the VOUT state, the RRB86848 must go through multiple startup and initialization transition states, including turning on ASGATE FET. This initialization transition duration might take longer than it takes to charge the VOUT voltage to 0.6V using a 10mA source by the VOUTOK function. If this initialization transition duration is longer than the duration of charging VOUT above 0.6V, the charger must wait until the transition duration is completed before switching starts, and vice versa.

Conversely, the duration of charging VOUT above 0.6V, which depends on the leakage current and capacitance value at VOUT, varies per individual system design. If estimating the duration in a worst-case scenario is required, Renesas recommends testing the design to determine the following:

- If the initialization transition duration is longer than the duration of charging VOUT above 0.6V, add a 30% margin (considering ±15% clock tolerance) to estimate worst-case duration.
- If the initialization transition duration is shorter than the duration of charging VOUT above 0.6V, check the tolerance of the VOUT capacitance or leakage current from VOUT downstream circuitry and then add a reasonable margin, such as 40% (considering ±20% cap tolerance), to estimate worst-case duration.

After switching starts, the charger enters the Fault state if VOUT drops below 0.6V again at any time. After entering the Fault State, the charger stops switching and turns off ASGATE and tries to start again with 1.3s or 150ms debounce time (configured by Control 2[11]).

After the initial POR, the VOUT rail short protection check can optionally be bypassed by disabling both the VOUTOK 0.6V Comparator using Control5 Bit[7] and the VOUTOK 10mA current source using Control5 Bit[6].

8.8.4 Output Voltage Undervoltage Protection (for Short-Circuit Protection)

The converter has a fixed undervoltage protection on the output side that can be configured using Control 6[2:0].

The initial value of the VOUT undervoltage is set as follows:

- POR from VOUT: VOUT UV is 000 = disabled,
- POR from adapter: VOUT UV is 001 = 3.0V.

1. Nominal protection values are provided in this section. Refer to the Electrical Specifications for accurate values.

When the VOUTS1 voltage falls to the VOUT UV threshold set by Control 6[2:0], there is a 100ms debounce before the converter enters FAULT state. After entering FAULT state, there is no switching, and the converter tries to start switching again after the 150ms or 1.3s debounce time (configurable by Control 2[11]).

8.8.5 Over-Temperature Protection

RRB86848 stops switching for self-protection when the junction temperature exceeds +150°C. When the temperature falls below +130°C and after a 100µs delay, RRB86848 resumes switching.

8.9 Power Source

RRB86848 uses the adapter to provide power in forward mode and uses VOUT to provide power in reverse mode.

The ASGATE pin drives a pair of back-to-back common source P-channel MOSFETs to connect/disconnect the adapter. Use of the ASGATE pin is optional.

When the output voltage, as detected at VOUTS2, is higher than 2.4V and the adapter voltage VADP is less than 3.4V, RRB86848 operates in reverse sleep mode, during which very little power is consumed. (Refer to the Reverse Supply Current specification.) The OTG input current monitor BMON can be turned on during this mode to monitor the current consumption.

From reverse sleep mode, the OTG function can be enabled provided that the output voltage VOUTS2 (OTG input voltage) is higher than 4.5V. After OTG is enabled, reverse sleep mode is exited. See USB On-the-Go (USB OTG) for details.

When the adapter voltage V_{ADP} is more than 3.4V, RRB86848 turns on ASGATE. If VDD is higher than 3.8V, the RRB86848 enters Forward Buck, Forward Boost, or Forward Buck-Boost mode depending on the ratio of the adapter voltage to the VOUT voltage. The output bus voltage is regulated at the voltage set on the OutputVoltage register.

9. Design Guidelines

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following sections. In addition to this guide, Renesas provides complete reference designs that include schematics, bill of materials, and example board layouts.

9.1 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 1:

(EQ. 1) $$D = \frac{V_{OUT}}{V_{IN}}$$

Use Equation 2 to calculate the output inductor peak-to-peak ripple current:

(EQ. 2) $$I_{P-P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L}$$

A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based on several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

Use Equation 3 to estimate the DC copper loss of the inductor, where I_{LOAD} is the converter output DC current.

(EQ. 3) $$P_{COPPER} = I_{LOAD}^{2} \cdot DCR$$

The copper loss can be significant, so select DCR carefully. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. Use Equation 4 and Equation 5 to calculate these two voltages:

(EQ. 4) $$\Delta V_{ESR} = I_{P-P} \cdot ESR$$

(EQ. 5) $$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}}$$

If the output of the converter must support a load with high pulsating current, several capacitors must be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the transient load has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Ensure that I_{P-P} is shared by enough parallel capacitors so that they operate below the maximum rated RMS current at f_{SW}. Consider that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

9.2 Selecting the Input Capacitor

The important parameters for input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and that can supply the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 39 is a graph of the input capacitor RMS ripple current that is normalized relative to output load current. The graph is also a function of duty cycle and is adjusted for converter efficiency.

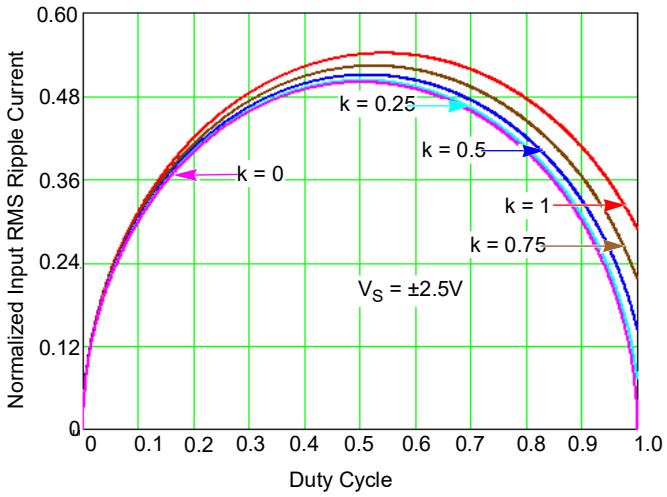


Figure 39. Normalized RMS Input Current at EFF = 1

Use Equation 6 to calculate the normalized RMS ripple current calculation:

(EQ. 6) $$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1 - D) + \frac{D \cdot k^2}{12}}}{I_{MAX}}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter.
- k is a multiplier (0 to 1) corresponding to the inductor peak-to peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)
- D is the duty cycle that is adjusted to consider the efficiency of the converter, which is calculated using Equation 7:

(EQ. 7) $$D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

In addition to any bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

9.3 Selecting the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs that are optimized for DC/DC converter applications are readily available. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately VIN - VOUT, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. *Note:* This is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices might be required.

The power loss of the Low-Side (LS) MOSFET can be assumed to be conductive only and is calculated using Equation 8:

(EQ. 8) $$P_{CON\_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)\_LS} \cdot (1 - D)$$

Use Equation 9 to calculate the conduction loss of the High-Side (HS) MOSFET:

(EQ. 9) $$P_{CON\_HS} = I_{LOAD}^2 \cdot r_{DS(ON)\_HS} \cdot D$$

Use Equation 10 to calculate the switching loss of the HS MOSFET:

(EQ. 10) $$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{SWON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{SWOFF} \cdot f_{SW}}{2}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current.
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current.
- $t_{SW(ON)}$ is the time required to drive the device into saturation.
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off.

9.4 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 11:

(EQ. 11) $$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on.

As an example, suppose the HS MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF is sufficient. Use an X7R or X5R ceramic capacitor. Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

9.5 Switching Power MOSFET Gate Capacitance

The RRB86848 includes an internal 5V LDO output at the VDD pin, which can provide the switching MOSFET gate driver power through the VDDP pin with an RC filter. The 5V LDO output overcurrent protection threshold is 85mA, minimal (check EC table for the accurate value). When selecting the switching power MOSFET, consider the MOSFET gate capacitance carefully to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, use Equation 12 to estimate the gate drive current:

(EQ. 12) $$I_{driver} = Q_g \bullet f_{SW}$$

where:

- Q_g is the total gate charge, which can be found in the MOSFET datasheet.
- f_{SW} is the switching frequency.

Renesas recommends using a 2.2µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

9.6 VDD Voltage Supply

When high voltages, such as 36V or more, are expected at VADP or VOUT, Renesas recommends generating a 5.5V bias voltage using a DC/DC supply external to the RRB86848. When overdriving VDD with such a bias voltage, the LDO output should be set to 4.5V using Control7 register Bit[3]. This approach provides a highly efficient bias supply.

For applications with low expected VADP and VOUT voltages, the DCIN input pin can be driven from an external OR-ing diode circuit having VADP and VOUT as inputs, and the internal LDO can supply VDD and VDDP. Such an approach requires minimal external components.

When using the internal LDO, the DCIN input should be filtered by connecting a 10Ω resistor between the DCIN pin and the VADP/VOUT diodes, and connecting a 4.7µF DCIN capacitor to GND, which has an effective capacitance higher than 0.4µF at 48V.

9.7 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the RRB86848 pins connecting to the adapter connector node. One low-cost solution is to add an R-C snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 40. A practical value of the R-C snubber is 2.2Ω to 2.2µF, while the appropriate values and power rating should be carefully

characterized based on the actual design. Renesas does not recommend adding a pure capacitor at the adapter connector node, which can cause an even larger voltage spike because of the adapter cable or the adapter current path parasitic inductance.

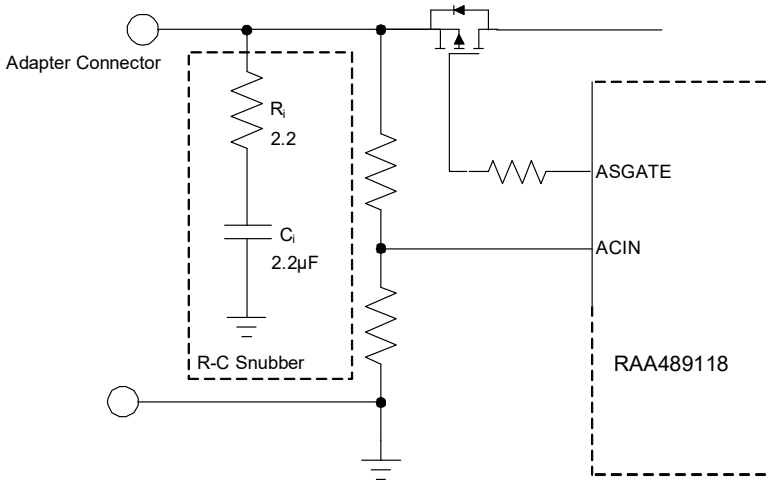
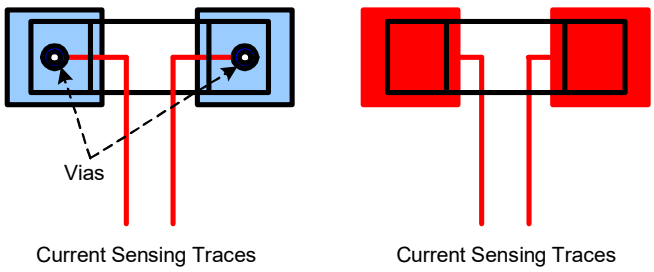
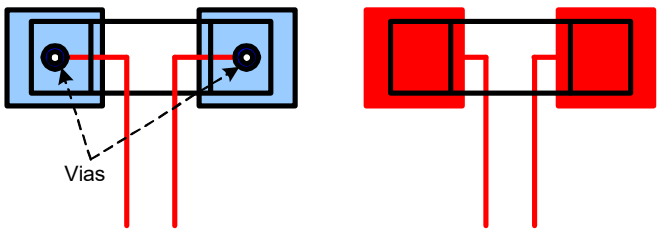


Figure 40. Adapter Input R-C Snubber Circuit

10. Layout

Pin Number	Pin Name	Layout Guidelines
Bottom Pad 33	GND	Connect this ground pad to the ground plane through a low impedance path. Use at least five vias to connect to the PCB ground planes to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current sensing resistor to the IC. Place the differential mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
2	CSOP	
3	VOUTS1	This signal pin provides feedback for the output bus voltage. Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from the output bus to the pin and do not route near the switching traces. Do not share the same trace with the signal routing to the DCIN pin OR-ing diodes and the CSOP trace.
4	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide traces. Avoid any sensitive analog signal traces from crossing over or getting close. Allocate a footprint for an external Schottky diode from VDDP to BOOT2.

Pin Number	Pin Name	Layout Guidelines
5	UGATE2	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close. Route the PHASE2 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the gate terminals of the switching MOSFETs and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source, and use the shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET source and low-side MOSFET drain terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
6	PHASE2	
7	LGATE2	Switching pin. Use sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close.
8	VDDP	Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to the VDD pin with sufficient width.
9	LGATE1	Switching pin. Use sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close.
10	PHASE1	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close. Route the PHASE1 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the gate terminals of the switching MOSFETs and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source, and use the shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET source and low-side MOSFET drain terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area big enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
11	UGATE1	
12	BOOT1	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide traces. Avoid any sensitive analog signal traces from crossing over or getting close. Allocate a footprint for an external Schottky diode from VDDP to BOOT1.
13	ASGATE	Run this trace with sufficient width in parallel fashion with the ADP pin trace.
14	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
15	CSIP	
16	ADP	Run this trace with sufficient width in parallel fashion with the ASGATE pin trace.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller. Run the VADP trace and VOUT trace to the OR diodes with sufficient width.
18	VDD	Place the RC filter connecting with the VDDP pin in the general proximity of the controller. Run the trace connecting to the VDDP pin with sufficient width.

Pin Number	Pin Name	Layout Guidelines
19	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
20	OTGEN/CMIN	No special consideration.
21	SDA	Digital pins. Avoid running these traces near noisy traces. Run the SDA and SCL traces in parallel.
22	SCL	
23	ALERT#	Digital pin, open-drain output. No special consideration.
24	ACOK	
25	RESERVED	Connect to GND.
26	PGOOD/ CMOUT	Digital pin, open-drain output. No special consideration.
27	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
28	COMP	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
29	AMON/BMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
30	RESERVED	This pin should not float. Connect to either VDD or GND.
31	VOUTS2	Place the optional R-C filter in the general proximity of the controller. Run a dedicated trace from the output voltage node VOUT to the IC.
32	Unused	-

11. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

12. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg #	Carrier Type[4]	Temp. Range
RRB86848-AT7	86848A7	32 Ld 4x4 TQFN	L32.4x4D	Reel, 6k	-10 to +100°C
RRB86848-AU7				Reel, 1k	
RRB86848-AT8	86848A8			Reel, 6k	-40 to +100°C
RRB86848-AU8				Reel, 1k	
RTKRB86848DE0000BU	RRB86848 Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 3. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

13. Revision History

Revision	Date	Description
1.01	May 13, 2025	Updated Input Voltage maximum from 54V to 55V. Updated Output Voltage maximum from 54V to 55V. Updated Figure 4, Block Diagram. Updated Pin 31 description. In Recommend Operating Conditions, updated Adapter Voltage maximum from 54V to 55V. In Electrical Specifications, updated Test Conditions for OTG Current, OTG Undervoltage Falling Threshold, OTG Undervoltage Rising Hysteresis, OTG Overvoltage Rising Threshold, and OTG Overvoltage Falling Hysteresis. Updated 8.1, Soft-Start. Added evaluation board to the Ordering Information section.
1.00	Feb 21, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRB86848-AT7	32	TQFN	L32.4x4D
RRB86848-AU7	32	TQFN	L32.4x4D
RRB86848-AT8	32	TQFN	L32.4x4D
RRB86848-AU8	32	TQFN	L32.4x4D

A.2 Symbol Pin Information

A.2.1 32-TQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	CSON	Input	-
2	CSOP	Input	-
3	VOUTS1	Input	-
4	BOOT2	Power	-
5	UGATE2	Output	-
6	PHASE2	Power	-
7	LGATE2	Output	-
8	VDDP	Power	-
9	LGATE1	Output	-
10	PHASE1	Power	-
11	UGATE1	Output	-
12	BOOT1	Power	-
13	ASGATE	Output	-
14	CSIN	Input	-
15	CSIP	Input	-
16	ADP	Input	-
17	DCIN	Power	-
18	VDD	Power	-
19	ACIN	Input	-
20	OTGEN	Input	CMIN
21	SDA	I/O	-
22	SCL	I/O	-
23	ALERT#	Output	-
24	ACOK	Output	-
25	RESERVED	Input	-
26	PGOOD	Output	CMOUT
27	PROG	Input	-
28	COMP	Output	-
29	AMON	Output	BMON
30	RESERVED	Input	-
31	VOUTS2	Input	-
32	NC	Passive	-
EPAD33	GND	Power	-

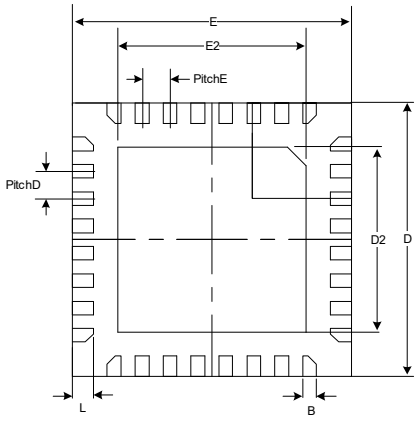
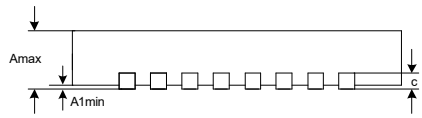
A.3 Symbol Parameters

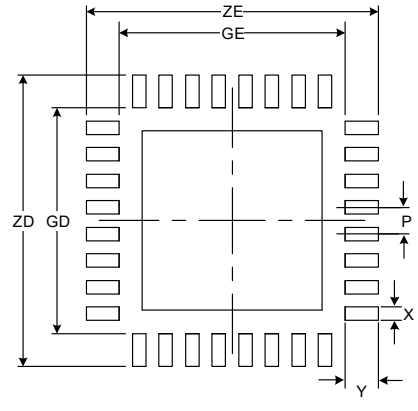
Orderable Part Number	Qualification	Mounting Type	Min Input Voltage	Max Input Voltage	Min Output Voltage	Max Output Voltage	Min Operating Temperature	Max Operating Temperature	Max Junction Temperature (Tj)	RoHS	Typ Switching Frequency	Switcher Configuration
RRB86848-AT7	Consumer	SMD	3.9 V	55 V	2.4 V	55 V	-10 °C	+100 °C	+125 °C	Yes	377 kHz	Buck, Boost, and Buck-Boost
RRB86848-AU7	Consumer	SMD	3.9 V	55 V	2.4 V	55 V	-10 °C	+100 °C	+125 °C	Yes	377 kHz	Buck, Boost, and Buck-Boost
RRB86848-AT8	Industrial	SMD	3.9 V	55 V	2.4 V	55 V	-40 °C	+100 °C	+125 °C	Yes	377 kHz	Buck, Boost, and Buck-Boost
RRB86848-AU8	Industrial	SMD	3.9 V	55 V	2.4 V	55 V	-40 °C	+100 °C	+125 °C	Yes	377 kHz	Buck, Boost, and Buck-Boost

A.4 Footprint Design Information

A.4.1 32-TQFN

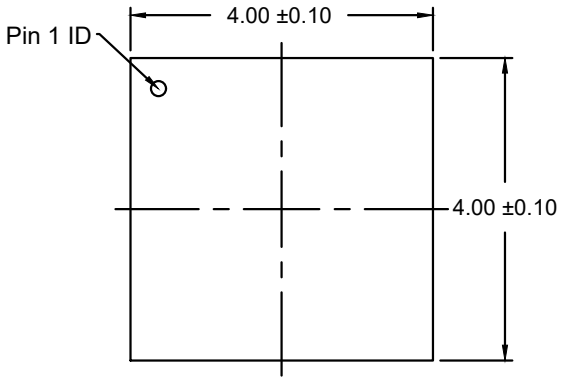
IPC Footprint Type	Package Code/ POD number	Number of Pins
QFN	L32.4x4D	32

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	3.90	
Maximum body span (vertical side)	Dmax	4.10	
Minimum body span (horizontal side)	Emin	3.90	
Maximum body span (horizontal side)	Emax	4.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Number of pins (vertical side)	PinCountD	8	
Number of pins (horizontal side)	PinCountE	8	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.4	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.4	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	2.6	
Maximum thermal pad size (vertical side)	D2max	2.8	
Minimum thermal pad size (horizontal side)	E2min	2.6	
Maximum thermal pad size (horizontal side)	E2max	2.8	
Maximum Height	Amax	0.8	
Minimum Standoff Height	A1min	0	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

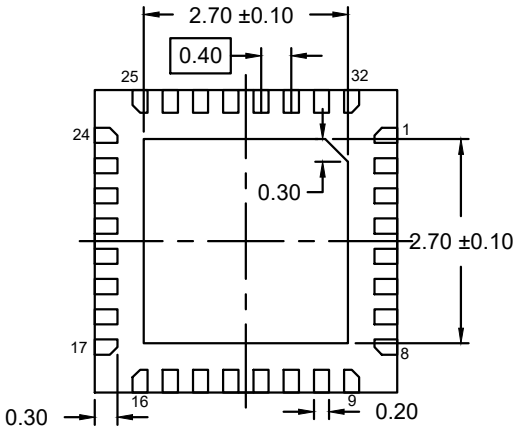
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	4.4	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	4.4	
Distance between left pad heel to right pad heel (horizontal side)	GE	3.4	
Distance between top pad heel to bottom pad heel (vertical side)	GD	3.4	
Pad Width	X	0.2	
Pad Length	Y	0.5	

Package Outline Drawing

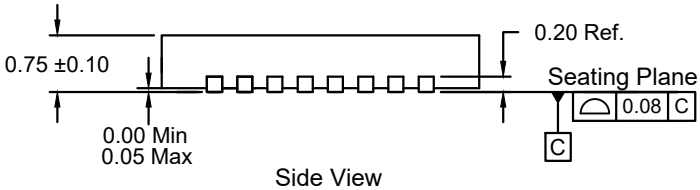
L32.4x4D
QW0032AA
32-QFN 4.0 x 4.0 x 0.75 mm Body, 0.40 mm Pitch
Rev04, Mar 26, 2025



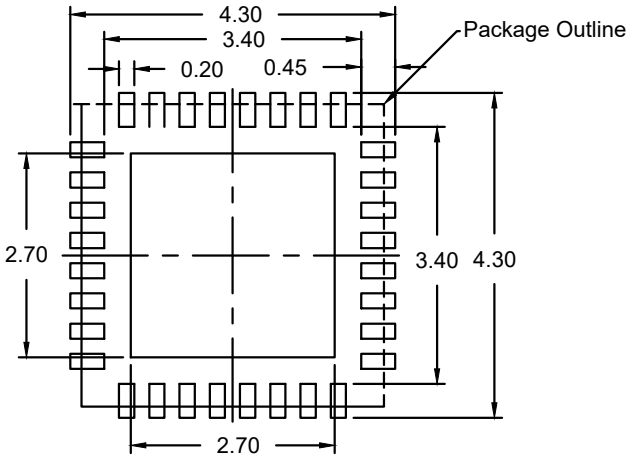
Top View



Bottom View



Side View



Typical Recommended Land Pattern

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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