RRB96838

Bidirectional 20V Buck-Boost Battery Charger with SMBus Interface

Description

The RRB96838 is a buck-boost battery charger supporting input voltages up to 23.4V and battery voltages up to 18.3V. The RRB96838 can operate in a direct battery charging mode without a battery FET, or it can operate in an NVDC charging mode with a battery FET. The advanced Renesas R3™ technology provides highly efficient light-load operation and fast transient response.

The direct battery charging mode supports charging of 2- to 4-cell batteries for applications such as power tools, portable vacuums, drones, robots, and power banks.

As a Narrow-Voltage DC (NVDC) charger, the RRB96838 also regulates the system output to a narrow voltage range for stable system bus voltage. Under NVDC operation, system power is either provided from the adapter, battery, or a combination of both.

The RRB96838 accepts input power from a wide range of DC power sources, including USB-C PD adapters, and safely charges battery packs having up to 4 serially connected Li battery cells. Additionally, the RRB96838 supports reverse buck, boost, and buck-boost operation, in which power is transferred from an attached battery to the input port.

The RRB96838 provides SMBus/I^2C serial communication that allows programming of many critical parameters to deliver a customized solution.

Features

- Buck-boost charger for 2-, 3-, or 4-cell Li-ion batteries
- Input voltage range: 3.9V to 23.4V (no dead zone)
- Battery output voltage: 2.4V to 18.304V
- Autonomous charging option (with BFET configuration only)
- Pass-Through mode in forward direction
- Up to 1MHz switching frequency
- Adapter current and battery current monitor (AMON/BMON)
- ALERT# open-drain output
- Supports trickle charging of depleted battery
- Reverse buck, boost, and buck-boost operation from battery
- Battery Ship mode option
- SMBus and auto-increment I^2C compatible
- 4×4 32 Ld TQFN package

Applications

- Charging for 2 to 4-cell batteries, including power tools, portable vacuums, drones, power banks, and any battery-powered device having a USB-C interface

Contents

1. Overview

1.1 Typical Application Diagrams

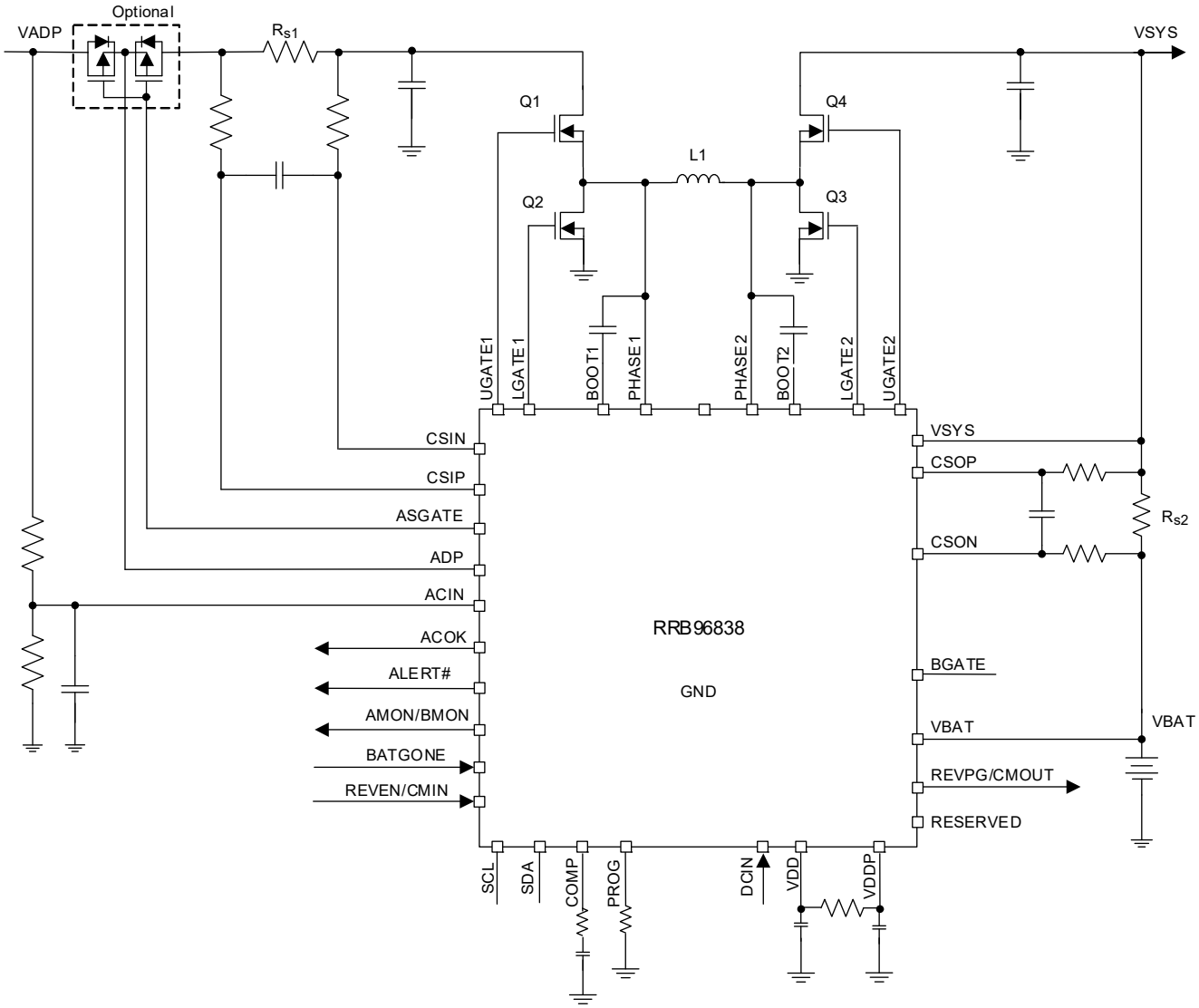


Figure 1. Circuit Topology for Battery-Charging Only Applications with No BFET

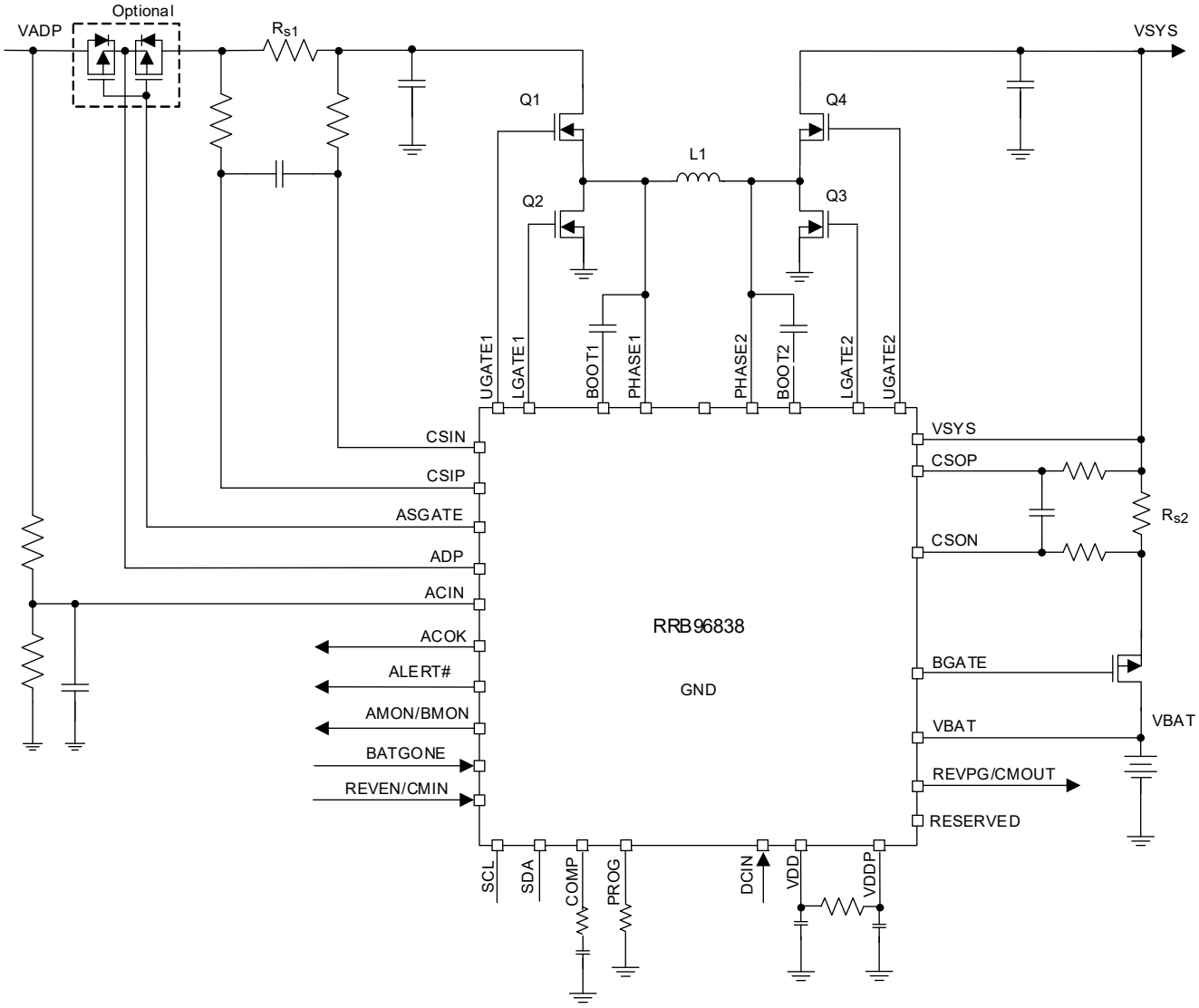


Figure 2. Circuit Topology for NVDC Charging with BFET

1.2 Block Diagram

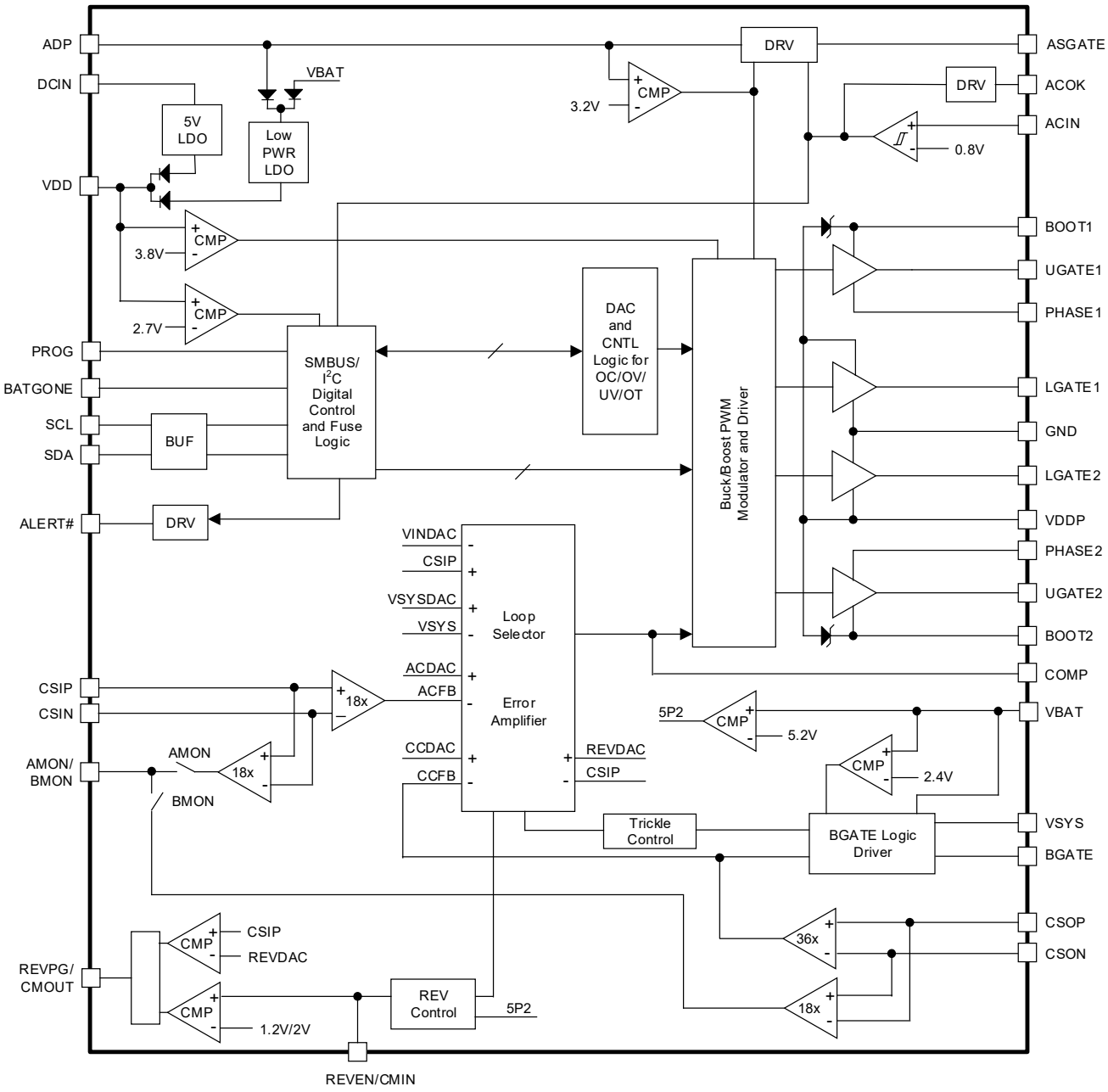


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

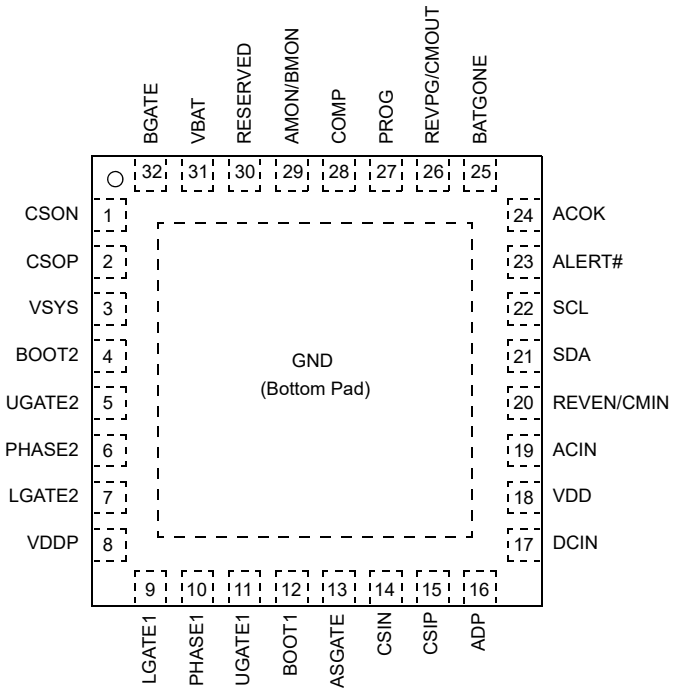


Figure 4. Pin assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat dissipation.
1	CSON	Battery current sense negative input. Connect to the battery current resistor negative input. Place a ceramic capacitor between CSOP to CSON to provide Differential mode filtering.
2	CSOP	Battery current sense positive input. Connect to the battery current resistor positive input. Place a ceramic capacitor between CSOP to CSON to provide Differential mode filtering.
3	VSYS	Provides feedback voltage for MaxSystemVoltage regulation.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins. Connect a 0.47µF bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain, and one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and the input terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.

Pin Number	Pin Name	Description
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins. Connect a 0.47µF bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional. If they are not used, leave the ASGATE pin floating. When ASGATE turns on, it is clamped 12V below the voltage of the ADP pin.
14	CSIN	Adapter current sense negative input.
15	CSIP	Adapter current sense positive input. The modulator also uses the CSIP pin for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Adapter input used to sense adapter voltage. ASGATE is turned on when the adapter voltage is higher than 3.2V. The ADP pin is also one of the two inputs to the internal low-power LDO.
17	DCIN	Internal LDO input that provides power to the IC. Connect a diode OR from the adapter and system outputs. Bypass DCIN with an MLCC capacitor. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7µF DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 20V.
18	VDD	Internal LDO output that provides the bias power for the internal analog and digital circuit. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V. If VDD is pulled below 2V for more than 1ms, the RRB96838 resets all the SMBus register values to their defaults.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.8V.
20	REVEN/ CMIN	Reverse Mode enable pin or stand-alone comparator input pin. Pull high to enable the Reverse mode. The Reverse mode is enabled when the control register is written to select Reverse mode and when the battery voltage is above 5.2V. When the Reverse mode is not selected, this pin is the general-purpose stand-alone comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
23	ALERT#	Open-drain output. Pulled low when ACHOT, DCHOT, or Low_VSYS are detected. Send an SMBus command to pull low with REVCURRENTHOT, BATGONE, ACOK, and the general-purpose comparator (see Table 11).
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	BATGONE	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high forces the BGATE FET to turn off in any circumstances.
26	REVPG/ CMOUT	Open-drain output. Reverse Mode output power-good indicator or stand-alone comparator output. When the Reverse Mode is enabled, this signal is low if the REV output voltage is not within the regulation window. When the Reverse Mode is not used, this signal is the general-purpose comparator output.
27	PROG	A resistor from the PROG pin to GND sets the following configurations: ▪ Default number of the battery cells in series: 2-, 3-, or 4-cell ▪ Default switching frequency: 733kHz or 1MHz ▪ Default adapter current limit value: 0.476A or 1.5A ▪ Autonomous Charging mode: Enabled or disabled See Table 23 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Adapter current, REV output current, battery charging current, or battery discharging current monitor output. ▪ V_{AMON} = 18x (V_{CSIP} - V_{CSIN}) for adapter current monitor ▪ $V_{REVCMON}$ = 18x (V_{CSIN} - V_{CSIP}) for REV output current monitor ▪ $V_{BMON\_DISCHARGING}$ = 18x (V_{CSON} - V_{CSOP}) for battery discharging current monitor ▪ $V_{BMON\_CHARGING}$ = 36x (V_{CSOP} - V_{CSON}) for battery charging current monitor
30	RESERVED	Reserved. Float this pin, do not connect

Pin Number	Pin Name	Description
31	VBAT	Battery voltage sensor. Used for trickle charging detection and Ideal Diode mode control. Connect a >1µF ceramic capacitor from VBAT to GND. The VBAT pin is also one of the two inputs to the internal low-power LDO.
32	BGATE	Gate drive output to the P-channel FET connecting the system and the battery. This pin can go high to disconnect the battery, or low to connect the battery or operate in Linear mode to regulate the trickle charge current during trickle charge. When BGATE turns on, it is clamped ~8.3V below the VSYS pin voltage. For applications having no BFET, leave BGATE floating.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Units
CSIP, CSIN, DCIN, ADP, ASGATE	-0.3	+28	V
PHASE1	GND - 0.3	+28	V
PHASE1	GND - 2 (<20ns)	+28	V
BOOT1, UGATE1	GND - 0.3	+33	V
PHASE2	GND - 0.3	+24	V
PHASE2	GND - 2 (<20ns)	+24	V
BOOT2, UGATE2	GND - 0.3	+29	V
LGATE1, LGATE2	GND - 0.3	+6.5	V
LGATE1, LGATE2	GND - 2 (<20ns)	+6.5	V
VBAT, VSYS, CSOP, CSON, BGATE	-0.3	+24	V
VDD, VDDP	-0.3	+6.5	V
COMP	-0.3	+6.5	V
AMON/BMON	-0.3	+6.5	V
REVEN, BATGONE	-0.3	+6.5	V
ACIN, ALERT#	-0.3	+6.5	V
SCL, SDA	-0.3	+6.5	V
BOOT1 - PHASE1, BOOT2 - PHASE2	-0.3	+6.5	V
CSIP - CSIN, CSOP - CSON	-0.3	+0.3	V
REVPG, ALERT#, ACOK	-	2	mA
Junction Temperature Range (T_J)	-10	+125	°C
Storage Temperature Range (T_S)	-65	+175	°C
Human Body Model (Tested per JS-001-2023)	-	2.5	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature	-10	+125	°C
Adapter Voltage	4	23	V
Ambient Temperature			
RRB96838-BU7/BT7	-10	+100	°C
RRB96838-BU8/BT8	-40	+100	°C

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	32 Ld TQFN Package	θ_{JA}[1]	Junction to ambient	37	°C/W
		θ_{JC}[2]	Junction to case	2	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r	-	**3.1**	3.3	**3.5**	V
VADP UVLO Hysteresis	VADP_UVLO_h	-	-	600	-	mV
V_{BAT} UVLO Rising	VBAT_UVLO_r	-	**2.30**	2.45	**2.65**	V
V_{BAT} UVLO Hysteresis	VBAT_UVLO_h	-	-	400	-	mV
V_{BAT} 5P2V Rising	VBAT_5P2_r	-	**5.05**	5.20	**5.7**	V
V_{BAT} 5P2V Hysteresis	VBAT_5P2_h	-	-	490	-	mV
VDD 2P7 POR Falling, SMBus and BGATE/BMON Active Threshold	VDD_2P7_f	-	**2.50**	2.70	**2.9**	V
VDD 2P7 POR Hysteresis	VDD_2P7_h	-	-	150	-	mV
VDD 3P8 POR Rising, Modulator and Gate Driver Active	VDD_3P8_r	-	**3.6**	3.8	**3.9**	V
VDD 3P8 POR Hysteresis	VDD_3P8_h	-	-	150	-	mV
ACIN Rising	ACIN_r	-	**0.775**	0.800	**0.825**	V
ACIN Hysteresis	ACIN_h	-	-	50	-	mV
Linear Regulator						
VDD Output Voltage	VDD	6V < V_{DCIN} < 23V, no load	**4.5**	5.0	**5.5**	V
VDD Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V	-	85	-	mV
VDD Overcurrent Threshold	VDD_OC	RRB96838-BU7/BT7	**80**	120	**155**	mA
VDD Overcurrent Threshold		RRB96838-BU8/BT8	**75**	120	**158**	mA
Battery Current	I_{BAT1}	Battery only, BGATE on, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}	-	24	**50**	µA
	I_{BAT2}	Battery only, BGATE on, BMON ON, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}	-	74	-	µA
Adapter Current Regulation, R_{S1} = 20mΩ						
Adapter Current Accuracy	-	CSIP - CSIN = 80mV	-	4	-	A
			-2	-	**2**	%
		CSIP - CSIN = 40mV	-	2	-	A
			-2.5	-	**2.5**	%
		CSIP - CSIN = 10mV	-	0.5	-	A
			-10	-	**10**	%

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Adapter Current ALERT# Threshold R_{s1} = 20mΩ	$I_{ADP\_HOT\_TH}$	ACALERT = 0x1580H (5504mA)	-	5504	-	mA
			-1.5	-	**1.5**	%
		ACALERT = 0x0A80H (2688mA)	-	2688	-	mA
			-3.0	-	**3.0**	%
		ACALERT = 0x0400H (1024mA)	-	1024	-	mA
			-6.0	-	**6.0**	%
System Voltage Regulation						
Maximum System Voltage Accuracy	-	MaxSystemVoltage for 2-cell (8.4V) (RRB96838-BU7/BT7)	**-0.6**	-	**0.6**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V) (RRB96838-BU7/BT7)	**-0.5**	-	**0.5**	%
	-	MaxSystemVoltage for 2-cell (8.4V) (RRB96838-BU8/BT8)	**-0.7**	-	**0.7**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V) (RRB96838-BU8/BT8)	**-0.5**	-	**0.5**	%
Minimum System Voltage Accuracy	-	VDAC = 5V to 14V	**-3**	-	**3**	%
Input Voltage Regulation Accuracy	-	Input Voltage Register = 4.096V	**3.98**	-	**4.22**	V
Charge Current Regulation, R_{s2} = 10mΩ (Limits apply across temperature range of 0°C to +85°C)						
Charge Current Accuracy	-	CSOP - CSON = 60mV	-	6	-	A
			-2.5	-	**2.5**	%
		CSOP - CSON = 20mV	-	2	-	A
			-4	-	**4**	%
		CSOP - CSON = 10mV	-	1	-	A
			-6	-	**6**	%
		CSOP - CSON = 5mV	-	0.5	-	A
			-12	-	**12**	%
BGATE Clamp						
VSYS - VBGATE ON	-	Charging enabled	**6.80**	8.30	**9.16**	V
VSYS - VBGATE OFF	-	Charging disabled	-	0	-	V
ASGATE Clamp						
VADP - VASGATE ON	-	-	-	12	-	V
VSYS - VBGATE OFF	-	-	-	0	-	V
Trickle Charging Current Regulation, R_{s2} = 10mΩ (Limits apply across temperature range of 0°C to +85°C)						
Trickle Charge Current Accuracy	-	Trickle, 512mA	**410**	512	**614**	mA
		Trickle, 256mA	**205**	256	**334**	mA
		Trickle, 128mA	**77**	128	**192**	mA
		Trickle, 64mA	**16**	64	**128**	mA
Fast Charge to Trickle Charge Threshold	-	V_{SYS} - V_{BGATE}	**4.23**	5.18	**5.97**	V
Trickle Charge to Fast Charge Threshold Hysteresis	-	V_{SYS} - V_{BGATE}	**50**	130	**260**	mV
Fast Charge to Trickle Charge BGATE Threshold	-	V_{SYS} > 7V, V_{FB} >> V_{REF}	-	1.15	-	V
Trickle Charge to Fast Charge BGATE Threshold Hysteresis	-	V_{SYS} > 7V, V_{FB} >> V_{REF}	-	50	-	mV

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Ideal Diode Mode						
Entering Ideal Diode Mode VSYS Voltage Threshold	-	BGATE off, VSYS falling V_{VBAT} - CSON	**100**	150	**200**	mV
Exiting Ideal Diode Mode Battery Discharging Current Threshold	-	R_{s2} = 10mΩ	**110**	200	**290**	mA
Exiting Ideal Diode Mode Battery Charging Current Threshold	-	R_{s2} = 10mΩ	**50**	130	**200**	mA
BGATE Source	-	VSYS - BGATE = 2V, charging disabled	**4**	6	**10**	mA
BGATE Sink	-	BGATE - GND = 2V, charging enabled	**20**	30	**40**	µA
BGATE Sink	-	BGATE - GND = 2V, in Ideal Diode mode	-	6	-	mA
AMON/BMON						
Input Current Sense Amplifier, R_{s1} = 20mΩ						
CSIP/CSIN Input Voltage Range	-	-	**4**	-	**23**	V
AMON Gain	-	-	-	17.97	-	V/V
AMON Accuracy V_{AMON} = 17.97 x (CSIP - CSIN)	-	V_{CSIP} - V_{CSIN} = 100mV (5A), CSIP = 5V, 20V	**-2**	-	**2**	%
	-	V_{CSIP} - V_{CSIN} = 20mV (1A), CSIP = 5V, 20V	**-5**	-	**5**	%
	-	V_{CSIP} - V_{CSIN} = 10mV (0.5A), CSIP = 5V, 20V	**-10**	-	**10**	%
	-	V_{CSIP} - V_{CSIN} = 2mV (0.1A), CSIP = 5V, 20V	**-40**	-	**40**	%
Reverse AMON Gain	-	-	-	17.9	-	V/V
Reverse AMON Accuracy V_{AMON} = 17.9 x (CSIN - CSIP)	-	V_{CSIN} - V_{CSIP} = 80mV (4A), CSIP = 4V, 22V	**-3**	-	**3**	%
	-	V_{CSIN} - V_{CSIP} = 20mV (1A), CSIP = 4V, 22V	**-6.5**	-	**5**	%
	-	V_{CSIN} - V_{CSIP} = 10mV (0.5A), CSIP = 4V, 22V	**-12**	-	**12**	%
	-	V_{CSIN} - V_{CSIP} = 5.12mV (0.256A), CSIP = 4V, 22V	**-25**	-	**25**	%
AMON Minimum Output Voltage	-	V_{CSIP} - V_{CSIN} = 0V	-	-	**30**	mV
Discharge Current Sense Amplifier, R_{s2} = 10mΩ						
BMON Gain (Battery Discharging)		-	-	17.97	-	V/V
BMON Accuracy V_{BMON} = 17.97 x (V_{CSON} - V_{CSOP})	-	V_{CSON} - V_{CSOP} = 100mV (10A), V_{CSON} = 8V	**-2.5**	-	**2.5**	%
		V_{CSON} - V_{CSOP} = 20mV (2A), V_{CSON} = 8V	**-7.0**	-1.5	**4.0**	%
		V_{CSON} - V_{CSOP} = 10mV (1A), V_{CSON} = 8V	**-10.5**	-2.5	**5.5**	%
		V_{CSON} - V_{CSOP} = 6mV (0.6A), V_{CSON} = 8V	**-17**	-4	**12**	%
Charge Current Sense Amplifier, R_{s2} = 10mΩ (Limits apply across the temperature range of 0°C to +85°C)						
BMON Gain (Battery Charging)	-	-	-	35.78	-	V/V
BMON Accuracy V_{BMON} = 35.78 x (V_{CSOP} - V_{CSON})	-	V_{CSOP} - V_{CSON} = 60mV (6A), V_{CSON} = 8V	**-3**	-	**3**	%
		V_{CSOP} - V_{CSON} = 40mV (4A), V_{CSON} = 8V	**-4**	-	**4**	%
		V_{CSOP} - V_{CSON} = 10mV (1A), V_{CSON} = 8V	**-10**	-	**10**	%
		V_{CSOP} - V_{CSON} = 5mV (0.5A), V_{CSON} = 8V	**-25**	-	**25**	%
BMON Minimum Output Voltage	-	V_{CSOP} - V_{CSON} = 0V	-	-	**30**	mV
Discharging Current ALERT# Threshold, R_{s2} = 10mΩ	$I_{DIS\_HOT\_TH}$	DCALERT = 2.048A	**1.77**	2.08	**2.39**	A
Discharging Current ALERT# Threshold, Battery Only, R_{s2} = 10mΩ	$I_{DIS\_HOT\_TH}$	DCALERT = 12A	**10.8**	13.5	**17**	A
		DCALERT = 6A	**5.2**	6.5	**8**	A
AMON/BMON Source Resistance[2]	-	-	-	-	**5**	Ω
AMON/BMON Sink Resistance[2]	-	-	-	-	**5**	Ω

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
BATGONE and REVEN						
High-Level Input Voltage	-	-	**0.9**	-	-	V
Low-Level Input Voltage	-	-	-	-	**0.4**	V
Pull-Down Current	-	BATGONE and REVEN = 5V	-	5	-	µA
ALERT#						
ALERT# Debounce Time	-	ALERT# Debounce register Bits[1:0] = 11	**0.85**	1	**1.15**	ms
		ALERT# Debounce register Bits[1:0] = 10	**425**	500	**575**	µs
ALERT# Duration Time	-	ALERT# Duration register Bits[2:0] = 011	**8.5**	10	**11.5**	ms
		ALERT# Duration register Bits[2:0] = 001	**17**	20	**23**	ms
Low VSYS ALERT# Trip Threshold	$V_{LOW\_VSYS\_HOT}$	Control1 register Bits[1:0] = 00	**5.8**	6.0	**6.2**	V
		Control1 register Bits[1:0] = 01	**6.1**	6.3	**6.5**	V
		Control1 register Bits[1:0] = 10	**6.4**	6.6	**6.8**	V
		Control1 register Bits[1:0] = 11	**6.7**	6.9	**7.1**	V
REV						
REV Voltage	-	REV Voltage register = 5.004V	**4.95**	5.03	**5.12**	V
REV Current (5V to 12V)	-	REV Current register = 512mA	**435**	512	**600**	mA
		REV Current register = 1024mA	**922**	1024	**1126**	mA
		REV Current register = 4096mA	**3975**	4096	**4250**	mA
General Purpose Comparator						
General Purpose Comparator Rising Threshold	-	Reference = 1.2V	**1.11**	1.2	**1.29**	V
		Reference = 2V	**1.95**	2	**2.05**	V
General Purpose Comparator Hysteresis	-	Reference = 1.2V	-	45	-	mV
		Reference = 2V	-	45	-	mV
Protection						
VSYS Overvoltage Rising Threshold	-	MaxSystemVoltage register value = 8.4V	**8.92**	9.15	**9.38**	V
VSYS Overvoltage Hysteresis	-	MaxSystemVoltage register value = 8.4V	**250**	400	**550**	mV
VSYS UV Falling Threshold	-	Control6 Register Bits[2:0] = 001	-	3	-	V
		Control6 Register Bits[2:0] = 010	-	3.9	-	V
		Control6 Register Bits[2:0] = 011	-	4.8	-	V
		Control6 Register Bits[2:0] = 100	-	5.7	-	V
		Control6 Register Bits[2:0] = 101	-	6.6	-	V
		Control6 Register Bits[2:0] = 110	-	7.5	-	V
		Control6 Register Bits[2:0] = 111	-	8.4	-	V
VSYS OK Threshold	-	-	**0.45**	0.6	**0.75**	V
VSYS OK Source Current	-	-	-	10	-	mA
Over-Temperature Threshold[2]	-	-	**140**	150	**160**	°C
Adapter Overvoltage Rising Threshold	-	-	**22.5**	23.4	**24**	V
Adapter Overvoltage Hysteresis	-	-	**150**	350	**500**	mV
REV Undervoltage Falling Threshold	-	REV voltage = 5.004V	**3.45**	3.80	**4.25**	V
REV Overvoltage Rising Threshold	-	REV voltage = 5.004V	**5.8**	6.2	**6.6**	V

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Oscillator						
Oscillator Frequency, Digital Core Only	-	-	**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy[2]	-	-	**-15**	-	**15**	%
Miscellaneous						
Switching Frequency Accuracy	-	COMP > 1.7V and not in period stretching	**-15**	-	**15**	%
Battery Learn Mode Auto-Exit Threshold	-	MinSystemVoltage = 5.376V Control1 register Bit[13] = 1	**5.05**	5.35	**5.7**	V
Battery Learn Mode Auto-Exit Hysteresis[2]	-	MinSystemVoltage = 5.376V Control1 register Bit[13] = 1	**180**	330	**480**	mV
ADP Discharge Current	-	ADP = 5V to 20V	-	15	-	mA
VSYS Discharge Current	-	VSYS = 5V to 18V	-	10	-	mA
SMBus						
SDA/SCL Input Low Voltage	-	-	-	-	**0.6**	V
SDA/SCL Input High Voltage	-	-	**1.3**	-	-	V
SDA/SCL Input Bias Current	-	-	-	-	**1**	µA
SDA, Output Sink Current	-	SDA = 0.4V	**4**	-	-	mA
SMBus Frequency	f_{SMB}	-	**10**	-	**400**	kHz
Gate Driver[2]						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current	-	800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2	-	A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current	-	350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8	-	A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current	-	800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2	-	A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current	-	300	**450**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5	-	A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current	-	800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2	-	A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current	-	300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5	-	A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current	-	800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2	-	A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current	-	300	**450**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**2.3**	3.5	-	A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$	-	**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$	-	**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$	-	**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$	-	**10**	20	**40**	ns

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Limits established by characterization and are not production tested.

3.5 SMBus Timing Specification

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
SMBus Frequency	F_{SMB}	-	10	-	400	kHz
Bus Free Time	t_{BUF}	-	4.7	-	-	µs
Start Condition Hold Time from SCL	$t_{HD:STA}$	-	4	-	-	µs
Start Condition Setup Time from SCL	$t_{SU:STA}$	-	4.7	-	-	µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$	-	4	-	-	µs
SDA Hold Time from SCL	$t_{HD:DAT}$	-	300	-	-	ns
SDA Setup Time from SCL	$t_{SU:DAT}$	-	250	-	-	ns
SCL Low Period	t_{LOW}	-	4.7	-	-	µs
SCL High Period	t_{HIGH}	-	4	-	-	µs
SMBus Inactivity Timeout	-	Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register	-	175	-	s

1. Limits established by characterization and are not production tested.

3.6 Gate Driver Timing Diagrams

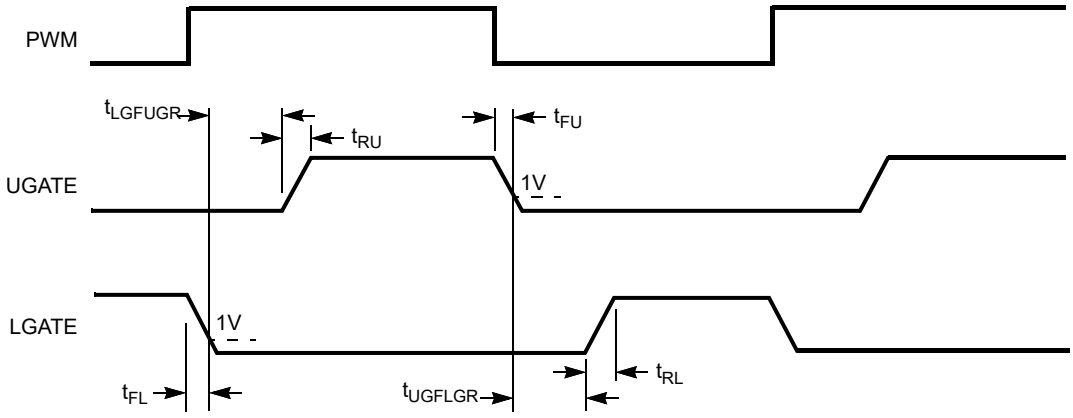


Figure 5. Gate Driver Timing Diagram

4. Typical Performance Curves

4.1 Battery Charging Only (No BFET)

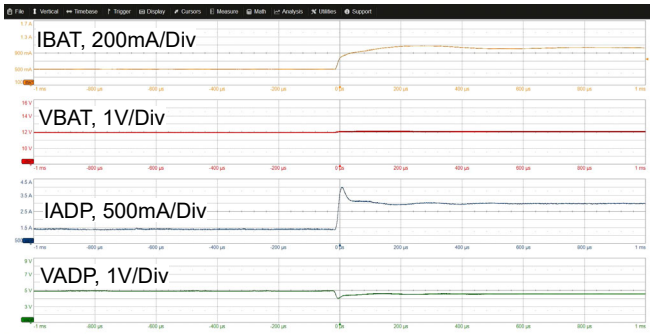


Figure 6. Boost Mode: Charge Current Loop to Adapter Current Loop, V_{ADP} = 5V, V_{BAT} = 12V, AdapterCurrentLimit = 3A, ChargeCurrent: 0.5A → 1.5A

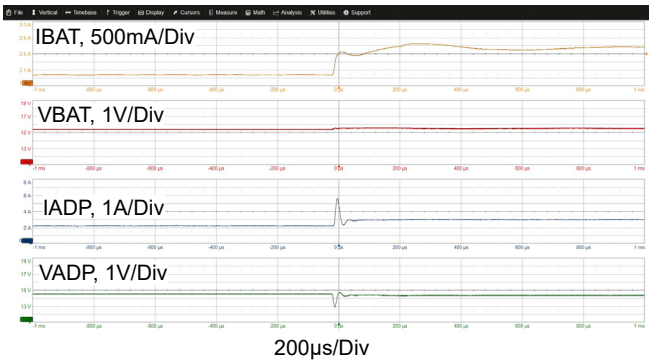


Figure 7. Buck_Boost Mode: Charge Current Loop to Adapter Current Loop, V_{ADP} = 15V, V_{BAT} = 15V, AdapterCurrentLimit = 3A, ChargeCurrent: 2A → 4A

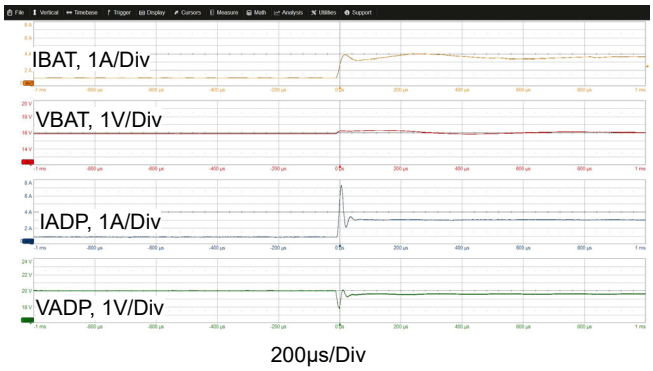


Figure 8. `Buck Mode: Charge Current Loop to Adapter Current Loop, V_{ADP} = 20V, V_{BAT} = 16V, AdapterCurrentLimit = 3A, ChargeCurrent: 1A → 6A

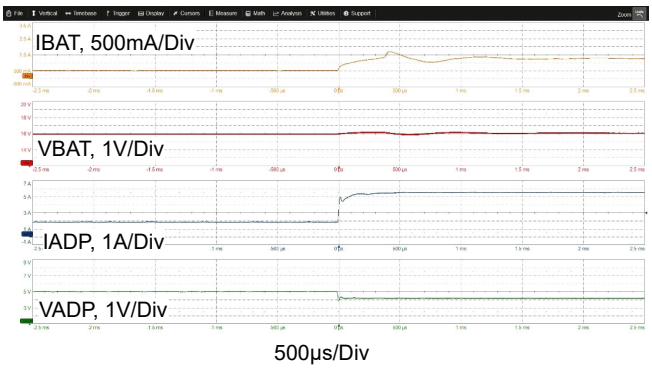


Figure 9. Boost Mode: Charge Current Loop to Input Voltage Loop, V_{ADP} = 5V, V_{BAT} = 16V, ChargeCurrent: 0.5A → 2A, InputVoltageLimit = 4.096V

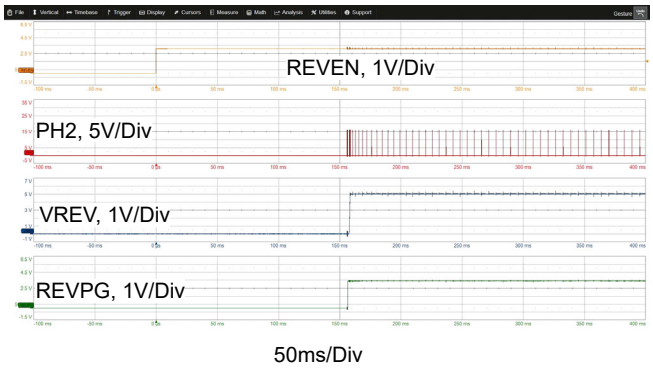


Figure 10. REV Mode Enable, REV_Debounce = 150ms, V_{BAT} = 16V, V_{REV} = 5V

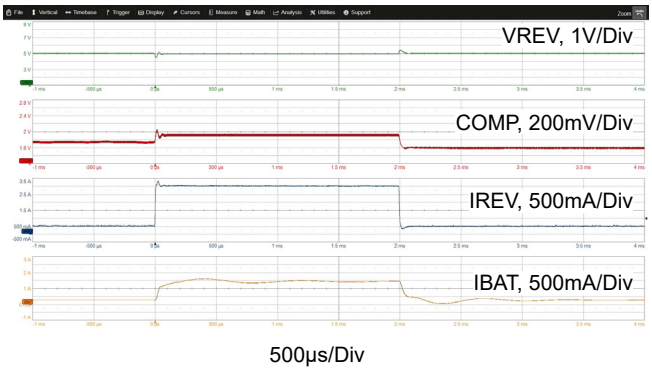


Figure 11. REV Mode Transients, V_{BAT} = 12V, V_{REV} = 5V, REV Load: 0.5A ↔ 3A

4.2 NVDC Charging (with BFET)

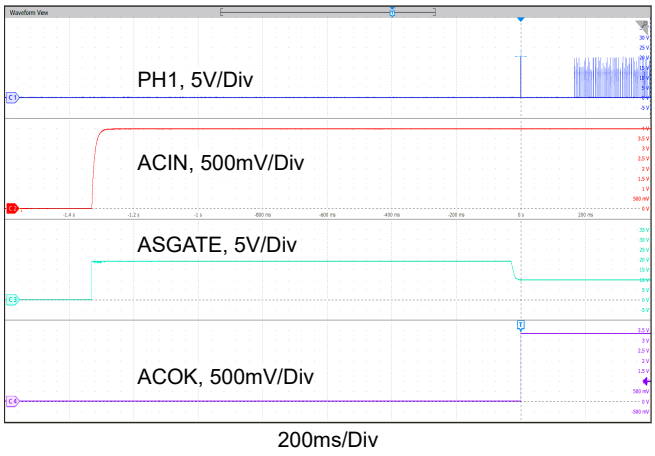


Figure 12. Adapter Insertion, V_{ADP} = 20V, V_{BAT} = 11V, ChargeCurrent = 0A

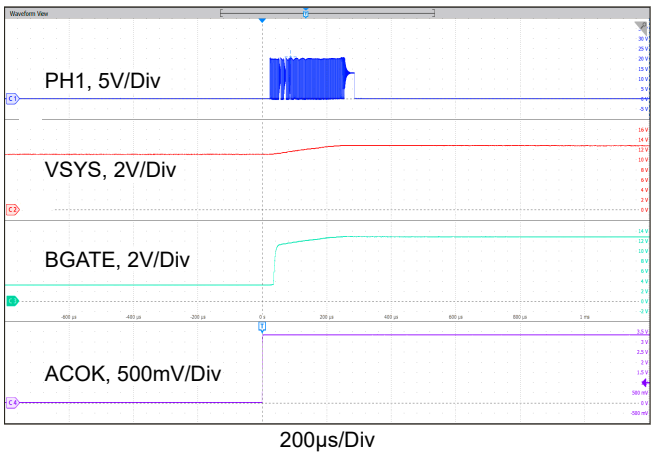


Figure 13. Adapter Insertion, V_{ADP} = 20V, V_{BAT} = 11V, ChargeCurrent = 0A (Figure 12 Zoomed In)

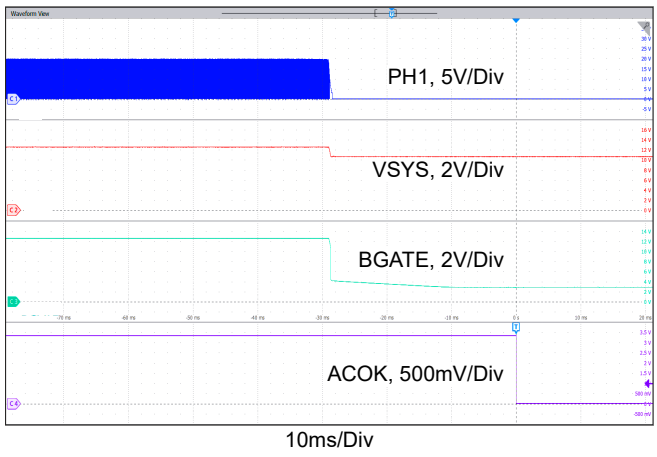


Figure 14. Adapter Removal, V_{ADP} = 20V, V_{BAT} = 11V, ChargeCurrent = 0A

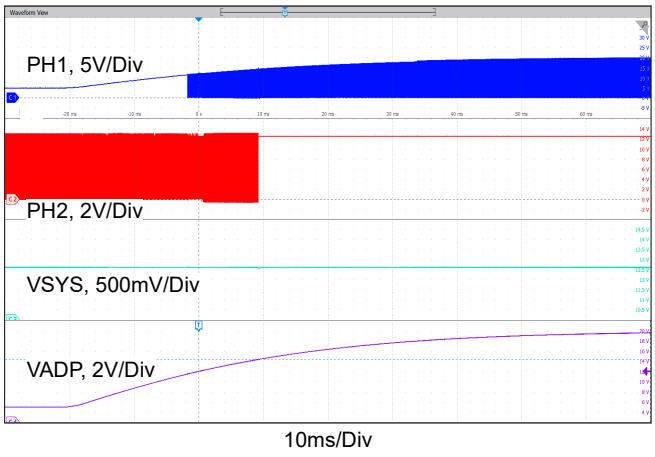


Figure 15. Adapter Voltage Ramps Up, Boost -> Buck-Boost -> Buck Operation Mode Transition

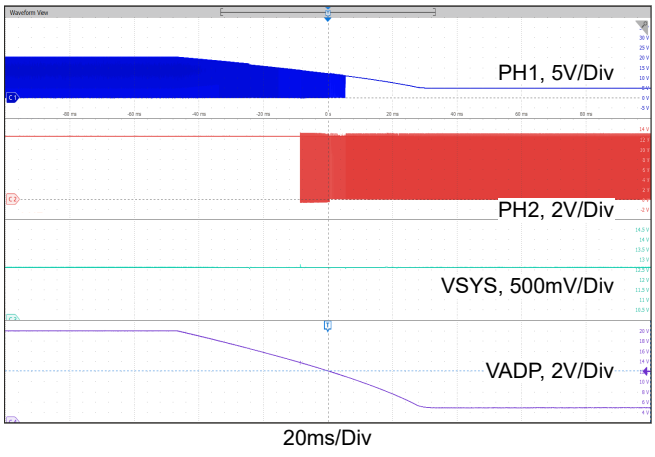


Figure 16. Adapter Voltage Ramps Down, Buck -> Buck-Boost -> Boost Operation Mode Transition

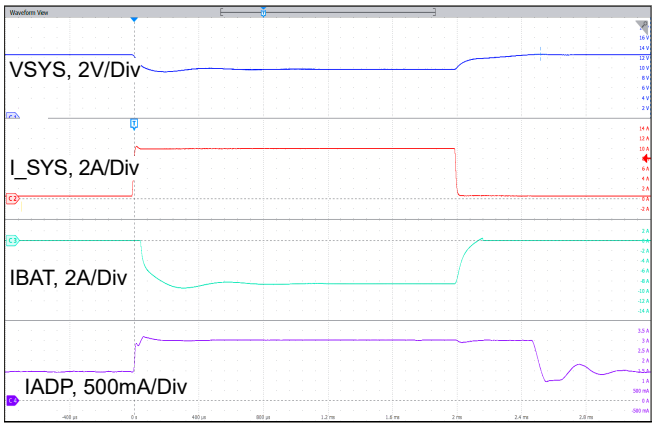


Figure 17. Boost Mode, Output Voltage Loop to Adapter Current Loop Transition. V_{ADP} = 5V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 0.5A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0A

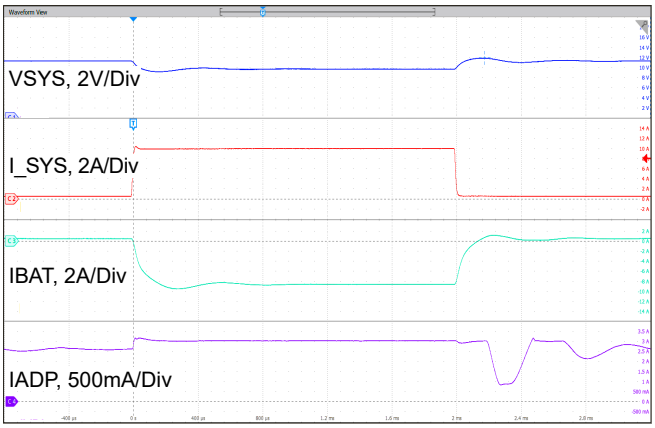


Figure 18. Boost Mode, Charging Current Loop to Adapter Current Loop Transition. V_{ADP} = 5V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 0.5A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0.5A

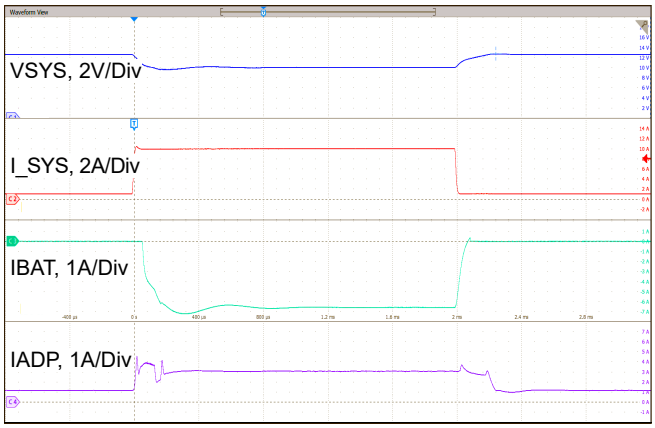


Figure 19. Buck-Boost Mode, Output Voltage Loop to Adapter Current Loop Transition. V_{ADP} = 12V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0A

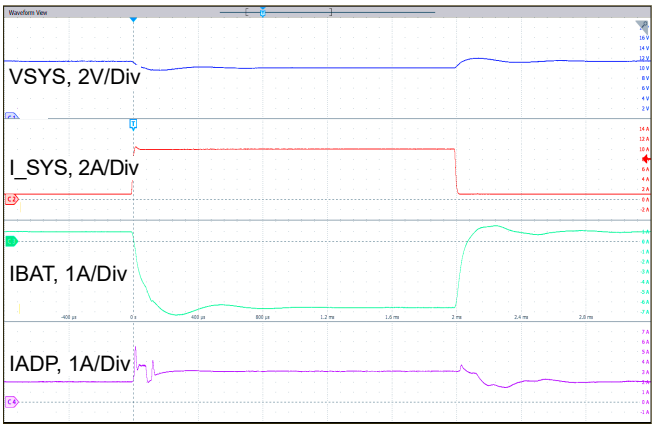


Figure 20. Buck-Boost Mode, Charging Current Loop to Adapter Current Loop Transition. V_{ADP} = 12V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 1A

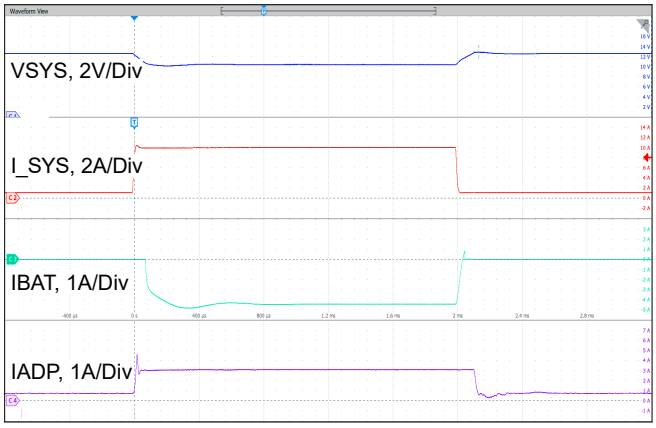


Figure 21. Buck Mode, Output Voltage Loop to Adapter Current Loop Transition. V_{ADP} = 20V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0A

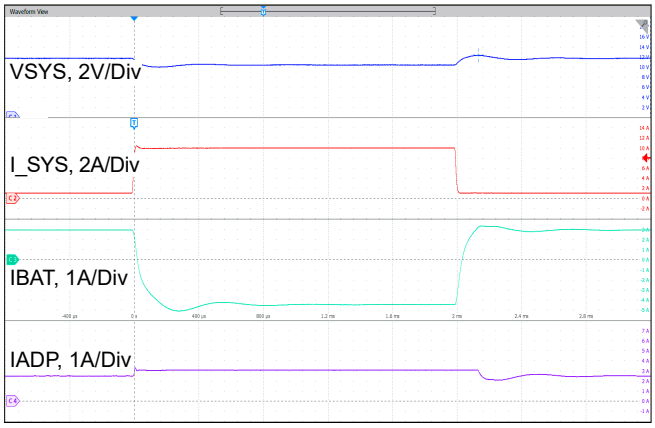


Figure 22. Buck Mode, Charging Current Loop to Adapter Current Loop Transition. V_{ADP} = 20V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 3A

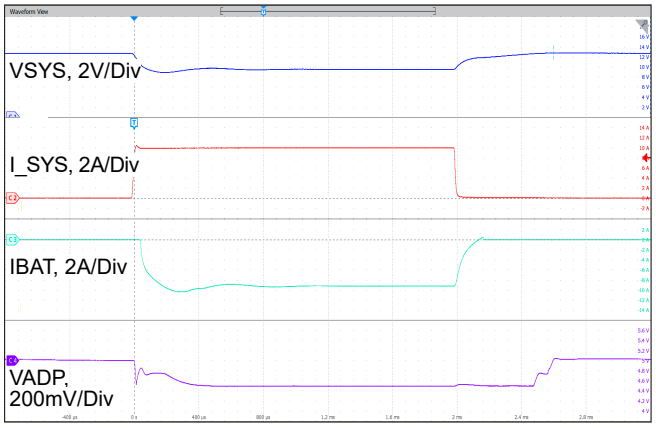


Figure 23. Boost Mode, Output Voltage Loop to Input Voltage Loop Transition. V_{ADP} = 5.004V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, VINDAC = 4.437V, System Load 0A to 10A Step, ChargeCurrent = 0A

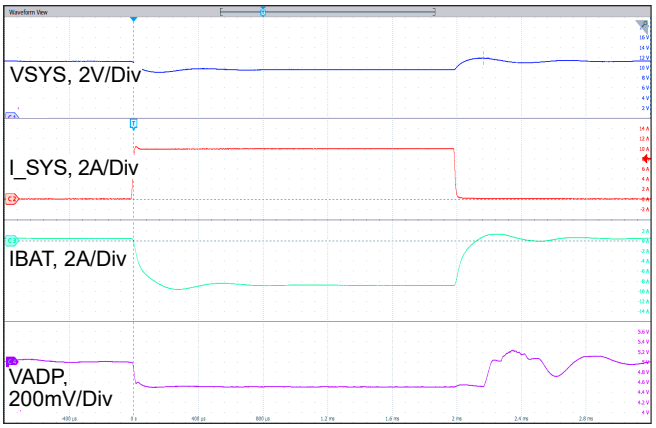


Figure 24. Boost Mode, Charging Current Loop to Input Voltage Loop Transition. V_{ADP} = 5.004V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, VINDAC = 4.437V, System Load 0A to 10A Step, ChargeCurrent = 0.5A

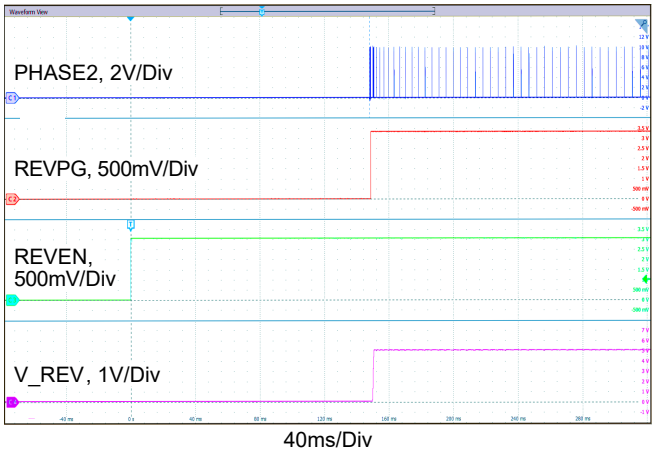


Figure 25. REV Mode Enable, REV Enable 150ms Debounce Time

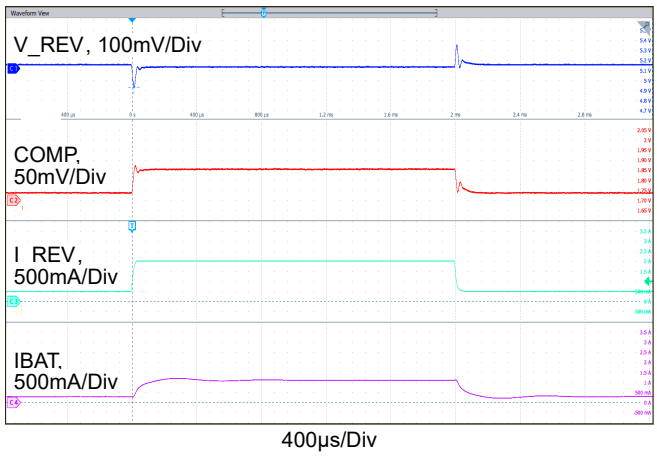


Figure 26. REV Mode 0.5A to 2A Transient Load, REV Voltage = 5.12V

5. General SMBus Architecture

Figure 27 shows the general SMBus Architecture.

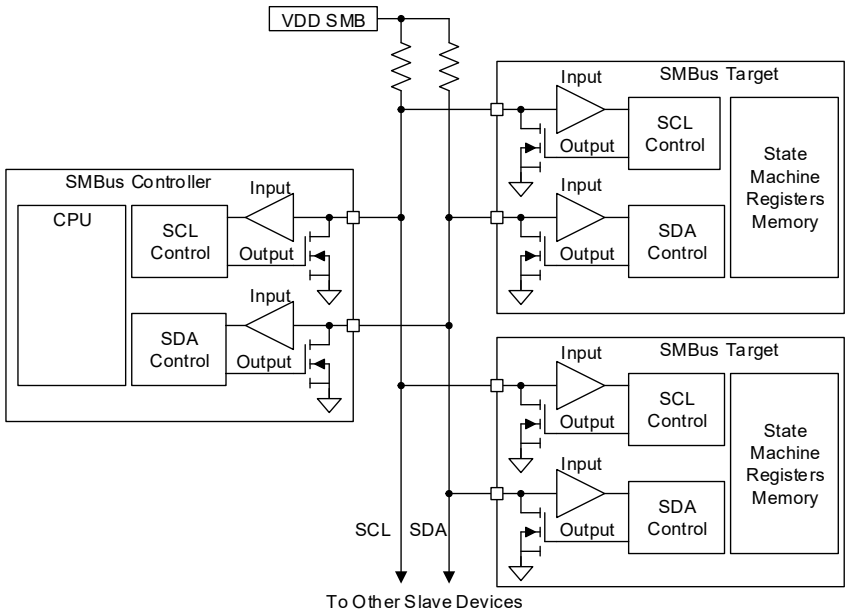


Figure 27. General SMBus

5.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 28.

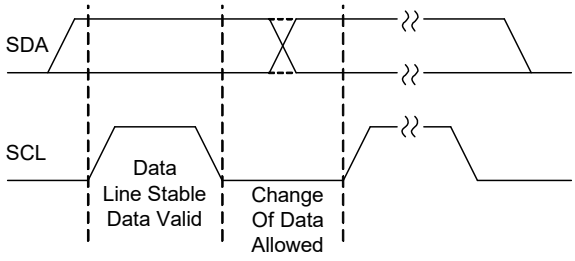


Figure 28. Data Validity

5.2 START and STOP Conditions

In Figure 29, the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

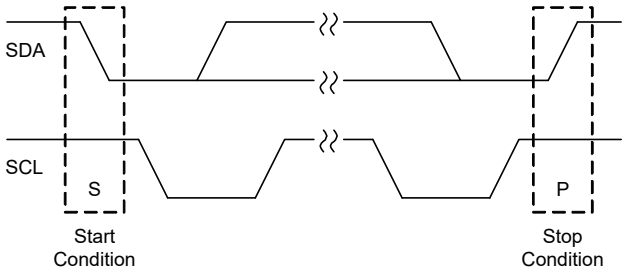


Figure 29. Start and Stop Waveforms

5.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the controller sends seven target address bits and a R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line LOW to acknowledge (see Figure 30). Both the controller and the target use the ACK bit to acknowledge receipt of register addresses and data.

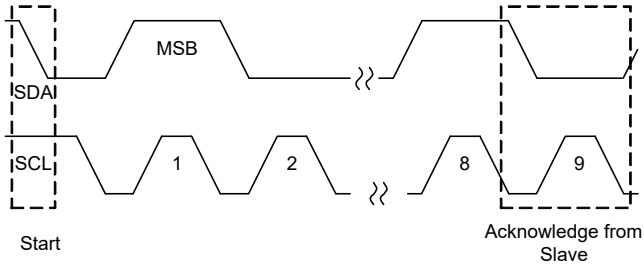


Figure 30. Acknowledge On The SMBus

5.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus controller device. The control byte begins with a Start condition followed by seven bits of target address (0001001) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any target device on the SMBus bus recognizes its address, it acknowledges by pulling the

Serial Data (SDA) line LOW for the last clock cycle in the control byte. If no target exists at that address or it is not ready to communicate, the data line is 1 indicating a not acknowledge condition.

When the control byte is sent and the RRB96838 acknowledges it, the second byte sent by the controller must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the RRB96838 which register the controller writes or reads. See Table 1 for register details. When the RRB96838 receives a register address byte, it responds with an acknowledge.

5.5 Byte Format

Every byte on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO Byte data is transferred before the HI Byte data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

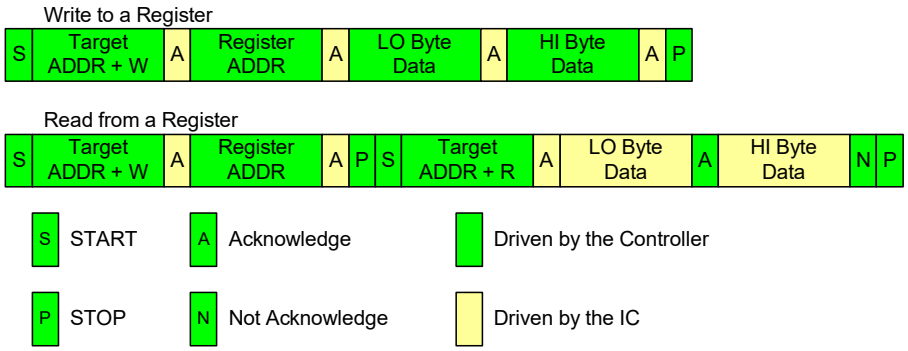


Figure 31. SMBus Read and Write Protocol

5.6 SMBus and I²C Compatibility

The RRB96838 SMBus minimum input logic high voltage is 1.3V, so it is compatible with I²C with pull-up power supplies higher than 1.3V.

The RRB96838 SMBus registers are 16 bits, so it is compatible with 16-bit I²C or 8-bit I²C with auto-increment capability.

6. SMBus Commands

The RRB96838 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification. The RRB96838 uses the SMBus Read-word and Write-word protocols (see Figure 31) to communicate with the host system and a smart battery. The RRB96838 is an SMBus target device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ as follows:

The Read and Write address for the RRB96838 is:

- Read address = 0b00010011 (0X13H)
- Write address = 0b00010010 (0X12H)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The information in this datasheet is based on current sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless otherwise specified.

Table 1. Register Summary

Register Names	Register Address	Read/ Write	# of Bits	Description	Default
ChargeCurrentLimit	0x14	R/W	11	[12:2] 11-bit, LSB size 4mA, total range 6080mA with 10mΩ R_{S2}	0A
MaxSystemVoltage	0x15	R/W	12	[14:3] 12-bit, LSB size 8mV, total range 18.304V	8.384V for 2-cell
					12.576V for 3-cell
					16.768V for 4-cell
Control0	0x39	R/W	16	Configures various charger options	0x0000h
Information1	0x3A	R	16	Indicates various charger statuses	0x0000h
Control1	0x3C	R/W	16	Configures various charger options	0x0000h
Control2	0x3D	R/W	16	Configures various charger options	0x0000h
MinSystemVoltage	0x3E	R/W	6	[13:8] 6-bit, LSB size 256mV, total range 13.824V	5.12V for 2-cell
					7.68V for 3-cell
					10.24V for 4-cell
AdapterCurrentLimit	0x3F	R/W	11	[12:2] 11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	Set by PROG pin
Revision ID	0x44	R	8	Revision ID register - Read only	0x01h
ACALERT#	0x47	R/W	6	[12:7] Adapter current ALERT# threshold Default 3.072A, 128mA resolution for 20mΩ R_{s1}.	3.072A
DCALERT#	0x48	R/W	6	[13:8] Battery discharging current ALERT# threshold Default 4.096A, 256mA resolution for 10mΩ R_{s2}.	4.096A
REV Voltage	0x49	R/W	12	[14:3] 12-bit, LSB size 12mV, total range 27.456V REV mode voltage reference	5.004V
REV Current	0x4A	R/W	6	[12:5] 8-bit, LSB size 32mA, total range 4.096A REV mode maximum current limit	0.512A
V_{IN} Voltage	0x4B	R/W	6	[13:8] 6-bit, LSB size 341.3mV, total range 18.432mV V_{IN} loop voltage reference	4.096V
Control3	0x4C	R/W	16	Configures various charger options	0x0000h
Information2	0x4D	R	16	Indicates various charger statuses	0x0000h
Control4	0x4E	R/W	16	Configures various charger options	0x0000h
Control6	0x37	R/W	8	[7:0] 8-bit, configures various charger options	0x0000h or 0x0003h[1]
Information3	0x90	R	1	[1] 1-bit, indicates pass-through mode status	0x0000h
Manufacturer ID	0xFE	R	8	Manufacturer ID register – 0x49 - Read only	0x0049h
Device ID	0xFF	R	8	Device ID register - 0x0C- Read only	0x000Ch

1. When inserting the battery for the first time, VSYS UV by default is 000 = Disabled. When inserting the adapter, VSYS UV threshold by default is 011 = 4.8V.

6.1 Setting the Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0x14H or 0b00010100) using the Write-word protocol shown in Figure 31 and the data format shown in Table 2 for a 10mΩ R_{s2} and a 5mΩ R_{s2}.

The RRB96838 limits the charging current by limiting the CSOP-CSON voltage. By using the recommended current sense resistor values R_{s1} = 20mΩ and R_{s2} = 10mΩ, the LSB of the register translates to 4mA of charging current (if Control3 register Bit[6] = 0). The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register and the maximum value is clamped at 6080mA for R_{s2} = 10mΩ.

The ChargeCurrentLimit register is reset to 0x0000H after POR. To set the battery charging current value, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

Table 2 shows the conditions to enable fast charging according to the ChargeCurrentLimit register setting.

Table 2. ChargeCurrentLimit Register 0x14H (11-Bit)

Bit	Description	
	4mA Step, 10mΩ Sense Resistor	8mA Step, 5mΩ Sense Resistor
[1:0]	Not used	Not used
[2]	0 = Add 0mA of charge current limit. 1 = Add 4mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
[3]	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
[4]	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
[5]	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
[6]	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
[7]	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
[8]	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
[9]	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
[10]	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
[11]	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
[12]	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.	0 = Add 0mA of charge current limit. 1 = Add 8192mA of charge current limit.
[13:15]	Not used	Not used
Maximum	[12:2] = 10111110000 6080mA	[12:2] = 10111110000 12160mA

6.2 Setting the Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit command (0x3FH or 0b00111111) using the Write-word protocol shown in Figure 31 and the data format shown in Table 3 for a 20mΩ R_{s1} and a 10mΩ R_{s1}.

The RRB96838 limits the adapter current by limiting the CSIP-CSIN voltage. By using the recommended current sense resistor values, the LSB of the register translates to 4mA of adapter current. Any adapter current limit command is accepted, but only the valid register bits are written to the AdapterCurrentLimit register and the maximum value is clamped at 6080mA for R_{s1} = 20mΩ.

After adapter POR, the AdapterCurrentLimit register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit register can be read back to verify its content.

Table 3. AdapterCurrentLimit Register 0x3FH (11-Bit)

Bit	Description	
	4mA Step, 20mΩ Sense Resistor	8mA Step, 10mΩ Sense Resistor
[1:0]	Not used	Not used
[2]	0 = Add 0mA of adapter current limit. 1 = Add 4mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
[3]	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
[4]	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
[5]	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
[6]	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
[7]	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
[8]	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
[9]	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
[10]	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
[11]	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
[12]	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.	0 = Add 0mA of adapter current limit. 1 = Add 8192mA of adapter current limit.
[13:15]	Not used	Not used
Maximum	[12:4] = 10111110000 6080mA	[12:4] = 10111110000 12160mA

6.3 Setting the Maximum Charging Voltage or System Regulating Voltage

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command (0x15H or 0b00010101) using the Write-word protocol shown in Figure 31 and the data format shown in Table 4.

The maximum system voltage range is 8mV to 18.304V. The MaxSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register and the maximum value is clamped at 18.304V. The RRB96838 accepts a 0V command, but the register value does not change.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting is also the system bus voltage regulation point when the battery is absent, or if the battery is present but is not in Charging mode. See System Voltage Regulation and Trickle Charging for details.

The VSYS pin senses the battery voltage for maximum charging voltage regulation. The VSYS pin is also the system bus voltage regulation sense point.

Table 4. MaxSystemVoltage Register 0x15H (8mV Step)

Bit	Description
[2:0]	Not used
[3]	0 = Add 0mV of charge voltage. 1 = Add 8mV of charge voltage.
[4]	0 = Add 0mV of charge voltage. 1 = Add 16mV of charge voltage.
[5]	0 = Add 0mV of charge voltage. 1 = Add 32mV of charge voltage.
[6]	0 = Add 0mV of charge voltage. 1 = Add 64mV of charge voltage.
[7]	0 = Add 0mV of charge voltage. 1 = Add 128mV of charge voltage.
[8]	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
[9]	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
[10]	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
[11]	0 = Add 0mV of charge voltage. 1 = Add 2048mV of charge voltage.
[12]	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
[13]	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
[14]	0 = Add 0mV of charge voltage. 1 = Add 16384mV of charge voltage.
[15]	Not used
Maximum	18304mV

6.4 Setting the Minimum System Voltage

To set the minimum system voltage, write a 16-bit MinSystemVoltage command (0x3EH or 0b00111110) using the Write-word protocol shown in Figure 31 and the data format shown in Table 5.

Table 5. MinSystemVoltage Register 0x3EH

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
[9]	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
[10]	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
[11]	0 = Add 0mV of charge voltage. 1 = Add 2048mV of charge voltage.
[12]	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
[13]	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
[15:14]	Not used
Maximum	13824mV

The minimum system voltage range is 256mV to 13.824V. The MinSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value and the value is clamped at 13.824V.

The MinSystemVoltage register sets the battery voltage threshold for entry and exit of Trickle Charging mode and for entry and exit of Learn mode. The VBAT pin senses the battery voltage to compare with the MinSystemVoltage register setting. See Battery Learn Mode for details.

The MinSystemVoltage register setting is also the system voltage regulation point when it is in Trickle Charging mode. The VSYS pin is the system voltage regulation sense point in Trickle Charging mode. See System Voltage Regulation and Trickle Charging for details.

6.5 Setting the ALERT# Threshold for Adapter Overcurrent Conditions

To set the ALERT# assertion threshold for adapter overcurrent conditions, write a 16-bit ACALERT# command (0x47H or 0b01000111) using the Write-word protocol shown in Figure 31 and the data format shown in Table 6. By using the recommended current sense resistor values, the LSB of the register translates to 128mA of adapter current. The ACALERT# register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 6400mA for R_{s1} = 20mΩ.

Table 6. ACALERT# Register 0x47H (20mΩ Sensing Resistor, 128mA Step, x18 Gain)

Bit	Description
[6:0]	Not used
[7]	0 = Add 0mA of ACALERT# threshold. 1 = Add 128mA of ACALERT# threshold.
[8]	0 = Add 0mA of ACALERT# threshold. 1 = Add 256mA of ACALERT# threshold.
[9]	0 = Add 0mA of ACALERT# threshold. 1 = Add 512mA of ACALERT# threshold.
[10]	0 = Add 0mA of ACALERT# threshold. 1 = Add 1024mA of ACALERT# threshold.
[11]	0 = Add 0mA of ACALERT# threshold. 1 = Add 2048mA of ACALERT# threshold.
[12]	0 = Add 0mA of ACALERT# threshold. 1 = Add 4096mA of ACALERT# threshold.
[15:13]	Not used
Maximum	[12:7] = 110010, 6400mA

After POR, the ACALERT# register is reset to 0x0C00H. The ACALERT# register can be read back to verify its content.

If the adapter current exceeds the ACALERT# register setting, the ALERT# signal asserts after the debounce time programmed by the Control2 register Bits[10:9] and latches on for the minimum time programmed by Control2 register Bits[8:6].

6.6 Setting the ALERT# Threshold for the Battery Over Discharging Current Condition

To set the ALERT# signal assertion threshold for the battery over discharging current condition, write a 16-bit DCALERT# command (0x48H or 0b01001000) using the Write-word protocol shown in Figure 31 and the data format shown in Table 7. By using the recommended current sense resistor values, the LSB of the register translates to 256mA of adapter current. The DCALERT# register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 12.8A for R_{s2} = 10mΩ.

After POR, the DCALERT# register is reset to 0x1000H. The DCALERT# register can be read back to verify its content.

If the battery discharging current exceeds the DCALERT# register setting, the ALERT# signal asserts after the debounce time programmed by the Control2 register Bits[10:9] and latches on for the minimum time programmed by Control2 register Bits[8:6].

In normal mode, the Alert# signal assertion threshold for battery over discharging current conditions is set by the DCALERT# value in DAC register 0x48. In battery-only low-power mode, the battery over-discharging threshold is set by the DCALERT# level configured by Control0 register Bits[4:3].

Table 7. DCALERT# Register 0x48H (10mΩ Sensing Resistor, 256mA Step, x18 Gain)

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mA of DCALERT# threshold. 1 = Add 256mA of DCALERT# threshold.
[9]	0 = Add 0mA of DCALERT# threshold. 1 = Add 512mA of DCALERT# threshold.
[10]	0 = Add 0mA of DCALERT# threshold. 1 = Add 1024mA of DCALERT# threshold.
[11]	0 = Add 0mA of DCALERT# threshold. 1 = Add 2048mA of DCALERT# threshold.
[12]	0 = Add 0mA of DCALERT# threshold. 1 = Add 4096mA of DCALERT# threshold.
[13]	0 = Add 0mA of DCALERT# threshold. 1 = Add 8192mA of DCALERT# threshold.
[15:14]	Not used.
Maximum	[13:8] = 110010, 12800mA

6.7 Setting the ALERT# Debounce Time and Duration Time

Control2 register Bits[10:9] configures the ALERT# signal debounce time before its assertion for ACALERT# and DCALERT#. The low system voltage ALERT# has a fixed debounce time of 8µs.

Control2 register Bits[8:6] configures the minimum duration of the ALERT# signal when asserted.

6.8 Setting the Control Registers

Control0, Control1, Control2, Control3, Control4, and Control6 registers configure the RRB96838 operation. To change certain functions or options after POR, write control commands to any of the following control registers using the Write-word protocol shown in Figure 31 and the data format shown in Table 8 through Table 13.

- 16-bit control command to the Control0 register (0x39H or 0b00111001)
- 16-bit control command to the Control1 register (0x3CH or 0b00111100)
- 16-bit control command to the Control2 register (0x3DH or 0b00111101)
- 16-bit control command to the Control3 register (0x4CH or 0b00111100)
- 16-bit control command to the Control4 register (0x4EH or 0b00111101)
- 16-bit control command to the Control5 register (0x38H or 0b00111000)
- 8-bit control command to the Control6 register (0x37H or 0b00110111)

Table 8. Control0 Register 0x39H

Bit	Bit Name	Description
[15:13]	Forward Buck Phase Comparator Threshold Offset	Bits[15:13] adjusts the phase comparator threshold offset for forward buck mode. 000 = 0mV 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[12:10]	Forward Buck-boost, Forward Boost, and Reverse Boost Phase Comparator Threshold Offset	Bits[12:10] adjusts the phase comparator threshold offset for Forward Buck-boost, Forward Boost, and Reverse Boost modes. 000 = 0mV 001 = 0.5mV 010 = 1mV 011 = 1.5mV 100 = -2mV 101 = -1.5mV 110 = -1mV 111 = -0.5mV
[9,8,0]	Reverse Buck and Reverse Buck Boost Phase Comparator Threshold Offset	Bits[9,8,0] adjusts the phase comparator threshold offset for Reverse Buck and Reverse Buck Boost modes. 000 = 0mV 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[7]	SMBus Timeout	The RRB96838 includes a timer to ensure the SMBus controller is active and to prevent overcharging the battery in NVDC applications that include a BFET. If the adapter is present and if the RRB96838 does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, the RRB96838 terminates charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register re-enables charging.For general battery charging without a BFET, the SMBus timeout function must be disabled. 0 = Enable the SMBus timeout function 1 = Disable the SMBus timeout function
[6:5]	High-Side FET Short Detection Threshold	Bits[6:5] configures the high-side FET short detection PHASE node voltage threshold while the low-side FET turns on. 00 = 400mV (default) 01 = 500mV 10 = 600mV 11 = 800mV

Table 8. Control0 Register 0x39H (Cont.)

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[4:3]</td><td>DCALERT# Threshold in Battery Only Low Power Mode</td><td>Bits[4:3] only configures the battery discharging current DCALERT# threshold in battery only Low Power mode indicated by Information1 register 0x3A Bit[15].
<table>
<tr><th>Bits[4:3]</th><th>R_{s2} = 10mΩ (A)</th><th>R_{s2} = 20mΩ (A)</th><th>R_{s2} = 5mΩ (A)</th></tr>
<tr><td>00</td><td>12 (Default)</td><td>6</td><td>24</td></tr>
<tr><td>01</td><td>10</td><td>5</td><td>20</td></tr>
<tr><td>10</td><td>8</td><td>4</td><td>16</td></tr>
<tr><td>11</td><td>6</td><td>3</td><td>12</td></tr>
</table></td></tr>
<tr><td>[2]</td><td>Input Voltage Regulation Loop</td><td>Bit[2] disables or enables the input voltage regulation loop.
0 = Enable the input voltage regulation loop (default)
1 = Disable the input voltage regulation loop</td></tr>
<tr><td>[1]</td><td>Force Buck Mode</td><td>Bit[1] disables or enables Force Buck mode. If the Force Buck mode bit is enabled, the Buck-Boost window narrows.
0 = Disable Force Buck mode (default)
1 = Enable Force Buck mode</td></tr>
</table>

Table 9. Control1 Register 0x3CH

Bit	Bit Name	Description
[15:14]	General Purpose Comparator Assertion Debounce Time	Bits[15:14] configures the general purpose comparator assertion debounce time. 00 = 2µs (default) 01 = 12µs 10 = 2ms 11 = 5s
[13]	Exit Learn Mode Option	Bit[13] provides the option to Exit Learn mode when the battery voltage is lower than the MinSystemVoltage register setting. 0 = Stay in Learn mode even if V_{BAT} < MinSystemVoltage register setting (default) 1 = Exit Learn mode if V_{BAT} < MinSystemVoltage register setting
[12]	Learn Mode	Bit[12] enables or disables Battery Learn mode. 0 = Disable Battery Learn mode (default) 1 = Enable Battery Learn mode To enter Learn mode, the BATGONE pin must be low, that is, the battery must be present.
[11]	Reverse Mode	Bit[11] enables or disables the Reverse Mode. 0 = Disable the Reverse Mode (default) 1 = Enable the Reverse Mode
[10]	Audio Filter	Bit[10] enables or disables the audio filter function. 0 = Disable the audio filter function (default) 1 = Enable the audio filter function
[9:8]	Switching Frequency	Bits[9:8] configures the switching frequency and overrides the switching frequency set by the PROG pin. 00 = Switching frequency set by the PROG pin (default) 01 = 839kHz 10 = 723kHz 11 = 635kHz To keep the switching frequency set by the PROG pin resistor, leave Bits[9:8] as it is or write code 00, which sets the same frequency as the PROG pin resistor does.
[7]	Not Used	Not used
[6]	Turbo	Bit[6] enables or disables Turbo mode. When the turbo function is enabled, the BGATE FET turns on in Turbo mode. See Table 22 for the BGATE ON/OFF truth table. This bit is only applicable to NVDC applications having a BFET. 0 = Enable Turbo mode (default) 1 = Disable Turbo mode

Table 9. Control1 Register 0x3CH (Cont.)

Bit	Bit Name	Description
[5]	AMON/BMON Function	Bit[5] enables or disables the current monitor function AMON and BMON. 0 = Enable AMON/BMON (default) 1 = Disable AMON/BMON Bit[5] is only valid in Battery Only mode. When the adapter is present, AMON/BMON is automatically enabled and Bit[5] becomes invalid.
[4]	AMON or BMON	Bit[4] selects AMON or BMON as the AMON/BMON pin output. 0 = AMON (default) 1 = BMON
[3]	Not Used	Not Used
[2]	VSYS	Bit[2] enables or disables the buck-boost charger switching VSYS output. When disabled, the RRB96838 stops switching and forces the BGATE on. 0 = Enables VSYS output (default) 1 = Disables VSYS output
[1:0]	Low_VSYS_ALERT# Reference	Bits[1:0] configures the Low_VSYS_ALERT# assertion threshold. 00 = 6.0V (default) 01 = 6.3V 10 = 6.6V 11 = 6.9V

Table 10. Control2 Register 0x3DH

Bit	Bit Name	Description
[15:14]	Trickle Charging Current	Bits[15:14] configures the charging current in Trickle Charging mode. 00 = 256mA (default) 01 = 128mA 10 = 64mA 11 = 512mA
[13]	Reverse Mode Enable Debounce Time	Control2 Bit[13] and Control 3 Bit[0] configures the REV Mode debounce time from when the RRB96838 receives the REV enable command. **Control2 Bit[13]** / **Control3 Bit[0]** / **REV Start-Up Delay** 0 (default) / 0 (default) / 1.3s 0 / 1 1 / 0 / 150ms 1 / 1 / 7.5ms
[12]	Reserved	Reserved bit, by default it is 0
[11]	Adapter Insertion to Switching Debounce	Bit[11] configures the debounce time from adapter insertion to when ACOK is asserted high. 0 = 1.3s (default) 1 = 150ms After VDD POR, for the first time the adapter is plugged in, the ASGATE turn-on delay is always 150ms, regardless of the Bit[11] setting. This bit sets the ASGATE turn-on delay only after ASGATE turns off at least one time when VDD is above its POR value and the Bit[11] default is 0 for 1.3s.
[10:9]	ALERT# Debounce	Bits[10:9] configures the ALERT# debounce time before its assertion for ACALERT# and DCALERT#. 00: 7µs (default) 01: 100µs 10: 500µs 11: 1ms The Low_VSYS_ALERT# has a fixed 8µs debounce time.

Table 10. Control2 Register 0x3DH (Cont.)

Bit	Bit Name	Description
[8:6]	ALERT# Duration	Bits[8:6] configures the minimum duration of the ALERT# signal when asserted. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 500µs 110 = 100µs 111 = 0s
[5]	ASGATE in REV Mode	Bit[5] turns the ASGATE FET on or off in REV mode. 0 = Turn on ASGATE in REV mode (default) 1 = Turn off ASGATE in REV mode
[4]	CMIN Reference	Bit[4] configures the general purpose comparator reference voltage. 0 = 1.2V (default) 1 = 2V
[3]	General Purpose Comparator	Bit[3] enables or disables the general purpose comparator. 0 = Enable the general purpose comparator (default) 1 = Disable the general purpose comparator
[2]	CMOUT Polarity	Bit[2] configures the general purpose comparator output polarity when asserted. The comparator reference voltage is connected at the inverting input node. 0 = CMOUT is High when CMIN is higher than reference (default) 1 = CMOUT is Low when CMIN is higher than reference
[1]	Not Used	Not Used
[0]	Pass-Through Mode	Bit[0] enables or disables Pass-Through mode. 0 = Disable Pass-Through mode (default) 1 = Enable Pass-Through mode

Table 11. Control3 Register 0x4CH

Bit	Bit Name	Description
[15]	Reread PROG Pin Resistor	Bit[15] specifies whether to reread the PROG pin resistor. 0 = Reread PROG pin resistor 1 = Do not reread PROG pin resistor
[14]	Reload ACLIM When Adapter Is Plugged In	Bit[14] reloads the AdapterCurrentLimit register set by the PROG pin resistor. 0 = Reload the AdapterCurrentLimit register 1 = Do not reload the AdapterCurrentLimit register
[13]	Autonomous Charging Termination Time	Bit[13] configures the autonomous charging termination time. 0 = 20ms 1 = 200ms
[12:11]	Charger Timeout	Bits[12:11] configures the SMBus charger timeout time. This setting is active only when the SMBus Timeout function is enabled (Control0 Bit[7] = 0). 00 = 175s (default) 01 = 87.5s 10 = 43.75s 11 = 5s
[10]	BGATE OFF	Bit[10] configures the BGATE operation between normal and force off. 0 = Normal BGATE operation (default) 1 = Force BGATE off
[9]	Not Used	Not Used
[8]	Exit IDM Timer	Bit[8] configures the Ideal Diode mode exit timer when the battery discharge current is less than 200mA. 0 = 40ms (default) 1 = 80ms

Table 11. Control3 Register 0x4CH (Cont.)

Bit	Bit Name	Description
[7]	Autonomous Charging Mode	Bit[7] enables Autonomous Charging mode. 0 = Enable Autonomous Charging mode 1 = Battery charging current control through SMBus
[6]	AC and CC Feedback Gain	Bit[6] configures AC and CC feedback gain for high current. 0 = x1 (default) 1 = x0.5
[5]	Input Current Limit Loop	Bit[5] disables the input current limit loop. 0 = Enable input current limit loop 1 = Disable input current limit loop
[4]	Input Current Limit Loop when BATGONE = 1	Bit[4] disables the input current limit loop when BATGONE = 1. 0 = Enable ACLIM when BATGONE = 1 1 = Disable ACLIM when BATGONE = 1
[3]	AMON/BMON Direction	Bit[3] configures the AMON/BMON direction. 0 = Adapter current monitor/battery charging current monitor 1 = REV output current monitor/battery discharging current monitor
[2]	Digital Reset	Bit[2] resets all SMBus register values to the POR default value. 0 = Idle 1 = Reset
[1]	Buck-Boost Stretch CCM Period	Buck-boost stretch CCM period (T2 TIME). See Control4 Bit[8] in Table 12. Control3[1] Control4[8] 00 = 2x (default) 01 = 3x 10 = 1x 11 = 0.6x
[0]	REV Start-Up Delay	Refer to the Control2 Bit[13] description in Table 10.

Table 12. Control4 Register 0x4EH

Bit	Bit Name	Description
[15:14]	Dither Enable	Bits[15:14] enables the switching frequency dithering function. 00 = Disable dither (default) 01 = Dither 100 - 102% 10 = Dither 100 - 104% 11 = Dither 100 - 106%
[13]	ADP Side Discharge	Bit[13] enables or disables the ADP side discharge function. Typical 15mA. 0 = Disable ADP side discharge function (default) 1 = Enable ADP discharge function
[12]	VSYS Sink	Bit[12] enables or turns on the discharge FET to pull down the VSYS. 0 = Disable, 10mA sink turned off (default) 1 = Enable, 10mA sink turned on
[11]	BGATE Tri-state	Bit[11] enables or disables the BGATE tri-state function. 0 = Disable BGATE tri-state (default) 1 = Enable BGATE tri-state
[10]	Not Used	Not used
[9]	T2DCM	Buck-Boost T2 time in DCM (T2DCM), reduces input ripple 0 = Reduced T2 time (increases switching frequency in DCM) (default) 1 = Normal T2 time
[8]	Buck-Boost Stretch CCM Period	Buck-Boost stretch CCM period (T2 TIME). See Control3 Bit[1] in Table 11. Control3[1] Control4[8] 00 = 2x (default) 01 = 3x 10 = 1x 11 = 0.6x

Table 12. Control4 Register 0x4EH (Cont.)

Bit	Bit Name	Description
[7]	REVCURRENT ALERT#	Bit[7] enables or disables trigger ALERT# with REVCURRENT. 0 = Disable trigger ALERT# with REVCURRENT 1 = Enable trigger ALERT# with REVCURRENT
[6]	BATGONE ALERT#	Bit[6] enables or disables trigger ALERT# with BATGONE. 0 = Disable trigger ALERT# with BATGONE 1 = Enable trigger ALERT# with BATGONE
[5]	ACOK ALERT#	Bit[5] enables or disables trigger ALERT# with ACOK. 0 = Disable trigger ALERT# with ACOK 1 = Enable trigger ALERT# with ACOK
[4]	Comparator ALERT#	Bit[4] enables or disables trigger ALERT# with General Purpose Comparator rising. 0 = Disable trigger ALERT# with General Purpose Comparator rising 1 = Enable trigger ALERT# with General Purpose Comparator rising
[3:2]	ACOK falling or BATGONE Rising Debounce	Bits[3:2] configures the debounce time from ACOK falling or BATGONE rising to ALERT# trip. 00 = 2µs 01 = 25µs 10 = 125µs 11 = 250µs
[1]	ALERT# Clear	Bit[1] clears ALERT#. 0 = Idle 1 = Clear ALERT#
[0]	ALERT# Latch	Bit[0] manually resets ALERT#. 0 = ALERT# signal auto-clear 1 = Hold ALERT# low when tripped

Table 13. Control6 Register 0x37H

Bit	Bit Name	Description
[15:8]	Not Used	Not used
[7]	Turn off BGATE at VSYSOV	Bit[7] turns off BGATE during VSYSOV 0 = No action 1 = Turn off BGATE
[6]	Charge Current and Maximum System Voltage Slew Rate (1 LSB/clk)[1]	Bit[6] enables the charger current and maximum system voltage slew rate control. 0 = Disable the charger current and maximum system voltage slew rate control (default) 1 = Enable the charger current and maximum system voltage slew rate control
[5]	REV Undervoltage and Overvoltage	Bit[5] disables REV undervoltage and overvoltage protection 0 = Enable REV undervoltage and overvoltage protection 1 = Disable REV undervoltage and overvoltage protection
[4]	CMOUT Latch Data/Clear	When CMOUT Latch is enabled with Ctrl6[3] = 0, the CMOUT Latch data can be read from Bit[4], and can be cleared to the current CMOUT data value by writing Bit[4] = 1. Read: CMOUT Latched Data Value Write 1 to clear CMOUT data to the current value.
[3]	CMOUT Latch	Bit[3] enables the CMOUT latch function. This bit also applies to REVPG. 1 = Disable the CMOUT latch function 0 = Enable the CMOUNT latch function (default)
[2:0]	VSYS Undervoltage Threshold[2]	Bits[2:0] set VSYS undervoltage threshold. 000 = Disable 001 = 3.0V 010 = 3.9V 011 = 4.8V (default) 100 = 5.7V 101 = 6.6V 110 = 7.5V 111 = 8.4V

1. Typical values of 1LSB/clk slew rate: 8mV/µs for system voltage, and 4mA/µs for charging current with 10mΩ sense resistor, and 12mV/µs for REV voltage.
2. When inserting the battery for the first time, VSYS UV by default is 000 = Disabled. When inserting the adapter, VSYS UV threshold by default is 011 = 4.8V.

6.9 REV Voltage Register

The REV Voltage register contains SMBus readable and writable REV mode output regulation voltage references. The default is 5.004V. This register accepts any voltage command, but only the valid register bits are written to the register and the maximum value is clamped at 27.456V.

Table 14. REV Voltage Register 0x49H

Bit	Description
[2:0]	Not Used
[3]	0 = Add 0mV of REV voltage 1 = Add 12mV of REV voltage
[4]	0 = Add 0mV of REV voltage 1 = Add 24mV of REV voltage
[5]	0 = Add 0mV of REV voltage 1 = Add 48mV of REV voltage
[6]	0 = Add 0mV of REV voltage 1 = Add 96mV of REV voltage
[7]	0 = Add 0mV of REV voltage 1 = Add 192mV of REV voltage
[8]	0 = Add 0mV of REV voltage 1 = Add 384mV of REV voltage
[9]	0 = Add 0mV of REV voltage 1 = Add 768mV of REV voltage
[10]	0 = Add 0mV of REV voltage 1 = Add 1536mV of REV voltage
[11]	0 = Add 0mV of REV voltage 1 = Add 3072mV of REV voltage
[12]	0 = Add 0mV of REV voltage 1 = Add 6144mV of REV voltage
[13]	0 = Add 0mV of REV voltage 1 = Add 12288mV of REV voltage
[14]	0 = Add 0mV of REV voltage 1 = Add 24576mV of REV voltage
[15]	Not used
Maximum[1]	27456mV

1. Renesas recommends a maximum operating voltage of 20V in Reverse Mode.

6.10 REV Current Register

The REV Current register contains SMBus readable and writable REV current limits. The default is 512mA. This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 4096mA for R_{s1} = 20mΩ.

Table 15. REV Current 0x4AH

Bit	Description
[4:0]	Not used
[5]	0 = Add 0mA of REV current 1 = Add 32mA of REV current
[6]	0 = Add 0mA of REV current 1 = Add 64mA of REV current
[7]	0 = Add 0mV of REV current 1 = Add 128mA of REV current
[8]	0 = Add 0mV of REV current 1 = Add 256mA of REV current
[9]	0 = Add 0mV of REV current 1 = Add 512mA of REV current
[10]	0 = Add 0mV of REV current 1 = Add 1024mA of REV current
[11]	0 = Add 0mV of REV current 1 = Add 2048mA of REV current
[12]	0 = Add 0mV of REV current 1 = Add 4096mA of REV current
[15:13]	Not used
Maximum	4096mA

6.11 Input Voltage Register

The Input Voltage register contains SMBus readable and writable input voltage limits. The default is 4.096V. This register accepts any voltage command, but only the valid register bits are written to the register and the maximum value is clamped at 18.432V.

Table 16. Input Voltage Register 0x4BH

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mV of input voltage 1 = Add 341.3mV of input voltage
[9]	0 = Add 0mA of input voltage 1 = Add 682.6mV of input voltage
[10]	0 = Add 0mV of input voltage 1 = Add 1365.3mV of input voltage
[11]	0 = Add 0mV of input voltage 1 = Add 2730.6mV of input voltage
[12]	0 = Add 0mV of input voltage 1 = Add 5461.3mV of input voltage
[13]	0 = Add 0mV of input voltage 1 = Add 10922.6mV of input voltage
[15:14]	Not used
Maximum	18432mV

6.12 Information Register

The Information register contains SMBus readable information about manufacturing and Operating modes. Table 17, Table 18, and Table 19 identify the bit locations of the information available.

Table 17. Information1 Register 0x3AH

Bit	Description
[3:0]	Not used
[4]	Bit[4] indicates whether the Trickle Charging mode is active. 0 = Trickle Charging mode is not active 1 = Trickle Charging mode is active
[9:5]	Not used
[10]	Bit[10] indicates whether the Low_VSYS_ALERT# is tripped. 0 = Low_VSYS ALERT# is not tripped 1 = Low_VSYS ALERT# is tripped
[11]	Bit[11] indicates whether DCALERT# is tripped. 0 = DCALERT# is not tripped 1 = DCALERT# is tripped
[12]	Bit[12] indicates whether ACALERT#/REVCURRENTALERT# is tripped. 0 = ACALERT#/REVCURRENTALERT# is not tripped 1 = ACALERT#/REVCURRENTALERT# is tripped
[14:13]	Bits[14:13] indicates the active control loop. 00 = MaxSystemVoltage control loop is active 01 = Charging current loop is active 10 = Adapter current limit loop is active 11 = Input voltage loop is active
[15]	Bit[15] indicates whether the internal reference circuit is active. Bit[15] = 0 indicates that the RRB96838 is in Low Power mode. 0 = Reference is not active 1 = Reference is active

Table 18. Information2 Register 0x4DH

Bit	Description
[4:0]	Program Resister read out Battery cell number Switching frequency Adapter current limit
[7:5]	Bits[7:5] indicates the RRB96838 operation mode. 001 = Boost Mode 010 = Buck Mode 011 = Buck-Boost Mode 101 = REV Boost Mode 110 = REV Buck Mode 111 = REV Buck-Boost Mode

Table 18. Information2 Register 0x4DH (Cont.)

Bit	Description
[11:8]	Bits[11:8] indicates the RRB96838 state machine status. 0000 = OFF 0001 = BATTERY 0010 = ADAPTER 0011 = ACOK 0100 = VSYS 0101 = CHARGE 0110 = ENREV 0111 = REV 1000 = ENLDO5 1001 = Not Applicable 1010 = TRIM/ENCHREF 1011 = ACHRG 1100 = CAL 1101 = AGON/AGONTG 1110 = WAIT
[12]	Bit[12] indicates the BATGONE pin status. 0 = Battery is present 1 = No battery
[13]	Bit[13] indicates the general purpose comparator output after debounce time. 0 = Comparator output is low 1 = Comparator output is high
[14]	Bit[14] indicates the ACOK pin status. 0 = No adapter 1 = Adapter is present
[15]	Not used

Table 19. Information3 Register 0x90H

Bit	Description
[15:2]	Not used
[1]	Pass-Through mode 0 = Inactive 1 = Active
[0]	Not used

7. Modulator Information

7.1 RRB96838 Buck-Boost Charger Modes of Operation

The RRB96838 buck-boost charger drives an external N-channel MOSFET bridge made of two transistor pairs as shown in Figure 32. The first pair, Q1 and Q2, is a buck arrangement with the transistor center tap connected to an inductor “input” as is the case with a buck converter. The second transistor pair, Q3 and Q4, is a boost arrangement with the transistor center tap connected to the same “output” of the inductor as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the battery and also boosting from a voltage input lower than the battery.

The CSIP pin is the output sensing point in REV mode.

Table 20. Operation Mode

Mode	Q1	Q2	Q3	Q4
Buck	Control FET	Sync. FET	OFF	ON
Boost	ON	OFF	Control FET	Sync. FET
Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
REV Buck	ON	OFF	Sync. FET	Control FET
REV Boost	Sync. FET	Control FET	OFF	ON
REV Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET
Pass-Through	ON	OFF	OFF	ON

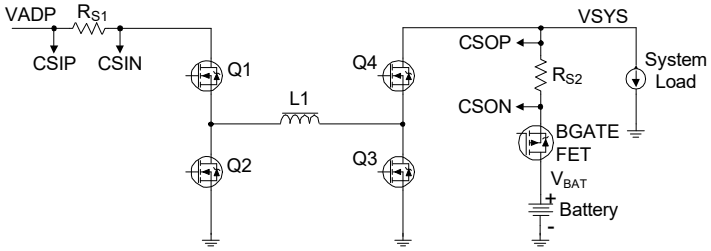


Figure 32. Buck-Boost Charger Topology

The RRB96838 optimizes the Operation mode transition algorithm by comparing the input and output voltage ratio and the load condition. When the adapter voltage V_{ADP} is rising and is higher than 94% of the system bus voltage VSYS, the RRB96838 transitions from Boost mode to Buck-Boost mode. If V_{ADP} is higher than 112% of VSYS, the RRB96838 forcedly transitions from Buck-Boost mode to Buck mode at any circumstance. At heavier loads, the mode transition point changes accordingly to accommodate the duty cycle change because of the power loss on the charger circuit.

When the adapter voltage V_{ADP} is falling and is lower than 106% the system bus voltage VSYS, the RRB96838 transitions from Buck mode to Buck-Boost mode. If V_{ADP} is lower than 92% of VSYS, the RRB96838 transitions from Buck-Boost mode to Boost mode.

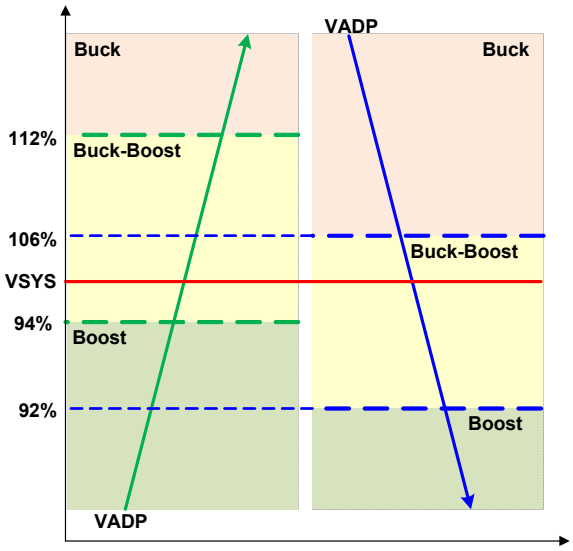


Figure 33. Operation Mode

After programming Force Buck Mode, the RRB96838 operates in Buck mode instead of Buck-Boost mode when VADP is 480mV higher than VSYS. Force Buck mode has a 240mV hysteresis window, so the RRB96838 operates in Buck-Boost mode when VADP is lower than VSYS + 240mV.

7.2 Reverse Mode

When the Reverse Mode is enabled with the SMBus command or REVEN pin, and if the battery voltage VBAT is higher than 5.2V, the RRB96838 operates in REV mode and Control2 Bit[5] controls ASGATE. BATGONE must be low to enable REV mode.

When the REV Mode is enabled with the SMBus command or REVEN pin and if the battery voltage VBAT is higher than 5.2V, the RRB96838 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode.

When the RRB96838 receives the command to enable the Reverse Mode, it starts switching after the debounce time set by Control2 register Bit[13] and Control3 register Bit[0]. When the REV output voltage reaches to the REV output voltage set by register 0x49 Bits[14:3], REV power-good REVPG asserts to High. Control2 register Bit[5] can also be used to turn the ASGATE FET off to cut off the REV output.

Before REV mode starts switching, the CSIP pin voltage must drop below the REV output overvoltage protection threshold (REV Voltage DAC(0x49H) + 1.2V) first.

The default REV output voltage is 5.004V, which can be configured using the REV Voltage register 0x49H.

The default REV output current is limited at 512mA through R_{s1}. The REV Current register 0x4AH can adjust the REV output current limit.

The RRB96838 includes the REV output undervoltage and overvoltage protection functions. The UVP threshold is REV output voltage -1.2V and the OVP threshold is REV output voltage +1.2V.

When UV is detected, the RRB96838 de-asserts REVPG. After 32ms, it stops switching and turns off ASGATE. It resumes switching after the 1.3s or 150ms debounce time set by Control2 register Bit[13].

When OV is detected, the RRB96838 stops switching and de-asserts REVPG. It resumes switching after 100µs when the REV voltage drops below the REV OV threshold.

Because the GPCOMP and REVEN share the same pin, there is some logic to control entry to the Reverse mode.

- If GPCOMP is enabled (Control2[3] = 0), REV is enabled by the Reverse Mode register bit (Control1[11]). The REVEN pin becomes the don't care condition.
- If GPCOMP is disabled (Control2[3] = 1), REV mode is activated by enabling the REV Mode register bit (Control1[11] = 1) and setting REVEN (pin 26) high.

The function must be set up and armed. Figure 34 shows the logical function.

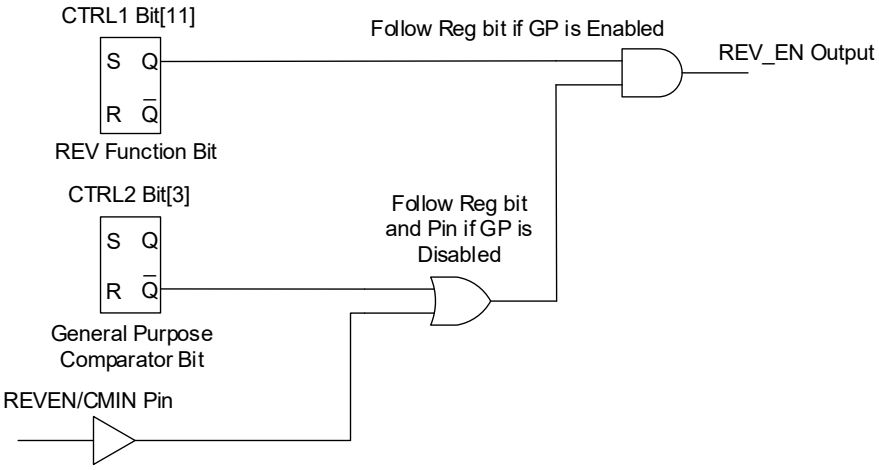


Figure 34. Simplified Control Logic for Reverse Mode

Table 21 shows the control logic for Reverse Mode.

Table 21. Control Logic Truth Table for Reverse Mode

Inputs			Outputs
External Pin REVEN/CMIN	**CTRL2 Bit[3] GP Comparator**	**CTRL1 Bit[11] Reverse Mode**	**Logic Control Signal**
	1 - Disable 0 - Enable	**1 -Enable 0 - Disable**	**REV Mode (REV_EN)**
0	1	0	0
0	1	1	0
1	1	0	0
1	1	1	1
x	0	0	0
x	0	1	1

7.2.1 Pass-Through Mode

Enable Pass-Through mode with Control2 register Bit[0]. When the Pass-Through mode control bit is enabled, the output voltage internal reference ramps to the input voltage and the switcher continues switching until the output voltage is within ±150mV of the input (adapter) voltage. When the regulating voltage is within the 300mV window to the input voltage, the latch is set to stop switching. Q1 and Q4 are always on while Q2 and Q3 are always off. The RRB96838 enters Pass-Through mode and all protections are still valid. The following methods can be used to exit Pass-Through mode.

- Unprogram Control2 register Bit[0]. The output voltage reference ramps to the DAC and switching resumes
- Enable adapter OV triggers
- Ideal DE mode is enabled or the battery discharge current is higher than 300mA

Before entering Pass-Through mode, Renesas recommends doing the following:

1. Ensure CV mode operation
2. Enable slew rate Control6 Bit[6] = 1
3. Change Vsysmax DAC to the value as close to VADP as possible.

When Q1 and Q4 are latching on to enter Pass-Through mode, the current limit loop turns on for more than 1ms.

7.3 Modulator Control Loops

Figure 35 shows the modulator's four main control loops. Each loop has a DAC register to provide settings as required for each system.

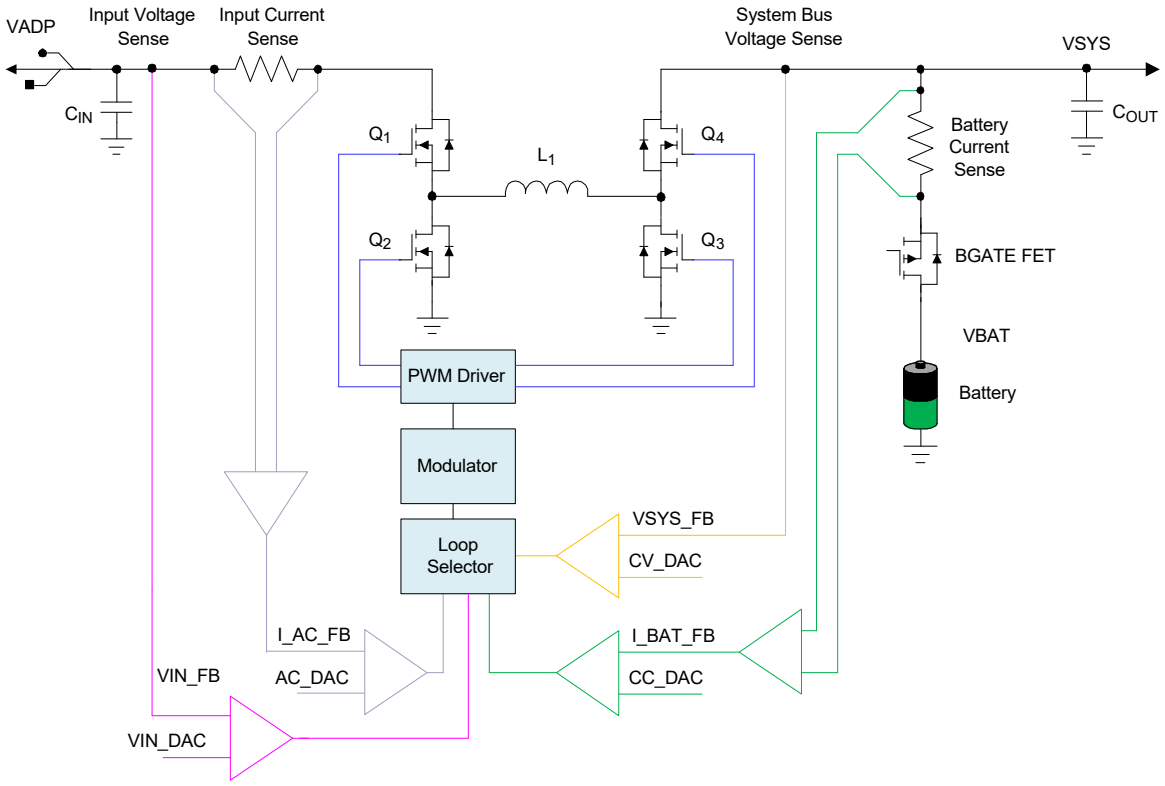


Figure 35. Charger Control Loops

7.3.1 Adapter Current Loop

To set the adapter current limit, write a 16-bit AdapterCurrentLimit command to register address 0x3FH using the Write-word protocol for a 20mΩ R_{s1}. See Table 1 for the DAC summary of values.

The RRB96838 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended current sense resistor values, the LSB of the register translates to 4mA of adapter current. Any adapter current limit command is accepted; however, only the valid register bits are written to the AdapterCurrentLimit registers and the maximum value is clamped.

After adapter POR, the AdapterCurrentLimit register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit register can be read back to verify the content.

7.3.2 USB-PD Reverse Mode Output Current

The REV output current regulation register DAC (Table 15) contains the SMBus readable and writable current that the current sense loop tries to regulate. This loop reuses the input current sense amplifier. If using the USB-PD Programmable Power Supply, this is the current limit loop. *Note*: Renesas recommends disabling REV undervoltage protection when the REV current limiting mode is anticipated as part of normal operation. This register accepts any current command, but only the valid register bits are written to the register. The maximum value is clamped.

7.3.3 Input Voltage Regulation Loop

7.3.3.1 Adapter Support Voltage

The input voltage regulation register DAC (Table 16) contains the SMBus readable and writable input voltage limit at which the input voltage loop tries to regulate when the input voltage is dropping. When the ADP is browning out or weak, the input voltage can droop and the input voltage loop tries to regulate to this setting by reducing battery charging current and then system power to try to hold up the input voltage. The system voltage might start to drop if the input power is not high enough to support the system.

This register accepts any current command but only the valid register bits are written to the register. The maximum value is clamped.

7.3.3.2 USB-PD Reverse Mode Output Voltage

The REV output voltage regulation register DAC (Table 14) contains the SMBus readable and writable voltage that the voltage loop tries to regulate. This loop reuses the input voltage sense amp.

This register accepts any voltage command, but only the valid register bits are written to the register. The maximum value is clamped.

7.3.4 System Voltage Regulation and Trickle Charging

This loop works for two different voltage settings, MaxSystemVoltage and MinSystemVoltage.

If the battery is absent, or present but BGATE is turned off or not charging, the system voltage is regulated to the same setting as the DAC. To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 31 and the data format shown in Table 4.

The RRB96838 supports trickle charging to an overly discharged battery. It can activate the trickle charging function when the battery voltage is lower than MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode.

To enable Trickle Charging, set the ChargeCurrent register to a non-zero value. To disable trickle charging, set the ChargeCurrent register to 0. See Table 22 for trickle charging control logic.

The trickle charging current can be programmed to be 512mA, 256mA, 128mA, or 64mA through SMBus Control2 register Bits[15:14] as shown in Table 10.

In Trickle Charging mode, the RRB96838 regulates the trickle charging current through the buck-boost switcher. For an NVDC application that includes a BFET, independent control loop controls the BGATE so that the system voltage is maintained at the voltage set in the MinSystemVoltage register. The VSYS pin is the system voltage sensing point in Trickle Charging mode.

When the battery voltage is charged to the MinSystemVoltage register value, the RRB96838 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

7.3.5 Charging Current Loop

This loop uses the charge current DAC (see Table 2) to set the fast charging current limit. To set it, write a 16-bit ChargeCurrentLimit command to register address 0x14H (Table 1).

The RRB96838 limits the charging current by limiting the CSOP - CSON voltage. Therefore, the charge current depends on the R_{s2} resistor value. For example, if the current sense resistor R_{s2} is halved, the regulated charge current doubles. By using the recommended current sense resistor values R_{s1} = 20mΩ and R_{s2} = 10mΩ, the LSB of the register translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

7.3.5.1 Reverse Mode Discharge Current

When the charger is in reverse mode of operation (REV), there is a discharge current limit loop that is set by 2xCharge Current limit register (0x14). This discharge current limit loop is in addition to the voltage regulation loop

set by the REV Voltage register and the current limit loop set by the REV Current register. The discharge current limit loop is disabled when charge current (0x14) is zero. When the charge current is a non-zero value, the charger limits the battery discharge current to be less than the Discharge current, which is set by 2xCharge current limit register setting. This function can limit inrush current from the battery when the REV Voltage ramps up or down (in addition to the slew rate function).

7.3.6 Turbo Mode Support

Turbo Mode only applies to NVDC applications having BFET connected. Turbo mode refers the system drawing more power than the power rating of the adapter.

If the adapter current reaches the AdapterCurrentLimit register set value or the adapter input voltage drops to the Input Voltage Regulation Reference enabled by Control0 register 0x39H Bit[2], the RRB96838 limits the input power by regulating the adapter current at the AdapterCurrentLimit register set value, or by regulating the adapter voltage at the Input Voltage Regulation Reference point.

In Turbo mode, the system bus voltage VSYS drops automatically or the charging current drops automatically to limit the adapter input power. If the VSYS pin voltage is 150mV lower than the VBAT pin voltage, the BGATE turns on so that the battery supplies the rest of the power required by the system.

If the RRB96838 detects 150mA charging current or if the battery discharging current is less than 200mA for longer than 40ms or 80ms, it turns off BGATE to exit Turbo mode. The Turbo mode exit timer can be configured through Control3 register 0x4C Bit[8]. See Table 22 for BGATE control logic.

Table 22. BGATE On/Off Truth Table

Turbo (Control Bit)	ChargeCurrent Register	BGATE On/Off	
0 = Enable 1 = Disable	0 = Zero 1 = Nonzero	System Load Not In Turbo Mode Range	System Load in Turbo Mode Range
0	0	OFF	ON
0	1	ON for fast charge; Trickle charge is enabled	ON
1	0	OFF	OFF
1	1	ON for fast charge; Trickle charge is enabled	ON

7.4 R3 Modulator

The RRB96838 uses the patented Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 36 conceptually shows the R3 modulator circuit, and Figure 37 shows the operation principles in steady state.

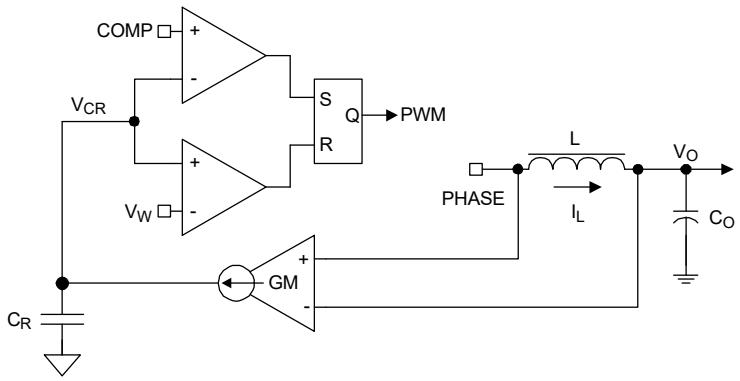


Figure 36. R3 Modulator

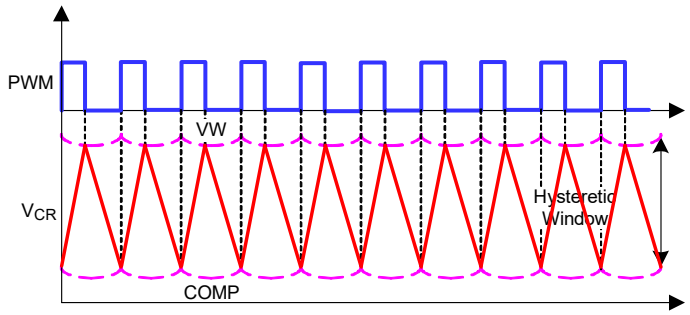


Figure 37. R3 Modulator Operation Principles In Steady State

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor C_R with a current source equal to $g_m(V_{IN}-V_O)$ during PWM on-time and discharges the ripple capacitor C_R with a current source equal to g_mV_O during PWM off-time, where g_m is a gain factor. The C_r voltage V_{CR} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulator.

Figure 38 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

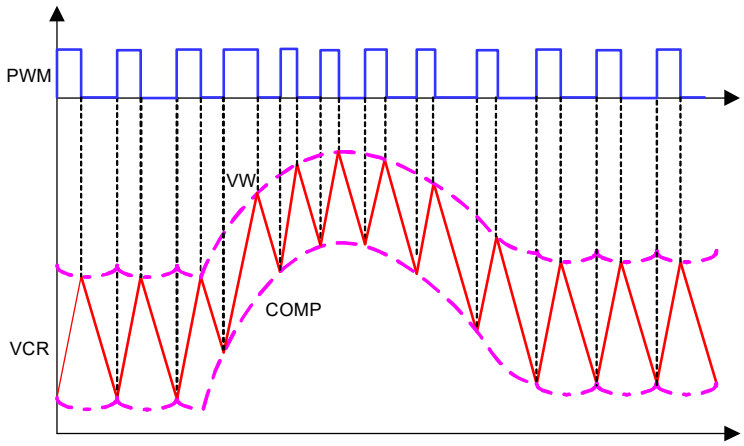


Figure 38. R3 Modulator Operation Principles In Dynamic Response

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, which emulates a diode. As shown in Figure 39, when LGATE is on, the low-side MOSFET carries current and creates negative voltage on the phase node because of the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

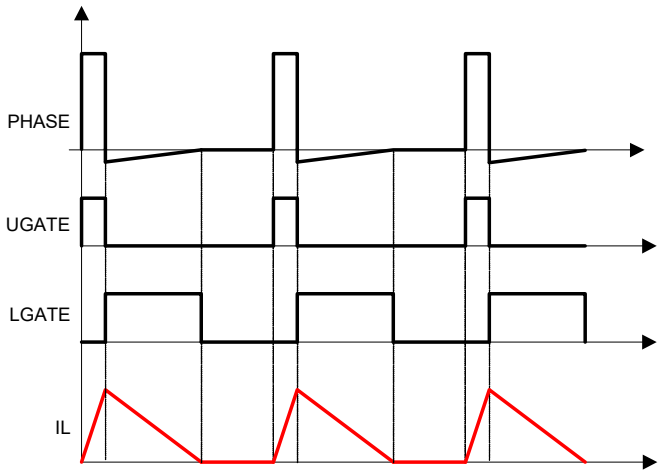


Figure 39. Diode Emulation

If the load current is light enough, as Figure 39 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A, and the regulator is in Continuous Conduction Mode (CCM) although the controller is in DE mode.

Figure 40 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, so the inductor current triangle is the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, which naturally stretches the switching period. The inductor current triangles move farther apart from each other so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

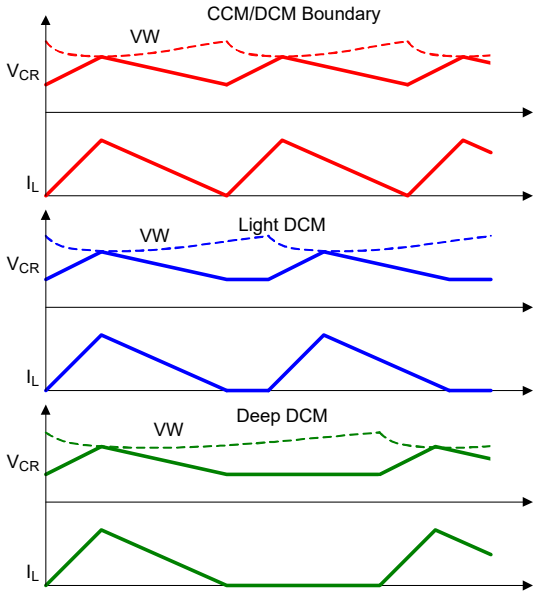


Figure 40. Period Stretching

8. Application Information

8.1 Soft-Start

The RRB96838 includes a low power LDO with nominal 5V output, with an input OR-ed from the VBAT and ADP pins. The RRB96838 also includes a high power LDO with nominal 5V output, with an input from the DCIN pin that connects to both the adapter and the system bus through an external OR-ing diode circuit. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for the RRB96838. The VDDP pin is the RRB96838 gate drive power supply input. Use an R-C filter to generate the VDDP pin voltage from the VDD pin voltage.

When V_{DD} > 2.7V, the RRB96838 digital block is activated and the SMBus register is ready to communicate with the controller.

When VADP > 3.2V, after the 1.3s or 150ms debounce time set by Control2 register Bit[11] (the ASGATE turn on delay is always 150ms the first time the adapter is plugged in after VDD POR), ASGATE starts turning on with 10µA of sink current. During the 1.3s or 150ms debounce time, the RRB96838 uses a patented Renesas technique to check whether the input bus is shorted; if CSIP <2V or ACIN <0.8V, ASGATE does not turn on. The soft-start scheme carefully biases up the input capacitors and protects the back-to-back ASGATE FETs against potential damage caused by the inrush current.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The RRB96838 monitors the ACIN pin voltage to determine the presence of the adapter. When V_{DD} > 3.8V, the ACIN pin voltage exceeds 0.8V, and ASGATE is fully turned on, the RRB96838 allows the external circuit to pull up the ACOK pin. When ACOK is asserted, the RRB96838 starts switching.

The ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The RRB96838 actively pulls ACOK low in the absence of the adapter.

Before ASGATE turns ON, the RRB96838 sources 10µA of current out of the PROG pin and reads the pin voltage to determine the PROG resistor value. The PROG resistor programs the configurations of the RRB96838.

In Battery Only mode, the RRB96838 enters Low Power mode if only the battery is present. V_{DD} is 5V from the low power LDO to minimize power consumption.

8.2 Programming Charger Option

The resistor from the PROG pin to GND programs the configuration of the RRB96838 for the default number of battery cells in series, the default switching frequency, the default AdapterCurrentLimit register value, and the autonomous charging function. Table 23 shows the programming options.

Table 23. PROG Pin Programming Options

PROG-GND Resistance (kΩ)			Cell Number	Default Switching Frequency (Hz)	Autonomous Charging	Default ACLimit Reg (A)
Min	Typ 1%	Max				
42.7	43.2	43.7	2	733k	Yes	1.5
51.7	52.3	52.9		733k	Yes	0.476
61.2	61.9	62.6		1M	No	0.476
70.6	71.5	72.4		1M	No	1.5
81.5	82.5	83.5		733k	No	1.5
92.0	93.1	94.2		733k	No	0.476

Table 23. PROG Pin Programming Options (Cont.)

PROG-GND Resistance (kΩ)			Cell Number	Default Switching Frequency (Hz)	Autonomous Charging	Default ACLimit Reg (A)
Min	Typ 1%	Max				
104	105	106	3	733kHz	No	0.476
116	118	120		733kHz	No	1.5
131	133	135		1MHz	No	1.5
145	147	149		1MHz	No	0.476
160	162	164		733kHz	Yes	0.476
176	178	180		733kHz	Yes	1.5
194	196	198	4	733kHz	Yes	1.5
212	215	218		733kHz	Yes	0.476
234	237	240		1MHz	No	0.476
258	261	264		1MHz	No	1.5
284	287	290		733kHz	No	1.5
312	316	320		733kHz	No	0.476

The RRB96838 uses the default number of cells in series as Table 23 shows and sets the default MaxSystemVoltage register value and default MinSystemVoltage register value accordingly.

The switching frequency can be changed through SMBus Control1 register Bits[9:8] after POR. See the SMBus Control1 register programming table (Table 9) for a detailed description.

Before ASGATE turns on, the RRB96838 sources 10µA of current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise can pollute the PROG pin voltage and cause incorrect readings. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs so the PROG pin voltage can rise to steady state before the RRB96838 reads it.

When the adapter is plugged in, the RRB96838 resets the AdapterCurrentLimit register to the default by reading the PROG pin resistor if it was not read before, or by loading the previous readings. The PROG resistor is only read after POR because of adapter insertion, and is not read at POR from a battery.

By default, the adapter current sensing resistor R_{s1} is 20mΩ and the battery current sensing resistor R_{s2} is 10mΩ. Using this R_{s1} = 20mΩ and R_{s2} = 10mΩ option results in a 4mA/LSB correlation in the SMBus current commands.

If the R_{s1} and R_{s2} values are different from this R_{s1} = 20mΩ and R_{s2} = 10mΩ option, the SMBus command requires scaling to obtain the correct current. Smaller current sense resistor values reduce power loss while larger current sense resistor values give better accuracy.

The information in this datasheet is based on current sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless specified otherwise.

8.3 Autonomous Charging Mode

Autonomous charging mode is only available in the NVDC charging configuration with BFET. Autonomous Charging mode can be enabled or disabled through the programming charging option resistor or SMBus Control3 register Bit[7]. When Autonomous Charging mode is enabled, this mode can also be disabled by writing to the SMBus ChargeCurrentLimit or MaxSystemVoltage command.

The RRB96838 enters Autonomous Charging mode when the battery voltage is lower than MaxSystemVoltage - 200mV per cell for 1ms of debounce time and the BGATE MOSFET is on.

In Autonomous Charging mode, the RRB96838 starts to charge the battery with 2A (with R_{S2} = 10mΩ), the ALERT# pin (Autonomous Charging mode indication pin) is pulled down to GND, and the 175s charging timeout timer is disabled. The RRB96838 exits from Autonomous Charging mode when the battery charging current is

less than 200mA (with R_{S2} = 10mΩ) for 20ms or 200ms in CV loop. This autonomous charging termination time can be set by Control3 register Bit[13]. The RRB96838 re-enters Autonomous Charging mode when the battery voltage is discharged below MaxSystemVoltage - 200mV per cell. When the RRB96838 stays in Autonomous Charging mode for 12hrs, which means the battery charging current is higher than 200mA and the battery cannot be charged to MaxSystemVoltage for 12hrs, the RRB96838 stops charging the battery and exits Autonomous Charging mode.

8.4 Battery Ship Mode

Battery Ship mode sets the lowest power state for the IC. Ship mode can only be entered from Battery Only mode. To achieve the lowest power, several analog functions must be disabled. Many are disabled by default and do not require to be written, but all are listed for completeness. However, the power level can be customized for the system.

- Control1 0x3Ch
  - Bit[5] = 1: Disable IMON
- Control2 0x3Dh
  - Bit[3] = 1: Disable GP Comparator
- Control3 0x4Ch
  - Bit[10] = 1: Force BGATE Off

To exit Battery Ship mode, use the SMBus to change the control bits.

8.5 Diode Emulation Operation

In Diode Emulation (DE) mode, the RRB96838 uses a phase comparator to monitor the PHASE node voltage during the low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator requires a minimum on-time of the low-side switching FET to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the RRB96838 can lose DE ability. To prevent this, the RRB96838 uses a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the RRB96838 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

8.6 Battery Learn Mode

Use Battery Learn mode to supply the system power from the battery even when the adapter is plugged in, such as calibration of the battery fuel gauge.

The RRB96838 enters Battery Learn mode when it receives the SMBus Control command. When entering Battery Learn mode, the RRB96838 turns on the BGATE FET.

In Battery Learn mode, the RRB96838 turns on BGATE and keeps ASGATE on but turns off the buck-boost switcher regardless of whether the adapter is present.

The three ways of exiting Battery Learn mode are:

- Receive the Battery Learn mode exit command through SMBus
- The battery voltage is less than MinSystemVoltage register setting (provided that Control1 register Bit[13] is set)
- The BATGONE pin voltage goes from logic LOW to HIGH

In all these cases, the RRB96838 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

8.7 Charger Timeout

The RRB96838 includes a timer to ensure the SMBus controller is active and to prevent overcharging the battery. The RRB96838 terminates charging by turning off the BGATE FET if the charger has not received a write command to the MaxSystemVoltage or ChargeCurrent register within 175s (SMBus Control3 register

Bits[12:11] = 00). Charger timeout time can be configured through SMBus Control3 register Bits[12:11]. When charging is terminated by the timeout, the ChargeCurrent register retains its value instead of resetting to zero. If a timeout occurs, the MaxSystemVoltage or ChargeCurrent register must be written to re-enable charging.

The RRB96838 allows disabling the charger timeout function through SMBus Control0 register Bit[7] as Table 8 shows. The charger timeout functionality must be disabled for Battery Charging Only configuration without BFET.

8.8 Monitoring

8.8.1 Current Monitor

The RRB96838 provides an adapter current monitor/REV current monitor or a battery charging current monitor/battery discharging current monitor through the AMON/BMON pin. The AMON output voltage is 18x (CSIP - CSIN) and 18x (CSIN - CSIP) voltage. The BMON output voltage is 18x (CSON - CSOP) and 36x (CSOP - CSON) voltage.

The AMON and BMON functions can be enabled or disabled through SMBus Control1 register Bit[5]. AMON or BMON can be selected through SMBus Control1 register Bit[4] and the AMON/BMON direction can be configured through SMBus Control3 register Bit[3] as Table 9 shows.

8.9 Stand-Alone Comparator

The RRB96838 includes a general purpose stand-alone comparator. The REVEN/CMIN pin is the comparator input. The internal comparator reference is connected to the inverting input of the comparator and can be configured as 1.2V or 2V through SMBus Control2 register Bit[4]. The comparator output is the REVPG/CMOUT pin. The output polarity can be configured through the SMBus register bit when the comparator is tripped.

- When Control2 register Bit[2] = 0 for normal comparator output polarity, CMOUT = High if CMIN > Reference; CMOUT = Low if CMIN < Reference.
- When Control2 register Bit[2] = 1 for inversed comparator output polarity, CMOUT = Low if CMIN > Reference; CMOUT = High if CMIN < Reference.

By default in Battery Only mode, the stand-alone comparator is enabled. This comparator can be enabled/disabled in Battery Only mode using Control 2 Bit[3]. In Battery Only mode, the reference is set to 1.2V only.

Table 24 shows the REV mode and the stand-alone comparator truth table.

Table 24. REV and Comparator Truth Table

				Description
Control1 Register 0x3C	Control2 Register 0x3D	PIN-2O	PIN-26	
Bit[11] Reverse Mode Enable/Disable	Bit[3] Comparator Enable/Disable	REVEN/CMIN	REVPG/CMOUT	
0	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	Reverse Mode is disabled. Comparator is enabled.
0	1	X	X	Both the Reverse Mode and comparator are disabled.
1	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	Both the Reverse Mode and comparator are enabled. Reverse Mode is enabled when V_{BAT} > 5.2V and Control1 register Bit[11] = 1 without REV power-good pin indication. The device is in REV mode while Information1 register 0x3A Bits[6:5] = 11.
1	1	REV Enable Input Pin REVEN	REV Power-Good Indication Pin REVPG	Comparator is disabled. Reverse Mode is enabled when V_{BAT} > 5.2V and ENREV pin = High and Control1 register Bit[11] = 1

8.10 Protections

8.10.1 Adapter Overvoltage Protection

If the ADP pin voltage exceeds 23.4V for more than 10µs, an adapter overvoltage condition occurs. The RRB96838 turns off the ASGATE MOSFETs to isolate the adapter from the system, de-asserts the ACOK signal by pulling it low, and stops switching. BGATE turns on for the battery to support the system load. When the ADP voltage drops below 23.04V from more than 100µs, it starts to turn on ASGATE and start switching.

8.10.2 System Overvoltage Protection

The RRB96838 provides system rail overvoltage protection. If the system voltage VSYS is 800mV higher than MaxSystemVoltage register set value, it declares the system overvoltage and stops switching. It resumes switching without the 1.3s or 150ms debounce when VSYS drops 400mV below the system overvoltage threshold.

8.10.3 System Voltage Rail Short Protection

The RRB96838 has a system rail short protection (VSYSOK) to prevent powering on the system rail into a short-circuit before switching starts. When the VSYS voltage is below 0.6V, the RRB96838 sources 10mA current from VDDP to charge VSYS before switching can start.

From VSYSOK (VSYS rail short protection) beginning to switching start in VSYS state, the parts must go through multiple startup and initialization transition states, including turning on A-FET. This initialization transition duration might take longer than VSYS voltage is charged above 0.6V using a 10mA source by the VSYSOK function. If this initialization transition duration is longer than the duration of charging VSYS above 0.6V, the charger must wait until the transition duration is completed before switching starts, and vice versa.

Conversely, the duration of charging VSYS above 0.6V, which depends on the leakage current and capacitance value at VSYS, varies per individual system design. If users would like to estimate the duration in a worst-case scenario, Renesas recommends testing their design to determine the following:

- If the initialization transition duration is longer than the duration of charging VSYS above 0.6V, add a 30% margin (considering ±5% clock tolerance) to estimate the duration.
- If the initialization transition duration is shorter than the duration of charging VSYS above 0.6V, check the tolerance of the VSYS capacitance or leakage current from VSYS downstream circuitry and then add a reasonable margin, such as 40% (considering ±20% cap tolerance), to estimate the duration.

After switching starts, the charger enters the Fault state if VSYS drops below 0.6V again at any time. After entering the Fault state, the charger stops switching and turns off ASGATE, and tries to start again with 1.3s or 150ms debounce time (configured by Control2 Bit[11]).

For RRB96838 startup without a battery pack, Renesas recommends checking total system loading on VSYS, zero load preferred, and ensuring it does not exceed the worst-case value, VSYS loading <19.8µA for VSYS <0.6V.

8.10.4 System Voltage Undervoltage Protection (for Short-Circuit Protection)

The charger has a fixed undervoltage protection on the system side that can be configured using Control6 Bits[2:0].

When inserting the battery for the first time, VSYS UV by default is 000 = Disabled. When inserting the adapter, VSYS UV threshold by default is 011 = 4.8V. When the VSYS voltage falls to the VSYS UV threshold set by Control6 Bit[2:0], there is a 100ms debounce before the charger enters FAULT state. After entering FAULT state, there is no switching and charger tries to start switching again after 1.3s (configurable by Control2 Bit[11]).

8.10.5 Over-Temperature Protection

The RRB96838 stops switching for self protection when the junction temperature exceeds +140°C. When the temperature falls below +120°C and after a 100µs delay, the RRB96838 resumes switching.

8.11 Selecting the Power Source

The RRB96838 automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin, which is optional, drives a P-channel MOSFET gate that connects/disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common source PFETs to connect/disconnect the adapter from the system and the battery. Use of the ASGATE pin is optional.

When the battery voltage V_{BAT} is higher than 2.4V and the adapter voltage V_{ADP} is less than 3.2V, the RRB96838 operates in Battery Only mode. During Battery Only mode, the RRB96838 turns on the BGATE FET to connect the battery to the system. In Battery Only mode, the RRB96838 consumes very low power (less than 20µA). The battery discharging current monitor BMON can be turned on during this mode to monitor the battery discharging current.

In Battery Only mode, the USB Reverse Mode can be enabled when the battery voltage V_{BAT} is higher than 5.2V. See Stand-Alone Comparator for details.

When the adapter voltage V_{ADP} is more than 3.2V, the RRB96838 turns on ASGATE. If VDD is higher than 3.8V, the RRB96838 enters Forward Buck, Forward Boost, or Forward Buck-Boost mode depending upon the adapter and system voltage VSYS duty cycle ratio. The system bus voltage is regulated at the voltage set on the MaxSystemVoltage register. If the charge current register is programmed (non-zero), the RRB96838 charges the battery either in Trickle Charging mode or Fast Charging mode, as long as BATGONE is low.

9. Design Guidelines

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Renesas provides complete reference designs that include schematics, bill of materials, and example board layouts.

9.1 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 1:

(EQ. 1) $$D = \frac{V_{OUT}}{V_{IN}}$$

The output inductor peak-to-peak ripple current is written by Equation 2:

(EQ. 2) $$I_{P\text{-}P} = \frac{V_{OUT} \times (1 - D)}{f_{SW} \times L}$$

A typical step-down DC/DC converter has an $I_{P\text{-}P}$ of 20% to 40% of the maximum DC output load current for a practical design. The value of $I_{P\text{-}P}$ is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 3 where I_{LOAD} is the converter output DC current.

(EQ. 3) $$P_{COPPER} = I_{LOAD}^{2} \times DCR$$

The copper loss can be significant, so select DCR carefully. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written by Equation 4 and Equation 5:

(EQ. 4) $$\Delta V_{ESR} = I_{P-P} \times ESR$$

(EQ. 5) $$\Delta V_C = \frac{I_{P-P}}{8 \times C_O \times f_{SW}}$$

If the output of the converter has to support a load with high pulsating current, several capacitors must be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

9.2 Selecting the Input Capacitor

The important parameters for input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and that are capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 41 is a graph of the input capacitor RMS ripple current that is normalized relative to output load current. The graph is also a function of duty cycle and is adjusted for converter efficiency.

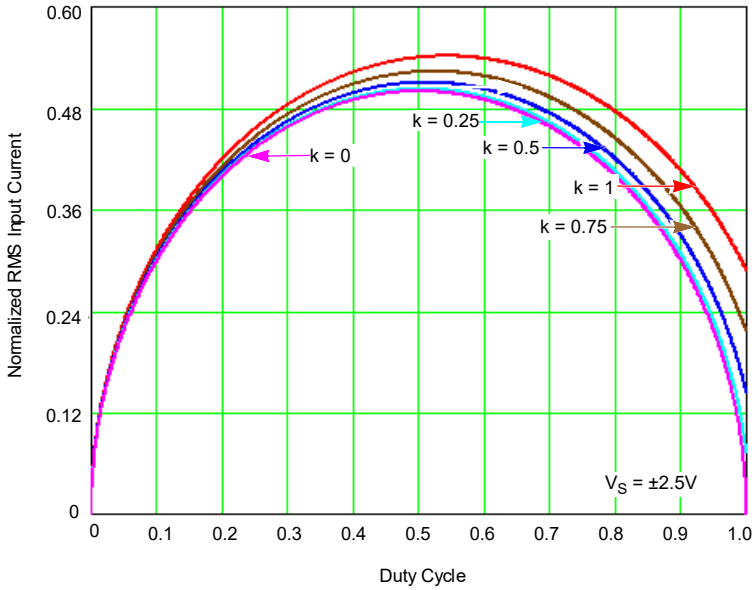


Figure 41. Normalized RMS Input Current at EFF = 1

The normalized RMS ripple current calculation is written by Equation 6:

(EQ. 6) $$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \times \sqrt{D \times (1 - D) + \frac{D \times k^2}{12}}}{I_{MAX}}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written by Equation 7:

(EQ. 7) $$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

9.3 Selecting the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds both the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs that are optimized for DC/DC converter applications are readily available. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately VIN - VOUT, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss.

Note: This is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices might be required.

The power loss of the Low-Side (LS) MOSFET can be assumed to be conductive only and is written by Equation 8:

(EQ. 8) $$P_{CON\_LS} \approx I_{LOAD}^{2} \times r_{DS(ON)\_LS} \times (1 - D)$$

The conduction loss of the High-Side (HS) MOSFET is written by Equation 9:

(EQ. 9) $$P_{CON\_HS} = I_{LOAD}^{2} \times r_{DS(ON)\_HS} \times D$$

The switching loss of the HS MOSFET is written by Equation 10:

(EQ. 10) $$P_{SW\_HS} = \frac{V_{IN} \times I_{VALLEY} \times t_{SWON} \times f_{SW}}{2} + \frac{V_{IN} \times I_{PEAK} \times t_{SWOFF} \times f_{SW}}{2}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{SW(ON)}$ is the time required to drive the device into saturation
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off

9.4 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 11:

(EQ. 11) $$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on.

As an example, suppose the HS MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF is sufficient. Use an X7R or X5R ceramic capacitor. Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high side MOSFET gate capacitance.

9.5 Switching Power MOSFET Gate Capacitance

The RRB96838 includes an internal 5V LDO output at the VDD pin, which can be used to provide the switching MOSFET gate driver power through the VDDP pin with an RC filter. The 5V LDO output overcurrent protection threshold is 100mA nominal. When selecting the switching power MOSFET, consider the MOSFET gate capacitance carefully to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 12:

(EQ. 12) $$I_{driver} = Q_g \times f_{SW}$$

where:

- Q_g is the total gate charge, which can be found in the MOSFET datasheet
- f_{SW} is the switching frequency

Renesas recommends using a 2.2µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

9.6 DCIN Filter

An RC filter is connected at the DCIN pin. Renesas recommends connecting a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7µF DCIN capacitor to GND, which has an effective capacitance higher than 0.4µF at 20V.

9.7 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the RRB96838 pins connecting to the adapter connector node. One low cost solution is to add an R-C snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 42. A practical value of the R-C snubber is 2.2Ω to 2.2µF, while the appropriate values and power rating should be carefully characterized based on the actual design. Renesas does not recommend adding a pure capacitor at the adapter connector node, which can cause an even larger voltage spike because of the adapter cable or the adapter current path parasitic inductance.

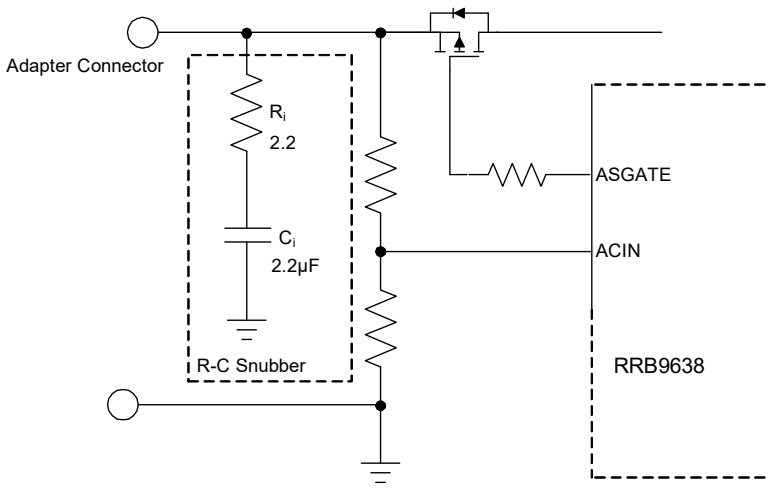
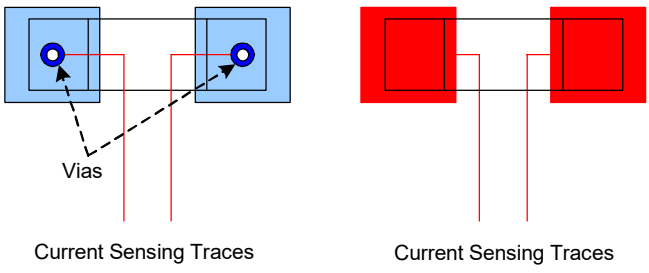
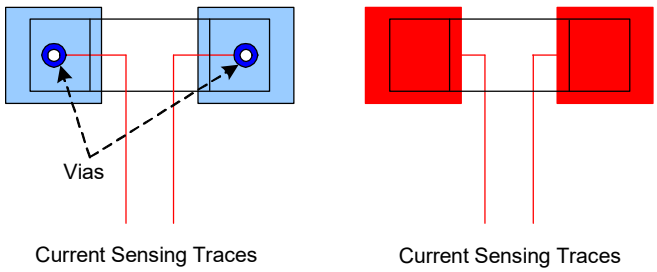


Figure 42. Adapter Input R-C Snubber Circuit

10. Layout

Pin Number	Pin Name	Layout Guidelines
Bottom Pad 33	GND	Connect this ground pad to the ground plane through a low impedance path. Use at least five vias to connect to the PCB ground planes to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current sensing resistor to the IC. Place the differential mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
2	CSOP	
3	VSYS	This signal pin provides feedback for the system bus voltage. Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from the system bus to the pin and do not route near the switching traces. Do not share the same trace with the signal routing to the DCIN pin OR diodes and the CSOP trace.
4	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide traces. Avoid any sensitive analog signal traces from crossing over or getting close.
5	UGATE2	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close. Route the PHASE2 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the gate terminals of the switching MOSFETs and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source, and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET source and low-side MOSFET drain terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
6	PHASE2	

Pin Number	Pin Name	Layout Guidelines
7	LGATE2	Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close.
8	VDDP	Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to the VDD pin with sufficient width.
9	LGATE1	Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close.
10	PHASE1	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close. Route the PHASE1 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the gate terminals of the switching MOSFETs and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source, and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET source and low-side MOSFET drain terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area big enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
11	UGATE1	
12	BOOT1	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficient wide trace. Avoid any sensitive analog signal traces from crossing over or getting close.
13	ASGATE	Run this trace with sufficient width in parallel fashion with the ADP pin trace.
14	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
15	CSIP	
16	ADP	Run this trace with sufficient width in parallel fashion with the ASGATE pin trace.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller. Run the VADP trace and VSYS trace to the OR diodes with sufficient width.
18	VDD	Place the RC filter connecting with the VDDP pin in the general proximity of the controller. Run the trace connecting to the VDDP pin with sufficient width.
19	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
20	REVEN/CMIN	No special consideration.
21	SDA	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
22	SCL	
23	ALERT#	Digital pin, open-drain output. No special consideration.
24	ACOK	
25	BATGONE	Digital pin. Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
26	REVPG/CMOUT	Digital pin, open-drain output. No special consideration.
27	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.

Pin Number	Pin Name	Layout Guidelines
28	COMP	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
29	AMON/BMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
30	RESERVED	Keep floating.
31	VBAT	Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC.
32	BGATE	Use sufficient width trace from the IC to the BGATE MOSFET gate. Place the capacitor from BGATE to ground close to the MOSFET.

11. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

12. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RRB96838-BU7	96838B7	32 Ld 4x4 TQFN	L32.4x4D	Reel, 1k	-10 to +100°C
RRB96838-BT7				Reel, 6k	
RRB96838-BU8	96838B8	32 Ld 4x4 TQFN	L32.4x4D	Reel, 1k	-40 to +100°C
RRB96838-BT8				Reel, 6k	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL), see the RRB96838 product page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 25. Key Differences Between Family of Parts

Part Number	Battery Cell Count	Adapter Voltage Range (V)	Battery Voltage Range (V)
RRB96838	2 to 4	3.9 to 23.4	2.4 to 18.304
RAA489118	2 to 7	3.9 to 30	2.4 to 30.8

13. Revision History

Revision	Date	Description
1.01	Jun 6, 2025	Updated pin descriptions for Pins 13, 23, and 32. Changed BU7/BT7 to RRB96838-BU7/BT7 and BU8/BT8 to RRB96838-BU8/BT8 in sections 3.2 and 3.4. Added Battery Charging Only (No BFET) section in Typical Performance Curves. Updated Tables 8, 10, and 11. Updated pin types for pins 4, 6, 10, and 12 in ECAD section.
1.00	Apr 8, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	POD Number
RRB96838-BU7	32	TQFN	L32.4x4D/QW0032AA
RRB96838-BT7	32	TQFN	L32.4x4D/QW0032AA
RRB96838-BU8	32	TQFN	L32.4x4D/QW0032AA
RRB96838-BT8	32	TQFN	L32.4x4D/QW0032AA

A.2 Symbol Pin Information

A.2.1 32-TQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	CSON	Input	-
2	CSOP	Input	-
3	VSYS	Input	-
4	BOOT2	Power	-
5	UGATE2	Output	-
6	PHASE2	Power	-
7	LGATE2	Output	-
8	VDDP	Power	-
9	LGATE1	Output	-
10	PHASE1	Power	-
11	UGATE1	Output	-
12	BOOT1	Power	-
13	ASGATE	Output	-
14	CSIN	Input	-
15	CSIP	Input	-
16	ADP	Input	-
17	DCIN	Power	-
18	VDD	Power	-
19	ACIN	Input	-
20	REVEN	Input	CMIN
21	SDA	I/O	-
22	SCL	I/O	-
23	ALERT#	Output	-
24	ACOK	Output	-
25	BATGONE	Input	-
26	REVPG	Output	CMOUT
27	PROG	Input	-
28	COMP	Output	-
29	AMON	Output	BMON
30	RESERVED	Passive	-
31	VBAT	Input	-
32	BGATE	Output	-
EPAD33	GND	Power	-

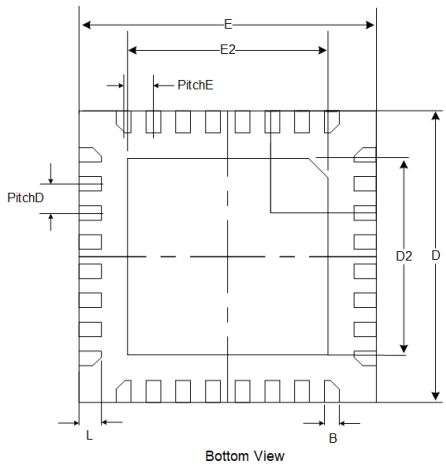
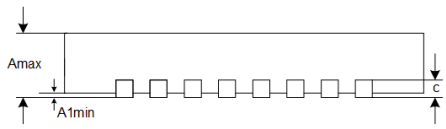
A.3 Symbol Parameters

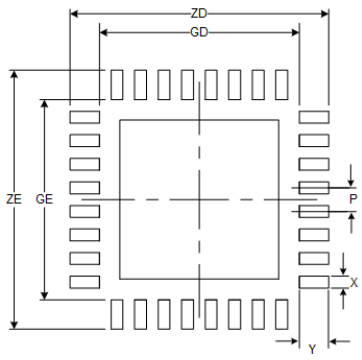
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Min Output Voltage	Max Output Voltage	Typ Switching Frequency	Switcher Configuration
RRB96838-BU7	Consumer	SMD	Compliant	-10 °C	100 °C	3.9 V	23.4 V	2.4 V	18.304 V	733 kHz	Buck, Boost and Buck-Boost
RRB96838-BT7	Consumer	SMD	Compliant	-10 °C	100 °C	3.9 V	23.4 V	2.4 V	18.304 V	733 kHz	Buck, Boost and Buck-Boost
RRB96838-BU8	Industrial	SMD	Compliant	-40 °C	100 °C	3.9 V	23.4 V	2.4 V	18.304 V	733 kHz	Buck, Boost and Buck-Boost
RRB96838-BT8	Industrial	SMD	Compliant	-40 °C	100 °C	3.9 V	23.4 V	2.4 V	18.304 V	733 kHz	Buck, Boost and Buck-Boost

A.4 Footprint Design Information

A.4.1 32-TQFN

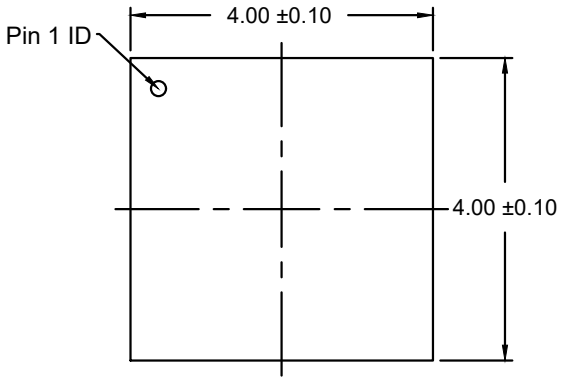
IPC Footprint Type	POD Number	Number of Pins
QFN	L32.4x4D/QW0032AA	32

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	3.90	 Bottom View
Maximum body span (vertical side)	Dmax	4.10	
Minimum body span (horizontal side)	Emin	3.90	
Maximum body span (horizontal side)	Emax	4.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Number of pins (vertical side)	PinCountD	8	
Number of pins (horizontal side)	PinCountE	8	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	2.60	
Maximum thermal pad size (vertical side)	D2max	2.80	
Minimum thermal pad size (horizontal side)	E2min	2.60	
Maximum thermal pad size (horizontal side)	E2max	2.80	
Maximum Height	Amax	0.85	 Side View
Minimum Standoff Height	A1min	0	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

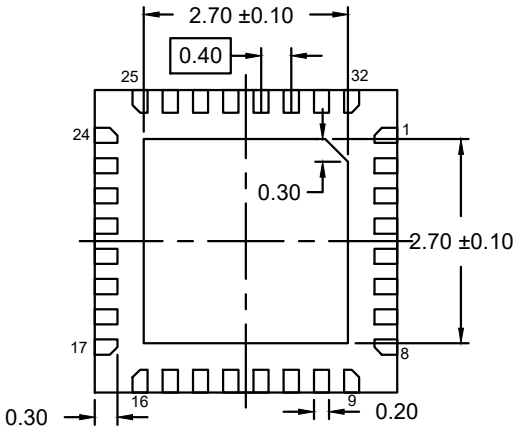
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	4.30	 PCB Top View
Distance between top pad toe to bottom pad toe (vertical side)	ZD	4.30	
Distance between left pad heel to right pad heel (horizontal side)	GE	3.40	
Distance between top pad heel to bottom pad heel (vertical side)	GD	3.40	
Pad Width	X	0.20	
Pad Length	Y	0.45	

Package Outline Drawing

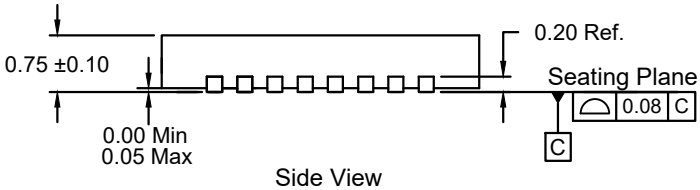
L32.4x4D
QW0032AA
32-QFN 4.0 x 4.0 x 0.75 mm Body, 0.40 mm Pitch
Rev04, Mar 26, 2025



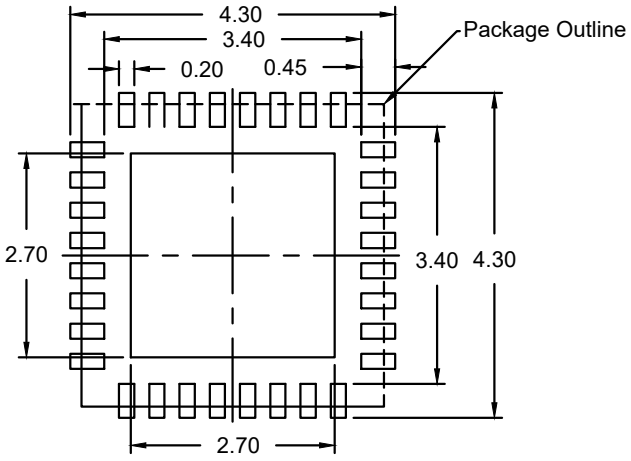
Top View



Bottom View



Side View



Typical Recommended Land Pattern

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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