RRP58000

80V 50mA Low IQ Adjustable Output Voltage Low Dropout Regulator

The RRP58000 is a low-quiescent current, adjustable output voltage low-dropout regulator capable of sourcing up to 50mA to a load. The LDO has a wide input voltage range of up to 80V. The output voltage is adjustable with external feedback resistors anywhere from 1.24V to 15V.

The LDOs feature a ±2.5% output voltage accuracy (over line, load, and temperature), input UVLO with hysteresis, enable control, internal current limit, and over-temperature shutdown protection with hysteresis.

The ground current is typically 5.8µA at no load and drops to 0.2µA when in shutdown, making it great for battery-powered and portable devices.

The device is stable with a minimum 2.2µF ceramic output capacitor and is available in an HMSOP8 package.

Features

- Wide input voltage range: up to 80V
- Adjustable output voltage (1.24V - 15V)
- Typical low-quiescent current: 5.8µA at no load
- Max output current: 50mA
- Excellent line and load regulation over temperature with Output voltage accuracy: ±2.5%
- Typical shutdown current: ≤0.2µA
- Stable with 2.2µF minimum ceramic output capacitor
- Typical dropout voltage: ≤0.8V at 50mA
- Overcurrent and over-temperature protection
- Junction temperature range: -40°C to 125°C

Applications

- Portable and battery-powered equipment
- Notebook computers
- Motor drives

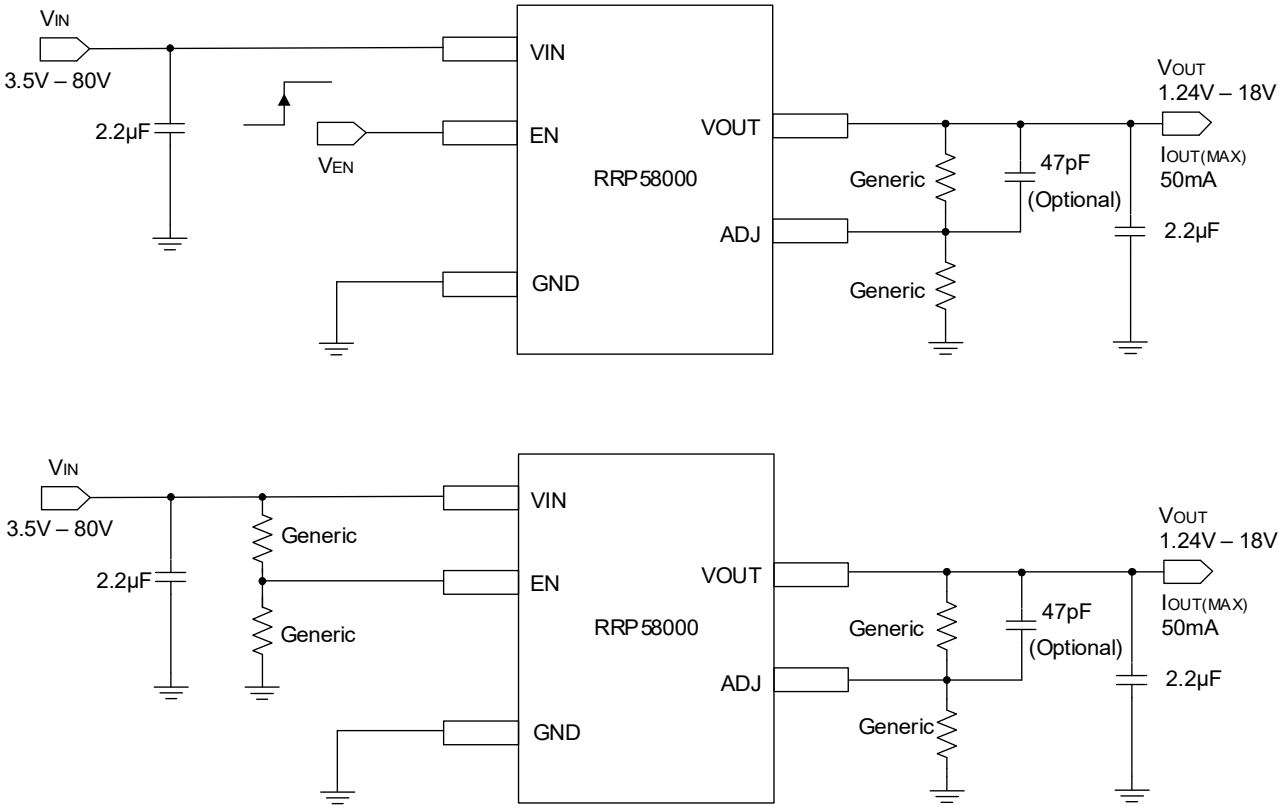


Figure 1. Typical Application Schematics

Contents

1. Overview

1.1 Block Diagram

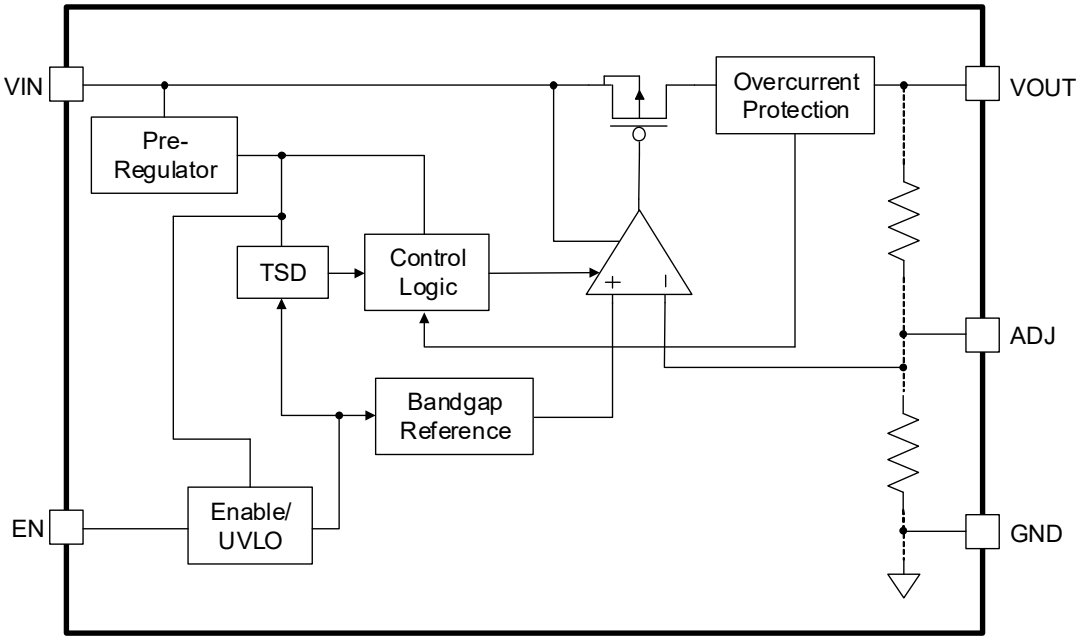


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

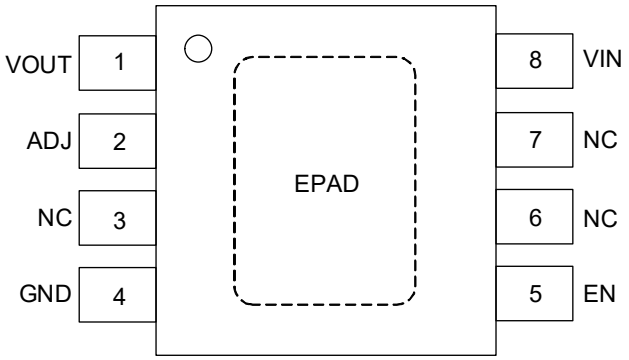


Figure 3. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	VOUT	Regulated output voltage pin. A minimum 2.2µF X5R/X7R output capacitor is required between this pin and GND. Place the capacitor as close to the output of the regulator as possible.
2	ADJ	Adjustable pin regulated at 1.24V (internal band gap voltage). Connected to an external resistor divider between VOUT and GND to set the output voltage. When the pin is shorted to VOUT, the output voltage is set to the minimum 1.23V.
3, 6, 7	NC	Not connected.
4	GND	Ground reference. This pin must be tied to the PCB ground plane.
5	EN	Enable input. Drive EN high to turn on the linear regulator, low to turn it off. This pin can be connected to VIN for automatic turn on.
8	VIN	Analog input supply voltage and positive supply for the linear regulator. Decouple this pin to ground with 0.1µF or larger high frequency ceramic capacitor to GND.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
VIN, VEN	-0.3	+85	V
VOUT	-0.3	+20	V
ADJ	-0.3	+4	V
Maximum Junction Temperature	-	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E)	-	100	mA

1. All voltages referenced to GND unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	3.5	80	V
Enable Voltage, V_{EN}	3.5	80	V
Output Voltage, V_{OUT}	1.24	15	V
Output Current, I_{OUT}	0	50	mA
Output Capacitor, C_{OUT}	2.2	200	µF
Junction Temperature	-40	+125	°C

1. All voltages referenced to GND unless otherwise specified.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance[1]	8-Ld HMSOP	θ_{JA}[2]	Junction to ambient	56	°C/W
		$\theta_{JA(EVB)}$[3]	Junction to EVB	39.6	°C/W
		θ_{JC}[4]	Junction to case	14	°C/W

1. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. See footnote 2 for test conditions to establish junction to ambient thermal resistance.
2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
3. $\theta_{JA(EVB)}$ is measured in free air with the component mounted on a 2-layer PCB (2oz Cu finish all layers) evaluation board.
4. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = 3.5V, V_{OUT} = V_{adj}, I_{OUT} = 1mA, V_{EN} = 5V, C_{OUT} = 2.2µF MLCC. Typical values are at T_A = +25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ.	Max[1]	Unit
Input						
Input Voltage Range V_{IN}	V_{IN}	-	3.5	-	80	V
Input UVLO Rising Threshold	-	VIN Rising	2.09	2.39	2.71	V
Input UVLO Falling Threshold	-	VIN Falling	1.90	2.20	2.50	V
Quiescent Current	I_Q	I_{OUT} = 0mA, V_{OUT} = V_{ADJ}	-	5	10	µA
Ground Current	I_{GND}	I_{OUT} = 10mA, V_{OUT} = V_{ADJ}	-	51	100	µA
		I_{OUT} = 50mA, V_{OUT} = V_{ADJ}	-	131	200	
Shutdown Current	I_{SHDN}	VEN = 0V	-	0.2	1.0	µA
Output						
Output Voltage	V_{OUT}	-	1.24	-	15	V
Adjust Pin Voltage	V_{ADJ}	-	1.21	1.24	1.27	V
Output Current	I_{OUT}	-	0	-	50	mA
Dropout Voltage	V_{DO}	I_{OUT} = 10mA, V_{OUT} = 3.3V	-	0.16	0.40	V
		I_{OUT} = 20mA, V_{OUT} = 3.3V	-	0.31	0.60	
		I_{OUT} = 50mA, V_{OUT} = 3.3V	-	0.77	1.40	
Load Regulation $\Delta V_{OUT}/\Delta I_{OUT}$	-	I_{OUT} = 100µA < I_{OUT} < 50mA	-	0.0001	0.010	%/mA
Line Regulation $\Delta V_{OUT}/\Delta V_{IN}$	-	V_{IN} = 3.5 - 80V	-	0.001	0.050	%/V
Start-Up Time	T_{ST}	Time from V_{IN} = V_{OUT} + 1.7V to 95% of V_{OUT}, I_{OUT} = 0mA	281	655	1206	µs
Power Supply Ripple Rejection Ratio	PSRR	FREQ = 10Hz	-	80	-	dB
		FREQ = 100Hz	-	75	-	dB
		FREQ = 1kHz	-	60	-	dB
Output Voltage Noise	Vn	BW = 100Hz to 100kHz V_{OUT} = V_{ADJ}	-	200	-	µVRMS
EN						
V_{EN} Rising Threshold	-	I_{OUT} = 1mA	1.21	1.47	1.70	V
V_{EN} Falling Threshold	-		1.00	1.27	1.50	V
EN Leakage Current	I_{EN}	V_{IN} = V_{EN} = 80V	-	0.1	0.2	µA
Protection						
Output Current Limit	I_{CL}	-	70	97	150	mA
Thermal Shutdown	T_{OTSD}	Temperature Rising	-	155	-	°C
Thermal Shutdown Hysteresis	$T_{OTSD(HYST)}$	-	-	20	-	°C

1. Compliance to datasheet limits is established by one or more methods: production test, characterization, and/or design.

4. Typical Performance Graphs

Operating conditions unless otherwise noted: V_{EN} = 5V, C_{IN} = 10µF MLCC, C_{OUT} = 2.2µF MLCC.

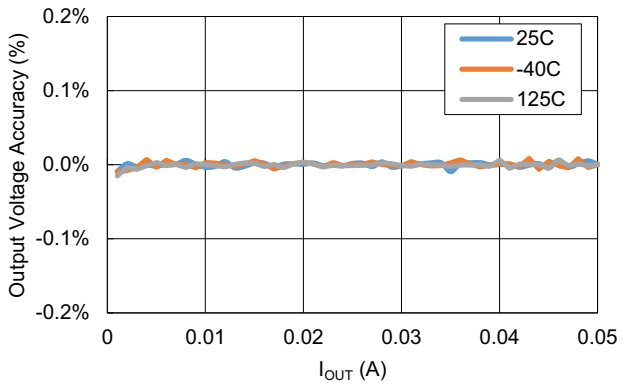


Figure 4. Output Voltage vs Output Current for Various Ambient Temperatures (V_{IN} = 3V, V_{OUT} = V_{ADJ})

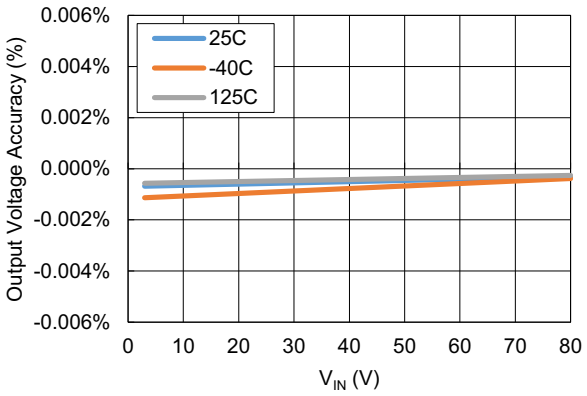


Figure 5. Output Voltage vs Input Voltage for Various Ambient Temperatures (V_{OUT} = V_{ADJ}, I_{OUT} = 0mA)

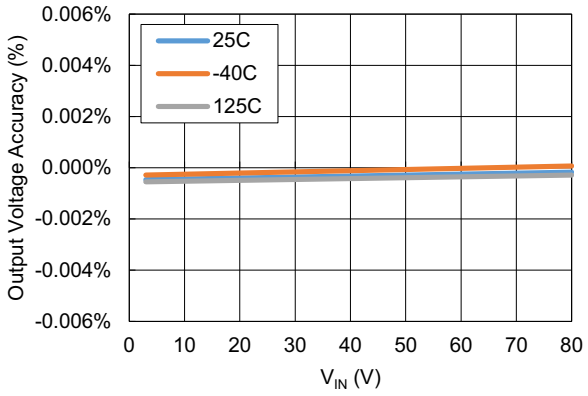


Figure 6. Output Voltage vs Input Voltage for Various Ambient Temperatures (V_{OUT} = V_{ADJ}, I_{OUT} = 1mA)

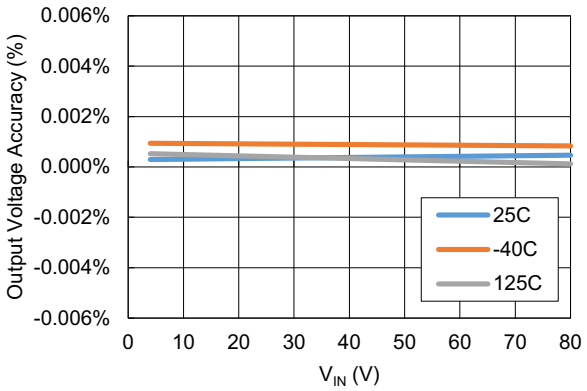


Figure 7. Output Voltage vs Input Voltage for Various Ambient Temperatures (V_{OUT} = 3.3V, I_{OUT} = 1mA)

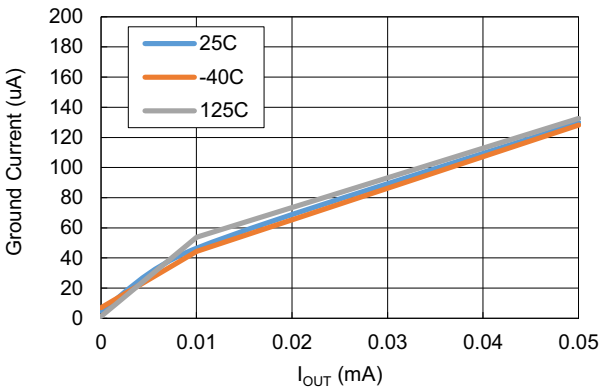


Figure 8. Ground Current for Various Ambient Temperatures (V_{IN} = 3V, V_{OUT} = V_{ADJ}, I_{OUT} = 0A to 50mA)

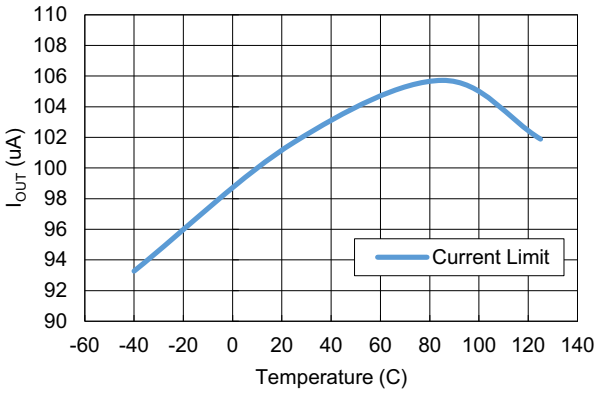


Figure 9. Short-Circuit Current Limit for Various Ambient Temperatures (V_{IN} = 3.5V, V_{OUT} = V_{ADJ})

Operating conditions unless otherwise noted: V_{EN} = 5V, C_{IN} = 10µF MLCC, C_{OUT} = 2.2µF MLCC. (Cont.)

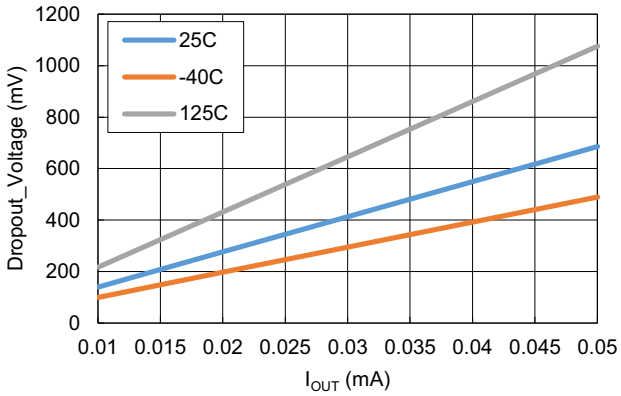


Figure 10. Dropout Voltage vs Output Current for Various Ambient Temperatures (V_{OUT} = 3.3V)

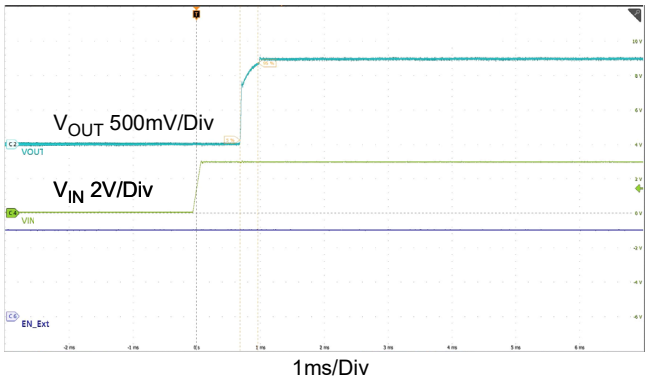


Figure 11. Startup for 25°C (V_{IN} = 2.94V, V_{OUT} = V_{ADJ}, I_{OUT} = 0A)

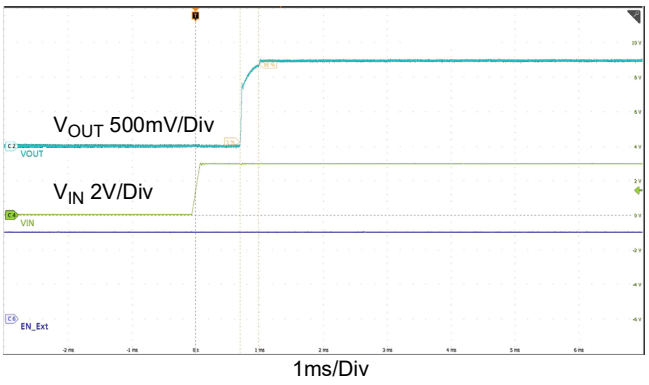


Figure 12. Startup for 25°C (V_{IN} = 2.94V, V_{OUT} = V_{ADJ}, I_{OUT} = 50mA)

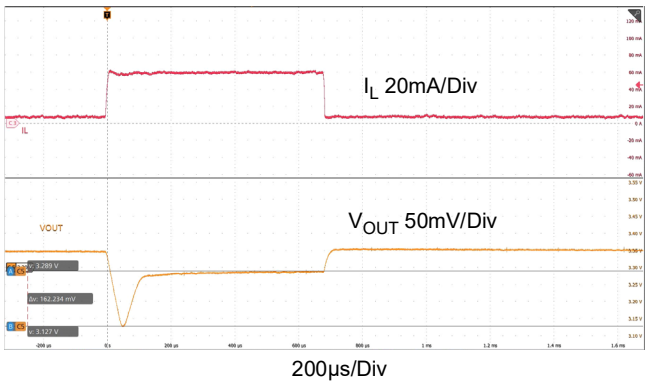


Figure 13. Load Transient Response for 25°C (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0A to 50mA in 10µs, C_{FF} = 47pF)

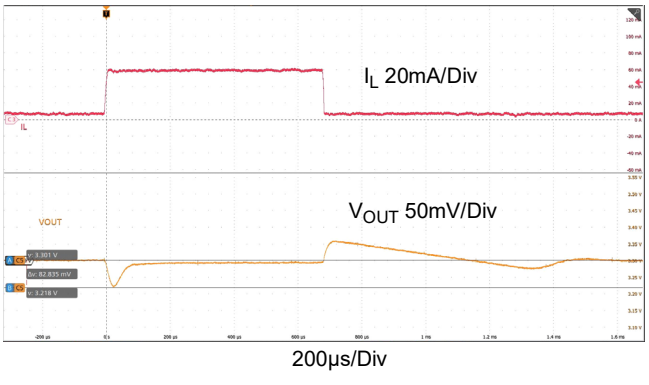


Figure 14. Load Transient Response for 25°C (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA to 50mA in 10µs, C_{FF} = 47pF)

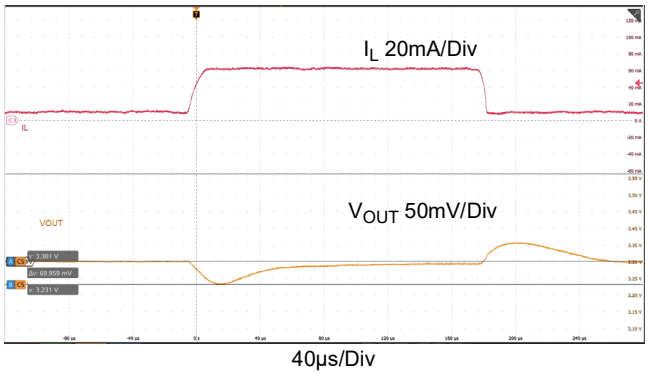


Figure 15. Load Transient Response for 25°C (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 10mA to 50mA in 10µs, C_{FF} = 47pF)

Operating conditions unless otherwise noted: V_{EN} = 5V, C_{IN} = 10µF MLCC, C_{OUT} = 2.2µF MLCC. (Cont.)

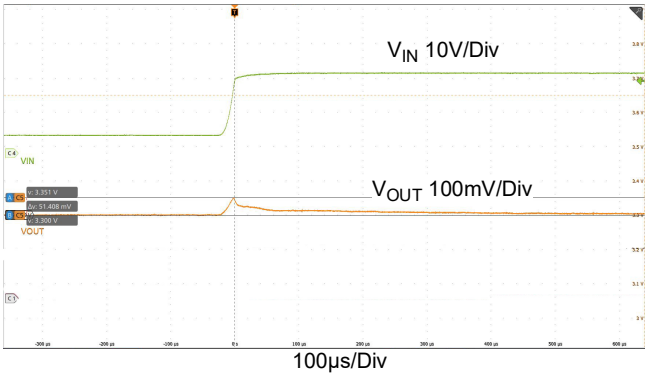


Figure 16. Line Transient Response for 25°C
(V_{IN} = 5V to 24V in 20µs, V_{OUT} = 3.3V, I_{OUT} = 10mA)

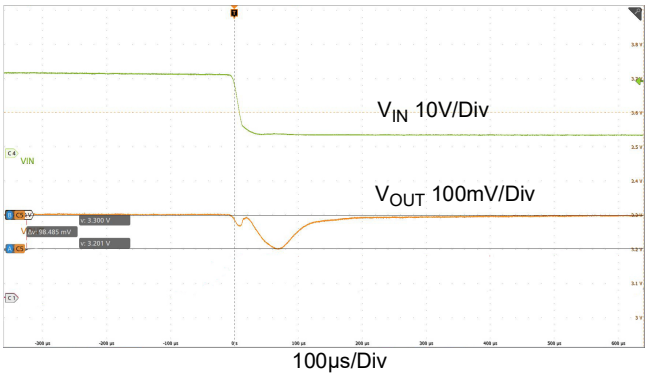


Figure 17. Line Transient Response for 25°C
(V_{IN} = 24V to 5V in 20µs, V_{OUT} = 3.3V, I_{OUT} = 10mA)

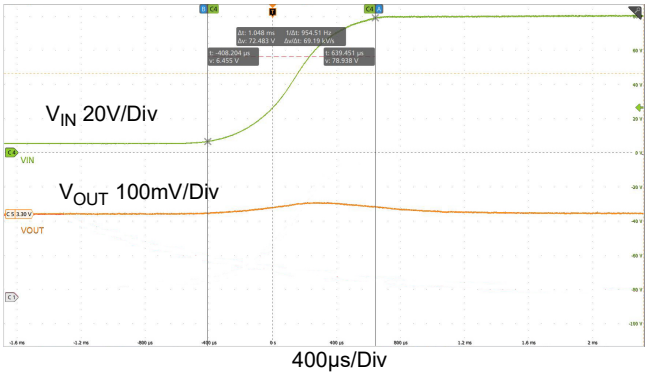


Figure 18. Line Transient Response for 25°C
(V_{IN} = 5V to 80V in 1ms, V_{OUT} = 3.3V, I_{OUT} = 1mA)

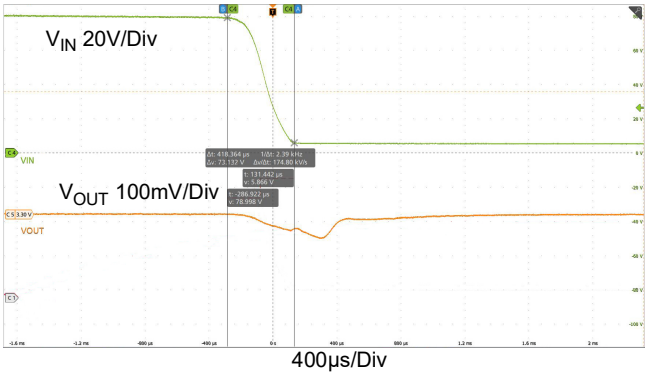


Figure 19. Line Transient Response for 25°C
(V_{IN} = 80V to 5V in 400µs, V_{OUT} = 3.3V, I_{OUT} = 1mA)

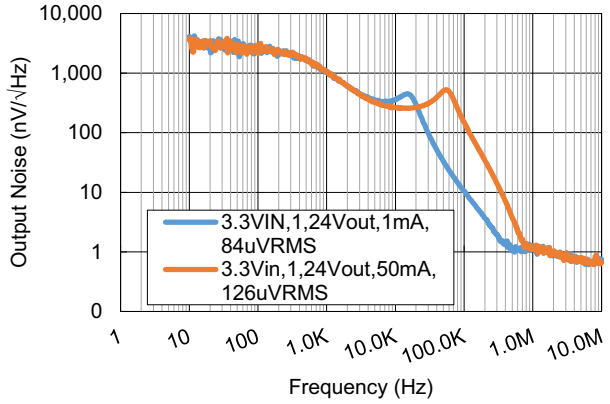


Figure 20. Output Noise vs Frequency for Various I_{OUT}
(V_{IN} = 3.3V, V_{OUT} = V_{ADJ})

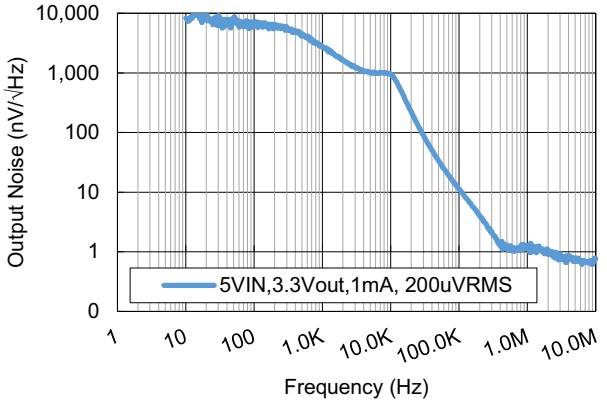


Figure 21. Output Noise vs Frequency
(V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA)

Operating conditions unless otherwise noted: V_{EN} = 5V, C_{IN} = 10µF MLCC, C_{OUT} = 2.2µF MLCC. (Cont.)

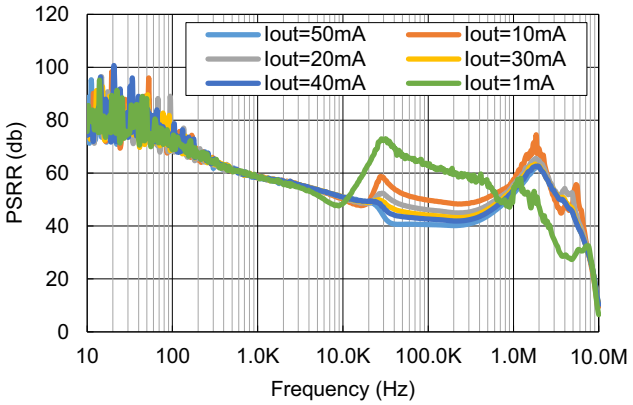


Figure 22. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 6V, V_{OUT} = 3.3V)

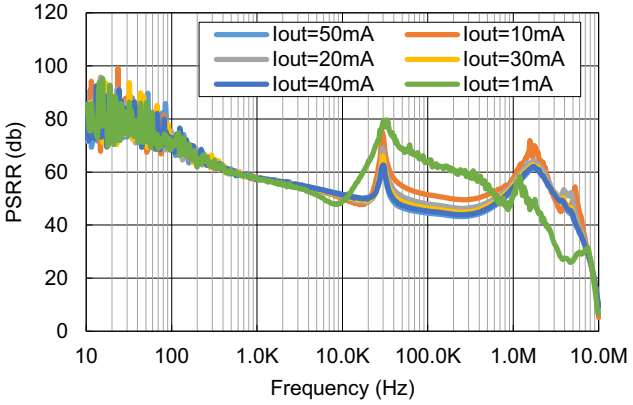


Figure 23. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 12V, V_{OUT} = 3.3V)

5. Application Information

5.1 Overview

The RRP58000 is an adjustable output voltage, low-quiescent current, and low-dropout regulator capable of sourcing up to 50mA. The LDOs work with a minimum 2.2µF ceramic output capacitor and have a wide input voltage range up to 80V. The LDOs feature a ±2.5% output voltage accuracy, input UVLO, enable UVLO, internal current limit, and over-temperature shutdown protection.

The combination of low-quiescent current, low-shutdown current, and small package size makes this an ideal choice for portable devices and battery-powered equipment.

5.2 Theory of Operation of PMOS LDOs

Like the majority of LDOs with a PMOS pass transistor, the RRP58000 DC output voltage (V_{OUT}) regulation can be modeled with a voltage reference (V_{REF}), PMOS pass-transistor, error amplifier, and feedback (FB) resistors as shown in Figure 24.

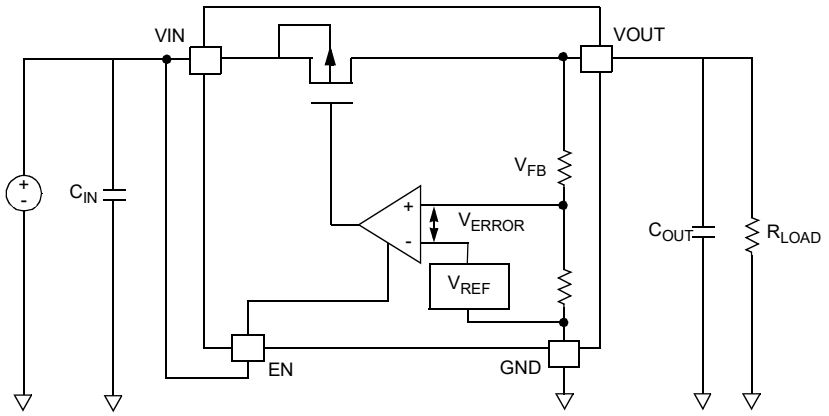


Figure 24. Simple PMOS LDO Regulator Block Diagram

The PMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assuming the input voltage (V_{IN}) remains constant, the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}. This relationship is summarized in Equation 1.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times r_{DS(ON)}$$

V_{OUT} is set by the internal resistors.

The error amplifier compares V_{FB} with the fixed V_{REF} voltage and works to minimize the difference or error voltage between V_{FB} and V_{REF} by changing the gate voltage of the PMOS pass transistor and therefore the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} decreases because the regulator has not responded to the change and the $r_{DS(ON)}$ is set too high. V_{FB} correspondingly decreases and is below the V_{REF} voltage therefore, increasing the error voltage. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more negative relative to the FET source to decrease the $r_{DS(ON)}$, which increases the output voltage bringing it back into regulation.

By similar logic, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to increase because the $r_{DS(ON)}$ is set too low. V_{FB} is then higher than the fixed V_{REF} voltage increasing the error. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more positive relative to the FET source to increase the $r_{DS(ON)}$, which decreases the output voltage bringing it back into regulation.

For a more detailed explanation of the DC regulation operation of a PMOS LDO regulator, see *R16AN0008: Fundamental Theory of PMOS Low-Dropout Voltage Regulators*.

6. Functional Description

6.1 UVLO

The RRP58000 integrates an internal UVLO circuit to keep the devices safely disabled if the input voltage is below the UVLO threshold. This prevents the parts from turning on in an unpredictable state.

When the input voltage is above the UVLO threshold, the parts are enabled, and the output voltage ramps up. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate, and the UVLO hysteresis prevents input voltage droops because of long input traces and wires from turning off the LDO when it turns on and draws current. Figure 25 illustrates the UVLO operation.

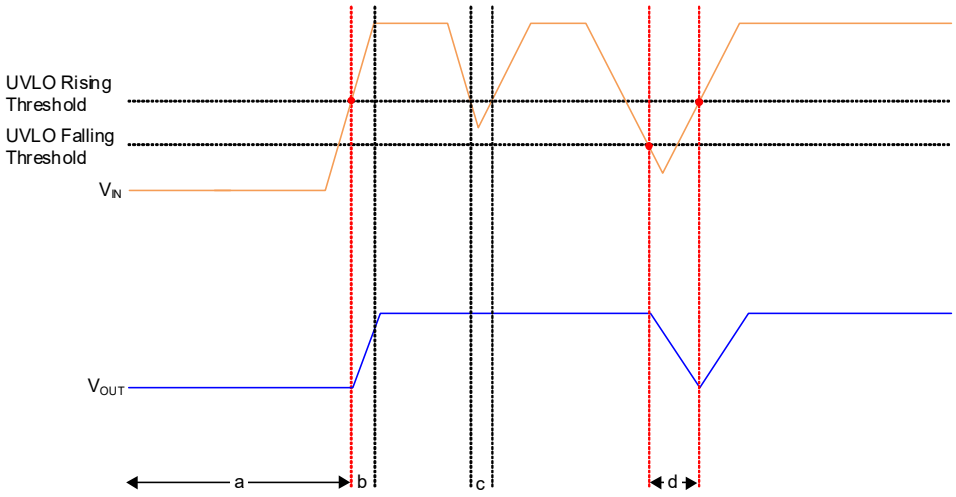


Figure 25. UVLO Operation

a, d The LDO is disabled.

b The LDO is enabled and the output starts to rise.

c The LDO remains enabled because the Input Voltage is still higher than the UVLO falling threshold.

6.2 Enable Control

The RRP58000 has an EN pin voltage (V_{EN}) to enable or disable the LDOs. If V_{EN} is less than the V_{EN} threshold, the LDO is disabled. If V_{EN} is greater than the V_{EN} threshold, the LDO is enabled. The V_{EN} hysteresis prevents enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically 0.2µA. When the LDO is enabled the quiescent current is typically 0.1µA no load.

The EN pin can be directly connected to the input voltage for automatic start-up or connected to a logic controller such as an MCU of FPGA. Some logic pins use an open-collector or open-drain transistor to pull LOW and float when HIGH. Make sure to connect a 1kΩ or 10kΩ pull-up resistor to ensure proper logic HIGH. To ensure proper Enable control operation, the V_{EN} signal source should be capable of swinging above and below the threshold values. The devices also have an accurate and stable Enable threshold, which allows programming of the Enable voltage through a resistor divider.

6.3 Short-Circuit Current Limit Protection

The short-circuit protection circuitry (ILIM) limits the maximum output current that the LDO can source during fault conditions such as short-circuits or start-up inrush current. During a short-circuit fault, the LDO becomes a constant current source resulting from a decrease in load resistance that causes a decrease in the output voltage. This relationship is summarized in Equation 2.

(EQ. 2) $V_{OUT} = ILIM \times R_{FAULT}$

When the short or overcurrent condition is removed, the LDO returns to normal output voltage regulation. Because of the high-power dissipation caused by overcurrent faults, the LDO can begin to cycle ON and OFF because the die junction temperature (T_J) is exceeding thermal fault conditions (typical: +155°C) and subsequently cooling down to +135°C when the LDO is disabled.

6.4 Over-Temperature Shutdown (OTSD) Protection

The RRP58000 is protected against thermal overloads caused by current limit protection or high ambient temperature (T_A). When the die junction temperature (T_J) exceeds the typical +155°C, the thermal shutdown circuit disables the LDO reducing the output current (I_{OUT}) to 0A, therefore, reducing the output voltage (V_{OUT}) to 0V and allowing the LDO to cool. A 20°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a T_J exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, it is important that the design considers the T_A the LDO works in, the thermal resistance between T_J and T_A (θ_{JA}), and any fault conditions that can cause the T_J to exceed the recommended operating range. In some applications, a heat sink might be required for implementation.

6.5 Voltage Requirements

6.5.1 Input Voltage

The RRP58000 operates with an input voltage of 3.5V to 80V on the VIN pin. The input supply must be able to supply enough current to keep the input voltage from drooping during load steps or high load currents.

For proper voltage regulation, the input voltage must be chosen so that it is higher than the sum of the output voltage and the maximum dropout voltage expected for a given application as expressed in Equation 3.

(EQ. 3) $V_{IN} > V_{OUT} + V_{DROPOUT(MAX)}$

The difference between V_{IN} and V_{OUT} required for proper regulation is commonly called the headroom voltage ($V_{HEADROOM}$).

6.5.2 Output Voltage

The RRP58000 output voltage can be programmed down to 1.24V and up to 15V using external resistor (R_1 and R_2) shown in Figure 26.

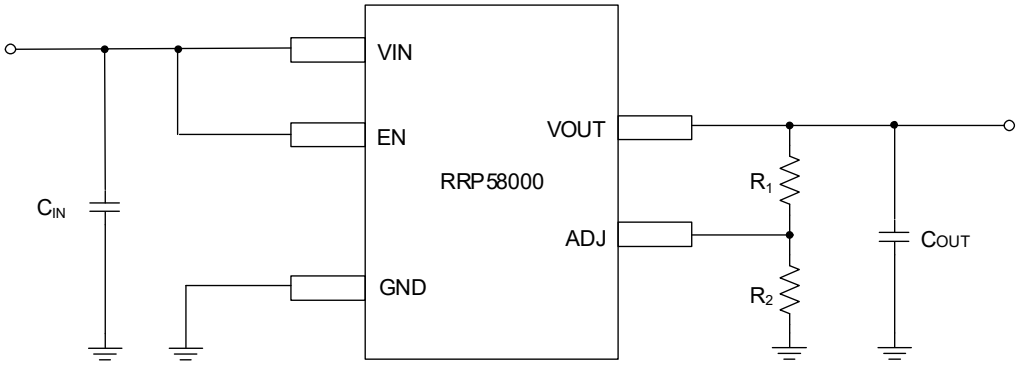


Figure 26. Setting the Output Voltage

V_{OUT} is the required output voltage and can be calculated using Equation 4, where 1.24V is the reference voltage.

(EQ. 4) $$V_{OUT} = 1.24V \times \left(1 + \frac{R_1}{R_2}\right)$$

Similarly, the R_2 resistor value is calculated for any target output voltage by rearranging Equation 4 to get Equation 5. The recommended R_1 (see Figure 26) resistance is 100kΩ. See Table 1 for R_1 and R_2 values for typical V_{OUT} applications.

(EQ. 5) $$R_2 = \frac{R_1}{\left(\frac{V_{OUT}}{1.24V}\right) - 1}$$

Resistors shown on Table 1 are commercially available in a 0.1% tolerance.

Table 1. Recommended R_1 and R_2 Resistor Values for Typical V_{OUT} applications

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)
1.24	0	None
1.5	100	47.5
1.8	100	221
2.5	100	98.8
3	100	70.6
3.3	100	60.4
5	100	33.2
9	100	15.8
12	100	11.5
15	100	8.98

6.6 External Capacitor Selection

The RRP58000 is stable with 2.2µF C_{IN} and C_{OUT} capacitors. For better load transient performance, a 4.7µF or higher output capacitor is recommended.

Multilayer ceramic capacitors (MLCC) are an excellent choice because of their small size, low ESR, low ESL, and wide operating temperature; although, they are not without their problems. Ceramic capacitor values can vary with the DC bias voltage, temperature, and tolerance. Therefore, Renesas recommends using de-rated capacitors.

X5R, X7R, and C0G capacitors are recommended. To ensure the performance of the RRP58000, it is important that the effects of DC bias voltage, temperature, and tolerances for a chosen capacitor are evaluated. The X7R type is recommended because it has lower capacitance variation over-temperature.

Place the bypass capacitors as close as is practical to their respective pins to minimize trace inductance.

6.6.1 Input Capacitor

The minimum input capacitor that is recommended is 2.2µF to reduce the negative effects of large input impedances because of long input traces of high source impedances. Renesas recommends connecting this capacitor between VIN and GND. A larger bulk capacitor such as a 10µF might be required to be added to minimize input voltage droops during large changes in load currents, such as during load transients or start-up to not affect stability. Larger input capacitors also improve the line transient response.

6.6.2 Output Capacitor

The RRP58000 is stable with a 2.2µF minimum output ceramic capacitor.

A large value output capacitor can help minimize the overshoot and undershoot transient response due to large changes in load current. Larger or multiple output capacitors can also be used to improve high-frequency PSRR.

6.7 Power Dissipation and Thermals

To ensure reliable operation, the die junction temperature (T_J) of the RRP58000 must not exceed +125°C. In applications with high ambient temperature (T_A), large headroom voltages ($V_{HEADROOM}$), and large load currents (I_{OUT}), the heat dissipated in the package can become large enough to cause the T_J to exceed the maximum operating temperature of +125°C.

6.7.1 Power Dissipation

The Power Dissipation (PD) is calculated using Equation 6.

(EQ. 6) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

Because the power dissipation contribution from the quiescent (or ground current) is typically small compared to the current, the LDO must supply to a load; it can be ignored, and Equation 6 simplifies to Equation 7.

(EQ. 7) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, to lower the power dissipated inside the die, the $V_{HEADROOM}$ and/or the I_{OUT} can be decreased.

6.7.2 The Junction Temperature and Thermal Resistance

The junction temperature (T_J) is the sum of the environmental ambient temperature (T_A) and the temperature rise in the T_J because of power dissipation, which is calculated using Equation 8.

(EQ. 8) $$T_J = T_A + \theta_{JA} \times PD$$

θ_{JA} is the thermal resistance between the junction temperature and ambient temperature and is dependent on the device package and the PCB design.

7. Layout Guidelines

The following are recommendations for the RRP58000 to achieve optimal performance:

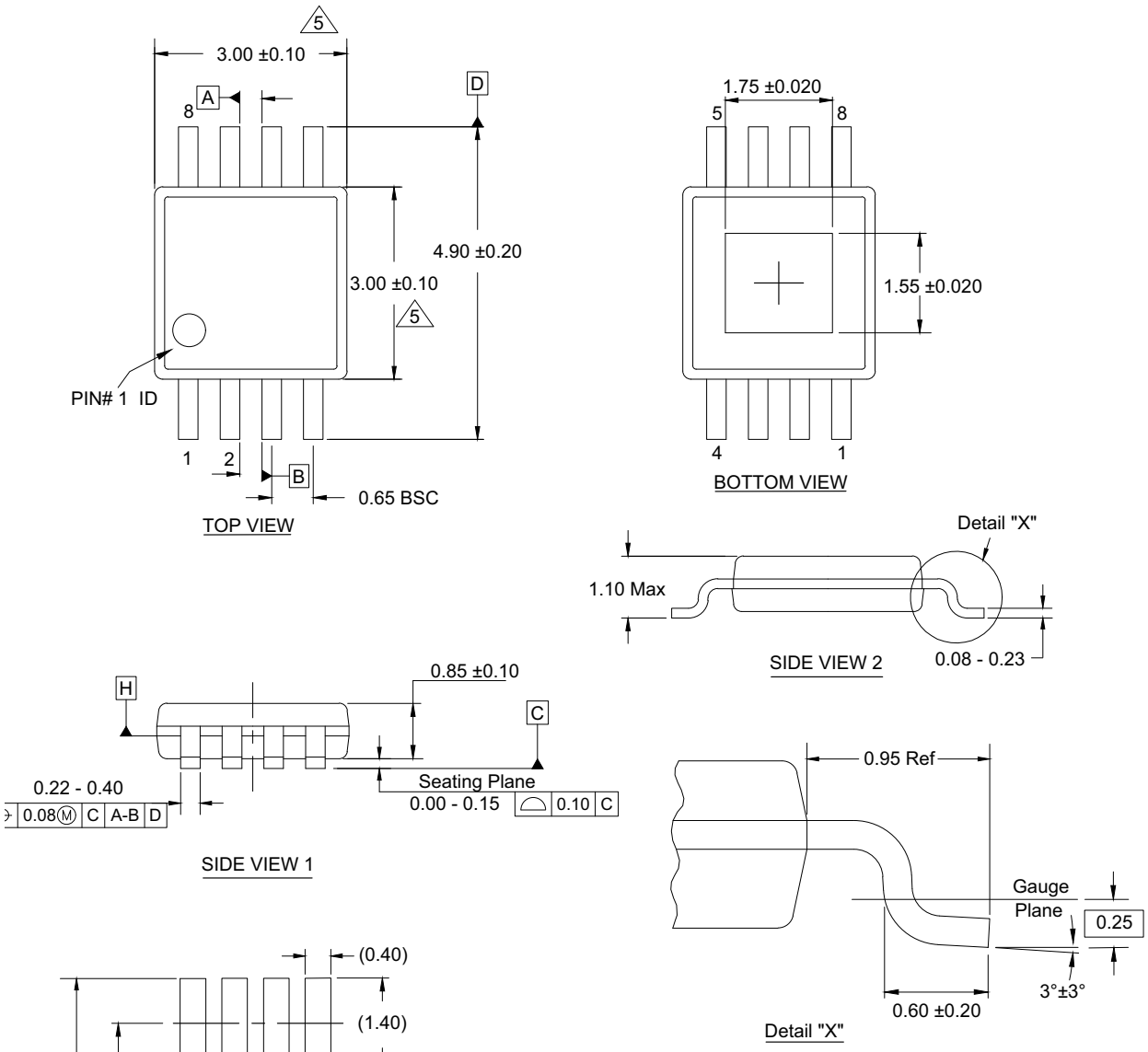
- Place all the required components for the RRP58000 on the same layer as the IC.
- Place a minimum capacitance of 2.2µF ceramic input capacitor to the VIN and GND pins of the LDO as close as practical.
- Place a minimum capacitance of 2.2µF ceramic output capacitor to the VOUT and GND pins of the LDO as close as practical.
- The package thermal EPAD is the largest heat conduction path for the package. Solder it to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area. If possible, adding thermal vias around the PCB package helps improve heat spread from the package to other layers of the board.
- Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow. For efficient heat transfer, the vias must have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane. The top copper GND layer that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

8. Package Outline Drawing

For the most recent package outline drawing, see M8.118C.

M8.118C

8 Lead Heat-Sink Mini Small Outline Plastic Package (HMSOP)
Rev 0, 9/2023



NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and ASME Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

9. Ordering Information

Part Number[1][2]	Part Marking	Output Voltage (V)	Package Description[3] (RoHS Compliant)	Pkg. Dwg #	Carrier Type	Temperature Range
RRP58000-SH0	58000	Adj.	8 Ld HMSOP	M8.118C	Tube	-40°C to +125°C
RTKA58000DR0000BU	Demonstration board					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL) rating, see the RRP58000 product page. For more information about MSL, see TB363.
3. For the Pb-Free reflow profile, see TB493.

10. Revision History

Revision	Date	Description
1.01	Jun 17, 2024	Updated 3.3 Thermal Specifications table: - Added Junction to EVB to the Conditions.
1.00	Jun 5, 2024	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.