RRP68150, RRP68151

100V, 2A Source, 5.3A Sink, 5V Powered, High Frequency GaN/MOS FET Half-Bridge Drivers

Description

The RRP6815x family (RRP68150, RRP68151) is a 5V powered, high frequency half-bridge driver for enhancement mode GaN FETs and low-threshold N-channel MOSFETs. It features 2A source and 5.3A sink current capability with its switching node supporting up to 100V DC. The driver's PWM inputs are 3.3/5V CMOS logic-compatible and can tolerate input voltages up to 14V, independent of the VDD supply voltage. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.4V. This clamping action prevents the gate voltage from exceeding the maximum gate-source voltage rating of the GaN FET. Its 5V operational supply enables convenient supply sharing with the controller.

The drivers feature a fast typical 19/17ns propagation delay and 1.5ns typical delay matching, making it optimal for multi-MHz switching frequency applications.

The RRP6815x family has split-gate outputs, providing the flexibility to adjust turn-on and turn-off strength independently. High-side boot and low-side VDD UVLO protection safeguard against undervoltage operation, enhancing system robustness.

The RRP6815x family is available in small 12-Ball WLCSP (2mm×2mm) package and 14-Lead FCQFN (3mm×3mm) package with wettable flanks. It includes two variants: RRP68150, which integrates anti-shoot-through protection, and RRP68151, which does not. This differentiation enables tailored solutions for diverse application requirements.

Features

- Independent high-side and low-side TTL logic inputs up to 14V regardless of the VDD voltage
- 3.3/5V CMOS I logic-level compatible input stage
- 100V PH voltage rating for high input voltage applications
- 2A sourcing and 5.3A sinking peak driving current for GaN/MOS FETs
- Separately adjustable turn-on and turn-off speed
- Fast propagation delay (19/17ns typical)
- Excellent propagation delay matching (1.5ns typical)
- 4.5V to 5.5V bias supply with UVLO mechanism
- Integrated input and output pull-down resistors
- 4.5ns typical rise time, 2.7ns typical fall time with 1nF Load
- Anti-shoot through protection (RRP68150)
- Small package: WLCSP12-2×2, FCQFN14-3×3

Applications

- Telecom/server half-bridge and full-bridge DC/DC converters
- Half and full-bridge converters
- Synchronous buck converters
- Power modules

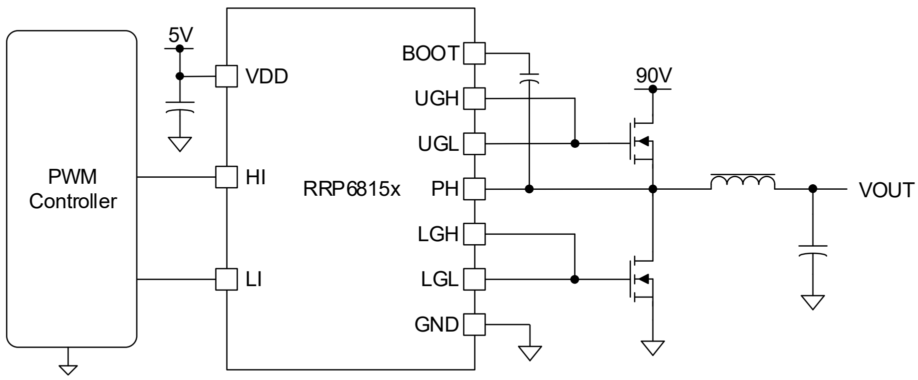


Figure 1. Typical Application

Contents

1. Overview

1.1 Block Diagram

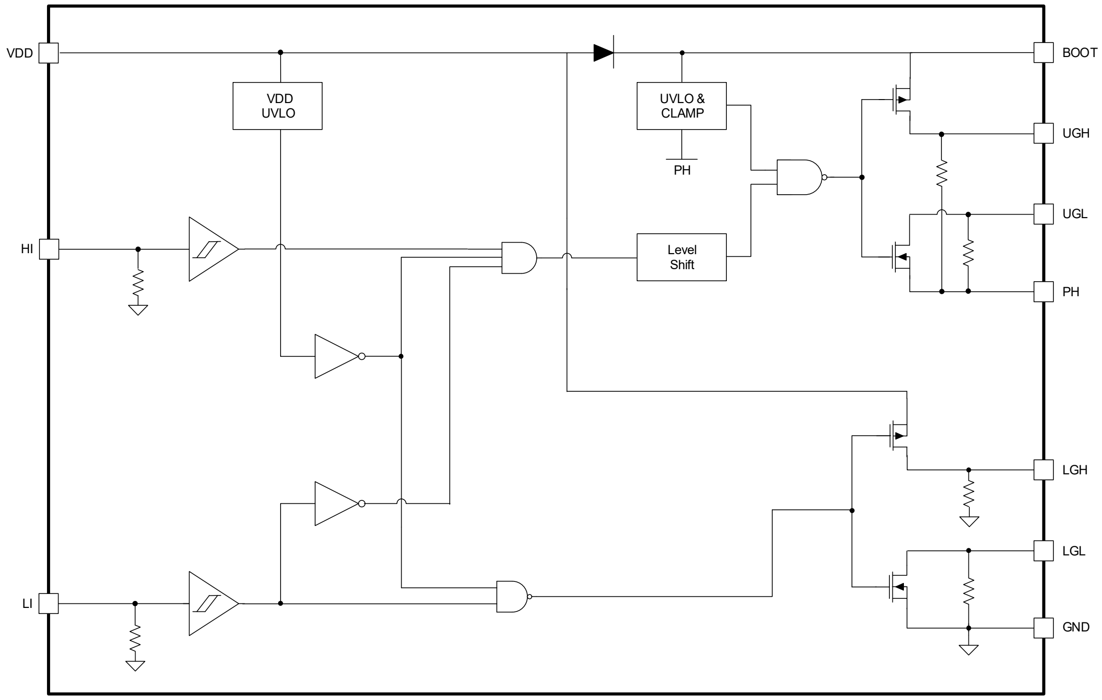


Figure 2. RRP68150 Block Diagram[1]

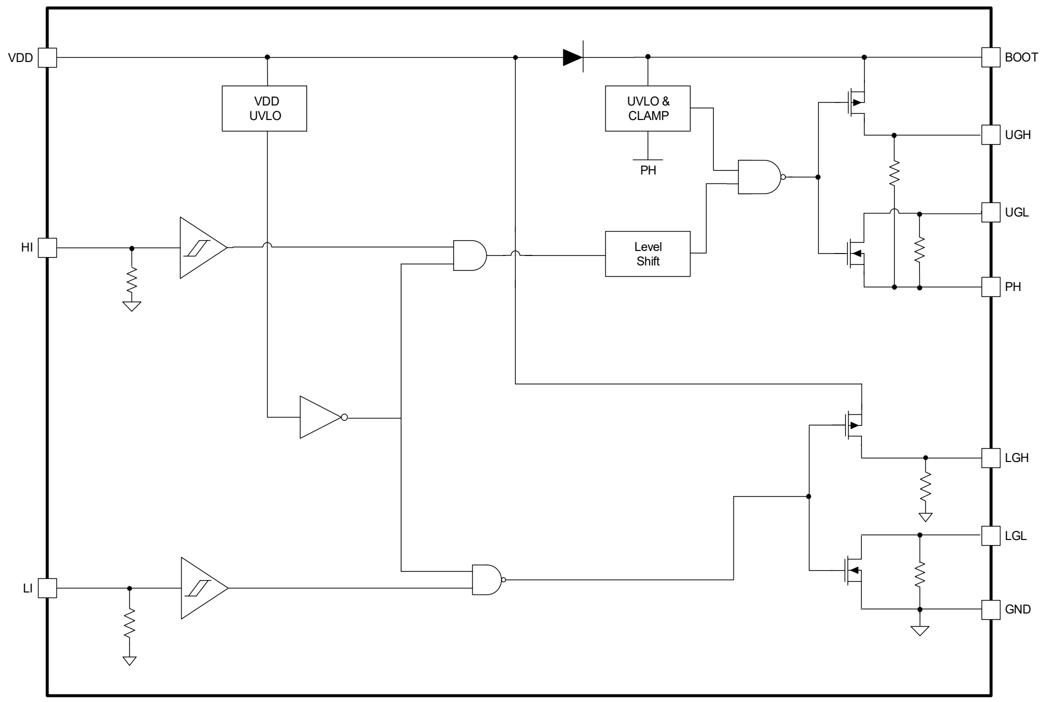


Figure 3. RRP68151 Block Diagram[1]

1. In the FCQFN14-3x3 package, the GND pin is split into AGND and PGND. AGND serves as the bias return path for signal blocks, such as logic gates, while PGND functions as the driver return path for the Low-Side Gate Logic (LGL).

2. Pin Information

2.1 WLCSP

2.1.1 Pin Assignments

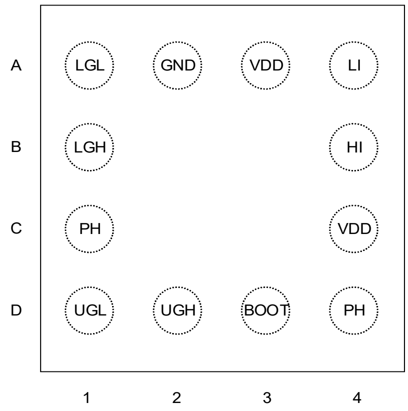


Figure 4. Pin Assignments (WLCSP12-2x2) - Top View

2.1.2 Pin Descriptions

Pin Number	Pin Name	Description
A1	LGL	Low-side gate driver sink-current output. Connect to the gate of the low-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
A2	GND	Ground reference for the VDD supply. Provides the ground return path for driver circuitry and internal reference.Connected to PGND inside the chip.
A3, C4	VDD	5V positive gate drive supply. The two VDD pins are connected internally within the chip. Renesas recommends connecting them externally on the PCB and decouple them to VSS using low ESR/ESL capacitors located as close as possible to the IC.
A4	LI	Low-side driver control input; 3.3/5V CMOS logic-compatible with 14V input tolerance.
B1	LGH	Low-side gate driver source-current output. Connect to the gate of the low-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
B4	HI	High-side driver control input; 3.3/5V CMOS logic-compatible with 14V input tolerance.
C1, D4	PH	High-side gate driver reference node. The two pins are connected internally within the chip. Connect this pin to the bootstrap capacitor negative terminal and the source of the upper GaN/MOS FET.
D1	UGL	High-side gate driver sink-current output. Connect to the gate of the high-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
D2	UGH	High-side gate driver source-current output. Connect to the gate of the high-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.
D3	BOOT	High-side bootstrap supply voltage for the upper gate driver referenced to HS. Connect an 1µF(typical) X7R ceramic capacitor to this pin and PH.

1. When driving GaN devices with relatively low gate charge (Qg) (usually associated with higher $R_{DS(ON)}$), the strong gate drive capability of the RRP6815x requires special consideration. Renesas provides a dedicated design note on this topic. See Input and Output for further details.

2.2 FCQFN14

2.2.1 Pin Assignments

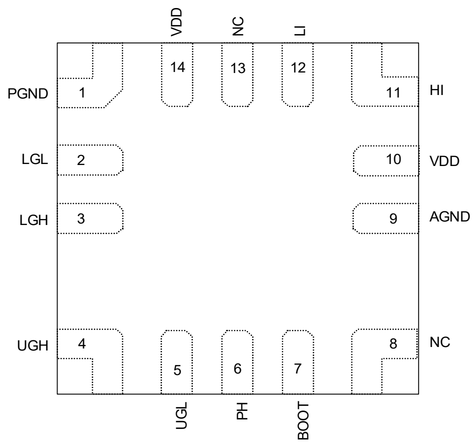


Figure 5. Pin Assignments (FCQFN14-3x3) - Top View

2.2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	PGND	Pin for low-side driving current return. Place the VDD bypass capacitor close to this pin. Connected to AGND inside the chip. For QFN package, Renesas recommends connecting the two GND pins together on the PCB.
2	LGL	Low-side gate driver sink-current output. Connect to the gate of the low-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
3	LGH	Low-side gate driver source-current output. Connect to the gate of the low-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
4	UGH	High-side gate driver source-current output. Connect to the gate of the high-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
5	UGL	High-side gate driver sink-current output. Connect to the gate of the high-side GaN/MOS FET. Maintain the driving path as short as possible to ensure optimal system robustness and safety.[1]
6	PH	High-side gate driver reference node. The two pins are connected internally within the chip. Connect this pin to the bootstrap capacitor negative terminal and the source of the upper GaN/MOS FET.
7	BOOT	High-side bootstrap supply voltage for the upper gate driver referenced to HS. Connect an 1µF(typical) X7R ceramic capacitor to this pin and PH.
8, 13	NC	Do not connect any extern circuit or GND net to these pins.
9	AGND	Ground reference for the VDD supply. Provides the ground return path for driver circuitry and internal reference.Connected to PGND inside the chip.
10, 14	VDD	5V positive gate drive supply. The two VDD pins are connected internally within the chip. Renesas recommends connecting them externally on the PCB and decouple them to VSS using low ESR/ESL capacitors located as close as possible to the IC.
11	HI	High-side driver control input; 3.3/5V CMOS logic-compatible with 14V input tolerance.
12	LI	Low-side driver control input; 3.3/5V CMOS logic-compatible with 14V input tolerance.

1. When driving GaN devices with relatively low gate charge (Qg) (usually associated with higher $R_{DS(ON)}$), the strong gate drive capability of the RRP6815x requires special consideration. Renesas provides a dedicated design note on this topic. See Input and Output for further details.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
VDD	-0.3	6	V
HI, LI	-0.3	18	V
PH	-5	109	V
BOOT to PH	-0.3	6	V
BOOT	0	115	V
LGL,LGH	-0.3	VDD+0.3	V
UGL, UGH to PH	-0.3	BOOT+0.3	V
Operating Junction Temperature Range	-40	150	°C
Maximum Storage Temperature Range	-65	150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	+100	mA

1. All voltages referenced to GND (AGND and PGND are connected together as GND) unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter[1]	Minimum	Typical	Maximum	Unit
Supply Voltage, VDD	4.5	5	5.5	V
Input Voltage, HI or LI	0	-	14	V
Voltage on phase, PH	-2	-	100	V
Bootstrap Voltage, BOOT-PH	PH+4	-	PH+5.5	V
PH-GND Slew Rate	-	-	50[2]	V/ns
Operating Junction Temperature Range	-40	-	125	°C

1. All voltages referenced to GND unless otherwise specified.
2. Guaranteed by design characterization.

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	12-Ball WLCSP 2mm×2mm	θ_{JA}[1]	Junction to ambient	91	°C/W
		θ_{JC}[2]	Junction to case	0.9	
		θ_{JB}	Junction to board	23	
Thermal Characterization		Ψ_{JC}[3]	PSI - Junction to case	32.2	
		Ψ_{JB}[3]	PSI - Junction to board	48.6	
Max Power Dissipation		P_{D_MAX}[4]	+25°C in Free Air	1.37	W
Thermal Resistance	14-Lead SCTQFN Plastic Package	θ_{JA}[1]	Junction to ambient	63	°C/W
		θ_{JC}[2]	Junction to case	43	
		θ_{JB}	Junction to board	18	
Thermal Characterization		Ψ_{JC}[3]	PSI - Junction to top	26.7	
		Ψ_{JB}[3]	PSI - Junction to board	36.8	
Max Power Dissipation		P_{D_MAX}[4]	+25°C in Free Air	1.98	W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board with direct attach features in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the top side of the package.
3. Tested on RTKP68150DE00010BC and RTKP68150DE00000BC.
4. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. based on test described in TB379.

3.4 Electrical Specifications

V_{DD} = $V_{BOOT\text{-}PH}$ = 5V; GND = PH = 0V; HI = LI = 0 No load on LG or UG, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C.**

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VDD Quiescent Current	I_{DD_S}	HI = LI = 0, V_{DD} = V_{HB} = 5V	-	150	**300**	µA
VDD Operation Current	I_{DD_D}	f = 500kHz, duty cycle = 50%	-	0.7	**1.26**	mA
BOOT Quiescent Current	I_{BOOT_S}	HI = LI = 0, V_{DD} = V_{HB} = 5V	-	450	**900**	µA
BOOT Operation Current	I_{BOOT_D}	f = 500kHz, duty cycle = 50%	-	0.75	**1.5**	mA
PWM Input Pins						
Input Voltage Threshold (Falling)	V_{TH_F}	-	**1.0**	1.4	**1.8**	V
Input Voltage Threshold (Rising)	V_{TH_R}	-	**1.6**	2.1	**2.7**	V
Input Voltage Hysteresis	-	-	-	0.7	-	V
Input Pull-Down Resistance	R_{IN}	-	**100**	200	**300**	kΩ
Undervoltage Protection						
VDD Rising Threshold	VDD_R	-	**3.9**	4.2	**4.5**	V
VDD Threshold Hysteresis	VDD_H	-	-	0.2	-	V
Bootstrap Rising Threshold	$BOOT_R$	-	**3.15**	3.4	**3.65**	V
Bootstrap Threshold Hysteresis	$BOOT_H$	-	-	0.6	-	V
Bootstrap Diode and Clamp						
Bootstrap Diode Forward Voltage	V_{DROP}	100µA load applied on BOOT and PH pins, BOOT charged by VDD	-	0.65	**0.85**	V
Dynamic Resistance	R_{DROP}	Calculated at 80mA and 100mA point	-	1	**2.5**	Ω
Boot to PH Clamp Regulation Voltage	V_{BT_REG}	V_{PH} = -2V	**5.1**	5.4	**5.7**	V
Low and High-Side Gate Driver						
Low-Level Output Voltage	V_{OL}	100mA into LGL or UGL pin	-	24[2]	-	mV

V_{DD} = $V_{BOOT-PH}$ = 5V; GND = PH = 0V; HI = LI = 0 No load on LG or UG, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C. (Cont.)**

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
High-Level Output Voltage	V_{OH}	100mA out from LGH or UGH pin	-	4.9[2]	-	V
UGH, UGL Pull-Down to PH Resistor	R_{OUT_H}	-	-	500	-	kΩ
LGH, LGL Pull-Down to GND Resistor	R_{OUT_L}	-	-	500	-	kΩ
Peak Sourcing Current	I_{SRC_P}	Output = 0V	-	2[2]	-	A
Peak Sinking Current	I_{SNK_P}	Output = 5V	-	5.3[2]	-	A

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Parameters that show only a typical value characterized by engineering sample, might not be fully tested in production.

3.5 Switching Specifications

V_{DD} = $V_{BOOT-PH}$ = 5V; GND = PH = 0V; HI = LI = 0V to 5V. No load on LG or UG, unless otherwise specified. **Boldface limits apply across the operating temperature range, - 40°C to +125°C.**

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
LG Turn-High Delay	t_{D_LGH}	No capacitor on Output pin	-	19	-	ns
LG Turn-Low Delay	t_{D_LGL}		-	17	-	ns
UG Turn-High Delay	t_{D_UGH}		-	19	-	ns
UG Turn-Low Delay	t_{D_UGL}		-	17	-	ns
Delay Matching[2]	-		-	1.5	-	ns
LG Rising Time	t_{R_LG}	1nF capacitor load on Output pin	-	4.5	-	ns
LG Falling Time	t_{F_LG}		-	2.7	-	ns
UG Rising Time	t_{R_UG}		-	4.5	-	ns
UG Falling Time	t_{F_UG}		-	2.7	-	ns
Minimum Positive Width of Input Pulse	t_{MIN_P}	No capacitor load on output pin	-	10	-	ns
Minimum Negative Width of Input Pulse	t_{MIN_N}		-	10	-	ns

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Parameters that show only a typical value characterized by engineering sample, may not be fully tested in production.

3.6 Timing Diagrams

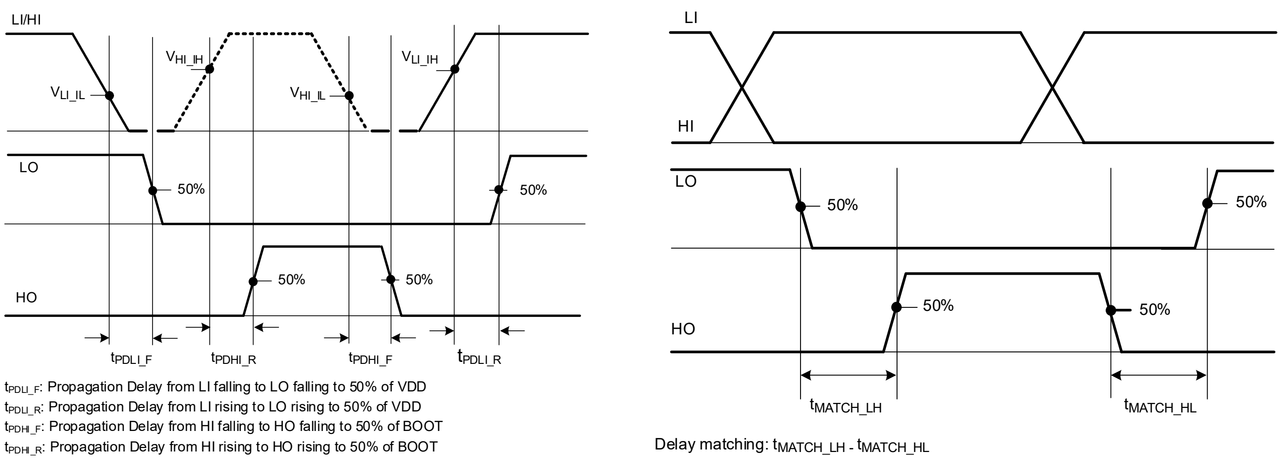


Figure 6. Propagation Delay Timing Diagram

Note: The LO output high state corresponds to LGH high and LGL low; the LO output low state corresponds to LGH low and LGL high. Similarly, the HO output high state corresponds to UGH high and UGL low; and the HO output low state corresponds to UGH low and UGL high.

4. Typical Performance Curves.

Unless otherwise specified, operating conditions at: T = +25°C; V_{DD} = $V_{BOOT\text{-}PH}$ = 5V; GND = PH = 0V; Capacitor from BOOT to PH pin C_{BOOT} = 1µF

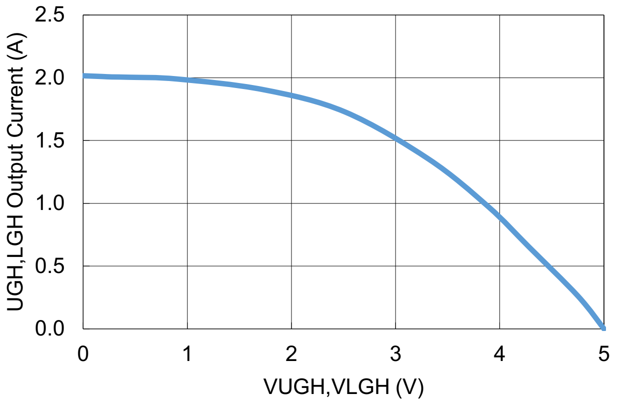


Figure 7. I_{SRC} vs Output Voltage

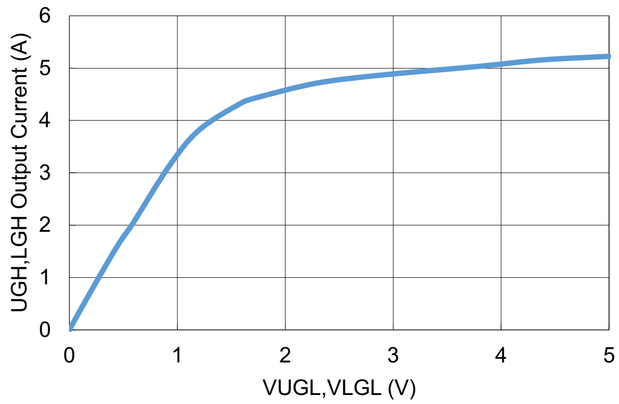


Figure 8. I_{SNK} vs Output Voltage

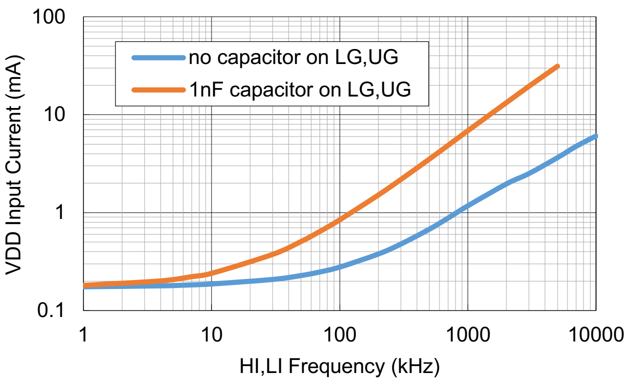


Figure 9. I_{DD_D} vs Frequency

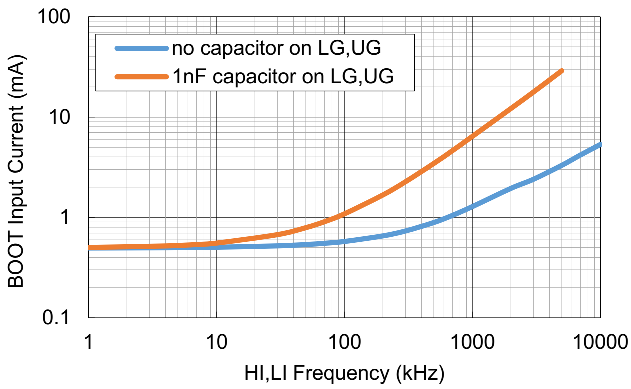


Figure 10. I_{BOOT_D} vs Frequency

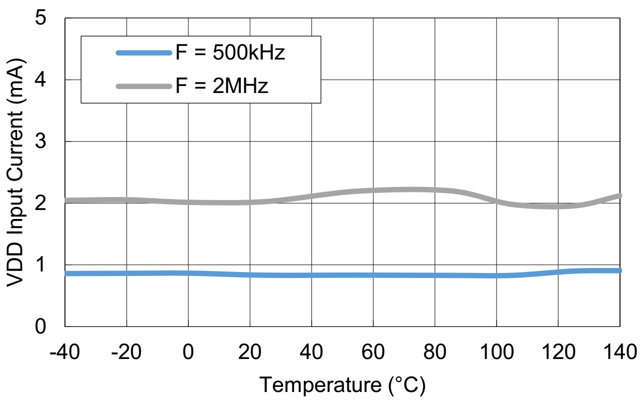


Figure 11. I_{DD_D} vs Temperature

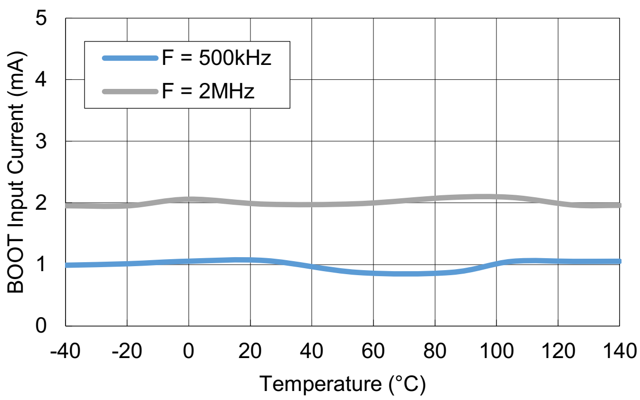


Figure 12. I_{BOOT_D} vs Temperature

Unless otherwise specified, operating conditions at: T = +25°C; V_{DD} = $V_{BOOT\text{-}PH}$ = 5V; GND = PH = 0V; Capacitor from BOOT to PH pin C_{BOOT} = 1µF (Cont.)

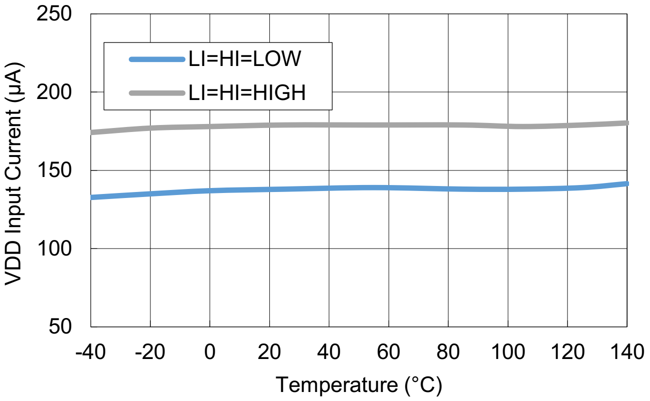


Figure 13. I_{DD_S} vs Temperature

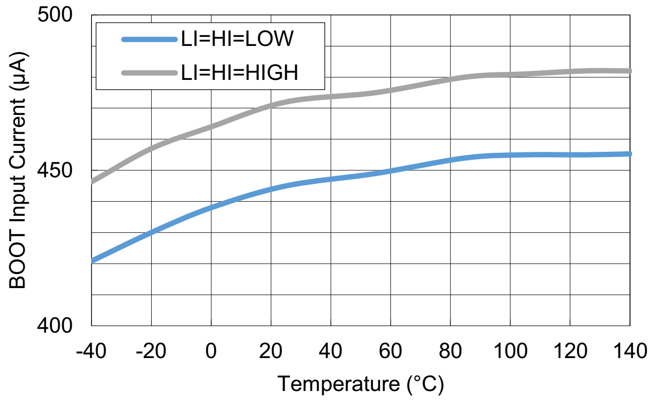


Figure 14. I_{BOOT_S} vs Temperature

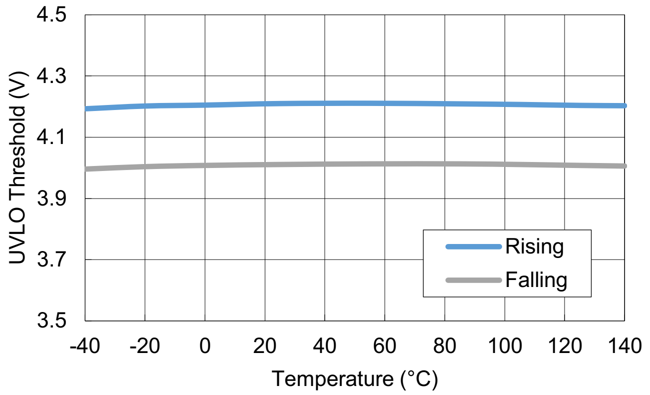


Figure 15. VDD UVLO Threshold vs Temperature

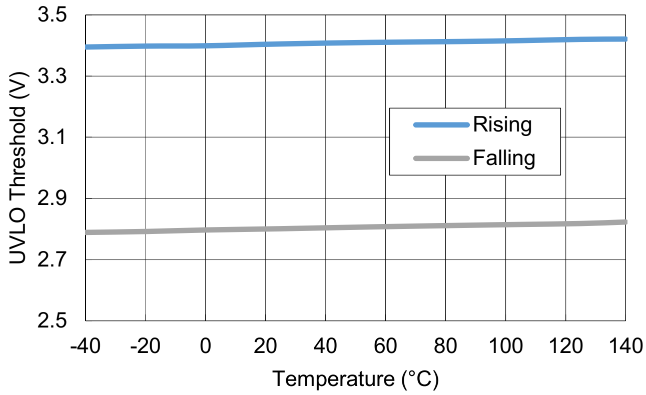


Figure 16. BOOT UVLO Threshold vs Temperature

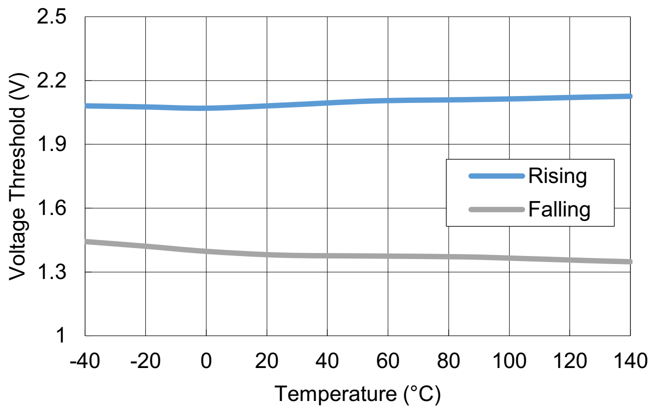


Figure 17. V_{TH} vs Temperature

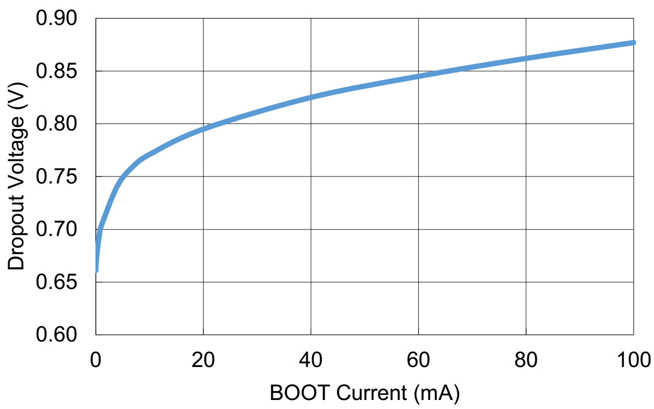


Figure 18. V_{DROP} vs BOOT Current

Unless otherwise specified, operating conditions at: T = +25°C; V_{DD} = $V_{BOOT\text{-}PH}$ = 5V; GND = PH = 0V; Capacitor from BOOT to PH pin C_{BOOT} = 1µF (Cont.)

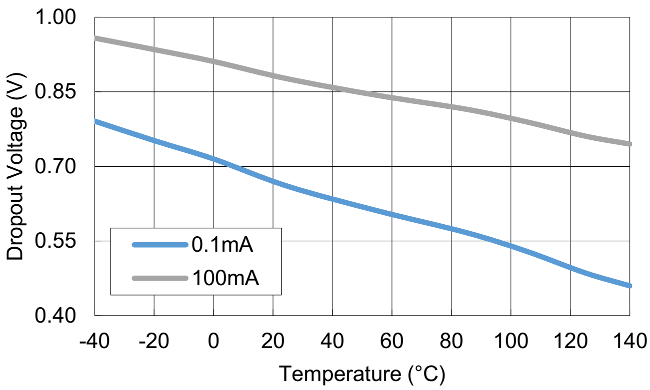


Figure 19. V_{DROP} vs Temperature

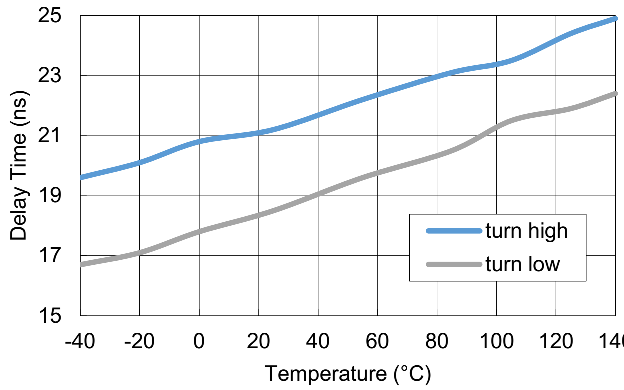


Figure 20. t_{D_LG} vs Temperature

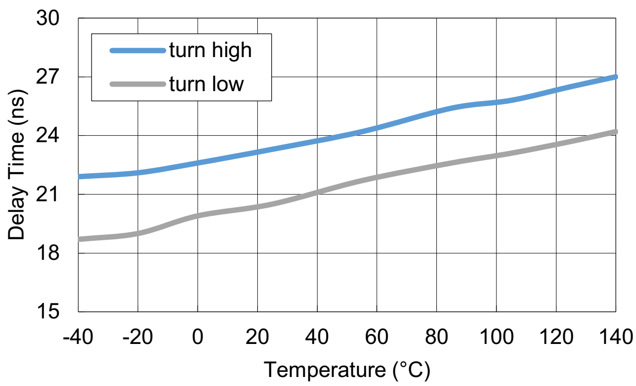


Figure 21. t_{D_UG} vs Temperature

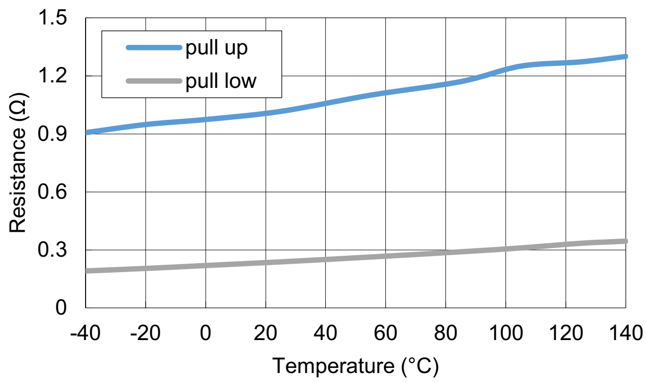


Figure 22. Output Resistance vs Temperature

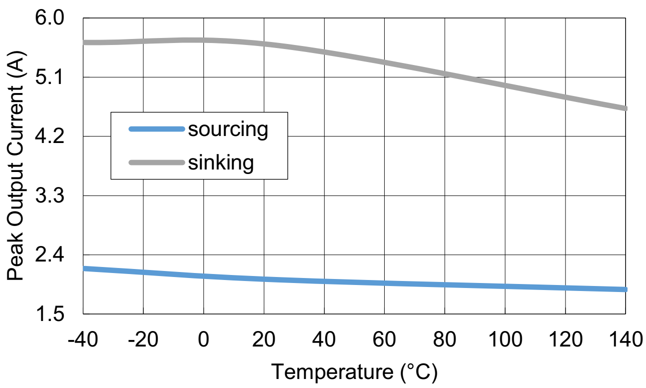


Figure 23. Peak Driving Current vs Temperature

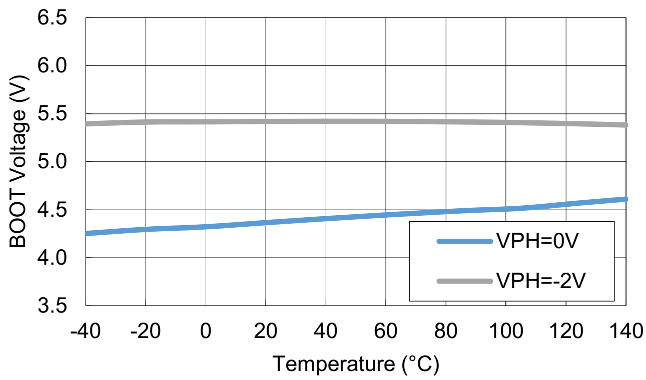


Figure 24. VBT_REG vs Temperature

5. Functional Description

5.1 Overview

The RRP6815x family is a half-bridge gate driver designed for high-frequency applications, powered by a standard 5V supply rail. It is specifically optimized for driving enhancement mode GaN FETs and N-channel MOSFETs, in synchronous buck, boost, LLC, or other half-bridge topologies.The device features a PH node voltage rating up to 100V, making it suitable for high voltage applications. The high-side bias voltage is generated via a bootstrap technique and is internally clamped at 5.4V, which ensures that the gate voltage remains within the maximum gate-source voltage rating of the GaN FETs.The RRP6815x family incorporates split-gate outputs that provide robust source and sink current capabilities, offering the flexibility to adjust the turn-on and turn-off speeds independently.

The driver is capable of operating at switching frequencies up to several MHz, depending on the specific capacitive load and ambient temperature. It is available in a WLCSP12-2x2 or a FCQFN14-3x3 package, providing a compact footprint and reduced package inductance.

5.2 Input and Output

The RRP6815x family features independent input pins with 3.3/5V CMOS logic-level compatibility. These inputs offer a high tolerance, capable of withstanding up to 14V stress regardless of the VDD supply voltage. This wide input range allows for a direct interface with analog PWM controllers powered by supplies up to 14V, therefore, eliminating the requirement for external buffer stages and reducing component count.

The resistance of RRP6815x's output MOS are specifically optimized for GaN FETs to ensure high-frequency and efficient operation. A 0.33Ω pull-down resistance establishes a robust, low-impedance turn-off path, which is essential for preventing unwanted turn-on events often caused by high dv/dt or high di/dt. Similarly, a 1Ω[1] pull-up resistance aids in minimizing ringing and overshoot on the switching node voltage. The split outputs of the RRP6815x provide flexibility to adjust turn-on and turn-off speeds by adding external resistance in the respective paths.

If the input signal is unused for either channel (HI or LI), the pin should be left floating. The input state is forced low by an internal 200kΩ pull-down resistor.

Note: When driving GaN devices with relatively low gate charge (Qg) (usually higher $R_{DS(ON)}$), due to RRP6815x's strong gate drive capability, Renesas recommends adding appropriately valued gate resistors individually to both the UGH and LGH pins before connecting them to the gates of the respective GaN devices to mitigate potential noise and ringing issues. As an illustration, 3Ω was effective for GaN devices with a Qg of ~11.7nC, while 5Ω was appropriate for GaN devices with a Qg of ~4.5nC, both verified up to 1.5MHz. For the UGL and LGL pins, a default resistor value of 0.33Ω is typically used regardless of the connected FETs.

5.3 Start-up and UVLO

The RRP6815x family integrates undervoltage lockout (UVLO) protection for both VDD and bootstrap supplies. When VDD falls below the VDD UVLO, HI and LI inputs are ignored to prevent partial turn-on of GaN/MOS FETs. In this condition, 500kΩ pull-down resistors on the output pins drive the LS and HS gate terminals to a low state. If VDD drops below the VDD UVLO, the driver actively pulls LG and UG low to protect the power devices. When VDD is above VDD UVLO but the BOOT–PH voltage is below the BOOT UVLO threshold, only UG is pulled low.

Table 1 shows a truth table between the inputs and outputs.

Table 1. Truth Table

HI	LI	Anti-Shoot Through	UGH	UGL	LGH	LGL
L	L	Any	Open	L	Open	L
L	H		Open	L	H	Open
H	L		H	Open	Open	L

Table 1. Truth Table (Cont.)

HI	LI	Anti-Shoot Through	UGH	UGL	LGH	LGL
H	H	N	H	Open	H	Open
		Y	L	Open	H	Open

Table 2 summarize the output states under various VDD and BOOT conditions.

Table 2. VDD and $V_{BOOT-PH}$ UVLO feature logic

VDD Condition	$V_{BOOT-PH}$ Condition	Anti-Shoot Through	HI	LI	UG	LG
VDD<VDD UVLO	Any	Any	0	0	0	0
			0	1	0	0
			1	0	0	0
			1	1	0	0
VDD>VDD UVLO	$V_{BOOT-PH}$<BOOT UVLO		0	0	0	0
			0	1	0	1
			1	0	0	0
			1	1	0	1
	$V_{BOOT-PH}$>BOOT UVLO		0	0	0	0
			0	1	0	1
			1	0	1	0
		N	1	1	1	1
		Y			0	1

5.4 PH Negative Voltage and Bootstrap Supply Voltage Clamping

Due to the nature of enhancement-mode GaN FETs, the bottom switch can exhibit a source-to-drain voltage greater than the forward voltage of a diode when its gate is low, resulting in a negative transient on the PH pin. This effect can be amplified by PCB layout and parasitic inductance at the drain/source terminals. In high-side driver applications using a floating bootstrap configuration, a negative PH voltage can cause the BOOT–PH voltage (high side gate drive voltage) exceeds GaN FET gate voltage limitation.

To mitigate this risk, the RRP6815x family incorporates an internal clamping circuit that limits the BOOT–PH voltage, thereby preventing potential damage to the high-side GaN FET. The clamp activates with a delay of ~82ns after the threshold is exceeded, during which the external BOOT capacitor helps prevent overvoltage. Effective clamping is ensured when PH remains within –1V to –3V (typical).

Note: Although the PH pin may momentarily reach –5V, resulting in a temporary increase in BOOT–PH voltage, it is critical to ensure that the negative transient is brief so the bootstrap capacitor can absorb the excess voltage without over stress.

5.5 Level Shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage, which is referenced to the switch node (PH). The level shift allows control of the UG output, which is referenced to the PH pin and provides excellent delay matching with the low-side driver. Typical delay matching between LG and UG is around 1.5ns. The level-shift circuit withstands 50V/ns slew rate.

5.6 Anti-Shoot-Through

This driver includes two types: RRP68150 and RRP68151. The RRP68150 integrates anti-shoot-through protection, ensuring that the upper gate output is allowed to go high only when the low-side input signal is low.

This built-in logic guarantees safe switching and preventing cross-conduction. In contrast, the RRP68151 offers enhanced flexibility by allowing users to configure the PWM dead time externally, enabling precise timing control according to specific application requirements.

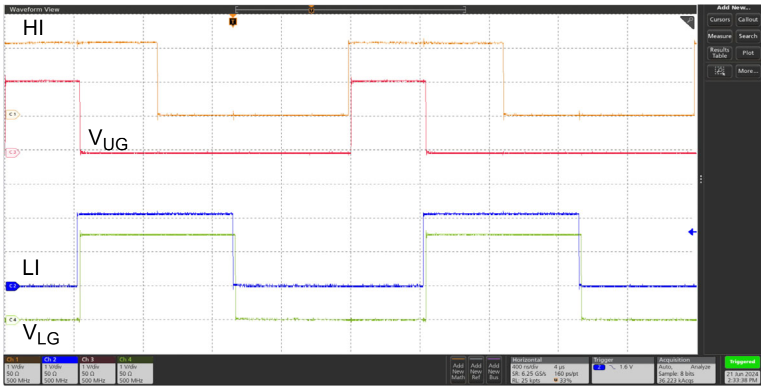


Figure 25. Operation Waveform of Anti-Shoot Through

Note: There is no built-in dead time between UG and LG; therefore, dead time must be implemented in the controller.

6. Applications Information

6.1 Overview

To enable high-frequency switching and minimize associated losses in GaN transistors, a high-performance gate driver is placed between the PWM controller and the transistor gates. Gate drivers are essential when the PWM controller's output lacks the voltage or current capability to directly drive the switching devices.

This is especially common in digital power systems, where PWM signals are typically 3.3/5V CMOS logic levels. These signals are referenced to ground and cannot effectively turn on power switches such as GaN FETs or MOS FETs whose source terminals often float above ground potential. To address this, a level-shift circuit is required to translate the ground-referenced PWM signal to a gate-drive voltage referenced to the switching node, ensuring full enhancement of the power device and minimizing conduction losses.

Traditional buffer drive circuits using NPN/PNP bipolar transistors in a totem-pole configuration are inadequate for digital power applications due to their lack of level-shifting capability. Gate drivers overcome this limitation by integrating both level-shifting and buffer-drive functions. In addition, gate drivers fulfill several critical roles:

- Suppressing high-frequency switching noise by placing the driver IC close to the power switch
- Driving gate transformers and managing floating gate configurations
- Offloading gate charge power losses from the controller to the driver, thereby reducing thermal stress and improving overall system efficiency.

The RRP6815x family is a high-frequency half bridge gate driver, designed for GaN/MOS FETs in synchronous buck, boost, and half-bridge topologies. It employs a bootstrap technique to generate the high-side bias voltage, which is internally clamped at 5.4V under normal PH conditions to prevent gate overdrive beyond the maximum gate-to-source rating of GaN devices. The driver features split-gate outputs with strong sink capability, enabling independent control of turn-on and turn-off drive strength for optimized switching performance.

6.2 Typical Application Circuit

Figure 26 shows a typical application of the RRP6815x in a buck regulator configuration. For the complete schematic and design details, refer to the *RTKP68150DE00000BC Evaluation Board Manual*. The following sections are derived based on this reference circuit.

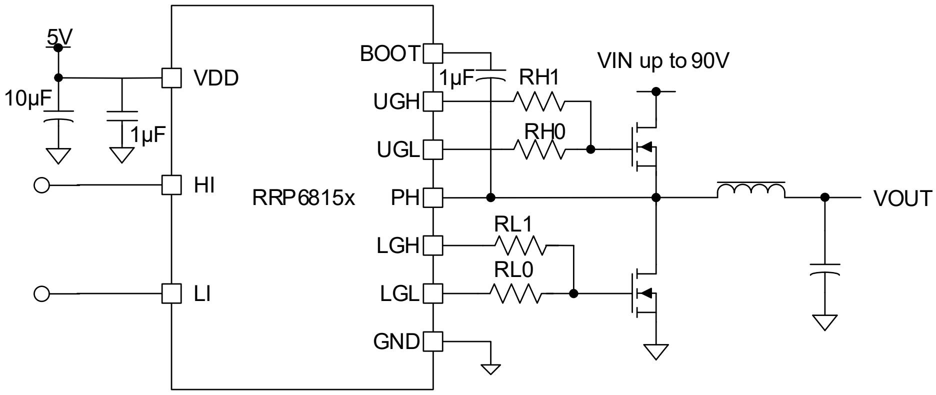


Figure 26. Typical Buck Application

6.3 Design Requirements

When designing a synchronous buck converter using the RRP6815x gate driver with GaN or MOSFETs, several key design parameters must be carefully evaluated to ensure optimal component selection. These include input voltage range, passive components, operating frequency, and controller selection.

Table 3 shows sample values for a typical application.

Table 3. Design Parameters

Parameters	Design Target
Power Input Voltage (V_{IN})	36V to 56V
Output Voltage (V_{OUT})	12V
Output Current (I_{OUT})	10A
Dead Time	20ns
Inductor (L)	4.7µH
Switching frequency (f_{SW})	350kHz

These specifications are essential for evaluating the electrical and thermal stress on the gate driver, including factors such as voltage transients, gate-induced spikes, ringing, switching slew rate, and overall thermal performance.

6.4 VDD Bypass Capacitor

The VDD bypass capacitor supplies the gate charge required for both the low-side and high-side transistors, and also absorbs the reverse recovery charge from the bootstrap diode, ensuring stable driver operation during high-speed switching events. Use Equation 1 to calculate the required bypass capacitance.

(EQ. 1)

$$C_{VDD} > \frac{Q_{gH} + Q_{gL} - Q_{rr}}{\Delta V}$$

where

- Q_{gH} is the total gate charge required to drive the high-side FET.
- Q_{gL} is the total gate charge required to drive the low-side FET.

- Q_{rr} is the reverse recovery charge of the internal bootstrap diode, dependent on the negative PH voltage. Use a worst-case value of 1nC for design calculations.
- ΔV is the acceptable ripple voltage across VDD capacitor, must remain below the VDD_H threshold.

If the calculated VDD bypass capacitance is 320nF, account for the DC bias-induced capacitance degradation typical of ceramic capacitors by applying a multiplier of 4 to 10. As a result, a final value of 1µF to 2µF is recommended.

Renesas advises using an X7R ceramic capacitor for VDD bias and ensuring a compact layout with a short loop between the capacitor, VDD pin, and GND pin. For improved transient response, one or two additional 10µF X5R capacitors should be placed nearby.

6.5 BOOT Bypass Capacitor

The bootstrap capacitor supplies the gate charge for the high-side switch, provides DC bias for the high-side undervoltage lockout circuitry, and absorbs the reverse recovery charge of the bootstrap diode. Use Equation 2 to calculate the required bypass capacitance.

(EQ. 2) $$C_{BST} > \frac{I_{BOOT\_S} \times T_{ON} + Q_{gH} + Q_{rr}}{\Delta V}$$

where:

- T_{ON} is the maximum on-time period of the high-side transistor.
- I_{BOOT_S} is the quiescent current of the high-side driver, which is illustrated in the Electrical Specifications.
- ΔV is the acceptable ripple voltage across BOOT capacitor, typically equal to $BOOT_H$.

If the calculated bootstrap capacitance is 62nF, consider the DC bias derating characteristics of ceramic capacitors. To ensure sufficient effective capacitance under operating conditions, apply a multiplier of 4 to 10, resulting in a recommended value of 0.22µF to 1µF.

Renesas advises using an X7R ceramic capacitor for BOOT bias and ensuring a compact layout with a short loop between the capacitor, BOOT pin, and PH pin.

In GaN-based applications, the PH node often exhibits fast negative voltage transients (typically -2V to -3V), which can elevate the BOOT–PH voltage and potentially distort pulse width. To maintain stable BOOT–PH operation, a 1µF capacitor is typically recommended.

6.6 Power Dissipation

The power consumption of the gate driver is a key factor in determining its maximum operating frequency. It must remain within the package's thermal dissipation limits at the target operating temperature to ensure reliable performance; specifically, the junction temperature should not exceed 150 °C. For the RRP68150, total power dissipation comprises gate driver losses and bootstrap diode losses.

losses. Gate driver losses result from charging and discharging the capacitive gate load and can be estimated using Equation 3.

(EQ. 3) $$P = [C_{GL} \times V_{DD}^2 + V_{GH} \times (V_{DD} - 0.7)^2] \times f_{SW} + Q_{gH} \times f_{SW} \times 0.7 + Q_{rr} \times f_{SW} \times (V_{IN} - V_{DD})$$

where

- C_{GL} is the capacitive load on low-side driver output.
- C_{GH} is the capacitive load on high-side driver output.
- f_{SW} is the switching frequency of the converter.
- V_{IN} is input voltage to the power the power stage (For example, buck topology).

The dropout of boot diode is assumed to be 0.8V. To be more precise, this can be iterated per Figure 18 based on the calculated boot current in last iteration step.

When operating at extreme duty cycles (very narrow or wide), Equation 3 may yield up to 30% deviation from measured results because of output ringing caused by PCB trace inductance and IC bond wire parasitics.

For a given ambient temperature, T_A, Equation 4 can be used to estimate the junction temperature.

(EQ. 4) $$T_J = T_A + P \times \theta_{JA}$$

6.7 Application Waveforms

Figure 27 and Figure 28 were captured from RTKP68150DE00000BC with 80V input and 40V output.

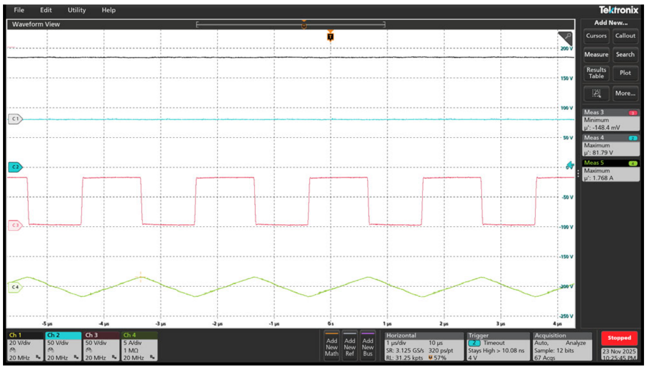


Figure 27. 0A load

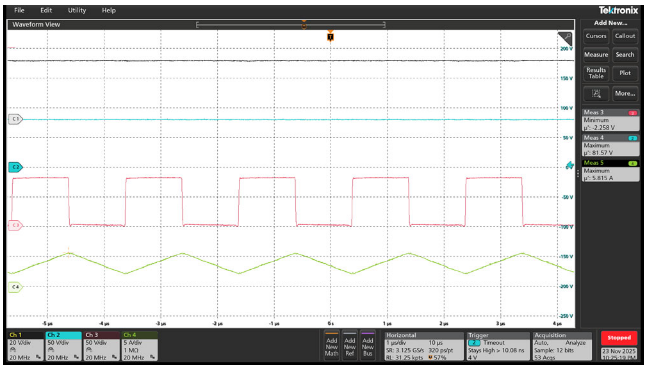


Figure 28. 4A load

6.8 PCB Layout

Lower gate capacitance and Miller capacitance enable enhancement mode GaN FETs to operate at fast switching speed. The RRP6815x family is optimized for such fast applications, however, careful PCB layout remains critical. High dv/dt and di/dt transients can induce gate and body voltage stress, which potentially lead to false turn-on events due to coupled or parasitic gate voltages. Here are some layout recommendations:

- When designing the driver layout, special attention should be paid to the VDD bypass capacitor. For the WLCSP12-2×2 package, a 1 µF ceramic capacitor should be placed close to pads A2 and A3, with a short trace connecting pad C4 to A3. For the FCQFN14-3×3 package, a 1 µF VDD capacitor should be located near Pins 1 and 14, and an additional 0.1 µF capacitor should be placed close to Pins 9 and 10. A short trace on another layer should connect Pins 9 and 1 to minimize parasitic inductance.
- The BOOT-PH capacitor layout is equally important. For the WLCSP12-2×2 package, a 1 µF ceramic capacitor should be placed close to pads C1 and D3, with a 1 mm-wide trace connecting C1 to D4 on another layer. To ensure robust connectivity, two to four vias should be used to link the BOOT-PH path across PCB layers. For the FCQFN14-3×3 package, the 1 µF BOOT capacitor should be placed close to Pins 6 and 7.
- Ensure the driving path is as short as possible, and minimize the loop area enclosed by the path. Specifically, the low-side driving path includes LGL/LGH, gate resistors, the GaN gate and source, and A2 or pin 1. Similarly, keep the high-side driving path (consisting of UGL/UGH, gate resistors, the GaN gate and source, and C1 or Pin 6) as short as possible.
- Ensure that HI and LI signals are routed close to their sources, such as the MCU or power controller. This helps minimize noise coupling and improves signal integrity.
- Ensure there is a single GND reference point. Connect the driver GND to the system or board GND at the HEMT/FET source node.

Figure 29 shows an example of typical layout for WLCSP12-2×2.

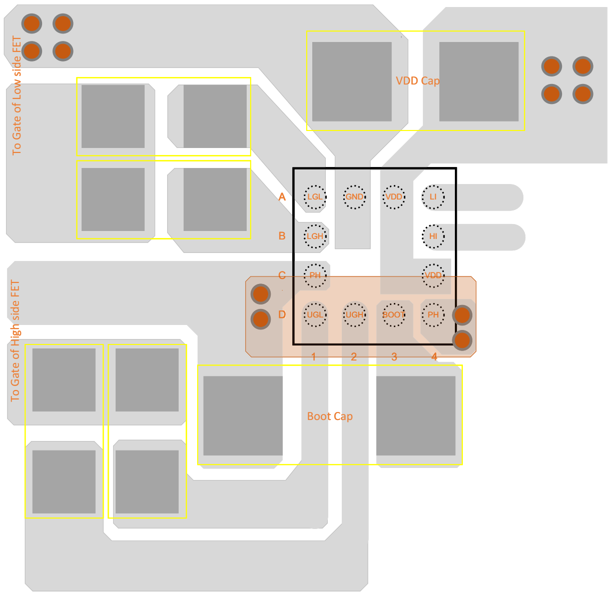


Figure 29. Layout Example for WLCSP12-2×2

Figure 30 shows an example of typical layout for FCQFN14-3×3.

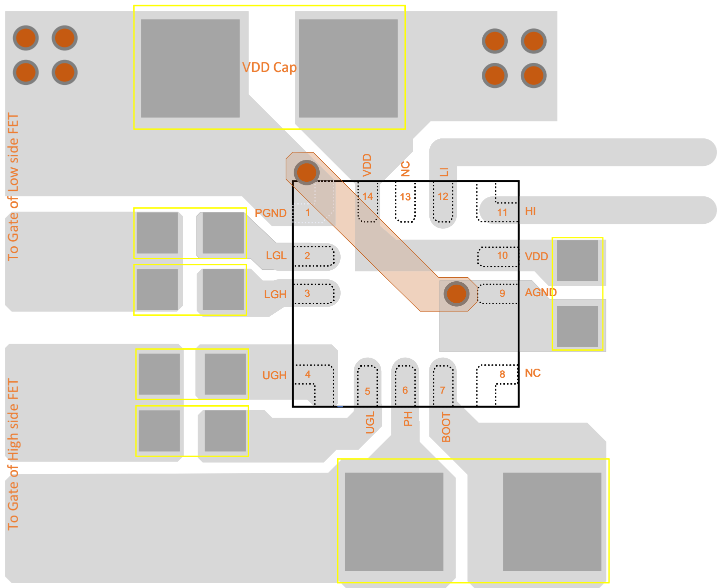


Figure 30. Layout Example for FCQFN14-3×3

7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1]	Anti-Shoot Through Protection	Part Marking	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Junction Temperature Range
RRP68150-BH0[4]	Y	8150[5]	12 Balls WLCSP 4×4	W4x4.12	Reel, 3k	-40 to 125°C
RRP68150-NH0[6]	Y	68150	14L SC-FCTQFN 3×3	L14.3x3	Reel, 6k	
RRP68151-BH0[4]	N	8151[5]	12 Balls WLCSP 4×4	W4x4.12	Reel, 3k	
RRP68151-NH0[6]	N	68151	14L SC-FCTQFN 3×3	L14.3x3	Reel, 6k	

1. For Moisture Sensitivity Level (MSL), see the RRP68150, RRP68151 product information pages. For more information about MSL, refer to TB363.
2. For the Pb-Free Reflow Profile, see TB493.
3. Refer to TB347 for details about reel specifications.
4. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu-e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
5. The part marking is located on the backside of die.
6. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

9. Revision History

Revision	Date	Description
1.02	Feb 19, 2026	Updated the timing diagram
1.01	Jan 8, 2026	Added ECAD Information
1.00	Dec 4, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRP68150-BH0	12	WLCSP	W4x4.12
RRP68150-NH0	14	SC-FCTQFN	L14.3x3
RRP68151-BH0	12	WLCSP	W4x4.12
RRP68151-NH0	14	SC-FCTQFN	L14.3x3

A.2 Symbol Pin Information

A.2.1 12-WLCSP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
A1	LGL	Output	-
A2	GND	Power	-
A3	VDD	Power	-
A4	LI	Input	-
B1	LGH	Output	-
B4	HI	Input	-
C1	PH	Passive	-
C4	VDD	Power	-
D1	UGL	Output	-
D2	UGH	Output	-
D3	BOOT	Power	-
D4	PH	Passive	-

A.2.2 14-SC-FCTQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	PGND	Power	-
2	LGL	Output	-
3	LGH	Output	-
4	UGH	Output	-
5	UGL	Output	-
6	PH	Passive	-
7	BOOT	Power	-
8	NC	Passive	-
9	AGND	Power	-
10	VDD	Power	-
11	HI	Input	-
12	LI	Input	-
13	NC	Passive	-
14	VDD	Power	-

A.3 Symbol Parameters

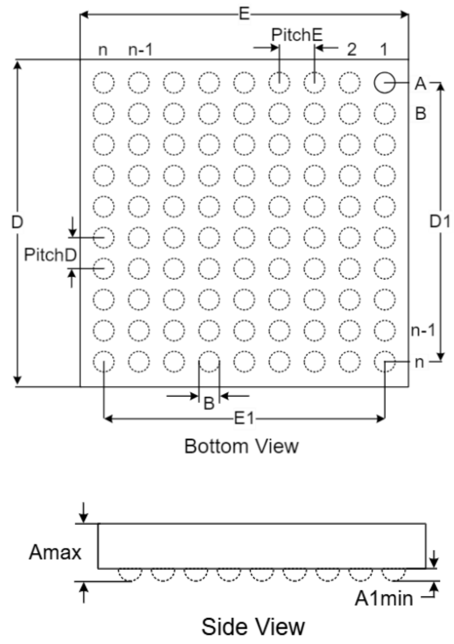
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Junction Temperature	Max Junction Temperature	Min Supply Voltage	Max Supply Voltage	Peak Source Current	Peak Sink Current	Max PH Voltage
RRP68150-BH0	Industrial	SMD	Compliant	-40 °C	125 °C	4.5 V	5.5 V	2 A	5.3 A	100 V
RRP68150-NH0	Industrial	SMD	Compliant	-40 °C	125 °C	4.5 V	5.5 V	2 A	5.3 A	100 V
RRP68151-BH0	Industrial	SMD	Compliant	-40 °C	125 °C	4.5 V	5.5 V	2 A	5.3 A	100 V
RRP68151-NH0	Industrial	SMD	Compliant	-40 °C	125 °C	4.5 V	5.5 V	2 A	5.3 A	100 V

A.4 Footprint Design Information

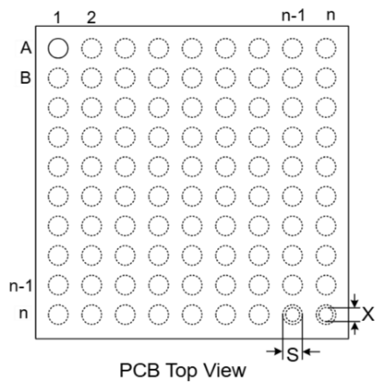
A.4.1 12-WLCSP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
WLCSP	W4x4.12/WA0012AA	12

Description	Dimension	Value (mm)	Diagram
Minimum body Length (vertical side)	Dmin	1.86	
Maximum body Length (vertical side)	Dmax	1.92	
Average length of grid (vertical side)	D1ave	1.20	
Minimum body Width (horizontal side)	Emin	1.86	
Maximum body Width (horizontal side)	Emax	1.92	
Average length of grid (horizontal side)	E1ave	1.20	
Average ball diameter	Bnom	0.265	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.40	
P = Plain Grid, S = Staggered Grid	GridType	P	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	SD	
Number of balls (vertical side)	Rows	4	
Number of balls (horizontal side)	Columns	4	
Maximum number of ball positions (Rows x Columns)	Nmax	16	
Number of actual balls present	PinCount	12	
Ball positions removed from matrix. Example: C5-H10,B6-B9,A1	DepopulateBalls	B2,B3,C2,C3	
Minimum Standoff Height	A1min	0.00	
Maximum Height	Amax	0.55	



Recommended Land Pattern (NSMD Design)			
Description	**Dimension**	**Value (mm)**	**Diagram**
Diameter of pad. If specified this overrides the calculated value. This can be used to specify a manufacturer's recommended pad size.	X	0.215	
Solder Mask Expansion.	S	0.315	

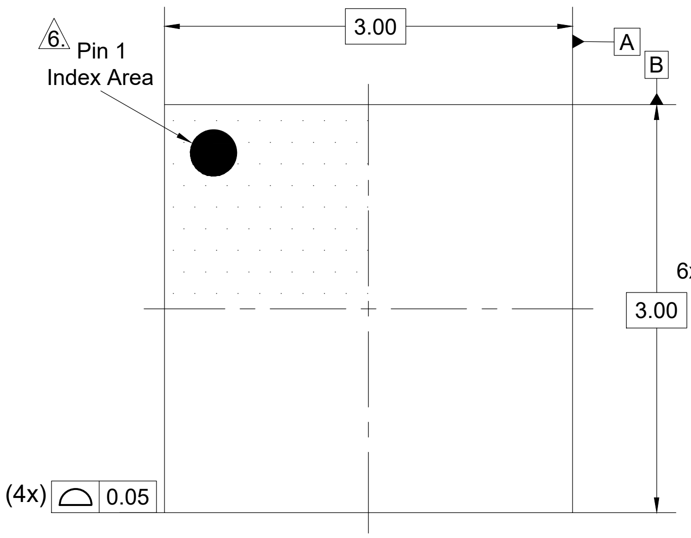


A.4.2 14-SC-FCTQFN

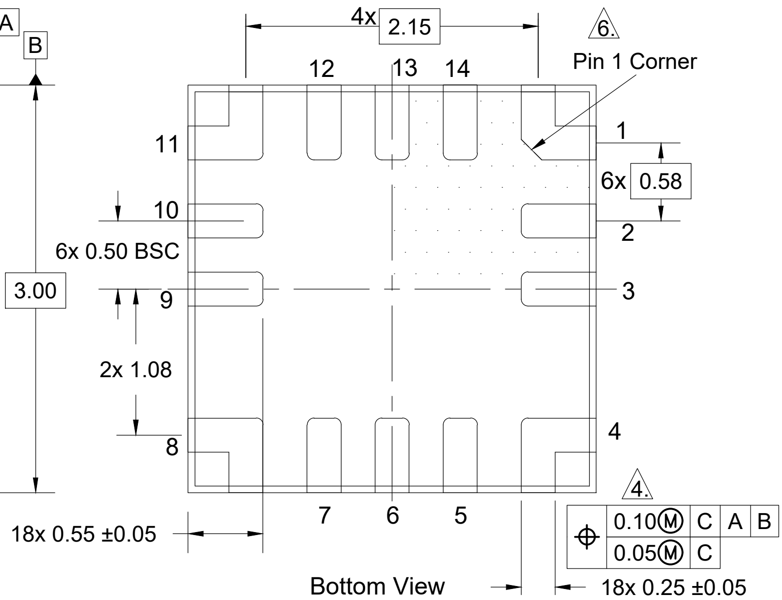
Follow the POD drawing for footprint generation of the 14 Lead Step Cut Thin Quad Flat No-Lead Plastic Package.

Package Outline Drawing

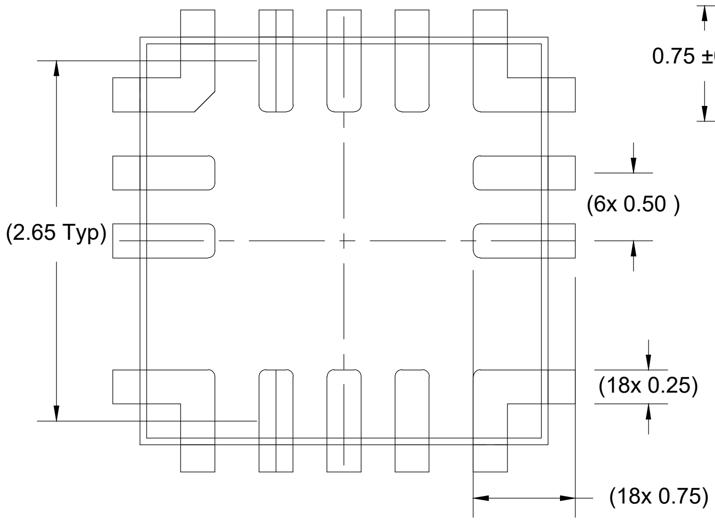
L14.3X3
QW0014AA
14 Lead (SCTQFN) 3.0 x 3.0 x 0.80 mm Body, 0.50 mm Pitch
Rev 02,Nov 25, 2025



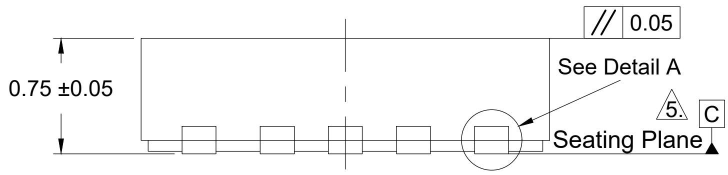
Top View



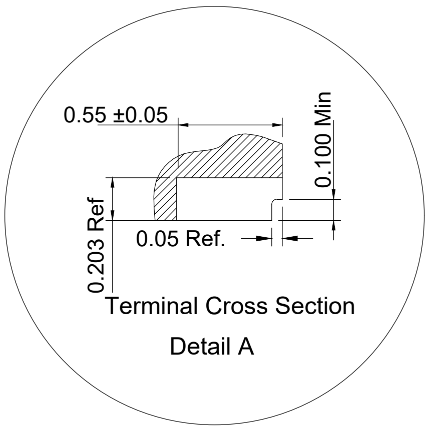
Bottom View



Recommended Land Pattern



Side View



Terminal Cross Section

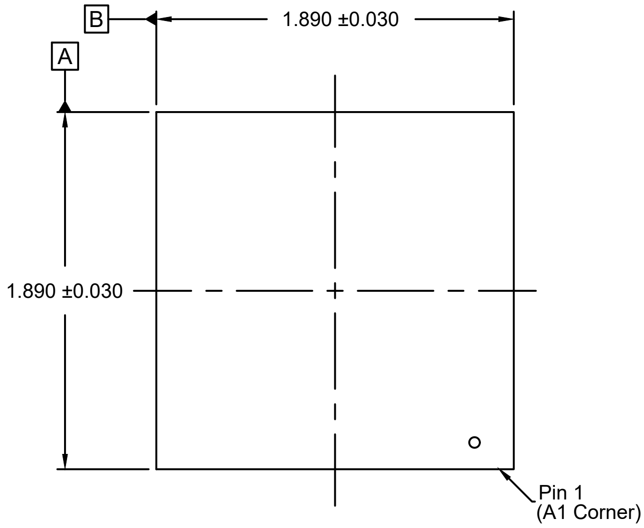
Detail A

Notes:

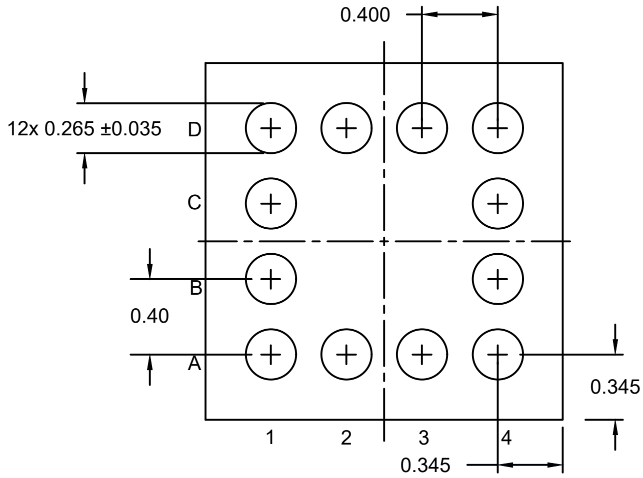
1. Dimensions are in millimeters.
   Dimensions ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05.
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin# 1 Identifier, but must be located within the zone indicated, The pin# 1 Identifier may be either a mold or mark feature.

Package Outline Drawing

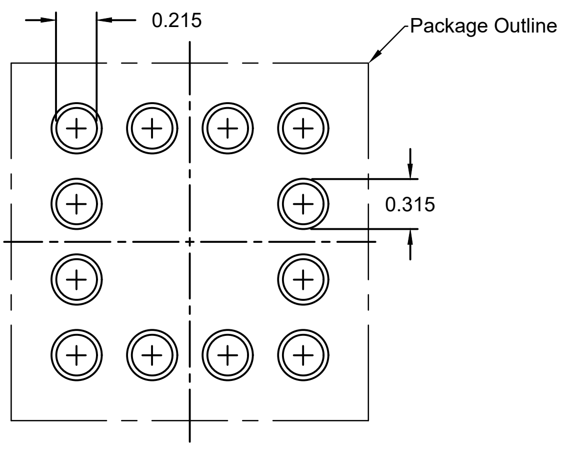
W4x4.12
WA0012AA
12 Ball Wafer Level Chip Scale Package 1.890 x 1.890 x 0.550 mm, 0.40 mm Pitch
Rev 02, Dec 1, 2025



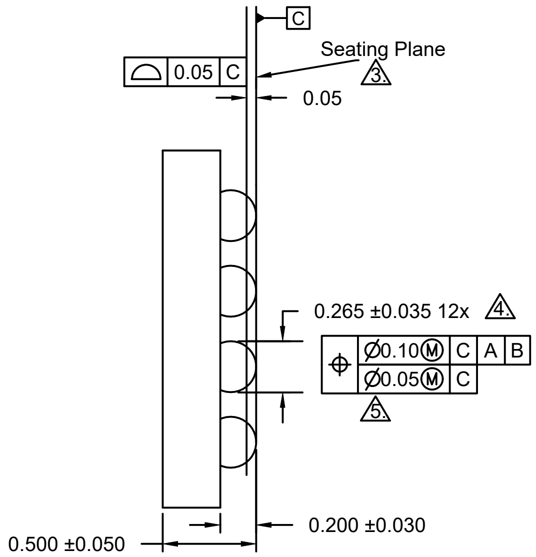
Top View



Bottom View



6 NSMD
Recommended Land Pattern



Side View

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5-1994.
3. Primary datum C and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum C .
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per TB451.

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