RRW21111/RRW21112/RRW21115

PrimAccurate™ AC/DC Controller with Integrated 700V SuperGaN® GaN FET

Description

The RRW2111x is a System-in-Package (SIP) product that integrates a 700V SuperGaN GaN FET with a high-performance digital AC/DC primary-side regulation (PSR) flyback controller. The product offers a unique light load mode that can be configured with an external resistor to allow the design to be optimized for ultra-low no-load power consumption or fast transient response. It operates in quasi-resonant mode to provide high efficiency at heavy loads and minimizes the external component count while simplifying EMI design and lowering the total bill of material cost.

Renesas' PrimAccurate primary-side regulation (PSR) technology allows the RRW2111x to eliminate the need for secondary-side feedback while achieving excellent line and load regulation. This proprietary digital control technology also eliminates the need for loop compensation components while maintaining stability over all operations. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range. Typical power converters use RRW21115 for around 25W, RRW21112 for around 45W and RRW21111 for around 65W applications.

Renesas' innovative proprietary technology ensures that power supplies built with the RRW2111x can achieve both the highest average active efficiency and less than 75mW no-load power consumption. RRW2111x's soft-start enables fast, yet smooth start-up into large capacitive loads at any output voltage, making it ideal for networking and monitor adaptor applications.

The RRW2111x offers a full range of fault protection circuits including internal and external over-voltage protection (OVP). The external OVP feature offers a supplemental output OVP.

Features

- System-in-Package (SIP) with integrated PSR flyback controller and 700V GaN with various $R_{DS(ON)}$ for RRW21111 (150mΩ), RRW21112 (240mΩ) and RRW21115 (480mΩ)
- External supplemental output over-voltage protection
- Adaptively controlled soft-start enables fast and smooth start-up into large capacitive loads (from 330µF to 6,000µF) at 9V+ output voltages
- Internal single-point fault protections against output short-circuit, output over-voltage and output over-current
- User-configurable light-load operation mode for optimized dynamic load response and no-load power consumption
- < 75mW no-load power consumption at $230V_{AC}$ with fast dynamic load response in typical 24W power supply
- PrimAccurate Primary-side feedback eliminates optocouplers and simplifies design
- Proprietary optimized 79kHz maximum PWM switching frequency with quasi-resonant operation achieves best size, efficiency and common mode noise
- EZ-EMI™ design enhances manufacturability
- Adaptive multi-mode PWM/PFM control improves efficiency
- User-configurable 5-level cable drop compensation provides design flexibility
- Tight constant-voltage and optional constant current regulation across line and load range
- SmartDefender™ smart hiccup technology helps to address issues of soft shorts in cables and connectors by effectively reducing the average output power at fault conditions without latch
- Optional on-chip internal over-temperature protection
- No audible noise over entire operating range
- QFN8x8 package

Applications

- Power adapters for network devices and monitors
- Universal AC/DC adapters (up to 65W)
- Auxiliary power

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1. Overview

1.1 Typical Application

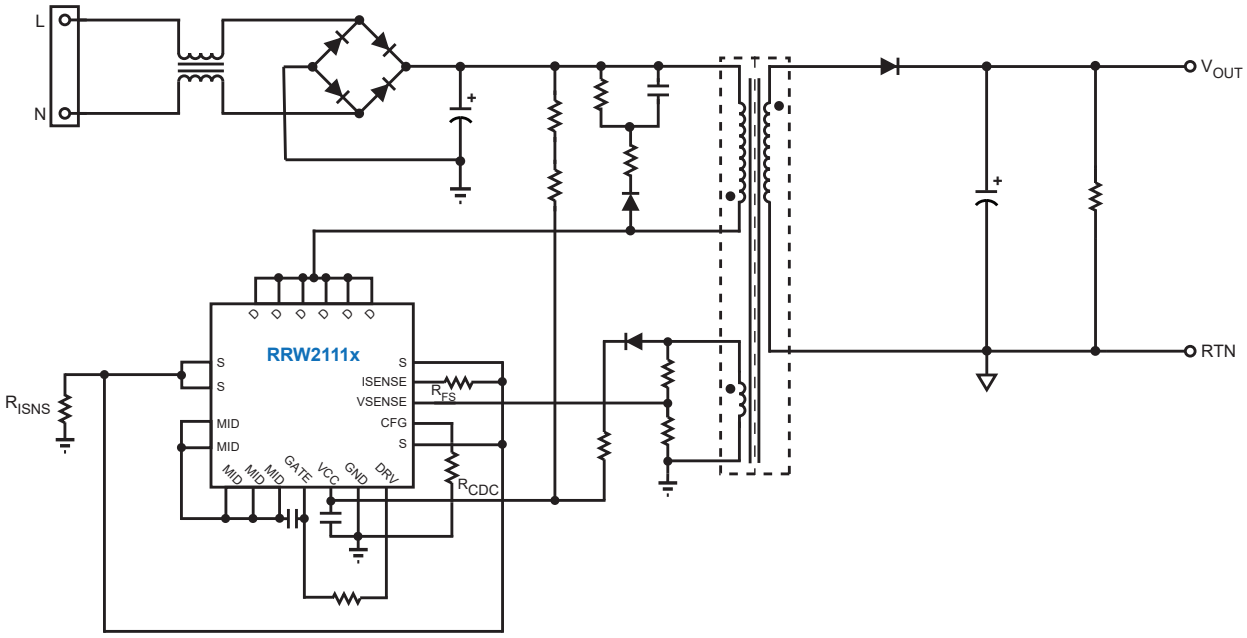

Figure 1 : RRW2111x Typical Application Circuit

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2. Pin Information

2.1 Pin Assignments

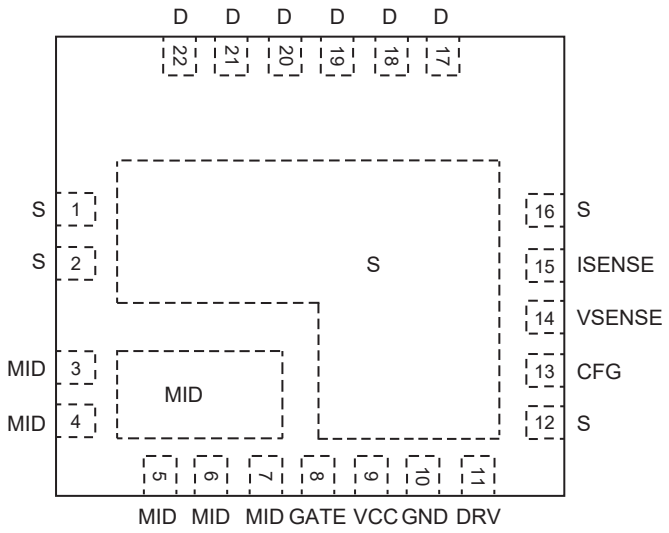

Figure 2 : QFN8x8 Package. Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Pin Description
1, 2, 12, 16	S	Analog input	Internal SiFET Source / GaN HEMT Gate.
3, 4, 5, 6, 7	MID	Analog input	Internal SiFET Drain / GaN HEMT Source.
8	GATE	Analog input	Internal SiFET Gate. Connect to DRV pin for proper operation.
9	VCC	Power	IC power supply.
10	GND	Ground	Ground.
11	DRV	Analog output	Gate drive for SuperGaN® GaN FET.
13	CFG	Analog input	Used for external cable drop compensation (CDC) configuration and supplemental over-voltage protection (OVP).
14	VSENSE	Analog input	Voltage sensing. Used for adapter output voltage sensing and valley mode switching.
15	ISENSE	Analog input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/ CC regulation.
17, 18, 19, 20, 21, 22	D	Analog input	Internal GaN HEMT Drain.

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3. Specifications

3.1 Absolute Maximum Ratings

T_C = 25°C unless otherwise stated

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Value	Units
V_{CC}	DC supply voltage range (pin 9, I_{CC} = 20mA max)	-0.3 to 25.0	V
I_{CC}	Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	20	mA
	DRV (pin 11)	-0.3 (-1.5 for < 100ns) to 20.0	V
	V_{SENSE} input (pin 14, I_{VSENSE} ≤ 10mA)	-0.7 to 4.0	V
	ISENSE (pin 15)	-0.3 (-1.5 for < 300ns) to 4.0	V
	CFG (pin 13, I_{CFG} ≤ 20mA)	-0.8 to 4.0	V
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	700	V
$V_{DSS(TR)\ ,\ non\text{-}repetitive}$	Transient drain to source voltage, non-repetitive (1)	800	V
$V_{DSS(TR)\ ,\ repetitive}$	Transient drain to source voltage, repetitive (2)	750	V
V_{GSS}	Gate to source voltage	±20	V
I_D(RRW21111)	Continuous drain current at T_C=25°C (3)	16	A
	Continuous drain current at T_C=100°C (3)	8.4	A
I_D(RRW21112)	Continuous drain current at T_C=25°C (3)	6.5	A
	Continuous drain current at T_C=100°C (3)	4.1	A
I_D(RRW21115)	Continuous drain current at T_C=25°C (3)	3.6	A
Symbol	**Parameter**	**Value**	**Units**
I_D(RRW21115)	Continuous drain current @T_C=100°C (3)	2.3	A
T_{JMAX}	Maximum junction temperature	150	°C
T_{JOPT}	Operating junction temperature	-40 to 150	°C
T_{STG}	Storage temperature	-65 to 150	°C
	ESD rating per JEDEC JS-001-2017(between pin pairs from controller or from power devices)	±2,000	V
	Latch-up test per JESD78E	±100	mA

Notes:

1. In off-state, spike duty cycle D<0.01, spike duration <30µs.
2. off-state, spike duration <5µs
3. For increased stability at high current operation

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3.2 Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Resistance Junction-to-Ambient	θ_{JA}	TBD	°C/W
Thermal Resistance Junction-to-Drain pin (pin 5 and pin 6)	ψ_{JB}	TBD	°C/W

3.3 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSENSE SECTION						
Input leakage current	I_{BVS}	V_{SENSE} = 2V	-	-	1	μA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A = 25°C, negative edge	1.521	1.536	1.551	V
V_{SENSE}-based output OVP threshold with no CDC compensation (Note 1)	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge	1.742	1.838	1.926	V
ISENSE SECTION						
Over-current threshold	V_{OCP}		1.11	1.15	1.19	V
ISENSE regulation upper limit (Note 2)	$V_{IPK(HIGH)}$		-	1.00	-	V
ISENSE regulation lower limit (Note 2) (Note 3)	$V_{IPK(LOW\_kHz)}$	R_{FS} < 0.65k or R_{FS} > 1.95k	-	0.23	-	V
ISENSE regulation lower limit (Note 2) (Note 3)	$V_{IPK(LOW\_Hz)}$	1.05k < R_{FS} < 1.35k	-	0.28	-	V
Input leakage current	I_{LK}	ISENSE = 1.0V	-	-	1	μA
CFG SECTION						
OVP shutdown threshold (rising edge)	$V_{SD-TH(R)}$		1.75	1.8	1.85	V
OVP recovery hysteresis	$V_{SD-HYS(R)}$		3	12	24	mV
DRV SECTION						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$	I_{SINK} = 5mA	5	9.6	15	Ω
Driver pull-up ON-resistance	$R_{DS(ON)PU}$	I_{SOURCE} = 5mA	65	75	90	Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330pF 10% to 90%	-	95	-	ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330pF 90% to 10%	-	14	-	ns
Maximum switching frequency (Note 2)(Note 4)	f_{SW_MAX}	> 50% load	-	79	-	kHz
Minimum switching frequency (Note 2)(Note 3)	f_{SW_MIN}	1.05k < R_{FS} < 1.35k	-	0.14	-	kHz
VCC SECTION						
Recommended operating voltage range (Note 2)	V_{CC}		-	-	18	V
Pre-start-up threshold	$V_{CC(PRE\_ST)}$	V_{CC} rising	11	12	14.5	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	12.7	13.7	14.7	V
Under-voltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	6.1	6.4	6.7	V
Latch release threshold	$V_{CC(RLS)}$	V_{CC} falling	3.8	4.5	5	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} over-voltage protection level	$V_{CC(OVP)}$	V_{CC} rising	21	23	24	V
Start-up current (Note 2)	$I_{IN(ST)}$	V_{CC} = 8V	-	1	-	μA
Start-up current level 2	$I_{IN(ST2)}$	$V_{CC(PRE\_ST)} < V_{CC} < V_{CC(ST)}$	-	10	12.5	μA
Quiescent current	I_{CCQ}	100pF at DRV, V_{SENSE} = 1.4V	1.8	2.6	3.3	mA
Quiescent current, low power mode, Adapter	$I_{CC\_NL\_AD}$		0.1	0.22	0.35	mA
GaN DEVICE SECTION (RRW21111)						
Maximum drain-source voltage	$V_{DSS(BL)}$	V_{GS}=0V	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.5	2.0	2.5	V
Drain-source on-resistance (Note 5)	$R_{DS(on)eff}$	V_{GS}=10V, I_D=8.5A, T_J=25°C	-	150	180	mΩ
		V_{GS}=10V, I_D=8.5A, T_J=150°C	-	307	-	
Drain-to-source leakage current	I_{DSS}	V_{DS}=700V, V_{GS}=0V, T_J=25°C	-	2.5	25	μA
		V_{DS}=700V, V_{GS}=0V, T_J=150°C	-	10	-	
Gate-to-source forward leakage current	I_{GSS}	V_{GS}=20V	-	-	10	μA
Gate-to-source reverse leakage current		V_{GS}=-20V	-	-	-10	
Input capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=400V, *f*=1MHz	-	598	-	pF
Output capacitance	C_{OSS}		-	30	-	
Reverse transfer capacitance	C_{RSS}		-	1	-	
Output capacitance, energy related (Note 6)	$C_{O(er)}$	V_{GS}=0V, V_{DS}=0V to 400V	-	37.3	-	pF
Output capacitance, time related (Note 7)	$C_{O(tr)}$		-	67	-	
Total gate charge	Q_G	V_{DS}=400V, V_{GS}=0V to 10V, I_D=4A	-	5.5	-	nC
Gate-source charge	Q_{GS}		-	2	-	
Gate-drain charge	Q_{GD}		-	2.4	-	
Output charge	Q_{OSS}	V_{GS}=0V, V_{DS}=0V to 400V	-	27	-	nC
GaN DEVICE SECTION (RRW21112)						
Maximum drain-source voltage	$V_{DSS(BL)}$	V_{GS}=0V	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.5	2.0	2.5	V
Drain-source on-resistance (Note 5)	$R_{DS(on)eff}$	V_{GS}=10V, I_D=8.5A, T_J=25°C	-	240	312	mΩ
		V_{GS}=10V, I_D=8.5A, T_J=150°C	-	492	-	
Drain-to-source leakage current	I_{DSS}	V_{DS}=700V, V_{GS}=0V, T_J=25°C	-	1.2	12	μA
		V_{DS}=700V, V_{GS}=0V, T_J=150°C	-	8	-	
Gate-to-source forward leakage current	I_{GSS}	V_{GS}=20V	-	-	10	μA
Gate-to-source reverse leakage current		V_{GS}=-20V	-	-	-10	
Input capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=400V, *f*=1MHz	-	487	-	pF
Output capacitance	C_{OSS}		-	16.3	-	
Reverse transfer capacitance	C_{RSS}		-	2	-	
Output capacitance, energy related (Note 6)	$C_{O(er)}$	V_{GS}=0V, V_{DS}=0V to 400V	-	24	-	pF
Output capacitance, time related (Note 7)	$C_{O(tr)}$		-	42	-	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total gate charge	Q_G	V_{DS}=400V, V_{GS}=0V to 10V, I_D=4A	-	5.4	-	nC
Gate-source charge	Q_{GS}		-	2	-	
Gate-drain charge	Q_{GD}		-	2.3	-	
Output charge	Q_{OSS}	V_{GS}=0V, V_{DS}=0V to 400V	-	17	-	nC
GaN DEVICE SECTION (RRW21115)						
Maximum drain-source voltage	$V_{DSS(BL)}$	V_{GS}=0V	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.5	2.0	2.5	V
Drain-source on-resistance (Note 5)	$R_{DS(on)eff}$	V_{GS}=10V, I_D=8.5A, T_J=25°C	-	480	560	mΩ
		V_{GS}=10V, I_D=8.5A, T_J=150°C	-	1000	-	
Drain-to-source leakage current	I_{DSS}	V_{DS}=700V, V_{GS}=0V, T_J=25°C	-	1	10	µA
		V_{DS}=700V, V_{GS}=0V, T_J=150°C	-	5	-	
Gate-to-source forward leakage current	I_{GSS}	V_{GS}=20V	-	-	10	µA
Gate-to-source reverse leakage current		V_{GS}=-20V	-	-	-10	
Input capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=400V, *f*=1MHz	-	465	-	pF
Output capacitance	C_{OSS}		-	8	-	
Reverse transfer capacitance	C_{RSS}		-	1.2	-	
Output capacitance, energy related (Note 6)	$C_{O(er)}$	V_{GS}=0V, V_{DS}=0V to 400V	-	11.6	-	pF
Output capacitance, time related (Note 7)	$C_{O(tr)}$		-	23	-	
Total gate charge	Q_G	V_{DS}=400V, V_{GS}=0V to 10V, I_D=4A	-	10	-	nC
Gate-source charge	Q_{GS}		-	2	-	
Gate-drain charge	Q_{GD}		-	2	-	
Output charge	Q_{OSS}	V_{GS}=0V, V_{DS}=0V to 400V	-	9.2	-	nC
THERMAL CHARACTERISTICS						
Thermal shutdown threshold (Note 2)	T_{SD}		-	140	-	°C
Thermal shutdown hysteresis (Note 2)	T_{SD_HYS}		-	20	-	°C
Thermal shutdown recovery (Note 2)	T_{SD_R}		-	120	-	°C
V_{AUX} Open Protection						
V_{AUX} open detection threshold	V_{AUX_OPEN}		20	40	70	mV

Notes:

1. The V_{SENSE}-based output OVP threshold depends on the CDC setup, see Section 6.13 for more details.
2. These parameters are not 100% tested. They are guaranteed by design and characterization.
3. The minimum switching frequency and the ISENSE regulation lower limit are user-configurable by the resistor connected to the ISENSE pin. Refer to Section 6.6 for details.
4. Operating frequency varies based on the load conditions, see Section 6.6 for more details.
5. Dynamic $R_{DS(on)}$, 100% tested
6. Equivalent capacitance to give same stored energy from 0V to 400V
7. Equivalent capacitance to give same charging time from 0V to 400V

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4. Typical Performance Graphs

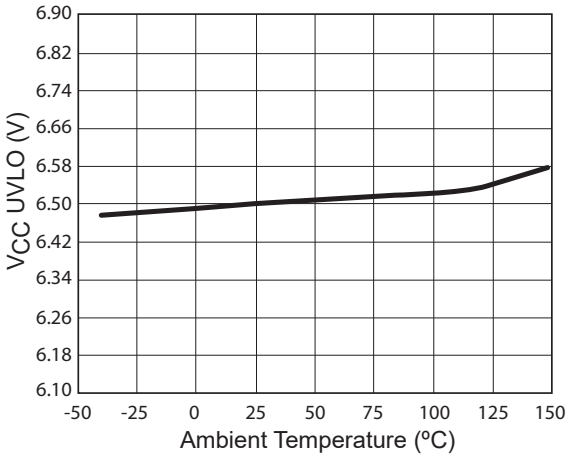

Figure 3 : V_{CC} UVLO vs. Temperature

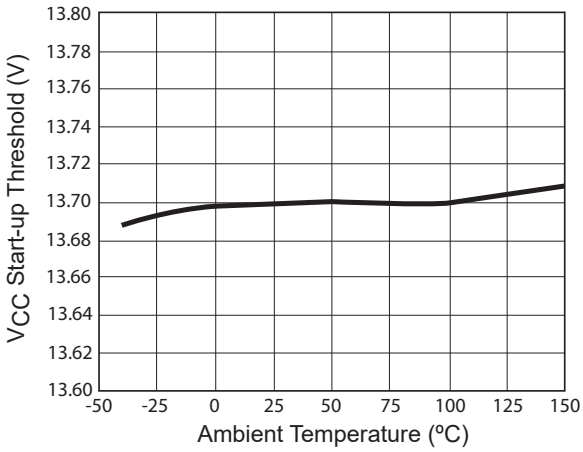

Figure 4 : Start-up Threshold vs. Temperature

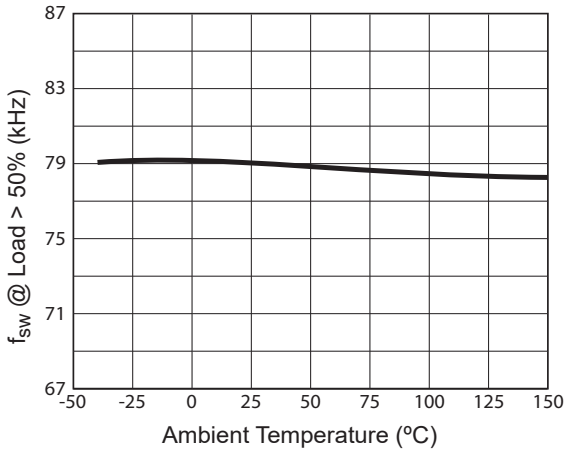

Figure 5 : Switching Frequency vs. Temperature[1]

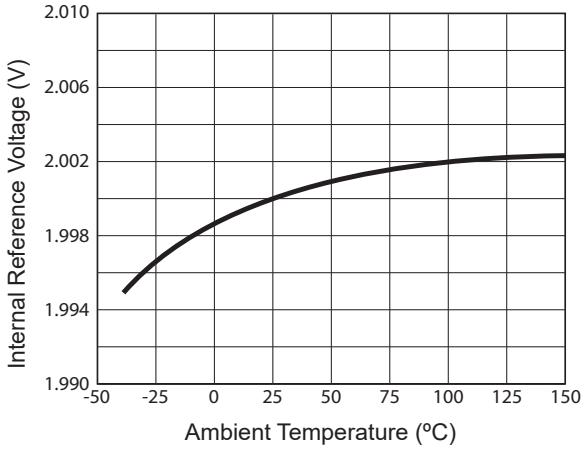

Figure 6 : Internal Reference vs. Temperature

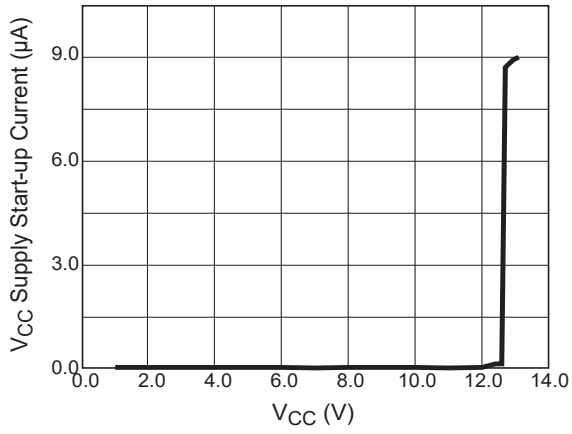

Figure 7 : V_{CC} Supply Start-up Current vs. V_{CC}

Note: Operating frequency varies based on the load conditions, see Section 6.6 for more details.

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5. Functional Block Diagram

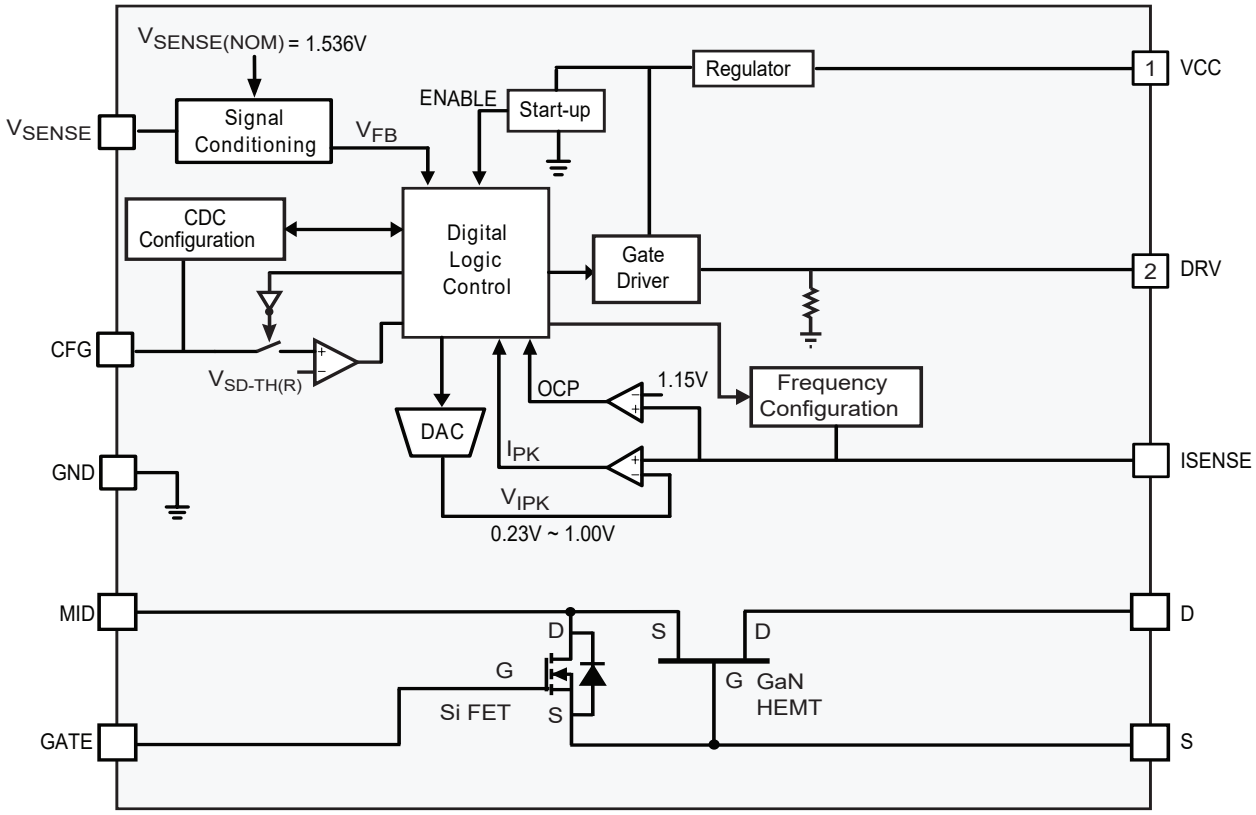

Figure 8 : RRW2111x Functional Block Diagram

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6. Theory of Operation

The RRW2111x is a system-in-package (SIP) product with integrated PSR flyback controller and 700V GaN with various $R_{DS(ON)}$ for RRW21111(150mΩ), RRW21112(240mΩ) and RRW21115(480mΩ). The digital controller uses a proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Renesas' digital control technology enables fast dynamic response, tight output regulation, and full-featured circuit protection with primary-side control.

The block diagram in Figure 8 illustrates the RRW2111x operating in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the internal GaN FET. The ISENSE is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the ISENSE to compare with, and it varies in the range of 0.23V (typical) to 1.00V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The RRW2111x uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant current operation is achieved without the need for any secondary-side sense and control circuits.

The RRW2111x uses adaptive multi-mode PWM/PFM control to dynamically change the switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), and ISENSE fault detection. When the no-load switching frequency is configured at 1.8kHz, the RRW2111x can achieve 75mW no-load power consumption with fast dynamic load response.

Renesas' digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as minimum cost, smallest size, and high performance output control.

6.1 Pin Details

Pin 9 – VCC

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 13.7V (typical), and shuts down when the V_{CC} voltage drops below 6.5V (typical). A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.

Pin 11 – DRV

Gate drive for SuperGaN GaN FET.

Pin 15 – ISENSE

Primary current sense and minimum switching frequency setting. Used for cycle-by-cycle peak current control and limit. It is also used to configure the minimum switching frequency at the beginning of start-up.

Pin 8 – Gate

Internal SiFET Gate. Connect to DRV pin for proper operation.

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Pin 17, 18, 19, 20, 21, 22 – D

Internal GaN HEMT Drain.

Pin 1, 2, 12, 16 – S

Internal SiFET Source / GaN HEMT Gate.

Pin 10 – GND

Ground.

Pin 14 – VSENSE

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 13 – CFG

Configure external cable drop compensation (CDC) at the beginning of start-up and provide output over-voltage protection during normal operation by sensing output voltage via the auxiliary winding.

Pin 3, 4, 5, 6, 7 – MID

Internal SiFET Drain / GaN HEMT Source.

6.2 Start-Up and Soft-Start

Prior to start-up, the ENABLE signal is low, as shown in Figure 9. The voltage on the input high voltage capacitor provides start-up current to charge the V_{CC} bypass capacitor. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and the RRW2111x begins to perform the initial OTP check (see Section 6.14), followed by auxiliary winding open detection, CDC configuration (see Section 6.12) and LOM configuration (see Section 6.6). Afterwards, the RRW2111x commences the soft-start function. During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator. If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, the RRW2111x goes to shutdown. At this time the ENABLE signal becomes low and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

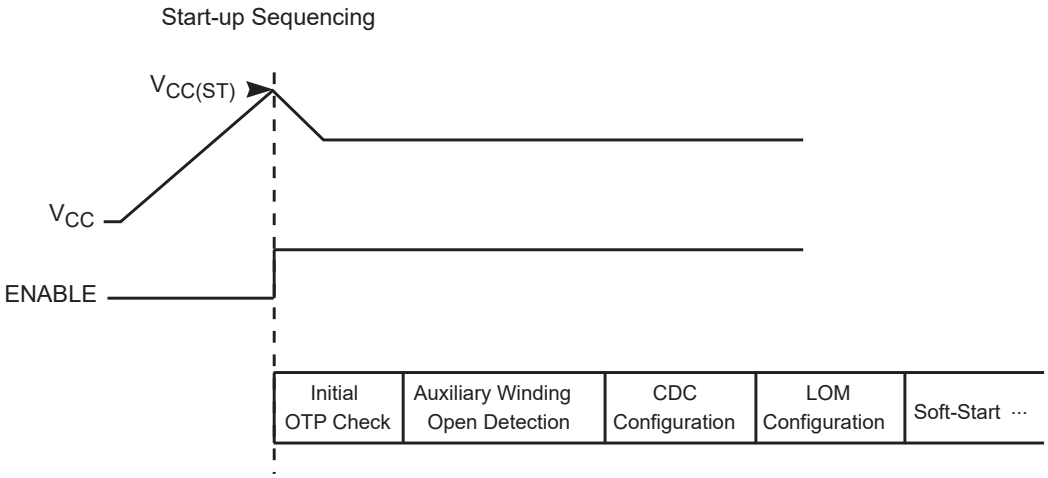

Figure 9 : Start-up Sequencing Diagram

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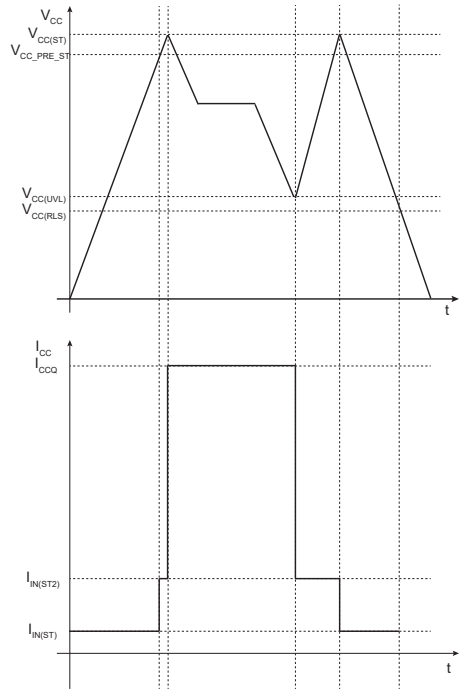

Figure 10 : Start-up Current

Figure 10 shows the I_{CC} current levels at different states. Before the start-up, the voltage at V_{CC} is zero. When input voltage is applied, it provides start-up current to charge the V_{CC} bypass capacitor. The current during this start-up state, noted as $I_{IN(ST)}$ in Figure 10, is as low as 1uA. As soon as the voltage at V_{CC} reaches $V_{CC(PRE\_ST)}$, the current at V_{CC} increases to $I_{IN(ST2)}$. When the V_{CC} reaches the start-up threshold $V_{CC(ST)}$, the operation current of RRW2111x becomes I_{CCQ}. The operation current varies with the system load and may drops to as low as 0.22mA if the system operates at low power mode.

During shut-down, the V_{CC} voltage drops. When V_{CC} reaches the under-voltage lockout threshold $V_{CC(UVL)}$, the current at V_{CC} drops to the level of $I_{IN(ST2)}$. If the V_{CC} continues to drop below the latch release threshold $V_{CC(RLS)}$, the current at V_{CC} further reduces to $I_{IN(ST)}$.

6.3 Understanding Primary Feedback

Figure 11 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reversely-biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

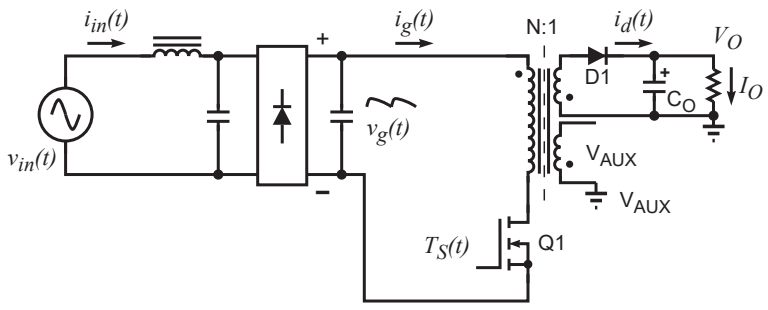

Figure 11 : Simplified Flyback Converter

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In order to tightly regulate the output voltage, the information about the output voltage and load current must be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (6.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (6.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (6.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (6.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave, the auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (6.5)$$

and reflects the output voltage as shown in Figure 12.

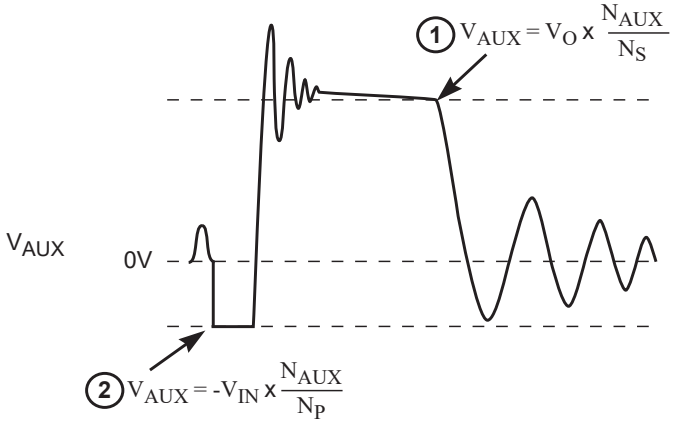

Figure 12 : Auxiliary Voltage Waveforms

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small.

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The real-time waveform analyzer in the RRW2111x reads this information cycle by cycle. The device then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

6.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (t_{ON}) and off time (t_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the RRW2111x shuts down.

6.5 Output Current Limit and Over Current Protection

In overload condition, the RRW2111x enters constant current (CC) mode to limit the output current on a cycle-by-cycle basis. In this mode of operation the output current is limited to a constant level regardless of the output voltage, while avoiding continuous conduction mode operation. In case of very heavy loading when it stays in CC mode for more than 60ms, the RRW2111x detects output over current and shuts down.

The RRW2111x senses the load current indirectly through the primary current, which is detected by the pin ISENSE through a resistor from the S pin to ground.

6.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching, and User-Configurable Light-Load Modes (LOM)

The RRW2111x uses a proprietary adaptive multi-mode PWM/PFM control to dramatically improve the light-load efficiency and the overall average efficiency. The operating mode changes as the load decreases in order to maximize efficiency. Figure 13 shows how the switching frequency and the V_{IPK} vary with the load. During constant voltage (CV) mode operation under heavy load, the RRW2111x operates in pulse-width-modulation (PWM) mode. In PWM mode, the switching frequency remains approximately constant. As the output load decreases, the on-time (t_{ON}) decreases, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. In PFM mode, the GaN FET is turned on for a set duration under a given instantly-rectified AC input voltage, but its off-time is modulated by the load current, decreasing the switching frequency.

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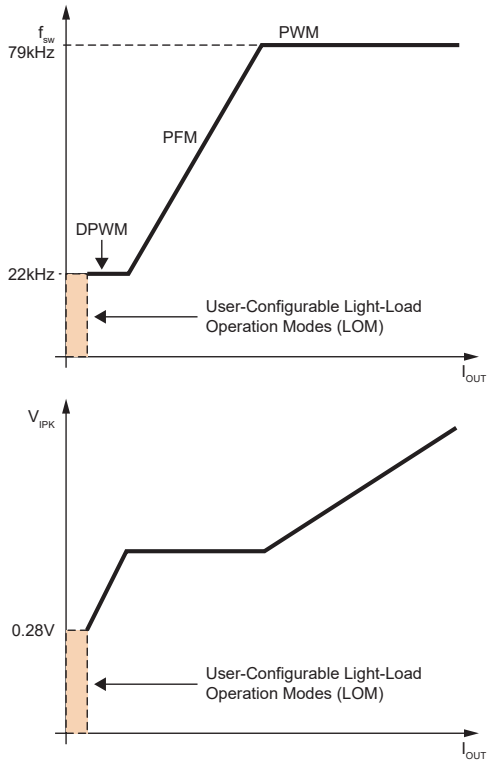

Figure 13 : Multi-Mode PWM/PFM in RRW2111x at Mid-High Loads

When the switching frequency approaches the human ear audio band, the RRW2111x transitions to a second level of PWM mode, namely the Deep PWM mode (DPWM). In the DPWM mode, the switching frequency stays approximately 22kHz in order to avoid audible noise. As the load current continues to decrease, the RRW2111x transitions to Deep PFM mode (DPFM), which reduces the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level and therefore, the power converter practically produces no audible noise.

The RRW2111x allows the user to configure the operation mode of the system at light/no load according to the system requirements in order to minimize the overall system cost. This light-load operation mode (LOM) configuration is only performed once during start-up. It is completed after the CDC configuration but before soft-start commences. During the LOM configuration, the internal digital control block senses the total external resistance value between the ISENSE pin and ground, and then sets a corresponding LOM. Figure 1 shows a simple circuit to set the LOM by connecting a resistor, R_{FS}, directly to the ISENSE pin. The R_{FS} resistor combined with the R_{ISNS} value creates the total resistance used to program the LOM. Figures 14 and 15 show how the switching frequency and V_{IPK} vary with load in different LOM settings.

Table 6.1 shows the resistance range for each of the four LOM settings. In practice, it is recommended to select resistance values in the middle of the range wherever possible. Resistor variation should be taken into consideration to ensure the correct setting.

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LOM #	R_{FS}+ R_{ISNS} Range (kΩ)		DDPWM Mode Switching Frequency (f_{sw_DDPWM}) (kHz)	Minimum Switching Frequency (f_{SW_MIN}) (kHz)	Secondary-Side Active Voltage Positioning Support	Primary Peak Current Regulation Voltage (V_{IPK}) at DPFM (V)
	Min	Max				
1	0	0.65	1.8	1.62	No	0.23
2	1.05	1.35	No DDPWM mode	0.14	Yes	0.28
3	1.95	2.86	2.7	2.43	No	0.23
4	3.7	6	4	3.6	No	0.23

Table 6.1: Recommended Resistance Range for Different Light-Load Operating Modes (LOM) and Their Corresponding Primary Peak Current Regulation Voltage

If the design requires very low no-load power consumption (< 50mW), LOM #2 should be chosen for 140Hz minimum switching frequency operation (Figure 14). In this LOM setting, the switching frequency in DPFM continues to drop as the load current reduces until the switching frequency reaches 140Hz. The primary peak current regulation voltage (V_{IPK}) in DPFM mode is set at 0.28V. The primary switch turns off when the voltage on the ISENSE pin reaches this level.

If the application can tolerate higher no-load power consumption (75mW or above), the device can be configured in LOM #1, 3 or 4 (Figure 15) to maintain relatively high no-load switching frequency for fast dynamic load response. In these modes, the primary peak current regulation voltage in the DPFM mode is set at 0.23V (Figure 15). As the load current reduces to very light load or no-load condition, the RRW2111x transitions from the DPFM to the third level of PWM mode, namely Deep-Deep PWM mode (DDPWM), in which the switching frequency is fixed at 1.8kHz, 2.7kHz, or 4kHz depending on the resistance set at the ISENSE pin. The primary on-time is reduced in DDPWM to reduce the energy delivered to the secondary side.

As the load further decreases, the primary on-time is reduced to minimum in DDPWM mode. The RRW2111x transitions to a third level of PFM mode, namely the Deep-Deep PFM Mode (DDPFM). In this mode, the switching frequency decreases as the load decrease. The minimum switching frequency is clamped at 90% of the DDPWM mode switching frequency.

The typical no-load operation point of the system is recommended to be in the middle of the DDPWM mode, as shown in Figure 15. The DDPFM mode is designed to provide additional margin of output voltage regulation at no load considering the variation of the system parameters.

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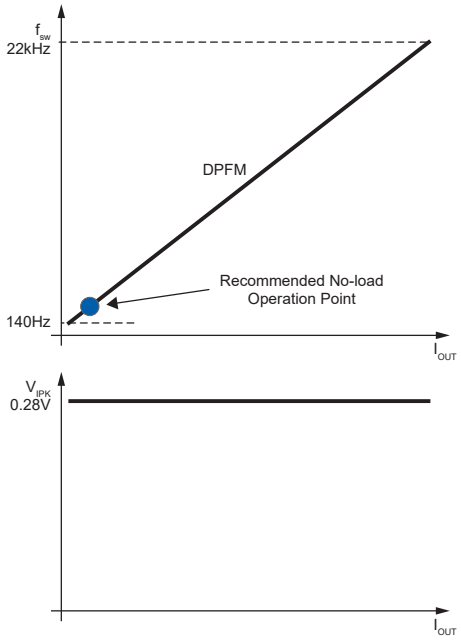

Figure 14 : Light-Load Operation Mode (LOM) #2

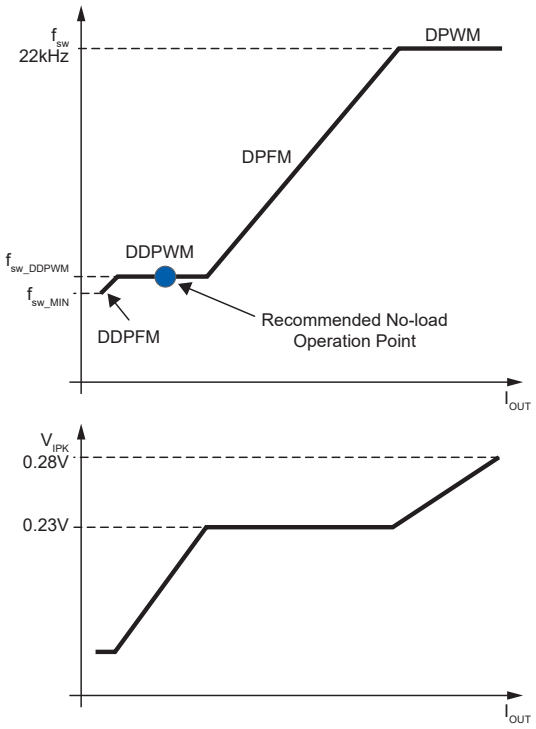

Figure 15 : Light-Load Operation Mode (LOM) #1, 3, or 4

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6.7 Less Than 75mW No-Load Power and Fast Load Transient Response

The RRW2111x features a distinctive DDPWM control in no-load conditions to help achieve low no-load power consumption and fast dynamic load response. With a 1.8kHz f_{SW_DDPWM}, the system no-load power can be less than 75mW for a typical 12V, 2A 24W application. The power supply system designs including the pre-load resistor selection should ensure the power supply can operate in the DDPWM mode under steady-state no-load condition. If the pre-load resistor is too small, the no-load power consumption increases; on the other hand, if it is too large, the output voltage may increase and even cause over-voltage since the switching frequency is fixed at a minimum 1.62kHz level.

While achieving ultra-low no-load power consumption, the RRW2111x implements innovative proprietary digital control technology to intelligently detect any load transient events, and achieve fast dynamic load response for both one-time and repetitive load transients.

The most stringent dynamic load transient requirement is the no-load to load transient. The output voltage drop (cable-drop not included) ΔV_{OUT} is a function of the no-load switching frequency (f_{sw_DDPWM}), output capacitance (C_{OUT}) and the load applied (I_{OUT_STEP}), as shown in Equation 6.6.

$$\Delta V_{OUT} = \frac{I_{OUT\_STEP}}{f_{SW\_DDPWM} \times C_{OUT}} + 0.1V \qquad (6.6)$$

If the system requirement specifies the maximum output voltage drop (ΔV_{OUT_MAX}) from the nominal output voltage (V_{OUT_NOM}) during no-load to I_{OUT_STEP} load change, the minimum output capacitance (C_{OUT_MIN}) required to meet the specification can be calculated with Equation 6.7.

$$C_{OUT\_MIN} = \frac{I_{OUT\_STEP}}{f_{SW\_DDPWM} \times (\Delta V_{OUT\_MAX} + 0.1V)} \qquad (6.7)$$

6.8 Variable Frequency Operation Mode

In each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time is extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110µs. When the transformer reset time reaches 110µs, the RRW2111x shuts off.

6.9 Internal Loop Compensation

The RRW2111x incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

6.10 Voltage Protection Features

The secondary maximum output DC voltage is limited by the RRW2111x. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 12, the RRW2111x shuts down.

The RRW2111x uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of the DC bulk capacitor voltage. This enables the RRW2111x to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in and unplug, and to take appropriate actions. When the AC input voltage drops to below normal operation range and the power supply input is still connected to the AC source, the RRW2111x initiates brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the RRW2111x continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply.

Also, the RRW2111x monitors the voltage on the V_{CC} pin, and the IC shuts down immediately when the voltage on this pin is below the UVLO threshold. The RRW2111x also has a V_{CC} over-voltage protection (V_{CC} OVP). During an abnormal event, if the V_{CC} voltage is higher than the protection threshold, the switching is stopped and the RRW2111x shuts down.

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When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed. For the latched OVP version, the controller can only start up when the fault is removed and input is unplugged to allow V_{CC} to drop to 2.0V below the UVLO threshold.

6.11 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the RRW2111x. With the ISENSE pin the RRW2111x is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the current sensing resistor (R_{ISNS} in Figure 1) is greater than 1.15V, over-current is detected and the IC immediately turns off the gate driver until the next cycle. The output driver sends out a switching pulse in the following cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the RRW2111x shuts down.

If the current sensing resistor R_{ISNS} is shorted prior to the power supply startup, there is a potential danger that an over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault during startup and the startup process is not pursued if the fault exists. The V_{CC} is discharged since the IC remains biased. Once the V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

6.12 CDC Configuration

The RRW2111x incorporates an innovative approach to allow users to configure cable drop compensation (CDC) externally. This configuration is only performed once at the beginning of start-up. It is completed after the auxiliary winding open detection check but before the LOM configuration. During the CDC configuration, the internal digital control block senses the external resistance value between the CFG pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

Figure 1 shows a simple circuit to set CDC level by connecting a resistor, R_{CDC}, from the CFG pin to ground. The RRW2111x provides five levels of CDC configurations: 0mV, 180mV, 360mV, 720mV, and 1.08V, which refer to 12V nominal output voltage. Table 6.2 below shows the resistance range for each of the five CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The “Cable Comp” specified in Table 6.2 refers to the voltage increment at PCB end from no-load to operating current in the CC mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the nominal output voltage of 12V. For different output voltage, the actual voltage increment needs to be scaled accordingly.

To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply it by the maximum output current.

For each of the CDC levels, the internal V_{SENSE}-based OVP thresholds are different. Table 6.2 also lists the typical OVP thresholds for each CDC level.

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R_{CDC} Range (kΩ)		Cable Comp (mV)	Output OVP Threshold (V)
Min	Max		
1.5	2.20	0	1.838
2.37	3.21	180	1.861
3.40	4.64	360	1.884
4.87	6.65	720	1.930
6.98	10	1080	1.976

Table 6.2: Recommended Resistance Range for Different CDC Levels and the Corresponding V_{SENSE}-Based Output OVP Threshold for 12V Output

6.13 External CFG-Based Supplemental Output OVP

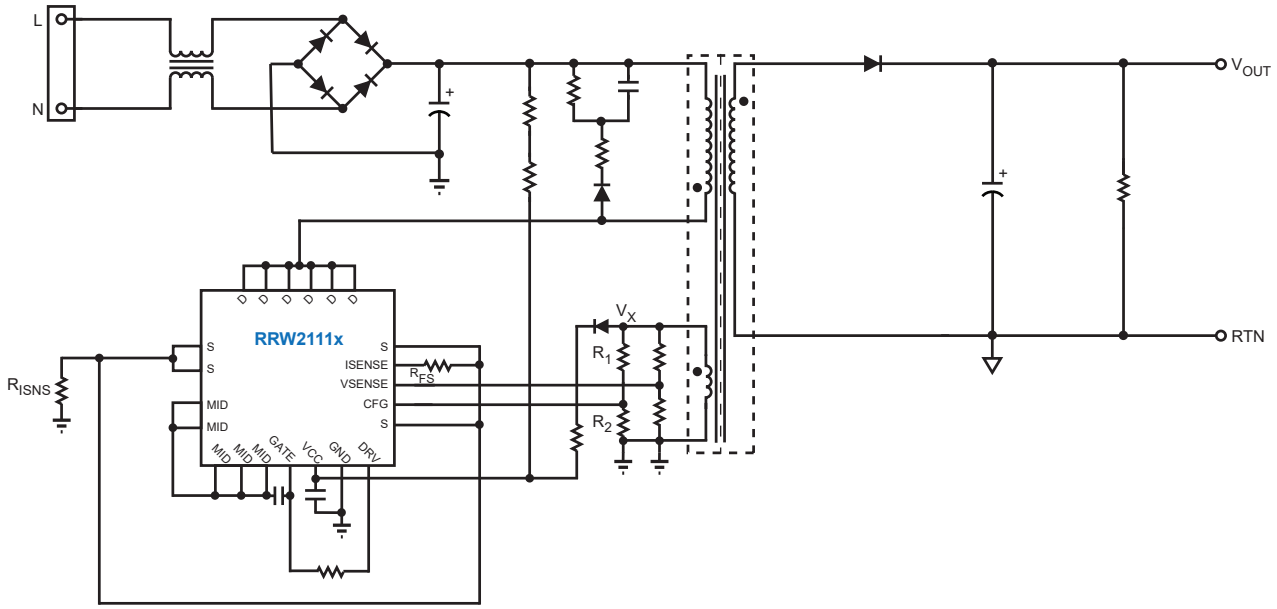

Figure 16 : Typical Application Circuit with CDC and CFG-pin Based Supplemental Output OVP

The CFG pin can be used to provide external over-voltage protection (OVP) as well as external cable drop compensation (CDC) configuration. This external CFG-based OVP serves as a supplemental or extra protection in addition to the V_{SENSE}-based OVP. The circuit implementation can be found in Figure 16, where two resistors R1 and R2 form a voltage divider to sense output voltage via auxiliary winding, with the tapping point connected to the CFG pin. During the CDC configuration the RRW2111x does not send out any drive signal at the DRV pin, and the internal GaN FET remains in the off state. The resistors R1 and R2 are essentially connected in parallel since the auxiliary winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 sets the CDC level. Meanwhile, during normal operation, the CFG pin reflects the output voltage in real-time, in the similar fashion as the V_{SENSE} does at point 1 in Figure 12. The ratio of R1 to R2 sets the external OVP threshold.

The resistance values for the resistor divider, R1 and R2, can be derived as follows.

First, for the given CDC level, the paralleled resistance of R1 and R2 should be within the range listed in Table 6.2:

$$R_{CDC} = \frac{R_1 \times R_2}{R_1 + R_2} \qquad (6.8)$$

Second, during normal operation the voltage divider, R1 and R2, sets the desired OVP threshold:

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$$\left(\frac{N_{AUX}}{N_{SEC}}\right) \times V_{OVP} \times \left(\frac{R_2}{R_2+R_1}\right) >= V_{SD\text{-}TH(R)} \quad (6.9)$$

where N_{AUX} is the number of turns for the auxiliary winding, N_{SEC} is the number of turns for the secondary winding, V_{OVP} is the desired OVP tripping point, and $V_{SD\text{-}TH(R)}$ is the internal comparator threshold (1.8V typically) for OVP detection.

The combination of Equations (6.8) and (6.9) leads to:

$$R_1 = \left(\frac{N_{AUX}}{N_{SEC}}\right) \times R_{CDC} \times \left(\frac{V_{OVP}}{V_{SD\text{-}TH(R)}}\right)$$
$$R_2 = \left(\frac{R_1}{R_1 - R_{CDC}}\right) \times R_{CDC} \quad (6.10)$$

It is recommended the R_{CDC} value is taken as the median value of the resistance range as given in Table 6.2, and R1 and R2 can then be readily derived from Equation (6.10).

6.14 Internal OTP

The RRW2111x features an internal OTP which shuts down the device if the internal die junction temperature reaches above 140°C (typical). The device is kept off until the junction temperature drops below 120°C (typical), when the device initiates a new soft-start process to build up the output voltage.

6.15 Latch and Release (Optional)

The RRW21115-113 has an optional latch and release feature. The output OVP (including V_{SENSE}-based and the external CFG-based OVP) and CC shutdown can be latched. When the latch occurs, the device does not attempt to start again even with the fault cleared. In the latch state, the controller recycles itself by periodically ramping V_{CC} up and down between $V_{CC(ST)}$ and $V_{CC(UVL)}$, and the controller does not start up, provided the input stays connected to the AC source. To get out of the latch state, unplugging the input from the AC source is required, so that the V_{CC} is allowed to drop to 2.0V below $V_{CC(UVL)}$ to release the latch.

6.16 SmartDefender Smart Hiccup Technology

In the traditional AC/DC adapter designs, once the control IC detects a fault and shuts down, there are two common ways to respond to a default:

(a) Shutdown and auto-restart —The switching pulses are sent out in every power-on-reset (POR) cycle after the V_{CC} reaches the startup threshold. In case of the USB cable short or partial short, this can have a high average output current from the USB and high average input power in the adapter, and it may generate excessive heat and cause damages. The auto-restart is commonly called “hiccup”.

(b) Shutdown and latch —This normally requires the user to unplug the adapter from the AC input and recycle the power, which can create an inconvenient or bad experience.

To address this issue, the RRW2111x implements Renesas’ innovative and proprietary SmartDefender smart hiccup protection function. With SmartDefender technology, during the smart hiccup, the power supply only re-starts after a certain number of POR cycles (which means sending the switching pulses after V_{CC} reaches the startup threshold) instead of auto-restart in every POR cycle. In the RRW2111x the SmartDefender function applies to the faults such as the output short and “CC shutdown,” etc. Once these faults are detected, the RRW2111x allows 2 cycles of auto-restart POR, and then blocks the next 6 cycles of auto-restart POR. This is equivalent to a 2/8 duty cycle. This operation mode continues until the faults are removed. In this way the ***SmartDefender*** technology effectively reduces the average output power at the fault conditions without latch.

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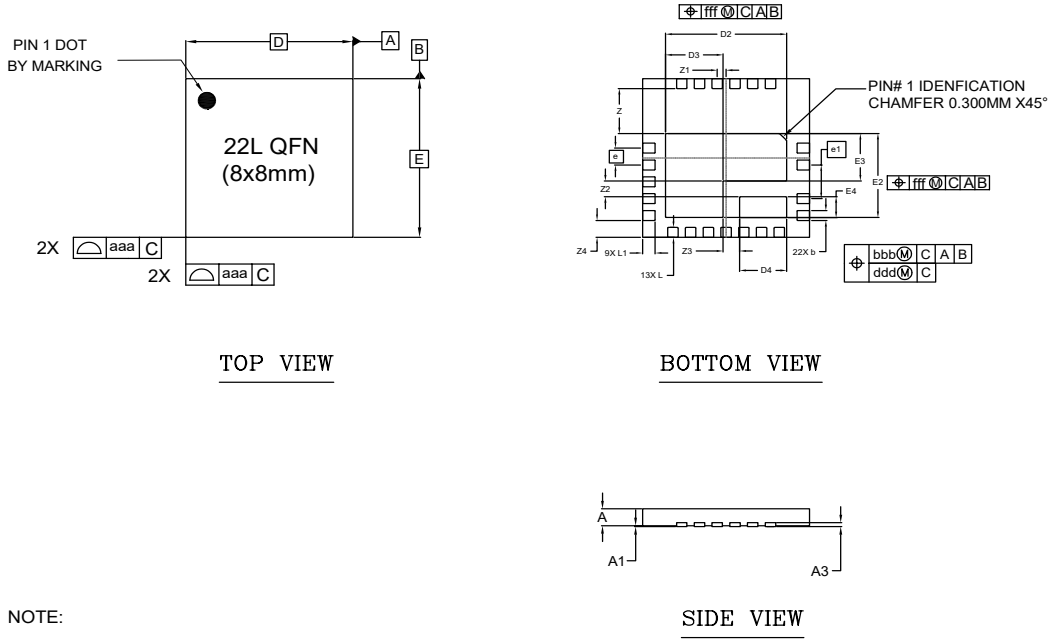
7. Package Outline Drawings



Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
A1	0.000	—	0.050
A3	0.203 REF		
D	8.000 BSC		
E	8.000 BSC		
D2	5.750	5.800	5.850
D3	2.700	2.750	2.800
D4	2.200	2.250	2.300
E2	4.180	4.230	4.280
E3	1.790	1.840	1.890
E4	1.000	1.050	1.100
b	0.450	0.500	0.550
e	0.850 BSC		
e1	1.700 BSC		
L	0.450	0.500	0.550
L1	0.550	0.600	0.650
Z	2.265 REF		
Z1	0.425 REF		
Z2	0.800 REF		
Z3	0.800 REF		
Z4	0.850 REF		
Dimensional Tol.			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

NOTE:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
2. N IS THE TOTAL NUMBER OF TERMINALS

Figure 17 : QFN8x8 package outline drawing

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8. Ordering Information

Part Number	Options[1]			Package	Description
	External CFG Over-Voltage Protection Option	Latch Conditions	CDC		
RRW21111-153	Output	No Latch	Yes	QFN8x8	Tape & Reel[2]
RRW21112-153	Output	No Latch	Yes	QFN8x8	Tape & Reel[2]
RRW21115-153	Output	No Latch	Yes	QFN8x8	Tape & Reel[2]
RRW21115-113	Output	Latch	Yes	QFN8x8	Tape & Reel[2]

Notes:

1. For availability of additional options, please contact Marketing.
2. Tape and reel packing quantity is 4,000/reel. Minimum packing quantity is 4,000.

9. Revision History

Revision	Date	Description
0.01	Mar 11, 2026	• Initial release.

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