

RRW22101/RRW22102/RRW22105

AC/DC Digital SSR Flyback Controller with Integrated SuperGaN® GaN FET

Description

The RRW2210x is a System-in-Package (SIP) product that integrates a 700V SuperGaN GaN FET with a high-performance AC/DC primary-side digital flyback controller for secondary-side regulation (SSR) operating with generic shunt regulator such as TL431 and other third party secondary-side controller for a broad range of end applications. The RRW2210x operates in Renesas' patented constant-frequency, quasi-resonant (QR) switching mode and adaptive multi-mode control (MMC). Typical applications use RRW22105 for 25W to 45W, RRW22102 for 45W to 65W, and RRW22101 for 45W to 65W and above. Such typical power supply designs build with RRW2210x and TL431 can meet no-power consumption of less than 75mW.

The RRW2210x's unique MMC mode of operation includes PWM, PFM and burst mode, which optimizes flyback converter performance including efficiency and EMI. The device also provides a number of key built-in protection features. The RRW2210x and TL431 or other third party secondary-side controller can achieve tight constant voltage (CV) regulation.

Renesas' innovative proprietary technology ensures that power supplies designed with the RRW2210x and generic shunt regulator or other third party secondary-side controller can achieve high efficiency, high accuracy voltage/current control and fast dynamic load response, all with the lowest system cost.

Features

- System-in-Package (SIP) with integrated SSR flyback controller and 700V GaN with various $R_{DS(ON)}$ for RRW22101 (150mΩ), RRW22102 (240mΩ) and RRW22105 (480mΩ)
- JEDEC-qualified GaN technology
- < 75mW standby power consumption (at 230V_{AC} in a typical 25W to 65W and above travel adapter application)
- Supports single-layer PCB design to reduce total system cost
- Supports third-party controllers and TL431-based secondary-side controllers for user defined RapidCharge™ applications and fixed-voltage power supply designs.
- Operates at Renesas' patented switching modes of adaptive multi-mode control (MMC) and continuous conduction mode (CCM) or quasi-resonant (QR) operation.
 - Improves efficiency and eliminate audible noise
 - Enables optimization for size, efficiency and EMI performance
- Supports voltage sensing and IC power supply with dual polarity options of auxiliary winding for improving EMI and simplifying transformer design
- Optimized gate drive for GaN power devices
- Supports high switching frequency up to 270kHz by product option
- Built-in single-point fault protections against AC line voltage brown-in, brown-out, output short-circuit, output over-voltage, and optocoupler failure
- User adjustable internal OTP threshold for various thermal requirements

Applications

- Rapid-charging AC/DC adapters for smart phones, tablets, power tools and other portable devices
- Other power supply applications for TV, networking, appliances and auxiliary power

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1. Overview

1.1 Block Diagram

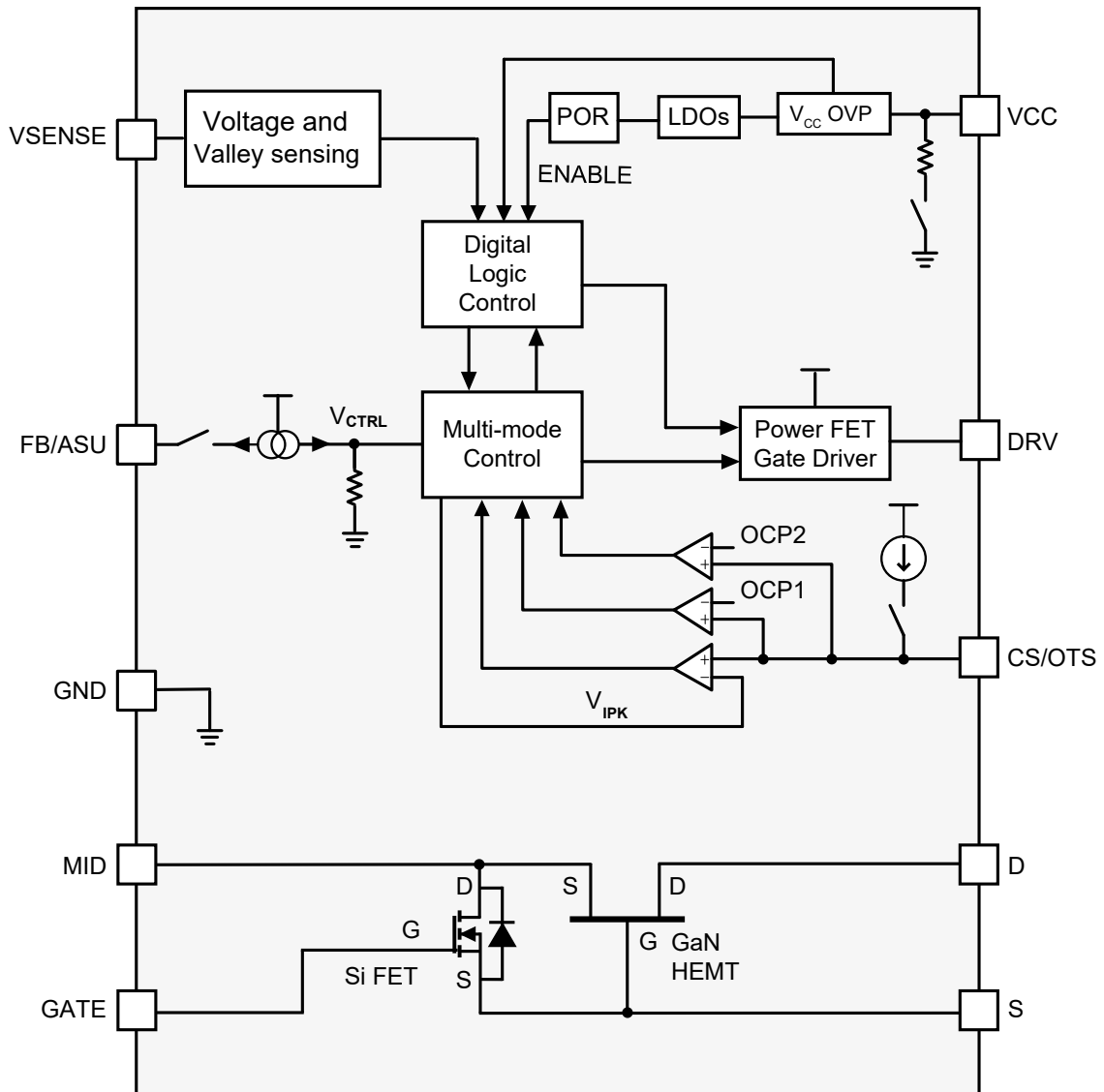


Figure 1. RRW2210x Functional Block Diagram

1.2 Typical Application

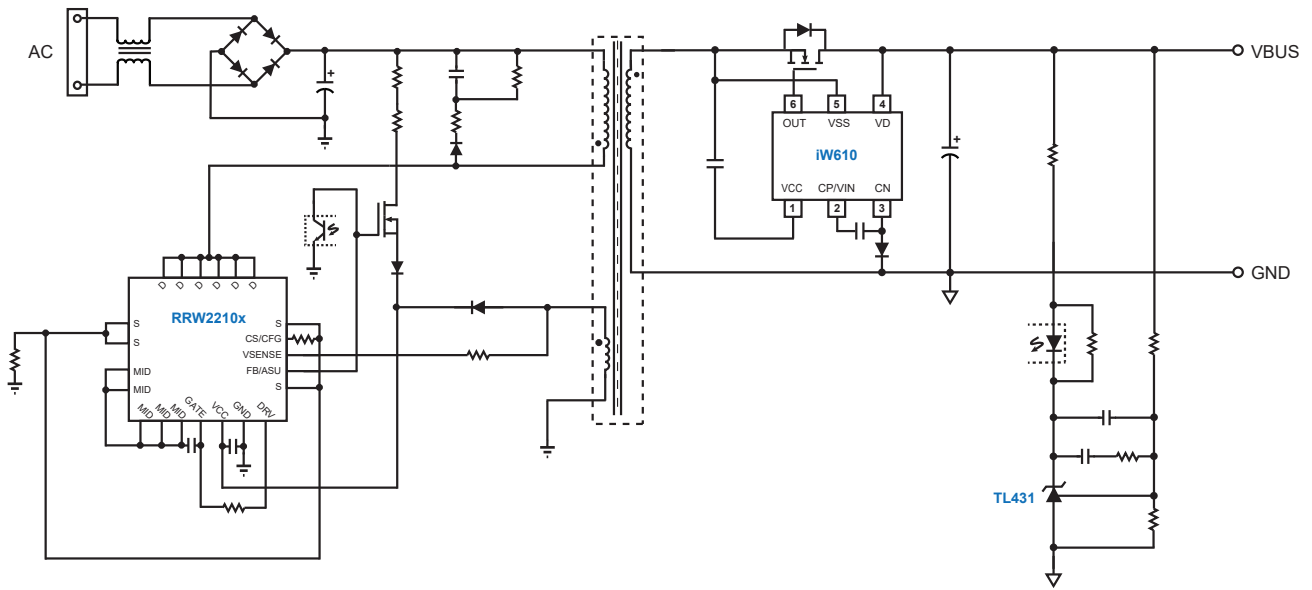


Figure 2. RRW2210x Typical Application Circuit with TL431 Secondary-Side Control Circuit - SR on top side with iW610

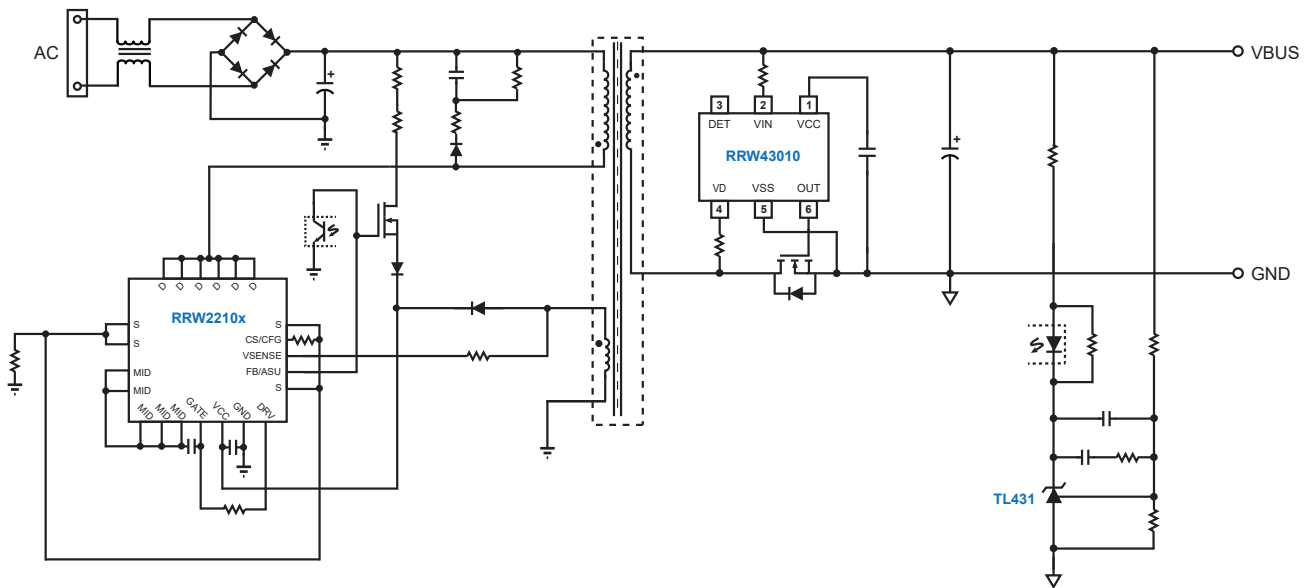


Figure 3. RRW2210x Typical Application Circuit with TL431 Secondary-Side Control Circuit - SR on bottom side with RRW43010

2. Pin Information

2.1 Pin Assignments

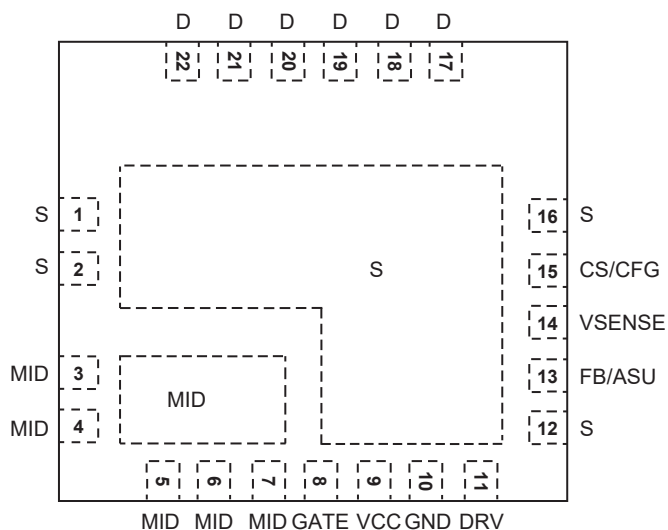


Figure 4. QFN8x8 Package. Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Pin Description
1, 2, 12, 16	S	PWR	SiFET Source/ GaN HEMT Gate
3, 4, 5, 6, 7	MID	PWR	SiFET Drain/ GaN HEMT Source
8	GATE	Analog input	SiFET Gate
9	VCC	PWR	IC power supply
10	GND	GND	Ground
11	DRV	Analog output	Gate drive for main power device
13	FB/ASU	Analog input/Output	Feedback voltage. Used for determining multi-mode control, switching frequency and cycle-by-cycle peak current control and for controlling active start-up device (depletion mode NFET)
14	VSENSE	Analog input/output	Voltage sensing. Used for adapter output voltage sensing and valley mode switching.
15	CS/CFG	Analog input	Current sensing and internal OTP setting. Used for cycle-by-cycle peak-current control and limit. During configuration stage, it can be used to configure internal OTP threshold setting.
17, 18, 19, 20, 21, 22	D	PWR	GaN HEMT Drain

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Conditions	Min	Max	Unit	VAL
T _{STG}	Storage temperature	Nonoperational	-65	150	°C	
T _J	Junction temperature			150	°C	
V _{CC}	DC supply voltage range (I _{CC} = 20mA max)		-0.3	45	V	
I _{CC}	Continuous DC supply current at V _{CC} pin (V _{CC} = 15V)			20	mA	
V _{FB_ASU}	FB/ASU pin voltage		-0.3	20	V	
V _{DRV}	DRV pin voltage		-0.3	20	V	
V _{SENSE}	V _{SENSE} pin voltage		-0.7	45	V	
V _{CS/CFG}	CS/CFG pin voltage		-0.3	5.5	V	
V _{DSS}	Drain to source voltage (T _J = -55°C to 150°C)			700	V	
V _{DSS(TR)} , non-repetitive	Transient drain to source voltage, non-repetitive ⁽¹⁾			800	V	
V _{DSS(TR)} , repetitive	Transient drain to source voltage, repetitive ⁽²⁾			750	V	
V _{GSS}	Gate to source voltage			±12	V	
I _D (RRW22101)	Continuous drain current at T _C =25°C ⁽³⁾			16	A	
	Continuous drain current at T _C =100°C ⁽³⁾			8.4	A	
I _D (RRW22102)	Continuous drain current at T _C =25°C ⁽³⁾			6.5	A	
	Continuous drain current at T _C =100°C ⁽³⁾			4.1	A	
I _D (RRW22105)	Continuous drain current at T _C =25°C ⁽³⁾			3.6	A	
	Continuous drain current at T _C =100°C ⁽³⁾			2.3	A	

1. In off-state, spike duty cycle D<0.01, spike duration <30μs.
2. In off-state, spike duration <5μs.
3. For increased stability at high current operation

3.2 ESD Ratings

ESD Model/Test	Maximum	Unit
JEDEC JS-001-2017 (HBM)	±2,000	V
Latch-up test per JESD78E	±100	mA

3.3 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
DC Supply Voltage Range during normal operation	V _{VCC}	-0.3	42	V
Operating Junction Temperature	T _{JOPT}	-40	150	°C

3.4 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)
QFN8x8 Package	TBD

Parameter	Symbol	Minimum	Maximum	Unit
Maximum Junction Temperature	T_{JMAX}		+150	°C
Maximum Storage Temperature Range	T_{STO}	-65	+150	°C

3.5 Electrical Specifications

Recommended operating conditions unless otherwise noted. $V_{VCC} = 12V$, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSENSE SECTION						
VSENSE input pin current at 5V V_{OUT} (Note 1) (Note 2)	I_{VSENSE_5V}		-	15	-	μA
CS SECTION						
CS regulation lower limit	$V_{IPK(LOW)}$		0.09	0.11	0.13	V
CS regulation upper limit	$V_{IPK(HIGH)}$		0.50	0.53	0.56	V
Switching-cycle over-current threshold	V_{OCP}		0.75	0.8	0.85	V
Configure current source	I_{CFG}		470	500	530	μA
FB/ASU SECTION						
FB/ASU pin clamping voltage	V_{FB/ASU_CLAMP}	Sourcing 500 μA	1.7	2.1	2.6	V
FB path pin internal resistance	R_{FB}		-	23.3	-	k Ω
DRV SECTION						
Driver pull-down ON-resistance	$R_{DS(ON)_PD}$	$I_{SINK} = 5mA$, $T_A = 25^{\circ}C$	8	12	17	Ω
Lowest driver pull-up ON-resistance	$R_{DS(ON)_PU_MIN}$	$I_{SOURCE} = 5mA$, $T_A = 25^{\circ}C$	65	95	120	Ω
Rise time (Note 1)	t_{R_DRV}	$T_A = 25^{\circ}C$, $CL = 330pF$, 10% to 90%	-	95	-	ns
Fall time (Note 1)	t_{F_DRV}	$T_A = 25^{\circ}C$, $CL = 330pF$, 90% to 10%	-	14	-	ns
Output driver voltage source	V_{DR_SOURCE}	$V_{VCC} = 12V$	-	10.5	-	V
VCC SECTION						
VCC maximum operating voltage (Note 1)	V_{VCC}		-	-	42	V
Start-up threshold	$V_{VCC(ST)}$	V_{VCC} rising	14	15.3	16.5	V
Under-voltage lockout threshold	$V_{VCC(UVL)}$	V_{VCC} falling	7.1	7.5	7.9	V
VCC over-voltage protection threshold	$V_{VCC(OVP)}$	V_{VCC} rising	42.5	43.9	45	V
Start-up current	$I_{VCC(ST)}$	$V_{VCC} = 12V$	4	8	13	μA
Quiescent current	I_{VCCQ}	$C_L = 330pF$	-	3.35	-	mA
Sleep mode current	I_{VCC_SLEEP}	$V_{VCC} = 10V$	40	55	70	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS						
Thermal Shutdown Threshold (Note 3)	T_{SD}		Varies by product option			°C
Thermal Shutdown Recovery (Note 3)	T_{SD-R}		$T_{SD}-10$			°C
GaN DEVICE SECTION (RRW22101)						
Maximum drain-source voltage	$V_{DSS(BL)}$	$V_{GS}=0V$	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.5	2	2.5	V
Drain-source on-resistance (Note 4)	$R_{DS(on)eff}$	$V_{GS}=10V, I_D=8.5A, T_J=25^\circ C$	-	150	180	mΩ
		$V_{GS}=10V, I_D=8.5A, T_J=150^\circ C$	-	307	-	
Drain-to-source leakage current	I_{DSS}	$V_{DS}=700V, V_{GS}=0V, T_J=25^\circ C$	-	2.5	25	μA
		$V_{DS}=700V, V_{GS}=0V, T_J=150^\circ C$	-	10	-	
Gate-to-source leakage current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	±10	μA
Input capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=400V, f=1MHz$	-	598	-	pF
Output capacitance	C_{OSS}		-	30	-	
Reverse transfer capacitance	C_{RSS}		-	1	-	
Output capacitance, energy related (Note 5)	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0V$ to 400V	-	43	-	pF
Output capacitance, time related (Note 6)	$C_{O(tr)}$		-	85	-	
Total gate charge	Q_G	$V_{DS}=400V, V_{GS}=0V$ to 10V, $I_D=8.5A$	-	8	-	nC
Gate-source charge	Q_{GS}		-	3.3	-	
Gate-drain charge	Q_{GD}		-	2	-	
Output charge	Q_{OSS}	$V_{GS}=0V, V_{DS}=0V$ to 400V	-	34	-	nC
GaN DEVICE SECTION (RRW22102)						
Maximum drain-source voltage	$V_{DSS(BL)}$	$V_{GS}=0V$	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.5	2	2.5	V
Drain-source on-resistance (Note 4)	$R_{DS(on)eff}$	$V_{DS}=V_{GS}, I_D=0.5mA, V_{GS}=8V, I_D=5A$	-	240	312	mΩ
		$V_{GS}=8V, I_D=5A, T_J=150^\circ C$	-	492	-	
Drain-to-source leakage current	I_{DSS}	$V_{DS}=700V, V_{GS}=0V$	-	1.2	12	μA
		$V_{DS}=700V, V_{GS}=0V, T_J=150^\circ C$	-	8	-	
Gate-to-source forward leakage current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	±10	μA
Input capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=400V, f=1MHz$	-	760	-	pF
Output capacitance	C_{OSS}		-	16	-	
Reverse transfer capacitance	C_{RSS}		-	2	-	
Output capacitance, energy related (Note 5)	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0V$ to 400V	-	24	-	pF
Output capacitance, time related (Note 6)	$C_{O(tr)}$		-	47	-	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total gate charge	Q_G	$V_{DS}=400V, V_{GS}=0V$ to $8V, I_D=4A$	-	9.6	-	nC
Gate-source charge	Q_{GS}		-	2.6	-	
Gate-drain charge	Q_{GD}		-	2.6	-	
Output charge	Q_{OSS}	$V_{GS}=0V, V_{DS}=0V$ to $400V$	-	19	-	nC
GaN DEVICE SECTION (RRW22105)						
Maximum drain-source voltage	$V_{DSS(BL)}$	$V_{GS}=0V$	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.5mA$	1.6	2.1	2.8	V
Drain-source on-resistance (Note 4)	$R_{DS(on)eff}$	$V_{DS}=V_{GS}, I_D=0.5mA, V_{GS}=8V, I_D=3.4A$	-	480	560	mΩ
		$V_{GS}=8V, I_D=3.4A, T_J=150^\circ C$	-	1000	-	
Drain-to-source leakage current	I_{DSS}	$V_{DS}=700V, V_{GS}=0V$	-	1	10	μA
		$V_{DS}=700V, V_{GS}=0V, T_J=150^\circ C$	-	5	-	
Gate-to-source forward leakage current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	±10	μA
Input capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=400V, f=1MHz$	-	760	-	pF
Output capacitance	C_{OSS}		-	9	-	
Reverse transfer capacitance	C_{RSS}		-	1.5	-	
Output capacitance, energy related (Note 5)	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0V$ to $400V$	-	13	-	pF
Output capacitance, time related (Note 6)	$C_{O(tr)}$		-	29	-	
Total gate charge	Q_G	$V_{DS}=400V, V_{GS}=0V$ to $8V, I_D=3.4A$	-	9	-	nC
Gate-source charge	Q_{GS}		-	2.1	-	
Gate-drain charge	Q_{GD}		-	2.1	-	
Output charge	Q_{OSS}	$V_{GS}=0V, V_{DS}=0V$ to $400V$	-	13.5	-	nC

1. These parameters are not 100% tested. They are guaranteed by design and characterization.
2. Refer to [section 5.6](#).
3. Thermal Shutdown Threshold (OTP) varies by product option and CS pin configuration. Refer to [section 5.8](#) and [section 7](#) for the OTP threshold for each product option.
4. Dynamic $R_{DS(on)}$, 100% tested
5. Equivalent capacitance to give same stored energy from 0V to 400V
6. Equivalent capacitance to give same charging time from 0V to 400V

4. Typical Performance Graphs

$T_A = +25^\circ\text{C}$, unless otherwise stated.

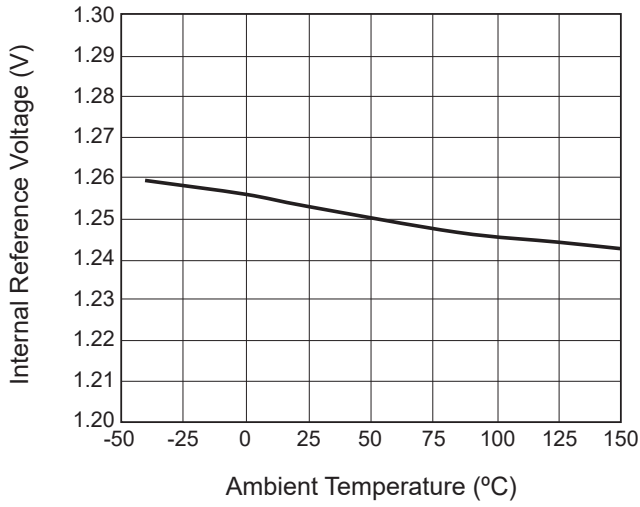


Figure 5. Internal Reference Voltage vs. Ambient Temperature

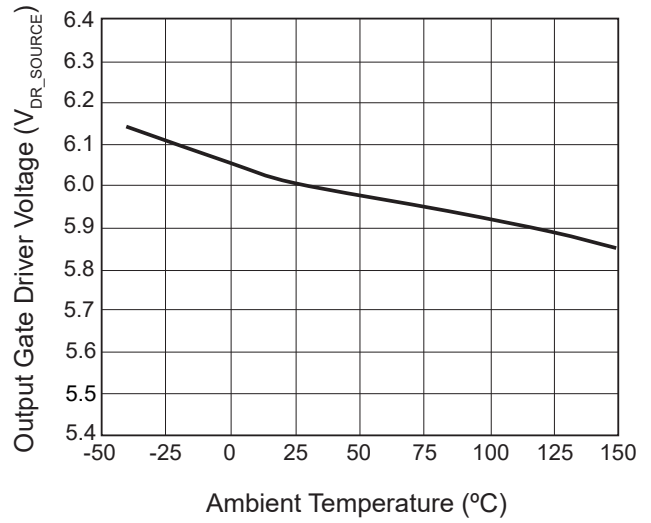


Figure 6. Output Gate Driver Voltage vs. Temperature

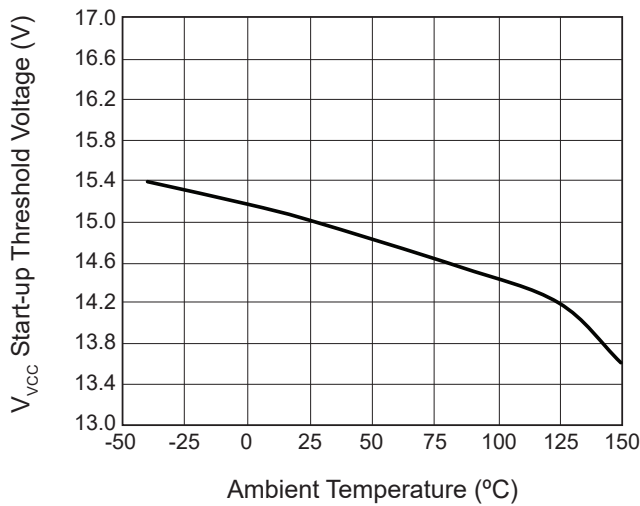


Figure 7. V_{VCC} Start-up Threshold Voltage vs. Ambient Temperature

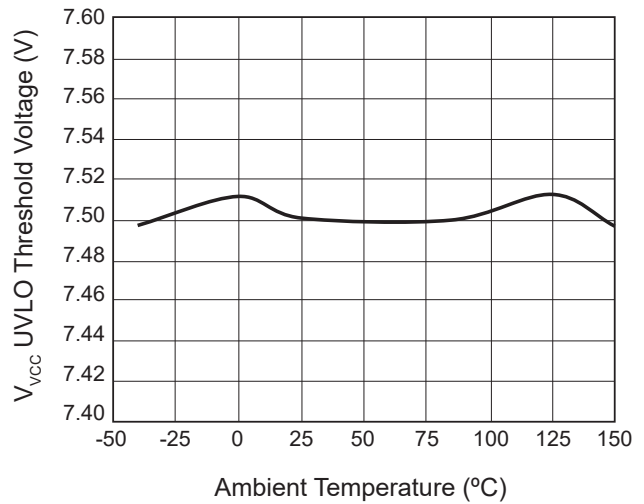


Figure 8. V_{VCC} Start-up Threshold Voltage vs. Ambient Temperature

5. Functional Description

The RRW2210x is a system-in-package (SIP) product with integrated SSR flyback controller and 700V GaN with various $R_{DS(ON)}$ for RRW22101 (150m Ω), RRW22102 (240m Ω) and RRW22105 (480m Ω). The RRW2210x has the AC/DC primary-side flyback controller with quasi-resonant (QR) operation and multi-mode-control (MMC) working with secondary-side regulation (SSR) for applications requiring high resolution in voltage/current steps. The RRW2210x is optimized to work with TL431 for fixed output voltage SSR and the 3rd party USB PD controllers. When pairing with other third party secondary-side USB PD controllers, the RRW2210x can achieve tight multi-level constant voltage (CV) and multi-level constant current (CC) regulation.

As indicated in [Figure 1](#), the RRW2210x operates in peak current control mode. Based on the control signal V_{CTRL} from the FB/ASU pin, the MMC block and the digital control logic block generate the multi-mode operation, switching-on and switching-off commands, and provide commands to dynamically control the gate voltage of power GaN Switch. The FB/ASU pin is used for receiving an SSR control signal through an optocoupler. The CS pin is an analog input pin to sense the power switch current. During the configuration period after power up, the external resistor connected to the CS pin is used to configure the internal OTP setting. During every switching cycle, the CS pin voltage is compared with the V_{IPK} signal from the MMC block to determine the main switch turn-off timing. Third party solutions such as TL431 control use traditional compensation networks for setting system phase and gain margin.

The RRW2210x uses adaptive multi-mode PWM/PFM/burst mode control to dynamically modulate the GaN switching frequency and its peak current V_{IPK} for the optimization of efficiency, EMI, and power consumption. The built-in single-point fault protection include over-voltage protection (OVP), output short-circuit (SCP), over-current protection (OCP), and voltage/current sense fault detection. In particular, the power supplies built with the RRW2210x can achieve no-load power consumption of less than 75mW for a typical 25W to 65W and above design.

Renesas' digital control scheme including the patented constant-frequency QR mode operation are specifically designed to address the challenge and trade-offs of power conversion design. The innovative technologies are ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as standby power and high performance output control.

In addition, the RRW2210x utilizes an innovative proprietary method to sense the input DC bulk capacitor voltage through V_{SENSE} pin. The sensed bulk capacitor voltage will be used in multiple functions, such as multi-mode control, and brown in/brown out protections.

5.1 Pin Details

Pins 1, 2, 12 and 16 – S

SiFET Source/ GaN HEMT Gate.

Pins 3 - 7 – MID

SiFET Drain/ GaN HEMT Source.

Pin 8 – GATE

SiFET Gate.

Pin 9 – VCC

Power supply for the controller during normal operation. The controller starts up when the V_{VCC} voltage reaches 15V (typical) and shuts down when the V_{VCC} voltage drops below 7.5V (typical). A decoupling capacitor of 0.1 μ F or so should be connected between the VCC pin and GND.

Pin 10 – GND

Power ground and signal ground.

Pin 11 – DRV

Gate drive for main power switch.

Pin 13 – FB/ASU

Feedback voltage signal. It is used for determining multi-mode control and cycle-by-cycle peak current control, and for controlling the active start-up device (depletion mode NFET).

Pin 14 – VSENSE

Voltage sensing. It is used for output voltage sensing, auxiliary winding ringing period sensing and input bulk capacitor voltage sensing.

Pin 15 – CS

Current sensing. It is used for cycle-by-cycle peak-current control and limit. During configuration stage, it can be used to configure internal OTP setting.

Pins 17 - 22 – D

GaN HEMT Drain.

5.2 Active Startup and Soft-Start

The RRW2210x has an active start-up circuit that uses an external depletion mode NFET. Prior to start-up, the ENABLE signal is low and the FB/ASU pin voltage closely follows the VCC pin voltage. Consequently, the depletion mode NFET is switched on, allowing the start-up current to charge the VCC bypass capacitor. When the VCC bypass capacitor is charged to a voltage higher than the start-up threshold $V_{VCC(ST)}$, the ENABLE signal becomes active and turns off the depletion mode NFET. The RRW2210x begins to perform internal OTP configuration and internal OTP check. Afterwards, the RRW2210x commences the soft-start function.

During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle-by-cycle by the V_{IPK} comparator. If at any time the V_{VCC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{VCC(UVL)}$, the RRW2210x shuts down. At this time the ENABLE signal is reset to low to turn off all internal circuits and the VCC capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

5.3 Secondary-Side Controller Interfacing

The RRW2210x works with TL431 and other 3rd party secondary-side controllers for SSR. During the RRW2210x soft-start process, the power supply output voltage ramps up and reaches the power-on level for the secondary-side controller. TL431 monitors the output voltage via a voltage divider connected to its reference pin. If the actual output voltage deviates from the desired level, the internal error amplifier will generate the control signal for the optocoupler driver and the optocoupler driver converts the control signal to a proper level of current to drive the diode side of the optocoupler.

The RRW2210x receives the secondary-side control signal in the form of optocoupler current through FB/ASU pin. The internal control signal for the RRW2210x’s multi-mode control is determined by:

$$V_{CTRL} = V_{FB_SRC} - I_{OPTO} \times R_{FB} \tag{5.1}$$

The overall control system including primary side and secondary side is illustrated in [Figure 9](#).

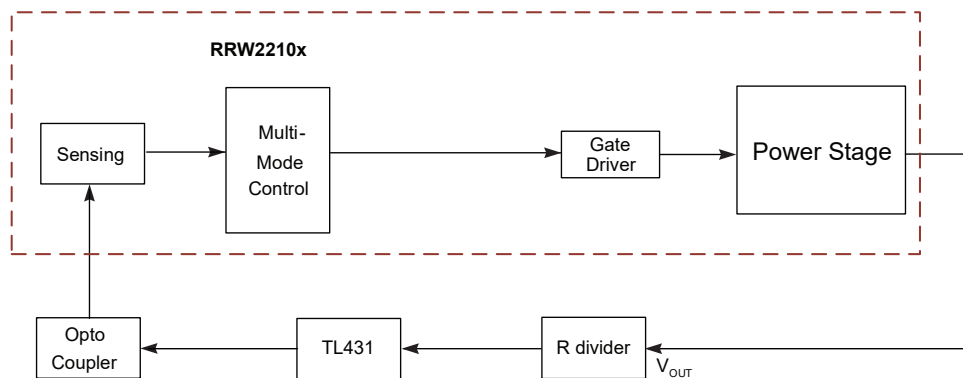


Figure 9. Overall System Level Control with Primary Side and Secondary Side

5.4 Patented Gate Driver Circuit

The RRW2210x features an internal gate drive control, configurable through product options (see section 7). When the Gate Driver CFG mode is enabled, the user can select the pull-up resistor using an external configuration resistor (RCFG) connected to the IC. As shown in Figure 10, the RCFG resistor determines the internal pull-up resistor (Rg), which slows down the dv/dt slope of the drain voltage. Once the drain voltage drops to zero, the Rg pull-up value automatically reduces, allowing the gate voltage to rise quickly to its maximum value. Table 1 provides the configuration resistor ranges corresponding to pull-up resistor values.

If the Gate Driver CFG mode is not enabled, the RCFG resistor is used to set the offset for the OTP set point (see Table 2 for details).

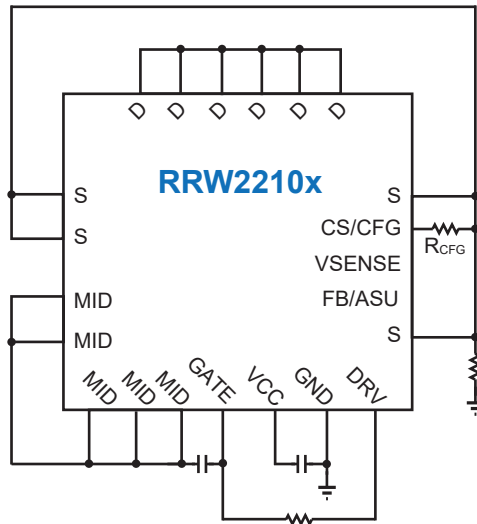


Figure 10. Configuration Resistor

Table 1. Configuration Resistor Pull-up Resistor Values

R _{CFG} resistor range (kΩ)		R _g pull-up values (Ω)
Min	Max	
3.76	4.31	1100
2.39	2.73	700
1.32	1.67	440
0.65	0.85	275
0	0.34	120

The other options available for the RRW2210x are adaptive control where the internal resistance value is dynamically adjusted to optimize the gate drive control. The second option is where the first stage pull-up resistance is pre-set by the product option. And the final option is no internal resistance control and the internal gate driver resistance is fixed at a minimum value and any gate resistance required can be set externally. This option is usually reserved for the highest output power applications.

5.5 Multi-mode PWM/PFM/Burst Mode Control and Quasi-Resonant Switching

The RRW2210x uses a patented adaptive MMC with PWM/PFM/burst modes based on the input voltage and output voltage/current to optimize the efficiency and standby power consumption at various load conditions and eliminate audible noise.

In the constant voltage CV operation, the RRW2210x normally operates in a pulse-width-modulation (PWM) mode under heavy load conditions. In the PWM mode, the switching frequency keeps around constant while the

on-time t_{ON} changes according to the load condition. The maximum switching frequency at PWM mode occurs at highest output voltage setting. As the output voltage decreases, the switching frequency at PWM mode decreases accordingly.

As the output load current decreases, the MMC control adaptively transitions to a pulse-frequency-modulation (PFM) mode. During PFM mode, the power switch peak current is kept constant, while the switching frequency is controlled by MMC block. With a decreasing load current, the switching frequency decreases.

When the switching frequency approaches the human ear audible frequency band, the RRW2210x transitions to the second level of PWM mode, namely the Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 28kHz in order to avoid audible noise. As the load current is further reduced, the RRW2210x transitions to burst mode operation to eliminate audible noise. In burst switching mode, the switching frequency in each burst group keeps 28kHz, while the burst group frequency depends on the load condition.

The RRW2210x also keeps a patented constant-frequency quasi-resonant (QR) switching scheme that has been used in previous generations of Renesas' AC/DC products. Unlike conventional QR modes, this unique QR scheme follows the basic switching frequency profile determined by the MMC control in a deterministic constant-frequency manner and achieves valley mode turn-on for every PWM/PFM/Burst switching cycle. This feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply.

5.6 Patented V_{SENSE} Structure for Output Voltage/Input Bulk Voltage Sensing

The RRW2210x uses a new proprietary technology that monitors the current flowing through V_{SENSE} pin to detect both output voltage and input bulk capacitor voltage. The signal current comes from auxiliary winding through the sensing resistor R_{VS} .

After power up, the VSENSE pin voltage will be regulated at a fixed value. At the steady-state CV operation 5V setting, the VSENSE pin input current at the instant corresponding to point 1 (as indicated in Figures 12 and 14) is regulated to I_{VSENSE_5V} . The VSENSE pin input current is used for output over voltage detection, AC line voltage brown in/out detection and MMC switching frequency control.

The voltage sense resistor is selected such that VSENSE pin current is 15 μ A when output voltage is 5V.

The RRW2210x can sense the auxiliary winding voltage using VCC-referenced configuration (Figures 11 and 12) or GND-referenced configuration (Figures 13 and 14). This allows optimized transformer construction based on the auxiliary winding configuration. This is determined by product option, please see section 7 for details.

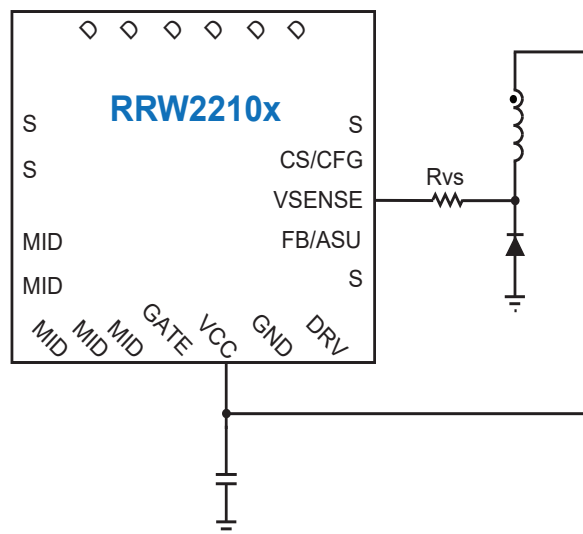


Figure 11. VCC-Referenced V_{SENSE} Structure for Output Voltage/Input Bulk Voltage Sensing

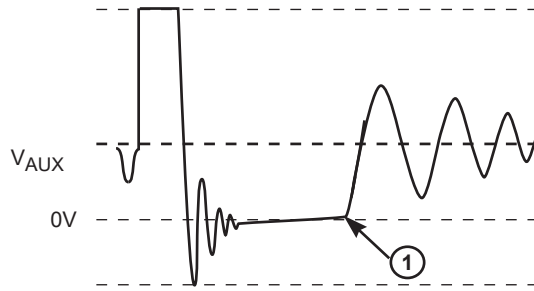


Figure 12. Auxiliary Voltage Waveform (VCC-Referenced)

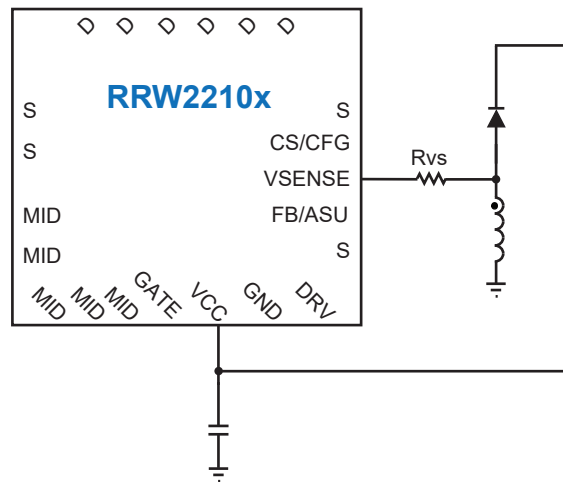


Figure 13. Ground-Referenced V_{SENSE} Structure for Output Voltage/Input Bulk Voltage Sensing

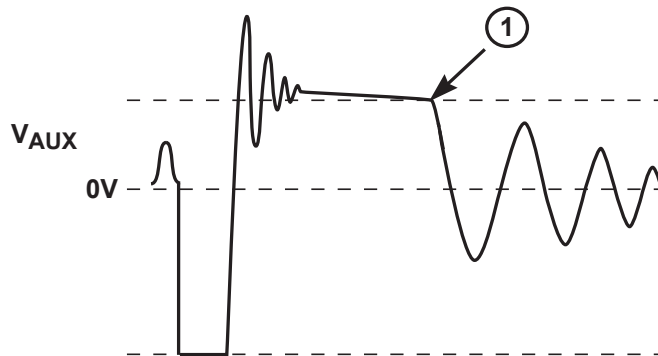


Figure 14. Auxiliary Voltage Waveform (Ground-Referenced)

5.7 Voltage Protection Features

The RRW2210x has its own layer of OVP through VSENSE pin to provide additional protection for some abnormal scenarios. Although there is no pin available to directly sense the input voltage, the RRW2210x uses Renesas’ patented input sensing technology to provide real-time indirect sensing of the magnitude of the DC bulk capacitor voltage. This enables the RRW2210x to detect various conditions of the AC input voltage such as brown-out and brown-in and to take appropriate actions. When the AC input voltage drops below the normal operation range and the power supply input is still connected to the AC source, the RRW2210x initiates a brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis.

Also, the RRW2210x monitors the voltage on the VCC pin, and shuts down when VCC voltage is below the UVLO threshold. The RRW2210x also has a V_{VCC} over-voltage protection (V_{VCC} OVP). During an abnormal event, if the VCC voltage is higher than the protection threshold, the RRW2210x stops switching and shuts down.

To ensure safe operation and add design margin, the VCC auxiliary winding should be designed to limit the VCC continuous operating voltage to be less than the max operating voltage specified in [section 3.5](#).

When any of these faults occur, the RRW2210x remains biased to discharge VCC supply voltage. Once the VCC voltage drops below the UVLO threshold, the RRW2210x resets itself and initiates a new power up cycle. The controller continues in the cycle of start-up, fault and UVLO, until the fault condition is removed.

5.8 Internal Over Temperature Protection (OTP)

The RRW2210x features a configurable internal OTP which shuts down the device if the internal die junction temperature reaches above the internal OTP threshold T_{SD} . After power up, the RRW2210x check internal temperature with the threshold level 10°C lower than T_{SD} . When internal temperature drops below this threshold, the RRW2210x initiates a new soft-start process to build up the output voltage.

The internal OTP threshold offset is set by the combination of the product option (see [section 7](#) for the OTP settings by product option), and an external configuration resistor connected between the CS pin and the R_{SENSE} resistor. The product option will determine the base OTP threshold in a range of 105°C to 143°C . The external configuration resistor determines the offset from nominal, set in 2°C increments as shown in the table below. Given an example, if the base OTP threshold set the product option is 105°C , and the external configuration resistor is between $2.39\text{k}\Omega$ and $2.73\text{k}\Omega$, the actual OTP threshold is $105+6 = 111^{\circ}\text{C}$. Please note that internal junction temperature may be different to pin temperature and package temperature due to thermal impedance.

Table 2. Internal OTP

Internal OTP Configuration Resistor Range (k Ω)		Internal OTP threshold offset ($^{\circ}\text{C}$)
Min	Max	
3.76	4.31	8
2.39	2.73	6
1.32	1.67	4
0.65	0.85	2
0	0.34	0

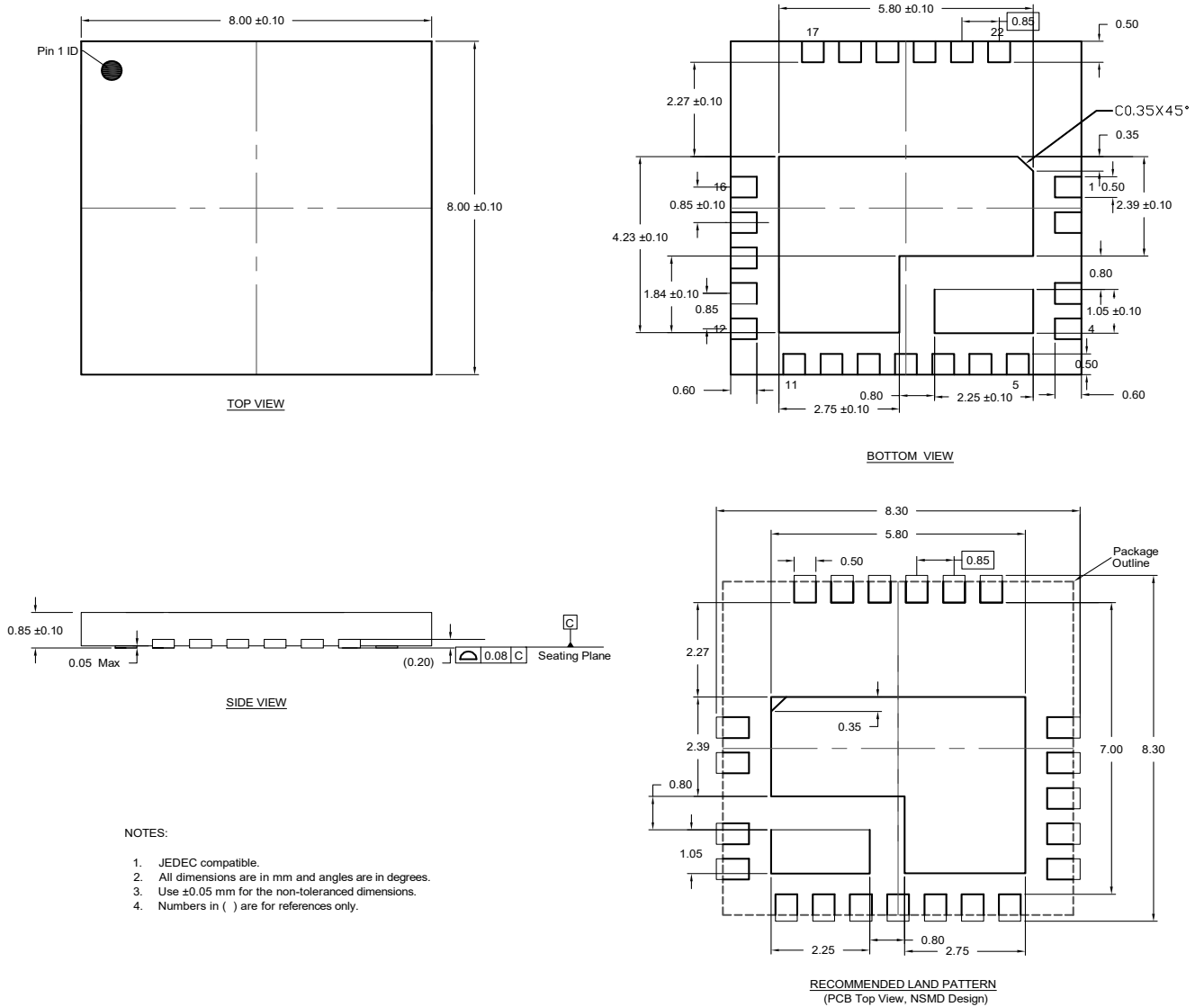
5.9 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built in the RRW2210x. The RRW2210x monitors the peak primary current by CS pin voltage. This allows cycle-by-cycle peak current control and shoot-through protection. When the peak primary current multiplied by the current sense resistor is greater than V_{OCP} , over-current event is detected, and the IC immediately turns off the gate driver until the next cycle. If the OCP event occurs in three consecutive switching cycle, the RRW2210x claims OCP fault and shuts down.

If the current sense resistor is shorted prior to the power supply startup there is a potential danger that over-current condition may not be detected. Thus, the RRW2210x is designed to detect this sense-resistor-short fault in the first several switching cycles during soft start-up.

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

Figure 15. QFN8x8 package outline drawing

7. Ordering Information

Part Number	Options									Package	Description
	Output Voltage Range	Secondary Side Controller	OTP Base	OTP Offset	R _g pull-up values	Max f _{sw}	CCM/DCM	Aux Winding Reference	GaN R _{DS(ON)}		
RRW22101-153	Fixed Vout	TL431	135°C	2°C	By Rcfg	70kHz	CCM	GND	150mΩ	QFN8x8	Tape & Reel ¹
RRW22102-153	Fixed Vout	TL431	135°C	2°C	By Rcfg	70kHz	CCM	GND	240mΩ	QFN8x8	Tape & Reel ¹
RRW22105-153	Fixed Vout	TL431	135°C	2°C	By Rcfg	70kHz	CCM	GND	480mΩ	QFN8x8	Tape & Reel ¹

1. Tape & Reel packing quantity is 4,000/reel. Minimum packing quantity is 4,000.

8. Revision History

Revision	Date	Description
0.02	Mar 11, 2026	▪ Updated Ordering Information.
0.01	Dec 10, 2025	▪ Initial release.