RX14T Group
Renesas MCUs

R01DS0453EJ0102
Rev.1.02
Dec 12, 2025

48-MHz, 32-bit RX MCUs, on-chip FPU, 204 Coremark, supportive of 5 V power supply, 12-bit A/D converter (2 units, programmable gain amplifier × 3 units, and comparator), 48-MHz PWM (three-phase complementary output × 2 channels), on-chip data flash memory

Features

■ 32-bit RXv2 CPU core
- Maximum operating frequency: 48 MHz
  Capable of 204 Coremark in operation at 48 MHz
- Enhanced DSP instructions: 32-bit multiply-accumulate instructions, and 16-bit multiply-subtract instructions are supported.
- On-chip FPU: 32-bit single-precision floating point compliant with IEEE-754
- On-chip divider that operated at the fastest of two clock cycles
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit

■ Arithmetic unit for trigonometric functions (TFUv1)

■ Low power design and architecture
- Operation from a single 2.7-V to 5.5-V supply
- Three low power consumption modes

■ On-chip flash memory for code
- 128 Kbytes size capacities
- User code is programmable by on-board programming.
- For instructions and operands

■ On-chip data flash memory
- 4K bytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states
- 12 Kbytes size capacities

■ DTC
- Five transfer modes

■ Reset and supply management
- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External clock input frequency: Up to 20 MHz
- Main clock oscillator frequency: 1 to 20 MHz
- PLL circuit input: 4 MHz to 12.5 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 24/32/48/64 MHz ± 1%
- IWDT-dedicated on-chip oscillator: 15 kHz
- On-chip clock frequency accuracy measurement circuit (CAC)

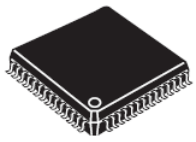
■ Independent watchdog timer
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, CRCA, etc.

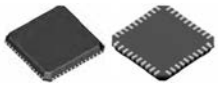
■ MPC
- Input/output functions selectable from multiple pins

■ Up to 5 communication functions
- SCI with multiple functionalities (4 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I²C, and extended serial mode.
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)

■ Up to 15 extended-function timers
- 16-bit MTU3 (6 channels): 48 MHz operation, input capture, output compare, three-phase complementary PWM × 1 channel-output, CPU-efficient complementary PWM, phase counting mode (2 channels)



PLQP0064GA-A 14 × 14 mm, 0.8 mm pitch
PLQP0064KB-C 10 × 10 mm, 0.5 mm pitch
PLQP0052JA-A 10 × 10 mm, 0.65 mm pitch
PLQP0048KB-B 7 × 7 mm, 0.5 mm pitch
PLQP0044GF-A 10 × 10 mm, 0.8 mm pitch
PLQP0032GB-A 7 × 7 mm, 0.8 mm pitch



PWQN0048KC-A 7 × 7 mm, 0.5 mm pitch
PWQN0032KE-A 5 × 5 mm, 0.5 mm pitch
PWQN0024KG-A 4 × 4 mm, 0.5 mm pitch

- 16-bit GPTW (3 channels): operation at 48 MHz, input capture, output compare, PWM waveforms: 6 output channels in single-phase complementary PWM mode/1 output channels in 3-phase complementary PWM mode, PWM waveforms: sawtooth-wave mode, triangle-wave mode (with dead time), linkage with comparator (counting operation, PWM negate control)
  Simultaneous starting of MTU3 and GPTW
- 8-bit TMR (4 channels)
- 16-bit compare-match timers (2 channels)

■ 12-bit A/D converter (2 units)
- Capable of conversion within 0.5 µs
- Unit 0: 8 channels unit 1: 8 channels
- Sampling time can be set for each channel
- Group scan priority control mode (3 levels)
- Self-diagnostic function and analog input disconnection detection assistance function
- Double trigger (data duplication) function for motor control
- Time-interleaved operation to achieve a high sample rate is possible.

■ Input signal amplification function by the programmable gain amplifier (3 units)

■ D/A converter
- 2 channels
- This can be used as reference voltage for a comparator

■ Analog Comparator: 3 channels

■ Register write protection function can protect values in important registers against overwriting.

■ Up to 60 pins for general I/O ports
- 5-V tolerant, open drain, input pull-up

■ Temperature sensor

■ Unique ID
- 32-byte ID code for the MCU

■ Operating temperature range
- –40 to +105°C
- –40 to +125°C

■ Applications
- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 48 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 (variable-length instruction format) • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and exceptions in conformance with the IEEE754 standard
Arithmetic unit for trigonometric functions (TFUv1)		• Sine, cosine, arctangent, $\sqrt{x^2+y^2}$ Simultaneous calculation of sine and cosine Simultaneous calculation of arctangent and $\sqrt{x^2+y^2}$
Memory	ROM	• Capacity: 128 Kbytes • 32 MHz ≤: No-wait cycle access • 32 MHz to 48 MHz: One-wait cycle access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 12 Kbytes • No-wait memory access
	E2 DataFlash	• Capacity: 4 Kbytes • Number of erase/write cycles: 1,000,000 (typ.)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 48 MHz (at max.) Peripheral modules run in synchronization with the PCLKB: 48 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 48 MHz (at max.) • ADCLK in the S12AD runs in synchronization with PCLKD: Up to 64 MHz
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 256 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (The NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCb)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Sequence transfer
I/O ports	General I/O ports	64-pin/52-pin/48-pin/44-pin/32-pin/24-pin • I/O: 59/47/43/39/27/19 • Input: 1/1/1/1/1/1 • Pull-up resistors: 59/47/43/39/27/19 • Open-drain outputs: 47/37/33/30/20/14 • 5-V tolerant: 2/2/2/2/2/2
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 3 (MTU3c)	• 6 units (16 bis × 6 channels) • Provides up to 16 pulse-input/output lines and three pulse-input lines • Select from among fourteen counter-input clock signals for each channel (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) other than channel 1/3/4, for which only eleven signals are available, channel 2 for 12, channel 5 for 10 • 26 output compare/input capture registers • Counter clear operation (with compare match- or input capture-sourced simultaneous counter clear capability) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffer operation • Cascaded operation • 28 interrupt sources • Automatic transfer of register data • Pulse output modes: Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode 3-phase non-overlapping waveform output for inverter control Automatic dead time setting Adjustable PWM duty cycle: from 0 to 100% A/D conversion request delaying function Interrupt at crest/trough can be skipped Double buffer function • Reset-synchronized PWM mode Outputs three phases each for positive and negative PWM waveforms in user-specified duty cycle • Phase counting modes: 16-bit mode (channel 1 and 2)/32-bit mode (channel 1 and 2) • Dead time compensation counter function • A/D converter start trigger can be generated • A/D converter start triggers can be skipped • Signals from the input capture and external counter clock pins are input via a digital filter
	Port output enable 3 (POE3E)	• Control of the high-impedance state of the MTU/GPTW's waveform output pins, and control of switching to the general I/O port pin • 5 pins for input from signal sources: POE0, POE8, POE10, POE11, POE12 • Initiation by detection of short-circuited outputs (detection of PWM outputs that have become an active level simultaneously) • Initiation by comparator detection/oscillation stop detection/software • Additional programming of output control target pins is enabled

Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Timers	General PWM timer (GPTWd)	• 16 bits × 3 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Capable of synchronous start, stop, or clearing of counter for any channel • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting 1 external triggers • Output pin disabling function by a dead time error or a short circuit detection among output pins • Capable of generating conversion start triggers for the A/D converters as well as monitoring external pins for a start timing of conversion. • Capable of using noise filter of input capture • Simultaneous starting of the GPT by MTU0 or MTU4
	Port output enable for GPTW (POEG)	• Controlling the output disable for GPTW waveform output • Initiation by input level detection of GTETRGA pin • Initiation by output disable request from GPTW • Initiation by detection of comparator interrupt request • Initiation by detection of oscillation stop or by software
	8-bit timer (TMRb)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed clock for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 4 channels (channel 1, 5, and 6: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers (SCI5, SCI6, SCI12) Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
12-bit A/D converter (S12AD)		• 12 bits 2 units (8 channels × 2 units) • Minimum conversion time: 0.5 µs per channel when the ADCLK is operating at 64 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Starting and stopping of scanning according to group priority control is possible in the group scan mode. The order of priority is group A (highest) > group B > group C (lowest). • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU, GPTW, TMR), or an external trigger signal • Time-interleaved operation is possible, with two units of the AD converter alternately converting the voltage on the same channel to achieve a high sample rate. • The reference voltage is selectable as VREFH0/VCC or VREFL0/VSS.
Programmable Gain Amplifier (PGA)		• Input signal amplification function by the programmable gain amplifier (3 units) Amplification rate: 4 times, 8 times, 16 times, 32 times (total of 4 steps)
Comparator C (CMPC)		• 3 channels • Function to compare the reference voltage and the analog input voltage • The reference voltage is selectable per comparator as either of the two outputs of the D/A converter or as an external input. • Analog input voltages: Four (for CMPC0 and CMPC1) or three (for CMPC2) • Digital filtering
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0 V to VCC • External output is possible, but only from DA0. Both outputs can be used as comparator C reference voltages.
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
Safety	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$, $X^{32}+X^{28}+X^{27}+X^{26}+X^{25}+X^{23}+X^{22}+X^{20}+X^{19}+X^{18}+X^{14}+X^{13}+X^{11}+X^{10}+X^9+X^8+X^6+1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOC)	Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 2.7 to 5.5 V: 48 MHz
Operating temperature range		G version: –40 to +105°C, M version: –40 to +125°C
Packages		64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 52-pin LQFP (PLQP0052JA-A) 10 × 10 mm, 0.65 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 44-pin LQFP (PLQP0044GF-A) 10 × 10 mm, 0.8 mm pitch 32-pin LQFP (PLQP0032GB-A) 7 × 7 mm, 0.8 mm pitch 48-pin HWQFN (PWQN0048KC-A) 7 × 7 mm, 0.5 mm pitch 32-pin HWQFN (PWQN0032KE-A) 5 × 5 mm, 0.5 mm pitch 24-pin HWQFN (PWQN0024KG-A) 4 × 4 mm, 0.5 mm pitch
Debugging interfaces		FINE interface

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX14T					
		64 Pins	52 Pins	48 Pins	44 Pins	32 Pins	24 Pins
Memory	ROM	128 Kbytes					
	RAM	12 Kbytes					
	E2 data flash	4 Kbytes					
External interrupts		NMI, IRQ0 to IRQ7					
DMA	Data transfer controller	Available					
Timers	Multi-function timer pulse unit 3	ch0 to ch5				ch0 to ch4	
	Port output enable 3	Available					
	General PWM timer	ch0 to ch2					
	Port output enable for GPTW	Available					
	8-bit timer	2 channels × 2 units					
	Compare match timer	2 channels × 1 unit					
	Independent watchdog timer	Available					
Communication functions	Serial communications interfaces (SCIg)	3 channels (SCI1, 5, 6)					
	Serial communications interfaces (SCIh)	1 channel (SCI12)					
	I²C bus interface	1 channel					
12-bit A/D converter		Number of pins: 14*1 8 in unit 0 8 in unit 1	Number of pins: 12*1 8 in unit 0 6 in unit 1	Number of pins: 12*1 8 in unit 0 6 in unit 1	Number of pins: 11*1 7 in unit 0 6 in unit 1	Number of pins: 8*1 5 in unit 0 5 in unit 1	Number of pins: 6*1 3 in unit 0 5 in unit 1
Programmable Gain Amplifier		3 units					
Comparator C		3 channels					
D/A converter		2 channels					
Temperature sensor		Available					
CRC calculator		Available					
Data operation circuit		Available					
Clock frequency accuracy measurement circuit		Available					
Packages		64-pin LFQFP (0.5 mm) 64-pin LQFP (0.8 mm)	52-pin LQFP (0.65 mm)	48-pin LFQFP (0.5 mm) 48-pin HWQFN (0.5 mm)	44-pin LQFP (0.8 mm)	32-pin LQFP (0.8 mm) 32-pin HWQFN (0.5 mm)	24-pin HWQFN (0.5 mm)

Note 1. Two of these pins are exclusively shared by units 0 and 1.

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency	Operating Temperature
RX14T	R5F514T5AGFM	PLQP0064KB-C	128 Kbytes	12 Kbytes	4 Kbytes	48 MHz	–40 to +105°C
	R5F514T5AGFK	PLQP0064GA-A					
	R5F514T5AGFD	PLQP0052JA-A					
	R5F514T5AGFL	PLQP0048KB-B					
	R5F514T5AGFV	PLQP0044GF-A					
	R5F514T5AGFJ	PLQP0032GB-A					
	R5F514T5AGNE	PWQN0048KC-A					
	R5F514T5AGNH	PWQN0032KE-A					
	R5F514T5AGNK	PWQN0024KG-A					
	R5F514T5AMFM	PLQP0064KB-C	128 Kbytes	12 Kbytes	4 Kbytes	48 MHz	–40 to +125°C
	R5F514T5AMFK	PLQP0064GA-A					
	R5F514T5AMFD	PLQP0052JA-A					
	R5F514T5AMFL	PLQP0048KB-B					
	R5F514T5AMFJ	PLQP0032GB-A					
	R5F514T5AMNE	PWQN0048KC-A					
	R5F514T5AMNH	PWQN0032KE-A					
	R5F514T5AMNK	PWQN0024KG-A					

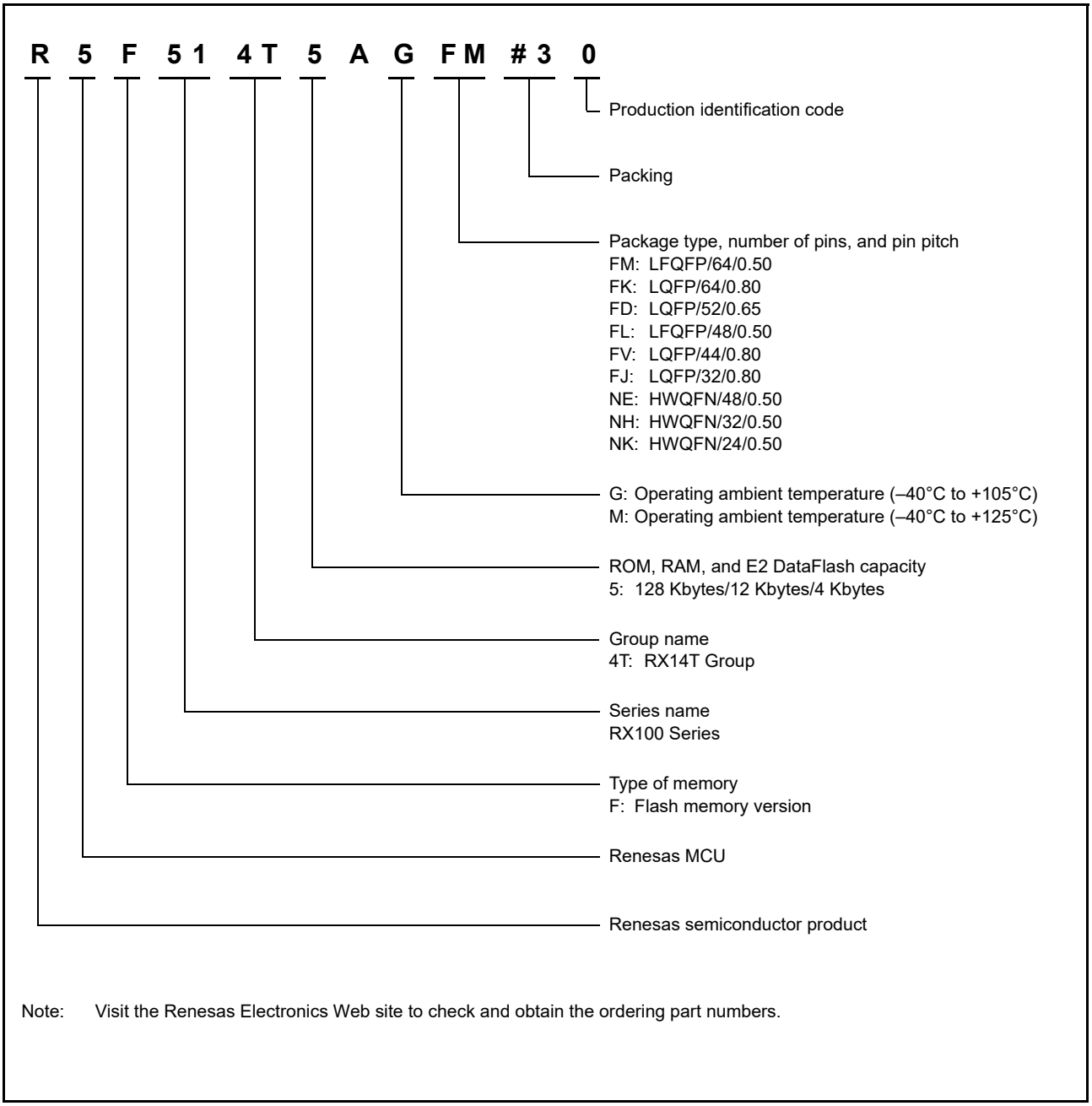


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

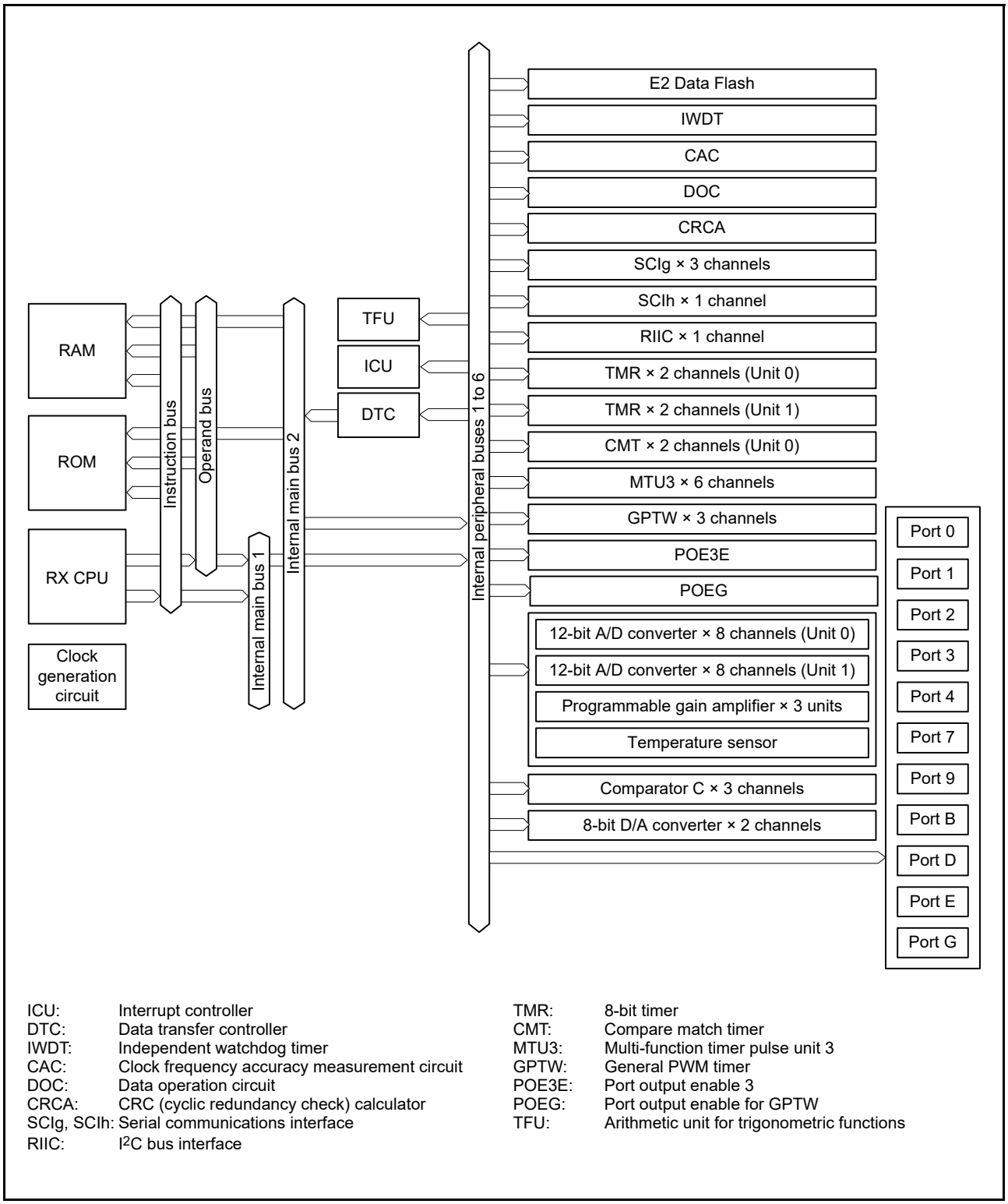


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. For usage, refer to section 3.1, Operating Mode Types and Selection in the User's Manual: Hardware.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
Clock frequency accuracy measurement circuit	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC0A#, MTIOC0B#, MTIOC0C#, MTIOC0D#	I/O	The TGRA0 to TGRD0 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC1A#, MTIOC1B#	I/O	The TGRA1 and TGRB1 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC2A#, MTIOC2B#	I/O	The TGRA2 and TGRB2 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC3A#, MTIOC3B#, MTIOC3C#, MTIOC3D#	I/O	The TGRA3 to TGRD3 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIOC4A#, MTIOC4B#, MTIOC4C#, MTIOC4D#	I/O	The TGRA4 to TGRD4 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins
	MTIC5U#, MTIC5V#, MTIC5W#	Input	The TGRU5, TGRV5, and TGRW5 input capture inverted input/external pulse inverted input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D conversion start request frame synchronization signal output pins.

Table 1.4 Pin Functions (2/3)

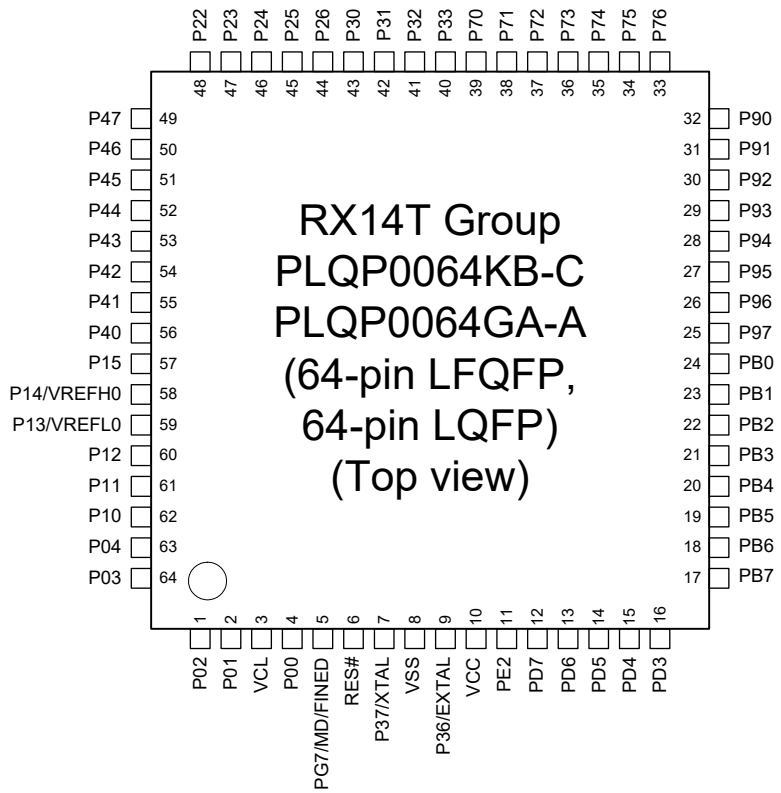
Classifications	Pin Name	I/O	Description
Port output enable 3	POE0#, POE8#, POE10#, POE11#, POE12#	Input	Input pins for request signals to switch the MTU and GPTW pins between the high impedance state
General PWM timer	GTETRGA	Input	External trigger input pin
	GTIOC0A to GTIOC2A, GTIOC0B to GTIOC2B	I/O	Input capture input/output compare output/PWM output pins
	GTIOC0A# to GTIOC2A#, GTIOC0B# to GTIOC2B#	I/O	Input capture inverted input/output compare inverted output/PWM inverted output pins
	GTCPPO0	Output	Synchronized PWM output
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6	Input	Input pins for received data.
	TXD1, TXD5, TXD6	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	SMISO1, SMISO5, SMISO6	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#	Input	Chip-select input pin.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Chip-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for received data.
	TXDX12	Output	Output pin for transmitted data.
	SIOX12	I/O	Input/output pin for received or transmitted data.

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
I²C bus interface	SCL0	I/O	Input/output pin for I²C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I²C bus interface data. Bus can be directly driven by the N-channel open drain output.
12-bit A/D converter	AN000 to AN007, AN102 to AN107	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signal that start the A/D conversion.
	ADST0, ADST1	Output	Output pins for A/D conversion status.
	ADSS0, ADSS1	Output	Output pins indicating results of AD sampling
PGA	PGAIN00 to PGAIN02	Input	PGA analog input pins
	PGAGND	Input	PGA ground pin
	PGAOUT0	Output	PGA monitoring pin
8-bit D/A converter	DA0	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C	COMP0 to COMP3	Output	Comparator detection result output pins.
	CVREFC0	Input	Analog reference voltage supply pins for comparator C.
	CMPCnm	Input	Analog input pin for CMPCnm (n = 0 to 2, m = 0 to 3)
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
I/O ports	P00 to P04	I/O	5-bit input/output pins.
	P10 to P15	I/O	6-bit input/output pins.
	P22 to P26	I/O	5-bit input/output pins.
	P30 to P33, P36, P37	I/O	6-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P90 to P97	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD3 to PD7	I/O	5-bit input/output pins.
	PE2	Input	1-bit input/output pin (PE2 input pin).
	PG7	I/O	1-bit input/output pin.

1.5 Pin Assignments

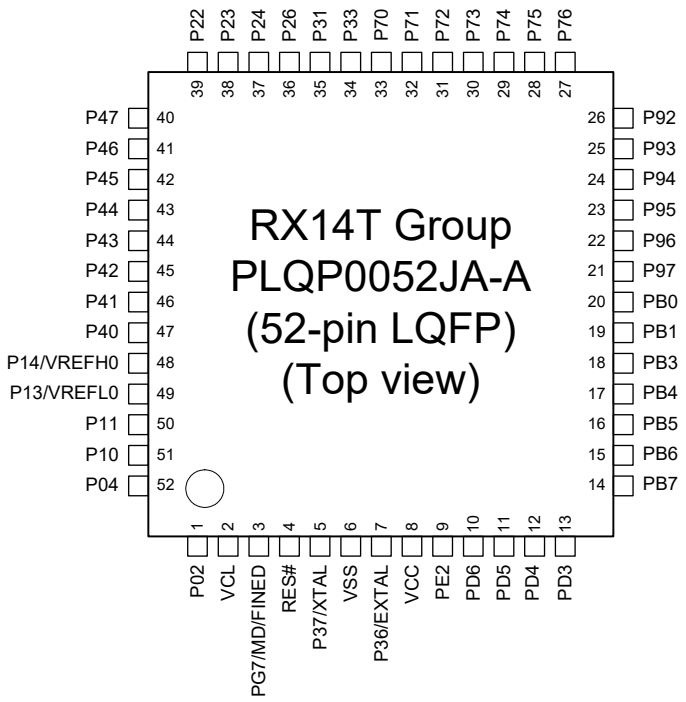
1.5.1 64-pin LFQFP, 64-pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP)”.

Figure 1.3 Pin Assignments of the 64-Pin LFQFP, 64-Pin LQFP

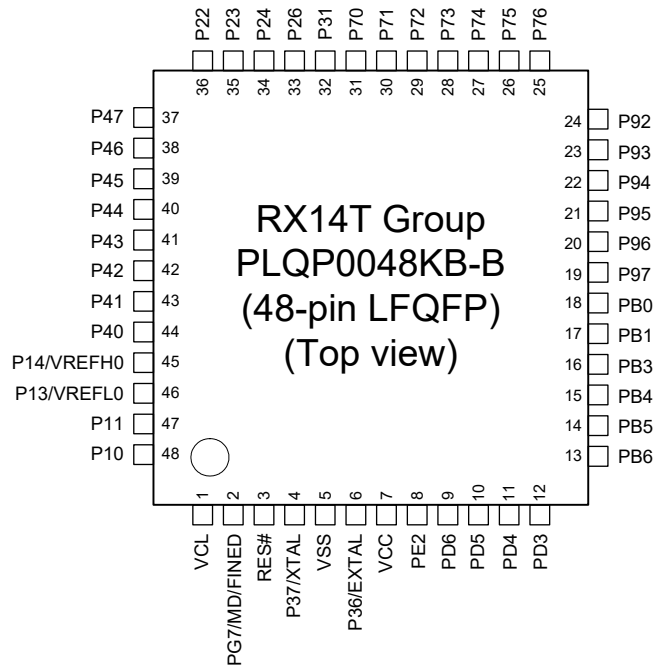
1.5.2 52-pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (52-Pin LQFP)”.

Figure 1.4 Pin Assignments of the 52-Pin LQFP

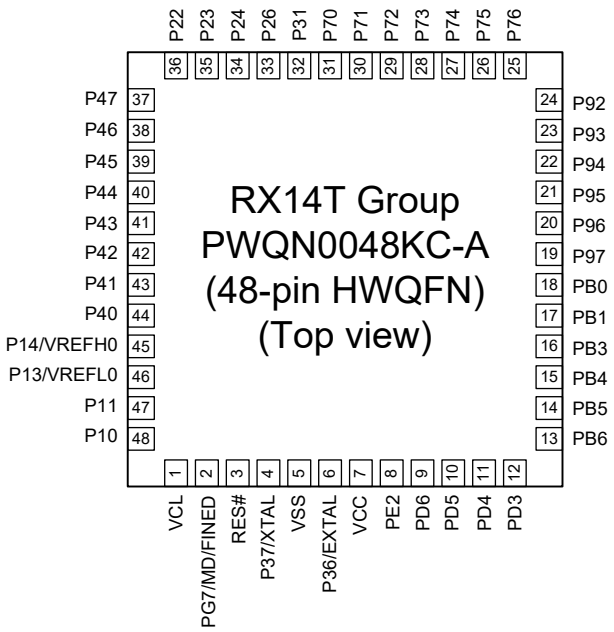
1.5.3 48-pin LFQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN)”.

Figure 1.5 Pin Assignments of the 48-Pin LQFP

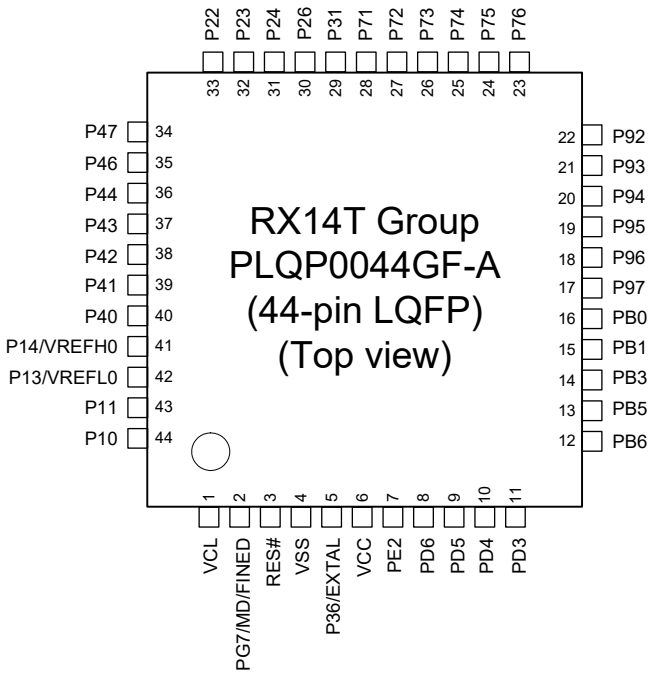
1.5.4 48-pin HWQFN



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN)”.

Figure 1.6 Pin Assignments of the 48-Pin HWQFN

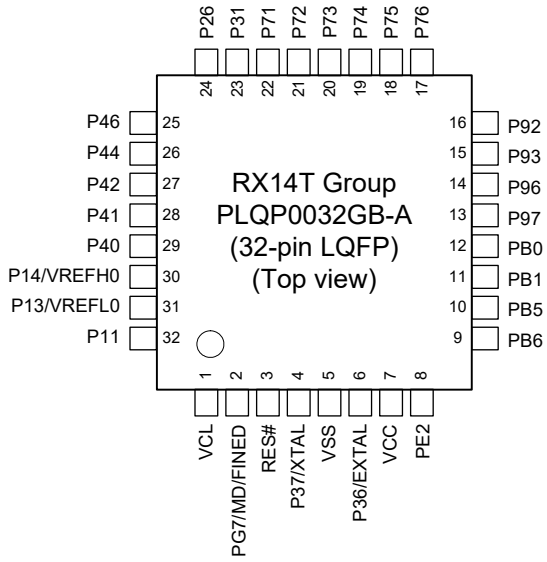
1.5.5 44-pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (44-Pin LQFP)”.

Figure 1.7 Pin Assignments of the 44-Pin LQFP

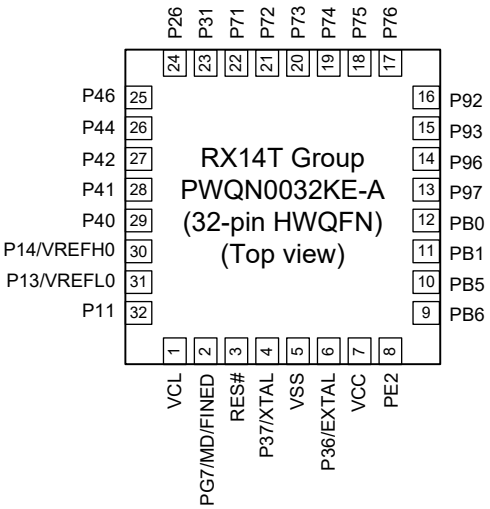
1.5.6 32-pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN)”.

Figure 1.8 Pin Assignments of the 32-Pin LQFP

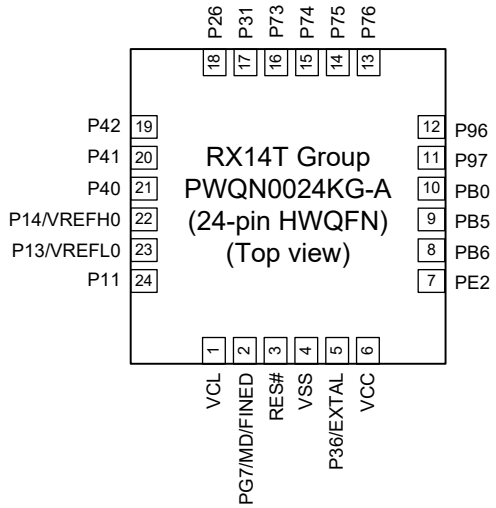
1.5.7 32-pin HWQFN



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN)”.

Figure 1.9 Pin Assignments of the 32-Pin HWQFN

1.5.8 24-pin HWQFN



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (24-Pin HWQFN)”.

Figure 1.10 Pin Assignments of the 24-Pin HWQFN

1.6 List of Pins and Pin Functions

1.6.1 64-pin LFQFP, 64-pin LQFP

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP) (1/3)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
1		P02		CTS1#/RTS1#/SS1#	IRQ5	ADST0
2		P01			IRQ2	ADST1
3	VCL					
4	CACREF	P00			IRQ4	ADSS0
5	MD/FINED	PG7		CTS5#/RTS5#/SS5#/SCK6/SCK12		ADST0
6	RES#					
7	XTAL	P37	POE11#	TXD6/SMOSI6/SSDA6/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12	IRQ0	ADSS1
8	VSS					
9	EXTAL	P36	MTIOC0A/MTIOC4A/ MTIOC1A/MTIOC0A#/ MTIOC4A#/MTIOC1A#/ GTIOC0A/GTCPPO0/ GTIOC0A#/POE12#	RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12	IRQ3	ADST1
10	VCC					
11		PE2	GTETRGA/TMCI1/TMRI0/ POE10#		IRQ0/ NMI	
12		PD7	TMRI1			
13		PD6	MTIOC0D/MTIOC4D/ MTIOC0D#/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMO1	CTS1#/RTS1#/SS1#	IRQ5	ADST0
14		PD5	MTIOC0C/MTIOC4C/ MTIOC0C#/MTIOC4C#/ GTIOC2A/GTIOC2A#/TMRI0	RXD1/SMISO1/SSCL1	IRQ3	ADSS0
15		PD4	MTIOC0B/MTIOC4B/ MTIOC0B#/MTIOC4B#/ GTIOC1B/GTIOC1B#/TMCI0	SCK1	IRQ2	
16		PD3	MTIOC0A/MTIOC4A/ MTIOC0A#/MTIOC4A#/ GTIOC1A/GTIOC1A#/TMO0	TXD1/SMOSI1/SSDA1		
17		PB7		SCK5/CTS6#/RTS6#/SS6#		
18		PB6	MTIOC3C/MTCLKD/ MTIOC2B/MTIOC3C#/ MTCLKD#/MTIOC2B#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI0/POE11#	RXD5/SMISO5/SSCL5/RXD1/SMISO1/ SSCL1	IRQ5	ADSS0
19		PB5	MTIOC1B/MTIOC3A/ MTIOC2A/MTIOC1B#/ MTIOC3A#/MTIOC2A#/ GTIOC1A/GTIOC2A/ GTIOC1A#/GTIOC2A#/ TMO0/POE12#	TXD5/SMOSI5/SSDA5/TXD1/SMOSI1/ SSDA1	IRQ7	ADSS1
20		PB4		RXD6/SMISO6/SSCL6		ADTRG0#
21		PB3	POE8#	TXD6/SMOSI6/SSDA6	IRQ3	ADTRG1#
22		PB2	MTIC5W/MTIC5W#	SCK6		
23	CACREF	PB1	MTIOC0A/MTIOC4D/ MTIOC0A#/MTIOC4D#/ GTIOC2B/GTIOC2B#	SCK5/SCK12	IRQ2	
24		PB0	MTIOC0B/MTCLKC/ MTIOC4C/MTIOC0B#/ MTCLKC#/MTIOC4C#/ GTIOC1B/GTADSM0/ GTIOC1B#/TMRI1	TXD5/SMOSI5/SSDA5/SCK1/SDA0		ADSM0
25		P97	MTIOC0C/MTCLKA/ MTIOC3D/MTIOC0C#/ MTCLKA#/MTIOC3D#/ GTIOC0B/GTADSM1/ GTIOC0B#/GTETRGA/ TMCI1	RXD5/SMISO5/SSCL5/SCL0	IRQ2	ADSM1

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP) (2/3)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
26	CLKOUT	P96	MTIOC0D/MTCLKB/ MTIOC4B/MTIOC0D#/ MTCLKB#/MTIOC4B#/ GTIOC2A/GTIOC2A#/ TMO1/POE0#	SCK5/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		
27		P95	MTIOC1B/MTIOC2A/ MTIOC4A/MTIOC1B#/ MTIOC2A#/MTIOC4A#/ GTIOC1A/GTIOC1A#	CTS12#/RTS12#/SS12#		
28		P94	MTIOC1A/MTIOC2B/ MTIOC3B/MTIOC1A#/ MTIOC2B#/MTIOC3B#/ GTIOC0A/GTIOC0A#	CTS5#/RTS5#/SS5#/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12	IRQ4	
29		P93	MTIOC0C/MTIOC2B/ MTCLKA/MTIOC0C#/ MTIOC2B#/MTCLKA#/ GTIOC1B/GTIOC1B#/TMO1	RXD12/SMISO12/SSCL12/RXDX12	IRQ1	ADTRG1#
30		P92	MTIOC0B/MTIOC1A/ MTIOC0B#/MTIOC1A#/ GTIOC1A/GTIOC1A#/TMRI1	SCK5/SCK12	IRQ0	ADTRG0#
31		P91	MTIC5U/MTIC5U#/TMCI1			
32		P90	MTIC5V/MTIC5V#		IRQ6	
33	CACREF	P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMRI2	RXD12/SMISO12/SSCL12/RXDX12		
34		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC1B#/ TMCI2/POE8#	SCK12		
35		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC0B#/TMO2	CTS6#/RTS6#/SS6#/CTS12#/RTS12#/ SS12#		
36		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMRI3	SCK6		
37		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC1A#	RXD1/SMISO1/SSCL1	IRQ7	
38		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#	TXD1/SMOSI1/SSDA1	IRQ6	
39		P70	GTCPPO0/POE0#	SCK1	IRQ5	
40		P33	MTIOC3A/MTCLKA/ MTIOC0C/MTIOC3A#/ MTCLKA#/MTIOC0C#			
41		P32	MTIOC3C/MTCLKB/ MTIOC0D/MTIOC3C#/ MTCLKB#/MTIOC0D#/ POE10#			
42		P31	MTIOC4A/MTIOC4A#/ GTIOC0B/GTIOC1A/ GTIOC0B#/GTIOC1A#/ TMCI3	TXD6/SMOSI6/SSDA6/SDA0*1		
43		P30	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ POE11#	SCK6		
44		P26	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#/TMO3	RXD6/SMISO6/SSCL6/SCL0*1	IRQ1	
45		P25	MTIOC0B/MTCLKD/ MTIOC4B/MTIOC0B#/ MTCLKD#/MTIOC4B#/ GTETRGA/TMRI3/POE12#			
46	CLKOUT	P24	MTIC5U/MTIC5U#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI2	RXD5/SMISO5/SSCL5	IRQ3	COMP0
47	CACREF	P23	MTIC5V/MTCLKA/MTIC5V#/ MTCLKA#/GTIOC2A/ GTADSM0/GTIOC2A#/ TMO2	TXD5/SMOSI5/SSDA5	IRQ4	ADSS0/COMP1

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP) (3/3)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
48		P22	MTIC5W/MTCLKB/ MTIC5W#/MTCLKB#/ GTADSM1/TMRI2	SCK5	IRQ2	ADSS1/COMP2/ PGAOUT0
49		P47				AN007/PGAGND
50		P46	GTADSM0			AN006/ADSS0/ CMPC13
51		P45				AN005
52		P44	GTADSM1			AN004/ADSS1/DA0/ CMPC03/CVREFC0
53		P43				AN003
54		P42				AN002/CMPC20/ CMPC21/PGAIN02
55		P41				AN001/CMPC10/ CMPC11/PGAIN01
56		P40				AN000/CMPC00/ CMPC01/PGAIN00
57		P15				AN107
58	VREFH0	P14			IRQ6	AN106/ADST0/CMPC22
59	VREFL0	P13			IRQ4	AN105/CMPC12
60		P12			IRQ7	AN104
61		P11	MTIOC3A/MTCLKC/ MTIOC4C/MTIOC3A#/ MTCLKC#/MTIOC4C#/ TMO3/TMO2/POE8#	CTS1#/RTS1#/SS1#/TXD6/SMOSI6/ SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12	IRQ1	AN102/CMPC02
62		P10	MTCLKD/MTCLKD#/TMRI3/ TMO1		IRQ0	AN103
63		P04	MTIOC1A/MTIOC1A#/ GTIOC2A/GTIOC2A#/ TMCI3/TMO0			ADSS1
64		P03	MTIOC1B/MTIOC1B#/ GTIOC2B/GTIOC2B#			ADTRG0#

Note 1. This pin is not 5-V tolerant. For the input voltages of the 5-V tolerant and non-5-V tolerant pins, see the input voltage column in Recommended Operating Conditions (1) under section 2, Electrical Characteristics.

1.6.2 52-pin LQFP

Table 1.6 List of Pins and Pin Functions (52-Pin LQFP) (1/3)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
1		P02		CTS1#/RTS1#/SS1#	IRQ5	ADST0
2	VCL					
3	MD/FINED	PG7		CTS5#/RTS5#/SS5#/SCK6/SCK12		ADST0
4	RES#					
5	XTAL	P37	POE11#	TXD6/SMOSI6/SSDA6/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12	IRQ0	ADSS1
6	VSS					
7	EXTAL	P36	MTIOC0A/MTIOC4A/ MTIOC1A/MTIOC0A#/ MTIOC4A#/MTIOC1A#/ GTIOC0A/GTCPPO0/ GTIOC0A#/POE12#	RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12	IRQ3	ADST1
8	VCC					
9		PE2	GTETRGA/TMCI1/TMRI0/ POE10#		IRQ0/ NMI	
10		PD6	MTIOC0D/MTIOC4D/ MTIOC0D#/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMO1	CTS1#/RTS1#/SS1#	IRQ5	ADST0
11		PD5	MTIOC0C/MTIOC4C/ MTIOC0C#/MTIOC4C#/ GTIOC2A/GTIOC2A#/TMRI0	RXD1/SMISO1/SSCL1	IRQ3	ADSS0
12		PD4	MTIOC0B/MTIOC4B/ MTIOC0B#/MTIOC4B#/ GTIOC1B/GTIOC1B#/TMCI0	SCK1	IRQ2	
13		PD3	MTIOC0A/MTIOC4A/ MTIOC0A#/MTIOC4A#/ GTIOC1A/GTIOC1A#/TMO0	TXD1/SMOSI1/SSDA1		
14		PB7		SCK5/CTS6#/RTS6#/SS6#		
15		PB6	MTIOC3C/MTCLKD/ MTIOC2B/MTIOC3C#/ MTCLKD#/MTIOC2B#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI0/POE11#	RXD5/SMISO5/SSCL5/RXD1/SMISO1/ SSCL1	IRQ5	ADSS0
16		PB5	MTIOC1B/MTIOC3A/ MTIOC2A/MTIOC1B#/ MTIOC3A#/MTIOC2A#/ GTIOC1A/GTIOC2A/ GTIOC1A#/GTIOC2A#/ TMO0/POE12#	TXD5/SMOSI5/SSDA5/TXD1/SMOSI1/ SSDA1	IRQ7	ADSS1
17		PB4		RXD6/SMISO6/SSCL6		ADTRG0#
18		PB3	POE8#	TXD6/SMOSI6/SSDA6	IRQ3	ADTRG1#
19	CACREF	PB1	MTIOC0A/MTIOC4D/ MTIOC0A#/MTIOC4D#/ GTIOC2B/GTIOC2B#	SCK5/SCK12	IRQ2	
20		PB0	MTIOC0B/MTCLKC/ MTIOC4C/MTIOC0B#/ MTCLKC#/MTIOC4C#/ GTIOC1B/GTADSM0/ GTIOC1B#/TMRI1	TXD5/SMOSI5/SSDA5/SCK1/SDA0		ADSM0
21		P97	MTIOC0C/MTCLKA/ MTIOC3D/MTIOC0C#/ MTCLKA#/MTIOC3D#/ GTIOC0B/GTADSM1/ GTIOC0B#/GTETRGA/ TMCI1	RXD5/SMISO5/SSCL5/SCL0	IRQ2	ADSM1
22	CLKOUT	P96	MTIOC0D/MTCLKB/ MTIOC4B/MTIOC0D#/ MTCLKB#/MTIOC4B#/ GTIOC2A/GTIOC2A#/ TMO1/POE0#	SCK5/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		

Table 1.6 List of Pins and Pin Functions (52-Pin LQFP) (2/3)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
23		P95	MTIOC1B/MTIOC2A/ MTIOC4A/MTIOC1B#/ MTIOC2A#/MTIOC4A#/ GTIOC1A/GTIOC1A#	CTS12#/RTS12#/SS12#		
24		P94	MTIOC1A/MTIOC2B/ MTIOC3B/MTIOC1A#/ MTIOC2B#/MTIOC3B#/ GTIOC0A/GTIOC0A#	CTS5#/RTS5#/SS5#/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12	IRQ4	
25		P93	MTIOC0C/MTIOC2B/ MTCLKA/MTIOC0C#/ MTIOC2B#/MTCLKA#/ GTIOC1B/GTIOC1B#/TMO1	RXD12/SMISO12/SSCL12/RXDX12	IRQ1	ADTRG1#
26		P92	MTIOC0B/MTIOC1A/ MTIOC0B#/MTIOC1A#/ GTIOC1A/GTIOC1A#/TMRI1	SCK5/SCK12	IRQ0	ADTRG0#
27	CACREF	P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMRI2	RXD12/SMISO12/SSCL12/RXDX12		
28		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC1B#/ TMCI2/POE8#	SCK12		
29		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC0B#/TMO2	CTS6#/RTS6#/SS6#/CTS12#/RTS12#/ SS12#		
30		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMRI3	SCK6		
31		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC1A#	RXD1/SMISO1/SSCL1	IRQ7	
32		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#	TXD1/SMOSI1/SSDA1	IRQ6	
33		P70	GTCPPO0/POE0#	SCK1	IRQ5	
34		P33	MTIOC3A/MTCLKA/ MTIOC0C/MTIOC3A#/ MTCLKA#/MTIOC0C#			
35		P31	MTIOC4A/MTIOC4A#/ GTIOC0B/GTIOC1A/ GTIOC0B#/GTIOC1A#/ TMCI3	TXD6/SMOSI6/SSDA6/SDA0*1		
36		P26	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#/TMO3	RXD6/SMISO6/SSCL6/SCL0*1	IRQ1	
37	CLKOUT	P24	MTIC5U/MTIC5U#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI2	RXD5/SMISO5/SSCL5	IRQ3	COMP0
38	CACREF	P23	MTIC5V/MTCLKA/MTIC5V#/ MTCLKA#/GTIOC2A/ GTADSM0/GTIOC2A#/ TMO2	TXD5/SMOSI5/SSDA5	IRQ4	ADSS0/COMP1
39		P22	MTIC5W/MTCLKB/ MTIC5W#/MTCLKB#/ GTADSM1/TMRI2	SCK5	IRQ2	ADSS1/COMP2/ PGAOUT0
40		P47				AN007/PGAGND
41		P46	GTADSM0			AN006/ADSS0/ CMPC13
42		P45				AN005
43		P44	GTADSM1			AN004/ADSS1/DA0/ CMPC03/CVREFC0
44		P43				AN003
45		P42				AN002/CMPC20/ CMPC21/PGAIN02
46		P41				AN001/CMPC10/ CMPC11/PGAIN01
47		P40				AN000/CMPC00/ CMPC01/PGAIN00
48	VREFH0	P14			IRQ6	AN106/ADST0/CMPC22
49	VREFL0	P13			IRQ4	AN105/CMPC12

Table 1.6 List of Pins and Pin Functions (52-Pin LQFP) (3/3)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
50		P11	MTIOC3A/MTCLKC/ MTIOC4C/MTIOC3A#/ MTCLKC#/MTIOC4C#/ TMO3/TMO2/POE8#	CTS1#/RTS1#/SS1#/TXD6/SMOSI6/ SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12	IRQ1	AN102/CMPC02
51		P10	MTCLKD/MTCLKD#/TMRI3/ TMO1		IRQ0	AN103
52		P04	MTIOC1A/MTIOC1A#/ GTIOC2A/GTIOC2A#/ TMCI3/TMO0			ADSS1

Note 1. This pin is not 5-V tolerant. For the input voltages of the 5-V tolerant and non-5-V tolerant pins, see the input voltage column in Recommended Operating Conditions (1) under section 2, Electrical Characteristics.

1.6.3 48-pin LFQFP, 48-pin HWQFN

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
1	VCL					
2	MD/FINED	PG7		CTS5#/RTS5#/SS5#/SCK6/SCK12		ADST0
3	RES#					
4	XTAL	P37	POE11#	TXD6/SMOSI6/SSDA6/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12	IRQ0	ADSS1
5	VSS					
6	EXTAL	P36	MTIOC0A/MTIOC4A/MTIOC1A/ MTIOC0A#/MTIOC4A#/MTIOC1A#/ GTIOC0A/GTCPPO0/GTIOC0A#/ POE12#	RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12	IRQ3	ADST1
7	VCC					
8		PE2	GTETRGA/TMCI1/TMRI0/POE10#		IRQ0/ NMI	
9		PD6	MTIOC0D/MTIOC4D/MTIOC0D#/ MTIOC4D#/GTIOC2B/GTIOC2B#/ TMO1	CTS1#/RTS1#/SS1#	IRQ5	ADST0
10		PD5	MTIOC0C/MTIOC4C/MTIOC0C#/ MTIOC4C#/GTIOC2A/GTIOC2A#/ TMRI0	RXD1/SMISO1/SSCL1	IRQ3	ADSS0
11		PD4	MTIOC0B/MTIOC4B/MTIOC0B#/ MTIOC4B#/GTIOC1B/GTIOC1B#/ TMCI0	SCK1	IRQ2	
12		PD3	MTIOC0A/MTIOC4A/MTIOC0A#/ MTIOC4A#/GTIOC1A/GTIOC1A#/ TMO0	TXD1/SMOSI1/SSDA1		
13		PB6	MTIOC3C/MTCLKD/MTIOC2B/ MTIOC3C#/MTCLKD#/MTIOC2B#/ GTIOC2B/GTCPPO0/GTIOC2B#/ TMCI0/POE11#	RXD5/SMISO5/SSCL5/RXD1/ SMISO1/SSCL1	IRQ5	ADSS0
14		PB5	MTIOC1B/MTIOC3A/MTIOC2A/ MTIOC1B#/MTIOC3A#/MTIOC2A#/ GTIOC1A/GTIOC2A/GTIOC1A#/ GTIOC2A#/TMO0/POE12#	TXD5/SMOSI5/SSDA5/TXD1/ SMOSI1/SSDA1	IRQ7	ADSS1
15		PB4		RXD6/SMISO6/SSCL6		ADTRG0#
16		PB3	POE8#	TXD6/SMOSI6/SSDA6	IRQ3	ADTRG1#
17	CACREF	PB1	MTIOC0A/MTIOC4D/MTIOC0A#/ MTIOC4D#/GTIOC2B/GTIOC2B#	SCK5/SCK12	IRQ2	
18		PB0	MTIOC0B/MTCLKC/MTIOC4C/ MTIOC0B#/MTCLKC#/MTIOC4C#/ GTIOC1B/GTADSM0/GTIOC1B#/ TMRI1	TXD5/SMOSI5/SSDA5/SCK1/SDA0		ADSM0
19		P97	MTIOC0C/MTCLKA/MTIOC3D/ MTIOC0C#/MTCLKA#/MTIOC3D#/ GTIOC0B/GTADSM1/GTIOC0B#/ GTETRGA/TMCI1	RXD5/SMISO5/SSCL5/SCL0	IRQ2	ADSM1
20	CLKOUT	P96	MTIOC0D/MTCLKB/MTIOC4B/ MTIOC0D#/MTCLKB#/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMO1/POE0#	SCK5/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		
21		P95	MTIOC1B/MTIOC2A/MTIOC4A/ MTIOC1B#/MTIOC2A#/MTIOC4A#/ GTIOC1A/GTIOC1A#	CTS12#/RTS12#/SS12#		
22		P94	MTIOC1A/MTIOC2B/MTIOC3B/ MTIOC1A#/MTIOC2B#/MTIOC3B#/ GTIOC0A/GTIOC0A#	CTS5#/RTS5#/SS5#/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12	IRQ4	
23		P93	MTIOC0C/MTIOC2B/MTCLKA/ MTIOC0C#/MTIOC2B#/MTCLKA#/ GTIOC1B/GTIOC1B#/TMO1	RXD12/SMISO12/SSCL12/RXDX12	IRQ1	ADTRG1#
24		P92	MTIOC0B/MTIOC1A/MTIOC0B#/ MTIOC1A#/GTIOC1A/GTIOC1A#/ TMRI1	SCK5/SCK12	IRQ0	ADTRG0#
25	CACREF	P76	MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#/TMRI2	RXD12/SMISO12/SSCL12/RXDX12		

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
26		P75	MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#/TMCI2/POE8#	SCK12		
27		P74	MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#/TMO2	CTS6#/RTS6#/SS6#/CTS12#/ RTS12#/SS12#		
28		P73	MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#/TMRI3	SCK6		
29		P72	MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	RXD1/SMISO1/SSCL1	IRQ7	
30		P71	MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	TXD1/SMOSI1/SSDA1	IRQ6	
31		P70	GTCPPO0/POE0#	SCK1	IRQ5	
32		P31	MTIOC4A/MTIOC4A#/GTIOC0B/ GTIOC1A/GTIOC0B#/GTIOC1A#/ TMCI3	TXD6/SMOSI6/SSDA6/SDA0*1		
33		P26	MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#/TMO3	RXD6/SMISO6/SSCL6/SCL0*1	IRQ1	
34	CLKOUT	P24	MTIC5U/MTIC5U#/GTIOC2B/ GTCPPO0/GTIOC2B#/TMCI2	RXD5/SMISO5/SSCL5	IRQ3	COMP0
35	CACREF	P23	MTIC5V/MTCLKA/MTIC5V#/ MTCLKA#/GTIOC2A/GTADSM0/ GTIOC2A#/TMO2	TXD5/SMOSI5/SSDA5	IRQ4	ADSS0/ COMP1
36		P22	MTIC5W/MTCLKB/MTIC5W#/ MTCLKB#/GTADSM1/TMRI2	SCK5	IRQ2	ADSS1/ COMP2/ PGAOUT0
37		P47				AN007/ PGAGND
38		P46	GTADSM0			AN006/ ADSS0/ CMPC13
39		P45				AN005
40		P44	GTADSM1			AN004/ ADSS1/DA0/ CMPC03/ CVREFC0
41		P43				AN003
42		P42				AN002/ CMPC20/ CMPC21/ PGAIN02
43		P41				AN001/ CMPC10/ CMPC11/ PGAIN01
44		P40				AN000/ CMPC00/ CMPC01/ PGAIN00
45	VREFH0	P14			IRQ6	AN106/ADST0/ CMPC22
46	VREFL0	P13			IRQ4	AN105/ CMPC12
47		P11	MTIOC3A/MTCLKC/MTIOC4C/ MTIOC3A#/MTCLKC#/MTIOC4C#/ TMO3/TMO2/POE8#	CTS1#/RTS1#/SS1#/TXD6/SMOSI6/ SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12	IRQ1	AN102/ CMPC02
48		P10	MTCLKD/MTCLKD#/TMRI3/TMO1		IRQ0	AN103

Note 1. This pin is not 5-V tolerant. For the input voltages of the 5-V tolerant and non-5-V tolerant pins, see the input voltage column in Recommended Operating Conditions (1) under section 2, Electrical Characteristics.

1.6.4 44-pin LQFP

Table 1.8 List of Pins and Pin Functions (44-Pin LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
1	VCL					
2	MD/FINED	PG7		CTS5#/RTS5#/SS5#/SCK6/SCK12		ADST0
3	RES#					
4	VSS					
5	EXTAL	P36	MTIOC0A/MTIOC4A/ MTIOC1A/MTIOC0A#/ MTIOC4A#/MTIOC1A#/ GTIOC0A/GTCPPO0/ GTIOC0A#/POE12#	RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12	IRQ3	ADST1
6	VCC					
7		PE2	GTETRGA/TMCI1/TMRI0/ POE10#		IRQ0/ NMI	
8		PD6	MTIOC0D/MTIOC4D/ MTIOC0D#/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMO1	CTS1#/RTS1#/SS1#	IRQ5	ADST0
9		PD5	MTIOC0C/MTIOC4C/ MTIOC0C#/MTIOC4C#/ GTIOC2A/GTIOC2A#/TMRI0	RXD1/SMISO1/SSCL1	IRQ3	ADSS0
10		PD4	MTIOC0B/MTIOC4B/ MTIOC0B#/MTIOC4B#/ GTIOC1B/GTIOC1B#/TMCI0	SCK1	IRQ2	
11		PD3	MTIOC0A/MTIOC4A/ MTIOC0A#/MTIOC4A#/ GTIOC1A/GTIOC1A#/TMO0	TXD1/SMOSI1/SSDA1		
12		PB6	MTIOC3C/MTCLKD/ MTIOC2B/MTIOC3C#/ MTCLKD#/MTIOC2B#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI0/POE11#	RXD5/SMISO5/SSCL5/RXD1/SMISO1/ SSCL1	IRQ5	ADSS0
13		PB5	MTIOC1B/MTIOC3A/ MTIOC2A/MTIOC1B#/ MTIOC3A#/MTIOC2A#/ GTIOC1A/GTIOC2A/ GTIOC1A#/GTIOC2A#/ TMO0/POE12#	TXD5/SMOSI5/SSDA5/TXD1/SMOSI1/ SSDA1	IRQ7	ADSS1
14		PB3	POE8#	TXD6/SMOSI6/SSDA6	IRQ3	ADTRG1#
15	CACREF	PB1	MTIOC0A/MTIOC4D/ MTIOC0A#/MTIOC4D#/ GTIOC2B/GTIOC2B#	SCK5/SCK12	IRQ2	
16		PB0	MTIOC0B/MTCLKC/ MTIOC4C/MTIOC0B#/ MTCLKC#/MTIOC4C#/ GTIOC1B/GTADSM0/ GTIOC1B#/TMRI1	TXD5/SMOSI5/SSDA5/SCK1/SDA0		ADSM0
17		P97	MTIOC0C/MTCLKA/ MTIOC3D/MTIOC0C#/ MTCLKA#/MTIOC3D#/ GTIOC0B/GTADSM1/ GTIOC0B#/GTETRGA/ TMCI1	RXD5/SMISO5/SSCL5/SCL0	IRQ2	ADSM1
18	CLKOUT	P96	MTIOC0D/MTCLKB/ MTIOC4B/MTIOC0D#/ MTCLKB#/MTIOC4B#/ GTIOC2A/GTIOC2A#/ TMO1/POE0#	SCK5/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		
19		P95	MTIOC1B/MTIOC2A/ MTIOC4A/MTIOC1B#/ MTIOC2A#/MTIOC4A#/ GTIOC1A/GTIOC1A#	CTS12#/RTS12#/SS12#		
20		P94	MTIOC1A/MTIOC2B/ MTIOC3B/MTIOC1A#/ MTIOC2B#/MTIOC3B#/ GTIOC0A/GTIOC0A#	CTS5#/RTS5#/SS5#/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12	IRQ4	

Table 1.8 List of Pins and Pin Functions (44-Pin LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
21		P93	MTIOC0C/MTIOC2B/ MTCLKA/MTIOC0C#/ MTIOC2B#/MTCLKA#/ GTIOC1B/GTIOC1B#/TMO1	RXD12/SMISO12/SSCL12/RXDX12	IRQ1	ADTRG1#
22		P92	MTIOC0B/MTIOC1A/ MTIOC0B#/MTIOC1A#/ GTIOC1A/GTIOC1A#/TMRI1	SCK5/SCK12	IRQ0	ADTRG0#
23	CACREF	P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMRI2	RXD12/SMISO12/SSCL12/RXDX12		
24		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC1B#/ TMCI2/POE8#	SCK12		
25		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC0B#/TMO2	CTS6#/RTS6#/SS6#/CTS12#/RTS12#/ SS12#		
26		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMRI3	SCK6		
27		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC1A#	RXD1/SMISO1/SSCL1	IRQ7	
28		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#	TXD1/SMOSI1/SSDA1	IRQ6	
29		P31	MTIOC4A/MTIOC4A#/ GTIOC0B/GTIOC1A/ GTIOC0B#/GTIOC1A#/ TMCI3	TXD6/SMOSI6/SSDA6/SDA0*1		
30		P26	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#/TMO3	RXD6/SMISO6/SSCL6/SCL0*1	IRQ1	
31	CLKOUT	P24	MTIC5U/MTIC5U#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI2	RXD5/SMISO5/SSCL5	IRQ3	COMP0
32	CACREF	P23	MTIC5V/MTCLKA/MTIC5V#/ MTCLKA#/GTIOC2A/ GTADSM0/GTIOC2A#/ TMO2	TXD5/SMOSI5/SSDA5	IRQ4	ADSS0/COMP1
33		P22	MTIC5W/MTCLKB/ MTIC5W#/MTCLKB#/ GTADSM1/TMRI2	SCK5	IRQ2	ADSS1/COMP2/ PGAOUT0
34		P47				AN007/PGAGND
35		P46	GTADSM0			AN006/ADSS0/ CMPC13
36		P44	GTADSM1			AN004/ADSS1/DA0/ CMPC03/CVREFC0
37		P43				AN003
38		P42				AN002/CMPC20/ CMPC21/PGAIN02
39		P41				AN001/CMPC10/ CMPC11/PGAIN01
40		P40				AN000/CMPC00/ CMPC01/PGAIN00
41	VREFH0	P14			IRQ6	AN106/ADST0/CMPC22
42	VREFL0	P13			IRQ4	AN105/CMPC12
43		P11	MTIOC3A/MTCLKC/ MTIOC4C/MTIOC3A#/ MTCLKC#/MTIOC4C#/ TMO3/TMO2/POE8#	CTS1#/RTS1#/SS1#/TXD6/SMOSI6/ SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12	IRQ1	AN102/CMPC02
44		P10	MTCLKD/MTCLKD#/TMRI3/ TMO1		IRQ0	AN103

Note 1. This pin is not 5-V tolerant. For the input voltages of the 5-V tolerant and non-5-V tolerant pins, see the input voltage column in Recommended Operating Conditions (1) under section 2, Electrical Characteristics.

1.6.5 32-pin LQFP, 32-pin HWQFN

Table 1.9 List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
1	VCL					
2	MD/FINED	PG7		CTS5#/RTS5#/SS5#/SCK6/SCK12		ADST0
3	RES#					
4	XTAL	P37	POE11#	TXD6/SMOSI6/SSDA6/TXD12/ SMOSI12/SSDA12/TXDX12/ SIOX12	IRQ0	ADSS1
5	VSS					
6	EXTAL	P36	MTIOC0A/MTIOC4A/ MTIOC1A/MTIOC0A#/ MTIOC4A#/MTIOC1A#/ GTIOC0A/GTCPPO0/ GTIOC0A#/POE12#	RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12	IRQ3	ADST1
7	VCC					
8		PE2	GTETRGA/TMCI1/TMRI0/ POE10#		IRQ0/ NMI	
9		PB6	MTIOC3C/MTCLKD/ MTIOC2B/MTIOC3C#/ MTCLKD#/MTIOC2B#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI0/POE11#	RXD5/SMISO5/SSCL5/RXD1/ SMISO1/SSCL1	IRQ5	ADSS0
10		PB5	MTIOC1B/MTIOC3A/ MTIOC2A/MTIOC1B#/ MTIOC3A#/MTIOC2A#/ GTIOC1A/GTIOC2A/ GTIOC1A#/GTIOC2A#/ TMO0/POE12#	TXD5/SMOSI5/SSDA5/TXD1/ SMOSI1/SSDA1	IRQ7	ADSS1
11	CACREF	PB1	MTIOC0A/MTIOC4D/ MTIOC0A#/MTIOC4D#/ GTIOC2B/GTIOC2B#	SCK5/SCK12	IRQ2	
12		PB0	MTIOC0B/MTCLKC/ MTIOC4C/MTIOC0B#/ MTCLKC#/MTIOC4C#/ GTIOC1B/GTADSM0/ GTIOC1B#/TMRI1	TXD5/SMOSI5/SSDA5/SCK1/SDA0		ADSM0
13		P97	MTIOC0C/MTCLKA/ MTIOC3D/MTIOC0C#/ MTCLKA#/MTIOC3D#/ GTIOC0B/GTADSM1/ GTIOC0B#/GTETRGA/TMCI1	RXD5/SMISO5/SSCL5/SCL0	IRQ2	ADSM1
14	CLKOUT	P96	MTIOC0D/MTCLKB/ MTIOC4B/MTIOC0D#/ MTCLKB#/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMO1/ POE0#	SCK5/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		
15		P93	MTIOC0C/MTIOC2B/ MTCLKA/MTIOC0C#/ MTIOC2B#/MTCLKA#/ GTIOC1B/GTIOC1B#/TMO1	RXD12/SMISO12/SSCL12/RXDX12	IRQ1	ADTRG1#
16		P92	MTIOC0B/MTIOC1A/ MTIOC0B#/MTIOC1A#/ GTIOC1A/GTIOC1A#/TMRI1	SCK5/SCK12	IRQ0	ADTRG0#
17	CACREF	P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMRI2	RXD12/SMISO12/SSCL12/RXDX12		
18		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC1B#/TMCI2/ POE8#	SCK12		
19		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC0B#/TMO2	CTS6#/RTS6#/SS6#/CTS12#/ RTS12#/SS12#		
20		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMRI3	SCK6		
21		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC1A#	RXD1/SMISO1/SSCL1	IRQ7	
22		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#	TXD1/SMOSI1/SSDA1	IRQ6	

Table 1.9 List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
23		P31	MTIOC4A/MTIOC4A#/ GTIOC0B/GTIOC1A/ GTIOC0B#/GTIOC1A#/ TMCI3	TXD6/SMOSI6/SSDA6/SDA0*1		
24		P26	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#/TMO3	RXD6/SMISO6/SSCL6/SCL0*1	IRQ1	
25		P46	GTADSM0			AN006/ADSS0/ CMPC13
26		P44	GTADSM1			AN004/ADSS1/DA0/ CMPC03/CVREFC0
27		P42				AN002/CMPC20/ CMPC21/PGAIN02
28		P41				AN001/CMPC10/ CMPC11/PGAIN01
29		P40				AN000/CMPC00/ CMPC01/PGAIN00
30	VREFH0	P14			IRQ6	AN106/ADST0/CMPC22
31	VREFL0	P13			IRQ4	AN105/CMPC12
32		P11	MTIOC3A/MTCLKC/ MTIOC4C/MTIOC3A#/ MTCLKC#/MTIOC4C#/TMO3/ TMO2/POE8#	CTS1#/RTS1#/SS1#/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12	IRQ1	AN102/CMPC02

Note 1. This pin is not 5-V tolerant. For the input voltages of the 5-V tolerant and non-5-V tolerant pins, see the input voltage column in Recommended Operating Conditions (1) under section 2, Electrical Characteristics.

1.6.6 24-pin HWQFN

Table 1.10 List of Pins and Pin Functions (24-Pin HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
1	VCL					
2	MD/FINED	PG7		CTS5#/RTS5#/SS5#/SCK6/SCK12		ADST0
3	RES#					
4	VSS					
5	EXTAL	P36	MTIOC0A/MTIOC4A/ MTIOC1A/MTIOC0A#/ MTIOC4A#/MTIOC1A#/ GTIOC0A/GTCPPO0/ GTIOC0A#/POE12#	RXD6/SMISO6/SSCL6/RXD12/ SMISO12/SSCL12/RXDX12	IRQ3	ADST1
6	VCC					
7		PE2	GTETRGA/TMCI1/TMRI0/ POE10#		IRQ0/ NMI	
8		PB6	MTIOC3C/MTCLKD/ MTIOC2B/MTIOC3C#/ MTCLKD#/MTIOC2B#/ GTIOC2B/GTCPPO0/ GTIOC2B#/TMCI0/POE11#	RXD5/SMISO5/SSCL5/RXD1/ SMISO1/SSCL1	IRQ5	ADSS0
9		PB5	MTIOC1B/MTIOC3A/ MTIOC2A/MTIOC1B#/ MTIOC3A#/MTIOC2A#/ GTIOC1A/GTIOC2A/ GTIOC1A#/GTIOC2A#/ TMO0/POE12#	TXD5/SMOSI5/SSDA5/TXD1/ SMOSI1/SSDA1	IRQ7	ADSS1
10		PB0	MTIOC0B/MTCLKC/ MTIOC4C/MTIOC0B#/ MTCLKC#/MTIOC4C#/ GTIOC1B/GTADSM0/ GTIOC1B#/TMRI1	TXD5/SMOSI5/SSDA5/SCK1/SDA0		ADSM0
11		P97	MTIOC0C/MTCLKA/ MTIOC3D/MTIOC0C#/ MTCLKA#/MTIOC3D#/ GTIOC0B/GTADSM1/ GTIOC0B#/GTETRGA/TMCI1	RXD5/SMISO5/SSCL5/SCL0	IRQ2	ADSM1
12	CLKOUT	P96	MTIOC0D/MTCLKB/ MTIOC4B/MTIOC0D#/ MTCLKB#/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMO1/ POE0#	SCK5/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		
13	CACREF	P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC2B#/TMRI2	RXD12/SMISO12/SSCL12/RXDX12		
14		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC1B#/TMCI2/ POE8#	SCK12		
15		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC0B#/TMO2	CTS6#/RTS6#/SS6#/CTS12#/ RTS12#/SS12#		
16		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC2A#/TMRI3	SCK6		
17		P31	MTIOC4A/MTIOC4A#/ GTIOC0B/GTIOC1A/ GTIOC0B#/GTIOC1A#/ TMCI3	TXD6/SMOSI6/SSDA6/SDA0*1		
18		P26	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC0A#/TMO3	RXD6/SMISO6/SSCL6/SCL0*1	IRQ1	
19		P42				AN002/CMPC20/ CMPC21/PGAIN02
20		P41				AN001/CMPC10/ CMPC11/PGAIN01
21		P40				AN000/CMPC00/ CMPC01/PGAIN00
22	VREFH0	P14			IRQ6	AN106/ADST0/CMPC22
23	VREFL0	P13			IRQ4	AN105/CMPC12

Table 1.10 List of Pins and Pin Functions (24-Pin HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control, Others	I/O Port	Timers (MTU, GPTW, TMR, POEG)	Communications (SCI, RIIC)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC, PGA)
24		P11	MTIOC3A/MTCLKC/ MTIOC4C/MTIOC3A#/ MTCLKC#/MTIOC4C#/TMO3/ TMO2/POE8#	CTS1#/RTS1#/SS1#/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12	IRQ1	AN102/CMPC02

Note 1. This pin is not 5-V tolerant. For the input voltages of the 5-V tolerant and non-5-V tolerant pins, see the input voltage column in Recommended Operating Conditions (1) under section 2, Electrical Characteristics.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	5-V tolerant pins: P97, PB0	V_{in}	–0.3 to +6.5	V
	Pins other than above		–0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	–0.3 to VCC + 0.3	V
Output sink current	Per pin	I_{IO}	–16	mA
	Total of all pins (T_j = –40 to 125°C)	ΣI_{IO}	–164	mA
	Total of all pins (T_j = –40 to 140°C)		–97	mA
Output source current	Per pin	I_{IO}	16	mA
	Total of all pins (T_j = –40 to 125°C)	ΣI_{IO}	76	mA
	Total of all pins (T_j = –40 to 140°C)		45	mA
Junction temperature		T_j	–40 to +140	°C
Storage temperature		T_{stg}	–65 to +150	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 2.15.1, Connecting VCL Capacitor and Bypass Capacitors.
Do not input signals or an I/O pull-up power supply to pins other than 5-V tolerant pins while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant pins, it will not cause problems such as damage to the MCU.

2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltages		VCC	2.7	—	5.5	V
		VSS	—	0	—	
Reference power supply voltages		VREFH0	2.7	—	VCC	V
		VREFL0	—	0	—	
Input voltage	Ports for 5 V tolerant: P97, PB0	V_{in}	–0.3	—	5.8	V
	PGAGND		—	0	—	
	Ports other than above		–0.3	—	VCC + 0.3	
Operating temperature	G version	T_{opr}	–40	—	105	°C
	M version		–40	—	125	
Junction temperature	G version	T_j	–40	—	125	°C
	M version		–40	—	140	

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance for stabilizing the internal voltage	C_{VCL}	4.7µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 4.7 µF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

2.3 Test Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.
Supported peripheral functions and pins differ from one product name to another.
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = 2.7 to 5.5 V
- VREFH0 = 2.7 V to VCC
- VSS = VREFL0 = 0 V
- $T_a = T_{opr} = –40$ to 125°C

Unless otherwise specified, typical values are those measured at room temperature of 25°C, and when VCC = VREFH0 = 5.0 V.
Figure 2.1 shows the timing conditions.

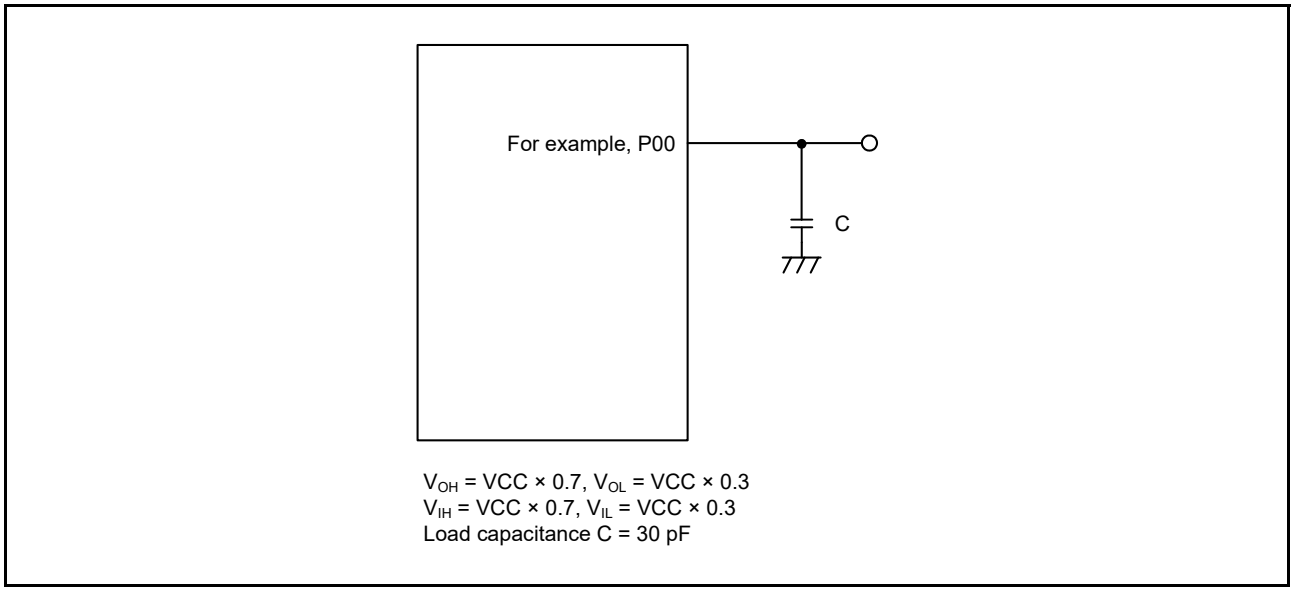


Figure 2.1 Input or Output Timing Measurement Conditions

2.4 DC Characteristics

2.4.1 Characteristics of the Input and Output Pins

Table 2.4 I/O Input Voltage Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pins (P97, PB0) (except for SMBus)	V_{IH}	0.7 × VCC	—	—	V	
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	RIIC input pins (P26, P31) (except for SMBus)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.1 × VCC	—	—		
	IRQ input pin, MTU input pin, GPTW input pin, POE3 input pin, POEG input pin, TMR input pin, SCI input pin, CAC input pin, ADTRG# input pin, RES#, NMI, MD	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.1 × VCC	—	—		
Input level voltage (except for schmitt trigger input pins)	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
	RIIC input pins (P97, PB0, P26, P31) (SMBus)	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
			2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
			—	—	0.5		VCC = 2.7 to 3.6 V
	General input pins other than those above	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		

Table 2.5 I/O Input Leakage Current

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, PE2	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC

Table 2.6 I/O Three-state Leakage Current

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Three-state leakage current (off-state)	P97, PB0	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V, 5.8 V
	P13, P14		—	—	1.0		V_{in} = 0 V, VCC
	Other than above		—	—	0.2		V_{in} = 0 V, VCC

Table 2.7 I/O Input Capacitance

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input capacitance	PE2	C_{in}	—	—	30	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Other than above		—	—	15		

Table 2.8 I/O Input Pull-up Resistor

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for PE2)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 2.9 I/O Output Voltage Characteristics

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	RIIC pins	P97, PB0	V_{OL}	—	0.6	V	I_{OL} = 6.0 mA
		P26, P31		—	0.5		I_{OL} = 2.0 mA
	Ports other than above			—	0.5		I_{OL} = 2.0 mA
High-level output voltage	All output ports		V_{OH}	VCC – 0.5	—	V	I_{OH} = –2.0 mA

Table 2.10 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = 3.3 V, VSS = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.02	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.05	—		I_{OH} = –1.0 mA
			—	VCC – 0.10	—		I_{OH} = –2.0 mA
			—	VCC – 0.22	—		I_{OH} = –4.0 mA

Table 2.11 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = 5.0 V, VSS = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.02	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.04	—		I_{OH} = –1.0 mA
			—	VCC – 0.08	—		I_{OH} = –2.0 mA
			—	VCC – 0.15	—		I_{OH} = –4.0 mA

Table 2.12 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = 3.3 V, VSS = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.04	—		I_{OL} = 2.0 mA
			—	0.08	—		I_{OL} = 4.0 mA
			—	0.17	—		I_{OL} = 8.0 mA

Table 2.13 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = 5.0 V, VSS = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.01	—		I_{OL} = 1.0 mA
			—	0.03	—		I_{OL} = 2.0 mA
			—	0.06	—		I_{OL} = 4.0 mA
			—	0.12	—		I_{OL} = 8.0 mA

2.4.2 Operating and Standby Currents

Table 2.14 Operating Current in the High-Speed Operating Mode*1 (1/3)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Normal operating mode	Supply of the clock signal to the peripheral modules is stopped.	T_a = 25°C	I_{CC}	2.4	—	mA	ICLK = 48 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		1.8	—		ICLK = 32 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		1.5	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		1.0	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
	The clock signal is being supplied to the peripheral modules.	T_a = 25°C		12.8	25.3		ICLK = 48 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 48 MHz
		T_a = 85°C			25.0		
		T_a = 105°C			24.9		
		T_a = 125°C			24.6		
		T_a = 25°C		9.9	19.8		ICLK = 32 MHz Clock Source = HOCO FCLK, PCLKB = 32 MHz PCLKD = 64 MHz
		T_a = 85°C			19.6		
		T_a = 105°C			19.5		
		T_a = 125°C			19.2		
		T_a = 25°C		7.3	15.1		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 24 MHz
		T_a = 85°C			14.9		
		T_a = 105°C			14.8		
		T_a = 125°C			14.6		
		T_a = 25°C		3.7	8.6		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 8 MHz
		T_a = 85°C			8.3		
		T_a = 105°C			8.3		
		T_a = 125°C			8.2		
Sleep mode	Peripheral module clocks are stopped	T_a = 25°C		1.3	—		ICLK = 48 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		1.0	—		ICLK = 32 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		

Table 2.14 Operating Current in the High-Speed Operating Mode*1 (2/3)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Sleep mode	Peripheral module clocks are stopped	T_a = 25°C	I_{CC}	0.8	—	mA	ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.7	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
	Peripheral module clocks are supplied	T_a = 25°C		7.4	—		ICLK = 48 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 48 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		6.2	—		ICLK = 32 MHz Clock Source = HOCO FCLK, PCLKB = 32 MHz PCLKD = 64 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		4.4	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 24 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		2.6	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 8 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
Deep sleep mode	Peripheral module clocks are stopped	T_a = 25°C		0.9	—		ICLK = 48 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.7	—		ICLK = 32 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.6	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.6	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		

Table 2.14 Operating Current in the High-Speed Operating Mode*1 (3/3)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Deep sleep mode	Peripheral module clocks are supplied	T_a = 25°C	I_{CC}	6.6	—	mA	ICLK = 48 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 48 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		5.7	—		ICLK = 32 MHz Clock Source = HOCO FCLK, PCLKB = 32 MHz PCLKD = 64 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		4.0	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 24 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		2.4	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 8 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
Increase during background operation*2				2.1	—		

Note 1. Operating current values do not include output charge/discharge current from all pins. The values apply when internal pull-up resistors are in the off state.

Note 2. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution. The operating current during background operation is not included.

Table 2.15 Operating Current in Middle-Speed Operating Mode*1 (1/2)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Normal operating mode	Peripheral module clocks are stopped	T_a = 25°C	I_{CC}	1.4	—	mA	ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.9	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.2	—		ICLK = 1 MHz Clock Source = LOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
	Peripheral module clocks are supplied	T_a = 25°C		7.1	14.7		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 24 MHz
		T_a = 85°C			14.5		
		T_a = 105°C			14.4		
		T_a = 125°C			14.2		
		T_a = 25°C		3.5	8.1		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 8 MHz
		T_a = 85°C			7.9		
		T_a = 105°C			7.9		
		T_a = 125°C			7.8		
		T_a = 25°C		1.7	4.9		ICLK = 1 MHz Clock Source = LOCO FCLK, PCLKB, PCLKD = 1 MHz
		T_a = 85°C			4.7		
		T_a = 105°C			4.6		
		T_a = 125°C			4.6		
Sleep mode	Peripheral module clocks are stopped	T_a = 25°C		0.8	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.7	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.2	—		ICLK = 1 MHz Clock Source = LOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
	Peripheral module clocks are supplied	T_a = 25°C		4.4	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 24 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		2.6	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 8 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		

Table 2.15 Operating Current in Middle-Speed Operating Mode*1 (2/2)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Sleep mode	Peripheral module clocks are supplied	T_a = 25°C	I_{CC}	1.4	—	mA	ICLK = 1 MHz Clock Source = LOCO FCLK, PCLKB, PCLKD = 1 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
Deep sleep mode	Peripheral module clocks are stopped	T_a = 25°C		0.6	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.6	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		0.1	—		ICLK = 1 MHz Clock Source = LOCO FCLK, PCLKB, PCLKD = Clock Source × 1/64
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
	Peripheral module clocks are supplied	T_a = 25°C		4.0	—		ICLK = 24 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 24 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		2.4	—		ICLK = 8 MHz Clock Source = HOCO FCLK, PCLKB, PCLKD = 8 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
		T_a = 25°C		1.3	—		ICLK = 1 MHz Clock Source = LOCO FCLK, PCLKB, PCLKD = 1 MHz
		T_a = 85°C			—		
		T_a = 105°C			—		
		T_a = 125°C			—		
Increase during background operation*2				2.1	—		

Note 1. Operating current values do not include output charge/discharge current from all pins. The values apply when internal pull-up resistors are in the off state.

Note 2. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution. The operating current during background operation is not included.

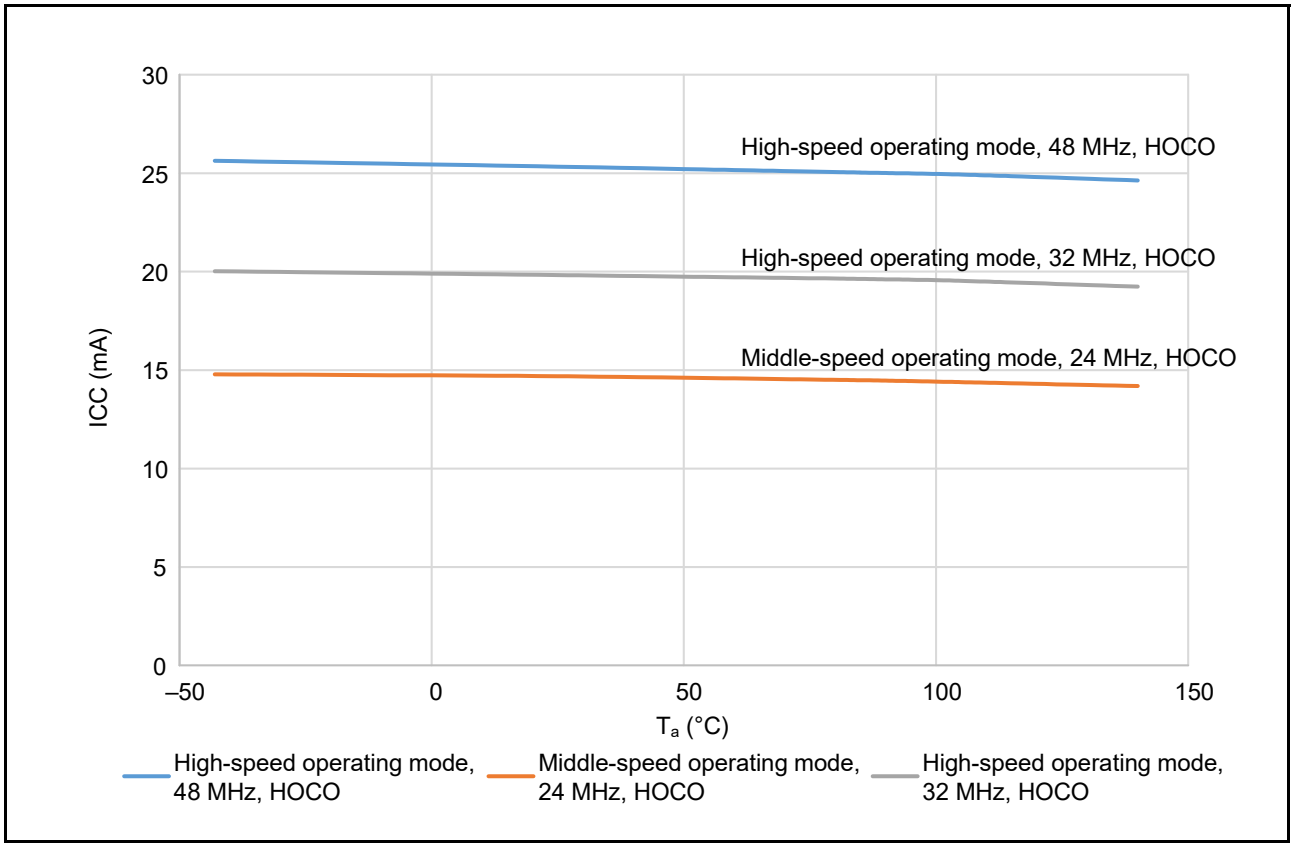
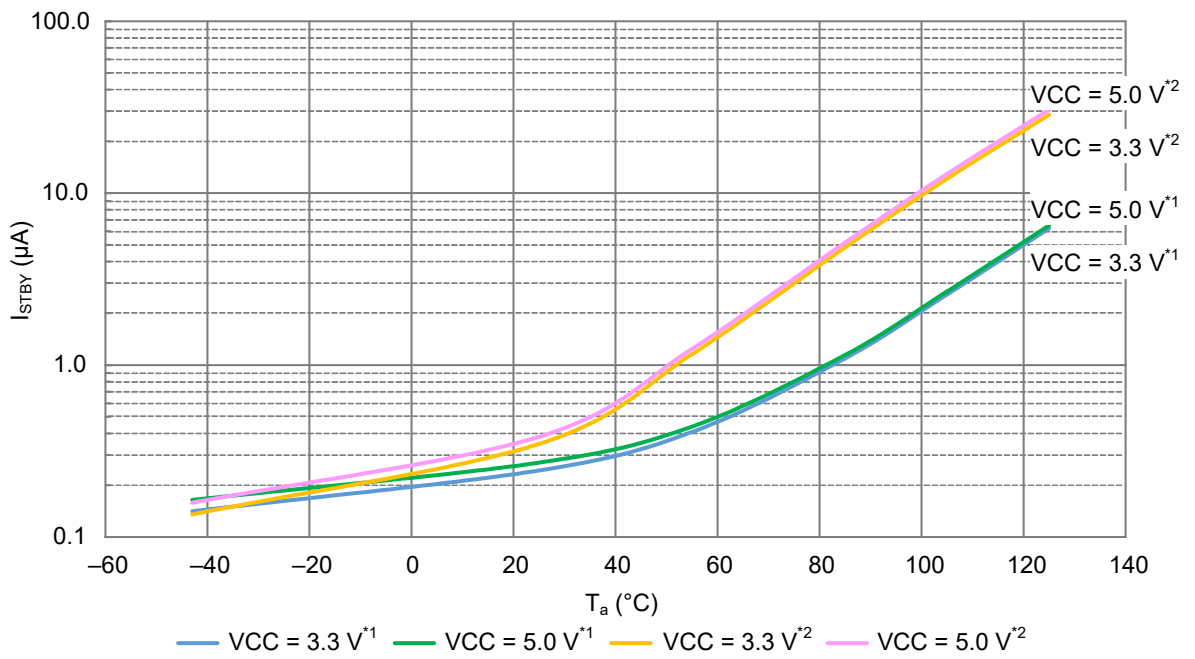


Figure 2.2 Temperature Dependence in the Normal Operating Mode

Table 2.16 Standby Current in Software Standby Mode[*1, *2]

Item		Symbol	Typ.	Max.	Unit	Test Conditions
Standby current (3.3 V)	T_a = 25°C	I_{STBY}	0.24	0.54	µA	
	T_a = 55°C		0.41	2.02		
	T_a = 85°C		1.10	8.51		
	T_a = 105°C		2.58	20.98		
	T_a = 125°C		6.24	48.36		
Standby current (5.0 V)	T_a = 25°C		0.27	0.57		
	T_a = 55°C		0.44	2.15		
	T_a = 85°C		1.15	9.02		
	T_a = 105°C		2.68	22.21		
	T_a = 125°C		6.49	51.27		

Note 1. Standby current values are with all output pins unloaded and all input pull-up resistors in the off state.
Note 2. The IWDT, LVD, and CMPC are stopped.



Note 1. This is the average of values measured for the central sample group in product evaluation.
Note 2. This is the average of values measured for the upper sample group in product evaluation.

Figure 2.3 Temperature Dependency in Software Standby Mode

Table 2.17 Operating Current by Functions

Conditions: ICLK = PCLKB = PCLKD = 48 MHz unless otherwise specified.

Item	Min.	Typ.	Max.	Unit
Voltage detection circuit (LVD0)	—	0.04	—	µA
Voltage detection circuit (LVD1, LVD2) (per channel)	—	0.12	—	
Independent watchdog timer	—	0.32	—	
Clock frequency accuracy measurement circuit	—	0.11	—	mA
Data transfer controller	—	2.50	—	
Multi-function timer pulse unit 3	—	1.32	—	
Port output enable 3	—	0.14	—	
General PWM timer	—	0.69	—	
GPTW port output enable	—	0.05	—	
8-bit timer (per unit)	—	0.06	—	
Compare match timer	—	0.05	—	
Serial communications interface (per unit)	—	0.41	—	
I^2C-bus interface	—	0.20	—	
CRC calculator	—	0.08	—	
Arithmetic unit for trigonometric functions	—	0.33	—	
12-bit A/D converter (per unit)*1	—	1.39	1.73	
12-bit A/D converter reference (per unit)*1	—	0.11	0.13	
Programmable gain amplifier	—	0.42	0.80	
D/A converter (per unit)	—	0.35	0.53	
Temperature sensor	—	0.12	—	
Comparator C (per unit)	—	0.09	0.17	
Data operation circuit	—	0.09	—	

Note 1. This applies when PCLKD = 64 MHz.

2.4.3 VCC Rising Gradient and Ripple Characteristics

Table 2.18 VCC Rising Gradient

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

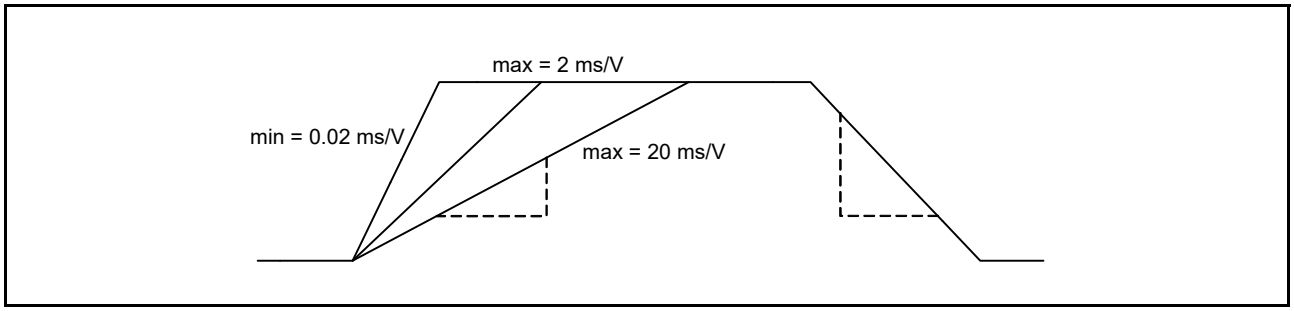


Figure 2.4 VCC Ramp Rate at Power-On

Table 2.19 Ripple Characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 2.5 $V_{r\,(VCC)} \leq 0.2 \times VCC$
		—	—	1	MHz	Figure 2.5 $V_{r\,(VCC)} \leq 0.08 \times VCC$
		—	—	10	MHz	Figure 2.5 $V_{r\,(VCC)} \leq 0.06 \times VCC$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

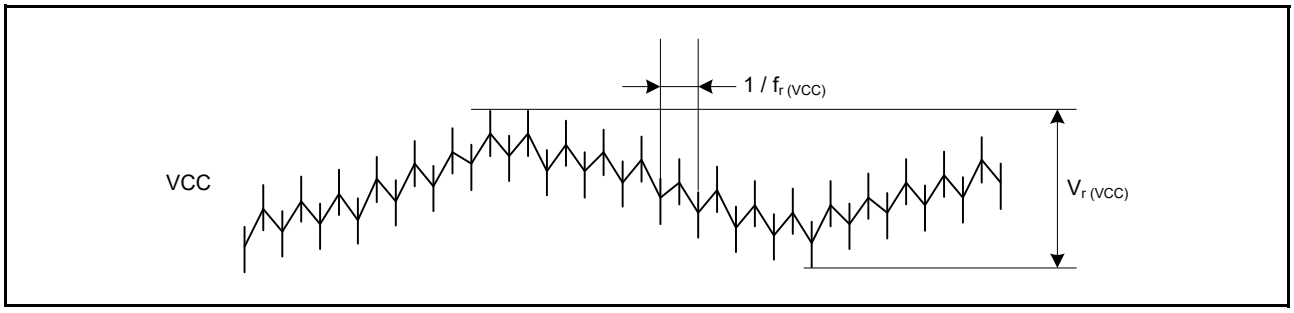


Figure 2.5 Ripple Waveform

2.4.4 Voltage of the VCL Pin

Table 2.20 Voltage of the VCL Pin

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage of the VCL pin	V_{CL}	—	1.5	—	V	

2.4.5 RAM Data Standby Characteristics

Table 2.21 RAM Data Standby Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	2.7	—	—	V	

2.4.6 Thermal Resistance Value (Reference Values)

Table 2.22 Thermal Resistance Value (Reference Values)

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal resistance	64-pin LFQFP (PLQP0064KB-C)	θja	—	—	53.7	°C/W	JESD51-2 and JESD51-7 compliant
	64-pin LQFP (PLQP0064GA-A)		—	—	53.3		
	52-pin LQFP (PLQP0052JA-A)		—	—	45.7		
	48-pin LFQFP (PLQP0048KB-B)		—	—	64		
	44-pin LQFP (PLQP0044GF-A)		—	—	53		
	32-pin LQFP (PLQP0032GB-A)		—	—	63.2		
	48-pin HWQFN (PWQN0048KC-A)		—	—	28.7*1		
	32-pin HWQFN (PWQN0032KE-A)		—	—	35.8*1		
	24-pin HWQFN (PWQN0024KG-A)		—	—	43.6*1		
	64-pin LFQFP (PLQP0064KB-C)	Ψjt	—	—	2.02		
	64-pin LQFP (PLQP0064GA-A)		—	—	2.02		
	52-pin LQFP (PLQP0052JA-A)		—	—	1.89		
	48-pin LFQFP (PLQP0048KB-B)		—	—	5.01		
	44-pin LQFP (PLQP0044GF-A)		—	—	2.02		
	32-pin LQFP (PLQP0032GB-A)		—	—	5.13		
	48-pin HWQFN (PWQN0048KC-A)		—	—	0.21*1		
	32-pin HWQFN (PWQN0032KE-A)		—	—	0.3*1		
	24-pin HWQFN (PWQN0024KG-A)		—	—	0.43*1		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the exposed die pad for this purpose is connected to VSS.

2.5 AC Characteristics

2.5.1 Clock Timing

Table 2.23 Operating Frequency Value (High-Speed Operating Mode)

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency	System clock (ICLK)	f	—	—	48	MHz
	FlashIF clock (FCLK)*1, *2		—	—	48	
	Peripheral module clock (PCLKB)		—	—	48	
	Peripheral module clock (PCLKD)		1	—	64	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 2.24 Operating Frequency Value (Middle-Speed Operating Mode)

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency	System clock (ICLK)	f	—	—	24	MHz
	FlashIF clock (FCLK)*1, *2		—	—	24	
	Peripheral module clock (PCLKB)		—	—	24	
	Peripheral module clock (PCLKD)		1	—	24	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 2.25 EXTAL Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.6
EXTAL external clock input frequency	f_{XMAIN}	—	—	20	MHz	
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

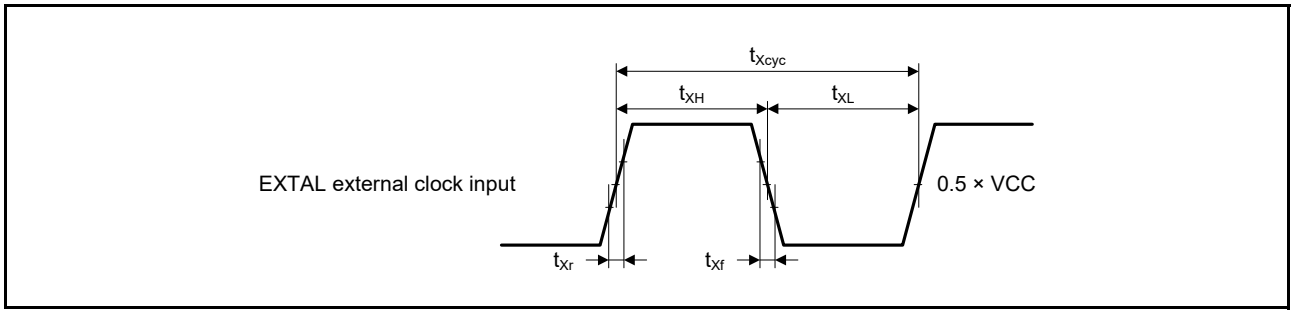


Figure 2.6 EXTAL External Clock Input Timing

Table 2.26 Main Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*1	$t_{MAINOSC}$	—	3	—	ms	Figure 2.7
Main clock oscillation stabilization time (ceramic resonator)*1	$t_{MAINOSC}$	—	50	—	µs	

Note 1. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

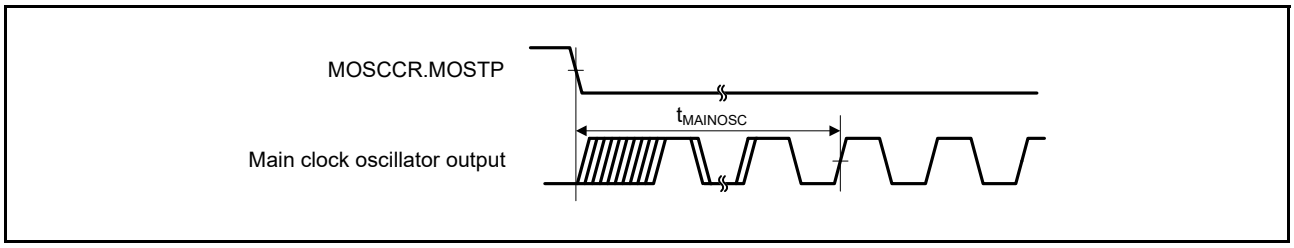


Figure 2.7 Main Clock Oscillation Start Timing

Table 2.27 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock oscillation frequency	f_{LOCO}	3.44 (–14%)	4.0	4.56 (+14%)	MHz	
LOCO clock oscillation frequency error	Δf_{LOCO}	—	—	±14	%	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	µs	Figure 2.8
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75 (–15%)	15	17.25 (+15%)	kHz	
IWDT-dedicated clock oscillation frequency error	Δf_{ILOCO}	—	—	±15	%	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	80	µs	Figure 2.9

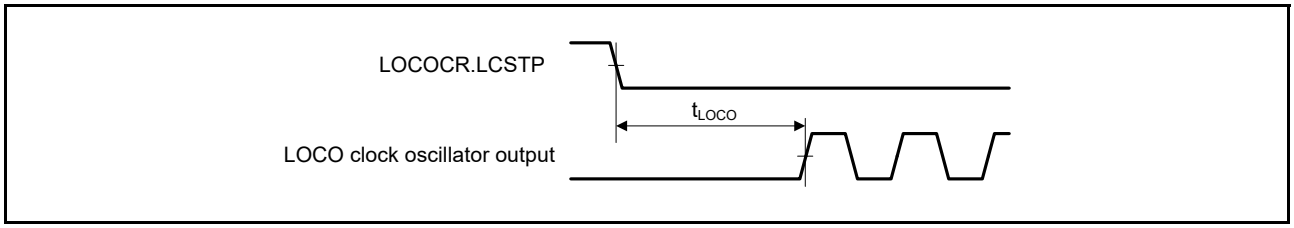


Figure 2.8 LOCO Clock Oscillation Start Timing

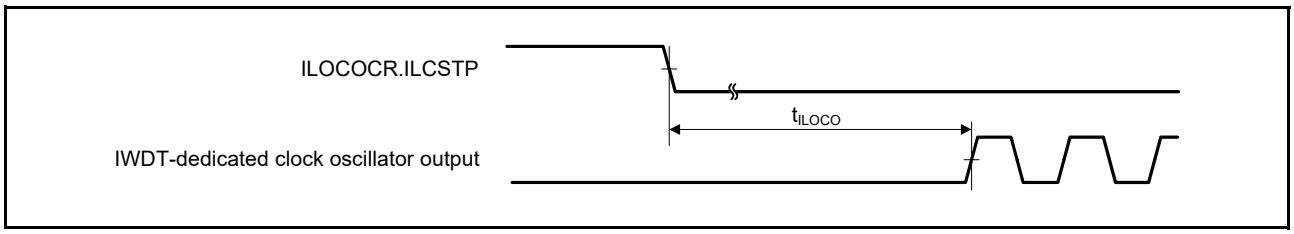


Figure 2.9 IWDT-Dedicated Clock Oscillation Start Timing

Table 2.28 HOCO Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	23.76 (–1.0%)	24	24.24 (+1.0%)	MHz	T_a = –40 to +125°C
		31.68 (–1.0%)	32	32.32 (+1.0%)		
		47.52 (–1.0%)	48	48.48 (+1.0%)		
		63.36 (–1.0%)	64	64.64 (+1.0%)		
HOCO oscillation frequency error	Δf_{HOCO}	—	—	±1.0	%	T_a = –40 to +125°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	4.95	μs	Figure 2.11

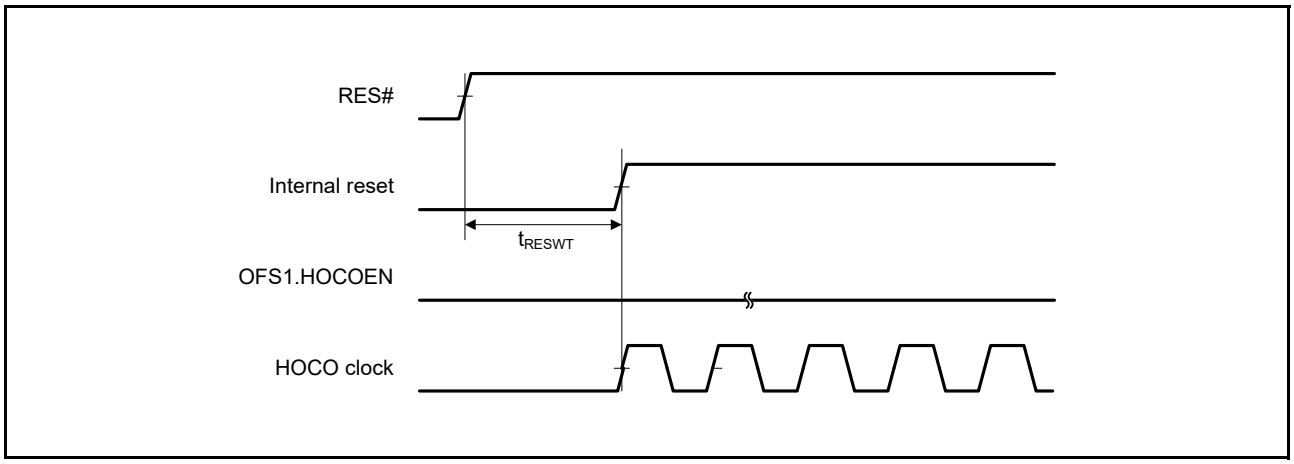


Figure 2.10 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

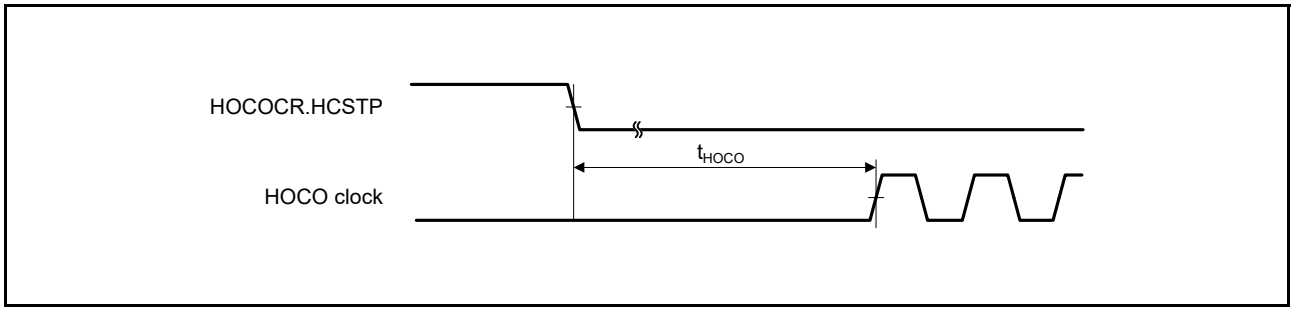


Figure 2.11 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

Table 2.29 PLL Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL input frequency	f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency	f_{PLL}	24	—	64	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	81.4	µs	Figure 2.12
PLL free-running oscillation frequency	f_{PLLFR}	—	9	—	MHz	

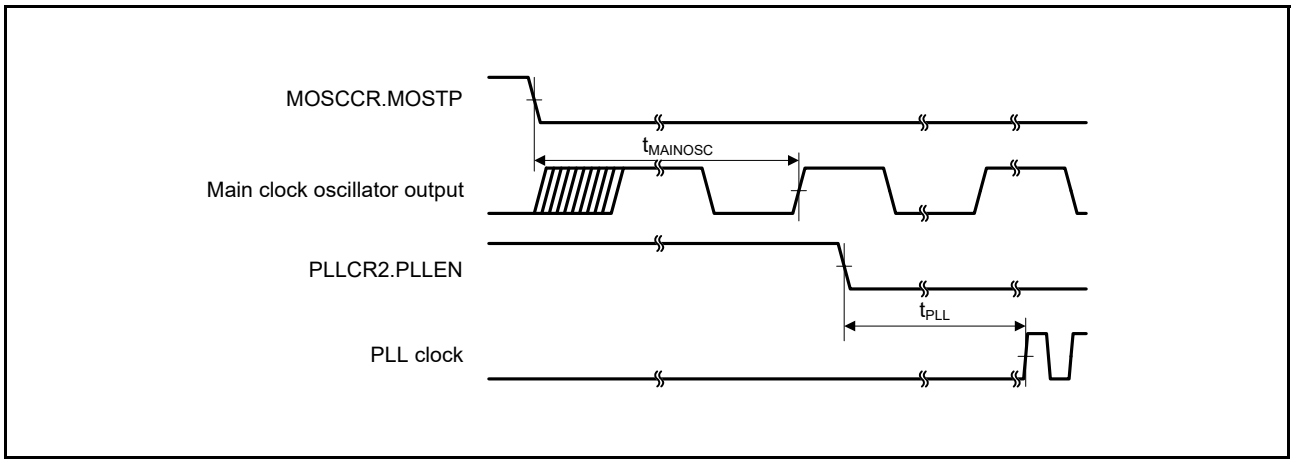


Figure 2.12 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

2.5.2 Reset Timing

Table 2.30 Reset Timing

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	10.5	—	—	ms	Figure 2.13
	Other than above	t_{RESW}	30	—	—	μs	Figure 2.14
Wait time after RES# cancellation (cold start)	At normal startup*1	t_{RESWT}	—	27.5	—	ms	Figure 2.13
	During fast startup time*2	t_{RESWT}	—	850	—	μs	
	Voltage monitoring 0 reset enabled at startup*4, *5	t_{RESWT}	—	850	—	μs	
Wait time after RES# cancellation (warm start)	LVD0 disabled*3	t_{RESWT}					Figure 2.14
	LVD0 enabled*4		—	850	—	μs	
Internal reset time (independent watchdog timer reset, software reset)	LVD0 disabled*3	t_{RESWT2}	—	190	—	μs	
	LVD0 enabled*4		—	910	—	μs	

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 1.
Note 4. When OFS1.LVDAS = 0.
Note 5. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

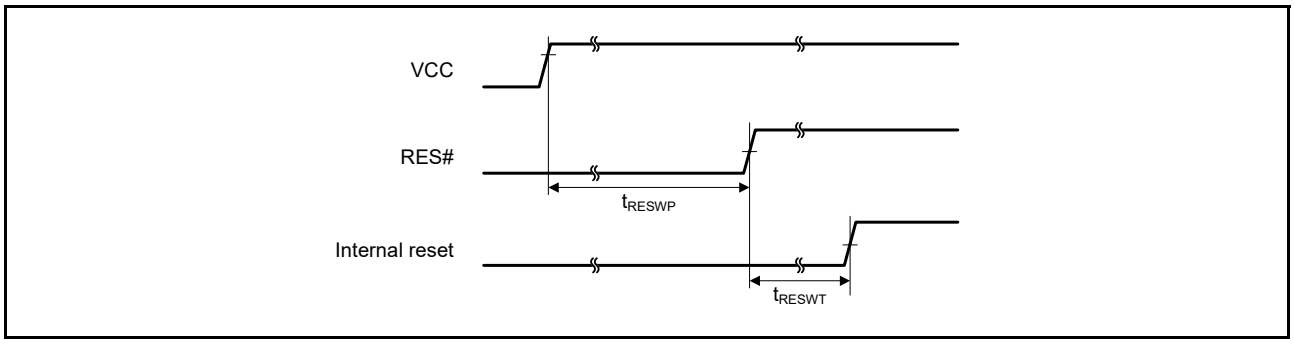


Figure 2.13 Reset Input Timing at Power-On

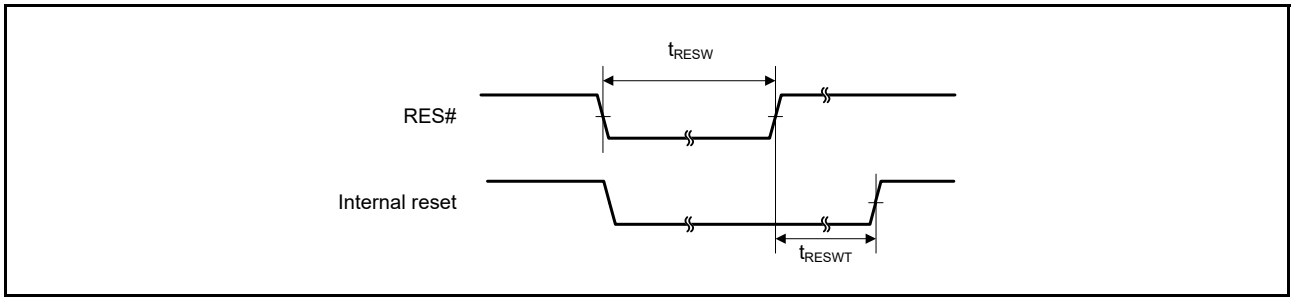


Figure 2.14 Reset Input Timing

2.5.3 Timing of Recovery from Low Power Consumption Modes

Table 2.31 Timing of Recovery from Low Power Consumption Modes (1)

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator	$t_{SBYOSCWTMC}$	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 3 / f_{MOSC} + 1 / f_{ICLK}	μs	
		PLL circuit (Main clock oscillator)	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (280 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 3 / f_{PLL} + 1 / f_{ICLK}		
		HOCO	$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 3 / f_{HOCO} + 1 / f_{ICLK}		
		PLL circuit (HOCO)	$t_{SBYOSCWTPH}$	—	—	t_{LOCO} + 296 / f_{LOCO} + 3 / f_{PLL} + 1 / f_{ICLK}		
		LOCO	$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2			t_{SBYSEQ}	—	—	4 / f_{LOCO} + 11 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*3	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator	t_{SBYMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 2.15
		PLL circuit (Main clock oscillator)	t_{SBYPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
		HOCO	t_{SBYHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
		PLL circuit (HOCO)	t_{SBYPH}	—	—	$t_{SBYOSCWTPH}$ + t_{SBYSEQ}		
		LOCO	t_{SBYLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.

Note 2. For n, the largest value is selected from among the internal clock division settings. The source clock is specified by the SCKCR3.CKSEL bits.

Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

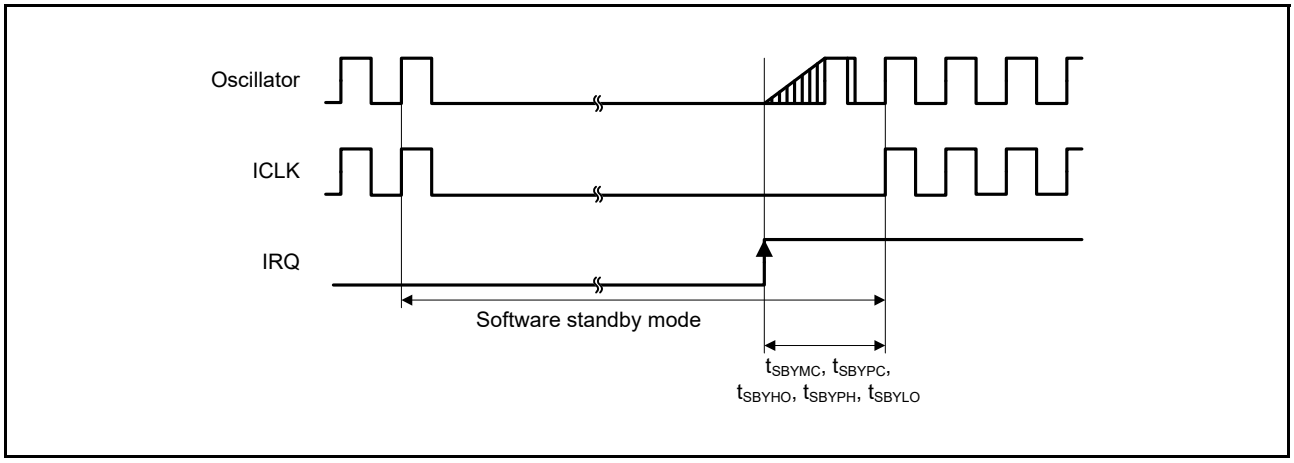


Figure 2.15 Software Standby Mode Recovery Timing

Table 2.32 Timing of Recovery from Low Power Consumption Modes (5)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1, *2	High-speed operating mode	t_{DSLP}	—	—	4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / $f_{source\ clock}$	µs	Figure 2.16
	Middle-speed operating mode						

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. For n, the largest value is selected from among the internal clock division settings. The source clock is specified by the SCKCR3.CKSEL bits.

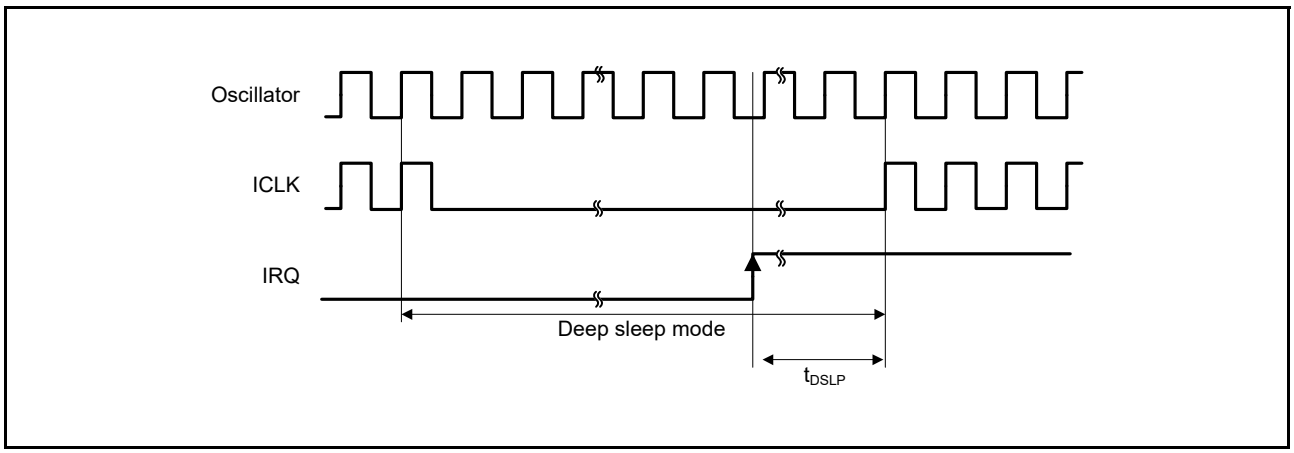


Figure 2.16 Deep Sleep Mode Recovery Timing

Table 2.33 Operating Mode Transition Time

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating mode	24 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	µs
Middle-speed operating mode	High-speed operating mode	24 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	

2.5.4 Control Signal Timing

Table 2.34 Control Signal Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{PBcyc} \times 2 \le 200$ ns
		$t_{PBcyc} \times 2$*1	—	—			$t_{PBcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{PBcyc} \times 2 \le 200$ ns
		$t_{PBcyc} \times 2$*1	—	—			$t_{PBcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{PBcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

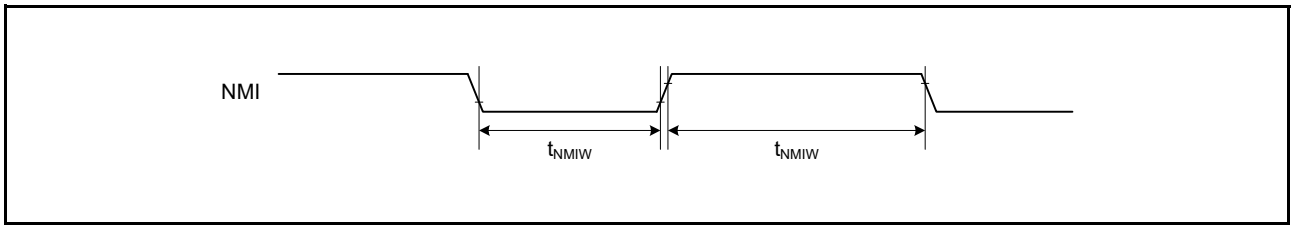


Figure 2.17 NMI Interrupt Input Timing

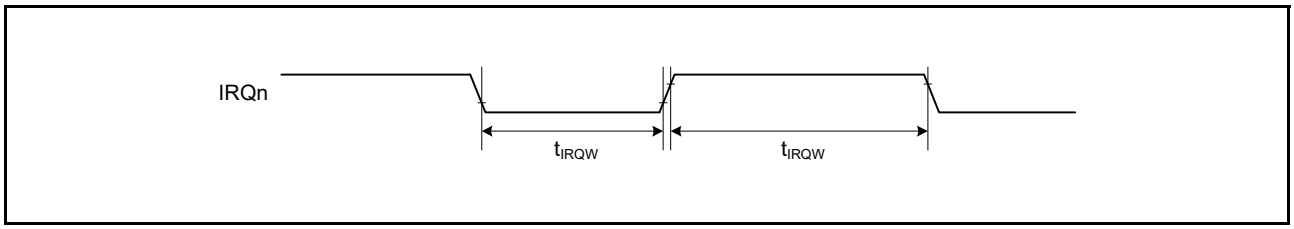


Figure 2.18 IRQ Interrupt Input Timing

2.5.5 Timing of On-Chip Peripheral Modules

2.5.5.1 I/O Port Input Timing

Table 2.35 I/O Port Input Timing

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.19

Note 1. t_{PBcyc}: PCLKB cycle

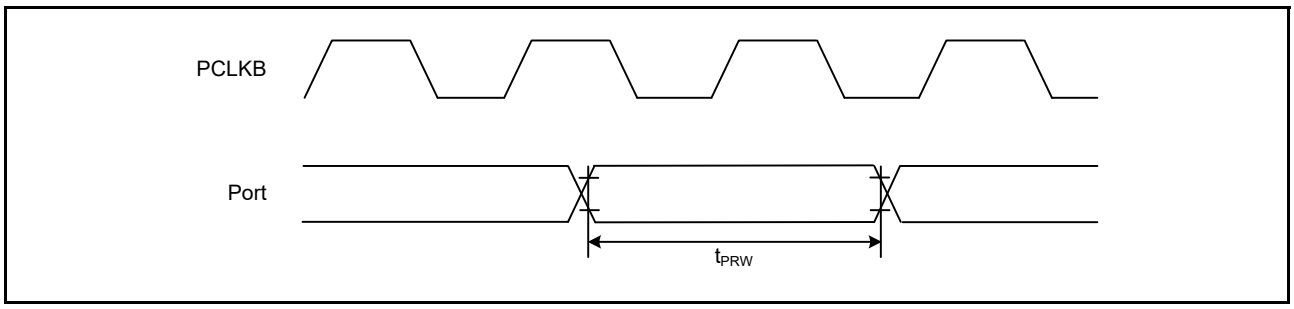


Figure 2.19 I/O Port Input Timing

2.5.5.2 MTU

Table 2.36 MTU Timing

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PBcyc}	Figure 2.20
		Both-edge setting		2.5	—		
	Input capture input rise/fall time		t_{TICr}, t_{TICf}	—	0.1	μs/V	
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PBcyc}	Figure 2.21
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
	Timer clock rise/fall time		t_{TCKr}, t_{TCKf}	—	0.1	μs/V	

Note 1. t_{PBcyc}: PCLKB cycle

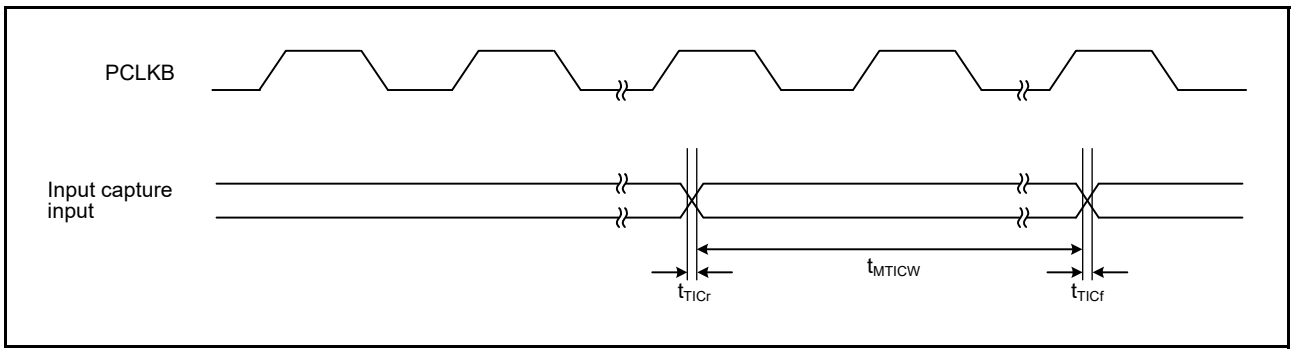


Figure 2.20 MTU Input/Output Timing

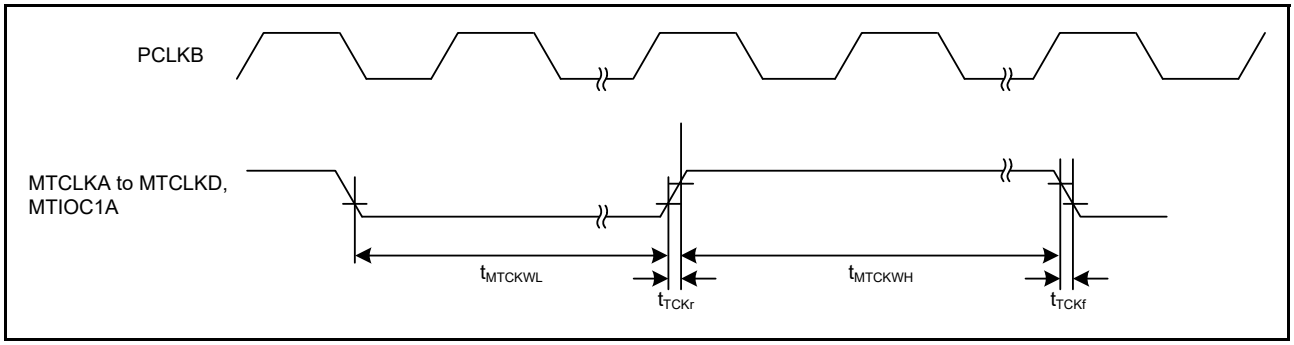


Figure 2.21 MTU Clock Input Timing

2.5.5.3 POE

Table 2.37 POE Timing

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{PBcyc}	Figure 2.22
	POE# input rise/fall time		t_{POEr}, t_{POEf}	—	0.1	μs/V	
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	5 × t_{PBcyc} + 0.24	μs	Figure 2.23 When detecting falling edges (ICSRm.POEnM[3:0] = 0000 (m = 1, 3 to 5, 7, n = 0, 8, 10 to 12))
		Simultaneous conduction of output pins	t_{POEDO}	—	3 × t_{PBcyc} + 0.2		Figure 2.24
		Detection of comparator outputs	t_{POEDC}	—	5 × t_{PBcyc} + 0.2		Figure 2.25 The time is that when the noise filter for comparator C is not in use (CMPCTL.NFE = 0) and excludes the time for detection by comparator C.
		Register setting	t_{POEDS}	—	t_{PBcyc} + 0.2		Figure 2.26 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	8		Figure 2.27

Note 1. t_{PBcyc}: PCLKB cycle

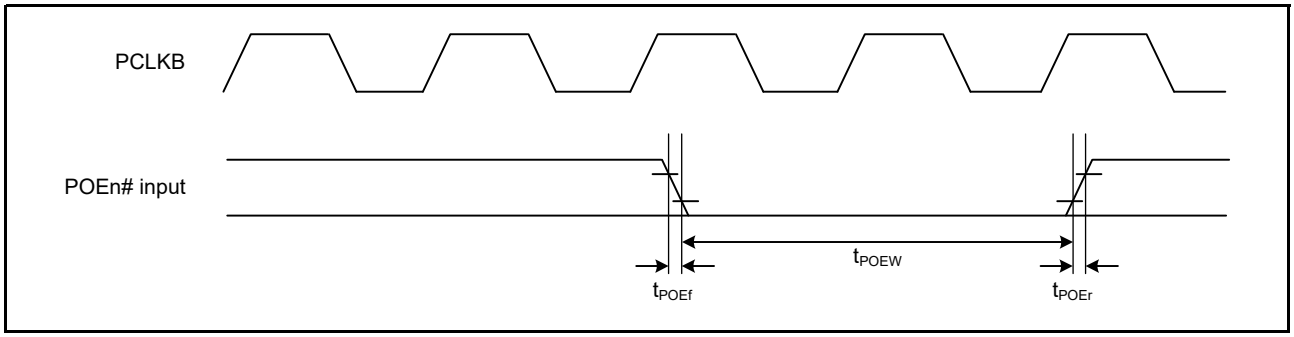


Figure 2.22 POE# Input Timing (n = 0, 8, 10 to 12)

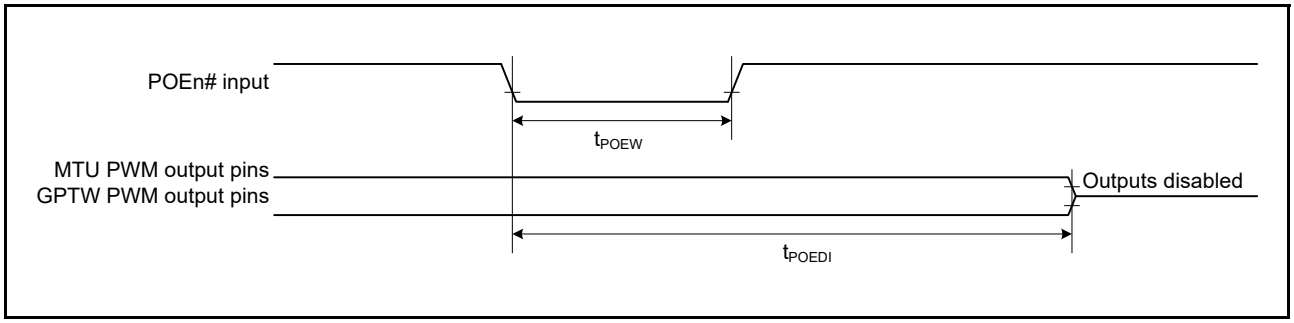
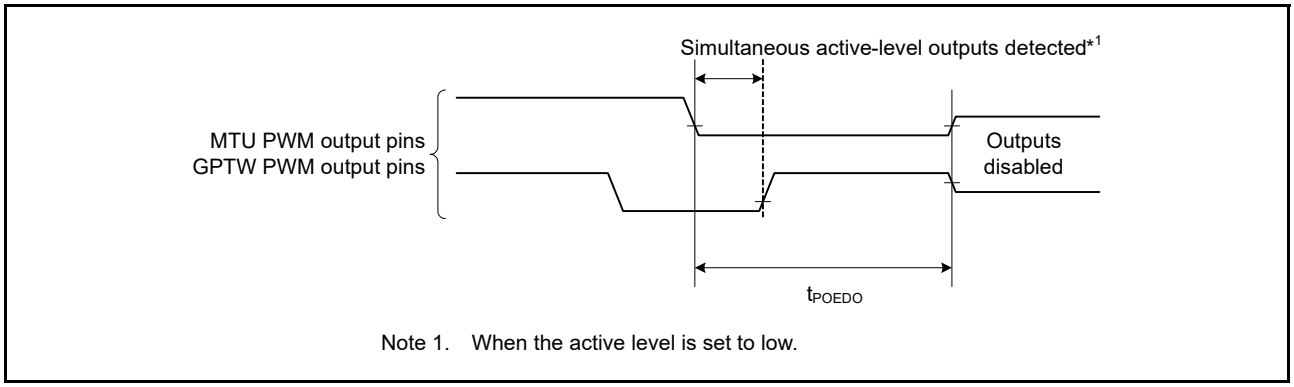


Figure 2.23 Output Disable Time for POE in Response to Transition of the POEn# Signal Level (n = 0, 8, 10 to 12)



Note 1. When the active level is set to low.

Figure 2.24 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

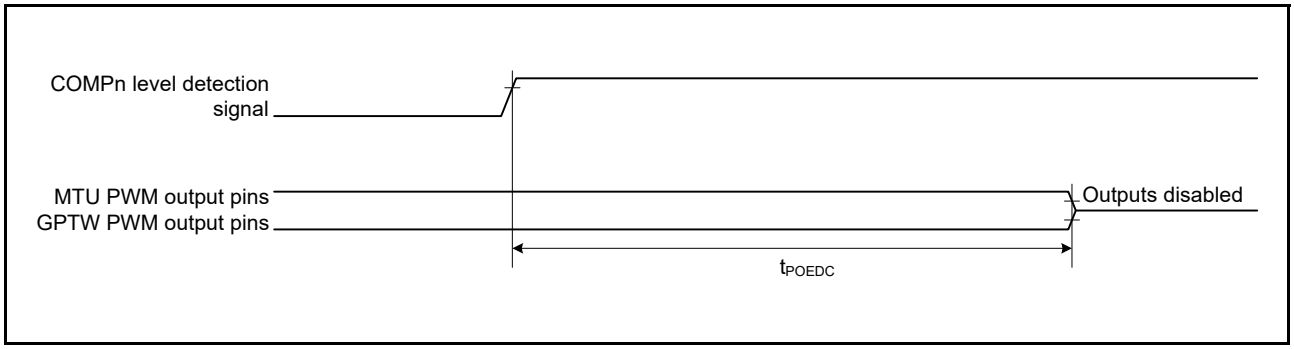


Figure 2.25 Output Disable Time for POE in Response to Detection of the Comparator Outputs (n = 0 to 2)

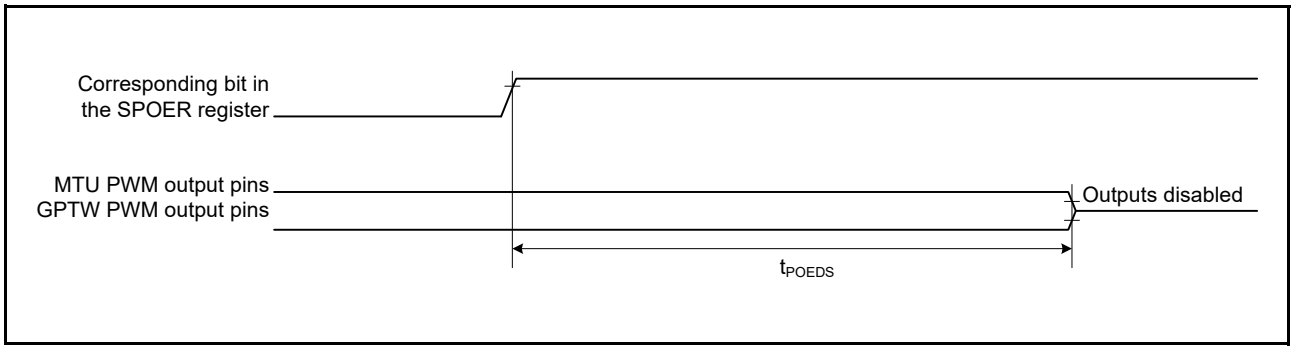


Figure 2.26 Output Disable Time for POE in Response to the Register Setting

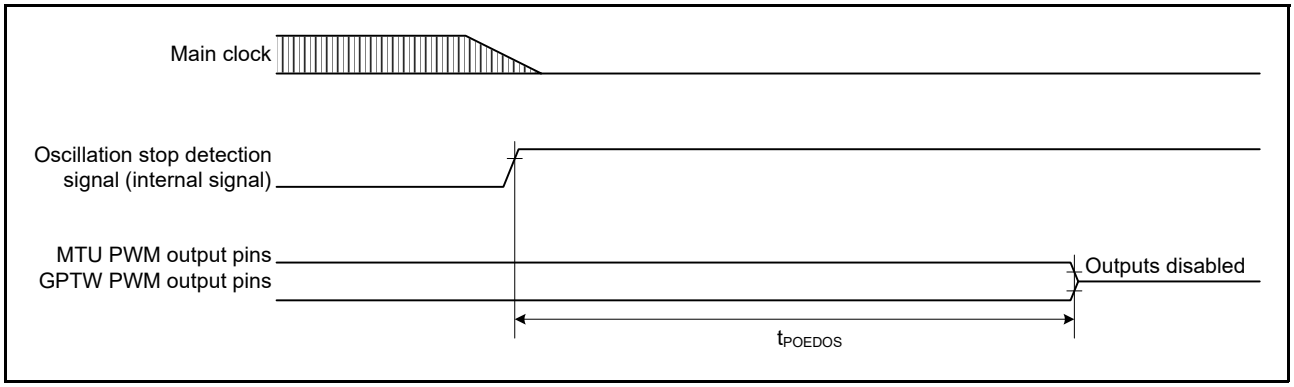


Figure 2.27 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.5.5.4 POEG

Table 2.38 POEG Timing

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
POEG	GTETRGn input pulse width (n = A)		t_{POEGW}	1.5	—	t_{PBcyc}	Figure 2.28
	GTETRGA input rise/fall time		t_{POEGr}, t_{POEGf}	—	0.1	µs	
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	3 × t_{PBcyc} + 0.34	µs	Figure 2.29 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A))
		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	0.5	µs	Figure 2.30
		Edge detection signal from a comparator	t_{POEGDC}	—	4 × t_{PBcyc} + 0.5	µs	Figure 2.31 The time is that when the noise filter for comparator C is not in use (CMPCTL.NFE = 0) and excludes the time for detection by comparator C.
		Register setting	t_{POEGDS}	—	t_{PBcyc} + 0.3	µs	Figure 2.32 Time for access to the register is not included.
		Oscillation stop detection	$t_{POEGDOS}$	—	8	µs	Figure 2.33
		Input level detection of the GTETRGn pin (direct path)	$t_{POEGDDI}$	—	3 × t_{PBcyc} + 0.34	µs	Figure 2.34
		Level detection signal from a comparator	$t_{POEGDDC}$	—	t_{PBcyc} + 0.3	µs	Figure 2.35 The time is that when the noise filter for comparator C is not in use (CMPCTL.NFE = 0) and excludes the time for detection by comparator C.

Note 1. t_{PBcyc}: PCLKB cycle

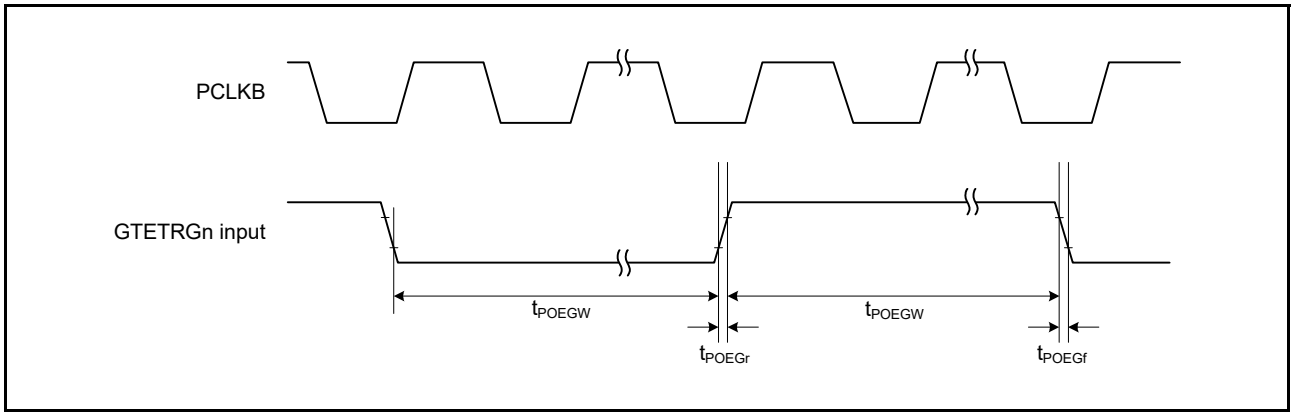


Figure 2.28 POEG Input Timing (n = A)

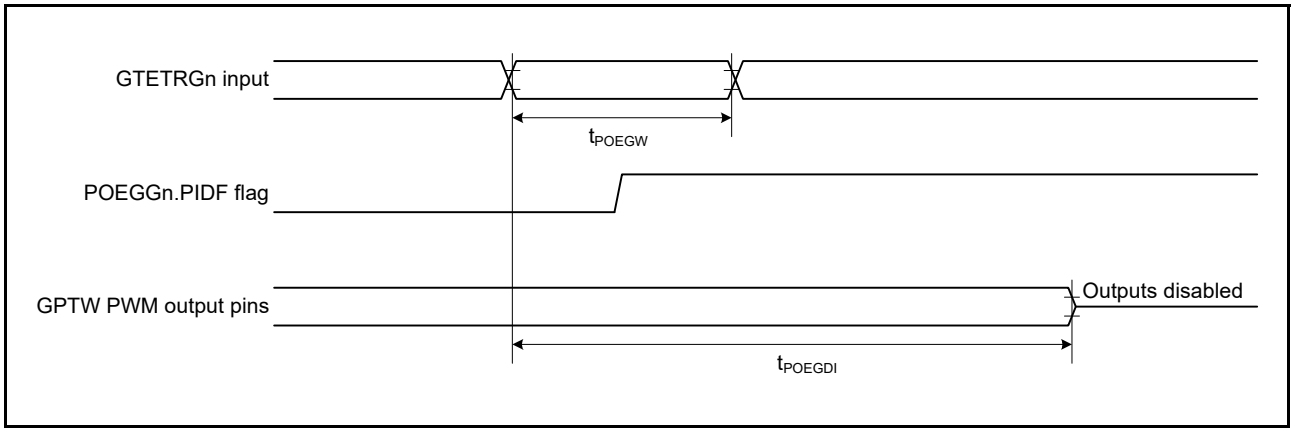
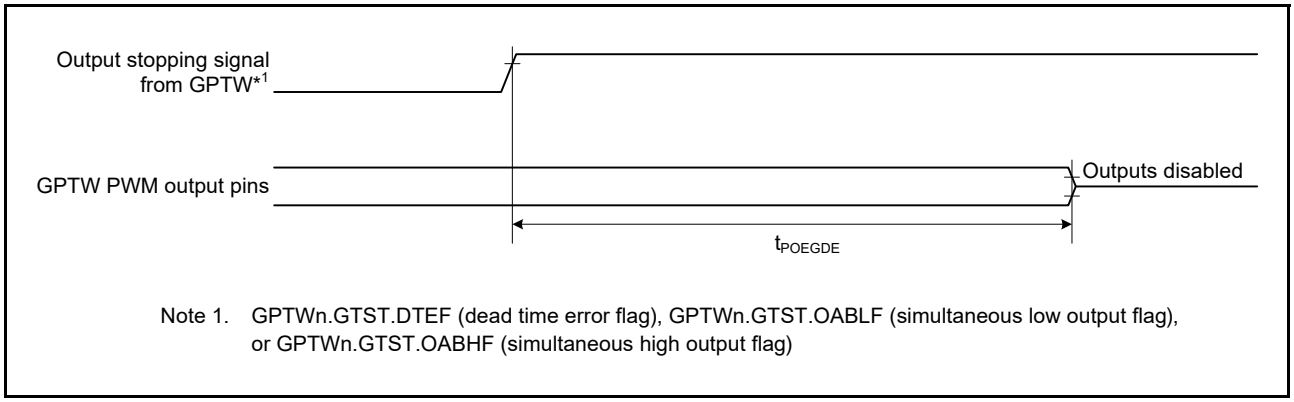


Figure 2.29 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin (n = A)



Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

Figure 2.30 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW (n = 0 to 2)

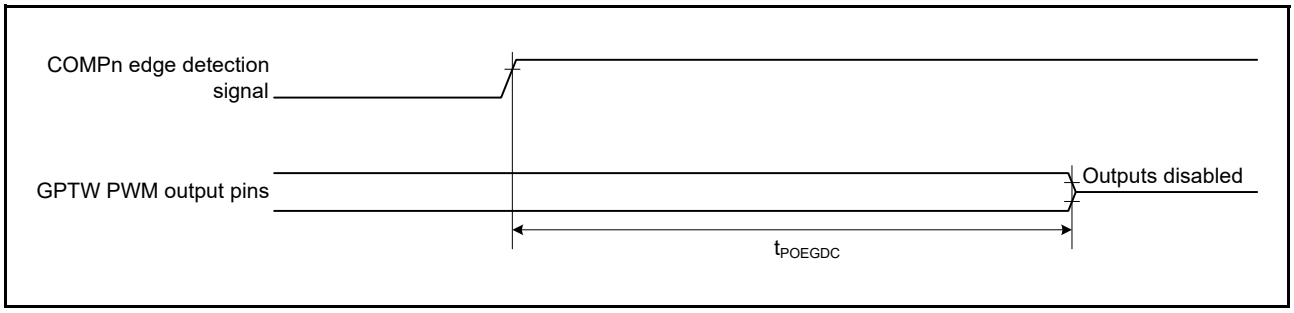


Figure 2.31 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator (n = 0 to 2)

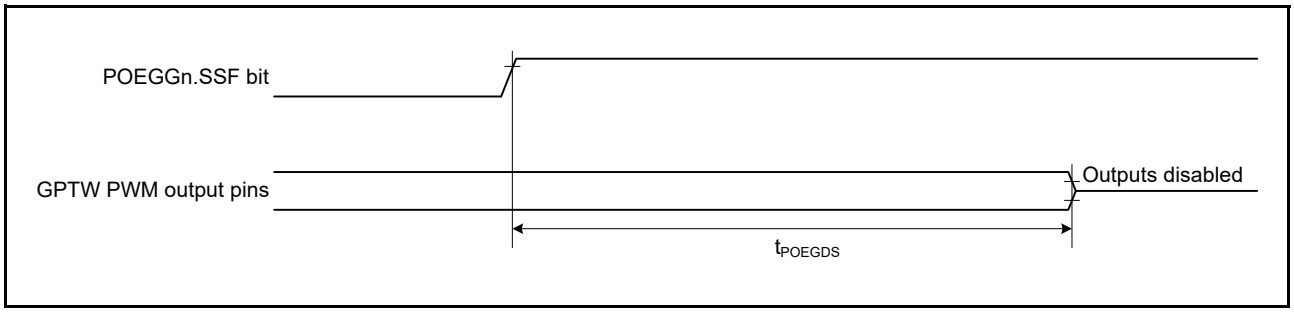


Figure 2.32 Output Disable Time for POEG in Response to the Register Setting (n = A)

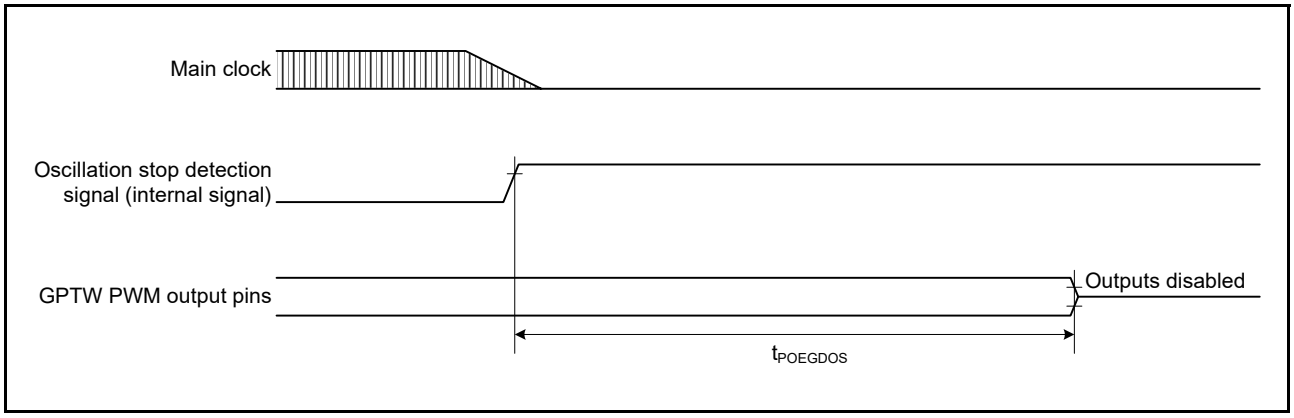


Figure 2.33 Output Disable Time of POEG in Response to the Oscillation Stop Detection

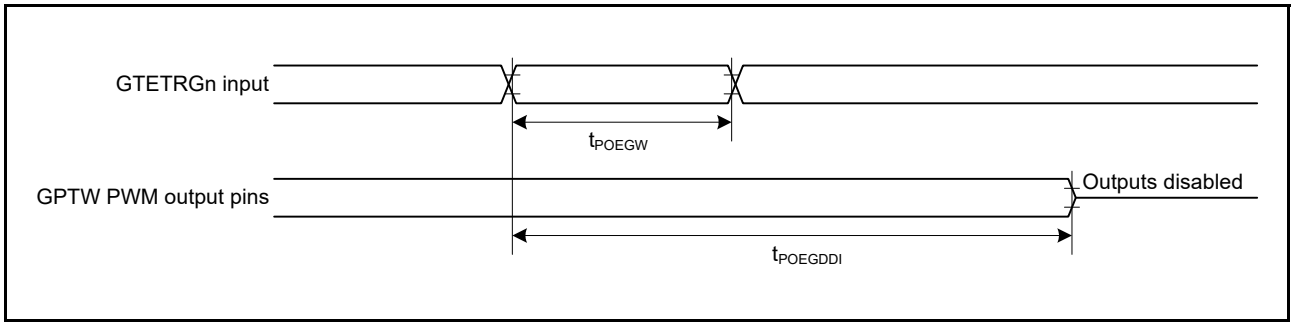


Figure 2.34 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin (n = A)

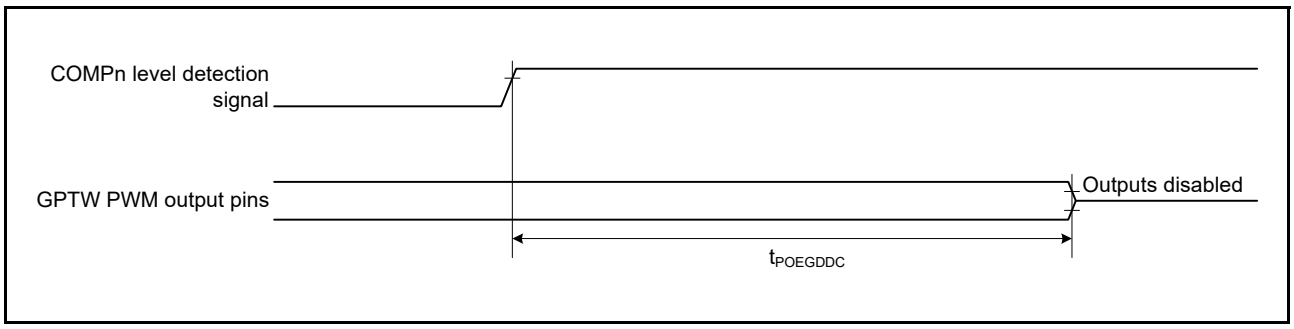


Figure 2.35 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator (n = 0 to 2)

2.5.5.5 GPTW

Table 2.39 GPTW Timing

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
GPTW	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{PBcyc}	Figure 2.36
		Both-edge setting		2.5	—		
	Input capture rise/fall time		t_{GTICr}/ t_{GTICf}	—	0.1	µs/V	Figure 2.36
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PBcyc}	Figure 2.37
		Both-edge setting		2.5	—		
	Timer clock pulse width		t_{GTCKWH}	1.5	—	t_{PBcyc}	Figure 2.38
			t_{GTCKWL}				
	Timer clock rise/fall time		t_{GTCKr}/ t_{GTCKf}	—	0.1	µs/V	Figure 2.38

Note 1. t_{PBcyc}: PCLKB cycle

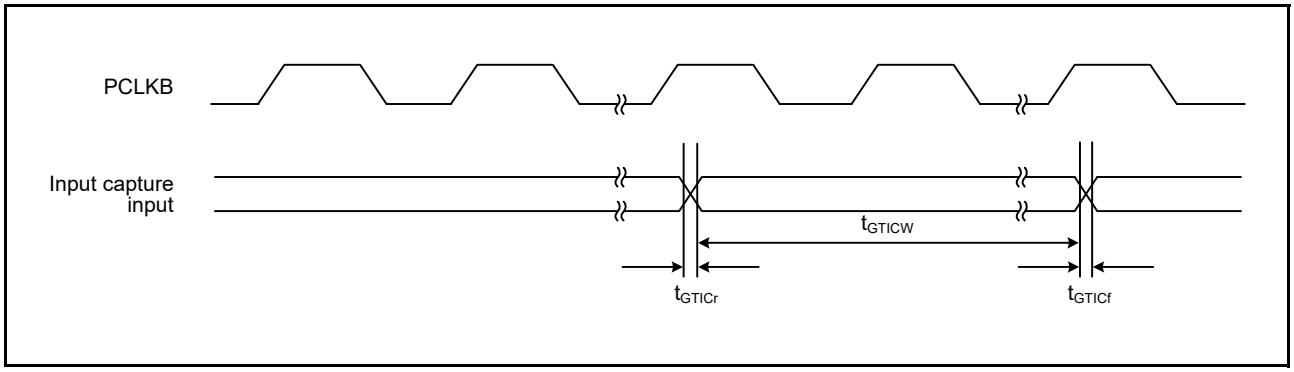


Figure 2.36 GPTW Input Capture Input Timing

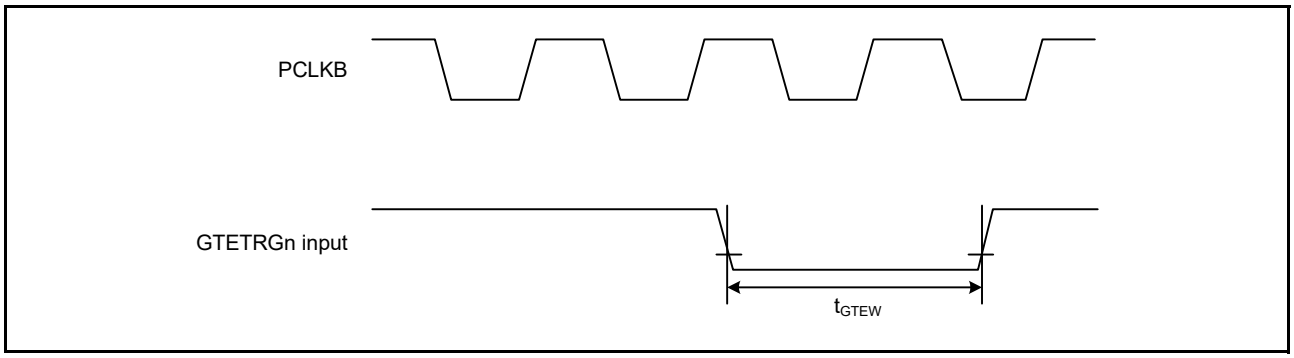


Figure 2.37 GPTW External Trigger Input Timing (n = A)

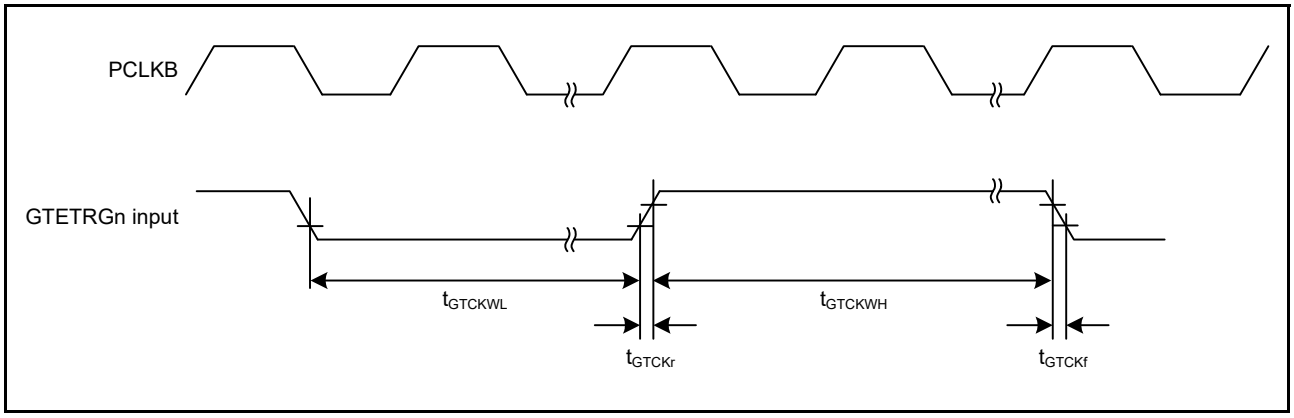


Figure 2.38 GPTW Clock Input Timing (n = A)

2.5.5.6 TMR

Table 2.40 TMR Timing

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.39
		Both-edge setting		2.5	—		
	Timer clock rise/fall time		t_{TMCr}, t_{TMCf}	—	0.1	μs/V	

Note 1. t_{PBcyc}: PCLKB cycle

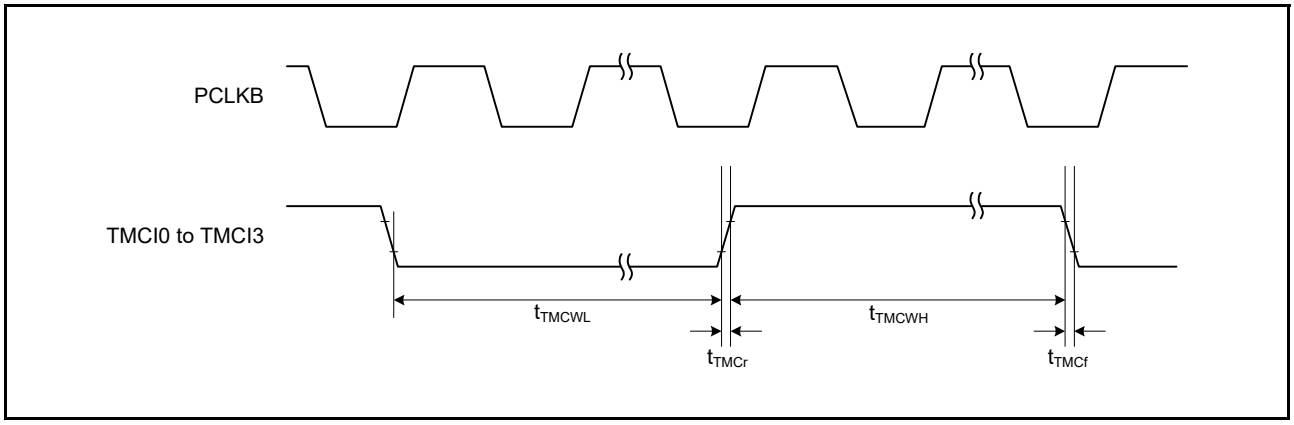


Figure 2.39 TMR Clock Input Timing

2.5.5.7 SCI

Table 2.41 SCI Timing

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
SCI (channel 1, 5, 6, 12)	Input clock cycle time		Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.40
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous		t_{Scyc}	8	—	t_{PBcyc}	Figure 2.41
		Clock synchronous			4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	4.0 V ≤ VCC		—	40	ns	
			2.7 V ≤ VCC		—	65	ns	
	Receive data setup time (master)	Clock synchronous	4.0 V ≤ VCC	t_{RXS}	40	—	ns	
			2.7 V ≤ VCC		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

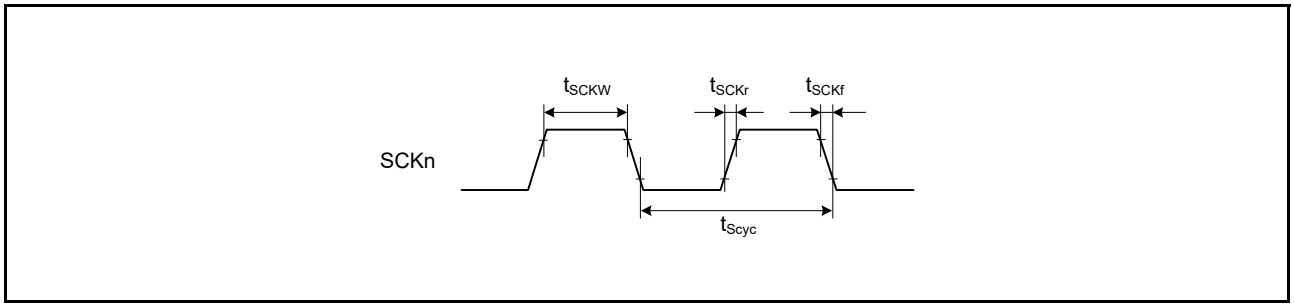


Figure 2.40 SCK Clock Input Timing (n = 1, 5, 6, 12)

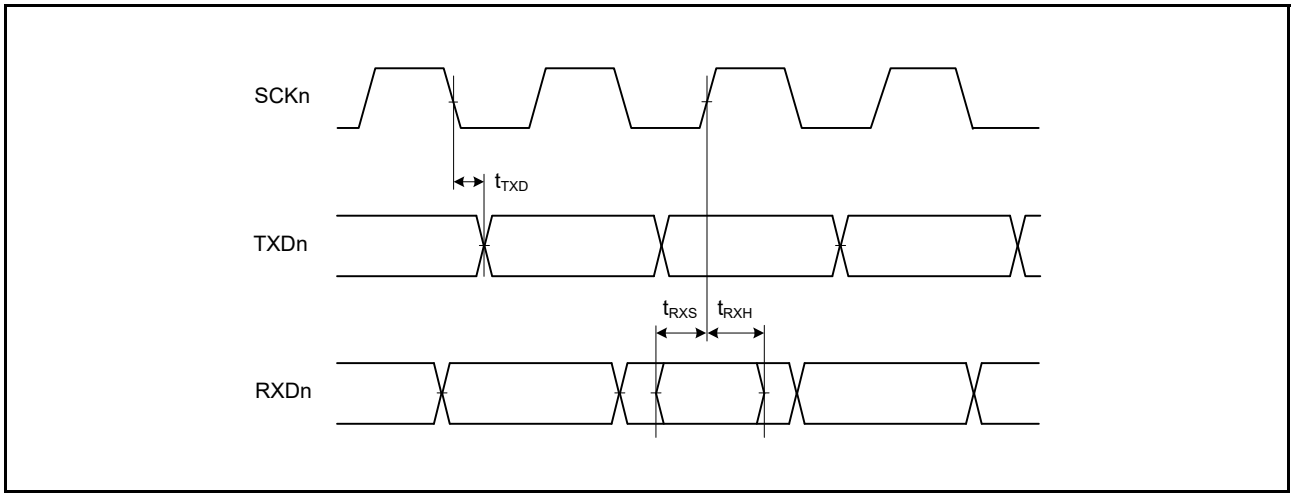
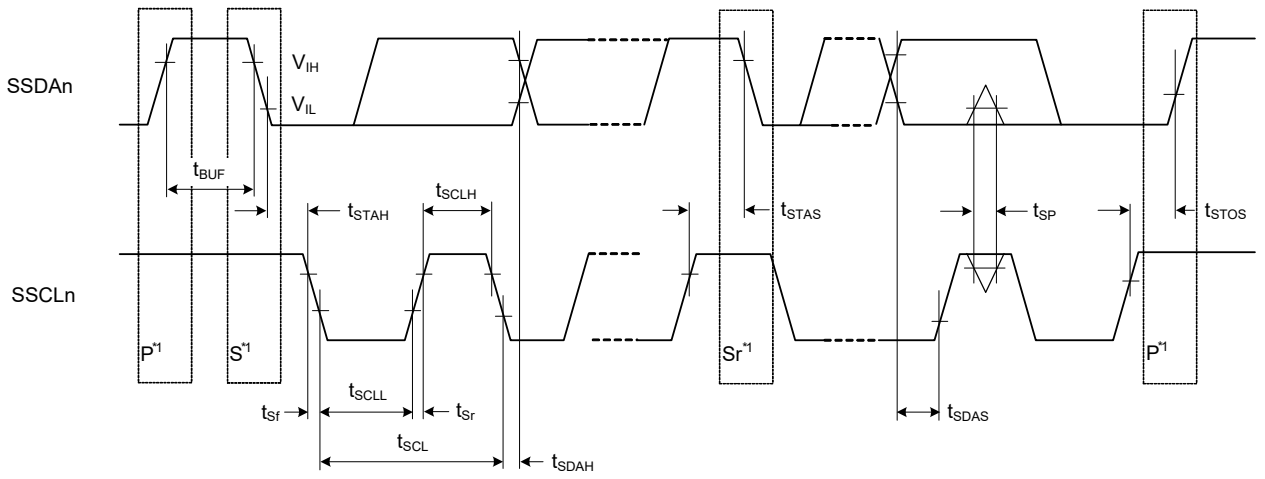


Figure 2.41 SCI Input/Output Timing: Clock Synchronous Mode (n = 1, 5, 6, 12)

Table 2.42 Simple I²C Timing

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 2.42
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple I²C (fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 2.42
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{PBcyc}: PCLKB cycle
Note 1. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.42 Output Timing and Simple I²C Bus Interface Input/Output Timing (n = 1, 5, 6, 12)

Table 2.43 Simple SPI Timing

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	—	t_{PBcyc}	Figure 2.43
	SCK clock cycle input (slave)			6	—	t_{PBcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	4.0 V ≤ VCC	t_{SU}	40	—	ns	Figure 2.44, Figure 2.45
		2.7 V ≤ VCC		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_{H}	40	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	4.0 V ≤ VCC		—	40		
		2.7 V ≤ VCC		—	65		
	Data output hold time (master)		t_{OH}	–10	—	ns	
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{PBcyc}	Figure 2.46, Figure 2.47
	Slave output release time		t_{REL}	—	6	t_{PBcyc}	

Note 1. t_{PBcyc}: PCLKB cycle

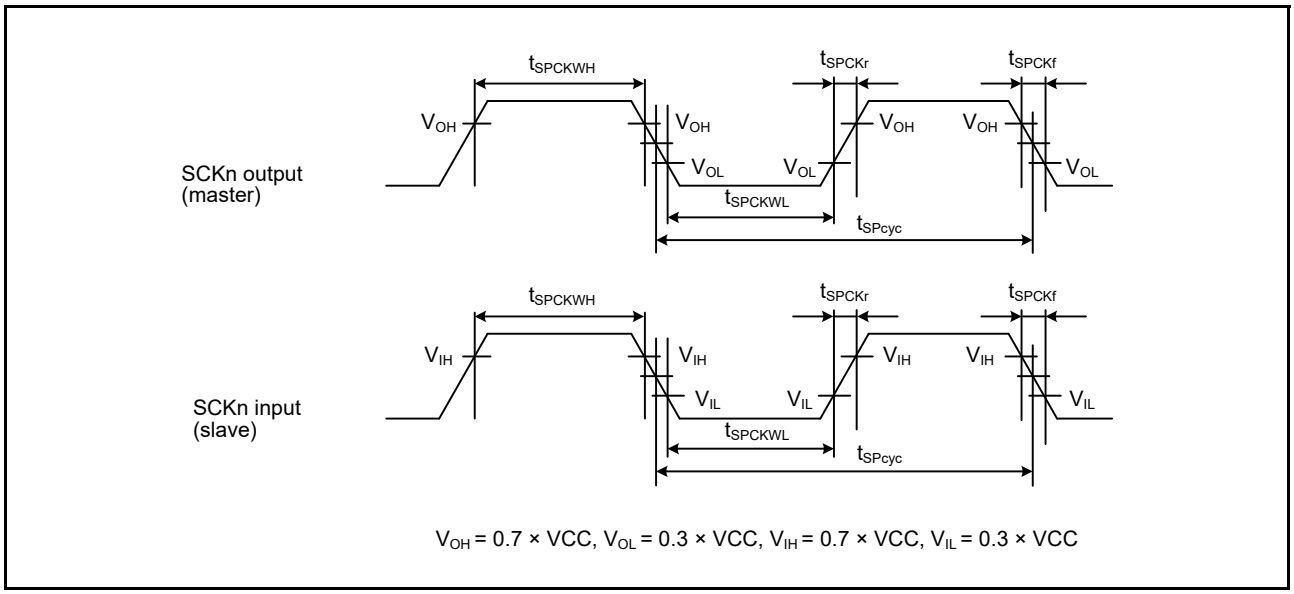


Figure 2.43 Simple SPI Clock Timing (n = 1, 5, 6, 12)

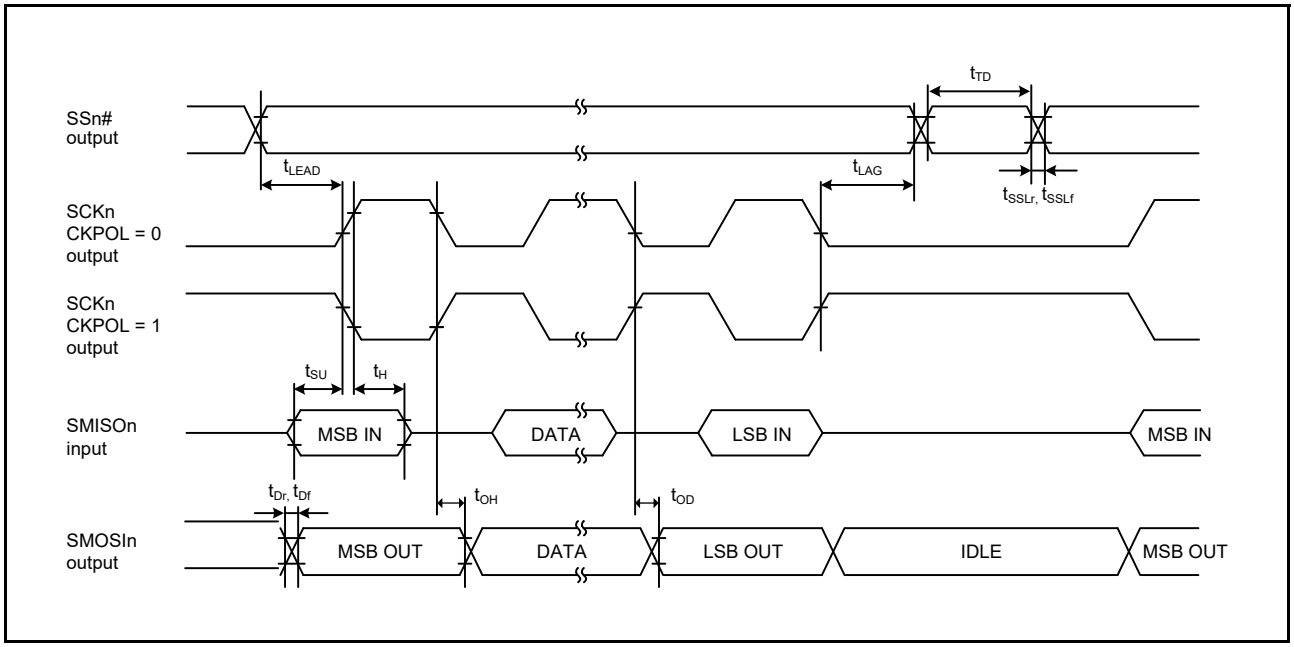


Figure 2.44 Simple SPI Timing (Master, CKPH = 1) (n = 1, 5, 6, 12)

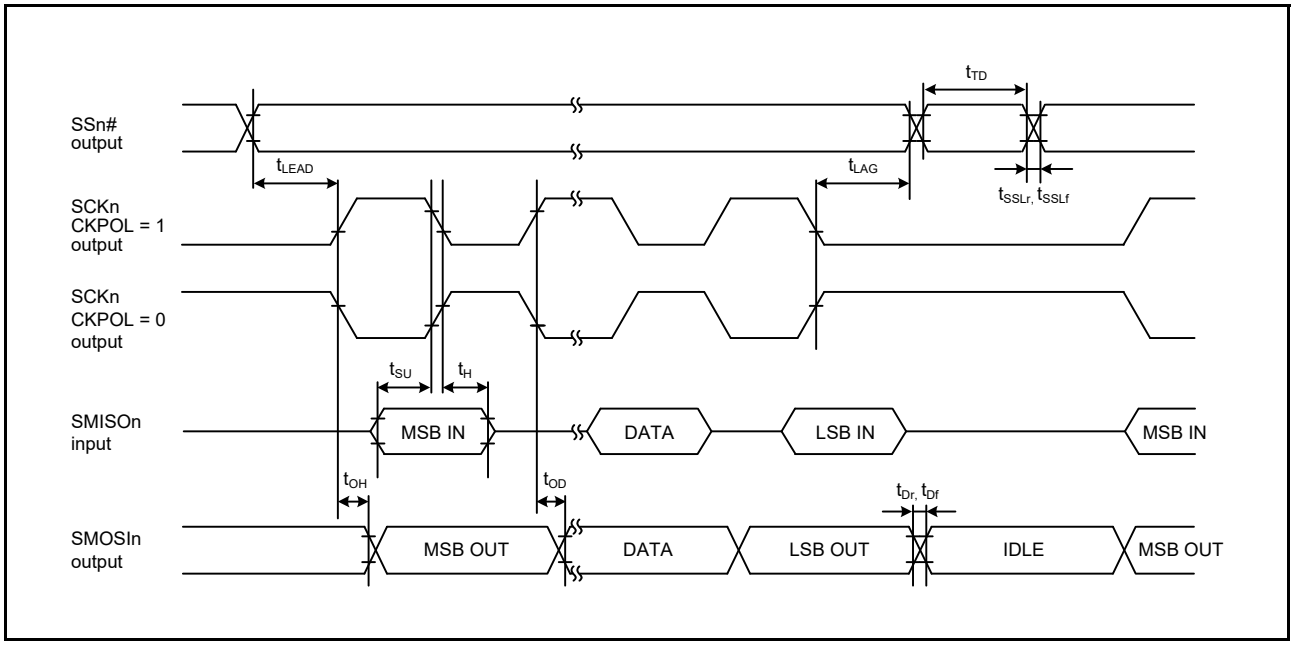


Figure 2.45 Simple SPI Timing (Master, CKPH = 0) (n = 1, 5, 6, 12)

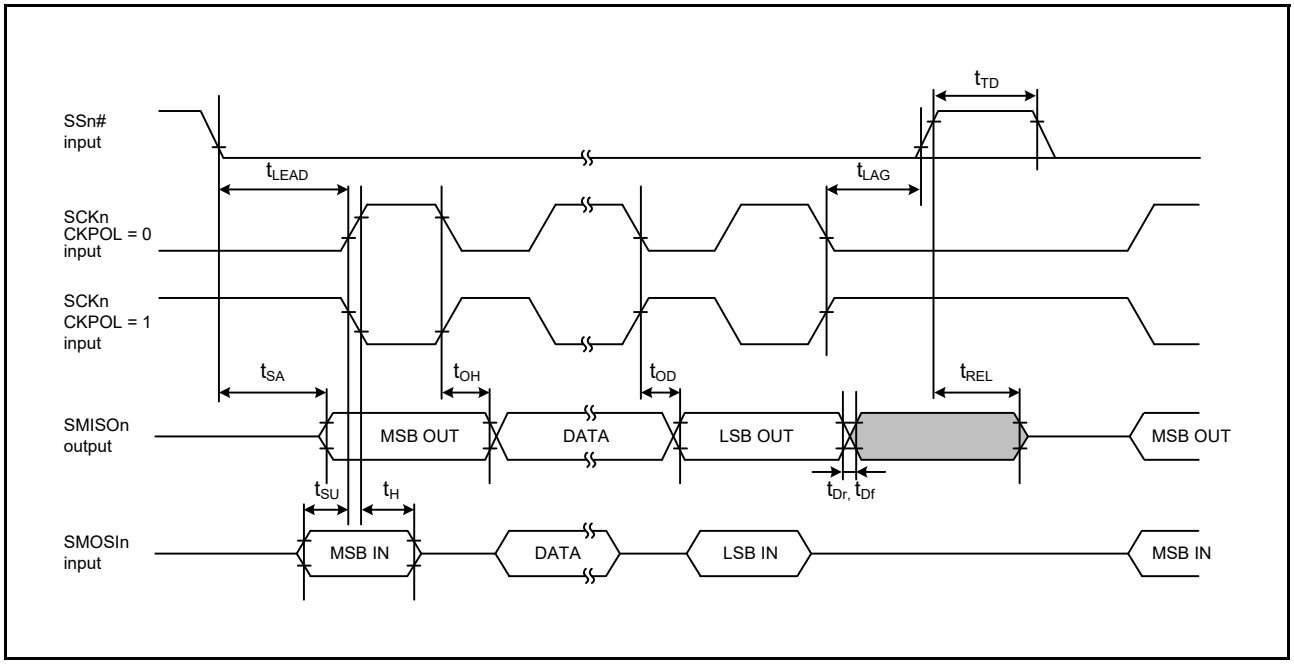


Figure 2.46 Simple SPI Clock Timing (Slave, CKPH = 1) (n = 1, 5, 6, 12)

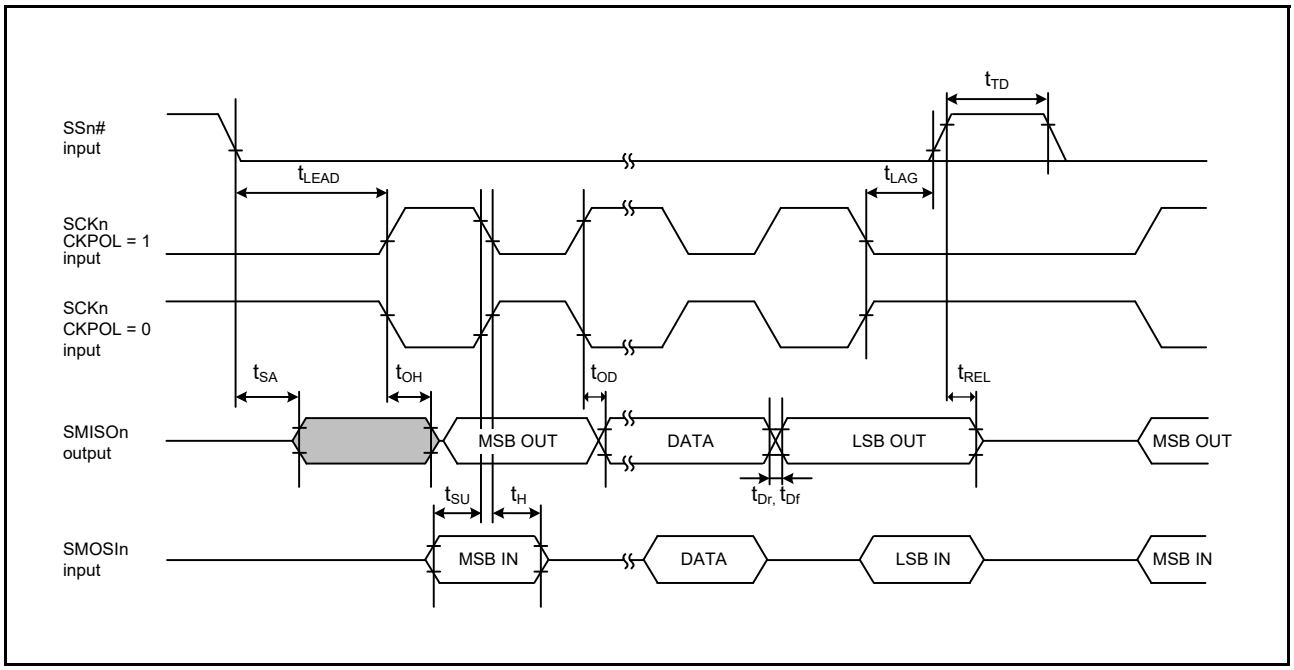


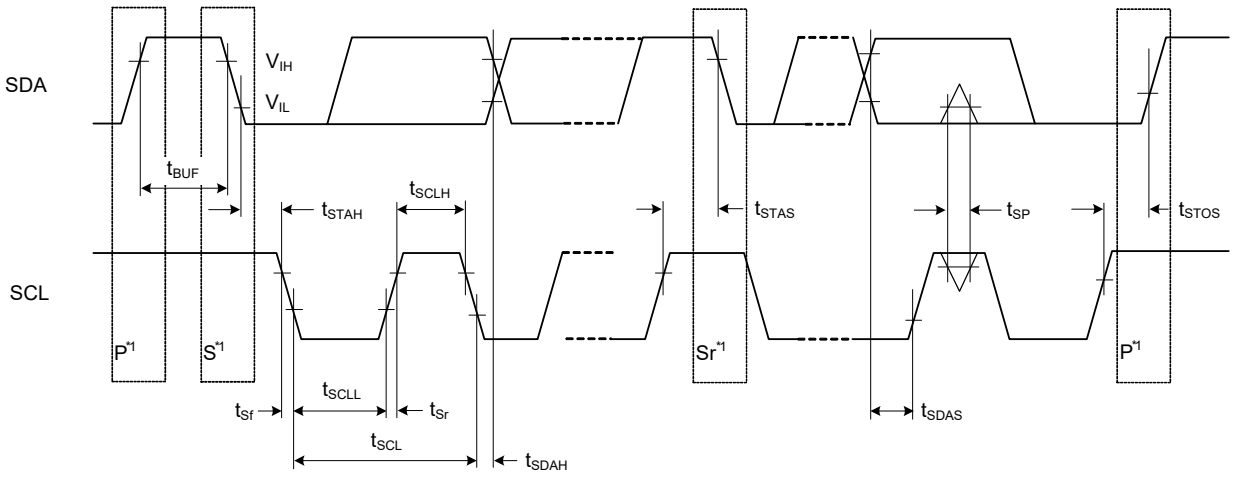
Figure 2.47 Simple SPI Timing (Slave, CKPH = 0) (n = 1, 5, 6, 12)

2.5.5.8 RIIC

Table 2.44 RIIC Timing

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.48
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.48
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	20 × (External pull-up voltage/5.5 V)	300	ns	
	SCL, SDA fall time	t_{Sf}	20 × (External pull-up voltage/5.5 V)	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle
Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.
Note 2. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.48 RIIC Bus Interface Input/Output Timing

2.5.5.9 A/D Converter Trigger

Table 2.45 A/D Converter Trigger Timing

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.49

Note 1. t_{PBcyc}: PCLKB cycle

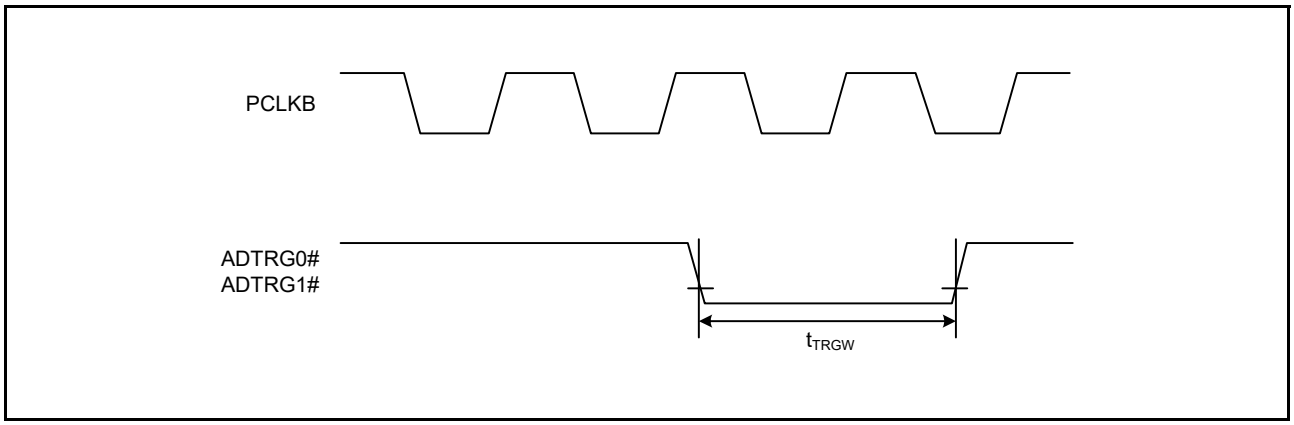


Figure 2.49 A/D Converter External Trigger Input Timing

2.5.5.10 CAC

Table 2.46 CAC Timing

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$ *2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	ns	
		$t_{PBcyc} > t_{cac}$ *2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$			
	CACREF input rise/fall time		$t_{CACREFr}$, $t_{CACREFf}$	—	0.1	µs/V	

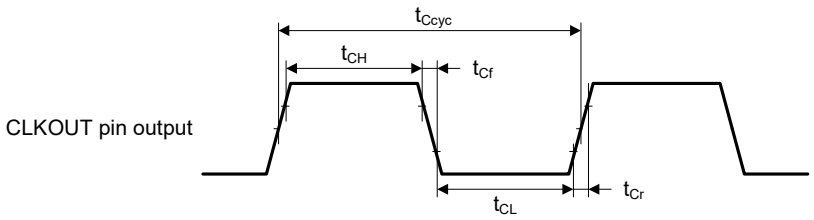
Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

2.5.5.11 CLKOUT

Table 2.47 CLKOUT Timing

Item		Symbol	Min.	Max.	Unit	Test Conditions
CLKOUT	CLKOUT pin output cycle*2	t_{Ccyc}	62.5	—	ns	Figure 2.50
	CLKOUT pin high pulse width*1	t_{CH}	15	—	ns	
	CLKOUT pin low pulse width*1	t_{CL}	15	—	ns	
	CLKOUT pin output rise time	t_{Cr}	—	12	ns	
	CLKOUT pin output fall time	t_{Cf}	—	12	ns	

Note 1. When the LOCO is selected as the clock output source (CKOCR.CKOSEL[3:0] bits = 0000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).
Note 2. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSEL[3:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.



Test conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.50 CLKOUT Output Timing

2.6 A/D Conversion Characteristics

Table 2.48 A/D Conversion Characteristics (1)

Conditions: 1 to 64 MHz, 4.5 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ VREFH0 ≤ VCC, VSS = VREFL0 = 0 V, T_a = –40 to 125°C, signal source impedance = 0.5 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	64	MHz	
Resolution		—	—	12	Bit	
Conversion time*1		0.50 (0.164)	—	—	µs	ADSSTRn = 0Ah
Analog input capacitance	Cs	—	—	9*2	pF	
Analog input resistance	Rs	—	—	1.3*2	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±4.5	LSB	VCC = VREFH0
		—	±1.0	±5.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±7.0	LSB	
Full-scale error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±4.5	LSB	VCC = VREFH0
		—	±1.0	±5.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±7.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	When the reference voltage is VREFH0 or VREFL0	—	±2.5	±5.0	LSB	VCC = VREFH0
		—	±2.5	±5.5	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±2.5	±7.5	LSB	
DNL differential nonlinearity error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±1.5	LSB	VCC = VREFH0
		—	±1.0	±2.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±1.5	LSB	
INL integral nonlinearity error	When the reference voltage is VREFH0 or VREFL0	—	±1.5	±3.0	LSB	VCC = VREFH0
		—	±1.5	±3.5	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.5	±3.0	LSB	

Note: The listed values apply when all pins other than one analog input pin that is a target of conversion are at fixed levels, and all peripheral modules (except for the unit handling the A/D conversion) and the CPU are stopped. Other conditions may lead to accuracy and errors falling beyond the ranges in the above specifications.

Note: Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The values in ( ) show the sampling times.

Note 2. The values are reference values.

Table 2.49 A/D Conversion Characteristics (2)

Conditions: 1 to 48 MHz, 4.5 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ VREFH0 ≤ VCC, VSS = VREFL0 = 0 V, T_a = –40 to 125°C, signal source impedance = 0.5 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	48	MHz	
Resolution		—	—	12	Bit	
Conversion time*1		0.67 (0.219)	—	—	µs	ADSSTRn = 0Ah
Analog input capacitance	Cs	—	—	9*2	pF	
Analog input resistance	Rs	—	—	1.3*2	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±4.5	LSB	VCC = VREFH0
		—	±1.0	±5.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±7.0	LSB	
Full-scale error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±4.5	LSB	VCC = VREFH0
		—	±1.0	±5.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±7.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	When the reference voltage is VREFH0 or VREFL0	—	±2.5	±5.0	LSB	VCC = VREFH0
		—	±2.5	±5.5	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±2.5	±7.5	LSB	
DNL differential nonlinearity error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±1.5	LSB	VCC = VREFH0
		—	±1.0	±2.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±1.5	LSB	
INL integral nonlinearity error	When the reference voltage is VREFH0 or VREFL0	—	±1.5	±3.0	LSB	VCC = VREFH0
		—	±1.5	±3.5	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.5	±3.0	LSB	

Note: The listed values apply when all pins other than one analog input pin that is a target of conversion are at fixed levels, and all peripheral modules (except for the unit handling the A/D conversion) and the CPU are stopped. Other conditions may lead to accuracy and errors falling beyond the ranges in the above specifications.

Note: Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The values in ( ) show the sampling times.

Note 2. The values are reference values.

Table 2.50 A/D Conversion Characteristics (3)

Conditions: 1 to 48 MHz, 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ VCC, VSS = VREFL0 = 0 V, T_a = –40 to 125°C, signal source impedance = 0.5 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	48	MHz	
Resolution		—	—	12	Bit	
Conversion time*1		0.79 (0.344)	—	—	µs	ADSSTRn = 10h
Analog input capacitance	Cs	—	—	9*2	pF	
Analog input resistance	Rs	—	—	1.9*2	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±4.5	LSB	VCC = VREFH0
		—	±1.0	±6.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±8.5	LSB	
Full-scale error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±4.5	LSB	VCC = VREFH0
		—	±1.0	±6.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±8.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	When the reference voltage is VREFH0 or VREFL0	—	±2.5	±5.5	LSB	VCC = VREFH0
		—	±2.5	±7.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±2.5	±9.5	LSB	
DNL differential nonlinearity error	When the reference voltage is VREFH0 or VREFL0	—	±1.0	±1.5	LSB	VCC = VREFH0
		—	±1.0	±2.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.0	±1.5	LSB	
INL integral nonlinearity error	When the reference voltage is VREFH0 or VREFL0	—	±1.5	±3.0	LSB	VCC = VREFH0
		—	±1.5	±4.0	LSB	VCC > VREFH0
	When the reference voltage is VCC or VSS	—	±1.5	±3.0	LSB	

Note: The listed values apply when all pins other than one analog input pin that is a target of conversion are at fixed levels, and all peripheral modules (except for the unit handling the A/D conversion) and the CPU are stopped. Other conditions may lead to accuracy and errors falling beyond the ranges in the above specifications.

Note: Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The values in ( ) show the sampling times.

Note 2. The values are reference values.

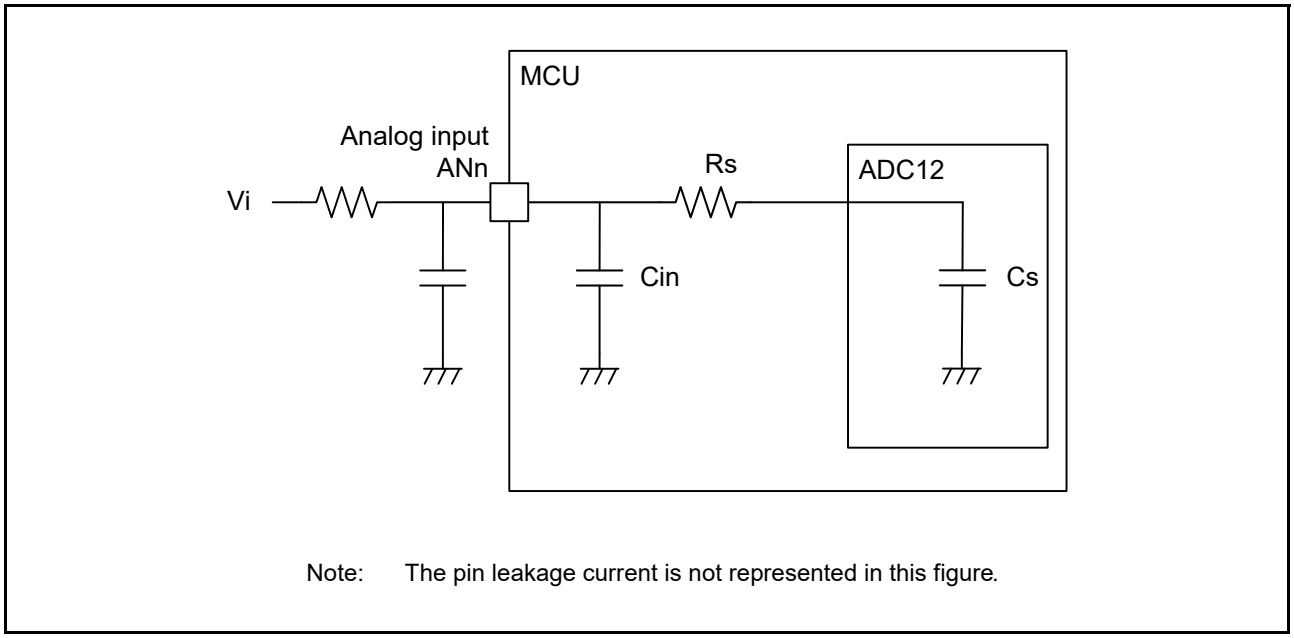
Table 2.51 Signal Source Impedance and Required Minimum Sampling Time

Signal source impedance [kΩ]	Required Sampling Time [ADCLK]		
	4.5 V ≤ VCC ≤ 5.5 V 4.5 V ≤ VREFH0 ≤ VCC		2.7 V ≤ VCC ≤ 5.5 V 2.7 V ≤ VREFH0 ≤ VCC
	ADCLK = 64 MHz	ADCLK = 48 MHz	ADCLK = 48 MHz
0.5	10	10	16
2.2	25	24	24
4.7	52	43	43
10	101	80	80
22	210	160	160

Table 2.52 A/D Internal Reference Voltage Characteristics

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*1	1.42	1.48	1.54	V	
Time until the internal reference voltage output becomes stable	—	—	5	μs	
Sampling time*2	3.9	—	—	μs	

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.
Note 2. Set the S12AD1.ADSSTRO register such that the sampling time of the 12-bit A/D converter satisfies this specification.



Note: The pin leakage current is not represented in this figure.

Figure 2.51 Equivalent Circuit of an Analog Input

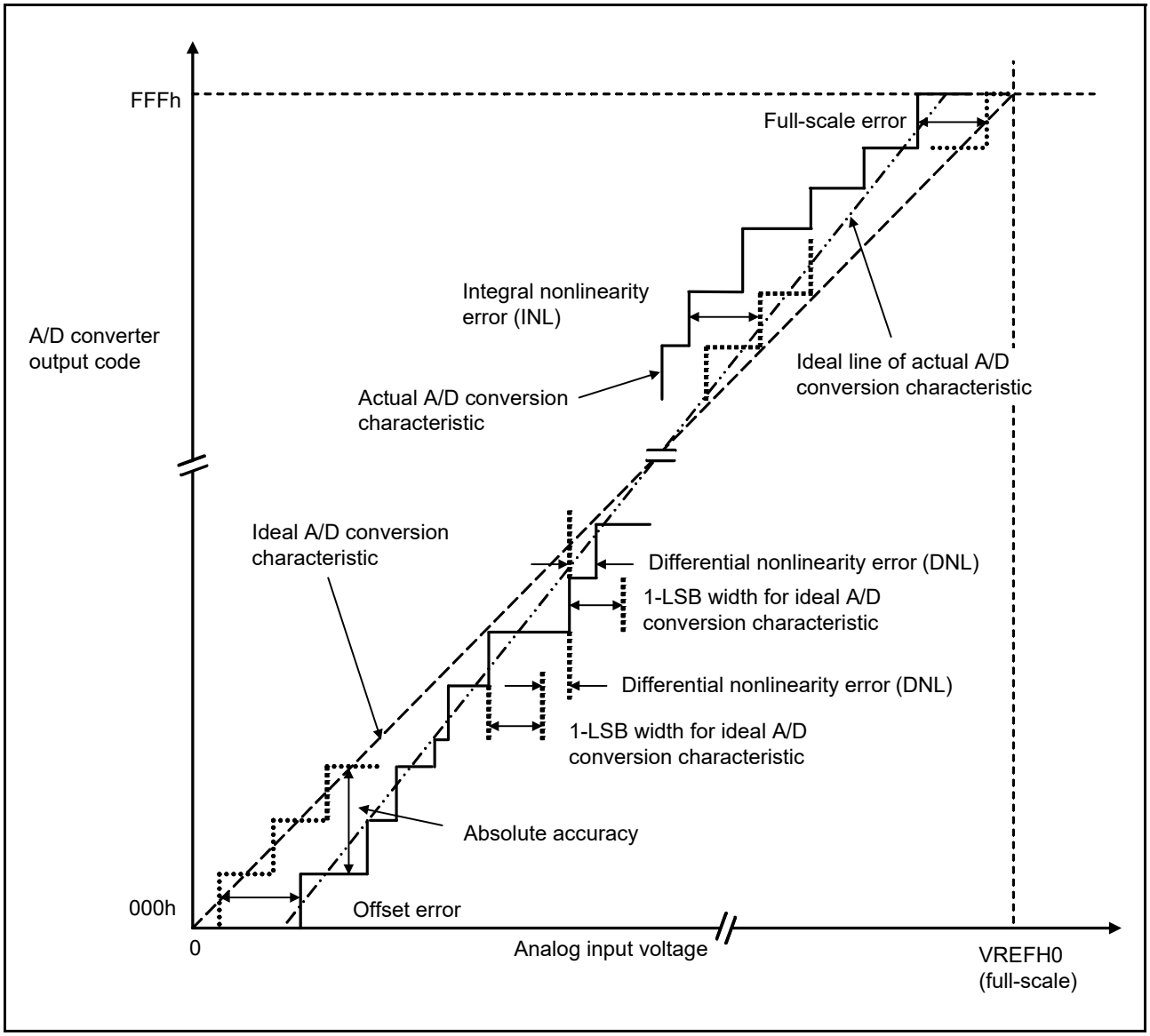


Figure 2.52 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, … are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

2.7 Programmable Gain Amplifier Characteristics

Table 2.53 Programmable Gain Amplifier Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage*1	V_{IO}	—	—	±5.7	mV	
Input voltage range	V_{ISR}	0	—	VCC	V	
Output voltage range	V_{OR}	0.07 × VCC	—	0.93 × VCC	V	
Gain	G	4, 8, 16, 32				
Gain error*1	E_G	—	±0.04	±0.47	%	G = 4, 8
		—	±0.02	±0.62	%	G = 16
		—	±0.03	±1.23	%	G = 32
Slew rate	SR	6.1	—	—	V/µs	4.0 V ≤ VCC ≤ 5.5 V, G = 4, 8, 16
		3.4	—	—	V/µs	4.0 V ≤ VCC ≤ 5.5 V, G = 32
		2	—	—	V/µs	2.7 V ≤ VCC ≤ 4.0 V
Operation stabilization time	t_{start}	—	—	2.66	µs	

Note 1. The listed values apply when PGAGND is selected as the ground for the feedback resistor. If VSS is selected, the values may fall beyond the listed ranges.

2.8 Comparator Characteristics

Table 2.54 Comparator Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{IO}	—	±5	±10.3	mV	
Reference input voltage range	V_{ref}	0	—	VCC	V	
Input voltage slope*1	dV/dt	—	—	±3.0	V/μs	
Response time	t_{PLH}	—	50	76	ns	VOD = 100 mV CMPCTL.NFE = 0
	t_{PHL}	—	50	73	ns	
Stabilization wait time for input selection	t_{cwait}	74	—	—	ns	
Operation stabilization time	t_{cmp}		—	0.51	μs	

Note 1. If this characteristic is not satisfied, take measures described in section 34.4.6, Appearance of a Pulse in the Result of Comparison in the User's Manual: Hardware.

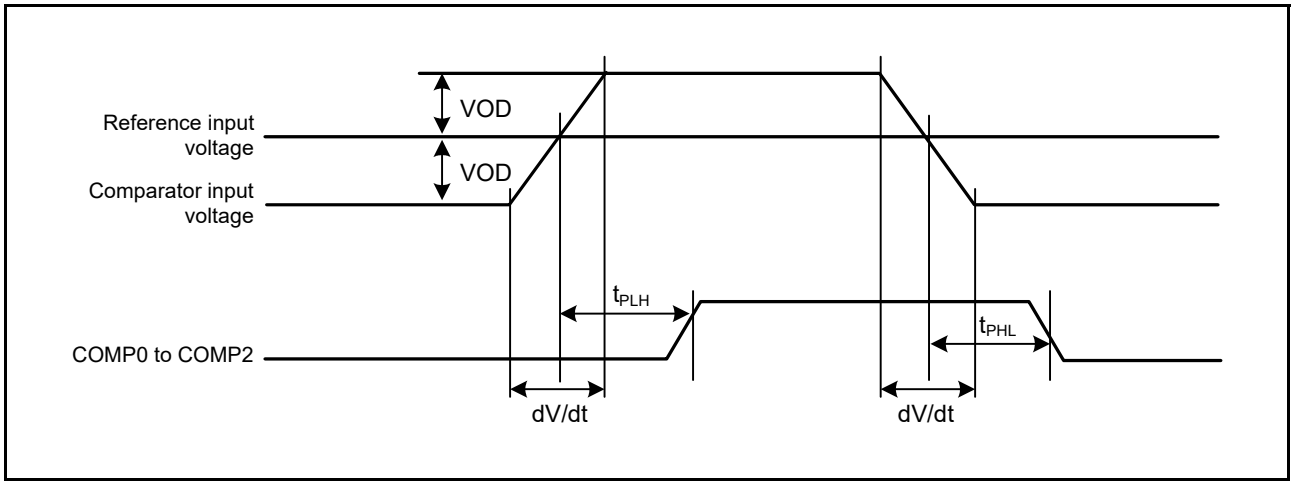


Figure 2.53 Comparator Response Time

2.9 D/A Conversion Characteristics

Table 2.55 D/A Conversion Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	35-pF capacitive load
Absolute accuracy	—	—	±1.0	±3.0	LSB	2-MΩ resistive load
	—	—	±1.0	±2.0	LSB	4-MΩ resistive load
Differential nonlinearity error (DNL)	—	—	±1.0	±2.0	LSB	
Output load resistance	—	4	—	—	MΩ	
Output load capacity	—	—	—	35	pF	
Output resistance	—	—	9.0	—	kΩ	

2.10 Temperature Sensor Characteristics

Table 2.56 Temperature Sensor Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	
Temperature slope	—	—	–3.3	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time*1	—	3.9	—	—	µs	

Note 1. Set the S12AD1.ADSSTRT register so that the sampling time of the 12-bit A/D converter meets this specification.

2.11 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.57 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)*1	V_{POR}	1.35	1.50	1.65	V	Figure 2.54, Figure 2.55
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.67	3.85	3.97	V	Figure 2.56 At falling edge VCC
		V_{det0_1}	2.70	2.85	3.00		
		V_{det0_2}	2.37	2.53	2.67		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.12	4.29	4.42	V	Figure 2.57 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.28		
		V_{det1_2}	3.86	4.03	4.16		
		V_{det1_3}	3.68	3.86	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.80	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.59	2.67		
Voltage detection level	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.08	4.32	4.48	V	Figure 2.58 At falling edge VCC
		V_{det2_1}	3.95	4.17	4.35		
		V_{det2_2}	3.82	4.03	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The MCU starts operation after the release from a power-on reset. The electrical characteristics of the voltage detection circuit are guaranteed when the operating voltage is at least 2.7 V.

Note 2. n in the symbol Vdet0_n denotes the value of the LDSEL1[1:0] bits.

Note 3. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 4. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

Table 2.58 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	31.5	—	ms	Figure 2.55
	During fast startup time*2	t_{POR}	—	5.0	—		
Wait time after voltage monitoring 0 reset cancellation		t_{LVD0}	—	860	—	µs	Figure 2.56
Wait time after voltage monitoring 1 reset cancellation	LVD0 disabled*4	t_{LVD1}	—	160	—	µs	Figure 2.57
	LVD0 enabled*5		—	860	—	µs	
Wait time after voltage monitoring 2 reset cancellation	LVD0 disabled*4	t_{LVD2}	—	160	—	µs	Figure 2.58
	LVD0 enabled*5		—	860	—	µs	
PDR response delay time		t_{det}	—	—	500	µs	Figure 2.54
LVD0 response delay time			—	—	500	µs	Figure 2.54
LVD1 response delay time			—	—	360	µs	Figure 2.54
LVD2 response delay time			—	—	600	µs	Figure 2.54
POR/LVD0 minimum VCC down time*3		t_{VOFF}	500	—	—	µs	Figure 2.54, VCC = 1.0 V or above
LVD1 minimum VCC down time*3			300	—	—	µs	Figure 2.54, VCC = 1.0 V or above
LVD2 minimum VCC down time*3			600	—	—	µs	Figure 2.54, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 2.55, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	300	µs	Figure 2.57
LVD2 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	1200	µs	Figure 2.58
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (LVD0, LVD1, and LVD2)		V_{LVH}	—	60	—	mV	LVD0 selected
			—	110	—		Vdet1_0 to Vdet1_2 selected
			—	70	—		Vdet1_3 to 9 selected
			—	90	—		LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

Note 4. When OFS1.LVDAS = 1b.

Note 5. When OFS1.LVDAS = 0b.

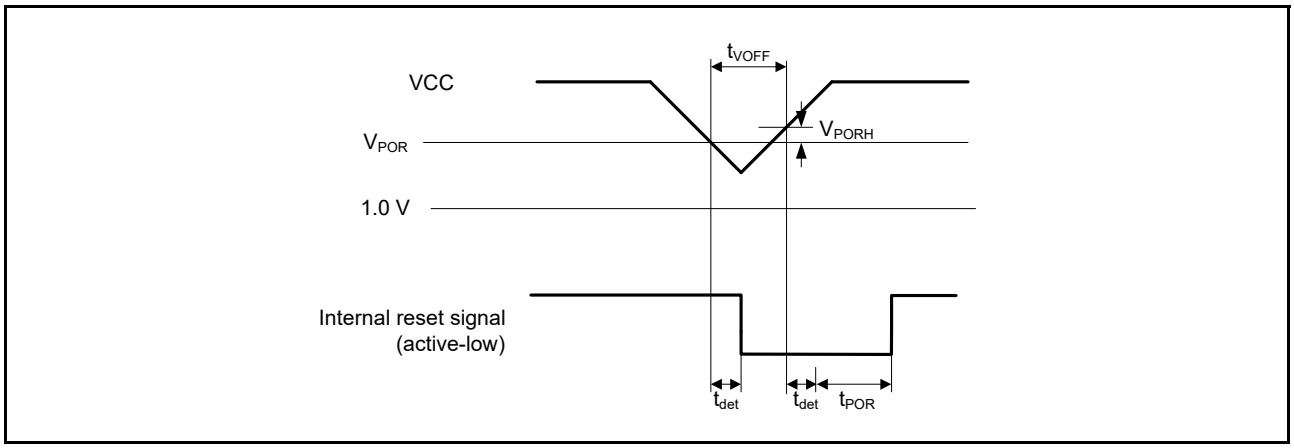
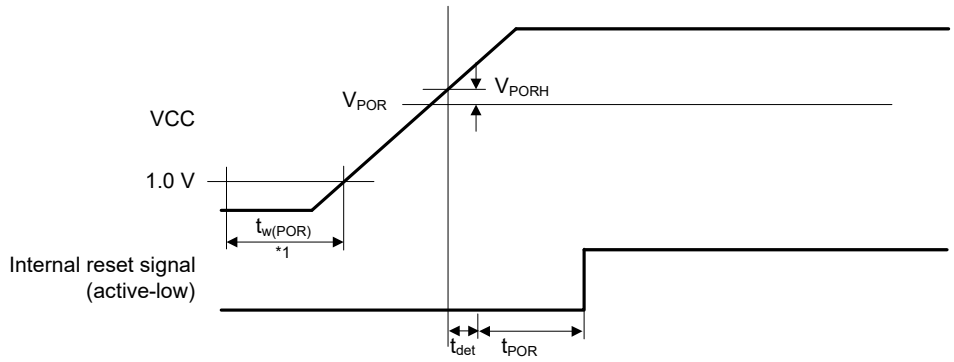


Figure 2.54 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.55 Power-On Reset Timing

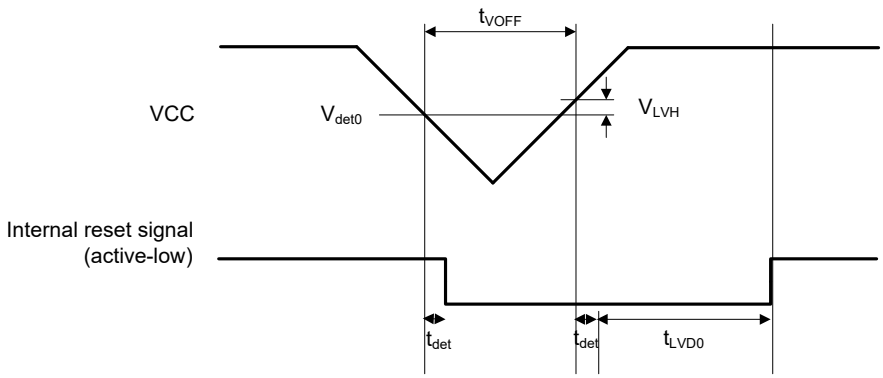


Figure 2.56 Voltage Detection Circuit Timing (V_{det0})

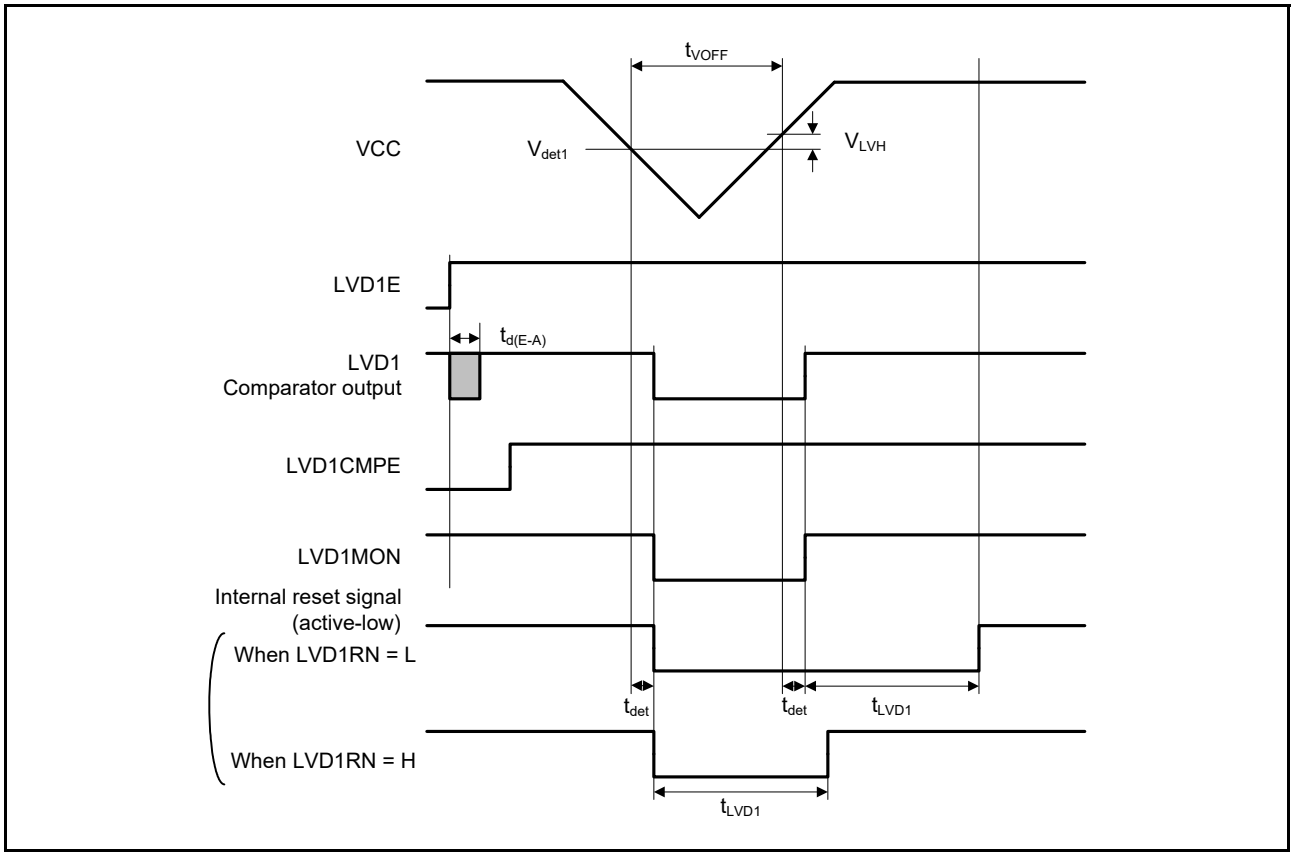


Figure 2.57 Voltage Detection Circuit Timing (V_{det1})

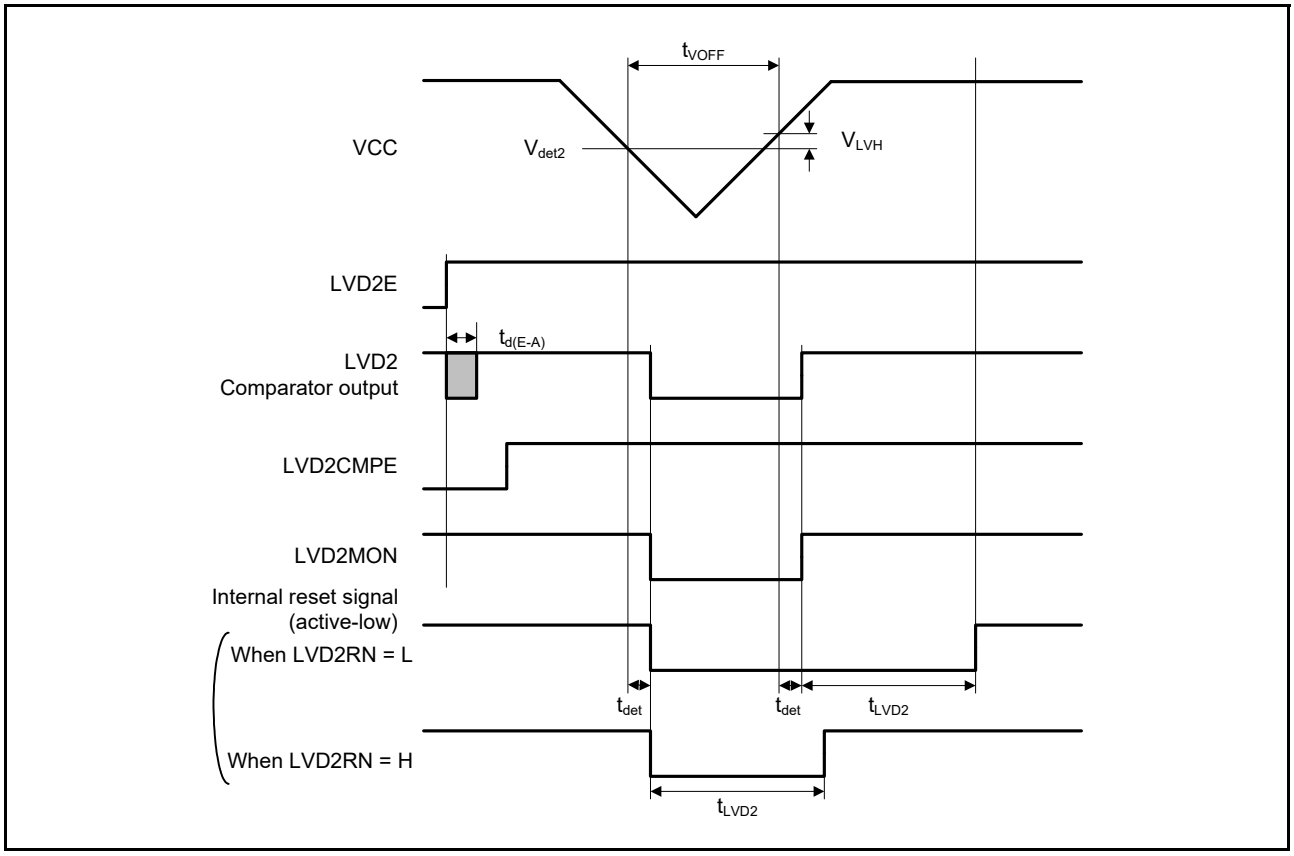


Figure 2.58 Voltage Detection Circuit Timing (V_{det2})

2.12 Oscillation Stop Detection Timing

Table 2.59 Oscillation Stop Detection Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.59

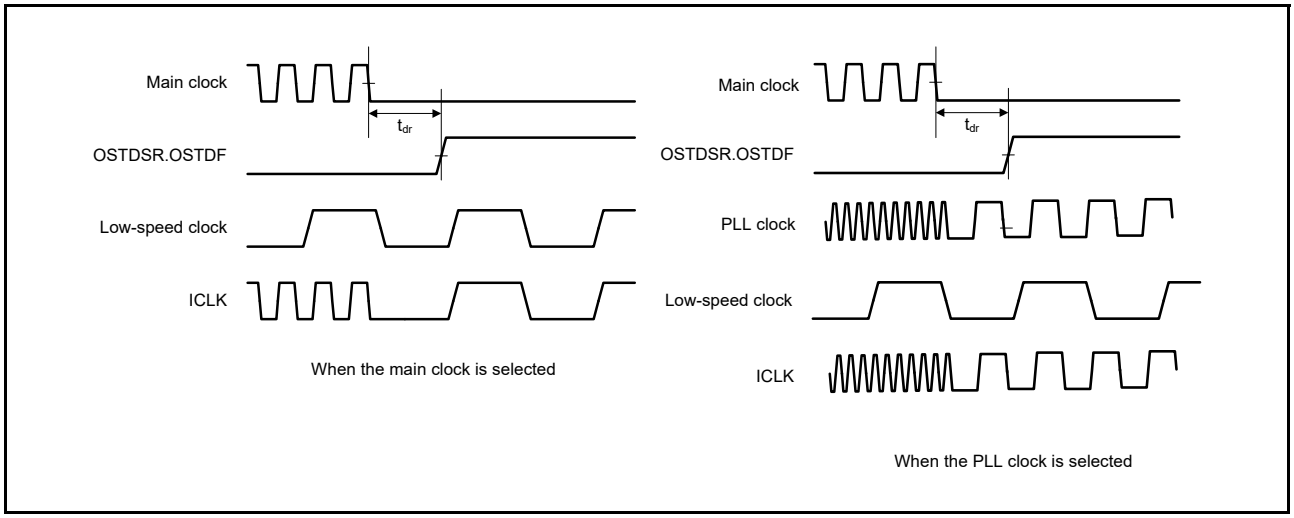


Figure 2.59 Oscillation Stop Detection Timing

2.13 ROM (Flash Memory for Code Storage) Characteristics

Table 2.60 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{PEC}	10K	—	—	Times	
Data retention*2, *3	After 10K times of N_{PEC}	t_{DRP}	20	—	—	Year	$T_a \leq +105°C$
			10	—	—		$T_a \leq +125°C$

Note 1. Definition of program/erase cycle: The program/erase cycle is the number of erasing for each block. For instance, when 8-byte program is performed 256 times for different addresses in a 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.61 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	—	45.4	448.7	—	45.1	446.0	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	—	5.4	220.4	—	5.4	220.1	ms
	128-Kbyte	t_{E128K}	—	204	4447	—	20.3	535.3	—	19.6	520.7	ms
Blank check time	8-byte	t_{BC8}	—	—	45.0	—	—	8.9	—	—	8.7	µs
	2-Kbyte	t_{BC2K}	—	—	1573	—	—	120	—	—	115	µs
Erase operation forcible stop time		t_{SED}	—	—	22.8	—	—	11.1	—	—	11.0	µs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	—	5.6	438.0	—	5.6	437.7	ms
Access window setting time		t_{AWS}	—	8.2	503.3	—	5.6	438.0	—	5.6	437.7	ms
ROM mode transition wait time		t_{MS}	15	—	—	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 2.62 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode

Item		Symbol	FCLK = 1 MHz			FCLK = 24 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	—	45.7	450.7	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	—	5.4	220.2	ms
	128-Kbyte	t_{E128K}	—	204	4447	—	19.6	521	ms
Blank check time	8-byte	t_{BC8}	—	—	45	—	—	9	µs
	2-Kbyte	t_{BC2K}	—	—	1573	—	—	115	µs
Erase operation forcible stop time		t_{SED}	—	—	22.8	—	—	11.2	µs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	—	5.6	437.7	ms
Access window setting time		t_{AWS}	—	8.2	503.3	—	5.6	437.7	ms
ROM mode transition wait time		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

2.14 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 2.63 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{DPEC}	100K	1000K	—	Times	
Data retention	After 10K times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	$T_a \leq +105°C$
			10*2, *3	—	—	Year	$T_a \leq +125°C$
	After 100K times of N_{DPEC}		5*2, *3	—	—	Year	$T_a \leq +125°C$
	After 1000K times of N_{DPEC}		—	1*2, *3	—	Year	$T_a = +25°C$

Note 1. Definition of program/erase cycle: The program/erase cycle is the number of erasing for each block. For instance, when 1-byte program is performed 256 times for different addresses in a 256-byte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.64 E2 DataFlash Characteristics (2) High-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	—	35.1	341.2	—	34.8	338.8	µs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	—	5.4	220.4	—	5.4	220.1	ms
	4-Kbyte	t_{DE4K}	—	55.0	1273.7	—	9.0	295.4	—	8.8	291.7	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	—	—	8.9	—	—	8.2	µs
	256-byte	t_{DBC256}	—	—	1573	—	—	120	—	—	115	µs
Erase operation forcible stop time		t_{DSED}	—	—	22.8	—	—	11.1	—	—	11.0	µs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 2.65 E2 DataFlash Characteristics (3) Middle-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	—	35.3	343.2	µs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	—	5.4	220.2	ms
	4-Kbyte	t_{DE4K}	—	55.0	1273.7	—	8.8	291.8	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	—	—	9.0	µs
	256-byte	t_{DBC256}	—	—	1573	—	—	115	ms
Erase operation forcible stop time		t_{DSED}	—	—	22.8	—	—	11.2	µs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

2.15 Usage Notes

2.15.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.

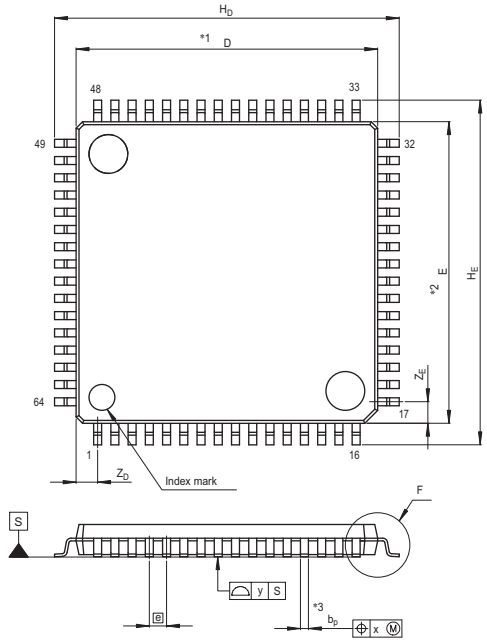
Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 30, 12-Bit A/D Converter (S12ADF) in the User's Manual: Hardware.

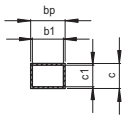
For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.

Appendix 1. Package Dimensions

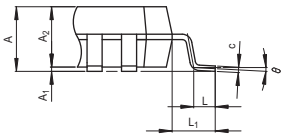
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



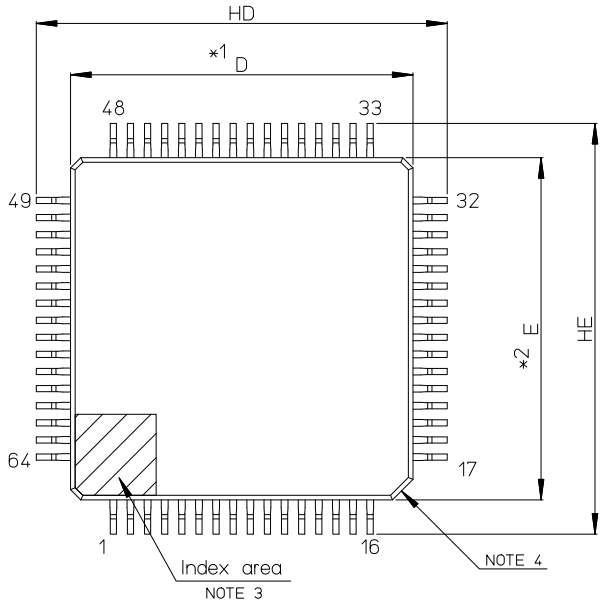
Detail F

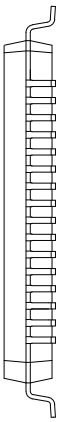
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

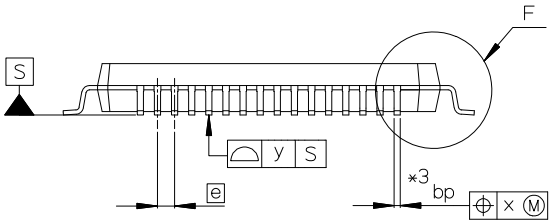
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure A 64-Pin LQFP (PLQP0064GA-A)

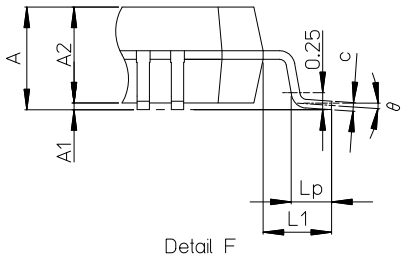
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g







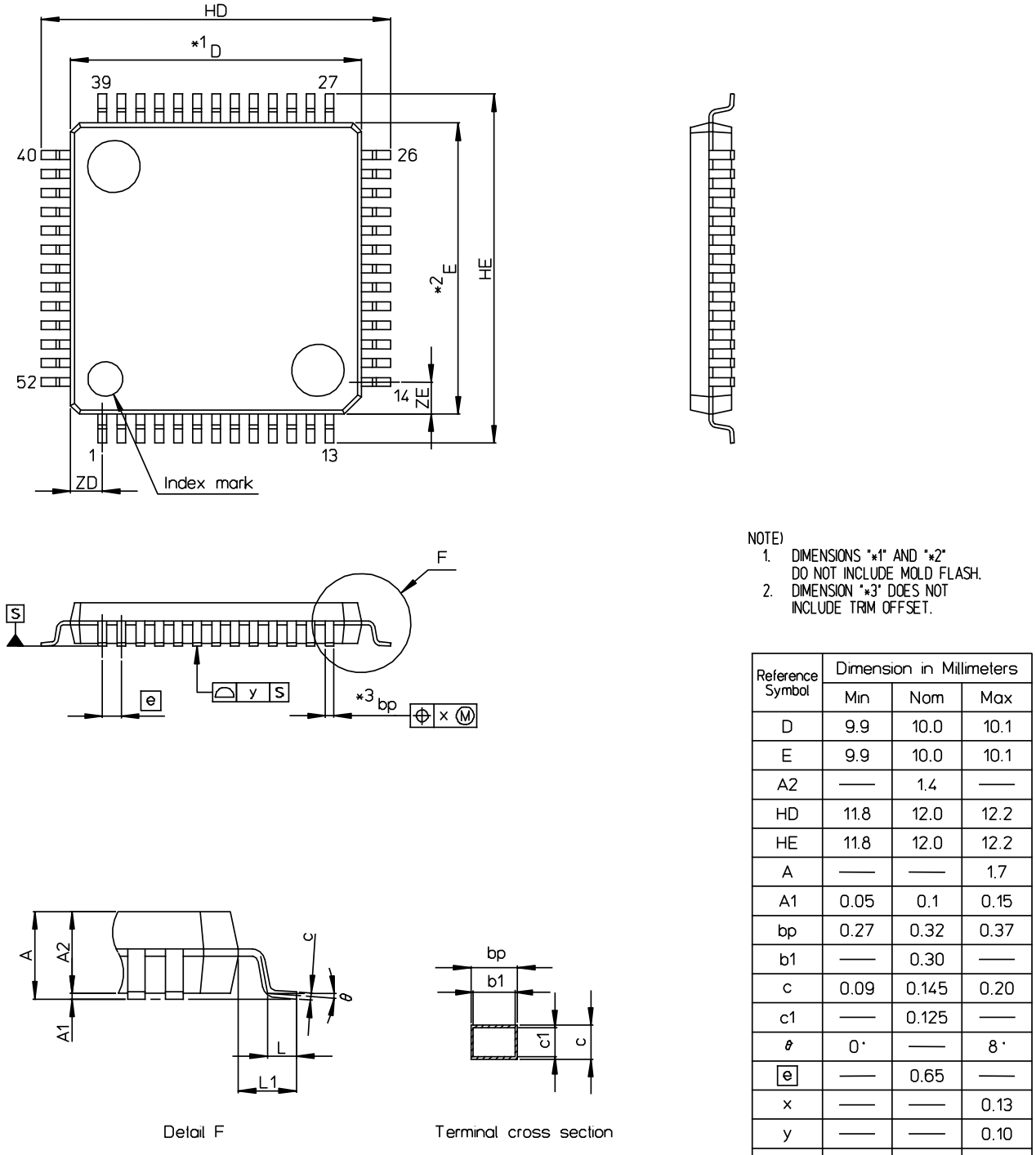
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure B 64-Pin LFQFP (PLQP0064KB-C)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3

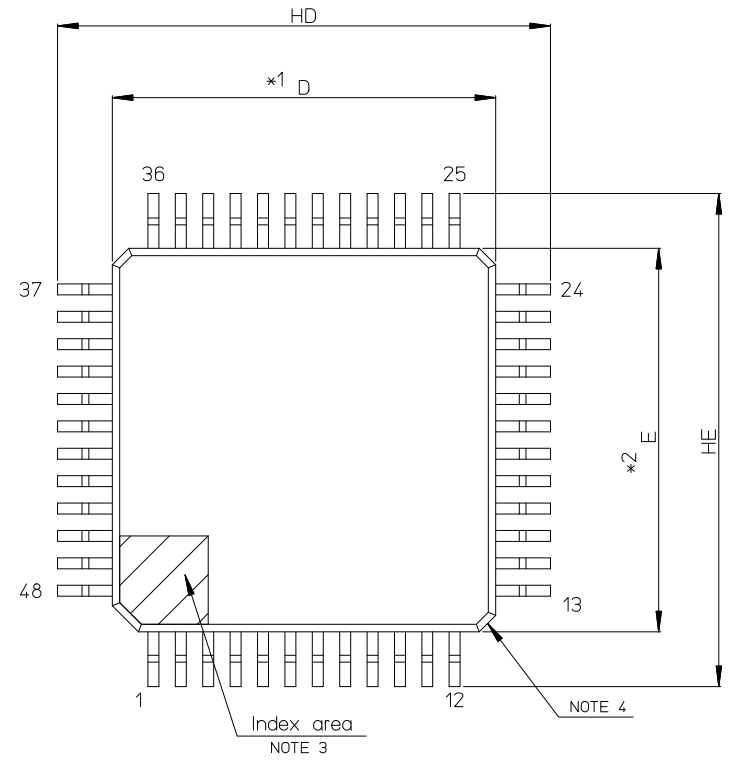


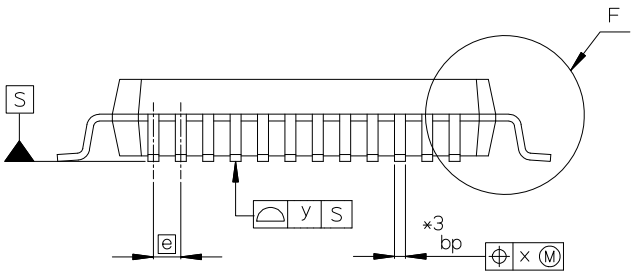
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

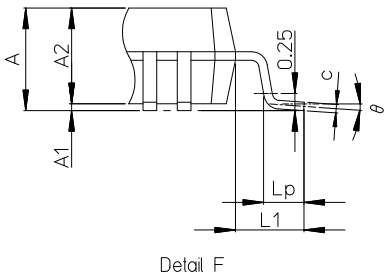
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	—	1.4	—
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	—	—	1.7
A1	0.05	0.1	0.15
bp	0.27	0.32	0.37
b1	—	0.30	—
c	0.09	0.145	0.20
c1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	1.1	—
ZE	—	1.1	—
L	0.35	0.5	0.65
L1	—	1.0	—

Figure C 52-Pin LQFP (PLQP0052JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







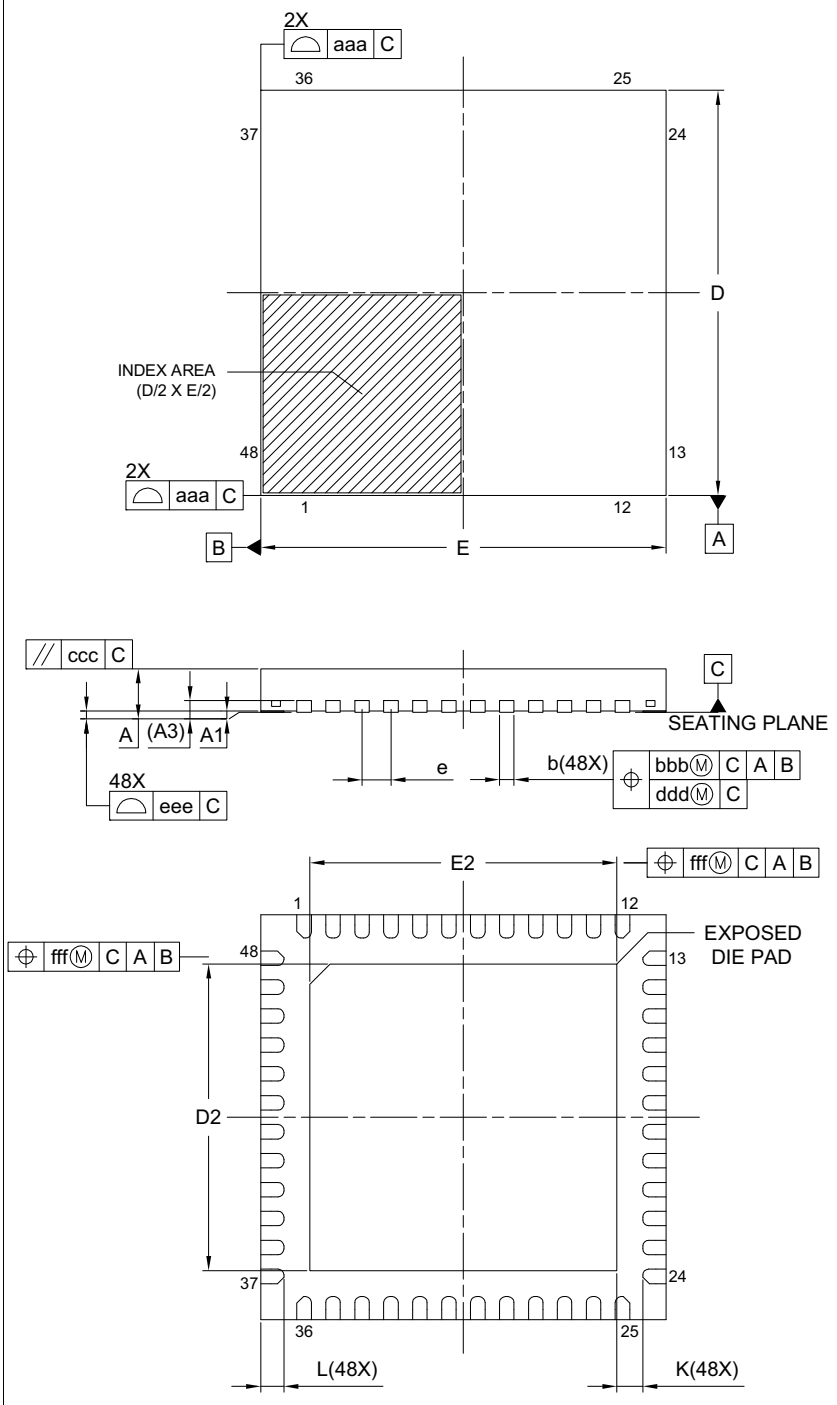
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure D 48-Pin LFQFP (PLQP0048KB-B)

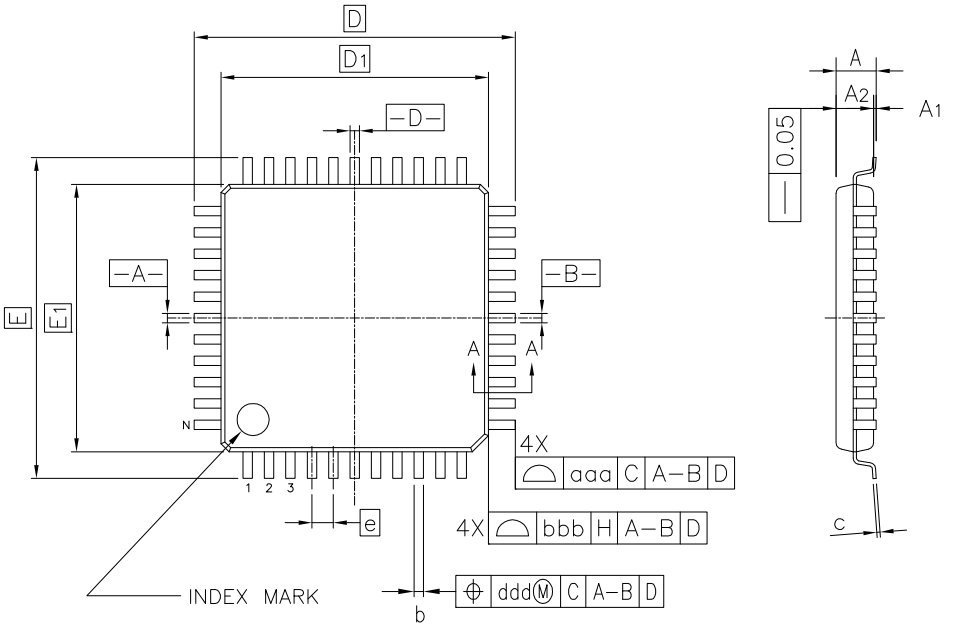
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

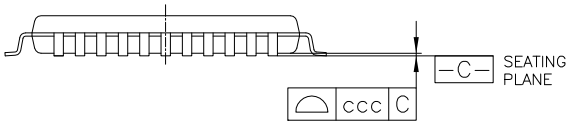


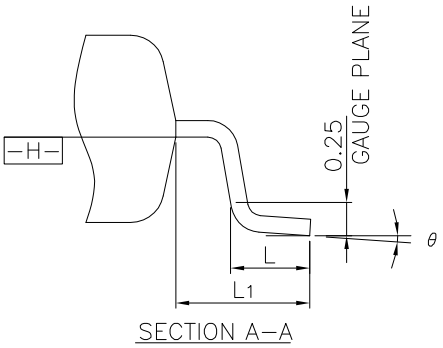
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure E 48-Pin HWQFN (PWQN0048KC-A)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP44-10x10-0.80	PLQP0044GF-A	0.3



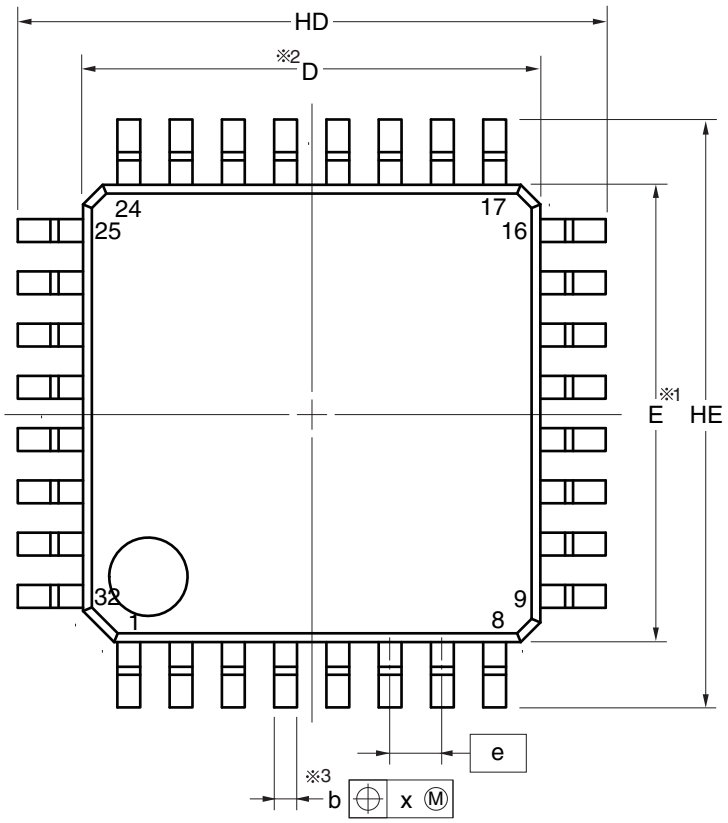


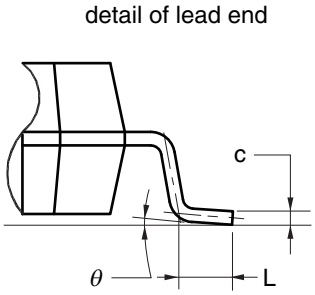


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.70
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	12.00 BSC.		
D_1	10.00 BSC.		
E	12.00 BSC.		
E_1	10.00 BSC.		
N	–	44	–
e	0.80 BSC.		
b	0.30	0.37	0.45
c	0.09	–	0.20
θ	0°	3.5°	8°
L	0.45	0.60	0.75
L_1	1.00 REF.		
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.10
ddd	–	–	0.20

Figure F 44-Pin LQFP (PLQP0044GF-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2





(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

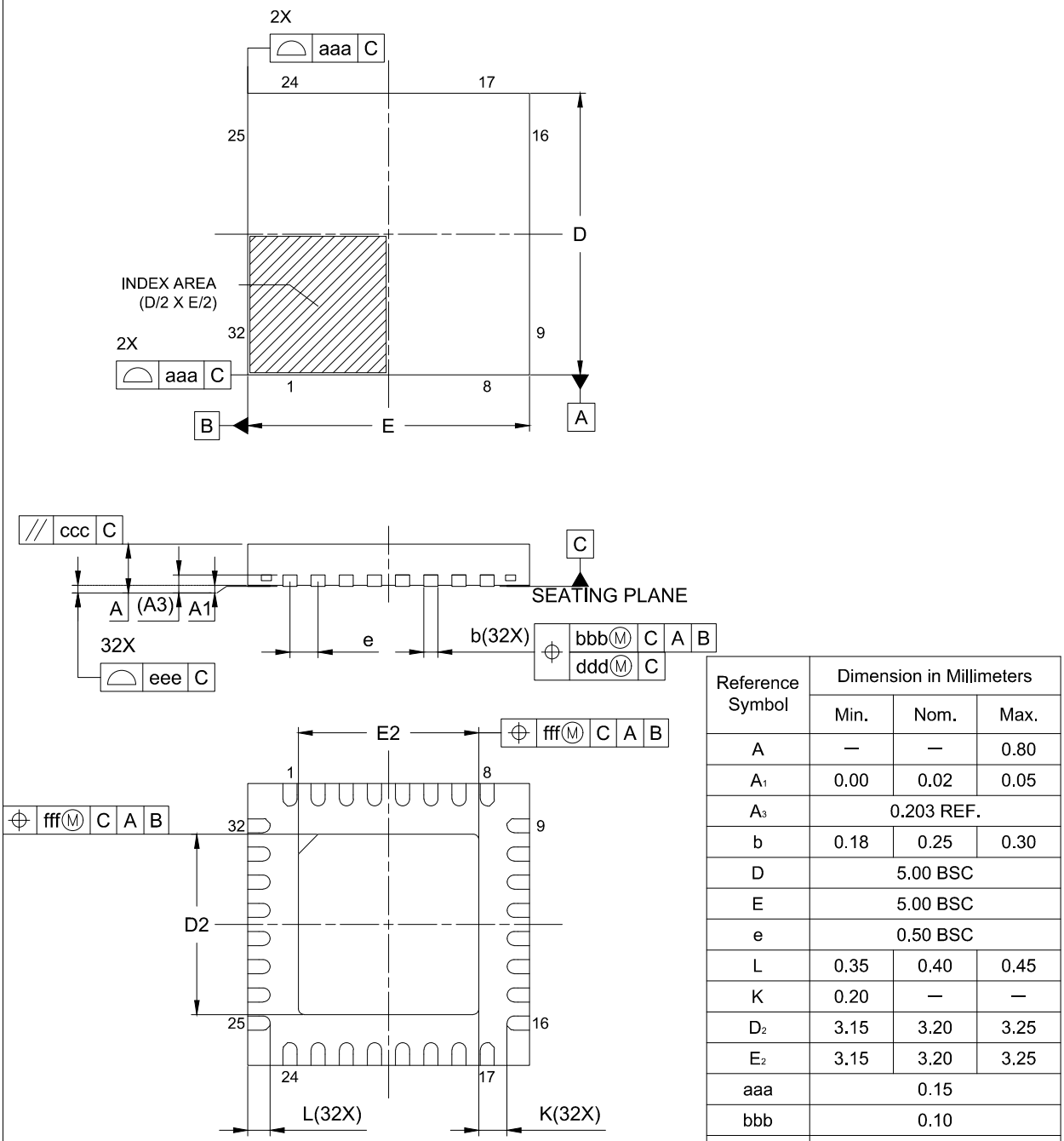
NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

Figure G 32-Pin LQFP (PLQP0032GB-A)

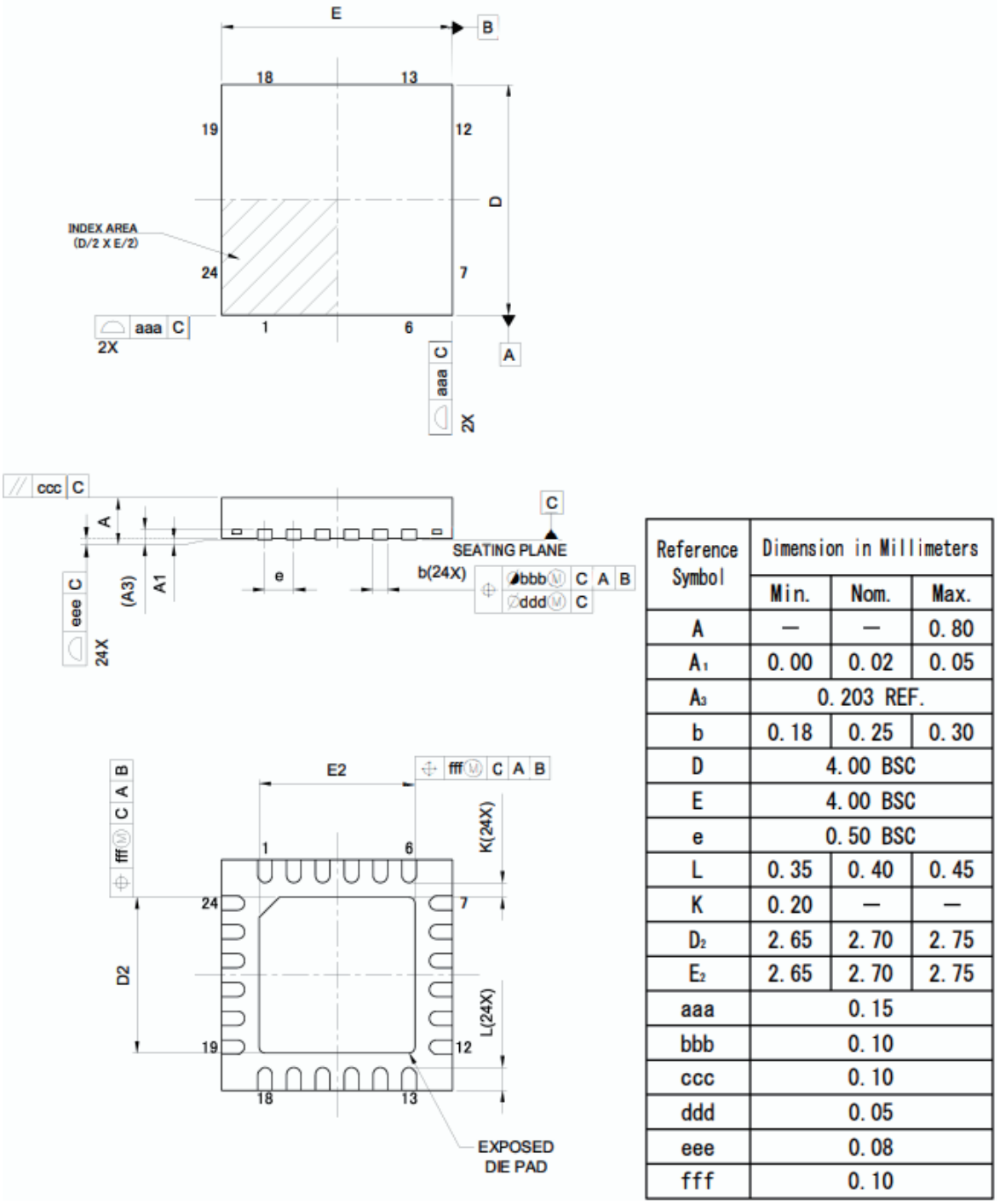
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure H 32-Pin HWQFN (PWQN0032KE-A)

JEITA Package Code	RENESAS Code	MASS (Typ.) [g]
P-HWQFN24-4×4-0.50	PWQN0024KG-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure I 24-Pin HWQFN (PWQN0024KG-A)

REVISION HISTORY	RX14T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Sep 30, 2025	—	First edition, issued	
1.01	Oct 22, 2025	—	52-pin package code, changed	
1.02	Dec 12, 2025	2. Electrical Characteristics		
		77	Table 2.48 A/D Conversion Characteristics (1) Note 1, changed, Note 2, deleted	
		78	Table 2.49 A/D Conversion Characteristics (2) Note 1, changed, Note 2, deleted	
		79	Table 2.50 A/D Conversion Characteristics (3) Note 1, changed, Note 2, deleted	
		83	Table 2.53 Programmable Gain Amplifier Characteristics, changed	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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