RX23E-A Group
Renesas MCUs

R01DS0330EJ0130
Rev.1.30
Dec 25, 2024

32-MHz, 32-bit RX MCUs with up to 256-KB flash memory,
2 low-noise and low-drift 24-bit delta-sigma A/D converters,
rail-to-rail programmable gain instrumentation amplifiers,
a low-drift voltage reference, and on-chip excitation current sources

Features

■ 32-bit RXv2 CPU core
- Max. operating frequency: 32 MHz
  Capable of 64 DMIPS in operation at 32 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit multiply-subtract instructions supported
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture
- Operation from a single 1.8-V to 5.5-V supply
- Three low power consumption modes
- Low power timer (LPT) that operates during the software standby state

■ On-chip flash memory for code
- Read cycle of 31.25 ns in 32-MHz operation
- No waiting time when the CPU is reading at full speed
- 128-Kbyte to 256-Kbyte capacities
- On-board or off-board user programming
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory
- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states
- 16- to 32-Kbyte size capacities

■ Data transfer functions
- DMAC: Incorporates four channels
- DTC: Four transfer modes

■ ELC
- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management
- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

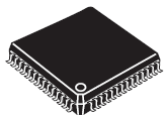
■ Clock functions
- Main clock oscillator frequency: 1 MHz to 20 MHz
- External clock input frequency: Up to 20 MHz
- PLL circuit input: 4 MHz to 8 MHz
- On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDT
- Clock frequency accuracy measurement circuit (CAC)

■ Independent watchdog timer
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

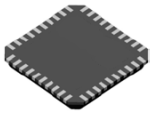
■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnect detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ MPC
- Input/output functions selectable from multiple pins

■ Up to eight communication functions
- CAN (one channel) compliant to ISO11898-1:
  Transfer at up to 1 Mbps
- SCI with many useful functions (up to four channels),
  asynchronous mode, clock synchronous mode, smart card interface, reduction of errors in communications using the bit rate modulation function
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps



PLQP0048KB-B 7 × 7 mm, 0.5 mm pitch



PWQN0040KD-A 6 × 6 mm, 0.5 mm pitch

■ Up to 12 extended-function timers
- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (two channels)

■ Analog functions
- Two 24-bit delta-sigma A/D converters
- A/D converter with up to 23-bit effective resolution (gain = 1, output data rate = 7.6 SPS)
- High-precision programmable gain instrumentation amplifier,
  30 nV_{RMS} (gain = 128, output data rate = 7.6 SPS)
- Rail-to-rail programmable gain instrumentation amplifier
  (gain = 1 to 128)
- Two operating modes and programmable data rates,
  Normal mode: Output data rate of 7.6 SPS to 15625 SPS,
  Low power mode: Output data rate of 1.9 SPS to 3906 SPS
- Offset drift 10 nV/°C (gain = 128)
- Gain drift 1 ppm/°C (gain = 1 (PGA), gain = 2 to 128)
- Up to six differential inputs, 11 single-ended inputs
- Fourth-order sinc filter
- Simultaneous 50 Hz/60 Hz rejection (output data rate = 10, 54 SPS)
- Offset error and gain error calibration
- Inter-unit A/D conversion synchronized start
- Delta-sigma A/D input disconnect detection assist
- Delta-sigma A/D reference voltage external input
- Voltage reference
  output voltage: 2.5 V,
  temperature drift: 10 ppm/°C, output current: ±10 mA
- Excitation current sources: Up to four,
  Output current: 50 µA to 1000 µA, current matching: ±0.2%, drift matching: 5 ppm/°C
- Bias voltage generator
  output voltage: (AVCC0 + AVSS0)/2
- Temperature sensor: Accuracy ±5°C
- Low-side switch: 10 Ω on-resistance
- Low power-supply-voltage detectors
- Delta-sigma A/D input voltage fault detectors
- Delta-sigma A/D reference voltage fault detectors and disconnect detectors
- Excitation current source disconnect detectors

■ 12-bit A/D converter
- Capable of conversion within 1.4 µs
- Six channels
- Sampling time can be set for each channel
- Self-diagnostic function and analog input disconnect detection assistance function

■ General I/O ports
- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Operating temperature range
- –40°C to +85°C
- –40°C to +105°C

■ Applications
- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 (variable-length instruction format) • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 128/256 Kbytes • 32 MHz: No-wait access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 16/32 Kbytes • 32 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) MTU2a runs in synchronization with the PCLKA: 32 MHz (at max.) The ADCLK for the S12AD runs in synchronization with the PCLKD: 32 MHz (at max.) Peripheral modules other than MTU2a and S12AD run in synchronization with the PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode • Low power timer that operates during the software standby state
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode and middle-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 256 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	48-pin/40-pin I/O: 20/16 • Input: 1/1 Pull-up resistors: 20/16 • Open-drain outputs: 20/16 • 5-V tolerance: 2/2
Event link controller (ELC)		• Event signals of 56 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode PWM/complementary PWM/reset synchronous PWM • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Low power timer (LPT)	• 16 bits × 1 channel • Clock source: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer

Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 4 channels (channel 1, 5, 6: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	Serial peripheral interface (RSPIb)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	CAN module (RSCAN)	• 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 Message boxes
24-bit delta-sigma A/D converter (DSAD)		• 24 bits (6 channels × 2 units) • Type of A/D conversion: delta-sigma • Post filter: Fourth-order sinc filter • 24-bit resolution • Input types: Differential, pseudo-differential, or single-ended • Operating modes Normal mode/low-power mode • Modulator clock: 500 kHz (typ.; 125 kHz in low-power mode) • Oversampling ratio: 32 to 65536 (only multiples of 16) • Includes a programmable gain instrumentation amplifier (PGA) Gain settings: ×1, ×2, ×4, ×8, ×16, ×32, ×64, ×128 PGA bypass function: with or without an analog input buffer • Configuration settings per channel • Conditions for starting A/D conversion: software trigger or ELC • Disconnect detection assist • Selectable reference voltage

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
Analog front end (AFE)		• Voltage reference (VREF) Output voltage: 2.5V • Output from bias voltage source (VBIAS) Output voltage: (AVCC0 + AVSS0)/2 • Internal temperature sensor (TEMPS) • Excitation current sources (IEXC) Two channels (up to 1000 µA) or four channels (up to 500 µA) Output current settings: 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, 1000 µA • Analog multiplexer (AMUX) Select from among external pins, bias voltage sources, internal temperature sensor, or excitation current sources • Low-side switch (LSW) On-resistance: 10 Ω (max.) Allowable current: 30 mA (max.) • Voltage detector (VDET) Voltage monitoring of AVCC0 Detection of abnormal voltages at analog inputs Detection of abnormal reference voltages and assistance in detecting disconnection Assistance in detecting disconnection for excitation current source output
12-bit A/D converter (S12ADE)		• 12 bits (6 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz AVCC0 = 2.7 to 5.5 V (1.8 to 5.5 V when only S12AD is operating)
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KD-A) 6 × 6 mm, 0.5 mm pitch
Debugging interface		One-wire type FINE interface

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX23E-A Group	
		48 Pins	**40 Pins**
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	
DMA	DMA controller	4 channels (DMAC0 to DMAC3)	
	Data transfer controller	Available	
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)	
	Port output enable 2	POE0# to POE3#, POE8#	
	8-bit timer	2 channels × 2 units	
	Compare match timer	2 channels × 1 unit	
	Low power timer	1 channel	
	Independent watchdog timer	Available	
Communication functions	Serial communications interfaces (SCIg)	3 channels (SCI1, 5, 6)	2 channels (SCI1, 5)
	Serial communications interfaces (SCIh)	1 channel (SCI12)	
	I^2C bus interface	1 channel	
	CAN module	1 channel	
	Serial peripheral interface	1 channel	
24-bit delta-sigma A/D converter		2 units, 6 channels of differential input	2 units, 4 channels of differential input
Analog front end	Voltage reference	Available	
	Excitation current sources	Available	
	Analog multiplexer	Available	
	Temperature sensor	Available	
	Voltage detector	Available	
12-bit A/D converter (including high-precision channels)		6 channels (6 channels)	4 channels (4 channels)
CRC calculator		Available	
Event link controller		Available	
Packages		48-pin LFQFP	40-pin HWQFN

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	DSAD	Operating Temperature
RX23E-A	R5F523E6ADFL	R5F523E6ADFL#30	PLQP0048KB-B	256 Kbytes	32 Kbytes	8 Kbytes	32 MHz	2 Units	–40 to +85°C
	R5F523E6ADNF	R5F523E6ADNF#20	PWQN0040KD-A						
	R5F523E5ADFL	R5F523E5ADFL#30	PLQP0048KB-B	128 Kbytes	16 Kbytes				
	R5F523E5ADNF	R5F523E5ADNF#20	PWQN0040KD-A						
	R5F523E6AGFL	R5F523E6AGFL#30	PLQP0048KB-B	256 Kbytes	32 Kbytes				–40 to +105°C
	R5F523E6AGNF	R5F523E6AGNF#20	PWQN0040KD-A						
	R5F523E5AGFL	R5F523E5AGFL#30	PLQP0048KB-B	128 Kbytes	16 Kbytes				
	R5F523E5AGNF	R5F523E5AGNF#20	PWQN0040KD-A						
	R5F523E6SDFL	R5F523E6SDFL#30	PLQP0048KB-B	256 Kbytes	32 Kbytes			1 Unit	–40 to +85°C
	R5F523E6SDNF	R5F523E6SDNF#20	PWQN0040KD-A						
	R5F523E5SDFL	R5F523E5SDFL#30	PLQP0048KB-B	128 Kbytes	16 Kbytes				
	R5F523E5SDNF	R5F523E5SDNF#20	PWQN0040KD-A						
	R5F523E6SGFL	R5F523E6SGFL#30	PLQP0048KB-B	256 Kbytes	32 Kbytes				–40 to +105°C
	R5F523E6SGNF	R5F523E6SGNF#20	PWQN0040KD-A						
	R5F523E5SGFL	R5F523E5SGFL#30	PLQP0048KB-B	128 Kbytes	16 Kbytes				
	R5F523E5SGNF	R5F523E5SGNF#20	PWQN0040KD-A						

Note: Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

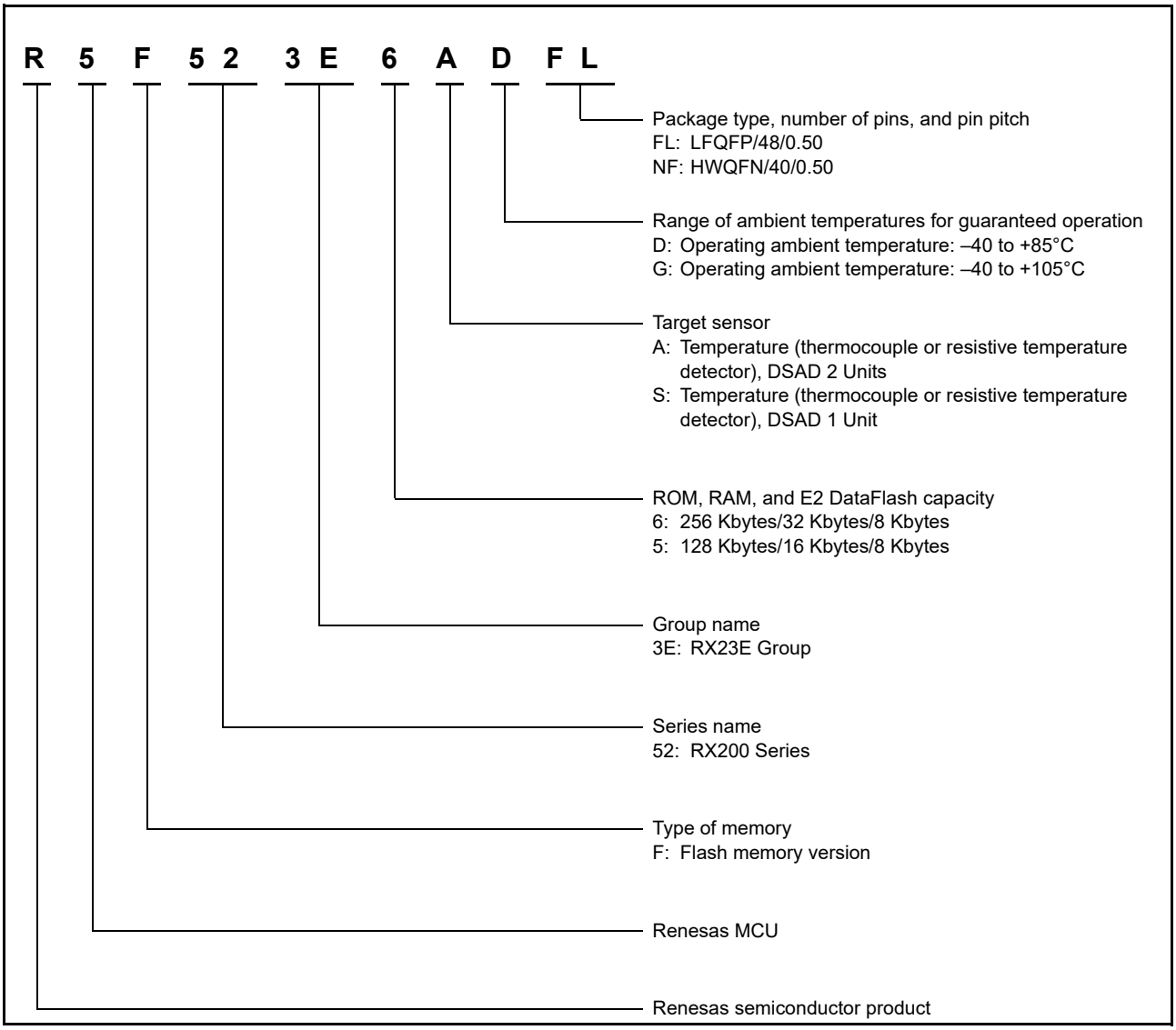


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram, and Figure 1.3 shows an analog block diagram.

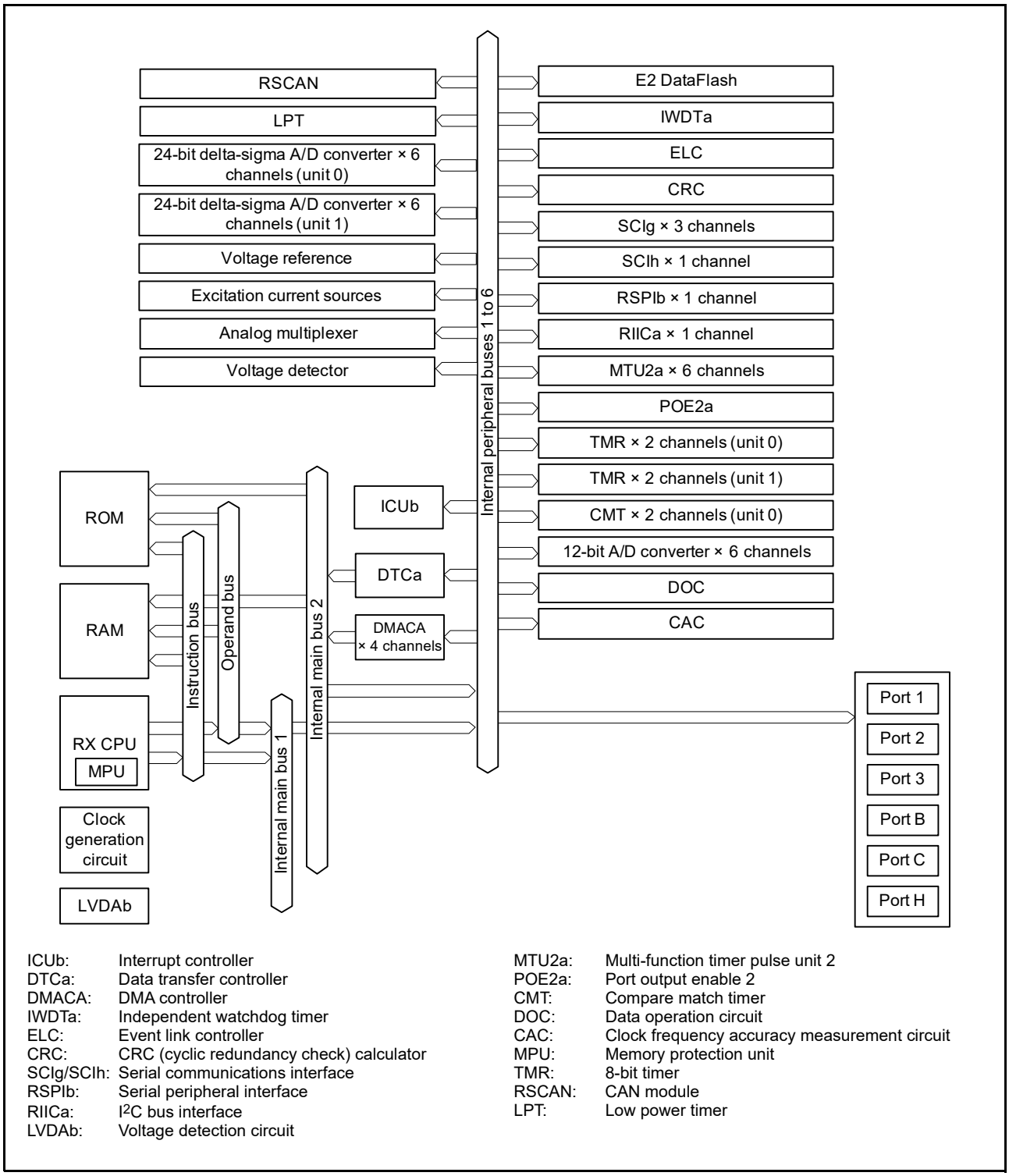


Figure 1.2 Block Diagram

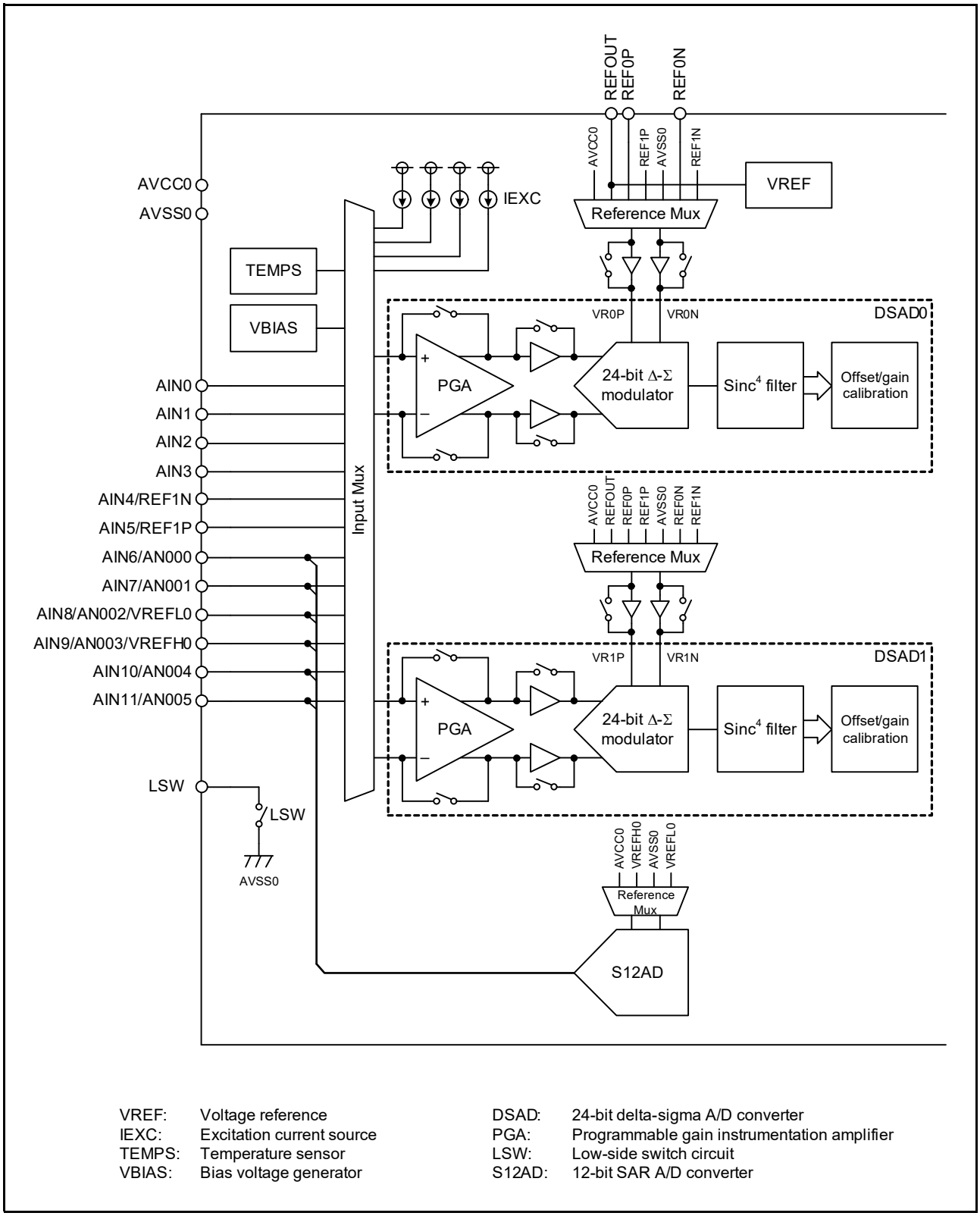


Figure 1.3 Analog Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6	Input	Input pins for received data.
	TXD1, TXD5, TXD6	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6	I/O	Input/output pins for the I^2C data.

Table 1.4 Pin Functions (2/3)

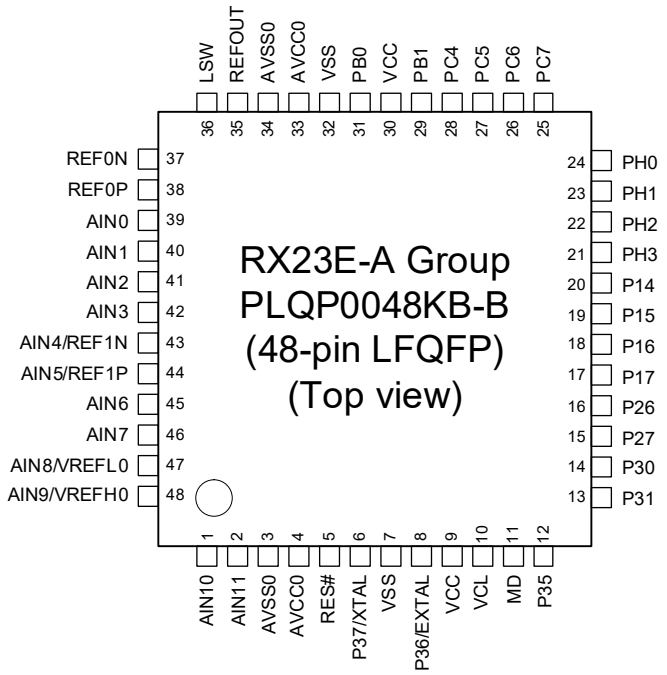
Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Simple SPI mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	SMISO1, SMISO5, SMISO6	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#	Input	Slave-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIh.
	TXDX12	Output	Output pin for data transmission by SCIh.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIh.
I^2C bus interface	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter	AN000 to AN005	Input	Analog input pins for the 12-bit A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
Analog front end	REF0P, REF1P	Input	Positive input pins of the reference voltage for the 24-bit delta-sigma A/D converter.
	REF0N, REF1N	Input	Negative input pins of the reference voltage for the 24-bit delta-sigma A/D converter.
	REFOUT	Output	Internal reference voltage output pin. Connect this to AVSS0 via a capacitor (0.47 μF) for stabilizing the internal reference voltage. Place the capacitor close to the pin.
	IEXC0 to IEXC3	Output	Excitation current source output pins.
	AIN0 to AIN11	I/O	Analog input/output pins.
	LSW	Output	Low-side-switch output pin.

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin. Connect this pin to VCC when not using.
	AVSS0	Input	Analog ground pin. Connect this pin to VSS when not using.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
I/O ports	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30, P31, P35 to P37	I/O	5-bit input/output pins (P35 input pin).
	PB0, PB1	I/O	2-bit input/output pins.
	PC4 to PC7	I/O	4-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.

1.5 Pin Assignments

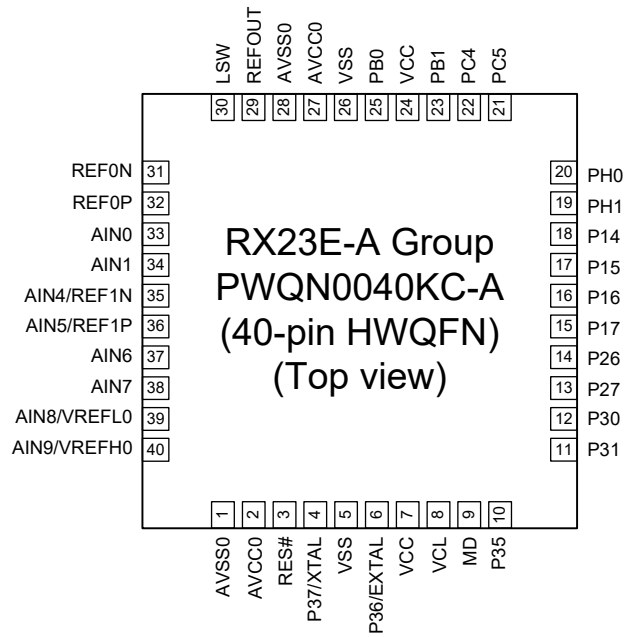
1.5.1 48-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 48-Pin LFQFP

1.5.2 40-Pin HWQFN



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (40-Pin HWQFN)”.
Note: It is recommended that the exposed die pad of HWQFN should be connected to VSS.

Figure 1.5 Pin Assignments of the 40-Pin HWQFN

1.6 List of Pins and Pin Functions

1.6.1 48-Pin LFQFP

Table 1.5 List of Pins and Pin Functions (48-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, VREF, IEXC, DSAD, AMUX)	Others
1					AIN10/AN004/ IEXC0 to IEXC3	
2					AIN11/AN005/ IEXC0 to IEXC3	
3	AVSS0					
4	AVCC0					
5	RES#					
6	XTAL	P37				
7	VSS					
8	EXTAL	P36				
9	VCC					
10	VCL					
11	MD					FINED
12		P35				NMI
13		P31	MTIOC1A/MTIOC4D/TMO3	CTS1#/RTS1#/SS1#		IRQ1
14		P30	MTIOC0A/MTIOC4B/TMCI3/ POE8#	RXD1/SMISO1/SSCL1		IRQ0
15		P27	MTIOC2B/MTIOC4A/TMRI3	SCK1		IRQ3
16		P26	MTIOC2A/MTIOC4C/TMO0	TXD1/SMOSI1/SSDA1		IRQ2
17		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
18		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL		IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1/SSLA1/ CRXD0		IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/SSLA3/ CTXD0		IRQ4
21		PH3	MTIC5W/MTCLKB/TMCI0/POE2#	CTS6#/RTS6#/SS6#/RSPCKA		
22		PH2	MTIC5V/MTCLKA/TMRI0	SCK5/MOSIA		IRQ1
23		PH1	MTIC5U/MTCLKD/TMO0/POE2#	TXD5/SMOSI5/SSDA5/SSLA0		IRQ0/CLKOUT
24		PH0	MTIOC0D/MTCLKC/TMRI0/ CACREF	RXD5/SMISO5/SSCL5/SSLA2		
25		PC7	MTIOC3A/MTCLKB/TMO2/ CACREF	TXD6/SMOSI6/SSDA6/MISOA		
26		PC6	MTIOC3C/MTCLKA/TMCI2	RXD6/SMISO6/SSCL6/MOSIA		
27		PC5	MTIOC3B/MTCLKD/TMRI2	SCK5/SCK6/SCK12/RSPCKA		
28		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA0		
29		PB1	MTIOC1B/MTIOC2A/TMRI1/ POE1#	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12		
30	VCC					
31		PB0	MTIOC0C/TMCI0/POE3#	RXD12/RXDX12/SMISO12/ SSCL12		IRQ4
32	VSS					
33	AVCC0					
34	AVSS0					
35					REFOUT	
36					LSW	
37					REF0N	
38					REF0P	
39					AIN0/IEXC0 to IEXC3	
40					AIN1/IEXC0 to IEXC3	
41					AIN2/IEXC0 to IEXC3	

Table 1.5 List of Pins and Pin Functions (48-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, VREF, IEXC, DSAD, AMUX)	Others
42					AIN3/IEXC0 to IEXC3	
43					AIN4/IEXC0 to IEXC3/REF1N	
44					AIN5/IEXC0 to IEXC3/REF1P	
45					AIN6/AN000/ IEXC0 to IEXC3	
46					AIN7/AN001/ IEXC0 to IEXC3	
47	VREFL0				AIN8/AN002/ IEXC0 to IEXC3	
48	VREFH0				AIN9/AN003/ IEXC0 to IEXC3	

1.6.2 40-Pin HWQFN

Table 1.6 List of Pins and Pin Functions (40-Pin HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, VREF, IEXC, DSAD, AMUX)	Others
1	AVSS0					
2	AVCC0					
3	RES#					
4	XTAL	P37				
5	VSS					
6	EXTAL	P36				
7	VCC					
8	VCL					
9	MD					FINED
10		P35				NMI
11		P31	MTIOC1A/MTIOC4D/TMO3	CTS1#/RTS1#/SS1#		IRQ1
12		P30	MTIOC0A/MTIOC4B/TMCI3/ POE8#	RXD1/SMISO1/SSCL1		IRQ0
13		P27	MTIOC2B/MTIOC4A/TMRI3	SCK1		IRQ3
14		P26	MTIOC2A/MTIOC4C/TMO0	TXD1/SMOSI1/SSDA1		IRQ2
15		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
16		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL		IRQ6/ADTRG0#
17		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1/SSLA1/ CRXD0		IRQ5
18		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/SSLA3/ CTXD0		IRQ4
19		PH1	MTCLKD/TMO0/POE2#	TXD5/SMOSI5/SSDA5/SSLA0		IRQ0/CLKOUT
20		PH0	MTIOC0D/MTCLKC/TMRI0/ CACREF	RXD5/SMISO5/SSCL5/SSLA2		
21		PC5	MTIOC3B/MTCLKD/TMRI2	SCK5/SCK12/RSPCKA		
22		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA0		
23		PB1	MTIOC1B/MTIOC2A/TMRI1/ POE1#	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12		
24	VCC					
25		PB0	MTIOC0C/TMCI0/POE3#	RXD12/RXDX12/SMISO12/ SSCL12		IRQ4
26	VSS					
27	AVCC0					
28	AVSS0					
29					REFOUT	
30					LSW	
31					REF0N	
32					REF0P	
33					AIN0/IEXC0 to IEXC3	
34					AIN1/IEXC0 to IEXC3	
35					AIN4/IEXC0 to IEXC3/REF1N	
36					AIN5/IEXC0 to IEXC3/REF1P	
37					AIN6/AN000/ IEXC0 to IEXC3	
38					AIN7/AN001/ IEXC0 to IEXC3	
39	VREFL0				AIN8/AN002/ IEXC0 to IEXC3	
40	VREFH0				AIN9/AN003/ IEXC0 to IEXC3	

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	P16 and P17 (5-V tolerant)	V_{in}	–0.3 to +6.5	V
	Ports other than above		–0.3 to VCC + 0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage		V_{AN}	–0.3 to AVCC0 + 0.3	V
Reference voltage for 24-bit delta-sigma A/D converter		REF0P, REF1P	–0.3 to AVCC0 + 0.3	V
		REF0N, REF1N	–0.3 to AVCC0 + 0.3	
Junction temperature	D version	T_j	–40 to +105	°C
	G version		–40 to +112	
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Exceeding absolute maximum ratings may permanently damage the MCU.
To preclude malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors with values of about 0.1 µF as close as possible to every power supply pin and use the shortest and widest possible traces.
Connect the VCL pin to a VSS pin via a 4.7-µF capacitor. The capacitor must be placed close to the pin. For details, refer to section 2.12.1, Connecting VCL Capacitor and Bypass Capacitors.
Do not input signals to ports other than 5-V tolerant ports while power is not being supplied to the MCU.
The current injection that results from the input of such a signal may lead to malfunctions and the abnormal current that passes through the MCU at such times may cause degradation of internal elements.
However, even if –0.3 to +6.5 V is input to a 5-V tolerant port, this will not cause problems such as damage to the MCU.

2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltages		VCC*1, *2	1.8	—	5.5	V
		VSS	—	0	—	
Analog power supply voltages		AVCC0*1, *2	1.8	—	5.5	V
		AVSS0	—	0	—	
		VREFH0	1.8	—	AVCC0	
		VREFL0	—	0	—	
Input voltage	Ports for 5 V tolerant: P16, P17	V_{in}	–0.3	—	5.8	V
	AIN0 to AIN11, REF0N, REF0P, REF1N, REF1P		–0.3	—	AVCC0 + 0.3	
	Ports other than above		–0.3	—	VCC + 0.3	
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	

Note 1. Use AVCC0 and VCC under the following conditions:
While VCC > 2.4 V: AVCC0 and VCC can be set independently when AVCC0 ≥ 2.4 V
While VCC ≤ 2.4 V: AVCC0 and VCC can be set independently when AVCC0 ≥ VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
VCL pin external capacitance	C_{VCL}	4.7 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 4.7 µF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5-V tolerant)	V_{IH}	0.7 × VCC	—	5.8	V	
	P16 and P17 (5-V tolerant)		0.8 × VCC	—	5.8		
	P14, P15, P26, P27, P30, P31, P35 to P37, PB0, PB1, PC4 to PC7, PH0 to PH3, and RES#		0.8 × VCC	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	0.3 × VCC		
	Other than RIIC input pin		–0.3	—	0.2 × VCC		
Hysteresis of Schmitt trigger input	RIIC input pin (except for SMBus)	ΔV_T	0.05 × VCC	—	—		
	P16 and P17		0.05 × VCC	—	—		
	Other than RIIC input pin		0.1 × VCC	—	—		
High-level input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	0.9 × VCC	—	VCC + 0.3	V	
	EXTAL (external clock input)		0.8 × VCC	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
Low-level input voltage (except for Schmitt trigger input pins)	MD	V_{IL}	–0.3	—	0.1 × VCC		
	EXTAL (external clock input)		–0.3	—	0.2 × VCC		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 2.5 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P16 and P17 (5-V tolerant)	V_{IH}	0.8 × VCC	—	5.8	V	
	P14, P15, P26, P27, P30, P31, P35 to P37, PB0, PB1, PC4 to PC7, PH0 to PH3, and RES#		0.8 × VCC	—	VCC + 0.3		
	P14 to P17, P26, P27, P30, P31, P35 to P37, PB0, PB1, PC4 to PC7, PH0 to PH3, and RES#	V_{IL}	–0.3	—	0.2 × VCC		
Hysteresis of Schmitt trigger input	P14 to P17, P26, P27, P30, P31, P35 to P37, PB0, PB1, PC4 to PC7, PH0 to PH3, and RES#	ΔV_T	0.01 × VCC	—	—		
High-level input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	0.9 × VCC	—	VCC + 0.3	V	
	EXTAL (external clock input)		0.8 × VCC	—	VCC + 0.3		
Low-level input voltage (except for Schmitt trigger input pins)	MD	V_{IL}	–0.3	—	0.1 × VCC		
	EXTAL (external clock input)		–0.3	—	0.2 × VCC		

Table 2.6 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, and P35	$\|I_{in}\|$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	P16 and P17	$\|I_{TSI}\|$	—	—	1.0	μA	V_{in} = 0 V, 5.8V
	Ports other than P16 and P17		—	—	0.2		V_{in} = 0 V, VCC
Input capacitance	P14 to P17, P26, P27, P30, P31, P36, P37, PB0, PB1, PC4 to PC7, PH0 to PH3, MD, and RES#	C_{in}	—	—	15	pF	V_{in} = 20 mV, f = 1 MHz, T_a = 25°C
	P35		—	—	30		
Output voltage of the VCL pin		V_{CL}	—	2.12	—	V	

Table 2.7 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for P35)	R_U	10	20	50	kΩ	V_{in} = 0 V

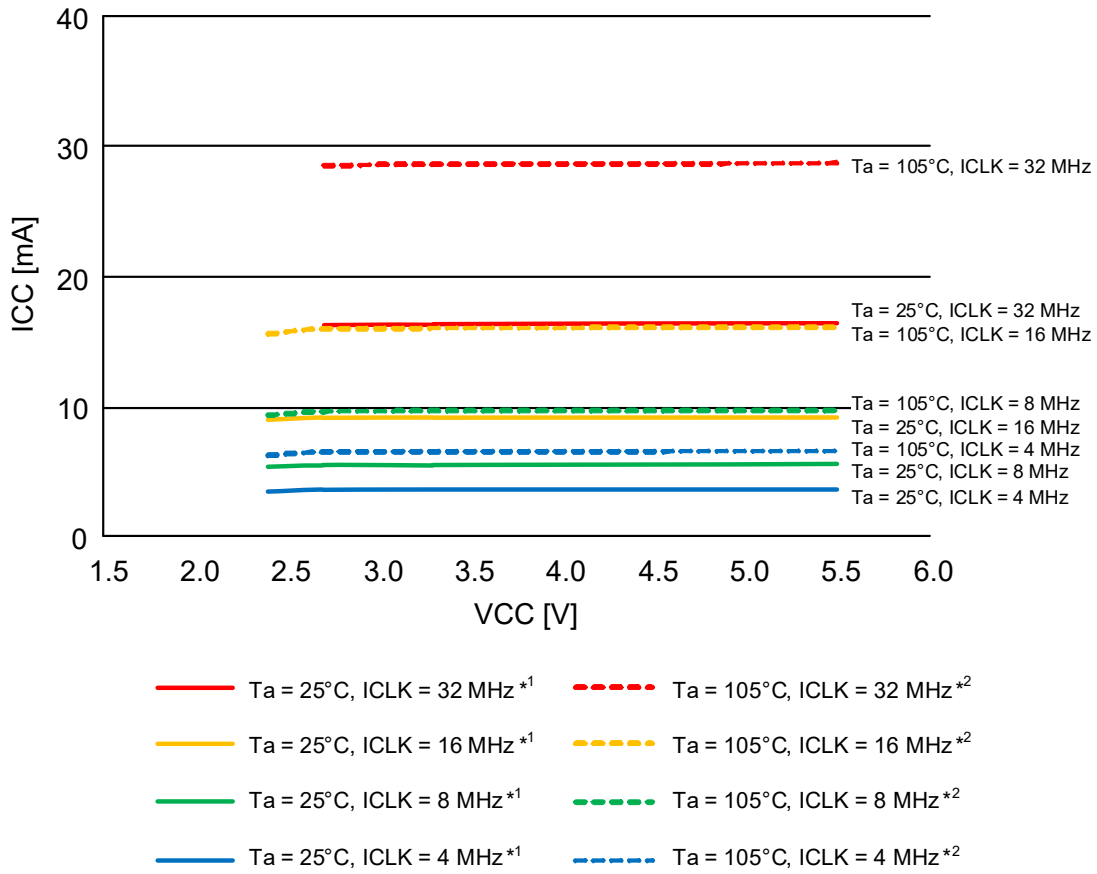
Table 2.8 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral modules are operating.*2	ICLK = 32 MHz	I_{CC}	4.1	—	mA	
				ICLK = 16 MHz		2.9	—		
				ICLK = 8 MHz		2.2	—		
				ICLK = 4 MHz		1.9	—		
			All peripheral modules are in normal operation.	ICLK = 32 MHz*3		16.3	—		
				ICLK = 16 MHz*3		9.1	—		
				ICLK = 8 MHz*3		5.5	—		
				ICLK = 4 MHz*3		3.7	—		
			All peripheral modules are in full operation.	ICLK = 32 MHz*3		—	30.3		
		Sleep mode	No peripheral modules are operating.*2	ICLK = 32 MHz		2.4	—		
				ICLK = 16 MHz		1.9	—		
				ICLK = 8 MHz		1.6	—		
				ICLK = 4 MHz		1.5	—		
			All peripheral modules are in normal operation.	ICLK = 32 MHz*3		8.9	—		
				ICLK = 16 MHz*3		5.4	—		
				ICLK = 8 MHz*3		3.5	—		
				ICLK = 4 MHz*3		2.5	—		
		Deep sleep mode	No peripheral modules are operating.*2	ICLK = 32 MHz		1.5	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.2	—		
				ICLK = 4 MHz		1.2	—		
			All peripheral modules are in normal operation.	ICLK = 32 MHz*3		7.2	—		
				ICLK = 16 MHz*3		4.4	—		
				ICLK = 8 MHz*3		2.8	—		
				ICLK = 4 MHz*3		2.1	—		
		Increase during BGO operation*5				2.5	—		

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current *1	Middle-speed operating mode	Normal operating mode	No peripheral modules are operating.*6	ICLK = 12 MHz	I_{CC}	2.1	—	mA	
				ICLK = 8 MHz		1.7	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 1 MHz		1.1	—		
			All peripheral modules are in normal operation.*7	ICLK = 12 MHz		6.8	—		
				ICLK = 8 MHz		5.0	—		
				ICLK = 4 MHz		3.1	—		
				ICLK = 1 MHz		1.6	—		
			All peripheral modules are in full operation.*7	ICLK = 12 MHz		—	13.5		
		Sleep mode	No peripheral modules are operating.*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		1.2	—		
				ICLK = 4 MHz		1.1	—		
				ICLK = 1 MHz		1.0	—		
			All peripheral modules are in normal operation.*7	ICLK = 12 MHz		4.0	—		
				ICLK = 8 MHz		3.0	—		
				ICLK = 4 MHz		2.1	—		
				ICLK = 1 MHz		1.3	—		
		Deep sleep mode	No peripheral modules are operating.*6	ICLK = 12 MHz		1.0	—		
				ICLK = 8 MHz		0.9	—		
				ICLK = 4 MHz		0.9	—		
				ICLK = 1 MHz		0.8	—		
			All peripheral modules are in normal operation.*7	ICLK = 12 MHz		3.3	—		
				ICLK = 8 MHz		2.6	—		
				ICLK = 4 MHz		1.8	—		
				ICLK = 1 MHz		1.2	—		
		Increase during BGO operation*5				2.5	—		

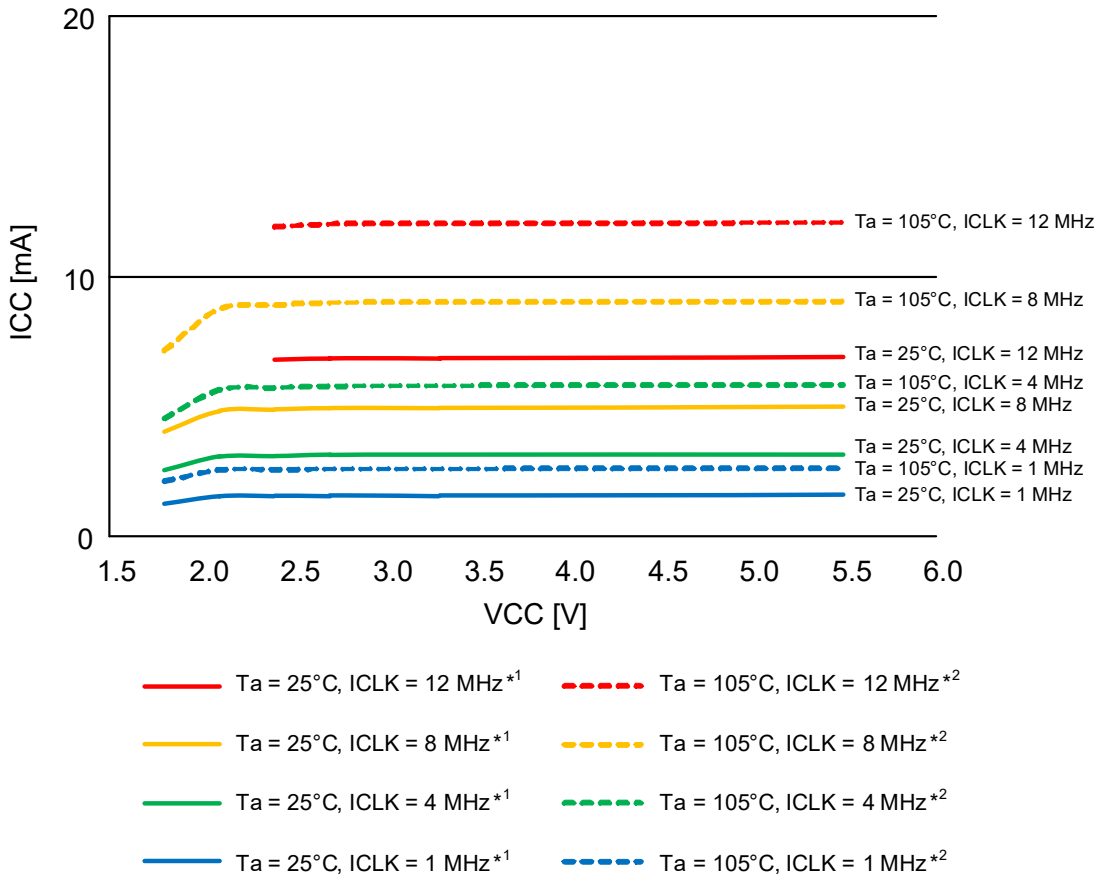
Note 1. Supply current values do not include the output charge/discharge current from all pins. The values apply when internal pull-up resistors are disabled.
Note 2. Peripheral module clocks are stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.
Note 3. Peripheral module clocks are supplied. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are the same frequency as that of ICLK.
Note 4. Conditions for typical values are at VCC = 3.3 V and T_a = 25°C.
Note 5. The increase is caused by program/erase operation to the ROM or E2 DataFlash during the execution of a user program.
Note 6. Peripheral module clocks are stopped. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK and PCLK are set to divided by 64.
Note 7. Peripheral module clocks are supplied. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK and PCLK are the same frequency of that of the ICLK.



Note 1. This result applies when all peripheral modules are in normal operation but BGO is not in use. Indicates the average of the typical samples through actual measurement during product evaluation.

Note 2. This result applies when all peripheral modules are in full operation but BGO is not in use. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 2.1 Voltage Dependence in High-Speed Operating Mode (Reference Data)



Note 1. This result applies when all peripheral modules are in normal operation but BGO is not in use. Indicates the average of the typical samples through actual measurement during product evaluation.

Note 2. This result applies when all peripheral modules are in full operation but BGO is not in use. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

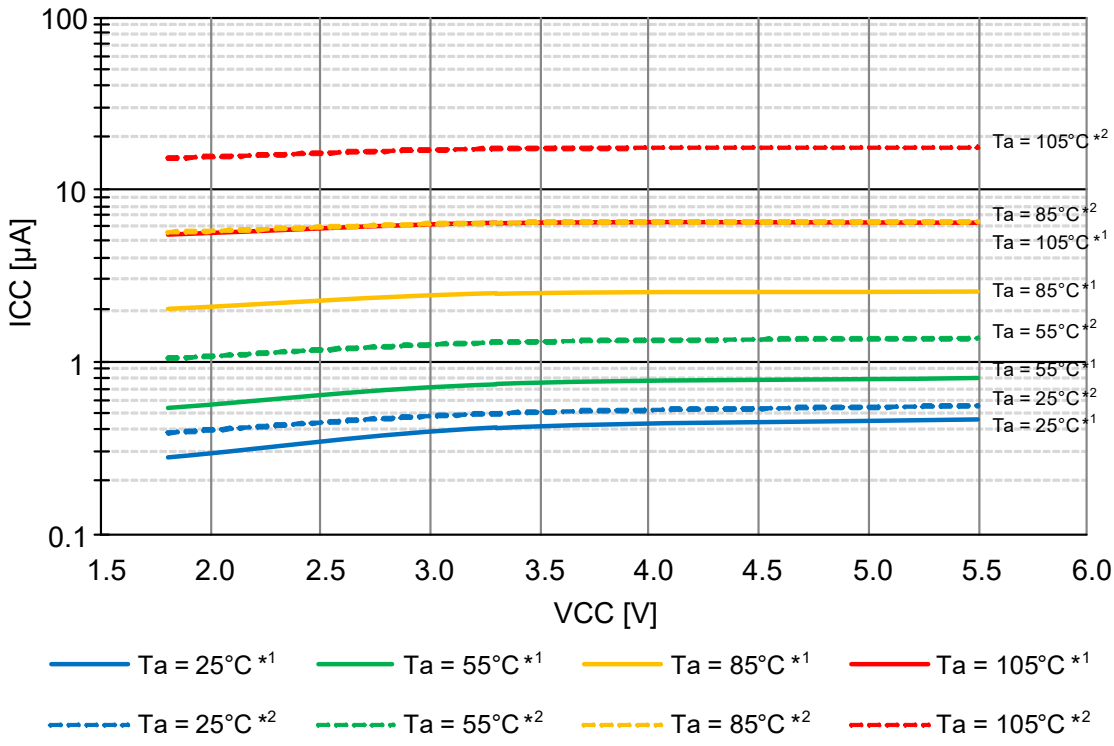
Figure 2.2 Voltage Dependence in Middle-Speed Operating Mode (Reference Data)

Table 2.9 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.4	2.6	µA	
		T_a = 55°C		0.8	3.0		
		T_a = 85°C		2.5	12.6		
		T_a = 105°C		6.3	31.2		
	Increment for IWDT operation			0.4	—		
	Increment for LPT operation			0.4	—		Use IWDT-Dedicated On-Chip Oscillator for clock source

Note 1. Supply current values were obtained with no load on any output pin and all internal pull-up resistors disabled.
Note 2. The IWDT and LVD are stopped.
Note 3. Conditions for typical values are at VCC = 3.3 V.



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 2.3 Voltage Dependence in Software Standby Mode (Reference Data)

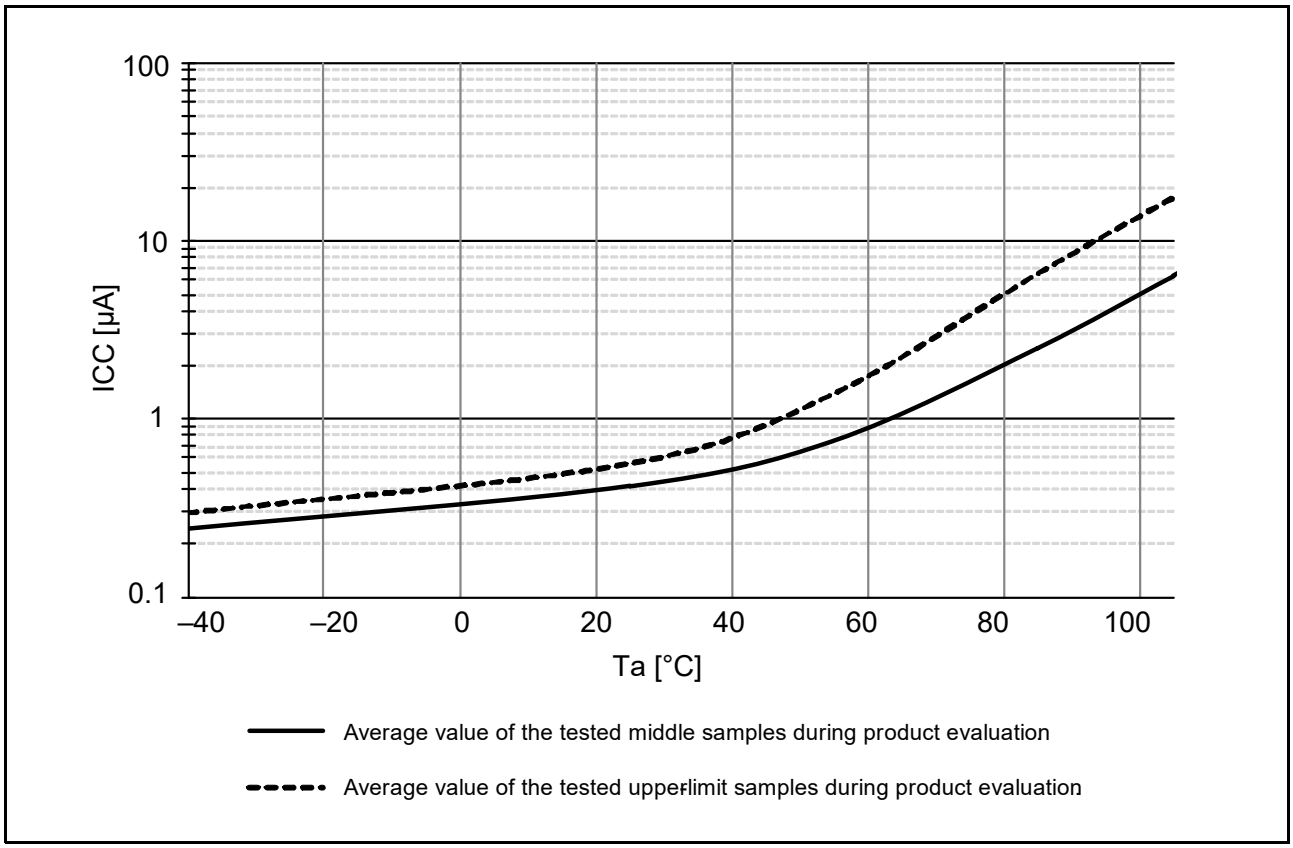


Figure 2.4 Temperature Dependence in Software Standby Mode (Reference Data)

Table 2.10 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
LVD	LVD0	I_{LVD}	—	0.10	—	µA	
	LVD1		—	0.10	—		
	LVD2		—	0.20	—		

Note 1. Conditions for typical values are at VCC = AVCC0 = 3.3 V and T_a = 25°C.

Table 2.11 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 2.12 DC Characteristics (9)

Conditions: 0 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC ramp-up rate at power-on	At normal startup*1	SrVCC	0.02	—	20.00	ms/V	
	During fast startup time*2		0.02	—	2.00		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When the OFS1.LVDAS and OFS1.FASTSTUP bits are 1
Note 2. When the OFS1.LVDAS bit is 1 and the OFS1.FASTSTUP bit is 0
Note 3. When the OFS1.LVDAS bit is 0
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 2.13 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

The result of any ripple must be within the limit on allowable ripple frequency $f_{r\,(VCC)}$ where the ripple voltage is within the range between the VCC upper limit and lower limit. The result of any ripple must be within the limit on the allowable VCC ramp rate in power fluctuation (dt/dVCC) where the change in VCC exceeds VCC ±10%.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 2.5 $V_{r\,(VCC)}$ ≤ 0.2 × VCC
		—	—	1	MHz	Figure 2.5 $V_{r\,(VCC)}$ ≤ 0.08 × VCC
		—	—	10	MHz	Figure 2.5 $V_{r\,(VCC)}$ ≤ 0.06 × VCC
Allowable VCC ramp rate at power fluctuation	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

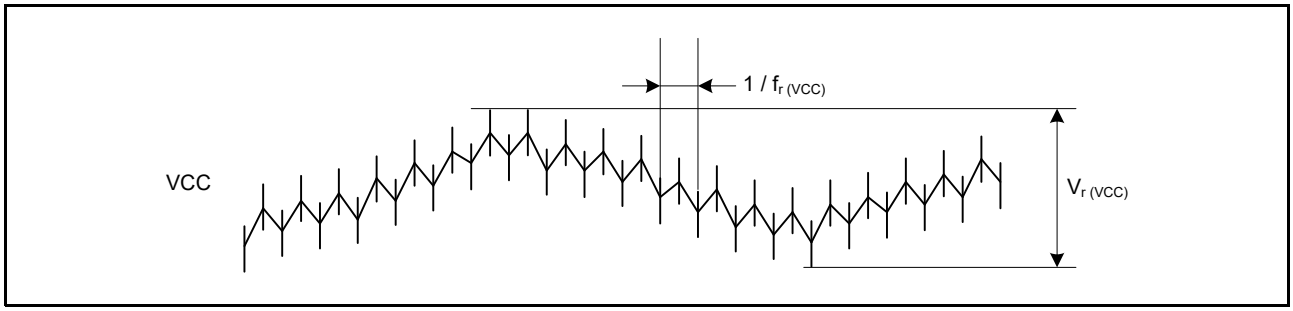


Figure 2.5 Ripple Waveform

Table 2.14 DC Characteristics (11)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating current of 24-bit delta-sigma A/D converter (normal mode)	Gain = 1 (PGA disabled, BUF disabled) OPCR.DSADLVM bit = 0	I_{AVCC0} (DSAD)	—	500*1	660	µA	Figure 2.6, Figure 2.7 1 unit, external reference in use, reference buffer disabled, AVCC0 = 3.6 to 5.5 V
	Gain = 1 to 16 (PGA enabled) OPCR.DSADLVM bit = 0		—	840*1	1130		
	Gain = 32 to 128 OPCR.DSADLVM bit = 0		—	1050*1	1360		
	Gain = 1 (PGA disabled, BUF disabled) OPCR.DSADLVM bit = 1		—	490*2	850		Figure 2.8, Figure 2.9 1 unit, external reference in use, reference buffer disabled, AVCC0 = 2.7 to 5.5 V
	Gain = 1 to 16 (PGA enabled) OPCR.DSADLVM bit = 1		—	820*2	1320		
	Gain = 32 to 128 OPCR.DSADLVM bit = 1		—	1040*2	1560		
Operating current of 24-bit delta-sigma A/D converter (low power mode)	Gain = 1 (PGA disabled, BUF disabled) OPCR.DSADLVM bit = 0		—	250*1	280	µA	Figure 2.10, Figure 2.11 1 unit, external reference in use, reference buffer disabled, AVCC0 = 3.6 to 5.5 V
	Gain = 1 to 16 (PGA enabled) OPCR.DSADLVM bit = 0		—	390*1	480		
	Gain = 32 to 128 OPCR.DSADLVM bit = 0		—	430*1	520		
	Gain = 1 (PGA disabled, BUF disabled) OPCR.DSADLVM bit = 1		—	240*2	350		Figure 2.12, Figure 2.13 1 unit, external reference in use, reference buffer disabled, AVCC0 = 2.7 to 5.5 V
	Gain = 1 to 16 (PGA enabled) OPCR.DSADLVM bit = 1		—	380*2	550		
	Gain = 32 to 128 OPCR.DSADLVM bit = 1		—	420*2	590		
Operating current of voltage reference		I_{AVCC0} (VREF)	—	45	75	µA	Figure 2.18
Operating current of temperature sensor		I_{AVCC0} (TEMPS)	—	15	40	µA	Figure 2.19
Operating current of bias voltage generator		I_{AVCC0} (VBIAS)	—	15	25	µA	Figure 2.20
Operating current of excitation current source		I_{AVCC0} (IEXC)	—	55	70	µA	Figure 2.21
Operating current of analog input buffer	Normal mode	I_{AVCC0} (BUF)	—	85	130	µA	Figure 2.14, 1 unit
	Low power mode		—	25	40		Figure 2.15, 1 unit
Operating current of reference buffer	Normal mode	I_{AVCC0} (REFBUF)	—	85	130	µA	Figure 2.16, 1 unit
	Low power mode		—	25	40		Figure 2.17, 1 unit
Operating current of voltage detector	Low voltage detector for power supply	I_{AVCC0} (LVDET)	—	5	9	µA	1 unit
	Excitation current source disconnect detector	I_{AVCC0} (IEXCDET)	—	1	2		
	DSAD input voltage fault detector	I_{AVCC0} (DSIDET)	—	5	7		
	DSAD reference voltage fault detector	I_{AVCC0} (DSRDET)	—	10	15		

Note 1. Conditions for this value is at AVCC0 = 5.0 V and T_a = 25°C.
Note 2. Conditions for this value is at AVCC0 = 3.3 V and T_a = 25°C.

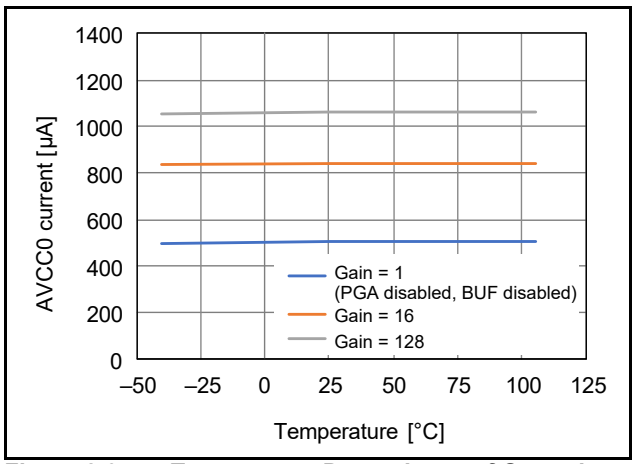


Figure 2.6 Temperature Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (AVCC0 = 5.0 V, Normal Mode, OPCR.DSADLVM bit = 0)

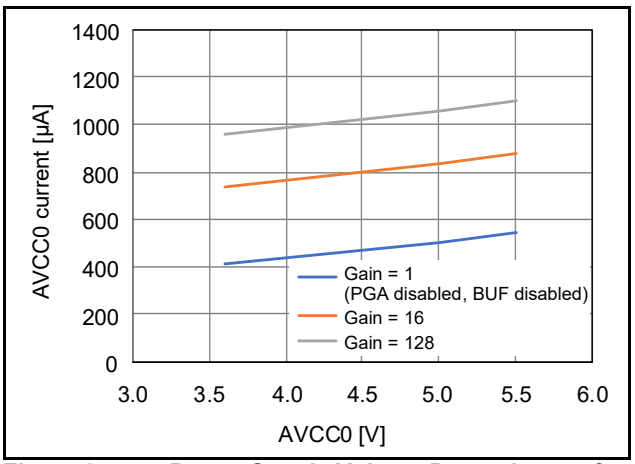


Figure 2.7 Power-Supply Voltage Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (T_a = 25°C, Normal Mode, OPCR.DSADLVM bit = 0)

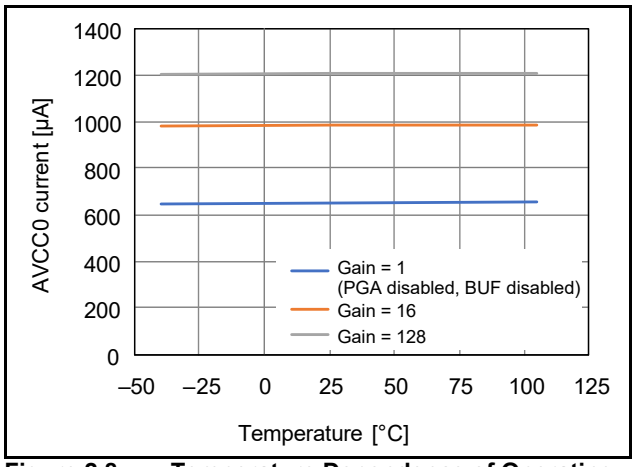


Figure 2.8 Temperature Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (AVCC0 = 5.0 V, Normal Mode, OPCR.DSADLVM bit = 1)

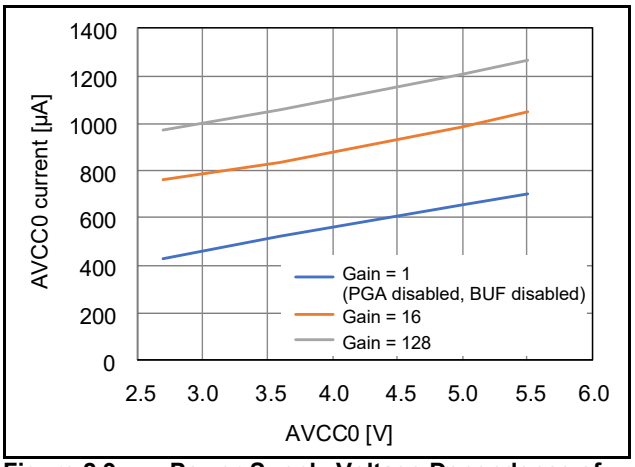


Figure 2.9 Power-Supply Voltage Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (T_a = 25°C, Normal Mode, OPCR.DSADLVM bit = 1)

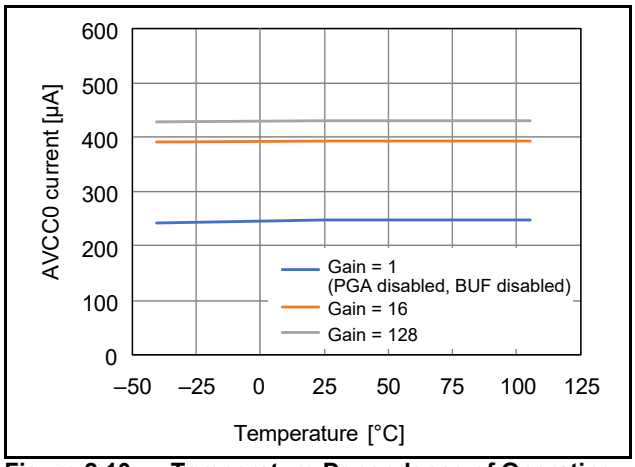


Figure 2.10 Temperature Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (AVCC0 = 5.0 V, Low Power Mode, OPCR.DSADLVM bit = 0)

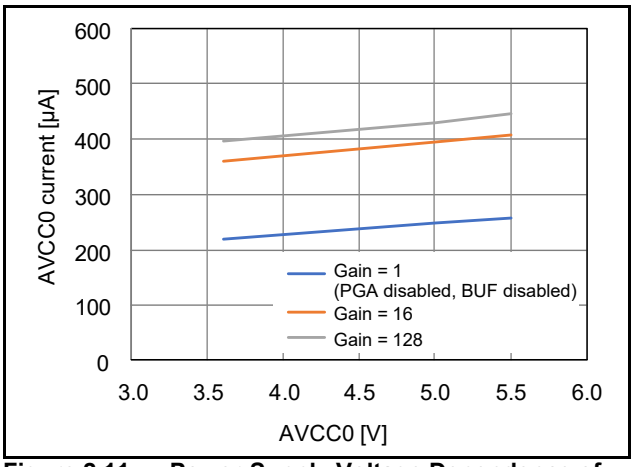


Figure 2.11 Power-Supply Voltage Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (T_a = 25°C, Low Power Mode, OPCR.DSADLVM bit = 0)

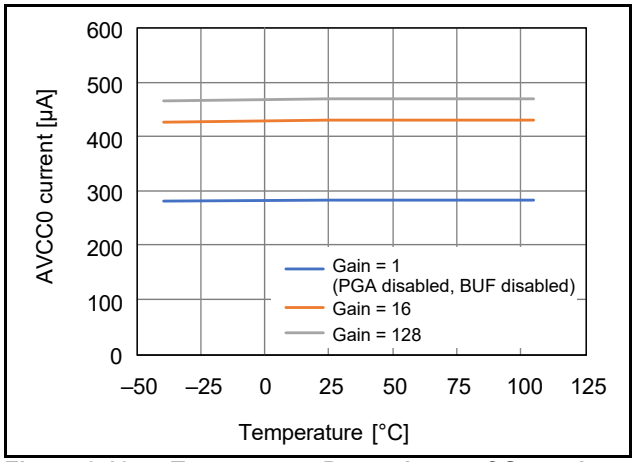


Figure 2.12 Temperature Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (AVCC0 = 5.0 V, Low Power Mode, OPCR.DSADLVM bit = 1)

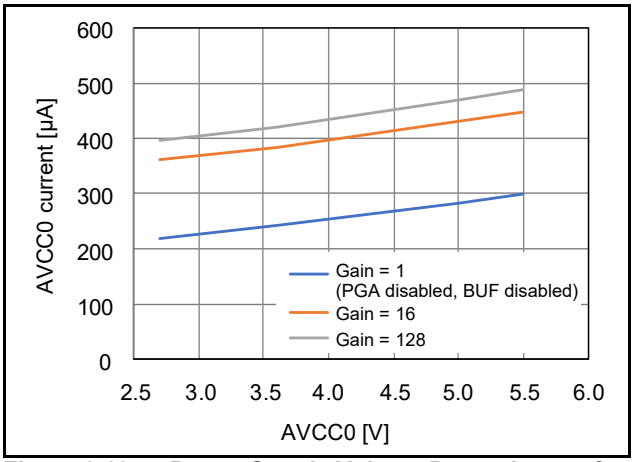


Figure 2.13 Power-Supply Voltage Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (T_a = 25°C, Low Power Mode, OPCR.DSADLVM bit = 1)

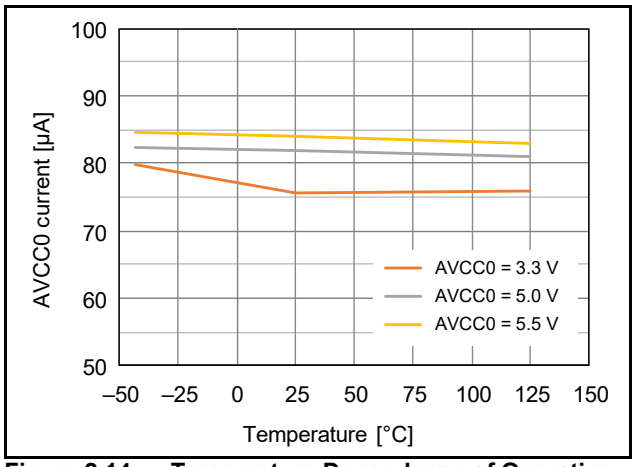


Figure 2.14 Temperature Dependence of Operating Current of Analog Input Buffer (Normal Mode)

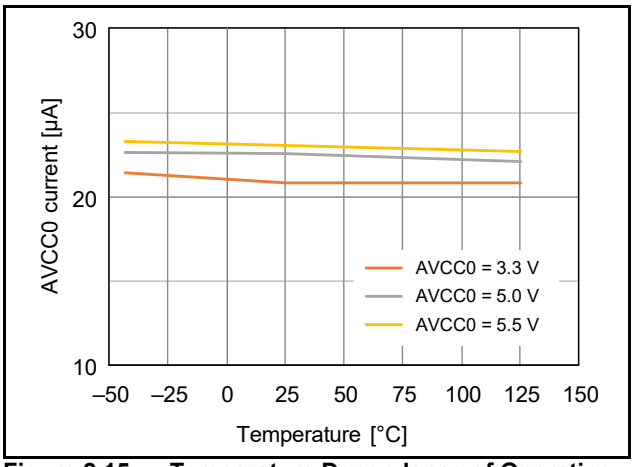


Figure 2.15 Temperature Dependence of Operating Current of Analog Input Buffer (Low Power Mode)

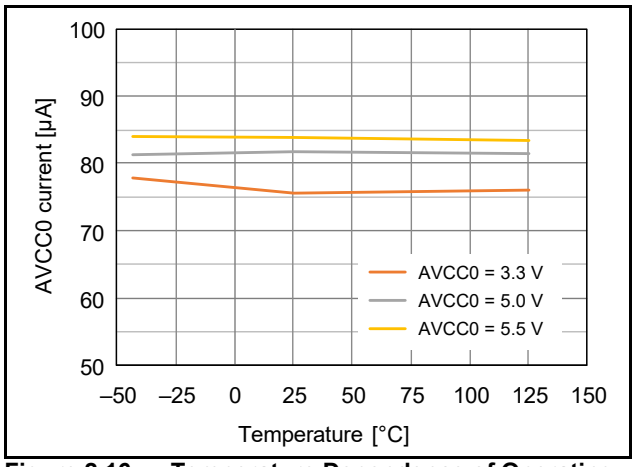


Figure 2.16 Temperature Dependence of Operating Current of Reference Buffer (Normal Mode)

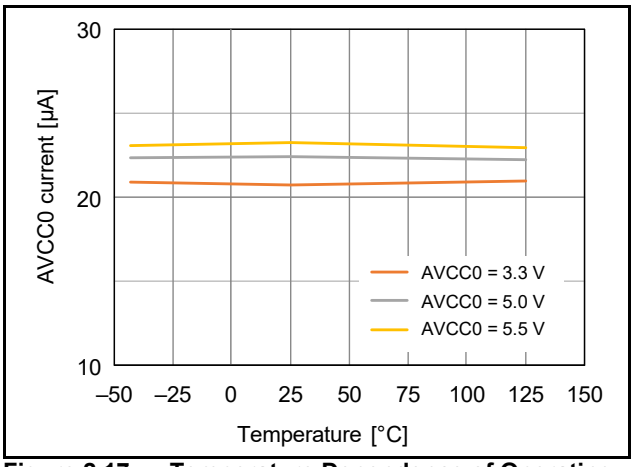


Figure 2.17 Temperature Dependence of Operating Current of Reference Buffer (Low Power Mode)

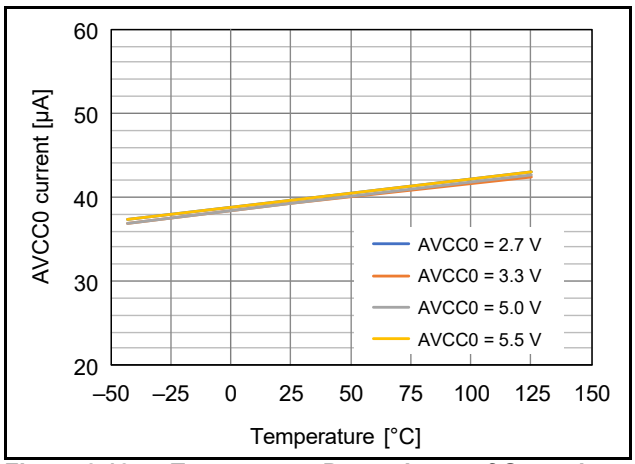


Figure 2.18 Temperature Dependence of Operating Current of Voltage Reference

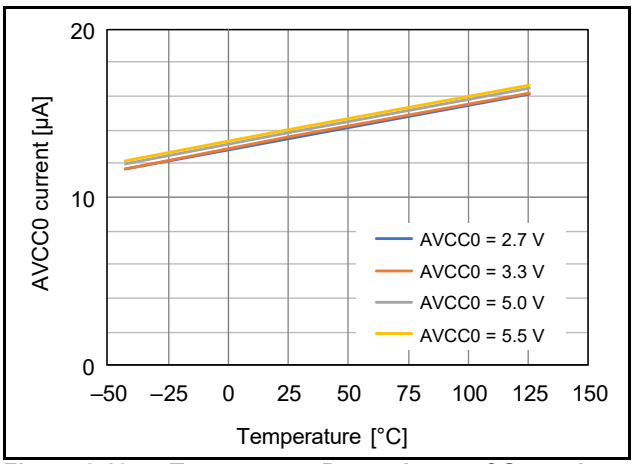


Figure 2.19 Temperature Dependence of Operating Current of Temperature Sensor

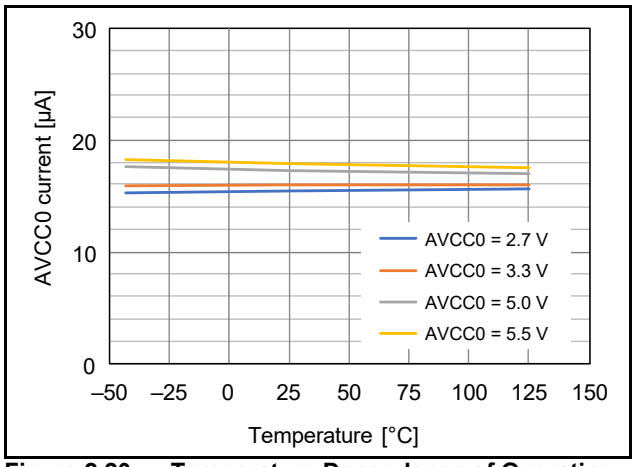


Figure 2.20 Temperature Dependence of Operating Current of Bias Voltage Generator

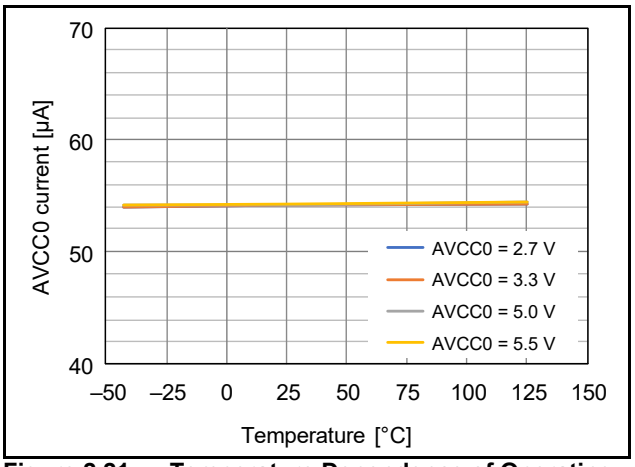


Figure 2.21 Temperature Dependence of Operating Current of Excitation Current Source

Table 2.15 DC Characteristics (12)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
12-bit A/D converter operating current	During A/D conversion (in high-speed conversion)	I_{AVCC0} (S12AD)	—	1.1	1.8	mA	
	During A/D conversion (in low-current mode)		—	0.6	1.1		
Reference power supply current	During A/D conversion (in high-speed conversion)	I_{REFH0}	—	71	122	µA	
	Current while waiting for A/D conversion (all units)		—	—	60	nA	
AVCC0 power down current		I_{STBY}	—	—	2.2	µA	

Note 1. Conditions for typical values are at AVCC0 = 5.0 V and T_a = 25°C.

Table 2.16 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible low-level output current (average value per pin)	P36 and P37		I_{OL}	4.0	mA
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current (maximum value per pin)	P36 and P37			4.0	
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current	Total of P14 to P17, P26, P27, P30, P31, P36, and P37		ΣI_{OL}	40	
	Total of PB0, PB1, PC4 to PC7, and PH0 to PH3			40	
	Total of all output pins			80	
Permissible high-level output current (average value per pin)	P36 and P37		I_{OH}	–4.0	
	Ports other than above	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
Permissible high-level output current (maximum value per pin)	P36 and P37			–4.0	
	Ports other than above	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
Permissible high-level output current	Total of P14 to P17, P26, P27, P30, P31, P36, and P37		ΣI_{OH}	–40	
	Total of PB0, PB1, PC4 to PC7, and PH0 to PH3			–40	
	Total of all output pins			–80	

Table 2.17 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible low-level output current (average value per pin)	P36 and P37		I_{OL}	4.0	mA
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current (maximum value per pin)	P36 and P37			4.0	
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current	Total of P14 to P17, P26, P27, P30, P31, P36, and P37		ΣI_{OL}	30	
	Total of PB0, PB1, PC4 to PC7, and PH0 to PH3			30	
	Total of all output pins			60	
Permissible high-level output current (average value per pin)	P36 and P37		I_{OH}	–4.0	
	Ports other than above	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
Permissible high-level output current (maximum value per pin)	P36 and P37			–4.0	
	Ports other than above	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
Permissible high-level output current	Total of P14 to P17, P26, P27, P30, P31, P36, and P37		ΣI_{OH}	–30	
	Total of PB0, PB1, PC4 to PC7, and PH0 to PH3			–30	
	Total of all output pins			–60	

Table 2.18 Output Voltage (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports	Normal drive output mode	V_{OL}	—	0.3	V	I_{OL} = 0.5 mA
		High-drive output mode		—	0.3		I_{OL} = 1.0 mA
High-level output voltage	All output ports	Normal drive output mode	V_{OH}	VCC – 0.3	—	V	I_{OH} = –0.5 mA
		High-drive output mode		VCC – 0.3	—		I_{OH} = –1.0 mA

Table 2.19 Output Voltage (2)

Conditions: 2.7 V ≤ VCC = AVCC0 < 4.0 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC pins)	Normal drive output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins	Normal drive output mode		—	0.4		I_{OL} = 3.0 mA
		High-drive output mode		—	0.6		I_{OL} = 6.0 mA
High-level output voltage	All output ports	Normal drive output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

Table 2.20 Output Voltage (3)

Conditions: 4.0 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC pins)	Normal drive output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins	Normal drive output mode		—	0.4		I_{OL} = 3.0 mA
		High-drive output mode		—	0.6		I_{OL} = 6.0 mA
High-level output voltage	All output ports	Normal drive output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

Table 2.21 Thermal Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	48-pin LFQFP (PLQP0048KB-B)	θ_{ja}	50.7	°C/W	JESD51-2 and JESD51-7 compliant
	40-pin HWQFN (PWQN0040KC-A)		18.8*1		
	48-pin LFQFP (PLQP0048KB-B)	Ψ_{jt}	1.07	°C/W	JESD51-2 and JESD51-7 compliant
	40-pin HWQFN (PWQN0040KC-A)		0.07*1		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the exposed die pad for this purpose is connected to VSS.

2.3.1 Typical I/O Pin Output Characteristics (1)

Figure 2.22 to Figure 2.26 show the characteristics when normal drive output is selected by the drive capacity control register.

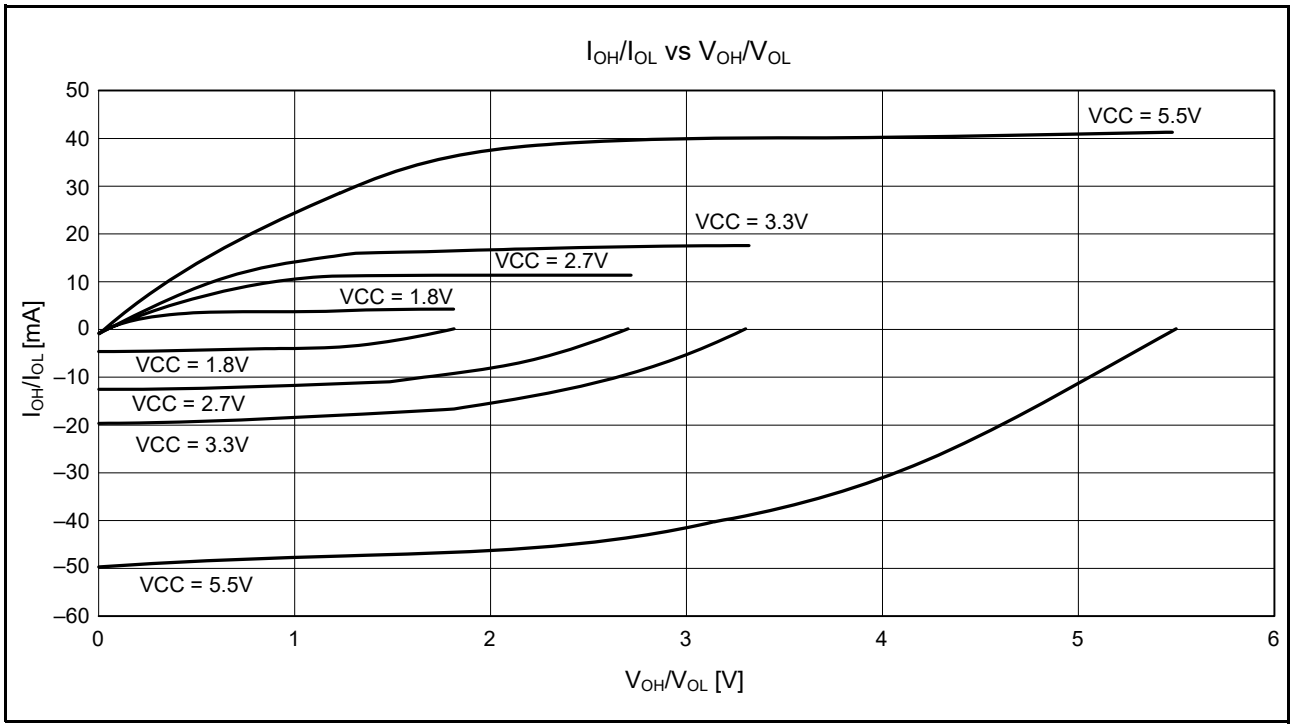


Figure 2.22 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Drive Output is Selected (Reference Data)

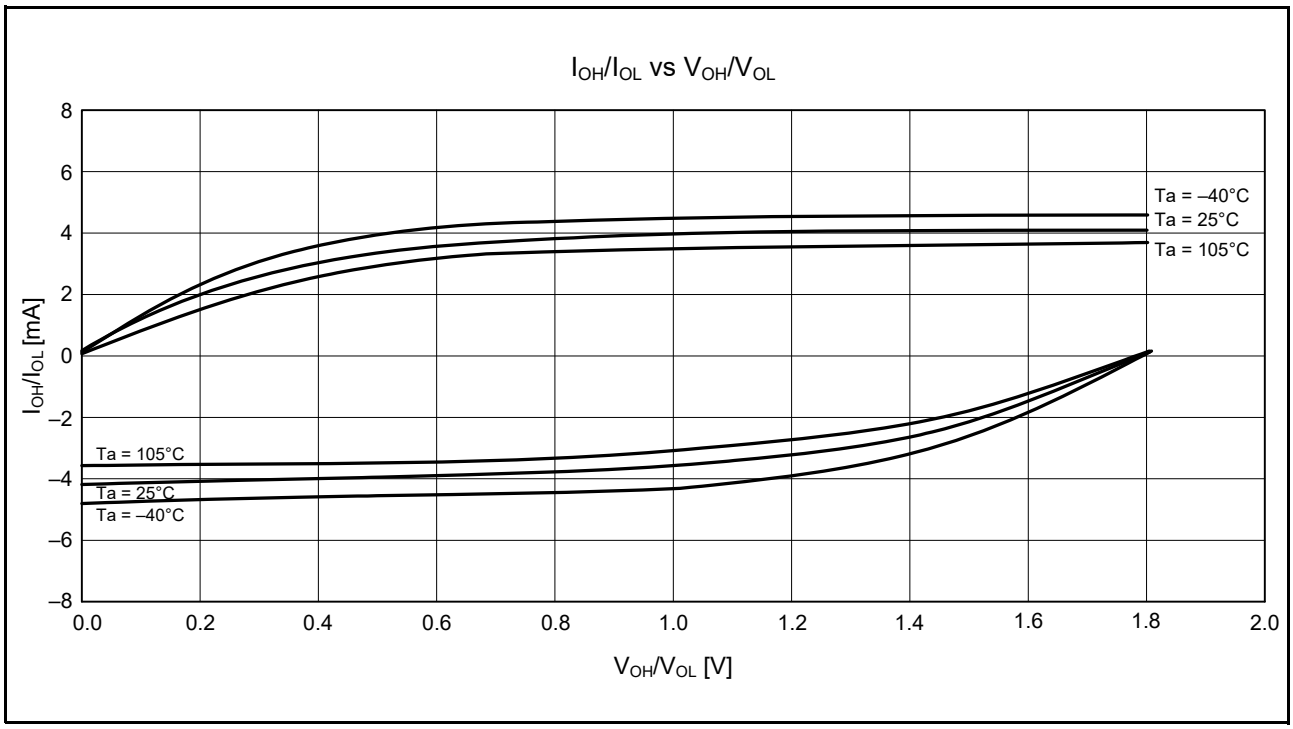


Figure 2.23 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Drive Output is Selected (Reference Data)

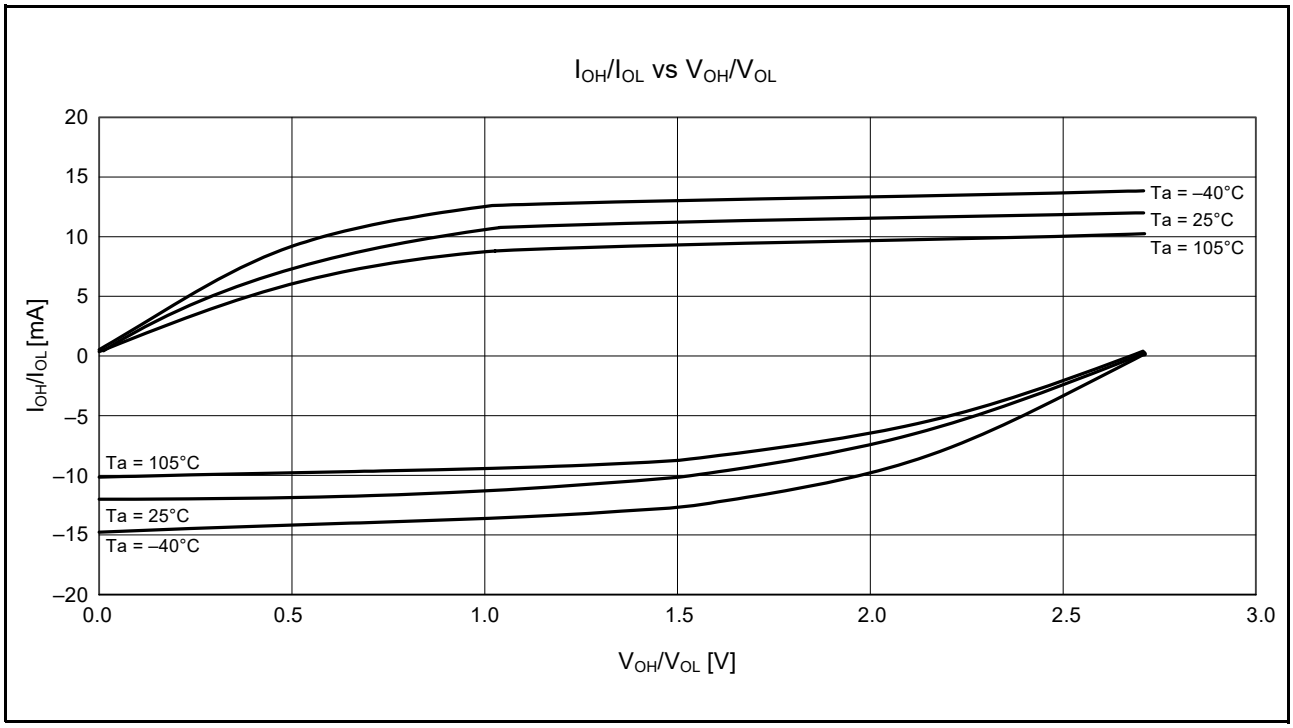


Figure 2.24 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Drive Output is Selected (Reference Data)

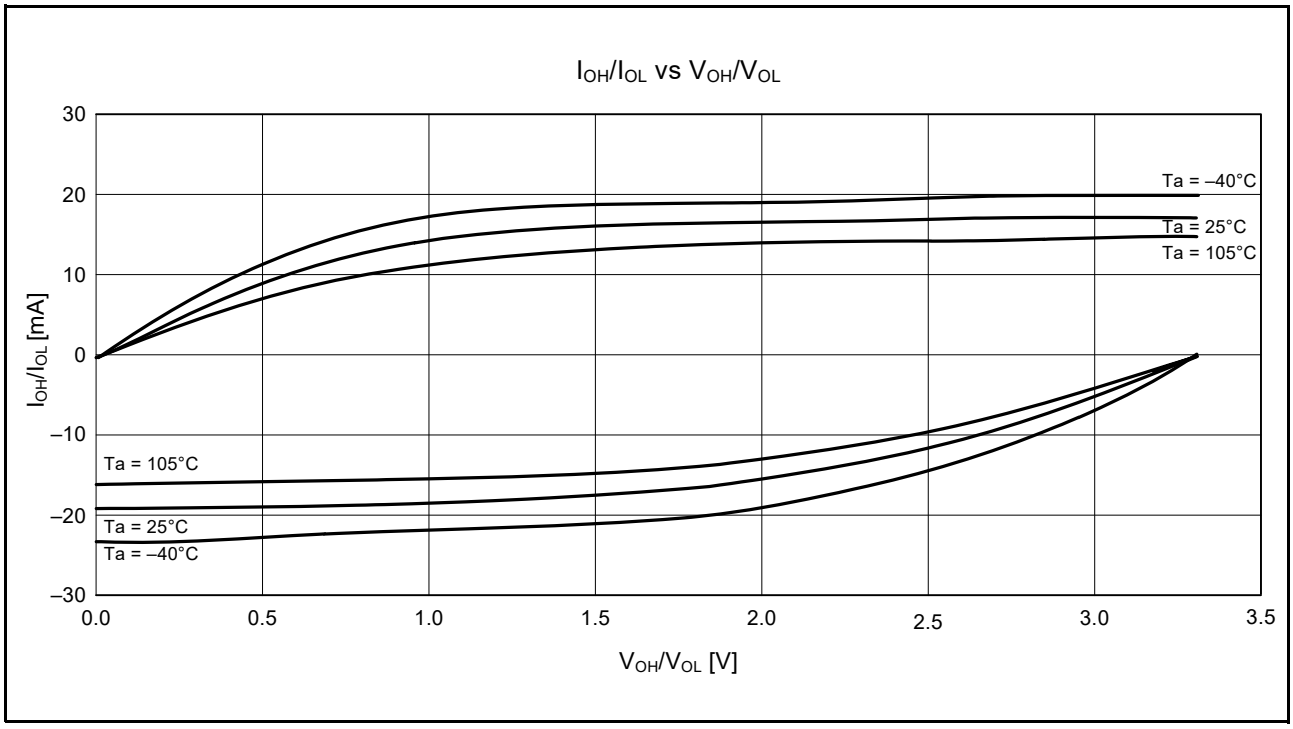


Figure 2.25 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Drive Output is Selected (Reference Data)

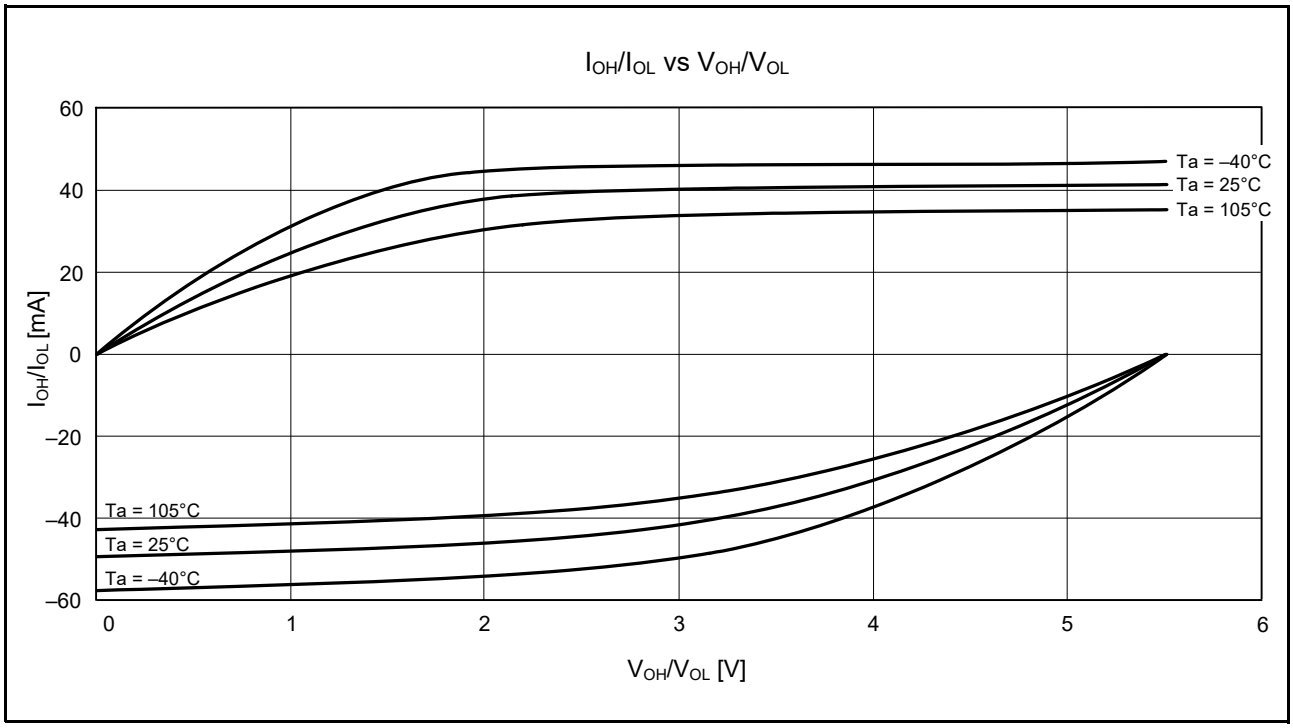


Figure 2.26 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When Normal Drive Output is Selected (Reference Data)

2.3.2 Typical I/O Pin Output Characteristics (2)

Figure 2.27 to Figure 2.31 show the characteristics when high-drive output is selected by the drive capacity control register.

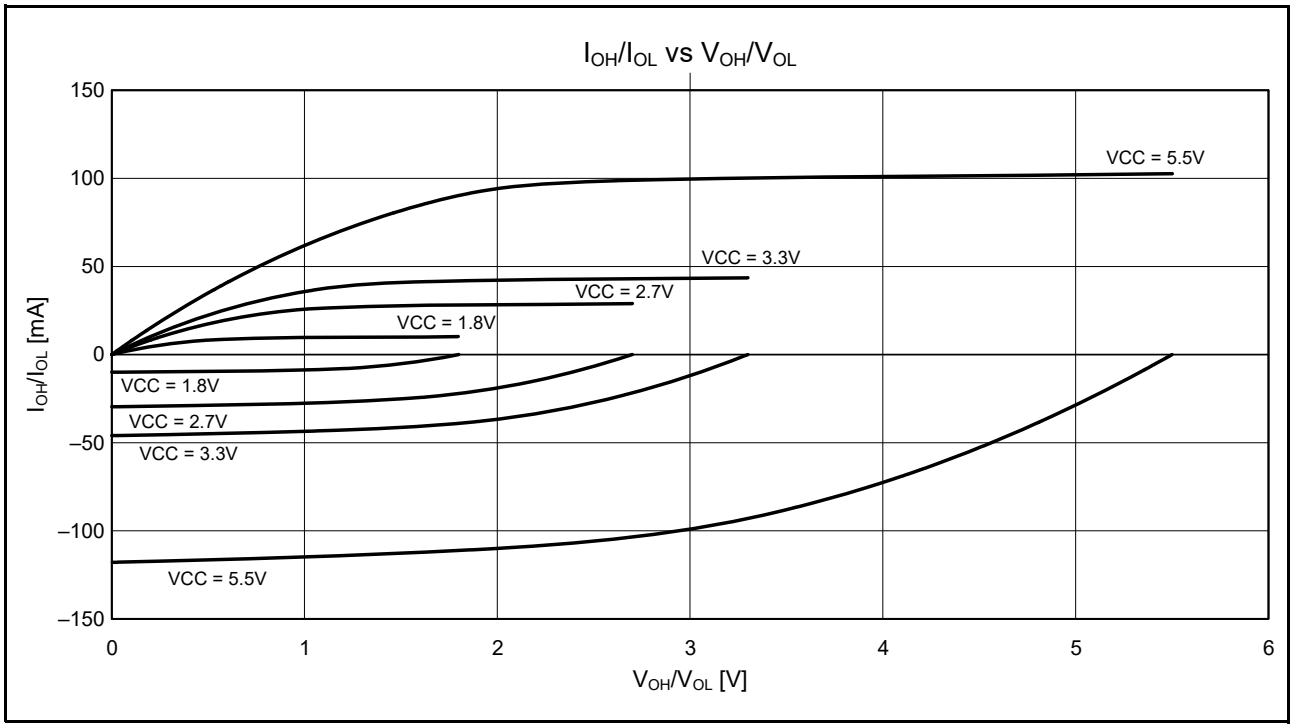


Figure 2.27 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When High-Drive Output is Selected (Reference Data)

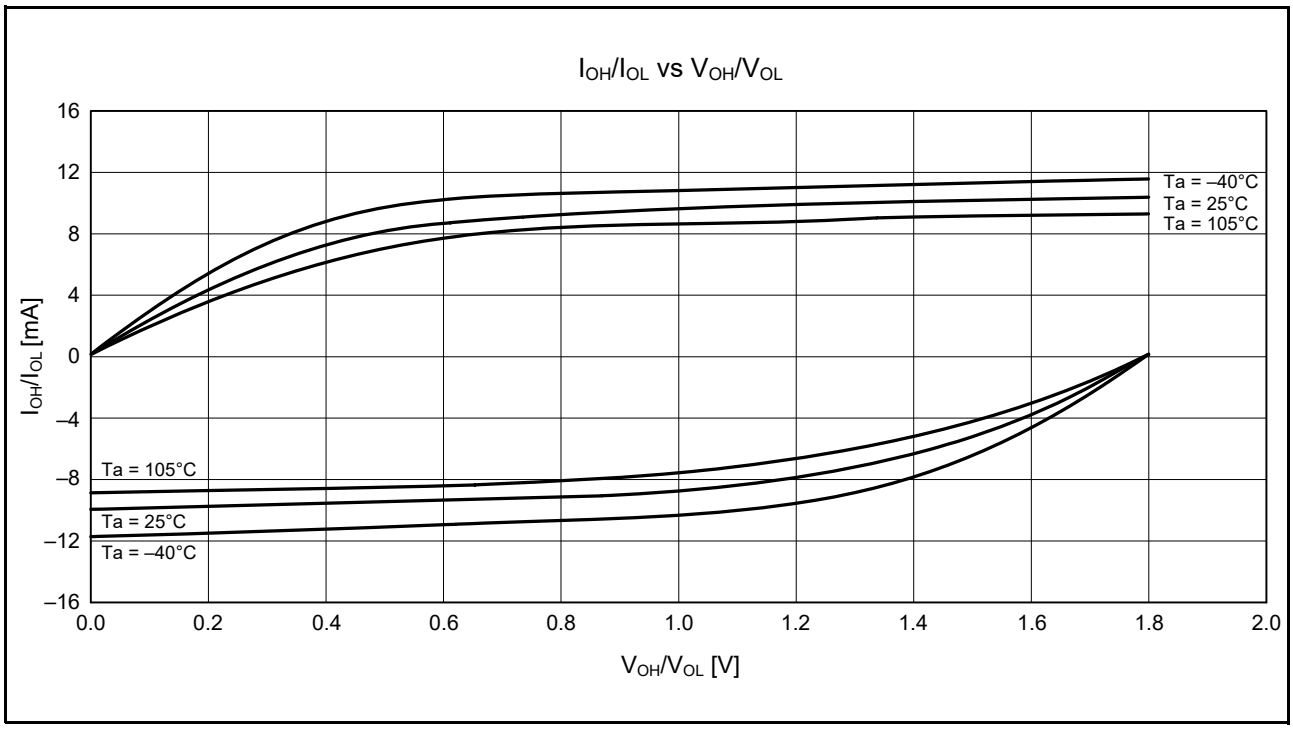


Figure 2.28 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When High-Drive Output is Selected (Reference Data)

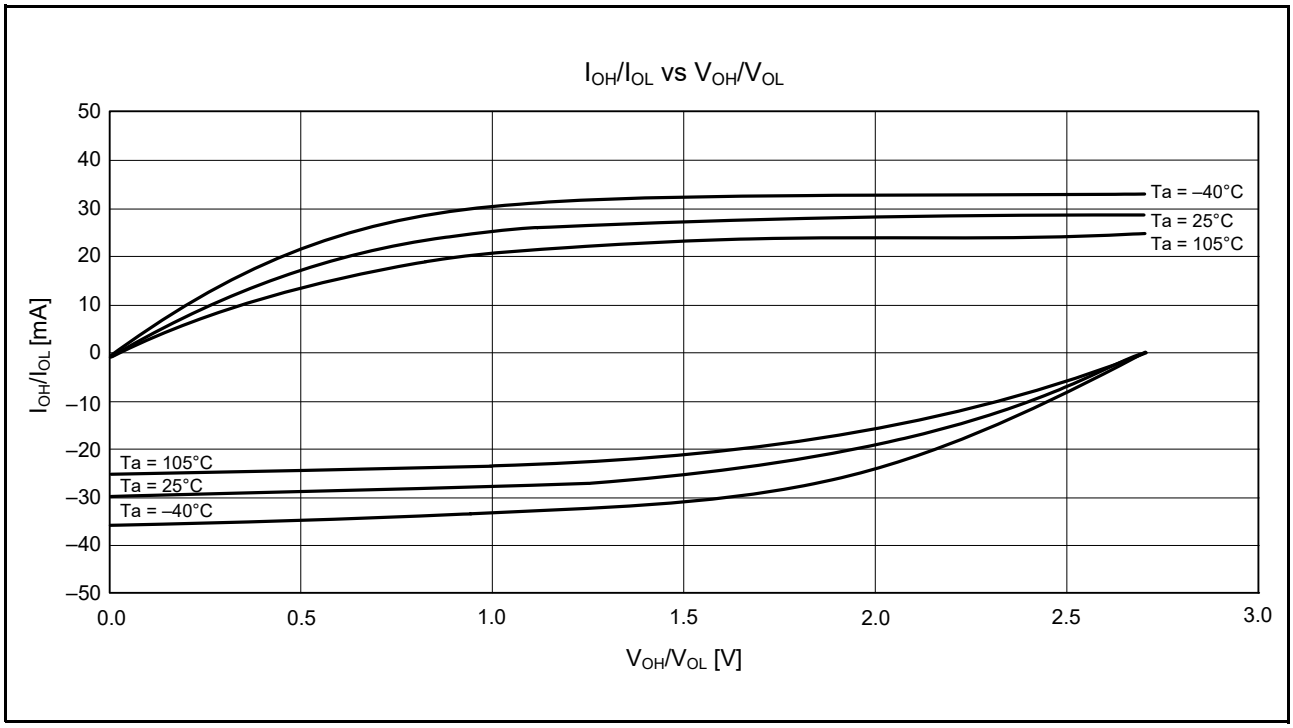


Figure 2.29 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When High-Drive Output is Selected (Reference Data)**

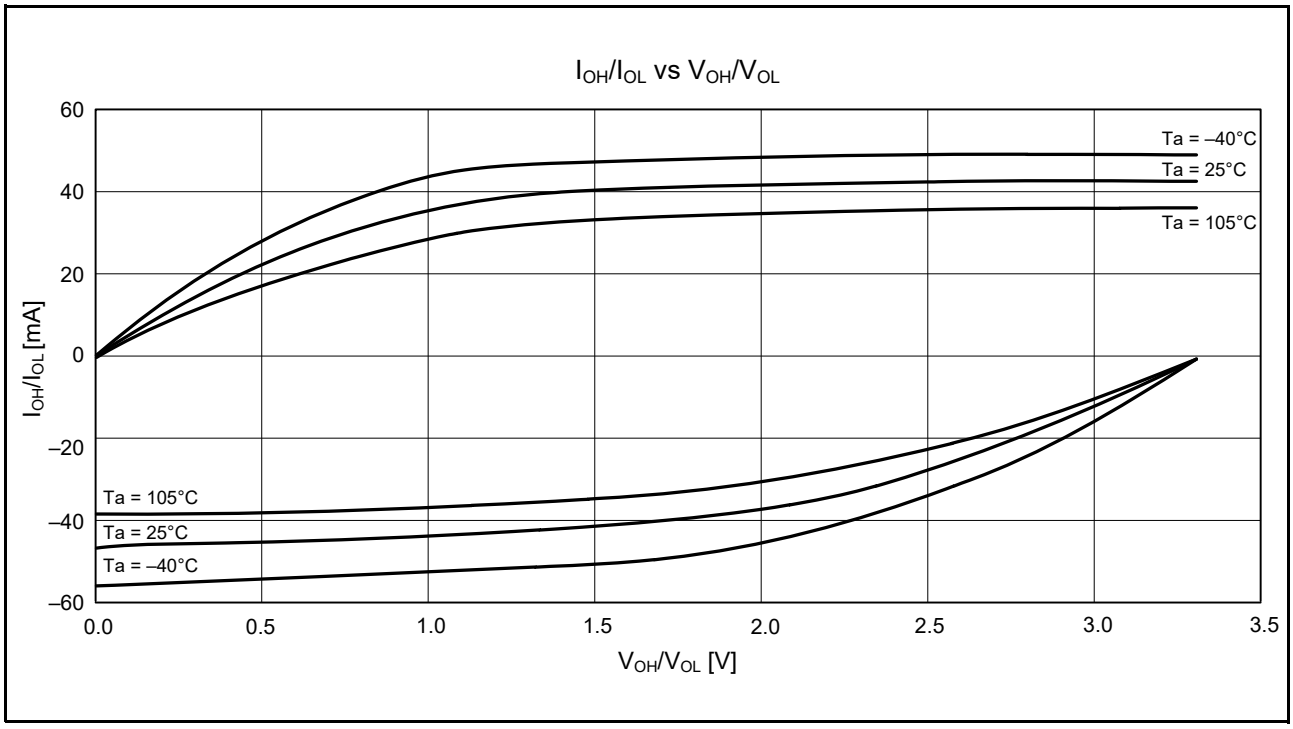


Figure 2.30 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When High-Drive Output is Selected (Reference Data)**

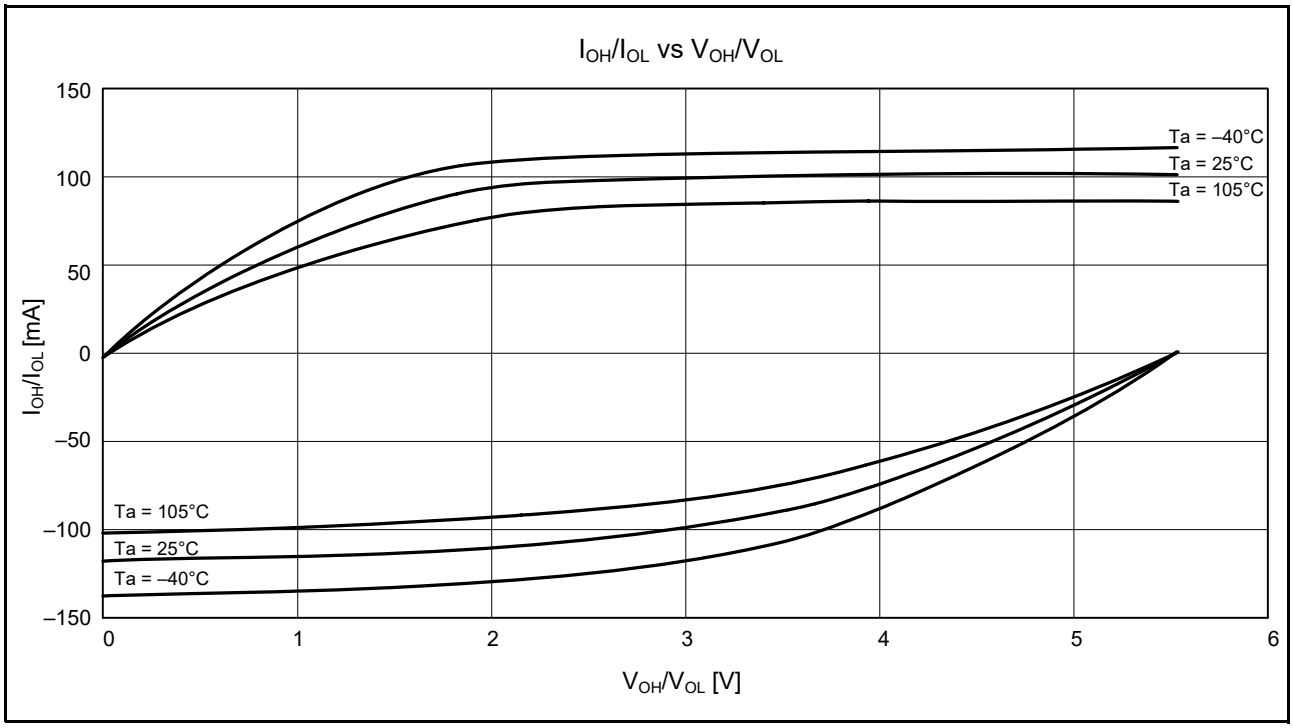


Figure 2.31 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)

2.3.3 Typical I/O Pin Output Characteristics (3)

Figure 2.32 to Figure 2.35 show the characteristics of the RIIC output pin.

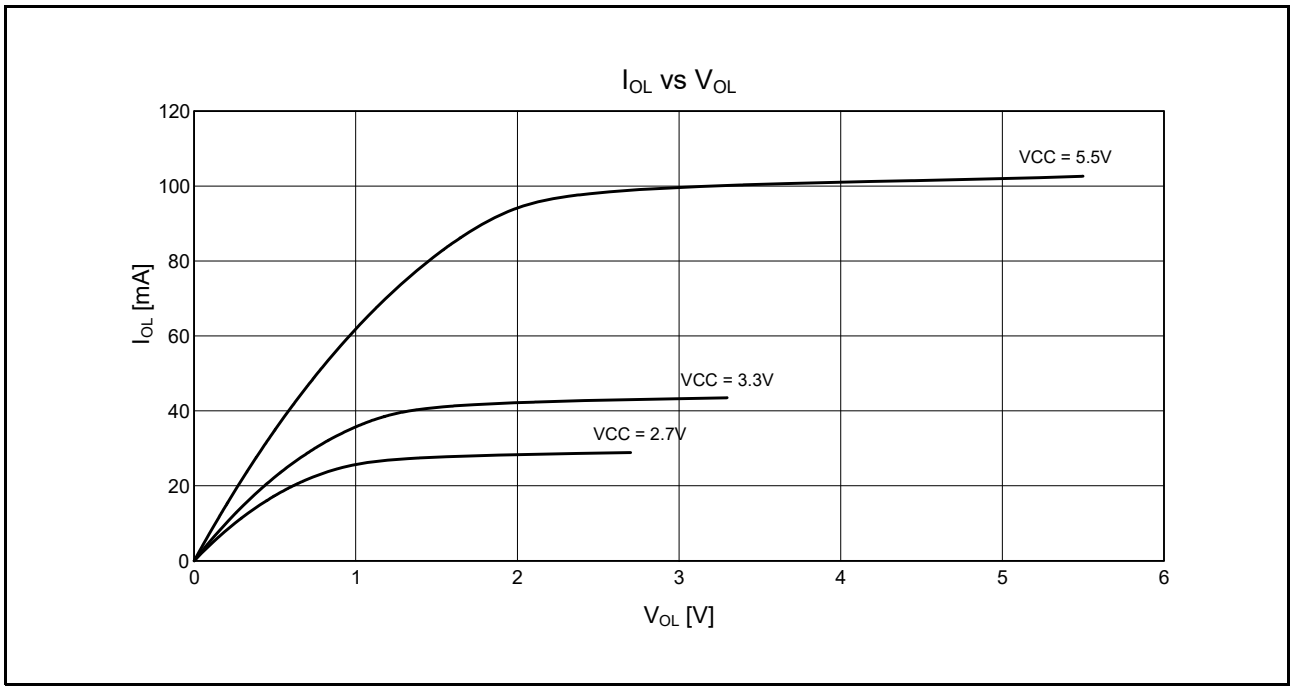


Figure 2.32 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

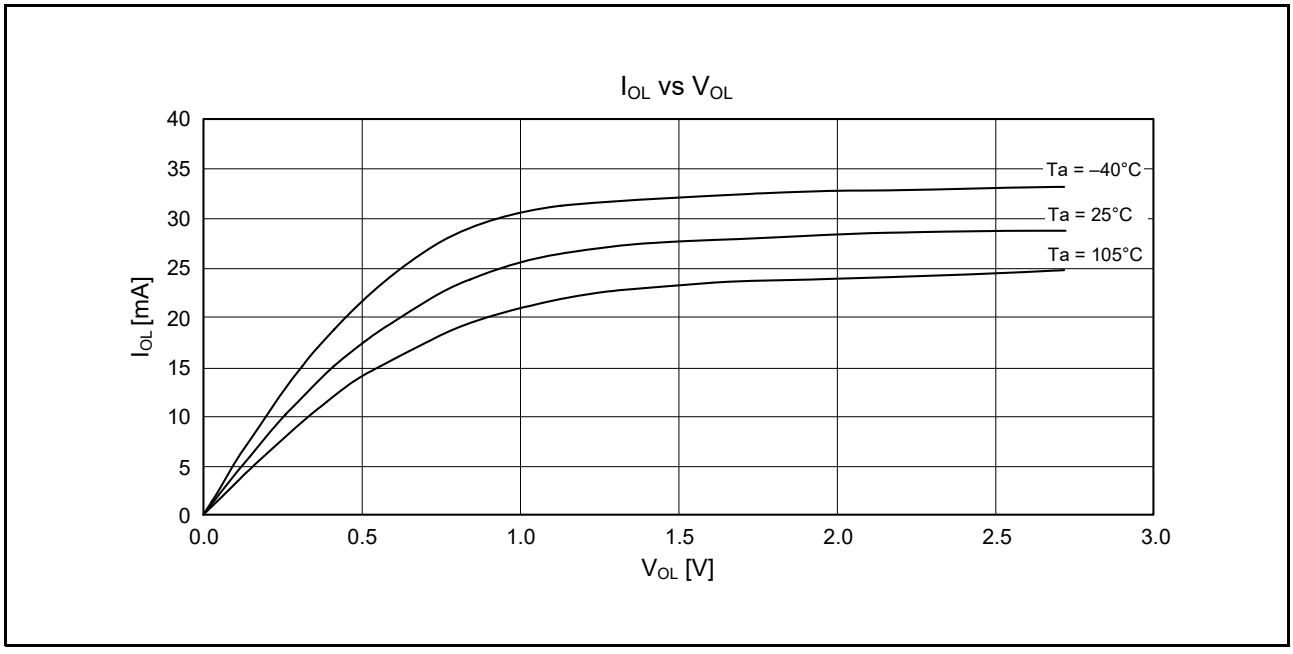


Figure 2.33 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

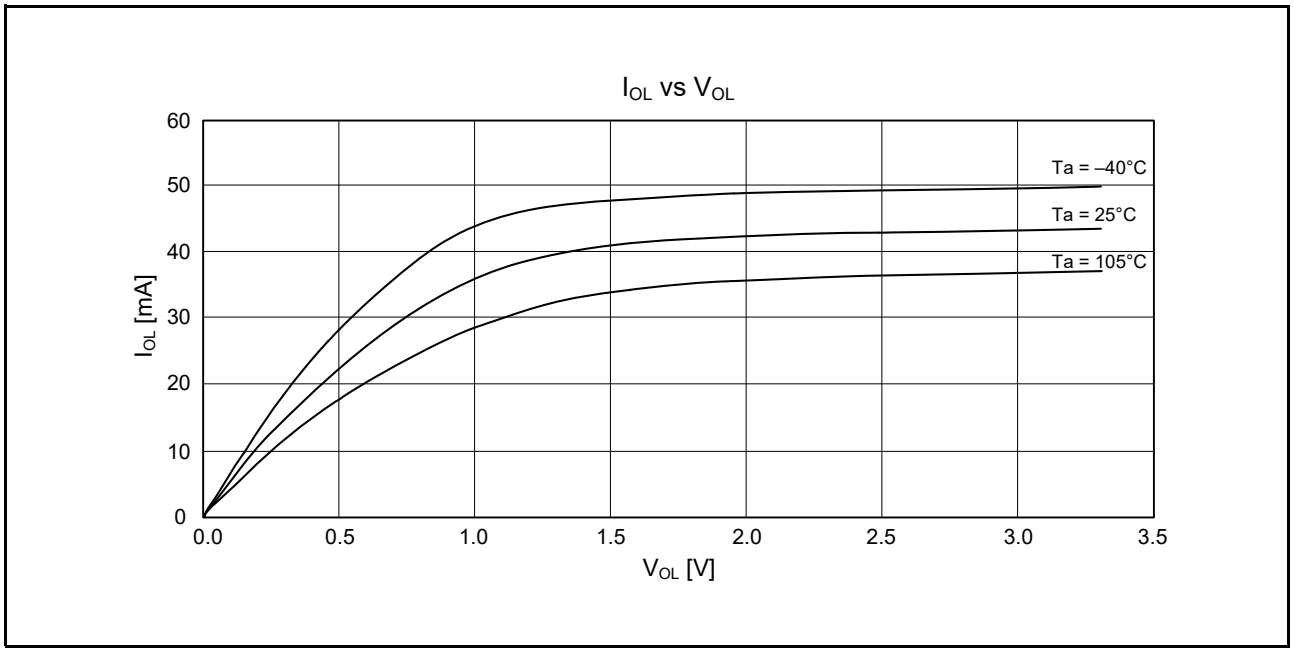


Figure 2.34 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

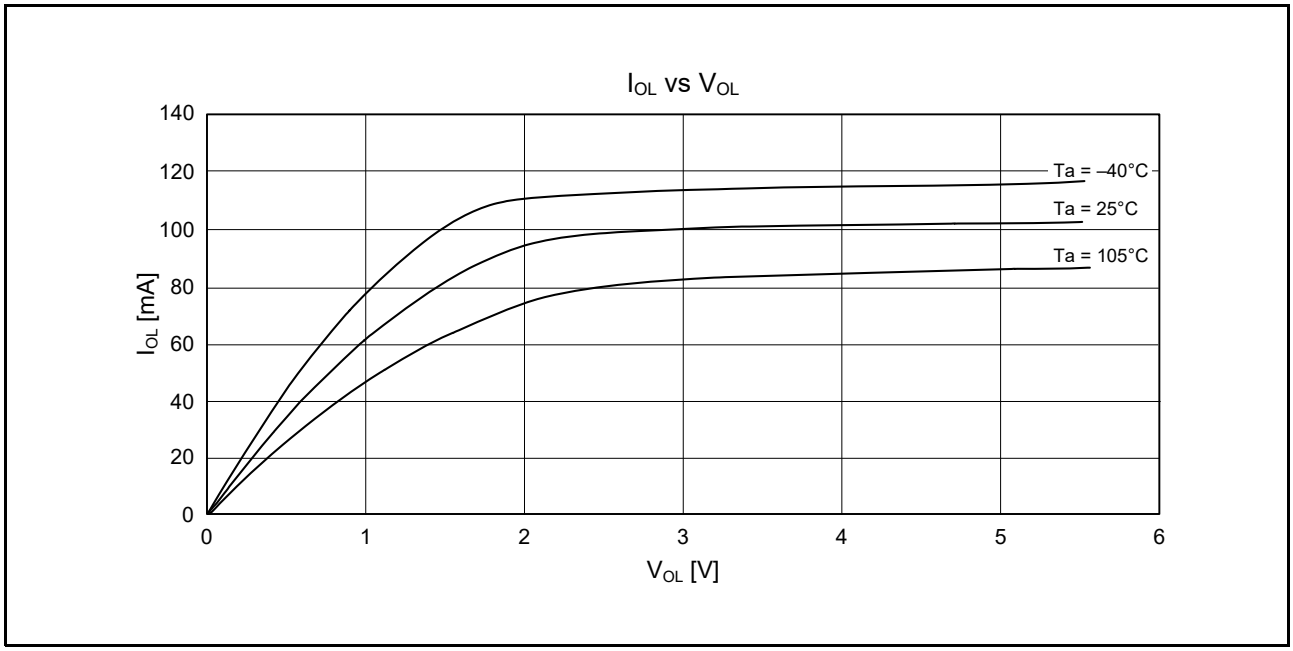


Figure 2.35 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

2.4 AC Characteristics

2.4.1 Clock Timing

Table 2.22 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKA)		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 2.24, Clock Timing.

Table 2.23 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKA)		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKD)		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 2.24, Clock Timing.

Table 2.24 Clock Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 2.36
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 2.37
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.00	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 2.38
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15.00	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 2.39
HOCO clock oscillation frequency		f_{HOCO}	31.52	32.00	32.48	MHz	T_a = –40 to +85°C
			31.68	32.00	32.32		T_a = –20 to +85°C
			31.36	32.00	32.64		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	41.3	μs	Figure 2.41
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	32	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	74.4	μs	Figure 2.42
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).
Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.
Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

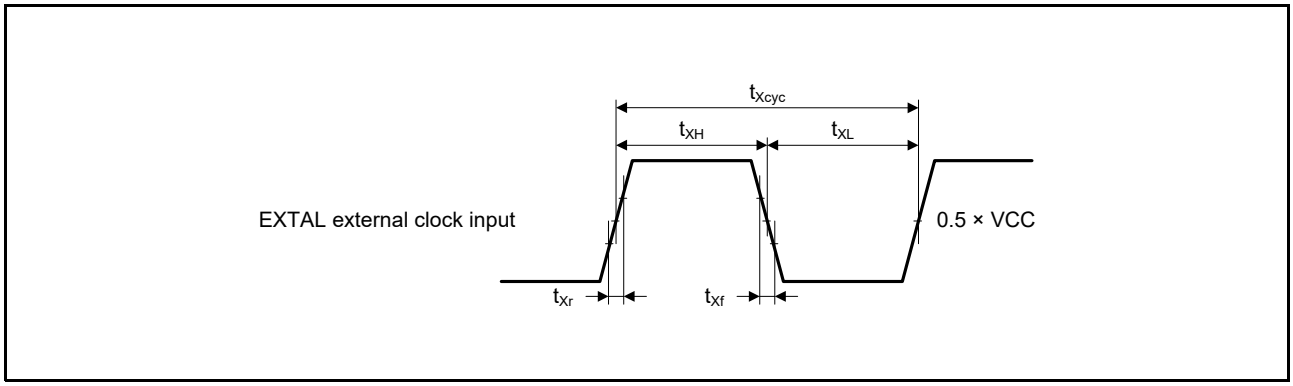


Figure 2.36 EXTAL External Clock Input Timing

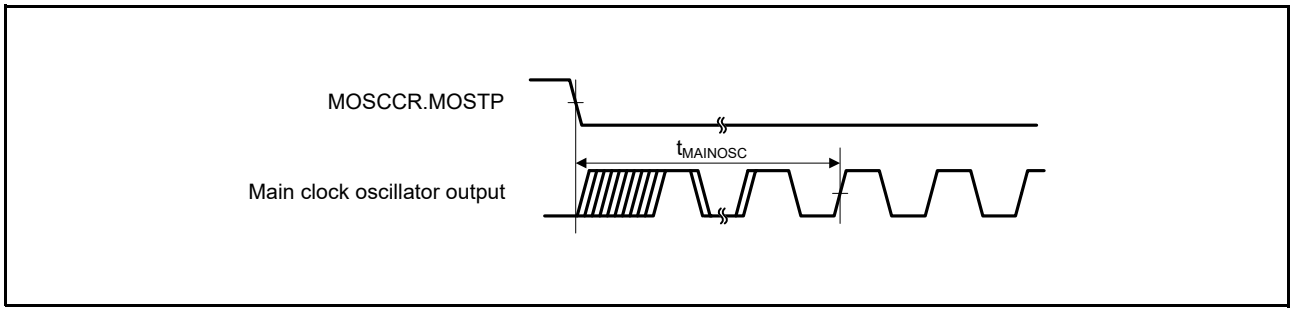


Figure 2.37 Main Clock Oscillation Start Timing

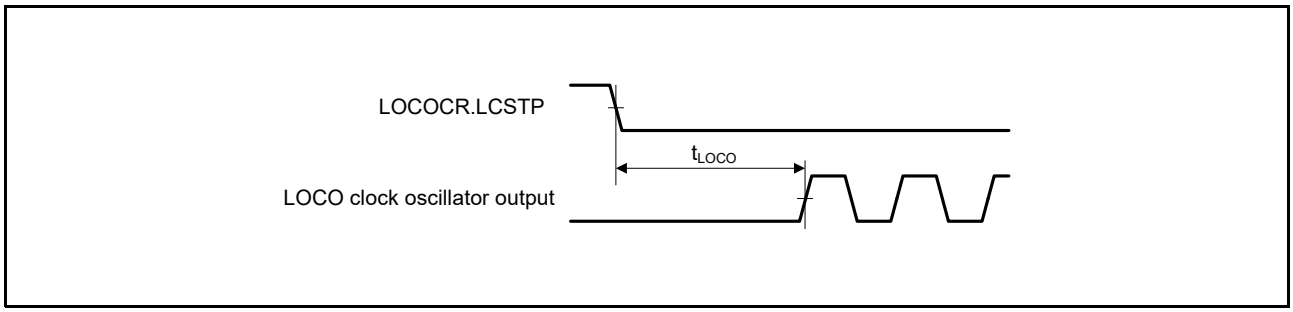


Figure 2.38 LOCO Clock Oscillation Start Timing

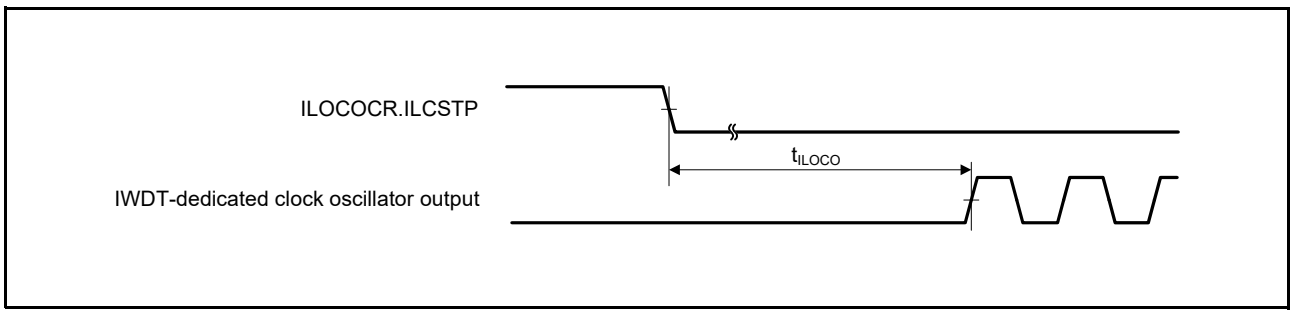


Figure 2.39 IWDT-Dedicated Clock Oscillation Start Timing

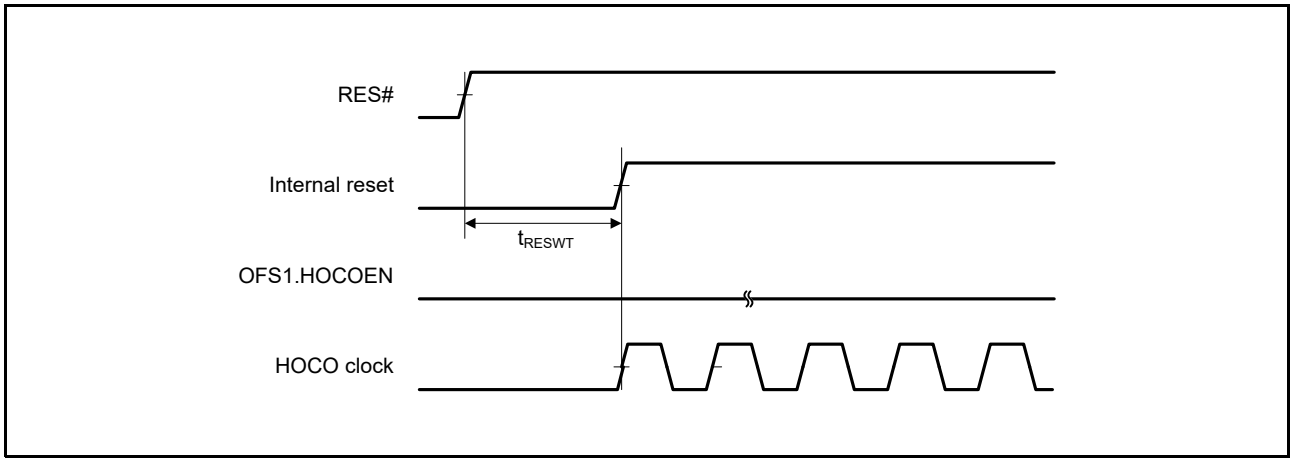


Figure 2.40 HOCO Clock Oscillation Start Timing
(After Release from a Reset by Setting OFS1.HOCOEN Bit to 0)

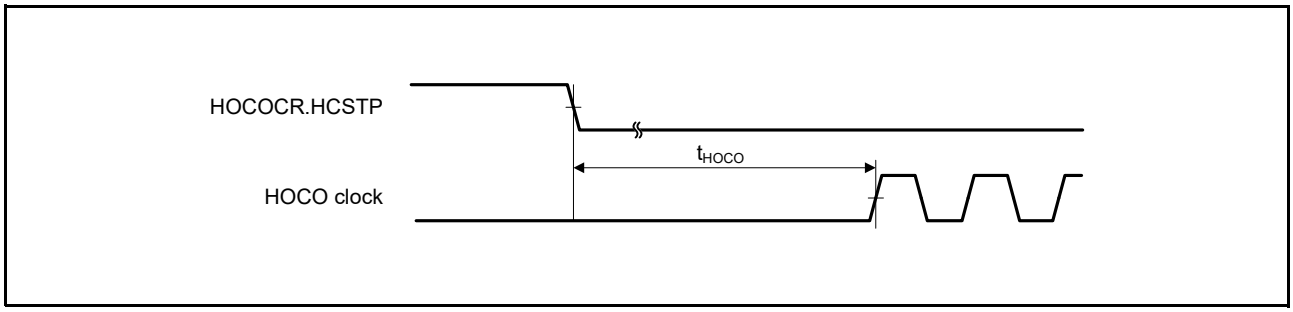


Figure 2.41 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

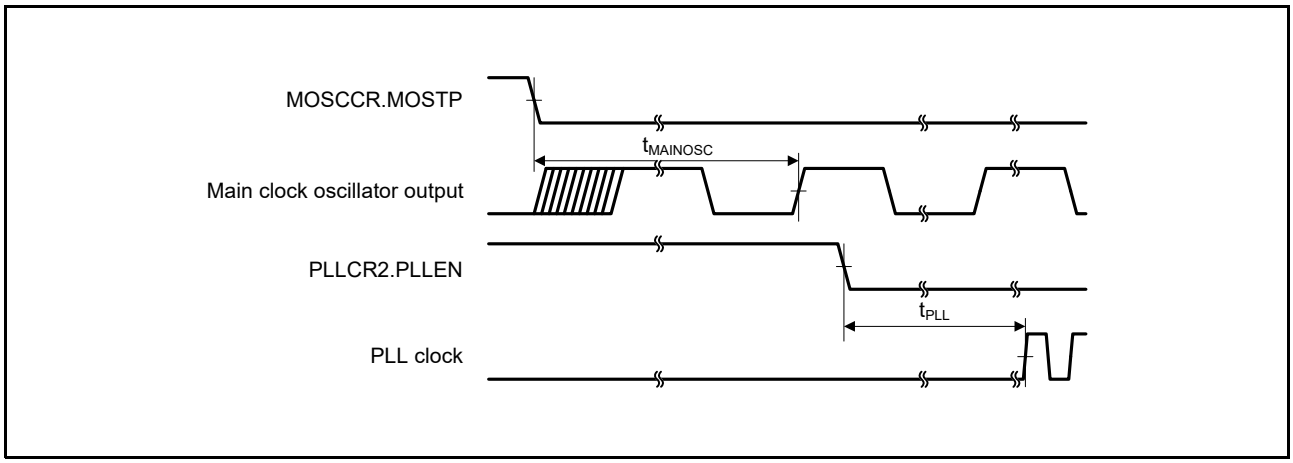


Figure 2.42 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Been Stabled)

2.4.2 Reset Timing

Table 2.25 Reset Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 2.43
	Other than above	t_{RESW}	30	—	—	µs	Figure 2.44
Wait time after release from the RES# pin reset (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 2.43
	During fast startup time*2	t_{RESWT}	—	650	—	µs	
Wait time after release from the RES# pin reset (from a warm start)		t_{RESWT}	—	310	—	µs	Figure 2.44
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 2.45
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after release from the independent watchdog timer reset*3		t_{RESWT2}	—	350	—	µs	
Wait time after release from the software reset		t_{RESWT2}	—	220	—	µs	

Note 1. When the OFS1.LVDAS and OFS1.FASTSTUP bits are 1
Note 2. When the OFS1.LVDAS and/or OFS1.FASTSTUP bits are 0
Note 3. When the IWDTCR.CKS[3:0] bits are 0000b

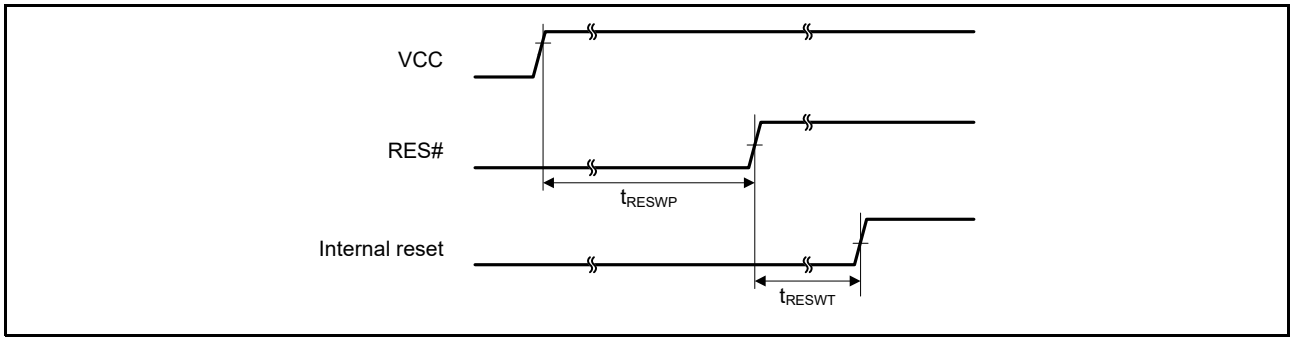


Figure 2.43 Reset Input Timing at Power-On

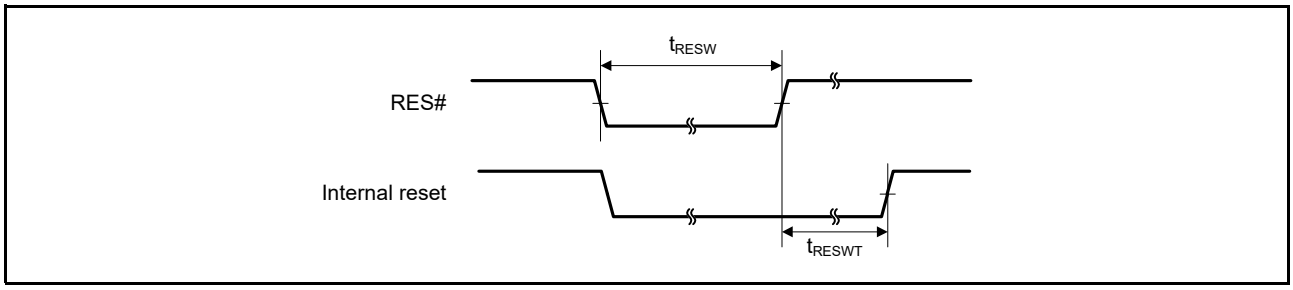


Figure 2.44 Reset Input Timing (1)

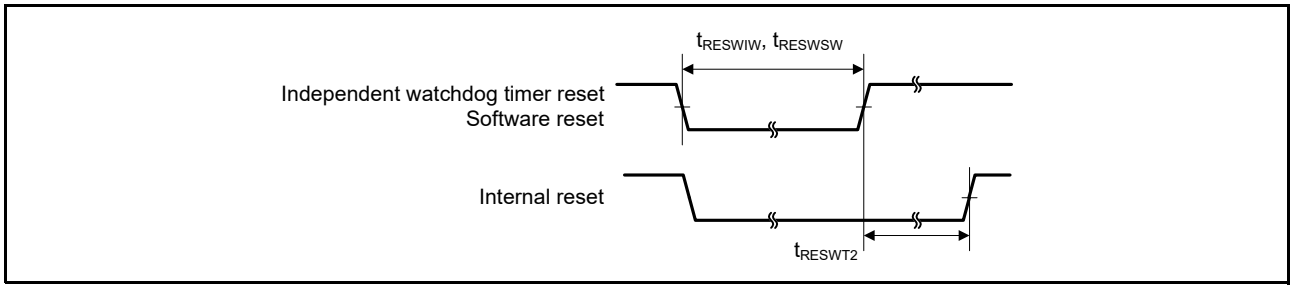


Figure 2.45 Reset Input Timing (2)

2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.26 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 2.46
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	35	50	µs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 20 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h
Note 3. When the frequency of the external clock is 20 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h

Table 2.27 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 2.46
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		HOCO clock oscillator operating*6		t_{SBYHO}	—	40	50	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h
Note 3. This is the case when PLL is selected as the system clock and its frequency division is set to be 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h
Note 4. When the frequency of the external clock is 12 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h
Note 5. This is the case when PLL is selected as the system clock and its frequency division is set to be 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h
Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.

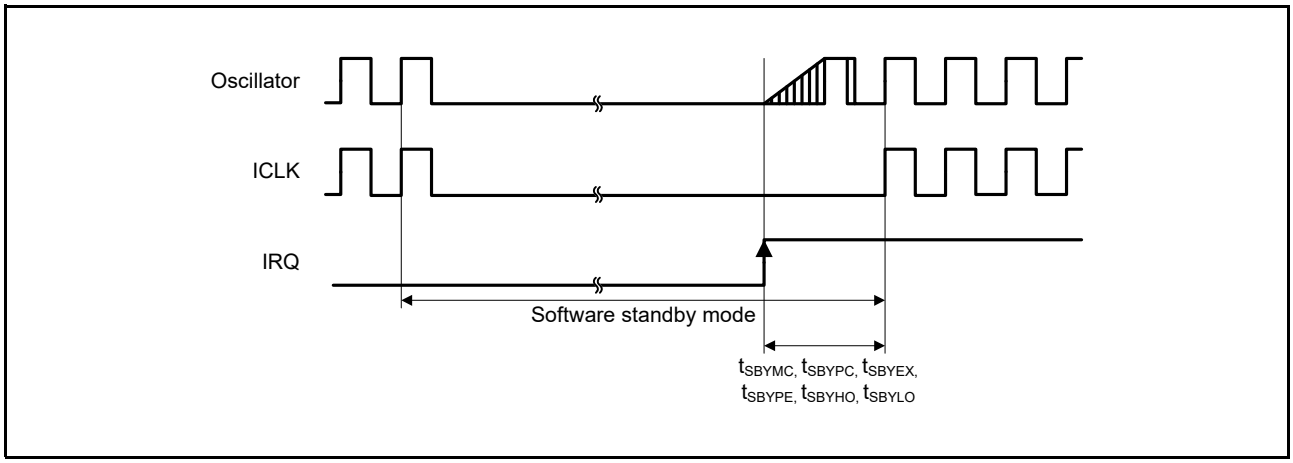


Figure 2.46 Software Standby Mode Recovery Timing

Table 2.28 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2.0	3.5	µs	Figure 2.47
	Middle-speed mode*3	t_{DSLP}	—	3.0	4.0	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz
Note 3. When the frequency of the system clock is 12 MHz

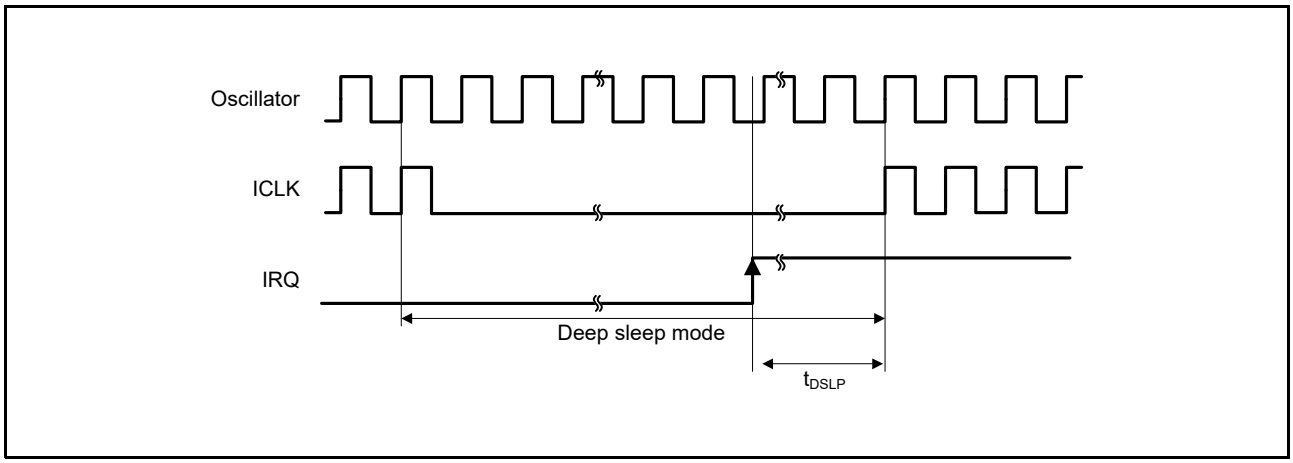


Figure 2.47 Deep Sleep Mode Recovery Timing

Table 2.29 Operating Mode Transition Time

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10.0	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

2.4.4 Control Signal Timing

Table 2.30 Control Signal Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	2 × t_{Pcyc} ≤ 200 ns
		2 × t_{Pcyc}*1	—	—			2 × t_{Pcyc} > 200 ns
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	3 × t_{NMICK} ≤ 200 ns
		3.5 × t_{NMICK}*2	—	—			3 × t_{NMICK} > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	2 × t_{Pcyc} ≤ 200 ns
		2 × t_{Pcyc}*1	—	—			2 × t_{Pcyc} > 200 ns
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	3 × t_{IRQCK} ≤ 200 ns
		3.5 × t_{IRQCK}*3	—	—			3 × t_{IRQCK} > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

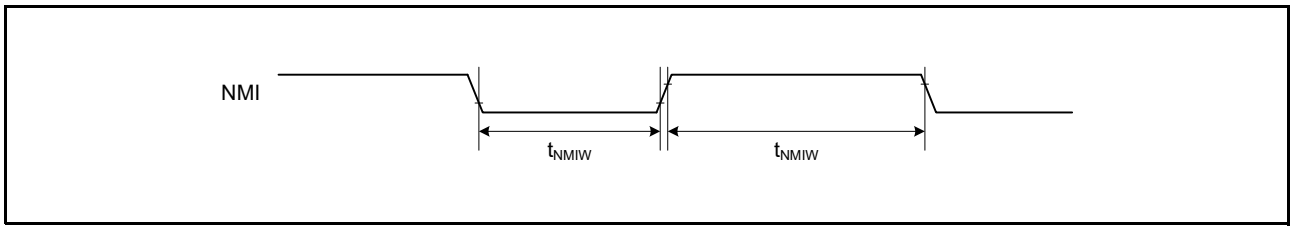


Figure 2.48 NMI Interrupt Input Timing

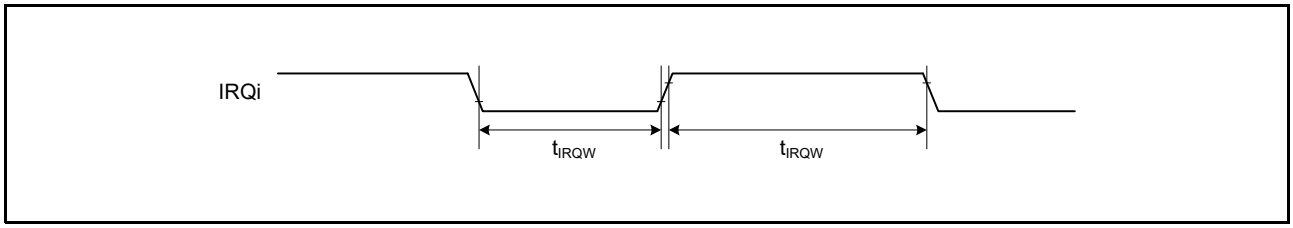


Figure 2.49 IRQ Interrupt Input Timing

2.4.5 Timing of On-Chip Peripheral Modules

2.4.5.1 I/O ports

Table 2.31 Timing of I/O ports

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	—	t_{Pcyc}	Figure 2.50

Note 1. t_{Pcyc}: PCLK cycle

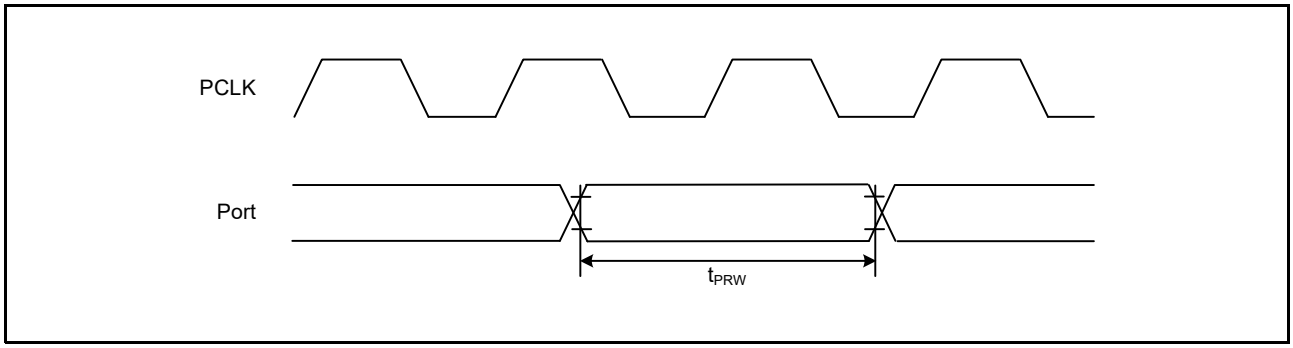


Figure 2.50 I/O Port Input Timing

2.4.5.2 MTU

Table 2.32 Timing of MTU

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	—	t_{Pcyc}	Figure 2.51
		Both-edge setting		2.5	—	—		
	Input capture input rise/fall time		t_{TICr}, t_{TICf}	—	—	0.1	µs/V	
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	—	t_{Pcyc}	Figure 2.52
		Both-edge setting		2.5	—	—		
		Phase counting mode		2.5	—	—		
	Timer clock rise/fall time		t_{TCKr}, t_{TCKf}	—	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle

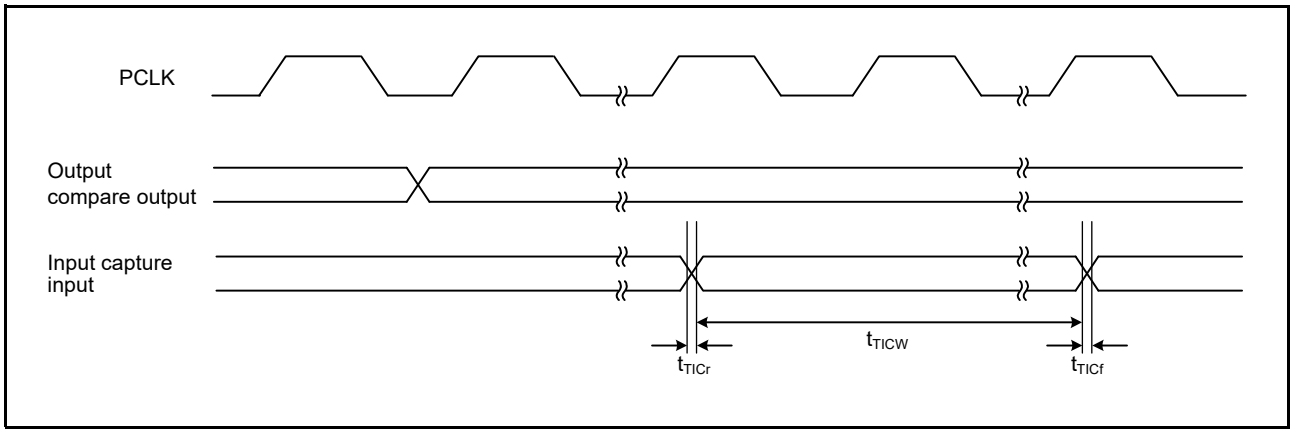


Figure 2.51 MTU Input/Output Timing

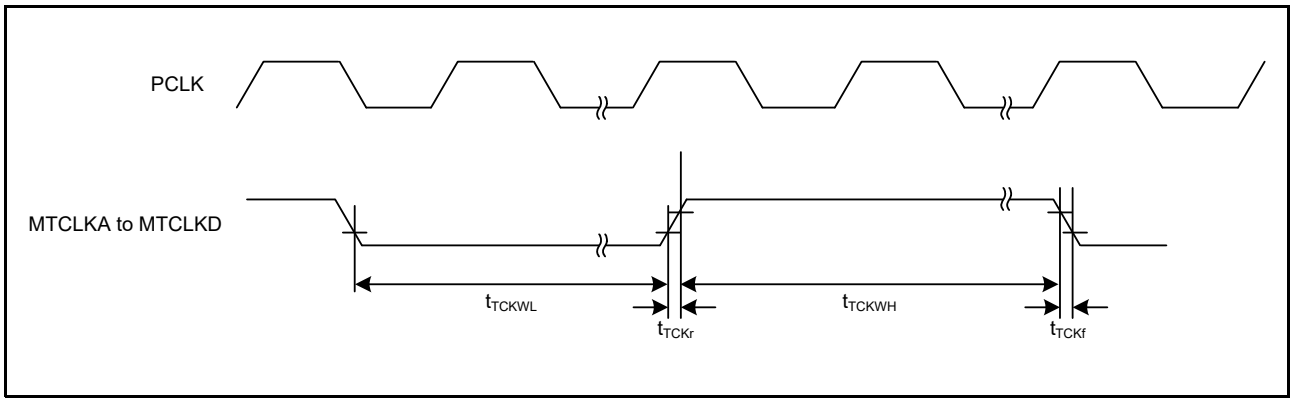


Figure 2.52 MTU Clock Input Timing

2.4.5.3 POE

Table 2.33 Timing of POE

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 2.53
	POE# input rise/fall time		t_{POEr}, t_{POEf}	—	—	0.1	μs/V	
	Output disable time	Transition of the POE# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	μs	Figure 2.54 When detecting falling edges (ICSRm.POEnM[1:0] = 00 (m = 1, 2; n = 0 to 3, 8))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	μs	Figure 2.55
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	μs	Figure 2.56 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	μs	Figure 2.57

Note 1. t_{Pcyc}: PCLK cycle

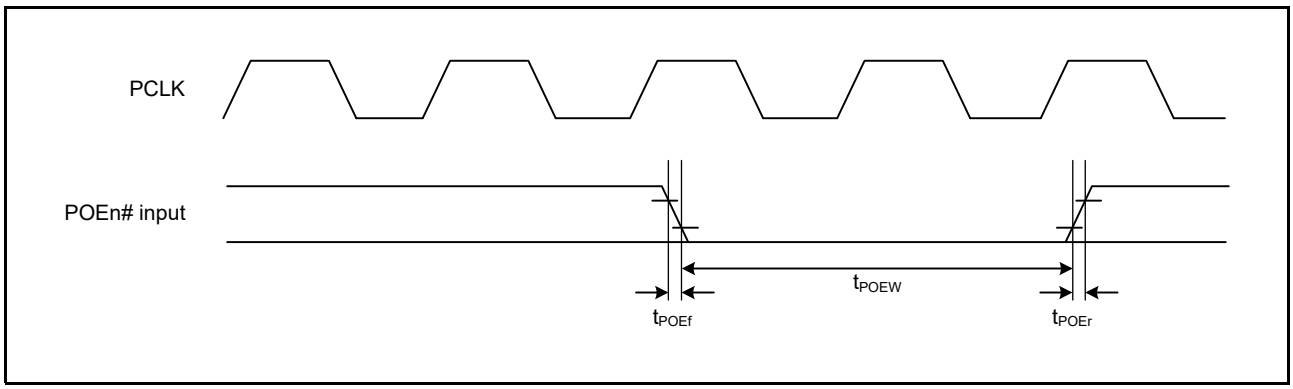


Figure 2.53 POE Input Timing (n = 0 to 3, 8)

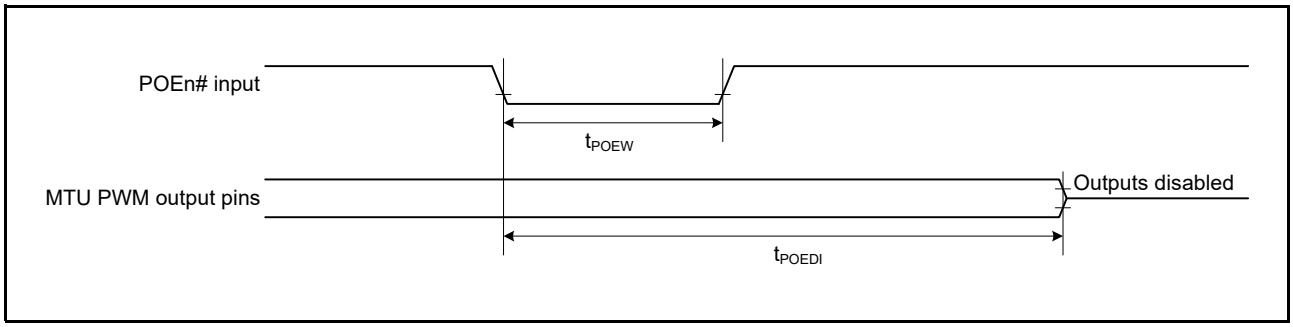
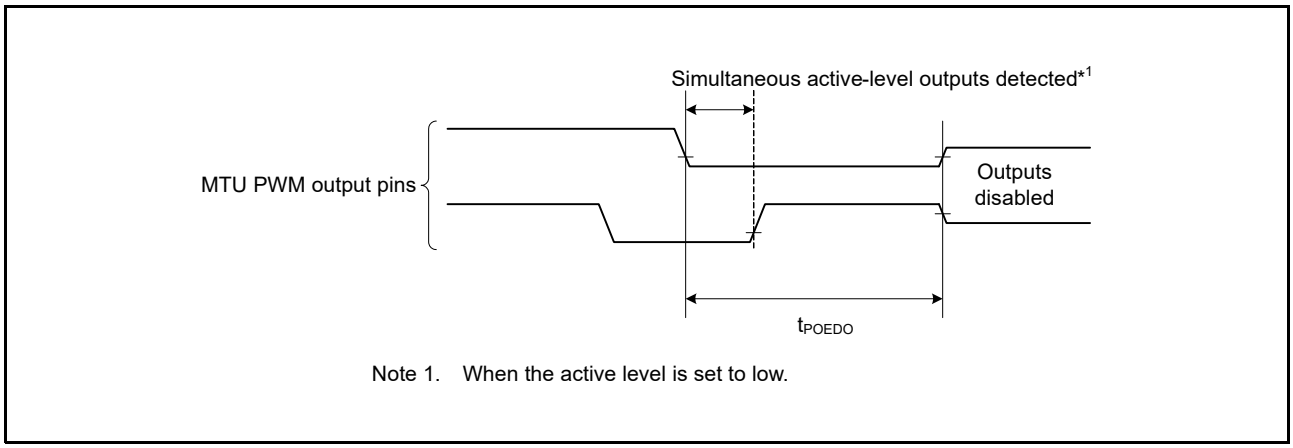


Figure 2.54 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.55 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

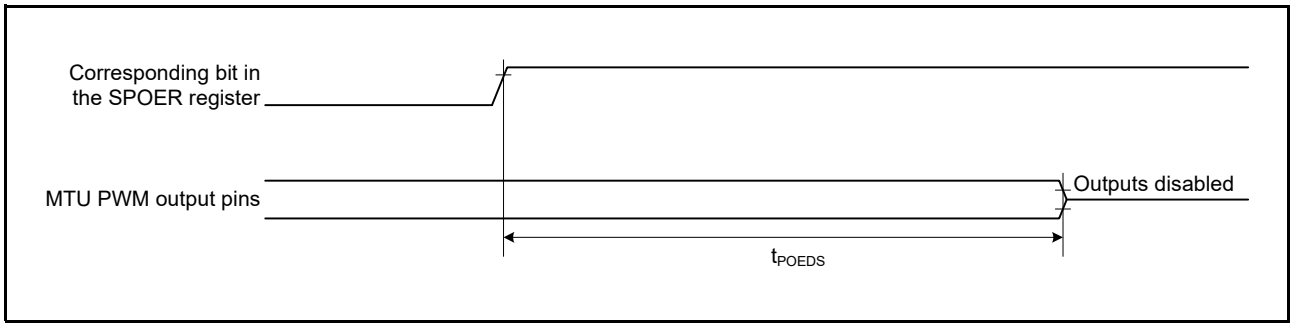


Figure 2.56 Output Disable Time for POE in Response to the Register Setting

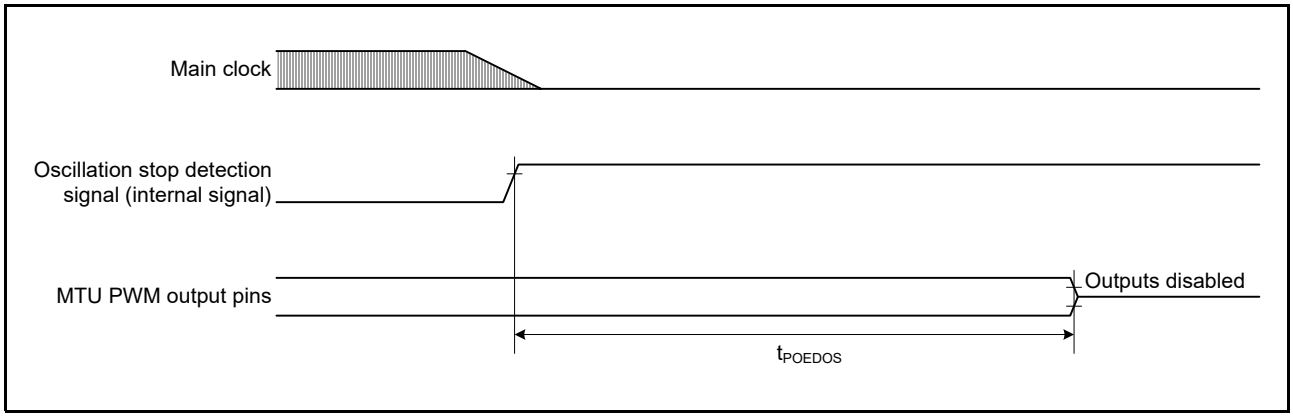


Figure 2.57 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.4.5.4 TMR

Table 2.34 Timing of TMR

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	—	t_{Pcyc}	Figure 2.58
		Both-edge setting		2.5	—	—		
	Timer clock rise/fall time		t_{TMCr}, t_{TMCf}	—	—	0.1	μs/V	

Note 1. t_{Pcyc}: PCLK cycle

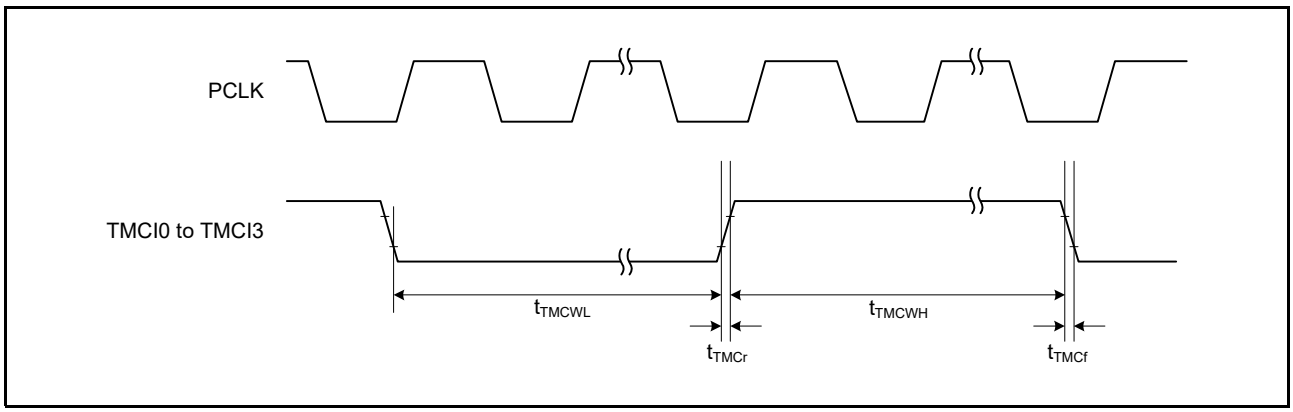


Figure 2.58 TMR Clock Input Timing

2.4.5.5 SCI

Table 2.35 Timing of SCI

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle time		Asynchronous	t_{Scyc}	4	—	—	t_{Pcyc}	Figure 2.59
			Clock synchronous		6	—	—		
	Input clock pulse width			t_{SCKW}	0.4	—	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	—	20	ns	
	Input clock fall time			t_{SCKf}	—	—	20	ns	
	Output clock cycle time		Asynchronous	t_{Scyc}	16	—	—	t_{Pcyc}	
			Clock synchronous		4	—	—		
	Output clock pulse width			t_{SCKW}	0.4	—	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	—	20	ns	
	Output clock fall time			t_{SCKf}	—	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	—	40	ns	Figure 2.60
	Transmit data delay time (slave)	Clock synchronous	VCC ≥ 2.7 V		—	—	65	ns	
			VCC < 2.7 V		—	—	100	ns	
	Receive data setup time (master)	Clock synchronous	VCC ≥ 2.7 V	t_{RXS}	65	—	—	ns	
			VCC < 2.7 V		90	—	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	—	ns	

Note 1. t_{Pcyc}: PCLK cycle

Table 2.36 Timing of Simple I²C

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 2.61
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple I²C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 2.61
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{Pcyc}: PCLK cycle
Note 1. C_b is the total capacitance of the bus lines.

Table 2.37 Timing of Simple SPI

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.62
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC ≥ 2.7 V	t_{SU}	65	—	ns	Figure 2.63, Figure 2.64
		VCC < 2.7 V		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC ≥ 2.7 V		—	65		
		VCC < 2.7 V		—	100		
	Data output hold time (master)	VCC ≥ 2.7 V	t_{OH}	–10	—	ns	
		VCC < 2.7 V		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 2.65, Figure 2.66
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

2.4.5.6 RIIC

Table 2.38 Timing of RIIC

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.61
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	RESTART condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.61
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	RESTART condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

2.4.5.7 RSPI

Table 2.39 Timing of RSPI

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.62
		Slave			6	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC ≥ 2.7 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			VCC < 2.7 V		—	15		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC ≥ 2.7 V	t_{SU}	10	—	ns	Figure 2.63 to Figure 2.66
			VCC < 2.7 V		30	—		
		Slave			25	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	20	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC ≥ 2.7 V	t_{OD}	—	14	ns	
			VCC < 2.7 V		—	30		
		Slave	VCC ≥ 2.7 V		—	65		
			VCC < 2.7 V		—	105		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	VCC ≥ 2.7 V	t_{Dr}, t_{Df}	—	10	ns	
			VCC < 2.7 V		—	15		
		Input			—	1	μs	
	SSL rise/fall time	Output	VCC ≥ 2.7 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			VCC < 2.7 V		—	15	ns	
		Input			—	1	μs	
	Slave access time		VCC ≥ 2.7 V	t_{SA}	—	6	t_{Pcyc}	Figure 2.65, Figure 2.66
			VCC < 2.7 V		—	7		
	Slave output release time		VCC ≥ 2.7 V	t_{REL}	—	5	t_{Pcyc}	
			VCC < 2.7 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

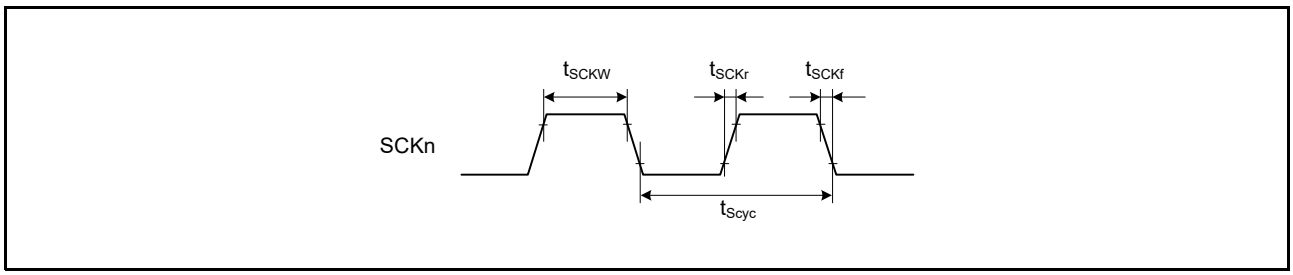


Figure 2.59 SCK Clock Input Timing (n = 1, 5, 6, 12)

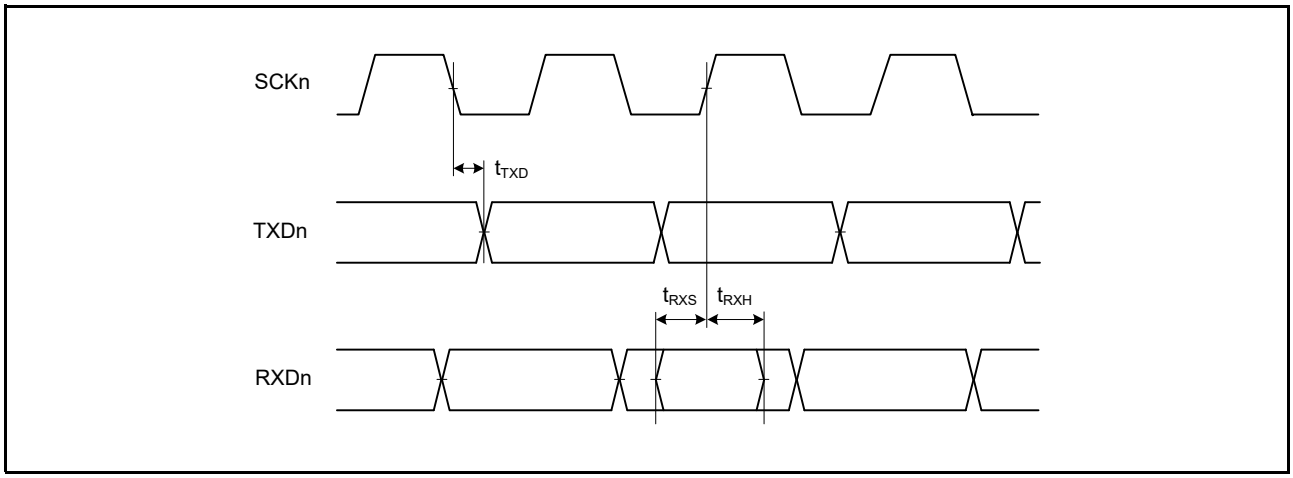
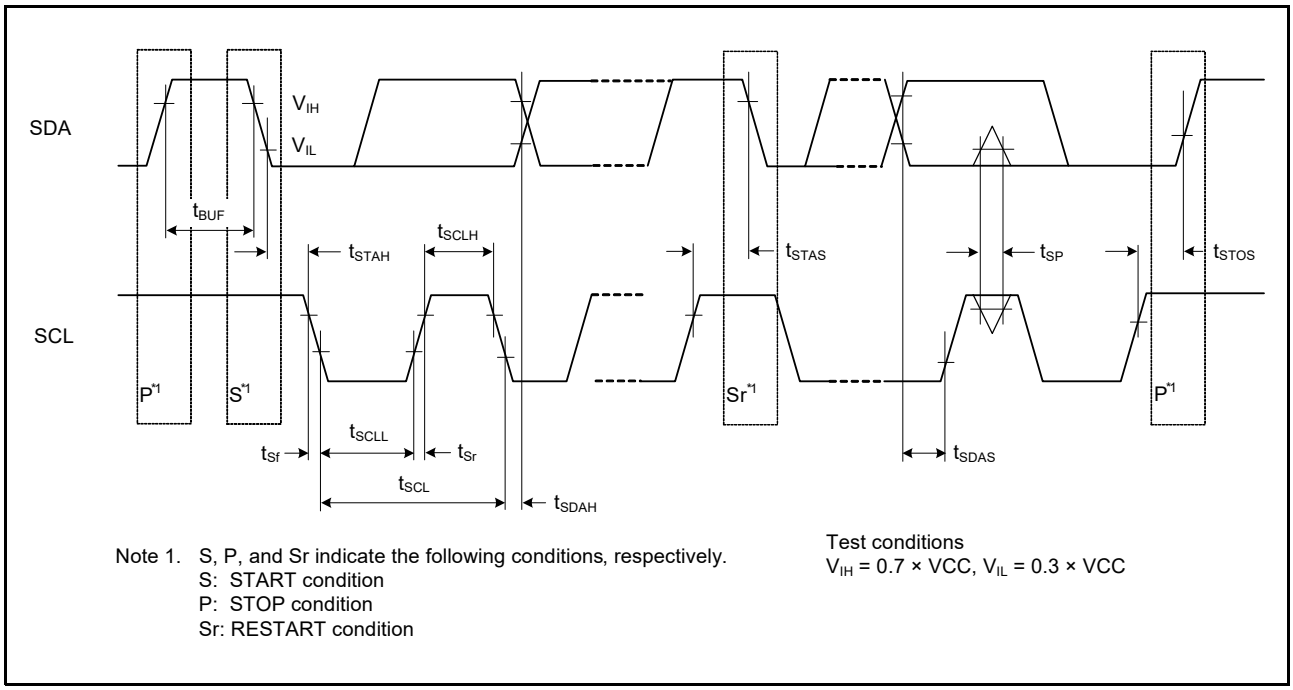


Figure 2.60 SCI Input/Output Timing: Clock Synchronous Mode (n = 1, 5, 6, 12)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: RESTART condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.61 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

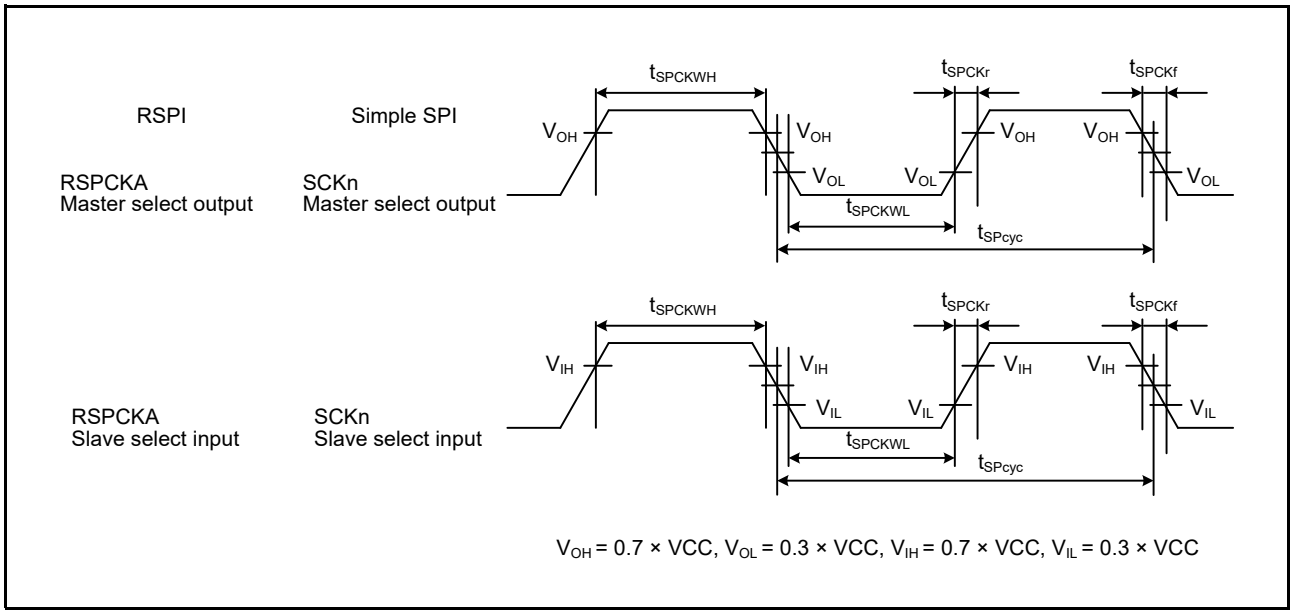


Figure 2.62 RSPI Clock Timing and Simple SPI Clock Timing (n = 1, 5, 6, 12)

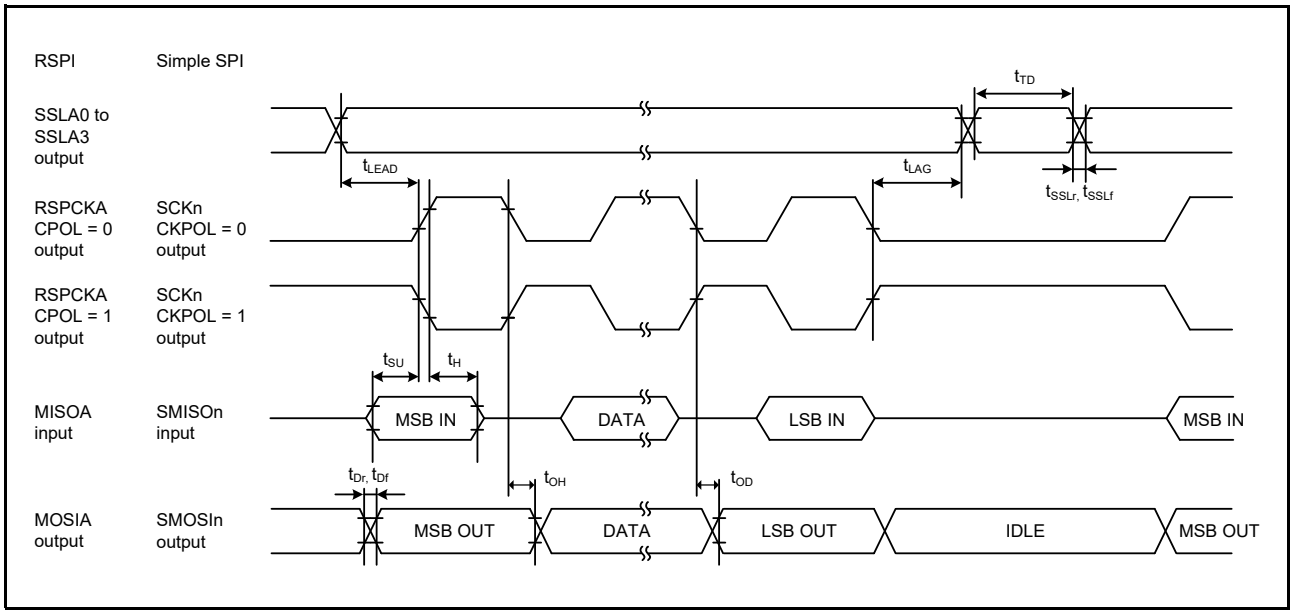


Figure 2.63 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1) (n = 1, 5, 6, 12)

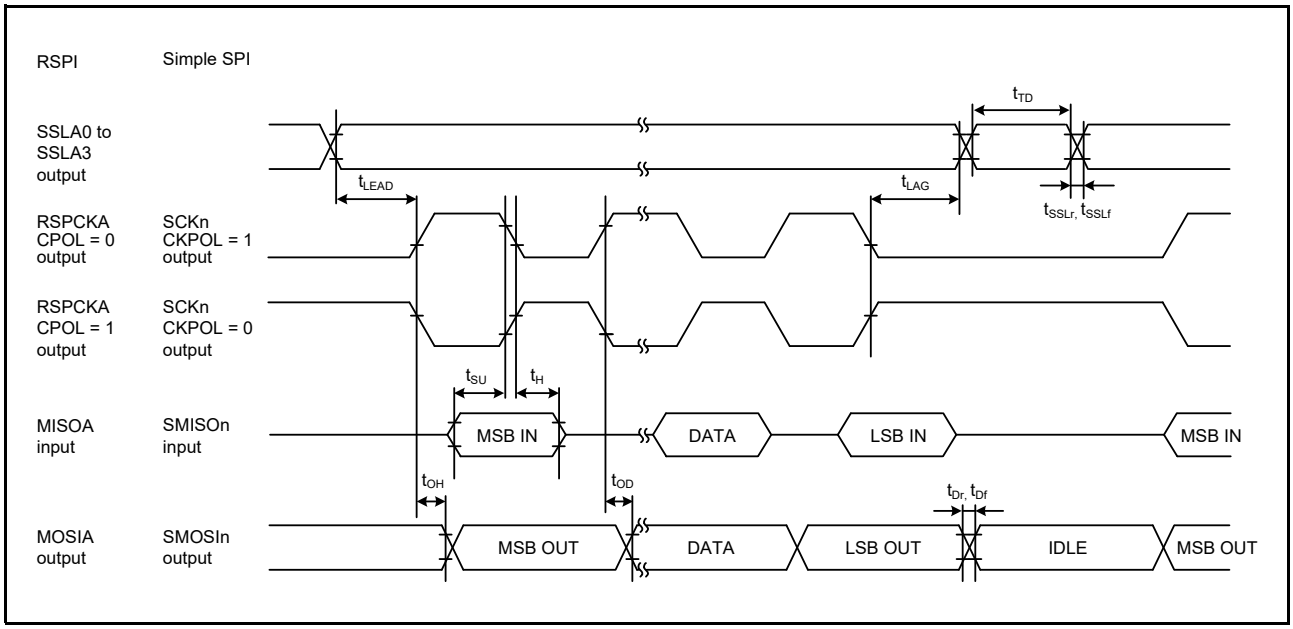


Figure 2.64 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0) (n = 1, 5, 6, 12)

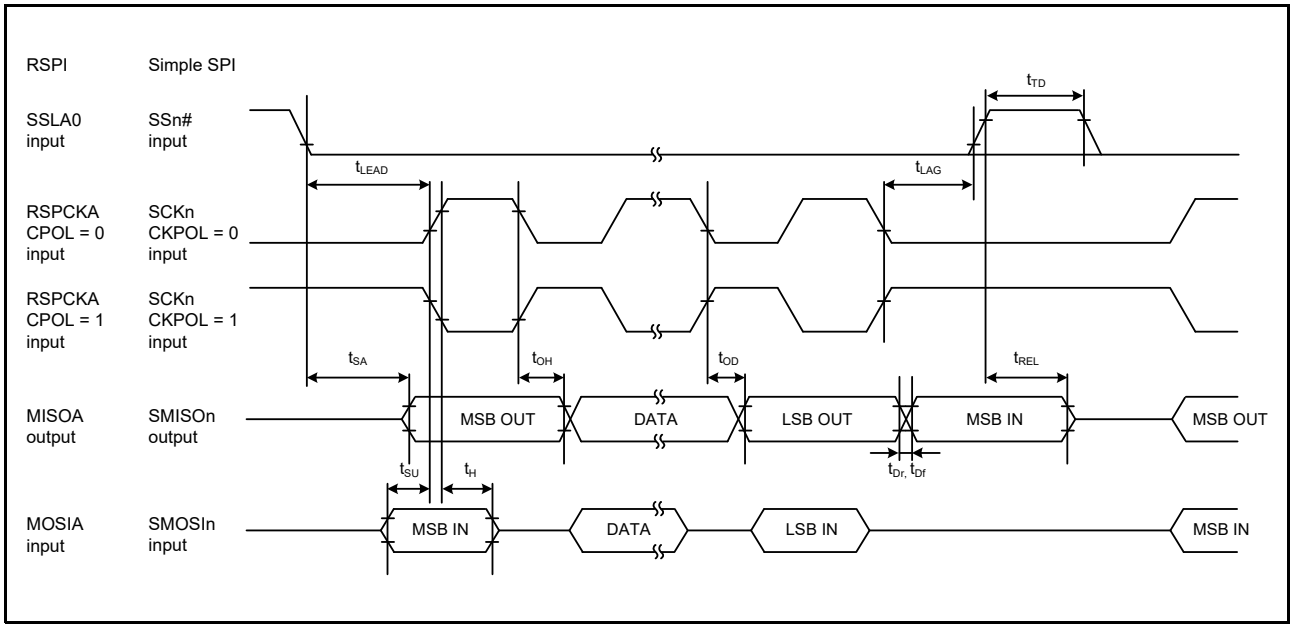


Figure 2.65 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1) (n = 1, 5, 6, 12)

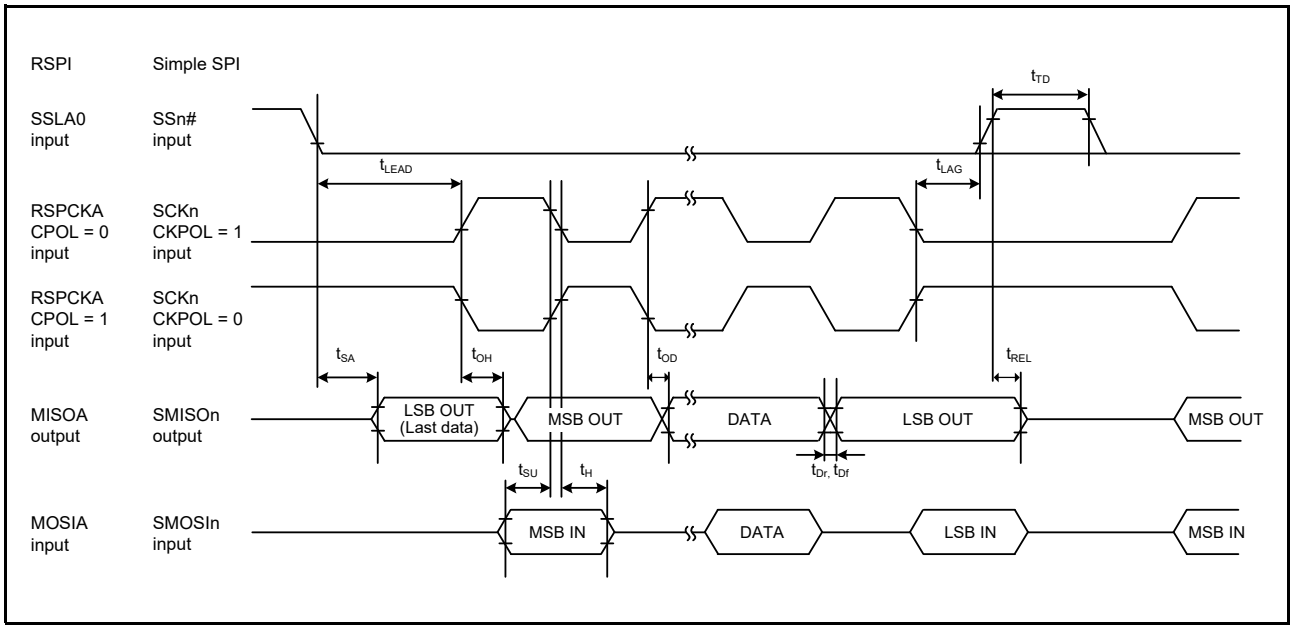


Figure 2.66 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0) (n = 1, 5, 6, 12)

2.4.5.8 A/D converter Trigger

Table 2.40 Timing of A/D converter Trigger)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	—	t_{Pcyc}	Figure 2.67

Note 1. t_{Pcyc}: PCLK cycle

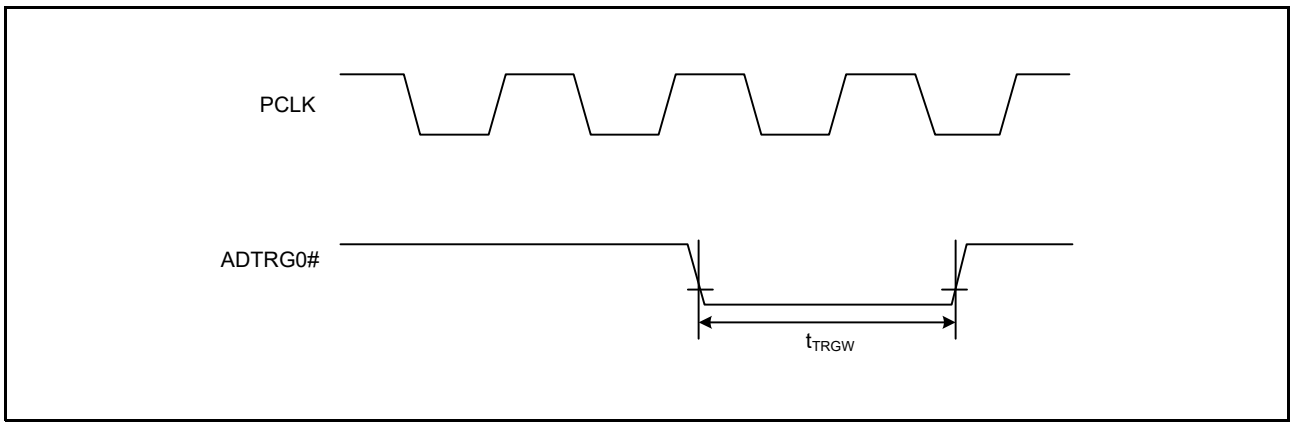


Figure 2.67 A/D Converter External Trigger Input Timing

2.4.5.9 CAC

Table 2.41 Timing of CAC

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—			
	CACREF input rise/fall time		$t_{CACREFr}$, $t_{CACREFf}$	—	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

2.4.5.10 CLKOUT

Table 2.42 Timing of CLKOUT

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
CLKOUT	CLKOUT pin output cycle*3	VCC ≥ 2.7 V	t_{Ccyc}	62.5	—	—	ns	Figure 2.68
		VCC < 2.7 V		125	—			
	CLKOUT pin high pulse width*2	VCC ≥ 2.7 V	t_{CH}	15	—	—	ns	
		VCC < 2.7 V		30	—			
	CLKOUT pin low pulse width*2	VCC ≥ 2.7 V	t_{CL}	15	—	—	ns	
		VCC < 2.7 V		30	—			
	CLKOUT pin output rise time	VCC ≥ 2.7 V	t_{Cr}	—	—	12	ns	
		VCC < 2.7 V			—	25		
	CLKOUT pin output fall time	VCC ≥ 2.7 V	t_{Cf}	—	—	12	ns	
		VCC < 2.7 V			—	25		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).
Note 3. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

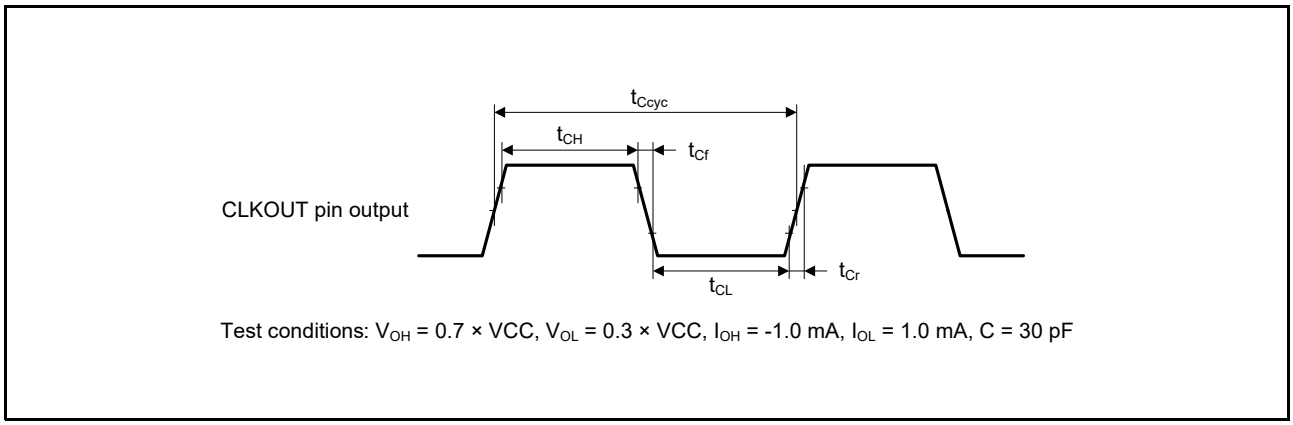


Figure 2.68 CLKOUT Output Timing

2.5 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 2.43 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 2.69, Figure 2.70
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	Figure 2.71 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 2.72 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.58	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48	V	Figure 2.73 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

Table 2.44 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after release from the power-on reset	At normal startup	t_{POR}	—	9.1	—	ms	Figure 2.70
	During fast startup time	t_{POR}	—	1.6	—		
Wait time after release from voltage monitoring 0 reset		t_{LVD0}	—	600	—	µs	Figure 2.71
Wait time after release from voltage monitoring 1 reset		t_{LVD1}	—	150	—	µs	Figure 2.72
Wait time after release from voltage monitoring 2 reset		t_{LVD2}	—	150	—	µs	Figure 2.73
Response delay time		t_{det}	—	—	350	µs	Figure 2.69
Minimum VCC down time*1		t_{VOFF}	350	—	—	µs	Figure 2.69, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 2.70, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 2.72, Figure 2.73
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (voltage detection circuit: LVD0, LVD1 and LVD2)		V_{LVH}	—	70	—	mV	When Vdet1_0 to Vdet1_4 is selected
			—	60	—		When Vdet1_5 to Vdet1_9 is selected
			—	50	—		When Vdet1_A or Vdet1_B is selected
			—	40	—		When Vdet1_C or Vdet1_D is selected
			—	60	—		When LVD0 or LVD2 is selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

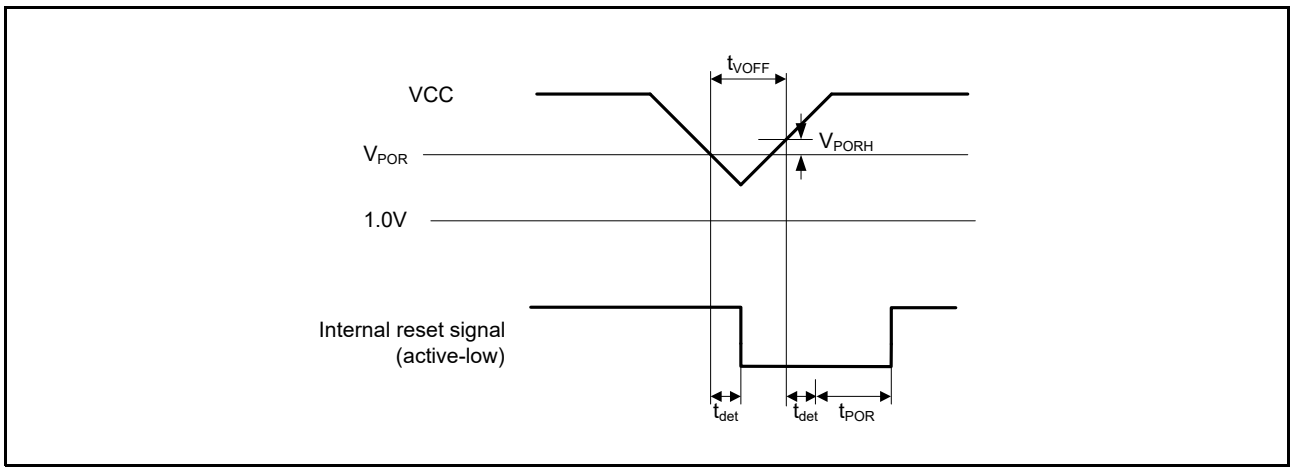
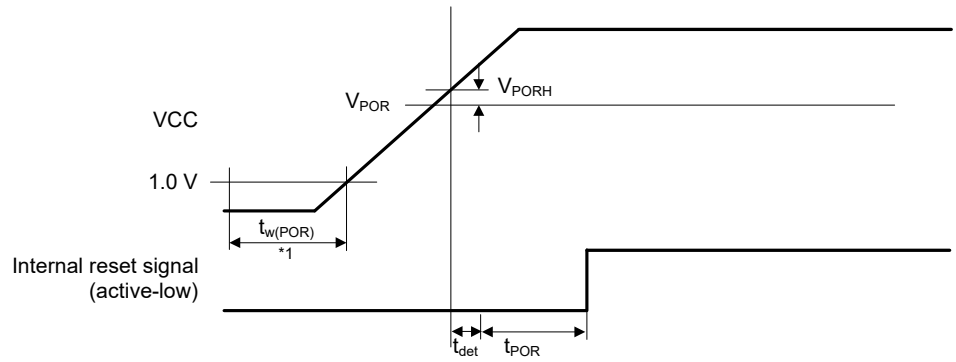


Figure 2.69 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 2.70 Power-On Reset Timing

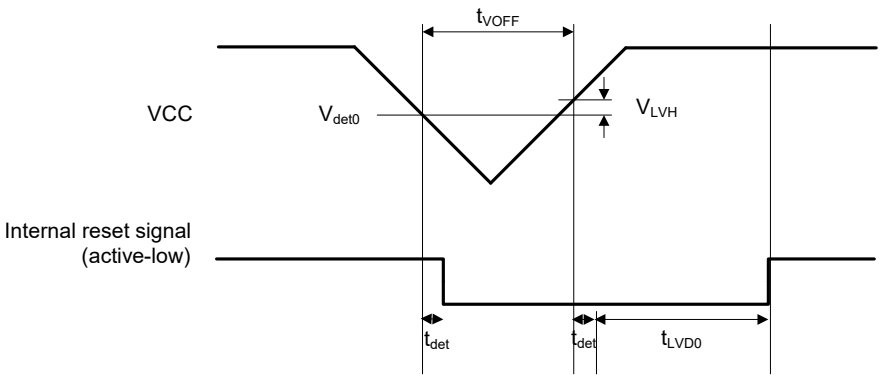


Figure 2.71 Voltage Detection Circuit Timing (Vdet0)

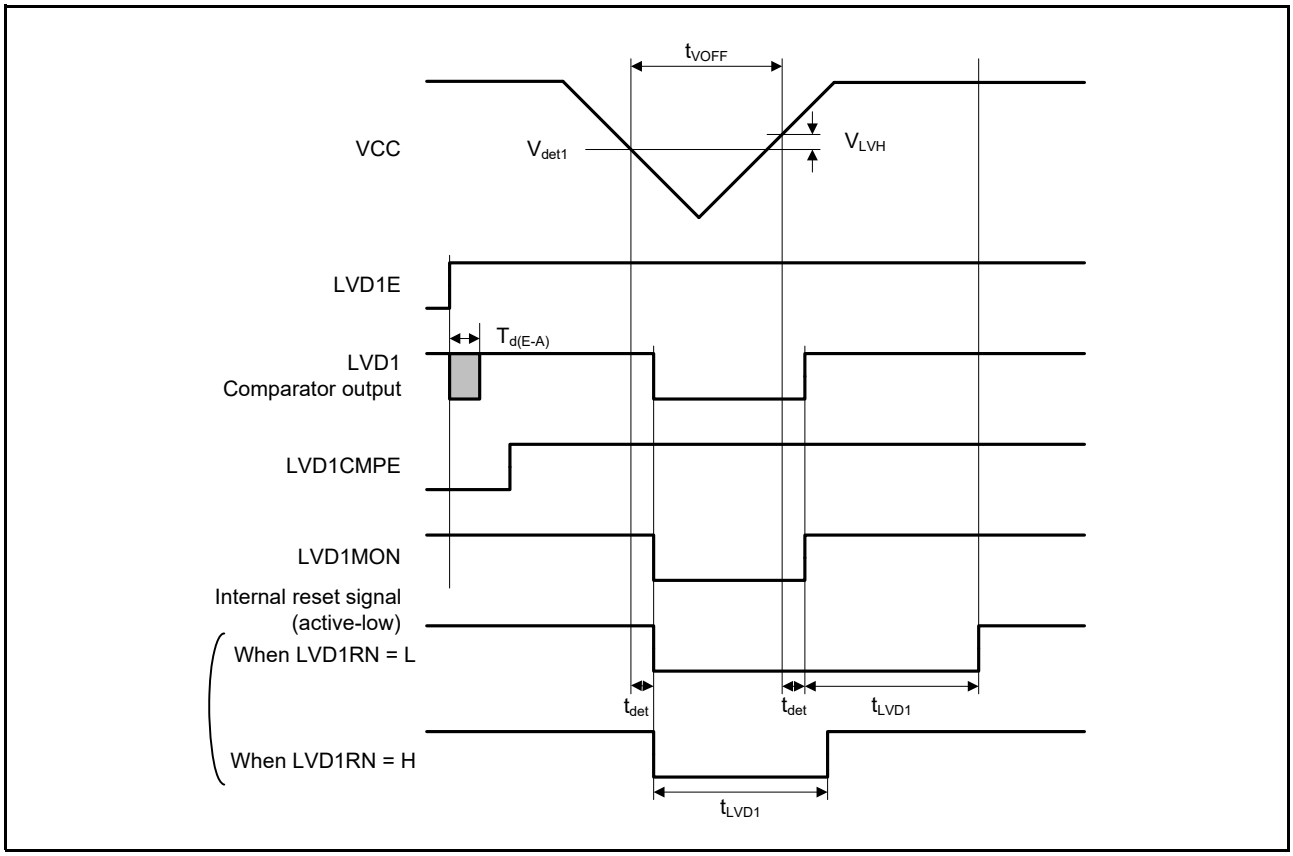


Figure 2.72 Voltage Detection Circuit Timing (V_{det1})

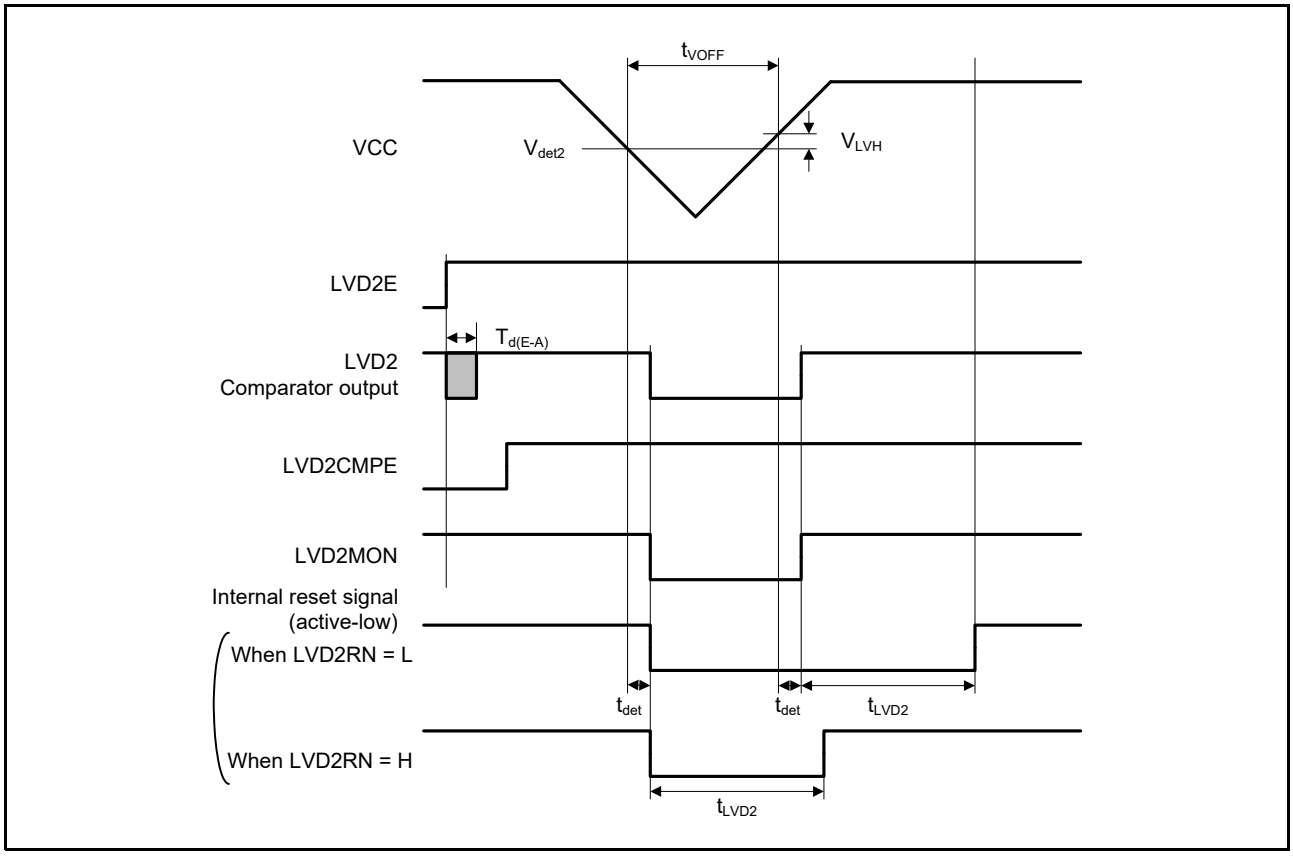


Figure 2.73 Voltage Detection Circuit Timing (V_{det2})

2.6 Oscillation Stop Detection Timing

Table 2.45 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.74

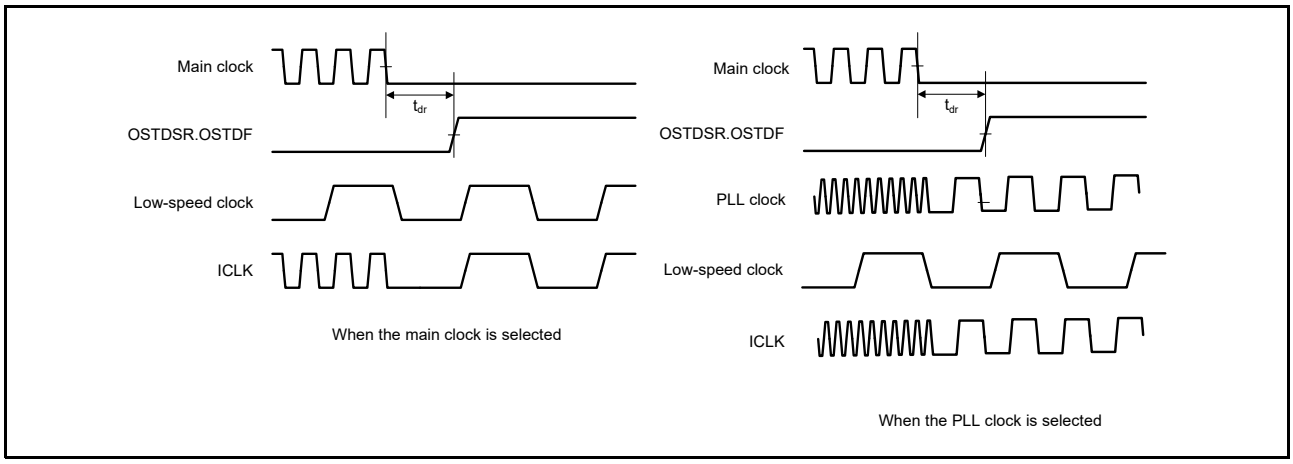


Figure 2.74 Oscillation Stop Detection Timing

2.7 ROM (Code Flash Memory) Characteristics

Table 2.46 ROM (Code Flash Memory) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{PEC}	1000	—	—	Times	
Data retention	After 1000 times of erase	t_{DRP}	20*2, *3	—	—	Year	T_a = 85°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 256 times for different addresses in a 1-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.47 ROM (Code Flash Memory) Characteristics (2) (High-Speed Operating Mode)

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	8-byte	t_{P8}	—	112.0	967.0	—	52.3	490.5	µs
Erase time	2-Kbyte	t_{E2K}	—	8.7	278.1	—	5.5	214.6	ms
	256-Kbyte (when block erase command is used)	t_{E256K}	—	469.1	9813.6	—	41.2	1049.2	ms
	256-Kbyte (when all-block erase command is used)	t_{EA256K}	—	463.9	9609.0	—	36.0	839.5	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840.0	—	—	135.7	µs
Erase operation forced stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching time		t_{SAS}	—	12.3	566.5	—	6.2	433.5	ms
Access window setting time		t_{AWS}	—	12.3	566.5	—	6.2	433.5	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 2.48 ROM (Code Flash Memory) Characteristics (3) (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	8-byte	t_{P8}	—	152.0	1367.0	—	97.9	936.0	µs
Erase time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	220.8	ms
	256-Kbyte (when block erase command is used)	t_{E256K}	—	469.2	9816.9	—	100.5	2260.1	ms
	256-Kbyte (when all-block erase command is used)	t_{EA256K}	—	464.0	9610.7	—	95.3	2053.7	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.9	µs
	2-Kbyte	t_{BC2K}	—	—	1870.0	—	—	401.5	µs
Erase operation forced stop time		t_{SED}	—	—	28.0	—	—	21.3	µs
Start-up area switching time		t_{SAS}	—	13.0	573.3	—	7.7	450.1	ms
Access window setting time		t_{AWS}	—	13.0	573.3	—	7.7	450.1	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.

2.8 E2 DataFlash (Data Flash Memory) Characteristics

Table 2.49 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{DPEC}	100000	1000000	—	Times	
Data retention	After 10000 times of erase	t_{DDRP}	20*2, *3	—	—	Year	T_a = 85°C
	After 100000 times of erase		5*2, *3	—	—	Year	
	After 1000000 times of erase		—	1*2, *3	—	Year	T_a = 25°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycle is n, each block can be erased n times. For instance, when 1-byte program is performed 1000 times for different addresses in a 1-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when the flash programmer is used and the self-programming library is provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.50 E2 DataFlash Characteristics (2) (High-Speed Operating Mode)

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	1 byte	t_{DP1}	—	95.0	797.0	—	40.8	375.5	µs
Erase time	1 Kbyte	t_{DE1K}	—	19.5	498.5	—	6.2	229.4	ms
	8 Kbyte	t_{DE8K}	—	119.8	2555.7	—	12.9	367.2	ms
Blank check time	1 byte	t_{DBC1}	—	—	55.0	—	—	16.1	µs
	1 Kbyte	t_{DBC1K}	—	—	7216.0	—	—	495.7	µs
Erase operation forced stop time		t_{DSED}	—	—	16.0	—	—	10.7	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 2.51 E2 DataFlash Characteristics (3) (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{DP1}	—	135.0	1197.0	—	86.5	822.5	µs
Erasure time	1 Kbyte	t_{DE1K}	—	19.6	500.1	—	8.0	264.1	ms
	8 Kbyte	t_{DE8K}	—	119.9	2557.4	—	27.7	668.2	ms
Blank check time	1 byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1 Kbyte	t_{DBC1K}	—	—	7246.0	—	—	1457.5	µs
Erase operation forced stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
DataFlash STOP recovery time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

2.9 24-Bit Delta-Sigma A/D Converter Characteristics

Table 2.52 24-Bit Delta-Sigma A/D Converter Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gain		Gain	1, 2, 4, 8, 16, 32, 64, 128			—	
Output data rate	Normal mode	f_{DR}	7.6	—	15625	SPS	
	Low power mode		1.9	—	3906		
Resolution (no missing codes)		—	24	—	—	Bits	
RMS noise		V_N	—	Table 2.53, Table 2.55	—	—	Figure 2.75 to Figure 2.91
Integral non-linearity	Gain = 1 (PGA enabled), Normal/low power mode, OPCR.DSADLVM bit = 0	INL	—	±7	±15	ppmFSR	Figure 2.92, Figure 2.93 AVCC0 = 3.6 to 5.5 V
	Gain = 2 to 64, Normal/low power mode, OPCR.DSADLVM bit = 0		—	±4	±15		
	Gain = 128, Normal mode, OPCR.DSADLVM bit = 0		—	±5	±15		
	Gain = 128, Low power mode, OPCR.DSADLVM bit = 0		—	±7	±20		
	Gain = 1 to 128 (PGA enabled), Normal/low power mode, OPCR.DSADLVM bit = 1		—	±7	±30		AVCC0 = 2.7 to 5.5 V
	Gain = 1 (PGA disabled, BUF disabled)		—	±7	±20		AVCC0 = 2.7 to 5.5 V, V_I < 2.6 V
	Gain = 1 (PGA disabled, BUF enabled)		—	±7	—		
Offset error	Before calibration	E_O	—	—	±10	μV	Figure 2.94 AVCC0 = 5.0 V, T_a = 25°C, Normal mode, Gain = 2
	After calibration		—	Less than or equal to the RMS noise	—		
Offset drift	Gain = 1 or 2 (PGA enabled)	dE_O	—	60	220	nV/°C	Figure 2.94
	Gain = 4 to 8		—	40	140		
	Gain = 16 to 32		—	15	40		
	Gain = 64 to 128		—	10	25		
	Gain = 1 (PGA disabled, BUF disabled)		—	50	140		
Gain error	Gain = 1 to 64 (PGA enabled)	E_G	—	±0.01	±0.03	%	Figure 2.95 T_a = 25°C
	Gain = 128		—	±0.01	±0.04		
	Gain = 1 (PGA disabled, BUF disabled)		—	±0.015	±0.04		
	Gain = 1 (PGA disabled, BUF enabled)		—	±0.03	—		
	After calibration of gain errors		—	Less than or equal to the RMS noise	—		

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gain drift	Gain = 1 to 128 (PGA enabled), OPCR.DSADLVM bit = 0	dE_G	—	1	3	ppm/°C	Figure 2.95
	Gain = 1 to 128 (PGA enabled), OPCR.DSADLVM bit = 1		—	1	5		AVCC0 = 3.0 to 5.5 V
			—	—	10		AVCC0 < 3.0 V
	Gain = 1 (PGA disabled)		—	1.4	—		Figure 2.95 V_I < 2.6 V
Power supply rejection ratio	Gain = 1 (PGA enabled)	PSRR	80	88	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 2 to 16		89	95	—		
	Gain = 32 to 128		102	115	—		
	Gain = 1 (PGA disabled, BUF disabled)		68	88	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		—	78	—		
Common mode rejection ratio	Gain = 1 to 8 (PGA enabled), OPCR.DSADLVM bit = 0	CMRR	95	100	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 32, OPCR.DSADLVM bit = 0		110	120	—		
	Gain = 64 to 128, OPCR.DSADLVM bit = 0		120	130	—		
	Gain = 1 to 8 (PGA enabled), OPCR.DSADLVM bit = 1		80	100	—		
	Gain = 16 to 32, OPCR.DSADLVM bit = 1		88	120	—		
	Gain = 64 to 128, OPCR.DSADLVM bit = 1		100	130	—		
	Gain = 1 (PGA disabled, BUF disabled)		60	88	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		—	78	—		
Normal mode rejection ratio	External clock, 50 Hz, 60 Hz	NMRR	120	—	—	dB	10 SPS, 50 ± 1 Hz, 60 ± 1 Hz
			75	—	—		54 SPS, 50 ± 1 Hz, 60 ± 1 Hz
	External clock, 50 Hz		120	—	—		50 SPS, 50 ± 1 Hz
	External clock, 60 Hz		120	—	—		60 SPS, 60 ± 1 Hz
	Internal clock (HOCO), 50 Hz, 60 Hz		110	—	—		10 SPS, 50 ± 1 Hz, 60 ± 1 Hz
			70	—	—		54 SPS, 50 ± 1 Hz, 60 ± 1 Hz
	Internal clock (HOCO), 50 Hz		110	—	—		50 SPS, 50 ± 1 Hz
	Internal clock (HOCO), 60 Hz		110	—	—		60 SPS, 60 ± 1 Hz
Burnout current		I_{BO}	0.5, 2, 4, 20			μA	
Modulator clock	Normal mode	f_{MOD}	430	500	570	kHz	
	Low power mode		107.5	125.0	142.5		

Table 2.53 Typical Noise Characteristics (Normal Mode)

Conditions: AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 500 kHz, V_{ID} = 0 V, V_{REF} = 2.5 V

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
7.6	65536	0.383 (2.39)	0.524 (2.69)	0.601 (3.89)	0.563 (3.59)	0.284 (2.02)	0.166 (1.08)	0.097 (0.60)	0.052 (0.34)	0.036 (0.28)	0.029 (0.20)
10	50048	0.426 (2.64)	0.671 (3.96)	0.680 (4.40)	0.618 (4.18)	0.322 (2.53)	0.185 (1.15)	0.108 (0.71)	0.056 (0.40)	0.041 (0.27)	0.033 (0.20)
50	9984	0.878 (5.42)	1.117 (7.59)	1.308 (9.76)	1.196 (7.59)	0.667 (5.15)	0.369 (2.51)	0.230 (1.69)	0.121 (0.92)	0.084 (0.61)	0.072 (0.52)
54	9216	0.929 (6.35)	1.225 (9.71)	1.359 (10.5)	1.254 (9.52)	0.702 (4.85)	0.392 (2.85)	0.240 (1.70)	0.127 (0.88)	0.090 (0.59)	0.076 (0.51)
60	8320	0.973 (7.31)	1.279 (8.99)	1.450 (10.7)	1.345 (9.27)	0.723 (4.50)	0.426 (3.30)	0.258 (1.48)	0.129 (1.07)	0.093 (0.59)	0.080 (0.58)
100	4992	1.228 (8.67)	1.673 (11.4)	1.873 (13.0)	1.673 (9.76)	0.904 (5.96)	0.536 (3.46)	0.327 (2.41)	0.172 (1.19)	0.128 (0.96)	0.100 (0.68)
195	2560	1.681 (12.7)	2.206 (18.6)	2.530 (16.7)	2.378 (16.7)	1.277 (8.45)	0.710 (4.65)	0.460 (3.15)	0.238 (1.55)	0.176 (1.16)	0.139 (0.90)
488	1024	2.697 (17.3)	3.311 (22.4)	3.954 (29.3)	3.881 (27.4)	2.007 (13.5)	1.175 (8.52)	0.723 (4.73)	0.355 (2.28)	0.264 (1.80)	0.231 (1.55)
977	512	3.691 (27.5)	4.740 (29.0)	5.758 (36.5)	5.442 (35.7)	2.871 (20.0)	1.656 (12.0)	1.025 (6.67)	0.522 (3.53)	0.389 (2.57)	0.321 (2.21)
1953	256	5.734 (35.3)	6.572 (42.5)	8.535 (55.3)	7.438 (48.9)	4.130 (28.2)	2.308 (15.8)	1.434 (9.34)	0.768 (4.85)	0.567 (4.05)	0.476 (2.71)
3906	128	7.446 (51.1)	9.607 (65.8)	12.32 (70.0)	11.15 (76.5)	5.778 (38.6)	3.476 (27.2)	2.237 (14.7)	1.162 (7.83)	0.831 (5.98)	0.669 (4.21)
7813	64	13.60 (102)	15.91 (110)	21.39 (143)	19.22 (120)	10.43 (67.6)	5.971 (39.0)	3.760 (26.4)	2.161 (13.9)	1.482 (11.0)	1.112 (6.96)
15625	32	120.5 (644)	117.5 (720)	112.5 (735)	67.81 (347)	36.42 (218)	17.96 (109)	9.766 (58.7)	5.812 (37.6)	3.726 (22.2)	2.498 (16.9)

Note: "Bypass" indicates the state where both PGA and BUF are disabled, "BUF" indicates the state where PGA is disabled and BUF is enabled, and "PGA" indicates the state where PGA is enabled.

Note: The upper rows indicate RMS noise (μV_{RMS}) and the lower rows (in parentheses) indicate peak-to-peak noise (μV_{PP}).

Table 2.54 Effective Resolution (Normal Mode)

Conditions: AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 500 kHz, V_{ID} = 0 V, V_{REF} = 2.5 V

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
7.6	65536	23.6 (21.0)	23.1 (20.8)	23.0 (20.3)	22.1 (19.4)	22.1 (19.2)	21.8 (19.1)	21.6 (19.0)	21.5 (18.8)	21.0 (18.1)	20.4 (17.6)
10	50048	23.5 (20.9)	22.8 (20.2)	22.8 (20.1)	22.0 (19.2)	21.9 (18.9)	21.7 (19.1)	21.5 (18.7)	21.4 (18.6)	20.9 (18.2)	20.2 (17.6)
50	9984	22.4 (19.8)	22.0 (19.3)	21.9 (19.0)	21.0 (18.3)	20.8 (17.9)	20.7 (17.9)	20.4 (17.5)	20.3 (17.4)	19.8 (17.0)	19.0 (16.2)
54	9216	22.4 (19.6)	21.9 (18.9)	21.8 (18.9)	20.9 (18.0)	20.8 (18.0)	20.6 (17.7)	20.3 (17.5)	20.2 (17.5)	19.7 (17.0)	19.0 (16.2)
60	8320	22.3 (19.4)	21.8 (19.0)	21.7 (18.8)	20.8 (18.0)	20.7 (18.1)	20.5 (17.5)	20.2 (17.7)	20.2 (17.2)	19.7 (17.0)	18.9 (16.1)
100	4992	22.0 (19.1)	21.5 (18.7)	21.4 (18.6)	20.5 (18.0)	20.4 (17.7)	20.2 (17.5)	19.9 (17.0)	19.8 (17.0)	19.2 (16.3)	18.6 (15.8)
195	2560	21.5 (18.6)	21.1 (18.0)	21.0 (18.2)	20.0 (17.2)	19.9 (17.2)	19.8 (17.0)	19.4 (16.6)	19.3 (16.6)	18.8 (16.0)	18.1 (15.4)
488	1024	20.8 (18.1)	20.5 (17.7)	20.3 (17.4)	19.3 (16.5)	19.3 (16.5)	19.0 (16.2)	18.7 (16.0)	18.8 (16.1)	18.2 (15.4)	17.4 (14.6)
977	512	20.4 (17.5)	20.0 (17.3)	19.7 (17.1)	18.8 (16.1)	18.7 (15.9)	18.5 (15.7)	18.2 (15.5)	18.2 (15.4)	17.6 (14.9)	16.9 (14.1)
1953	256	19.7 (17.1)	19.5 (16.8)	19.2 (16.5)	18.4 (15.6)	18.2 (15.4)	18.1 (15.3)	17.7 (15.0)	17.6 (15.0)	17.1 (14.2)	16.3 (13.8)
3906	128	19.4 (16.6)	18.9 (16.2)	18.6 (16.1)	17.8 (15.0)	17.7 (15.0)	17.5 (14.5)	17.1 (14.4)	17.0 (14.3)	16.5 (13.7)	15.8 (13.2)
7813	64	18.5 (15.6)	18.2 (15.4)	17.8 (15.1)	17.0 (14.3)	16.9 (14.2)	16.7 (14.0)	16.3 (13.5)	16.1 (13.5)	15.7 (12.8)	15.1 (12.5)
15625	32	15.3 (12.9)	15.3 (12.7)	15.4 (12.7)	15.2 (12.8)	15.1 (12.5)	15.1 (12.5)	15.0 (12.4)	14.7 (12.0)	14.4 (11.8)	13.9 (11.2)

Effective resolution = $\log_2$(full-scale voltage/RMS noise)

Noise-free resolution = $\log_2$(full-scale voltage/peak-to-peak noise)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate effective resolution (bits) and the lower rows (in parentheses) indicate noise-free resolution (bits).

Table 2.55 Typical Noise Characteristics (Low Power Mode)

Conditions: AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 125 kHz, V_{ID} = 0 V, V_{REF} = 2.5 V

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
1.9	65536	0.463 (3.29)	0.640 (4.19)	0.892 (5.38)	0.708 (4.63)	0.444 (2.62)	0.245 (1.72)	0.140 (0.90)	0.070 (0.47)	0.048 (0.34)	0.038 (0.25)
10	12512	1.053 (7.03)	1.313 (8.79)	1.596 (11.4)	1.492 (10.6)	0.797 (5.27)	0.437 (2.86)	0.286 (1.79)	0.143 (1.00)	0.109 (0.72)	0.085 (0.61)
50	2496	2.412 (15.7)	2.883 (18.4)	3.390 (21.7)	3.093 (22.5)	1.669 (11.0)	0.954 (5.96)	0.592 (3.86)	0.317 (2.35)	0.228 (1.69)	0.187 (1.22)
54	2304	2.558 (19.4)	3.098 (20.5)	3.544 (23.9)	3.139 (19.4)	1.719 (11.3)	0.962 (6.39)	0.637 (3.92)	0.333 (2.12)	0.242 (1.81)	0.199 (1.39)
60	2080	2.491 (16.3)	3.230 (20.8)	3.598 (26.4)	3.348 (25.0)	1.810 (13.6)	1.024 (7.38)	0.645 (4.50)	0.346 (2.30)	0.257 (1.88)	0.207 (1.37)
100	1248	3.237 (21.7)	3.843 (26.6)	4.794 (32.5)	4.274 (27.1)	2.319 (15.3)	1.357 (9.35)	0.872 (6.37)	0.454 (2.98)	0.338 (2.29)	0.268 (1.83)
195	640	4.663 (37.7)	5.666 (37.7)	6.826 (46.5)	5.799 (39.7)	3.245 (21.3)	1.930 (12.9)	1.164 (7.50)	0.627 (4.61)	0.474 (3.31)	0.371 (2.68)
488	256	7.451 (46.6)	9.151 (62.5)	10.30 (70.9)	9.404 (59.6)	5.216 (35.7)	2.934 (20.2)	1.869 (13.6)	1.006 (6.13)	0.729 (5.46)	0.599 (4.56)
977	128	10.37 (72.4)	13.13 (83.1)	15.63 (111)	13.71 (93.3)	7.605 (63.0)	4.383 (30.3)	2.796 (18.0)	1.510 (9.78)	1.099 (7.60)	0.908 (7.23)
1953	64	16.80 (117)	19.92 (153)	25.41 (177)	22.23 (138)	12.30 (94.9)	7.226 (50.9)	4.520 (30.6)	2.531 (16.2)	1.927 (13.6)	1.499 (11.1)
3906	32	120.9 (720)	120.4 (761)	126.6 (634)	73.29 (507)	36.82 (216)	19.83 (124)	11.22 (78.4)	6.332 (39.1)	4.427 (27.3)	3.143 (20.0)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate RMS noise (μV_{RMS}) and the lower rows (in parentheses) indicate peak-to-peak noise (μV_{PP}).

Table 2.56 Effective Resolution (Low Power Mode)

Conditions: AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 125 kHz, V_{ID} = 0 V, V_{REF} = 2.5 V

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
1.9	65536	23.4 (20.5)	22.8 (20.1)	22.4 (19.8)	21.8 (19.0)	21.4 (18.9)	21.3 (18.5)	21.1 (18.4)	21.1 (18.4)	20.6 (17.8)	20.0 (17.3)
10	12512	22.2 (19.4)	21.8 (19.1)	21.6 (18.7)	20.7 (17.9)	20.6 (17.9)	20.5 (17.7)	20.1 (17.4)	20.1 (17.3)	19.5 (16.7)	18.8 (16.0)
50	2496	21.0 (18.3)	20.7 (18.0)	20.5 (17.8)	19.6 (16.8)	19.5 (16.8)	19.3 (16.7)	19.0 (16.3)	18.9 (16.0)	18.4 (15.5)	17.7 (15.0)
54	2304	20.9 (18.0)	20.6 (17.8)	20.4 (17.7)	19.6 (17.0)	19.5 (16.8)	19.3 (16.6)	18.9 (16.3)	18.8 (16.2)	18.3 (15.4)	17.6 (14.8)
60	2080	20.9 (18.2)	20.5 (17.8)	20.4 (17.5)	19.5 (16.6)	19.4 (16.5)	19.2 (16.4)	18.9 (16.1)	18.8 (16.1)	18.2 (15.3)	17.5 (14.8)
100	1248	20.6 (17.8)	20.3 (17.5)	20.0 (17.2)	19.2 (16.5)	19.0 (16.3)	18.8 (16.0)	18.5 (15.6)	18.4 (15.7)	17.8 (15.1)	17.2 (14.4)
195	640	20.0 (17.0)	19.7 (17.0)	19.5 (16.7)	18.7 (15.9)	18.6 (15.8)	18.3 (15.6)	18.0 (15.4)	17.9 (15.1)	17.3 (14.5)	16.7 (13.8)
488	256	19.4 (16.7)	19.0 (16.2)	18.9 (16.1)	18.0 (15.4)	17.9 (15.1)	17.7 (14.9)	17.4 (14.5)	17.3 (14.6)	16.7 (13.8)	16.0 (13.1)
977	128	18.9 (16.1)	18.5 (15.8)	18.3 (15.4)	17.5 (14.7)	17.3 (14.3)	17.1 (14.3)	16.8 (14.1)	16.7 (14.0)	16.1 (13.3)	15.4 (12.4)
1953	64	18.2 (15.4)	17.9 (14.9)	17.6 (14.8)	16.8 (14.2)	16.6 (13.7)	16.4 (13.6)	16.1 (13.3)	15.9 (13.2)	15.3 (12.5)	14.7 (11.8)
3906	32	15.3 (12.8)	15.3 (12.6)	15.3 (12.9)	15.1 (12.3)	15.1 (12.5)	14.9 (12.3)	14.8 (12.0)	14.6 (12.0)	14.1 (11.5)	13.6 (10.9)

Effective resolution = $\log_2$(full-scale voltage/RMS noise)

Noise-free resolution = $\log_2$(full-scale voltage/peak-to-peak noise)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate effective resolution (bits) and the lower rows (in parentheses) indicate noise-free resolution (bits).

Table 2.57 24-Bit Delta-Sigma A/D Converter Analog Input Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Differential input voltage range	Gain = 1 (PGA disabled)	V_{IDR}	$-V_{REF}$	—	$+V_{REF}$	V	$V_{REF} = V_{(REFnP)} - V_{(REFnN)}$ (n = 0, 1), or $V_{REF} = V_{REFOUT}$
	Gain = 1 (PGA enabled)		Whichever is greater of the values of $-V_{REF}$ and $-$(AVCC0 – AVSS0 – 0.5V)	—	Whichever is smaller of the values of $+V_{REF}$ and +(AVCC0 – AVSS0 – 0.5V)		
	Gain ≥ 2		$-V_{REF}$/ Gain	—	$+V_{REF}$ / Gain		
Absolute input voltage range	Gain = 1 (PGA disabled, BUF disabled)	V_I	AVSS0 – 0.05	—	AVCC0 + 0.05	V	
	Gain = 1 (PGA disabled, BUF enabled)		AVSS0 + 0.1	—	AVCC0 – 0.1		
	Gain = 1 to 128 (PGA enabled)		AVSS0 – 0.05	—	AVCC0 + 0.05		
Input bias current	Gain = 1 to 128 (PGA enabled)	I_{IB}	—	±5	±25	nA	Figure 2.96 T_a = 25°C
	Gain = 1 (PGA disabled, BUF disabled), OPCR.DSADLVM = 0		—	±1	±5		
	Gain = 1 (PGA disabled, BUF enabled)		—	±1	±5		
	Gain = 1 (PGA disabled, BUF disabled), OPCR.DSADLVM = 1		—	±1.5	±3.0	µA	
Input offset current	Gain = 1 to 128 (PGA enabled)	I_{IO}	—	±3	±10	nA	Figure 2.97 T_a = 25°C
	Gain = 1 (PGA disabled, BUF enabled)		—	±0.5	±2.0		
	Gain = 1 (PGA disabled, BUF disabled)		—	5	10	µA/V	
Input bias current drift	Gain = 1 to 16 (PGA enabled)	dI_{IB}	—	50	180	pA/°C	
	Gain = 32 to 128		—	70	200		
	Gain = 1 (PGA disabled, BUF enabled)		—	50	100		
	Gain = 1 (PGA disabled, BUF disabled), OPCR.DSADLVM = 0		—	50	100		
	Gain = 1 (PGA disabled, BUF disabled), OPCR.DSADLVM = 1		—	300	500		
Input offset current drift	Gain = 1 to 128 (PGA enabled)	dI_{IO}	—	50	200	pA/°C	
	Gain = 1 (PGA disabled, BUF enabled)		—	45	80		
	Gain = 1 (PGA disabled, BUF disabled)		—	170	350	pA/V/°C	

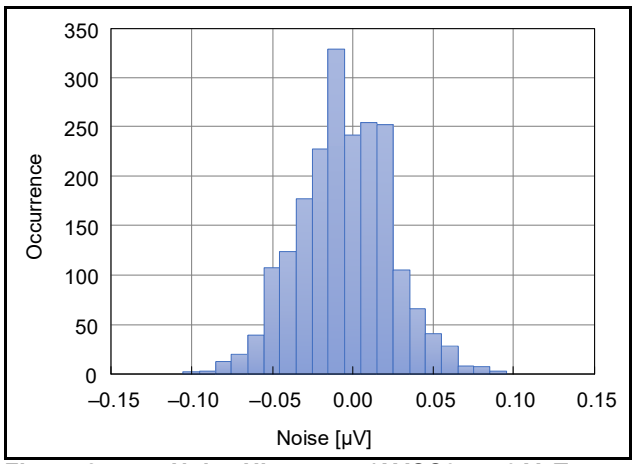


Figure 2.75 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 128, f_{DR} = 7.6 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

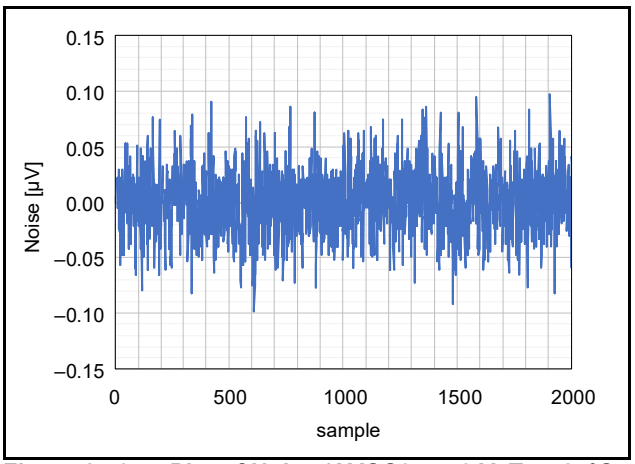


Figure 2.76 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 128, f_{DR} = 7.6 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

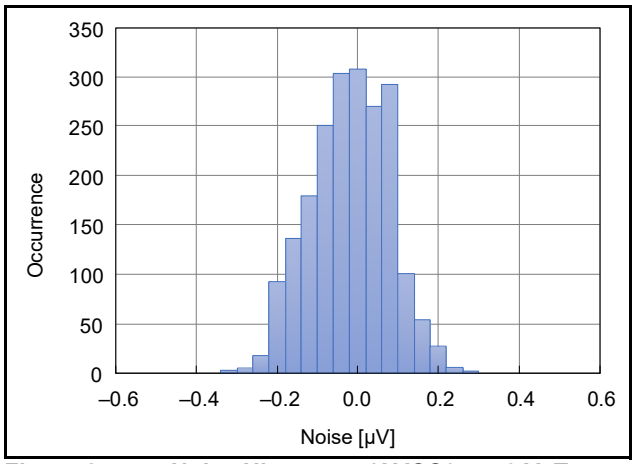


Figure 2.77 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 16, f_{DR} = 7.6 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

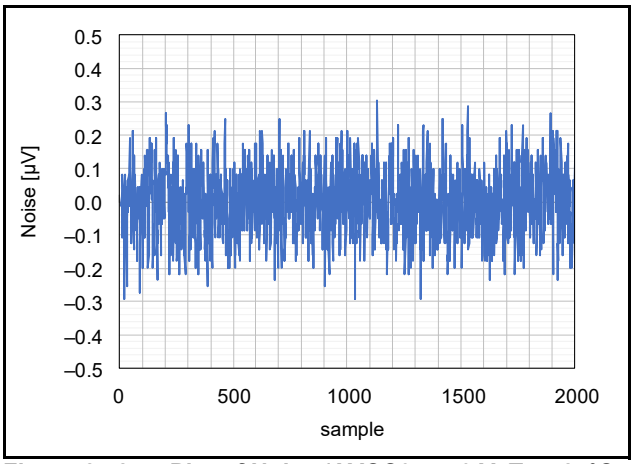


Figure 2.78 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 16, f_{DR} = 7.6 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

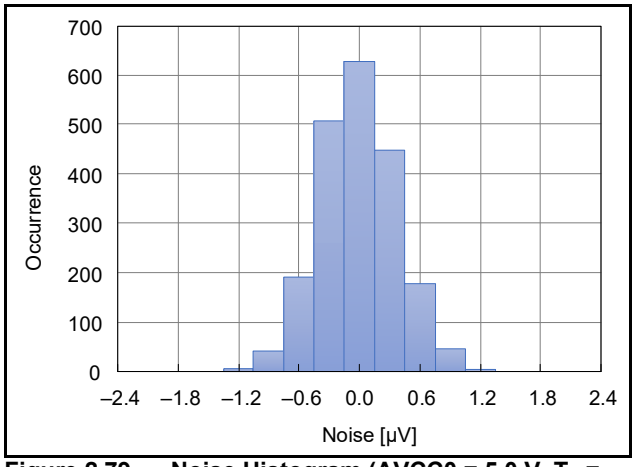


Figure 2.79 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 1 (PGA disabled, BUF disabled), f_{DR} = 7.6 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

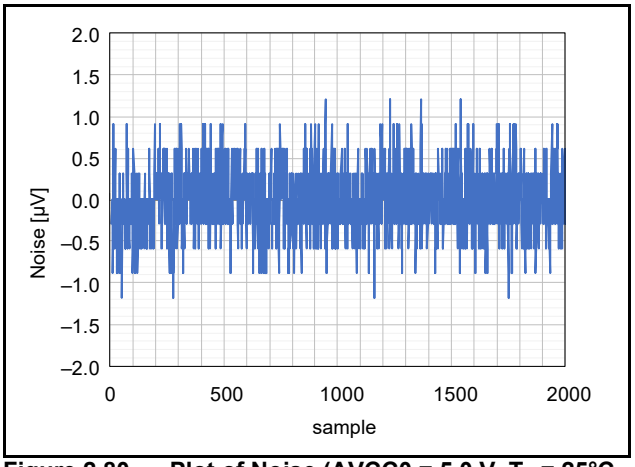


Figure 2.80 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 1 (PGA disabled, BUF disabled), f_{DR} = 7.6 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

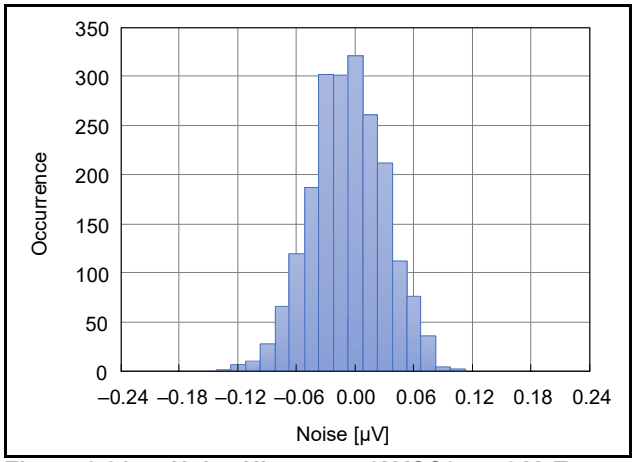


Figure 2.81 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, Gain = 128, f_{DR} = 1.9 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

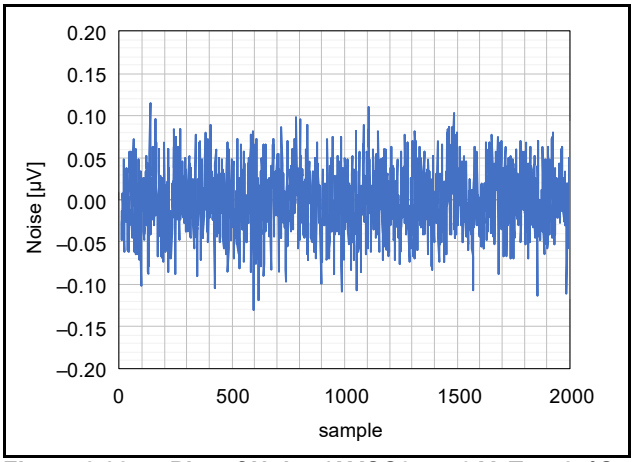


Figure 2.82 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, Gain = 128, f_{DR} = 1.9 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

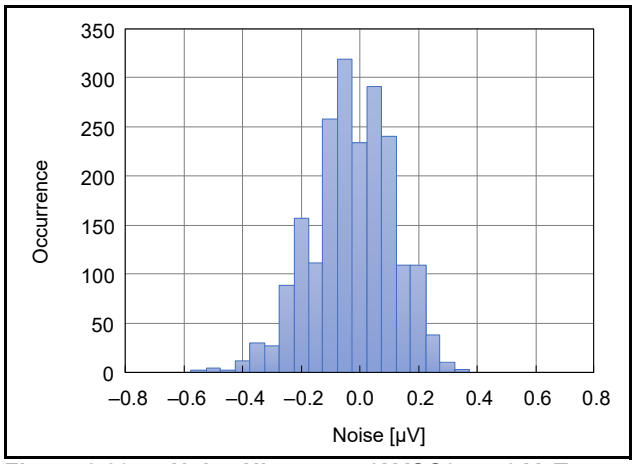


Figure 2.83 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, Gain = 16, f_{DR} = 1.9 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

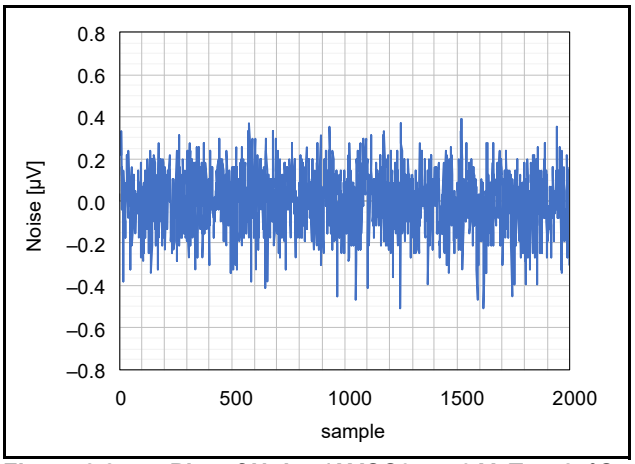


Figure 2.84 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, Gain = 16, f_{DR} = 1.9 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

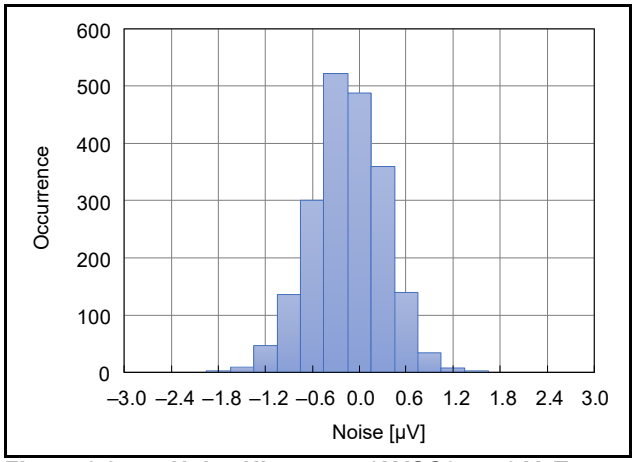


Figure 2.85 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, Gain = 1 (PGA disabled, BUF disabled), f_{DR} = 1.9 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

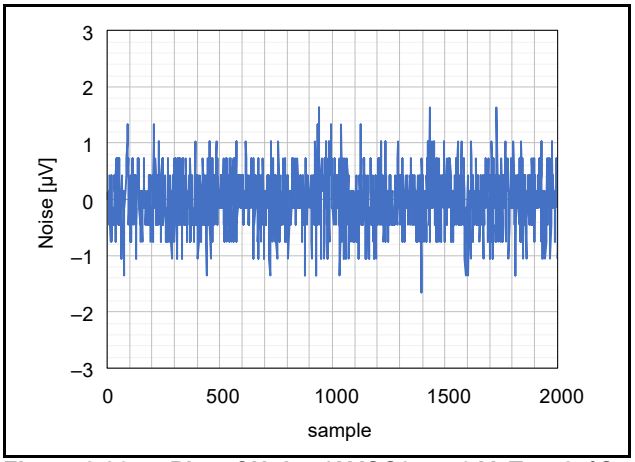


Figure 2.86 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, Gain = 1 (PGA disabled, BUF disabled), f_{DR} = 1.9 SPS, V_{ID} = 0V, V_{REF} = 2.5V)

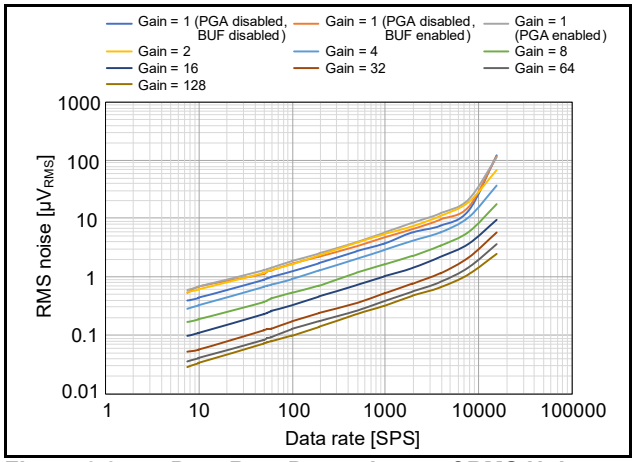


Figure 2.87 Data Rate Dependence of RMS Noise (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, V_{ID} = 0V, V_{REF} = 2.5V)

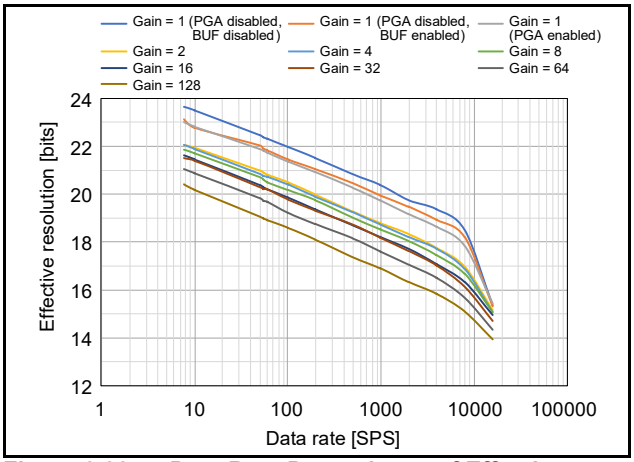


Figure 2.88 Data Rate Dependence of Effective Resolution (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, V_{ID} = 0V, V_{REF} = 2.5V)

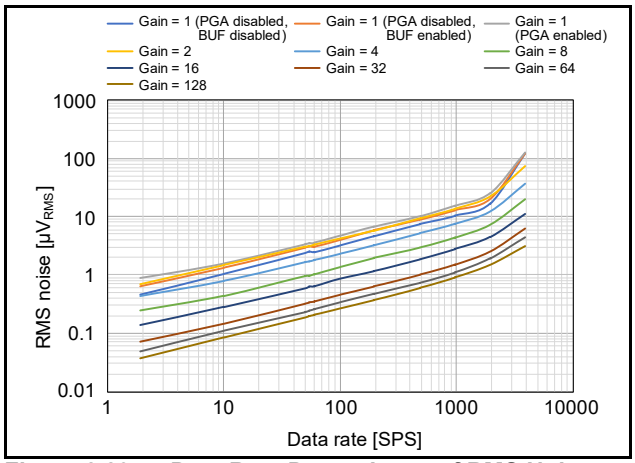


Figure 2.89 Data Rate Dependence of RMS Noise (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, V_{ID} = 0V, V_{REF} = 2.5V)

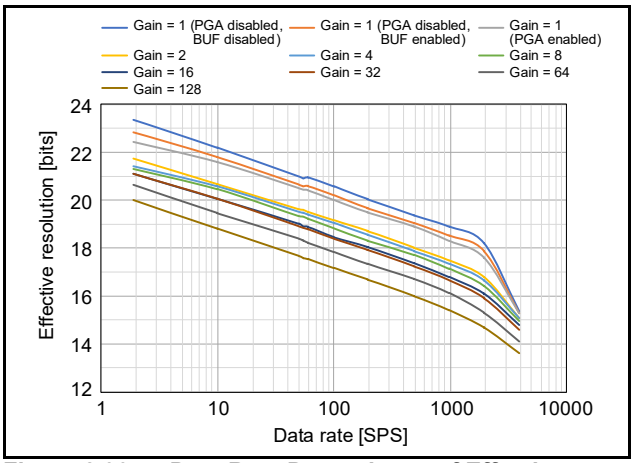


Figure 2.90 Data Rate Dependence of Effective Resolution (AVCC0 = 5.0 V, T_a = 25°C, Low Power Mode, V_{ID} = 0V, V_{REF} = 2.5V)

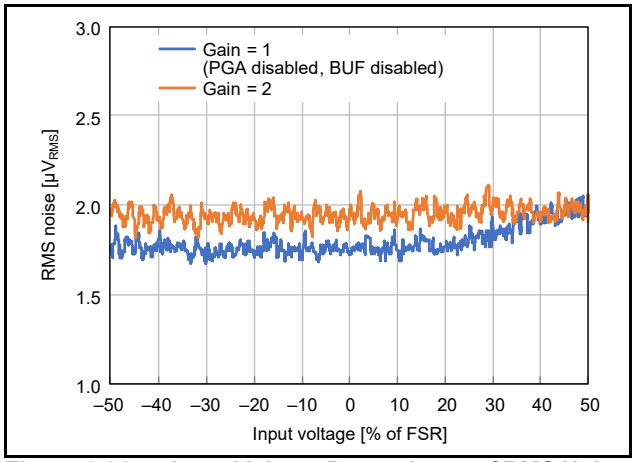


Figure 2.91 Input Voltage Dependence of RMS Noise (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, f_{DR} = 122 SPS, V_{REF} = 2.5V)

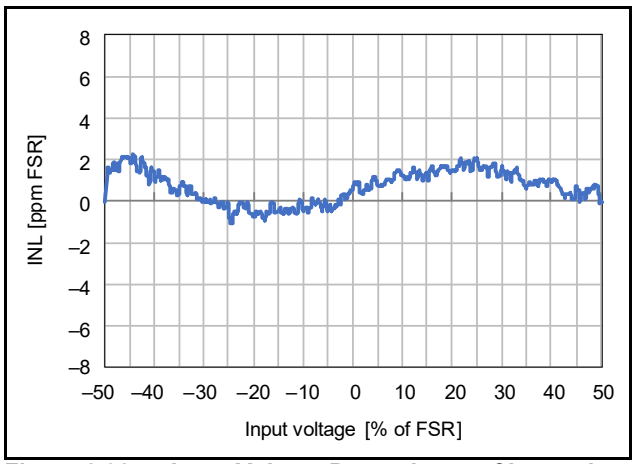


Figure 2.92 Input Voltage Dependence of Integral Non-Linearity (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 2, OPCR.DSADLVM bit = 0, V_{REF} = 2.5V)

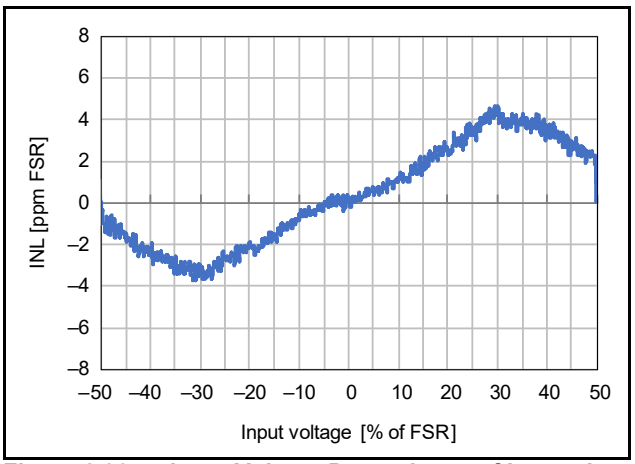


Figure 2.93 Input Voltage Dependence of Integral Non-Linearity (AVCC0 = 5.0 V, T_a = 25°C, Normal Mode, Gain = 1 (PGA disabled, BUF disabled), OPCR.DSADLVM bit = 0, V_{REF} = 2.5V)

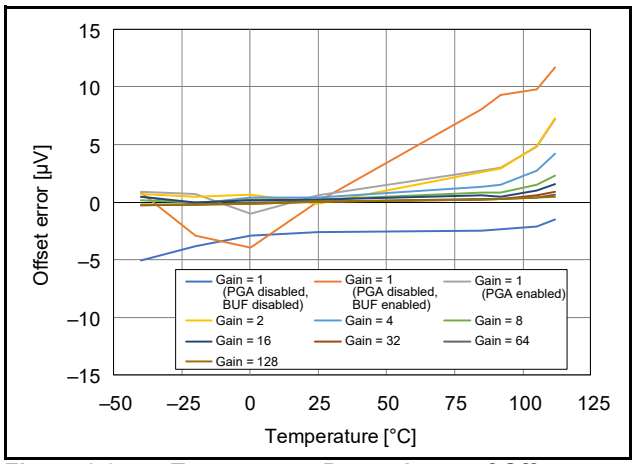


Figure 2.94 Temperature Dependence of Offset Error (AVCC0 = 5.0 V, V_{ID} = 0V, V_{REF} = 2.5V)

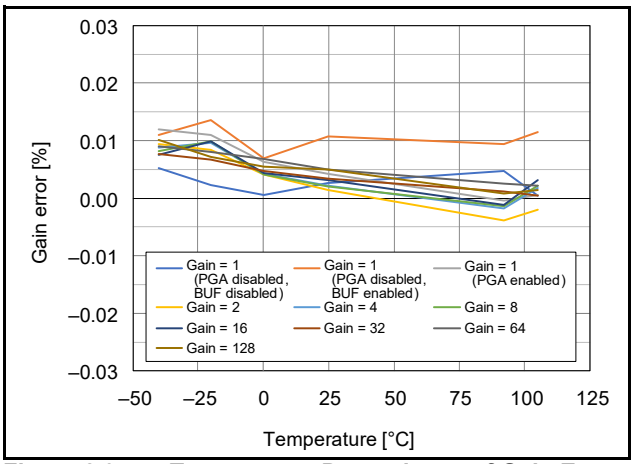


Figure 2.95 Temperature Dependence of Gain Error (AVCC0 = 5.0 V, OPCR.DSADLVM bit = 0, V_{REF} = 2.5V)

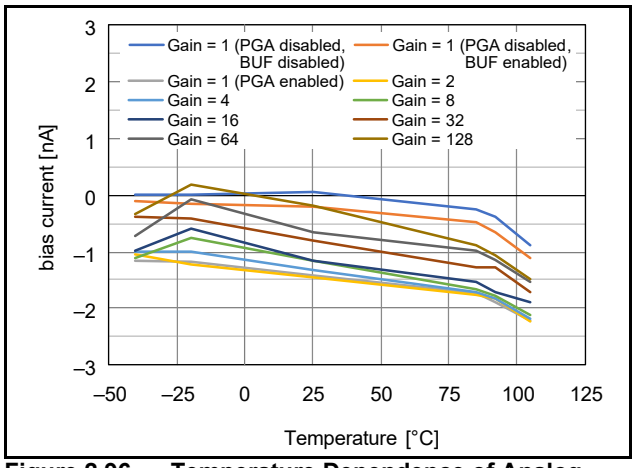


Figure 2.96 Temperature Dependence of Analog Input Bias Current (AVCC0 = 5.0 V)

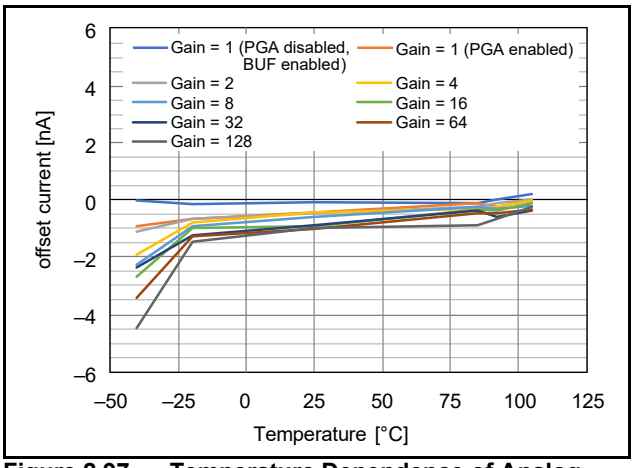


Figure 2.97 Temperature Dependence of Analog Input Offset Current (AVCC0 = 5.0 V)

2.10 Analog Front End Characteristics

Table 2.58 Voltage Reference Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage	V_{REFOUT}	—	2.5	—	V	Figure 2.98
Initial accuracy	—	—	±0.04	—	%	Figure 2.99 T_a = 25°C
Temperature drift	—	—	10	—	ppm/°C	T_a = –40 to +85°C
		—	10	—		T_a = –40 to +105°C
Load current	I_L	—	—	±10	mA	
Load regulation	—	—	–35	–50	µV/mA	Figure 2.100 I_L= 0 to +10 mA
		—	250	400		I_L = –10 to 0 mA
Power supply rejection ratio	PSRR	70	80	—	dB	DC

Table 2.59 Bias Voltage Generator Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage	V_{BIAS}	(AVCC0 + AVSS0)/2 – 0.02	(AVCC0 + AVSS0)/2	(AVCC0 + AVSS0)/2 + 0.02	V	
Startup time	t_{START}	—	—	20	µs/nF	

Table 2.60 Temperature Sensor Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Accuracy		—	—	—	±5	°C	Figure 2.101
Voltage sensitivity coefficient	Second-order	TC_{SNS}	—	$–6.2 \times 10^{–13}$	—	°C/LSB^2	
	First-order		—	$7.5 \times 10^{–5}$	—	°C/LSB	
Output code		—	—	3D4F50h (4018000)	—	—	

Table 2.61 Excitation Current Source Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output current	2 channels mode	IEXC	50, 100, 250, 500, 750, 1000			µA	Figure 2.102
	4 channels mode		50, 100, 250, 500				
Initial accuracy		—	—	±1	±5	%	Figure 2.103 T_a = 25°C
Temperature drift		—	—	25	60	ppm/°C	
Current matching		—	—	±0.2	±2.0	%	Figure 2.104, Figure 2.105 T_a = 25°C
Drift matching		—	—	5	30	ppm/°C	Matching between IEXC0 and IEXC1 Matching between IEXC2 and IEXC3
Line regulation		—	—	0.05	0.30	%/V	
Load regulation		—	—	0.1	0.5	%/V	
Compliance voltage		V_{COMP}	AVSS0 – 0.05	—	AVCC0 – 0.5	V	Figure 2.106 Output current error = –2.0%

Table 2.62 External Reference Input Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Differential input voltage range		V_{REF}	1	2.5	AVCC0	V	$V_{REF} = V_{(REFnP)} - V_{(REFnN)}$ (n = 0, 1)
Absolute input voltage range	Reference buffer disabled	$V_{(REF0P)}$, $V_{(REF1P)}$, $V_{(REF0N)}$, $V_{(REF1N)}$	AVSS0 – 0.05	—	AVCC0 + 0.05	V	
	Reference buffer enabled		AVSS0 + 0.1	—	AVCC0 – 0.1		
Input current	Reference buffer disabled	I_b	—	7	15	µA/V	Figure 2.107 T_a = 25°C
	Reference buffer enabled		—	±1	±3	nA	Figure 2.108 T_a = 25°C
Input current drift	Reference buffer disabled	dI_b	—	0.8	1.5	nA/V/°C	T_a = –40 to +105°C
	Reference buffer enabled		—	18	60	pA/°C	T_a = –40 to +85°C
			—	30	150	pA/°C	T_a = –40 to +105°C
Common mode rejection ratio	Reference buffer disabled	CMRR	70	90	—	dB	
	Reference buffer enabled		70	80	—		

Table 2.63 Low Side Switch Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
On-state resistance	R_{ON}	—	—	10	Ω	
Off-state leakage current	I_{lkg}	—	—	0.1	µA	
Allowable current	I_{LIMIT}	—	—	30	mA	

Table 2.64 Low Power-Supply Voltage Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage (LVDET0)	DET0LVL = 0	V_{DET0}	1.88	2.00	2.12	V	Negative-going AVCC0
	DET0LVL = 1		1.74	1.86	1.98		
Non-responsive period (LVDET0)		t_{DET0}	—	—	20	µs	
Detection voltage (LVDET1)	DET1LVL[1:0] = 00b	V_{DET1}	2.75	2.91	3.07	V	Negative-going AVCC0
	DET1LVL[1:0] = 01b		2.65	2.82	2.99		
	DET1LVL[1:0] = 10b		3.60	3.80	4.00		
	DET1LVL[1:0] = 11b		3.50	3.70	3.90		
Non-responsive period (LVDET1)		t_{DET1}	—	—	20	µs	

Table 2.65 Input Voltage Fault Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Upper detection level for the analog input voltage	V_{IDETH}	AVCC0 + 0.05	AVCC0 + 0.2	—	V	
Lower detection level for the analog input voltage	V_{IDETL}	—	AVSS0 – 0.2	AVSS0 – 0.05	V	
Non-responsive period	t_{IDET}	—	—	20	µs	

Table 2.66 Reference Voltage Fault Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection level for external reference voltage differential	V_{RDET}	0.70	0.85	1.00	V	
Upper detection level for the external reference voltage	V_{RDETH}	AVCC0 – 0.5	AVCC0 – 0.4	—	V	
Lower detection level for the external reference voltage	V_{RDETL}	—	AVSS0 + 0.4	AVSS0 + 0.5	V	
Non-responsive period	t_{RDET}	—	—	20	µs	

Table 2.67 Excitation Current Source Disconnect Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection level for disconnection of the excitation current source	$V_{IEXCDET}$	AVCC0 – 0.18	AVCC0 – 0.06	—	V	
Non-responsive period	$t_{IEXCDET}$	—	—	20	µs	

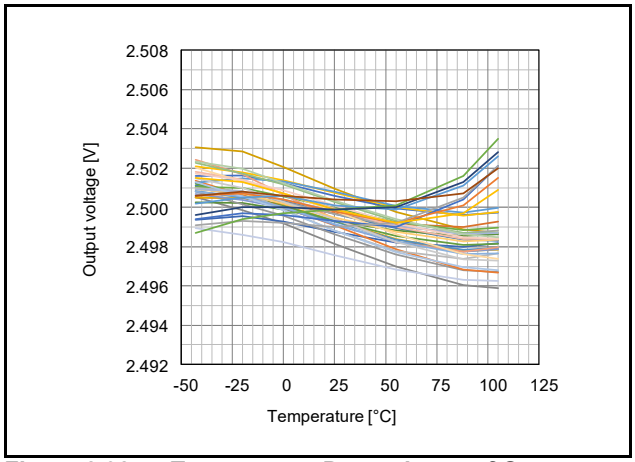


Figure 2.98 Temperature Dependence of Output Voltage of Voltage Reference (AVCC0 = 5.0 V)

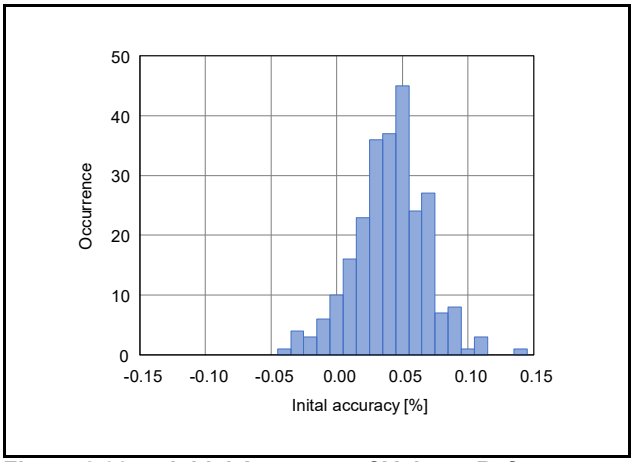


Figure 2.99 Initial Accuracy of Voltage Reference (AVCC0 = 5.0 V)

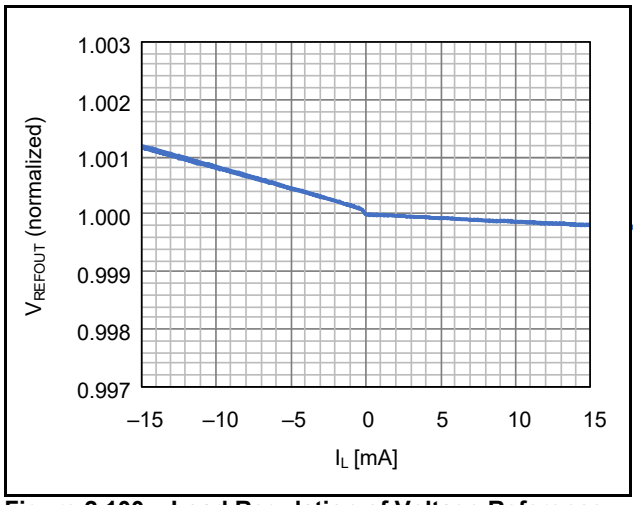


Figure 2.100 Load Regulation of Voltage Reference (AVCC0 = 5.0 V, T_a = 25°C)

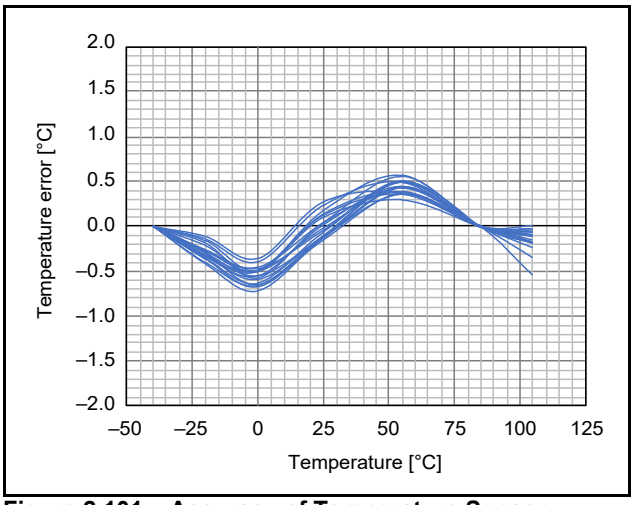


Figure 2.101 Accuracy of Temperature Sensor (AVCC0 = 5.0 V)

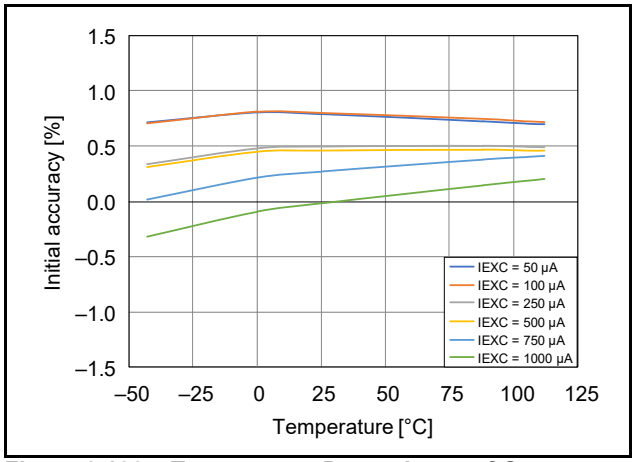


Figure 2.102 Temperature Dependence of Output Current of Excitation Current Source (AVCC0 = 5.0 V)

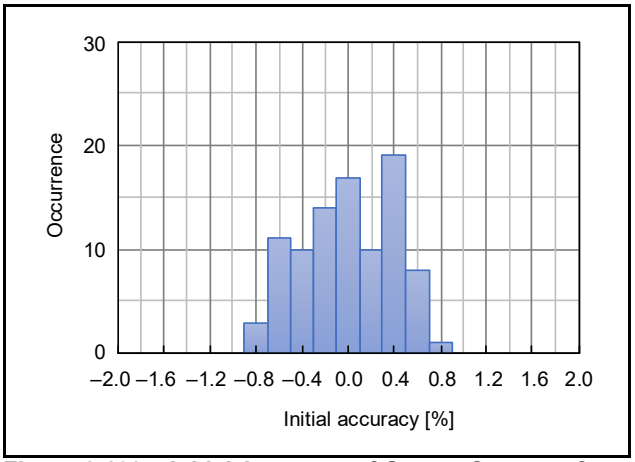


Figure 2.103 Initial Accuracy of Output Current of Excitation Current Source (AVCC0 = 5.0 V, T_a = 25°C, IEXC = 250 µA, 93 samples)

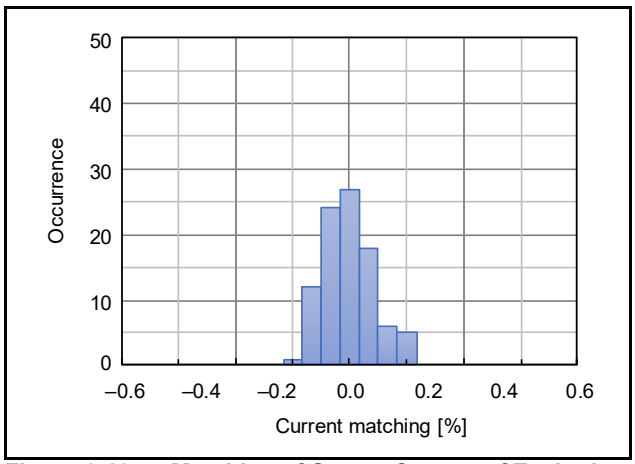


Figure 2.104 Matching of Output Current of Excitation Current Source (AVCC0 = 5.0 V, T_a = 25°C, IEXC = 250 µA, 93 samples)

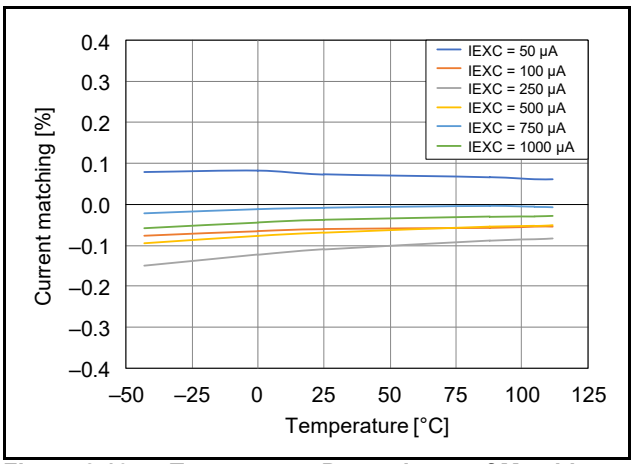


Figure 2.105 Temperature Dependence of Matching of Output Current of Excitation Current Source (AVCC0 = 5.0 V)

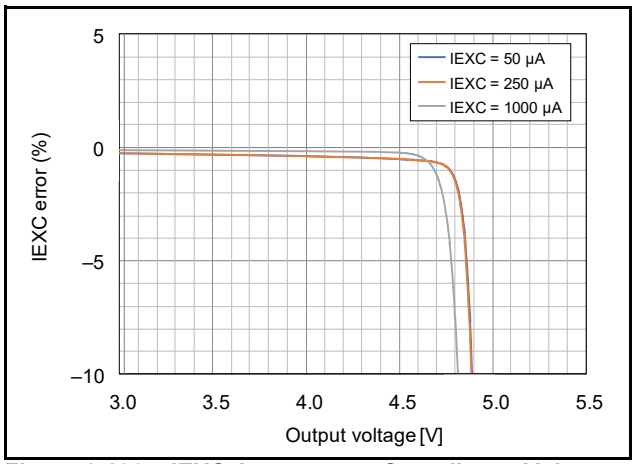


Figure 2.106 IEXC Accuracy vs Compliance Voltage (AVCC0 = 5.0 V, T_a = 25°C)

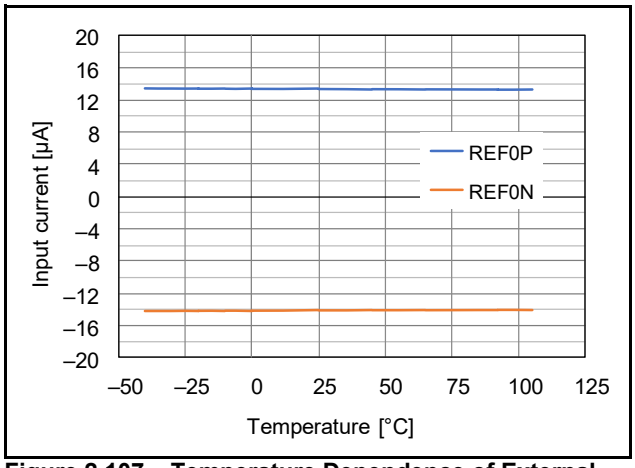


Figure 2.107 Temperature Dependence of External Reference Input Current (AVCC0 = 5.0 V, Reference Buffer Disabled)

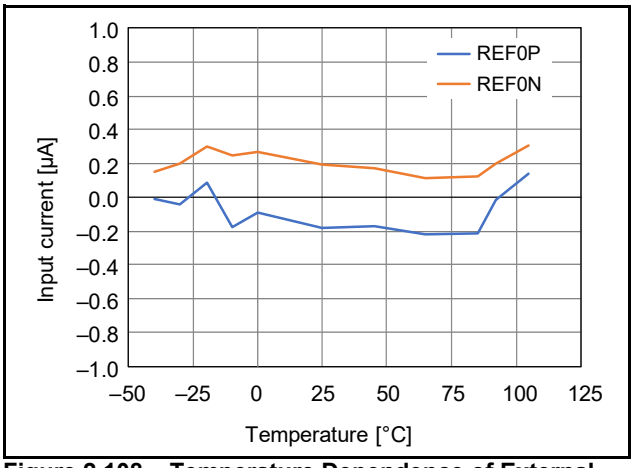


Figure 2.108 Temperature Dependence of External Reference Input Current (AVCC0 = 5.0 V, Reference Buffer Enabled)

2.11 12-Bit A/D Conversion Characteristics

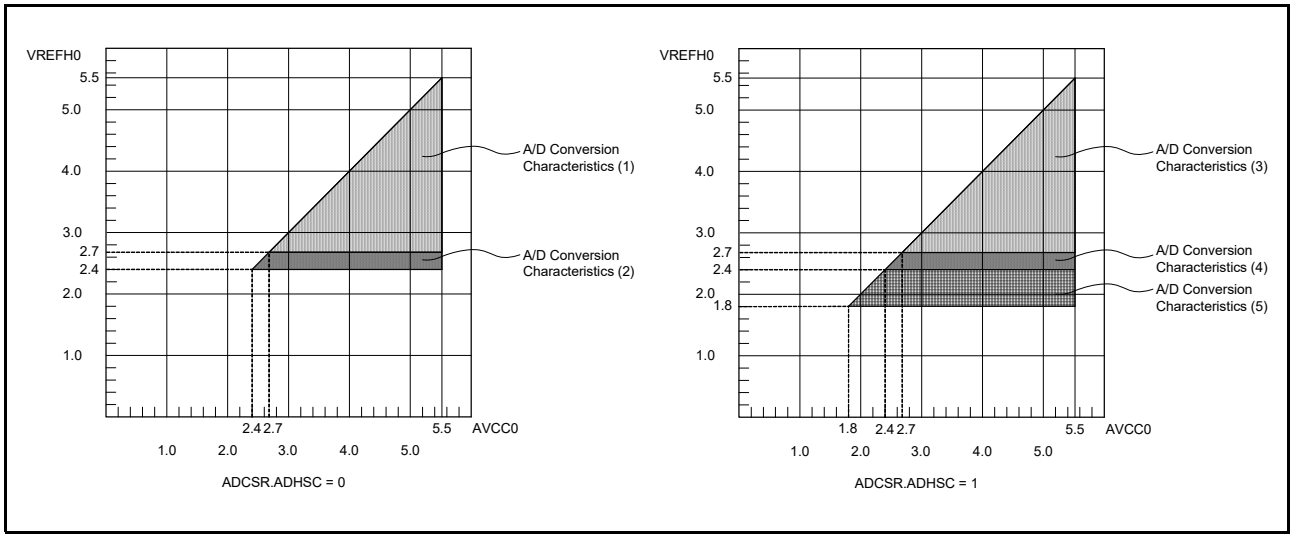


Figure 2.109 AVCC0 to VREFH0 Voltage Range

Table 2.68 12-Bit A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 0.3 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)		1.41	—	—	µs	ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
Analog input capacitance	Cs	—	—	25	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.69 12-Bit A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 1.3 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)		2.82	—	—	µs	ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
Analog input capacitance	Cs	—	—	25	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.70 12-Bit A/D Conversion Characteristics (3)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, Ta = –40 to +105°C, Source impedance = 1.1 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)		3	—	—	µs	ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	25	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.71 12-Bit A/D Conversion Characteristics (4)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, Ta = –40 to +105°C, Source impedance = 2.2 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)		5.06	—	—	µs	ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	25	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.72 12-Bit A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, 1.8 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, Ta = –40 to +105°C, Source impedance = 5 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)		10.13	—	—	µs	ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	25	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±3.00	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.73 12-Bit A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
Analog input channel	AN000 to AN005	AVCC0 = 1.8 to 5.5 V	

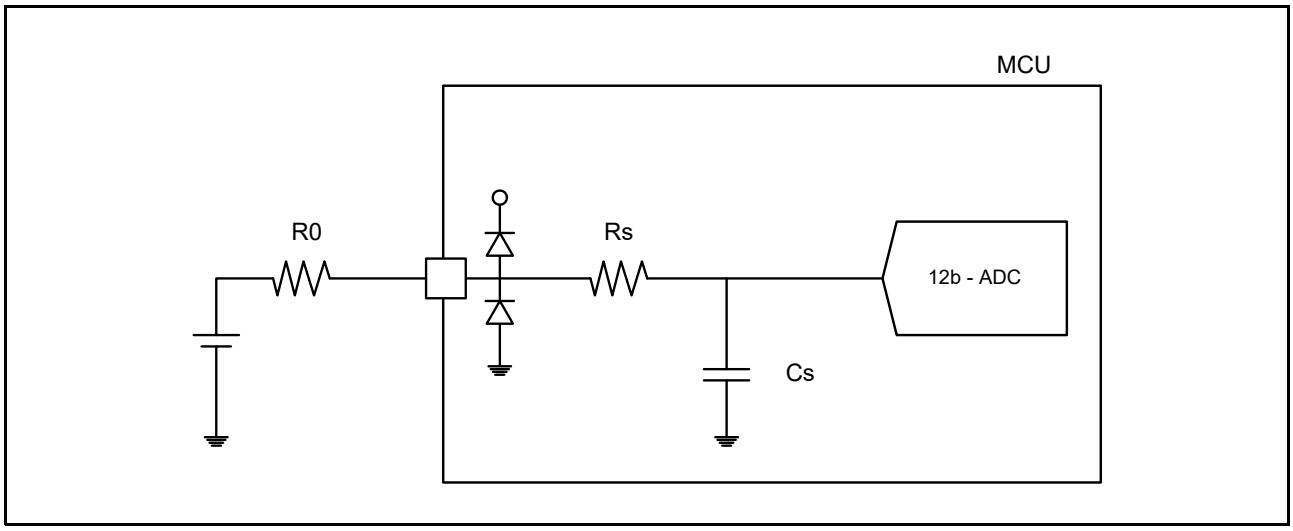


Figure 2.110 Equivalent Circuit

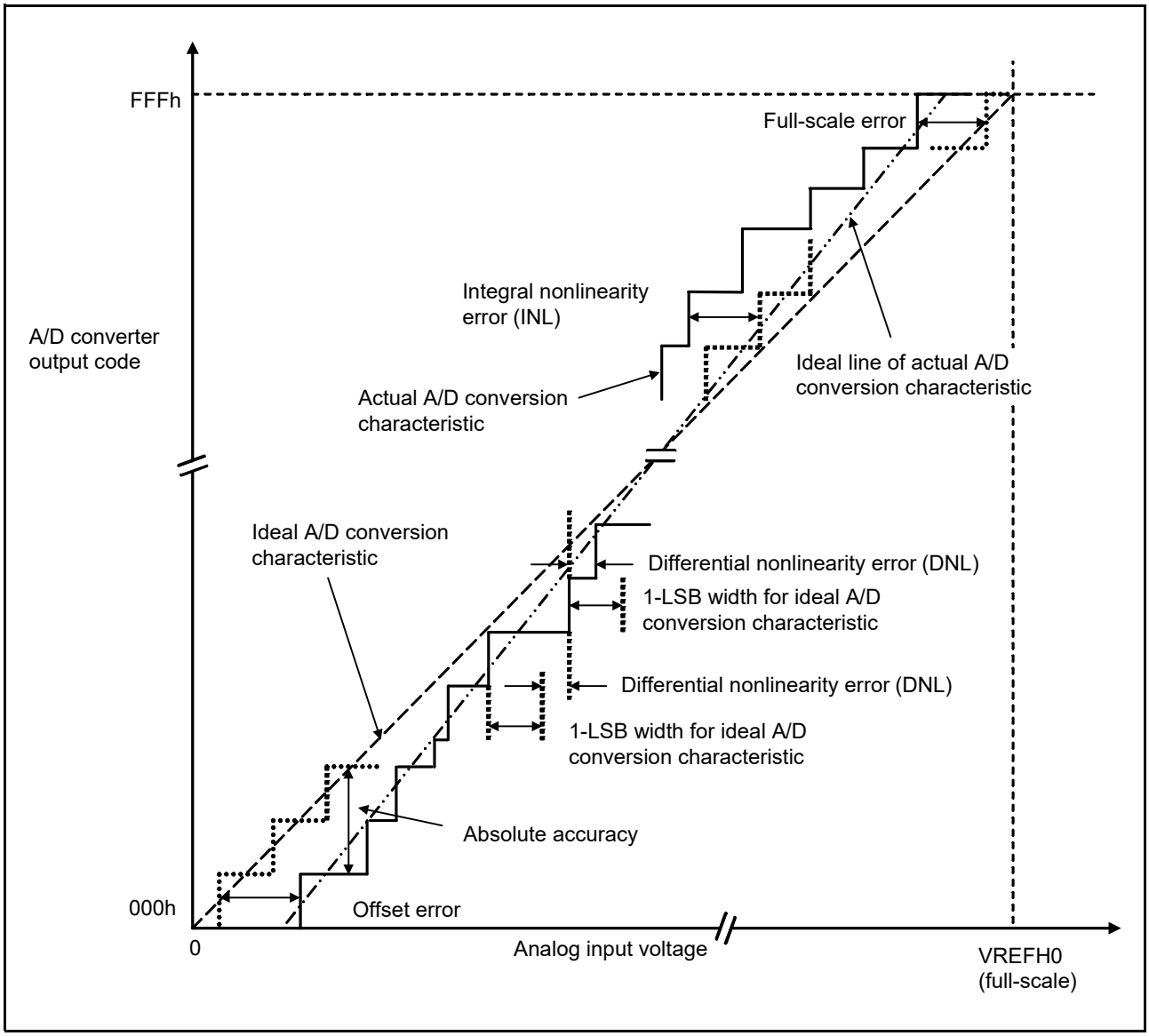


Figure 2.111 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

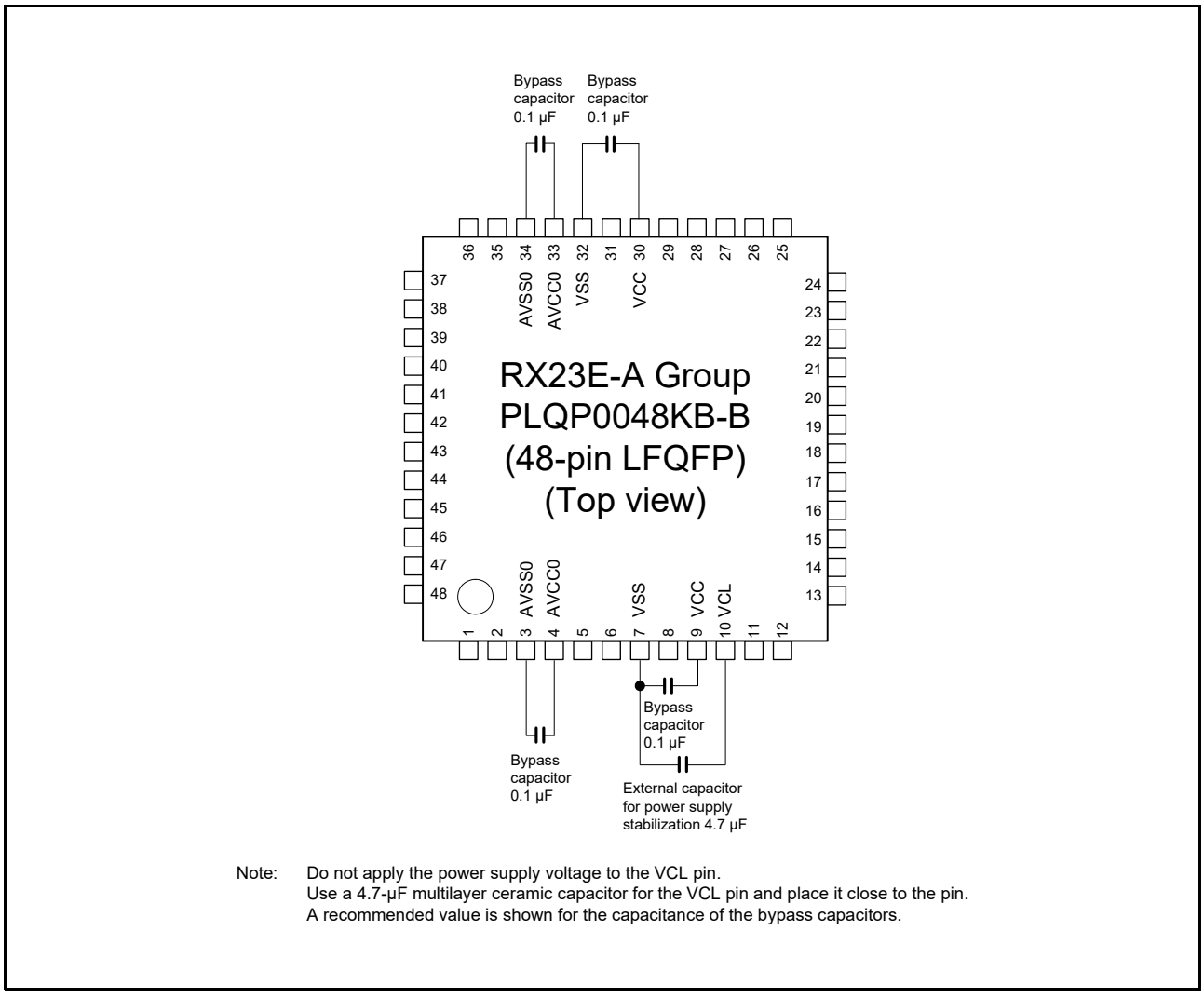
Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

2.12 Usage Notes

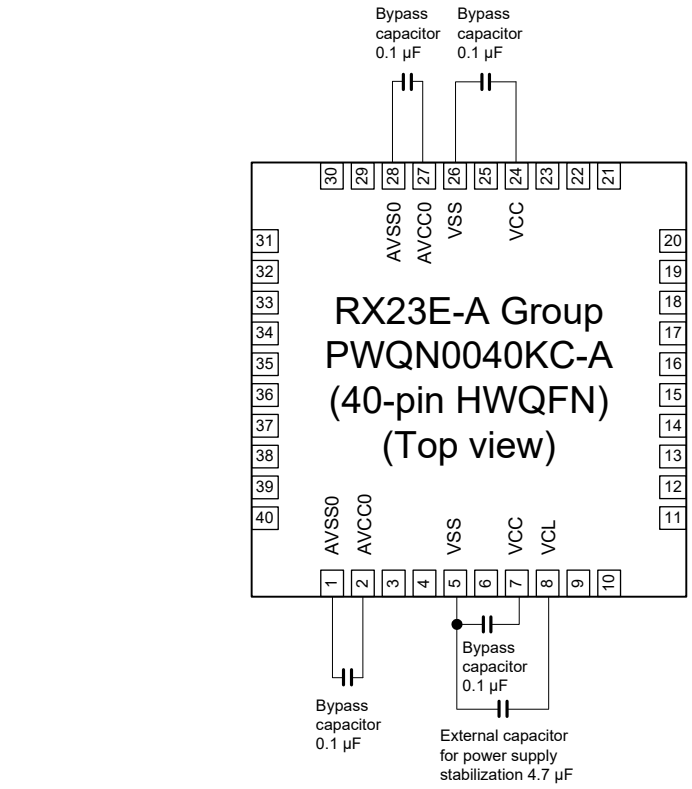
2.12.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Figure 2.112 and Figure 2.113 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.
Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 33, Analog Front End (AFE), and section 35, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.112 Connecting Capacitors (48 Pins)



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

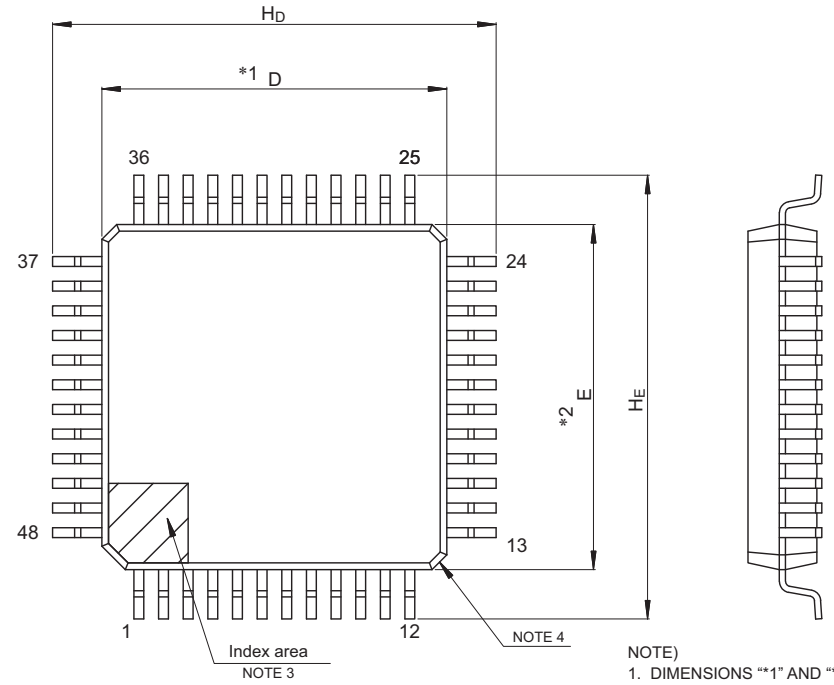
Figure 2.113 Connecting Capacitors (40 Pins)

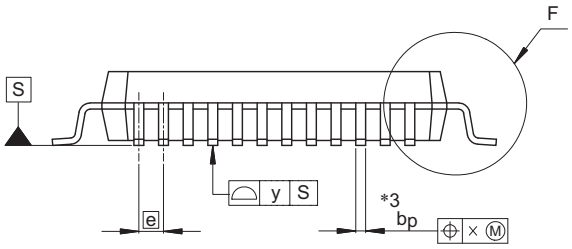
Appendix 1. Package Dimensions

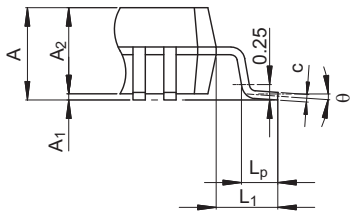
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







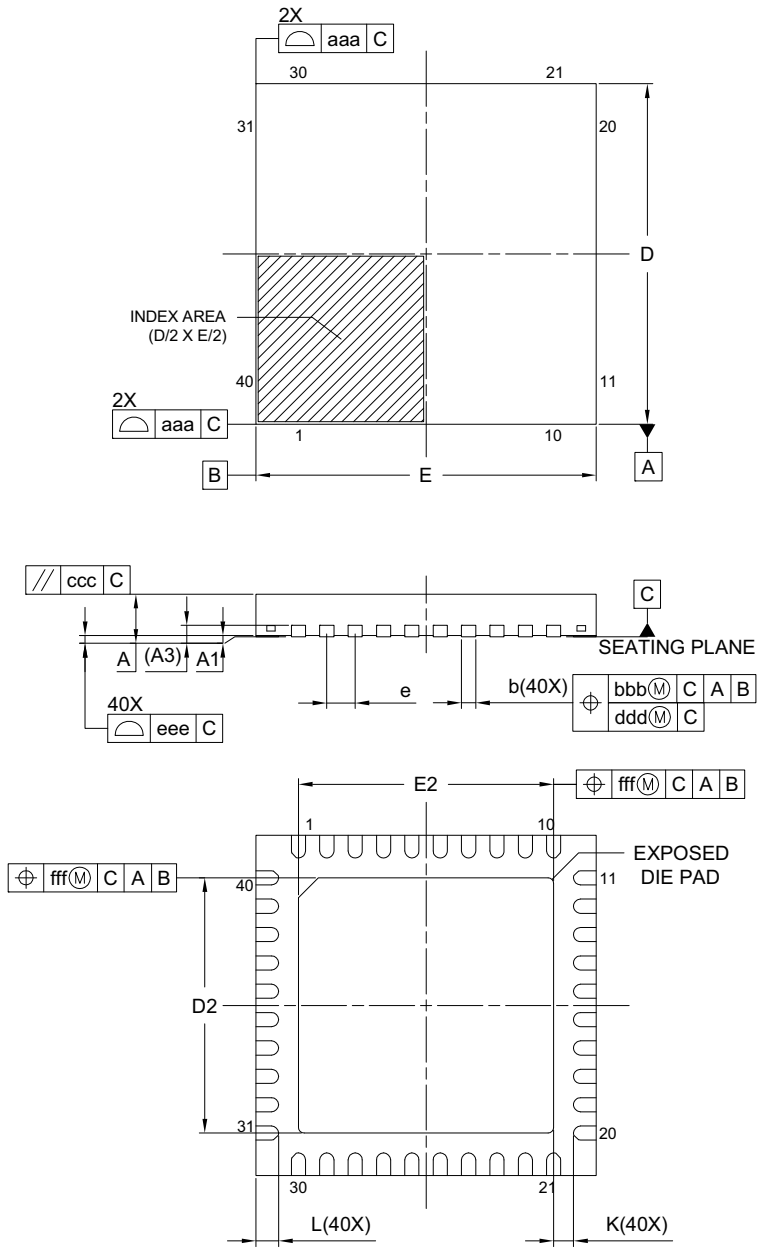
Detail F

NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 48-Pin LFQFP (PLQP0048KB-B)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	4.45	4.50	4.55
E_2	4.45	4.50	4.55
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure B 40-Pin HWQFN (PWQN0040KD-A)

REVISION HISTORY	RX23E-A Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 30, 2019	—	First edition, issued	
1.10	Oct 09, 2020	1. Overview		
		7	Table 1.3 List of Products, changed	TN-RX*-A0253A/E
		8	Figure 1.1 How to Read the Product Part Number, changed	
		2. Electrical Characteristics		
		51 to 63	2.4.5 Timing of On-Chip Peripheral Modules, Layout changed	
1.20	Apr 20, 2022	Features		
		1	Package type, changed	
		1	Analog functions, changed	TN-RX*-A0255A/E
		1. Overview		
		5	Table 1.1 Outline of Specifications (4/4), changed	
		7	Table 1.3 List of Products, changed	
		2. Electrical Characteristics		
		82	Table 2.58 Voltage Reference Characteristics, changed	TN-RX*-A0255A/E
		85	Figure 2.98 Temperature Dependence of Output Voltage of Voltage Reference (AVCC0 = 5.0 V), changed	
		85	Figure 2.99 Initial Accuracy of Voltage Reference (AVCC0 = 5.0 V), changed	
		Appendix 1. Package Dimensions		
		—	Figure B 40-Pin HWQFN (PWQN0040KC-A), deleted	
1.30	Dec 25, 2024	1. Overview		
		10	Figure 1.3 Analog Block Diagram, added	
		2. Electrical Characteristics		
		20	Table 2.2 Recommended Operating Conditions (1), changed	
		20	Table 2.3 Recommended Operating Conditions (2), changed	TN-RX*-A0269A/E
		35	Table 2.21 Thermal Resistance Value (Reference), changed	
		57	Table 2.38 Timing of RIIC, changed	
		59	Figure 2.61 RIIC Bus Interface Input/Output Timing and Simple I^2C Bus Interface Input/Output Timing, changed	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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