# RZ/A2M Group

## Features

This LSI has following features.

### ■ CPU (Arm® Cortex®-A9)

- Operating frequency: 528 MHz
- Single-precision/double-precision FPU
- Arm® NEON™

### ■ On-chip memory

- 4 MB

### ■ Main graphics and camera input functions

- Video display controller (VDC6): 1 channel
  - LCD output: Max. WXGA
  - Screen superimposition: 3 layers
  - Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- MIPI-CSI2 interface: 1 channel
- Distortion compensation unit (IMR): 1 channel
- 2D graphics engine: 1 channel
- Sprite engine: 1 channel
- JPEG coding engine: 1 channel

### ■ Main memory interface functions

- NOR flash, SDRAM, NAND flash
- Serial flash: 1-bit/4-bit/8-bit: 1 channel, 8-bit: 1 channel (ability to run stored programs directly)
- SD/MMC host interface: 2 channels

### ■ Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 2 channels
- SCIF: 5 channels
- I2C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN-FD: 2 channels

### ■ Optional functions

- DRP (Dynamically Reconfigurable Processor)

# 1.    Overview

## 1.1    Outline of Specification

Table 1.1        Features of RZ/A2M

| Items | Specification |
|---|---|
| CPU | • Arm Cortex-A9 processor<br>• Maximum operating frequency: 528 MHz<br>• Instruction cache size: 32 Kbytes<br>• Data cache size: 32 Kbytes (write-back algorithm)<br>• TLB entries: 128 entries<br>• Jazelle® architecture extension: Full implementation<br>• Media processing engine with NEON™ technology |
| Boot modes | • Eight boot modes<br>  Boot mode 0: Booting from memory (bus width: 16 bits) connected to the CS0 space<br>    Note: This only applies to 324-pin products.<br>  Boot mode 1: Booting from a NAND flash memory with SD controller<br>  Boot mode 2: Booting from a NAND flash memory with MMC controller (data bus width: 8 bits)<br>  Boot mode 3: Booting from a serial flash memory (3.3 V) connected to the SPI multi I/O bus space<br>  Boot mode 4: Booting from an Octal-SPI flash memory connected to the SPI multi I/O bus space<br>  Boot mode 5: Booting from a HyperFlash connected to the SPI multi I/O bus space<br>  Boot mode 6: Booting from an OctaFlash connected to the OctaFlash space<br>  Boot mode 7: Booting from a HyperFlash connected to the HyperFlash space |
| Secondary cache | • Arm CoreLink™ Level 2 Cache Controller L2C-310<br>• Operating frequency: 132 MHz<br>• Cache size: 128 Kbytes |
| Clock pulse generator | • Clock mode: Input clock can be selected from external input (EXTAL) or crystal resonator.<br>• Input clock can be multiplied by 44 (max.) by the internal PLL circuit.<br>• Peak values of EMI noise can be reduced by the on-chip SSCG circuit.<br>• Five types of clocks generated:<br>    —CPU clock (Iφ): Maximum 528 MHz<br>    —Image processing clock (Gφ): Maximum 264 MHz<br>    —Internal bus clock (Bφ): Maximum 132 MHz<br>    —Peripheral clock 1 (P1φ): Maximum 66 MHz<br>    —Peripheral clock 0 (P0φ): Maximum 33 MHz |
| Interrupt controller | • Arm CoreLink™ Generic Interrupt Controller (GIC-400)<br>• External interrupt pins (NMI, IRQ7 to IRQ0, and TINT31 to TINT0)<br>• On-chip peripheral interrupts: Priority level set for each module<br>• 32 priority levels available |
| Bus state controller<br>[Only for 324-pin products] | • Address space divided into six areas (0 to 5), each a maximum of 64 Mbytes<br>• The following features settable for each area independently<br>    —Bus size (8 or 16 bits): Available sizes depend on the area.<br>    —Number of access wait cycles (different wait cycles can be specified for read and write access<br>      cycles in some areas)<br>    —Idle wait cycle insertion (between the same area access cycles or different area access cycles)<br>    —Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM<br>      with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The<br>      address/data multiplexed I/O (MPX) interface is also available.<br>• Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing<br>  can be selected by software)<br>• SDRAM refresh<br>  Auto refresh or self refresh mode selectable<br>• SDRAM burst access |
| Direct memory access controller | • Two modules, sixteen channels; external requests are available for one channel.<br>• Can be activated by on-chip peripheral modules.<br>• A specific DMA transfer interval can be specified to adjust the bus occupancy.<br>• Link mode (DMA transfer under descriptor control) supported<br>• Transfer information can be automatically reloaded. |

Table 1.1      Features of RZ/A2M

| Items | Specification |
|---|---|
| Multi-function timer pulse unit 3 | • 9 channels (16 bits × 8 channels, 32 bits × 1 channel)<br>• Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs<br>• 14 types of count clocks (P1φ/1, P1φ/2, P1φ/4, P1φ/8, P1φ/16, P1φ/32, P1φ/64, P1φ/256, P1φ/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) selectable<br>  —14 types of count clocks selectable (channel 0)<br>  —12 types of count clocks selectable (channel 2)<br>  —11 types of count clocks selectable (channels 1, 3, 4, 6, 7, and 8)<br>  —10 types of count clocks selectable (channel 5)<br>• Input capture function<br>• 39 output compare and input capture registers<br>• Counter clear operation ( Simultaneous counter clearing by Compare match or Input capture is available. )<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Synchronous input/output of each register due to synchronous operation of the counter.<br>• Buffered operation<br>• Cascade-connected operation<br>• 43 types of interrupt sources<br>• Automatic transfer of register data<br>• Pulse output modes<br>  Toggle, PWM, complementary PWM, and reset-synchronized PWM modes<br>• Synchronization of multiple counters<br>• Complementary PWM output mode<br>  —Non-overlapping waveforms output for 3-phase inverter control<br>  —Automatic dead time setting<br>  —0% to 100% PWM duty value specifiable<br>  —A/D converter start request delaying function<br>  —Interrupt skipping at crest or trough<br>• Reset-synchronized PWM mode<br>  Three-phase PWM waveforms in positive and negative phases can be output with a required duty value.<br>• Phase counting mode: 16-bit mode (channels 1 and 2) / 32-bit mode (channels 1 and 2)<br>• Counter function of dead time compensation<br>• Conversion start trigger of A/D converter can be generated.<br>• Conversion start trigger of A/D converter can be skipped.<br>• Digital filter functions for the input capture and external count clock pin. |
| Port output enable 3 | • Control of the high-impedance state of the MTU3a waveform output pins<br>• Activation with four input pins<br>• Activation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level)<br>• Activation by register write<br>• Additional programming of output control target pins is possible. |
| General PWM timer | • 32 bits × 8 channels<br>• Counting up or down (sawtooth wave), counting up and down (triangular wave) selectable for all channels.<br>• Independent selectable for each channel.<br>• 2 input/output pins per channel<br>• 2 output compare/input capture registers per channel<br>• For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use.<br>• In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms.<br>• Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow)<br>• Generation of dead times in PWM operation<br>• Synchronous start / stop / clear of counters on arbitrary channels.<br>• Starting, stopping, and clearing up/down counters in response to a maximum of eight events<br>• Starting, stopping, and clearing up/down counters in response to input level comparison<br>• Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers<br>• Output pin invalidation functions due to dead time error or detection of short circuit between output pins.<br>• Generation of triggers for A/D converter conversion<br>• Digital filter functions for the input capture and external trigger pins |

Table 1.1          Features of RZ/A2M

| Items | Specification |
|---|---|
| Port output enable for GPT | • Output prohibition control of the GPT waveform output pin<br>• Activation with up to four input pins<br>• Activation by dead time error detection or output short detection<br>• Activation by register write |
| OS timer | • Three-channel 32-bit counters<br>• Two operating modes:<br>    —Interval timer mode<br>    —Free-running comparison mode<br>• DMA transfer request or interrupt request can be issued when a compare match occurs. |
| Watchdog timer | • On-chip one-channel watchdog timer<br>• A counter overflow can reset the LSI.<br>• CPU parity error can reset the LSI. |
| Realtime clock | • Internal clock, Two types of count mode, alarm function<br>• Interrupts can be generated at intervals of 1/64 s by the on-chip 32.768-kHz oscillator. |
| Serial communications interface with FIFO | • Five channels<br>• Clock synchronous mode or asynchronous mode selectable<br>• Simultaneous transmission and reception (full-duplex communication) supported<br>• Dedicated baud rate generator<br>• Separate 16-byte FIFO registers for transmission and reception<br>• Modem control function (channels 0, 1, and 2 in asynchronous mode) |
| Serial communications interface | • Two channels<br>• Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable.<br>• Simultaneous transmission and reception (full-duplex communication) supported<br>• Dedicated baud rate generator<br>• LSB first/MSB first selectable<br>• Modem control function<br>• Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0) |
| Renesas serial peripheral interface | • Three channels<br>• SPI operation<br>• Master mode and slave mode selectable<br>• Programmable bit length, clock polarity, and clock phase can be selected.<br>• Consecutive transfers<br>• MSB first/LSB first selectable<br>• Maximum transfer rate: 33.00 Mbps |
| SPI multi I/O bus controller | • One channel<br>• Up to two serial flash memories with multiple I/O bus sizes (single/quad) can be connected.<br>• Connectable with one Octal-SPI flash memory.<br>• Connectable with one HyperFlash™ memory.<br>• External address space read mode (built-in read cache)<br>• SPI operating mode<br>• Maximum frequency: 132 MHz (QSPI0_SPCLK) |
| HyperBus controller | • Two channels<br>• Support HyperBus interface<br>• One HyperFlash and HyperRAM can be connected per channel.<br>• Maximum frequency: 132 MHz (HM_CK, HM_CK#) |
| Octa memory controller | • Two channels<br>• Support Macronix Serial Multi I/O (MXSMIO®) Octa Peripheral Interface (OPI) interface.<br>• One OctaFlash and OctaRAM can be connected per channel.<br>• Support memory-map read/write feature with independent Flash/RAM address space.<br>• OctaFlash supports STR (Single Transfer Rate) mode and DTR (Double Transfer Rate) mode.<br>• SPI operation<br>• Support Read-While-Write (RWW) function<br>• Maximum frequency: 132 MHz (OM_SCLK) |
| I2C bus interface | • Four channels<br>• Master mode and slave mode supported<br>• Support for 7-bit and 10-bit slave address formats<br>• Support for multi-master operation<br>• Timeout detection |

Table 1.1 Features of RZ/A2M

| Items | Specification |
|---|---|
| Serial sound interface | • Four-channel bidirectional serial transfer<br>• Duplex communication (channels 0, 1, and 3)<br>• Support of I$^2$S, Monaural, and TDM audio formats<br>• Support of master and slave functions<br>• Generation of programmable word clock and bit clock<br>• Multi-channel formats<br>• Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats<br>• Support of 32-stage FIFO for transmission and reception<br>• Support of LR-clock continue function in which the LR-clock signal is not stopped. |
| CANFD interface | • Two channels<br>• ISO11898-1 (2003) compliant<br>• CAN-FD ISO 11898-1 (2015) compliant<br>• Message buffer:<br>　—Up to 64 × 2-channel receive message buffers: shared among all channels.<br>　—16 transmit message buffers per channel |
| Renesas SPDIF interface | • Support of IEC60958 standard (stereo and consumer use modes only)<br>• Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz<br>• Audio word sizes of 16 to 24 bits per sample<br>• Biphase mark encoding<br>• Double buffered data<br>• Parity encoded serial data |
| Ethernet MAC controller | • 176-pin products: 1 channel when the media independent interface (MII) is in use, 2 channels when the reduced media independent interface (RMII) is in use<br>256-, 272-, or 324-pin products: 2 channels whether the MII or RMII is in use<br>• Conforms with the Ethernet / IEEE802.3 MAC (Media Access Control) layer standard<br>• Supports transfer at 10 and 100 Mbps<br>• Supports full-duplex and half-duplex mode<br>• Supports Media Independent Interface (MII) compliant with the IEEE802.3u standard and Reduced Media Independent Interface (RMII)<br>• Magic Packet$^{TM}$* detection and Wake-On-LAN (WOL) signal output<br>• Built-in PTP controller (EPTPC) for Ethernet controller that uses Time Precision Time Protocol (PTP) defined by IEEE 1588-2008 (Version 2.0) to synchronize time between devices.<br>• E-DMAC (Direct Memory Access Controller for Ethernet controller) function<br>Note: * Magic Packet is a trademark of Advanced Micro Devices, Inc. |
| A/D converter | • 12-bit resolution<br>• Eight input channels<br>• Minimum conversion time: 1 μs per channel<br>• A/D conversion request by the external trigger or timer trigger |
| NAND flash controller | • Direct-connected memory interface with NAND-type flash memory<br>• ONFI 1.0 (mode 1 to 2)<br>• ECC: 2, 4, 8, 16, 24, and 32 bits<br>• Supports flash memory requiring Large block (2048+64)<br>• Supports flash memory requiring 5-byte addresses (2 Gbits and more)<br>• Interrupt request<br>• Two types of DMA mode |
| USB 2.0 host/function module | • Two channels<br>• USB 2.0-compliant host/function module<br>• 480-Mbps, 12-Mbps, and 1.5-Mbps transfer rates provided (host mode)<br>• 480-Mbps and 12-Mbps transfer rates provided (function mode)<br>• On-chip 1-Kbyte RAM as communication buffers (host mode)<br>• On-chip 8-Kbyte RAM as communication buffers (function mode) |

Table 1.1    Features of RZ/A2M

| Items | Specification |
|---|---|
| Video display controller 6 | • Video input interface: <br> BT601, BT656 format (NTSC/PAL) input: Input clock: 27 MHz/54 MHz <br> Digital pin input (channel 0): <br> YCbCr422, YCbCr444, RGB888, RGB666, RGB565 <br> Digital pin input size: <br> Maximum input video image size to be set*: 1920 pixels × 1080 lines (horizontal × vertical) <br> Note: * Depends on the AC characteristics of the connected device. <br> Examples of input video image size: <br>   XGA (1024 × 768) <br>   SVGA (800 × 600), <br>   WVGA (800 × 480), <br>   VGA (640 × 480), <br>   WQVGA (480 × 240), <br>   QVGA (320 × 240, 240 × 320) <br> • Input video control <br> Horizontal noise reduction (NR), brightness adjustment and contrast adjustment using matrix operation <br> • Scaling control <br> Vertical and horizontal scaling up or down of input video possible at a desired ratio (scaling up of graphics also possible) <br> Scaling up ratio: 1 to 8; scaling down ratio: 1/8 to 1 <br> Interpolation: Hold or linear selectable <br> 2D IP conversion: 2D IP conversion through separately setting the initial phases <br>                 for the top and bottom fields <br> • Video recording <br> Output pixel format: YCbCr444, YCbCr422, RGB888, RGB565 <br> Output field rate: 1/1, 1/2, 1/4, 1/8 <br> Rotation: Horizontal mirroring and 90/180/270 degree rotation for YCbCr422 and RGB565 <br> Maximum video image size to be stored: ×1 size of input video image <br> • Output video control <br> Black stretch: Black area stretched according to Y signal state <br> Enhancer capability: LTI (transient improvement) and sharpness (contour emphasis) for Y signal <br><br> • Three graphics layers (one of them also for input video) <br>   Available input pixel formats <br>   1 bit/pixel: CLUT1 <br>   4 bits/pixel: CLUT4 <br>   8 bits/pixel: CLUT8 <br>   16 bits/pixel: YCbCr422 (graphics layers 0), RGB565, ARGB1555, RGBA5551, ARGB4444 <br>   32 bits/pixel: ARGB8888, RGBA8888, RGB888, YCbCr444 (graphics layers 0) <br> • Superimposition <br>   Alpha blending in a rectangular area: <br>     Input video, layer 1, and layer 2 blended according to the transparency percentage α <br>     (fade-in and fade-out function available) <br>   Chroma key function: <br>     Mixing based on transparency percentage α using the specified RGB and CLUT value <br>   Pixel-base alpha blending: <br>     Alpha blending for each pixel based on transparency percentage α <br><br> • Panel output control <br>   Panel output correction: <br>     Brightness adjustment and contrast adjustment, gamma correction, panel dithering <br>   TCON: <br>     Various timing output for LCD panel driving provided by a total of seven vertical and horizontal <br>     panel driver signals <br>   Panel output pixel format: RGB888, RGB666, RGB565, serial RGB <br>   Output video image size: <br>   Maximum output video image size to be set*: <br>     1999 pixels × 2035 lines (horizontal × vertical) <br>   Note: * Depends on the AC characteristics of the display panel. <br>   Examples of output video image size: <br>     XGA (1024 × 768) <br>     SVGA (800 × 600), <br>     WVGA (800 × 480), <br>     VGA (640 × 480), <br>     WQVGA (480 × 240), <br>     QVGA (320 × 240, 240 × 320) |

Table 1.1        Features of RZ/A2M

| Items | Specification |
|---|---|
| LVDS output interface | • Four pairs of differential output conforming to the TIA/EIA-644 standard (three pairs for data and one pair for the clock)<br>• When the LVDS output interface is not used, the LVDS pins can be used as CMOS input/output.<br>• The LVDS PLL generates clocks of various frequencies.<br>• LVDS Power-down function |
| Image renderer (IMR-LS2) | • One channel<br>• Refers to the video captured data as two-dimensional texture data and draws a shape by performing texture mapping for an arbitrary shape divided into triangular objects.<br>• Display list system<br>• Drawing functions<br>Texture mapping, bilinear filtering, automatic coordinate generation (and relative coordinate input)<br>• Instruction system<br>Draw instruction: TRI for drawing a triangle<br>Control instructions: TRAP, INT, NOP, SYNCM, SYNCW, WTL, and WTS<br>• Drawing space<br>Destination coordinates: $0 \leq X \leq 2{,}047$, $0 \leq Y \leq 2{,}047$<br>• Source coordinates: $0 \leq u \leq 1{,}439$, $0 \leq v \leq 1{,}023$ |
| 2D drawing engine (DRW) | • Support almost any object geometry, rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or anti-aliased.<br>• Color Formats<br>Frame buffer formats<br>8-bit: a (8)<br>16-bit: RGB (565), aRGB (4444), aRGB (1555)<br>32-bit: aRGB (8888).<br>Texture formats<br>1-bit: CLUT (1)/I (1)<br>2-bit: CLUT (2)/I (2)<br>4-bit: CLUT (4)/I (4)<br>8-bit: a (8), CLUT (8)/I (8), aCLUT (44)<br>16-bit: aRGB (4444), aRGB (1555), RGB (565)<br>24-bit: RGB (888) (run length encoded (RLE) unit)<br>32-bit: aRGB (8888).<br>CLUT formats use a 256-entry color lookup table. |
| Sprite engine (SPEA) | • RLE Unit<br>Supports Targa RLE data packet formats<br>• Sprite Unit<br>Two channels<br>Up to 16 separate sprites processed by each channel |
| JPEG codec unit | • Compression and decompression method conforming to the JPEG baseline standard within the range described in this document.<br>• Operational precision: Conforming to JPEG Part 2, ISO-IEC10918-2<br>• Pixel format:<br>Compression: YCbCr422<br>Decompression: YCbCr444, YCbCr422, YCbCr411, YCbCr420<br>Output pixel format to the buffer: YCbCr422, ARGB8888, RGB565<br>• Four quantization tables provided<br>• Four Huffman tables provided (two tables for AC coefficients and two tables for DC coefficients)<br>• Markers supported: SOI, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI<br>• Image data rate: Max. 132 Mbytes/s (at 66-MHz operation) |

Table 1.1          Features of RZ/A2M

| Items | Specification |
|---|---|
| Capture engine unit | • Examples of input video image size :<br>　　5 megapixels (2,560 × 1,920)<br>　　3 megapixels (2,048 × 1,536)<br>　　2 megapixels (1,632 × 1,224)<br>　　UXGA (1,600 × 1,200)<br>　　SXGA (1) (1,280 × 1,024)<br>　　SXGA (2) (1,280 × 960)<br>　　WXGA (1,280 × 768)<br>　　XGA (1,024 × 768)<br>　　SVGA (800 × 600)<br>　　WVGA (800 × 480)<br>　　VGA (640 × 480)<br>　　WQVGA (480 × 240)<br>　　QVGA (320 × 240, 240 × 320)<br>　　Note: Depends on the AC characteristics of the connected device, frame rate of the connected<br>　　　　　device, and transfer speed to the destination RAM.<br>• Input format: 8- or 16-bit binary data<br>• Memory output format: YCbCr422, YCbCr420<br>　Note: The captured data cannot be displayed via the video display controller 6 because the Y data<br>　　　　and CbCr data are split when written to memory. |
| MIPI CSI-2 interface<br>[Only for 256-, 272-, or 324-pin products] | • Up to 1.0-Gbps transfer rate of MIPI CSI-2<br>• ECC 1-bit error correction and 2-bit or more error detection of a packet header<br>• CRC error detection of a payload data part<br>• Generation of VD (vertical sync), HD (horizontal sync), and FLD (field) signals<br>• Lane swapping |
| Video input module | • Input formats<br>　MIPI CSI2 interface: YCbCr422, RGB888, RAW8<br>　Up to 2048 × 2048 pixels capture area<br>• Memory output data formats<br>　YCbCr422, RGB565, ARGB1555, RGB888, ARGB8888 |
| SD/MMC host interface | • 176-pin products: 1 channel<br>　256-, 272-, or 324-pin products: 2 channels<br>• SD memory I/O card interface (1-/4-bit SD bus)<br>• SD, SDHC, and SDXC SD memory card access supported<br>• Default, high-speed, UHS-I/SDR50, DDR50, and SDR104 transfer modes supported<br>• Error check function: CRC7 (command), CRC16 (data)<br>• Interrupt request: 2<br>• Card detection function, write protect supported<br>• MMC interface (1-/4-/8-bit MMC bus)<br>　Note: Channel 1 only supports a 1- or 4-bit MMC bus.<br>• e-MMC device access supported<br>• High-speed, HS200 transfer modes supported |
| On-chip RAM | • 4-Mbyte large capacity memory for video display/recording and work<br>　(128 Kbytes are used for data retention)<br>• 128-Kbyte memory for data retention<br>　(16 Kbytes × 2, 32 Kbytes × 1, 64 Kbytes × 1) |
| General I/O ports | • 176-pin products: 47 I/Os, 8 inputs with open-drain outputs, 14 inputs (input only), and 1 output (output only)<br>• 256-pin products: 92 I/Os, 8 inputs with open-drain outputs, 14 inputs (input only), and 1 output (output only)<br>• 272-pin products: 92 I/Os, 8 inputs with open-drain outputs, 14 inputs (input only), and 1 output (output only)<br>• 324-pin products: 128 I/Os, 8 inputs with open-drain outputs, 14 inputs (input only), and 1 output (output only)<br>• Input or output can be selected for each bit. |
| Power-down modes | • Four power-down modes provided to reduce the power consumption in this LSI<br>　　—Sleep mode<br>　　—Software standby mode<br>　　—Deep standby mode<br>　　—Module standby mode |
| Debugger interface | • Arm CoreSight™ architecture<br>• JTAG-standard pin assignment |

Table 1.1        Features of RZ/A2M

| Items | Specification |
|---|---|
| Trusted Secure IP [option] | • Security algorithm<br>Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4<br>Non-common key encryption: RSA<br>• Other features<br>TRNG (true-random number generator)<br>Hash value generation: SHA1, SHA224, SHA256, GHASH<br>Support of unique ID |
| OTP | • A nonvolatile memory that can be written only once<br>• Security setting, authentication setting and the OTP boot setting are possible. |
| Dynamic reconfigurable processor (DRP) [option] | • Dynamically reconfigurable intellectual property module<br>• 6 tiles<br>• 32 I/O ports |
| Power supply voltage | • Vcc: 1.14 to 1.26 V, PVcc: 3.0 to 3.6 V, PVcc_HO: 1.7 to 1.9 V<br>• PVcc_SPI/PVcc_SD0/PVcc_SD1: 1.7 to 1.9 V/3.0 to 3.6 V |
| Temperature range | -40 to +85°C |
| Quality level | Industrial usage, etc. |
| Package | • PLBG0176GA-B<br>176-pin BGA, 13-mm square, 0.8-mm pitch<br>JEITA Package Code: P-LFBGA176-13×13-0.80<br>RENESAS Code: PLBG0176GA-B<br>• PLBG0256KA-A<br>256-pin BGA, 11-mm square, 0.5-mm pitch<br>JEITA Package Code: P-LFBGA256-11×11-0.50<br>RENESAS Code: PLBG0256KA-A<br>• PRBG0272GA-A<br>272-pin BGA, 17-mm square, 0.80-mm pitch<br>JEITA Package Code: P-LFBGA272-17×17-0.80<br>RENESAS Code: PRBG0272GA-A<br>• PRBG0324GA-A<br>324-pin BGA, 19-mm square, 0.8-mm pitch<br>JEITA Package Code: P-FBGA324-19x19-0.80<br>RENESAS Code: PRBG0324GA-A |

## 1.2    Block Diagram

This LSI has two main buses: the north main bus where peripheral modules are connected and the south main bus where on-chip RAM and external ROM and RAM are connected. Figure 1.1 is a schematic diagram of the internal buses.
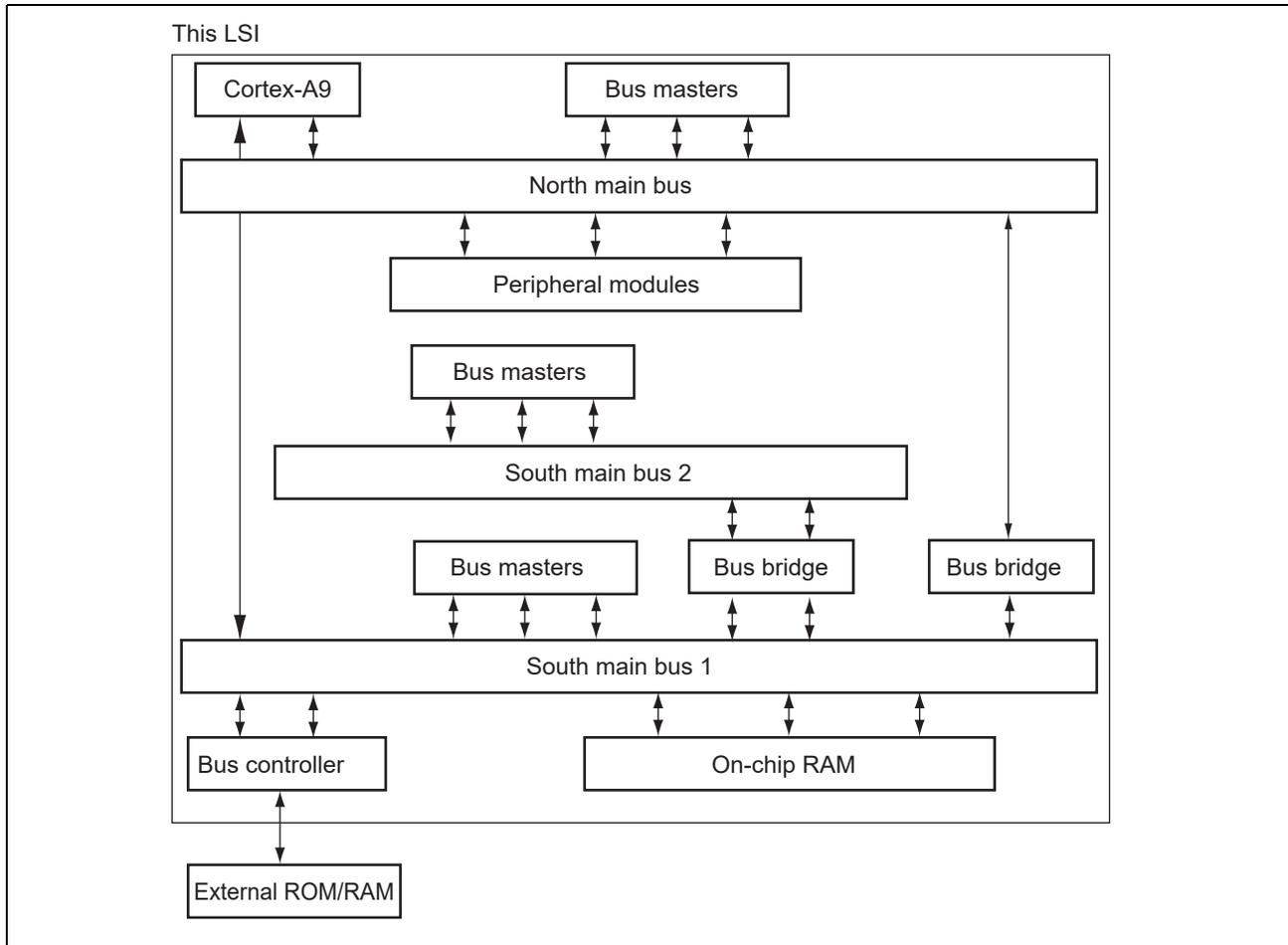


Figure 1.1          Schematic Diagram of LSI Internal Bus

Figure 1.2 shows the schematic diagram of North Main Bus, Figure 1.3 shows the schematic diagram of South Main Bus.



Figure 1.2          North Main Bus Configuration



Figure 1.3          Configuration of the South Main Buses

## 1.3    Product Lineup

Table 1.2    Product Lineup

| Group | Part Number | DRP Function | Trusted Secure IP | Package |
|-------|-------------|--------------|-------------------|---------|
| RZ/A2M | R7S921040VCBG | No DRP | No Trusted Secure IP | PLBG0176GA-B |
| | R7S921041VCBG | | | PLBG0256KA-A |
| | R7S921042VCBG | | | PRBG0272GA-A |
| | R7S921043VCBG | | | PRBG0324GA-A |
| | R7S921045VCBG | | Available | PLBG0176GA-B |
| | R7S921046VCBG | | | PLBG0256KA-A |
| | R7S921047VCBG | | | PRBG0272GA-A |
| | R7S921048VCBG | | | PRBG0324GA-A |
| | R7S921051VCBG | Available | No Trusted Secure IP | PLBG0256KA-A |
| | R7S921052VCBG | | | PRBG0272GA-A |
| | R7S921053VCBG | | | PRBG0324GA-A |
| | R7S921056VCBG | | Available | PLBG0256KA-A |
| | R7S921057VCBG | | | PRBG0272GA-A |
| | R7S921058VCBG | | | PRBG0324GA-A |

Note:    Usable pins of the modules listed below depend on the type of package in which the given product comes.
For details, see section 2.1.2, List of Pins.
• Interrupt controller
• Direct memory access controller
• Multi-function timer pulse unit 3
• General PWM timer
• HyperBus controller
• Serial sound interface
• CANFD interface
• Renesas SPDIF interface
• NAND flash controller
• Video display controller 6

# 2.    Pin

## 2.1    Pin Functions

### 2.1.1        Pin Function of Functional Blocks

Table 2.1        List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| Power supply | Vcc | I | Power supply | Power supply pins. All the Vcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open. |
| | Vss | I | Ground | Ground pins. All the Vss pins must be connected to the system power supply (0 V). This LSI does not operate correctly if there is a pin left open. |
| | PVcc | I | Power supply for I/O circuits | Power supply for I/O pins. All the PVcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open. |
| | PVcc_SPI, PVcc_HO, PVcc_SD0, PVcc_SD1 | I | Power supply for I/O circuits | Power supply for I/O pins. All the PVcc_SPI, PVcc_HO, PVcc_SD0, PVcc_SD1 pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open. |
| | PLLVcc | I | Power supply for PLL | Power supply for the on-chip PLL oscillator. |
| Clock | EXTAL | I | External clock | Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin. |
| | XTAL | O | Crystal | Connected to a crystal resonator. |
| | CKIO | O | System clock output | Supplies the system clock to external devices. |
| | AUDIO_CLK | I | External clock for audio | Input pin of external clock for audio. A clock input to the divider is selected from an oscillation clock input on this pin or pins AUDIO_X1 and AUDIO_X2. |
| | AUDIO_X1 | I | Crystal resonator/ external clock for audio | Pins connected to a crystal resonator for audio. An external clock can be input on pin AUDIO_X1. A clock input to the divider is selected from an oscillation clock input on these pins or the AUDIO_CLK pin. |
| | AUDIO_X2 | O | | |
| | AUDIO_XOUT | O | AUDIO_X1 clock output | Output for the on-chip oscillator on AUDIO_X1 or the external clock signal. |
| Operating mode control | MD_BOOT2, MD_BOOT1, MD_BOOT0 | I | Mode set | Sets the operating mode. Do not change the signal levels on these pins while the RES# pin is asserted or until the mode is fixed, after the negation. |
| | MD_CLK | I | Clock mode set | Sets the clock operating mode. Do not change the signal levels on this pin while the RES# pin is asserted or until the mode is fixed, after the negation. |
| | MD_CLKS | I | SSCG clock mode set | Switches the SSCG circuit on or off. Do not change the signal levels on this pin while the RES# pin is asserted or until the mode is fixed, after the negation. |
| | BSCANP | I | Boundary scan set | Boundary scan setting pin. This pin is set to the high level for a boundary scan and to the low level for normal operation. |
| System control | RES# | I | Power-on reset | This LSI enters the power-on reset state when this signal goes low. |
| | WDTOVF# / PERROUT# | O | Watchdog timer overflow / CPU Parity error | Outputs an overflow signal from the watchdog timer. Outputs the CPU parity error. |

Table 2.1        List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| Interrupts | NMI | I | Non-maskable interrupt | Non-maskable interrupt request pin. It is handled as an FIQ exception. Fix it high when not in use. |
| | IRQ7 to IRQ0 | I | Interrupt requests 7 to 0 | Maskable interrupt request pins. Level-input or edge-input detection can be selected. When the edge-input detection is selected, the rising edge, falling edge, or both edges can also be selected. |
| Address bus | A25 to A0 | O | Address bus | Outputs addresses |
| Data bus | D15 to D0 | I/O | Data bus | Bidirectional data bus |
| Bus control | CS5# to CS0# | O | Chip select 5 to 0 | Chip-select signals for external memory or devices. |
| | RD# | O | Read | Indicates that data is read from an external device. |
| | RD/WR# | O | Read/write | Read/write signal |
| | BS# | O | Bus start | Bus-cycle start signal |
| | AH# | O | Address hold | Address hold timing signal for the device that uses the address/data-multiplexed bus. |
| | WAIT# | I | Wait | Inserts a wait cycle into the bus cycles during access to the external space. |
| | WE0# | O | Byte select | Indicates a write access to bits 7 to 0 of data of external memory or device. |
| | WE1# | O | Byte select | Indicates a write access to bits 15 to 8 of data of external memory or device. |
| | DQML | O | Byte select | Selects bits D7 to D0 when SDRAM is connected. |
| | DQMU | O | Byte select | Selects bits D15 to D8 when SDRAM is connected. |
| | RAS# | O | RAS | Connected to the RAS# pin when SDRAM is connected. |
| | CAS# | O | CAS | Connected to the CAS# pin when SDRAM is connected. |
| | CKE | O | CK enable | Connected to the CKE pin when SDRAM is connected. |
| Direct memory access controller | DREQ0 | I | DMA-transfer request | Input pin to receive external requests for DMA transfer. |
| | DACK0 | O | DMA-transfer request accept | Output pin for signals indicating acceptance of external requests from external devices. |
| | TEND0 | O | DMA-transfer end output | Output pin for DMA transfer end. |

Table 2.1       List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| Multi-function timer pulse unit 3 | MTCLKA, MTCLKB, MTCLKC, MTCLKD | I | Timer clock input | Input pins for external clock signals or for phase counting mode clock signals. |
| | MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D | I/O | Input capture/output compare (channel 0) | TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins. |
| | MTIOC1A, MTIOC1B | I/O | Input capture/output compare (channel 1) | TGRA_1 and TGRB_1 input capture input/output compare output/PWM output pins. |
| | MTIOC2A, MTIOC2B | I/O | Input capture/output compare (channel 2) | TGRA_2 and TGRB_2 input capture input/output compare output/PWM output pins. |
| | MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D | I/O | Input capture/output compare (channel 3) | TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins. |
| | MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D | I/O | Input capture/output compare (channel 4) | TGRA_4 to TGRD_4 input capture input/output compare output/PWM output pins. |
| | MTIC5U, MTIC5V, MTIC5W | I/O | Input capture/output compare (channel 5) | TGRU_5, TGRV_5, and TGRW_5 input capture input/dead time compensation input pins. |
| | MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D | I/O | Input capture/output compare (channel 6) | TGRA_6 and TGRB_6 input capture input/output compare output/PWM output pins. |
| | MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D | I/O | Input capture/output compare (channel 7) | TGRA_7 to TGRD_7 input capture input/output compare output/PWM output pins. |
| | MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D | I/O | Input capture/output compare (channel 8) | TGRA_8 to TGRD_8 input capture input/output compare output pins. |
| Port output enable 3 | POE0#, POE4#, POE8#, POE10# | I | High impedance request | Input pins for request signals to place the MTU3a waveform output pins in the high impedance state. |
| General purpose PWM timer | GTETRGA to GTETRGD | I | External trigger | External trigger input pins. |
| | GTIOC0A to GTIOC7A, GTIOC0B to GTIOC7B | I/O | Timer I/O | Input capture, output compare, or PWM output pins. |
| Realtime clock | RTC_X1 | I | Crystal resonator for realtime clock/external clock | Connected to 32.768-kHz crystal resonator The RTC_X1 pin can also be used to input an external clock. |
| | RTC_X2 | O | | |
| | EXTAL | I | Crystal resonator for internal clock/external clock | Connected to a crystal resonator. |
| | XTAL | O | | |
| Serial communication interface with FIFO | TxD4 to TxD0 | O | Transmit data | Data output pins. |
| | RxD4 to RxD0 | I | Receive data | Data input pins. |
| | SCK4 to SCK0 | I/O | Serial clock | Clock input/output pins. |
| | RTS2#, RTS1#, RTS0# | O | Transmit request | Modem control pins. |
| | CTS2#, CTS1#, CTS0# | I/O | Transmit enable | Modem control pins. |
| Serial communication interface | SCI_SCK1, SCI_SCK0 | I/O | Serial clock | Clock input/output pins. |
| | SCI_TXD1, SCI_TXD0 | O | Transmit data | Data output pins. |
| | SCI_RXD1, SCI_RXD0 | I | Receive data | Data input pins. |
| | SCI_CTS1# / RTS1#, SCI_CTS0# / RTS0# | I/O | Transmit and receive start control | I/O pins for controlling the start of transmission and reception. |
| $I^2C$ bus interface | RIIC3SCL to RIIC0SCL | I/O | Serial clock pin | Serial clock I/O pins. |
| | RIIC3SDA to RIIC0SDA | I/O | Serial data pin | Serial data I/O pins. |
| Serial sound interface | SSITxD3, SSITxD1, SSITxD0 | O | Data output | Serial data output pin. |
| | SSIRxD3, SSIRxD1, SSIRxD0 | I | Data input | Serial data input pin. |
| | SSIDATA2 | I/O | Data I/O | Serial data I/O pins. |
| | SSIBCK3 to SSISBCK0 | I/O | bit clock I/O | I/O pins for bit clocks. |
| | SSILRCK3 to SSILRCK0 | I/O | LR clock I/O | I/O pins for LR clock / frame sync. |

Table 2.1        List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| CANFD interface | CAN_CLK | I | Clock source for CAN communication | Clock source for CAN communication. |
| | CAN1TX, CAN0TX | O | CAN bus transmit data | Output pins for transmit data on the CAN bus. |
| | CAN1RX, CAN0RX | I | CAN bus receive data | Input pins for receive data on the CAN bus. |
| | CAN0RX_DATARATE_EN, CAN1RX_DATARATE_EN | O | CAN Bus receive data phase | This pin indicates the receive data phase of the CAN bus. This pin is set to "1" in the data (high-speed bit rate) area. |
| | CAN0TX_DATARATE_EN, CAN1TX_DATARATE_EN | O | CAN bus transmit data phase | This pin indicates the transmit data phase of the CAN bus. This pin is set to "1" in the data (high-speed bit rate) area. |
| Renesas SPDIF interface | SPDIF_OUT | O | Data output | Transmit data output pin. |
| | SPDIF_IN | I | Data input | Receive data input pin. |
| Renesas serial peripheral interface | MOSI2 to MOSI0 | I/O | Data | Data I/O pins. |
| | MISO2 to MISO0 | I/O | Data | Data I/O pins. |
| | RSPCK2 to RSPCK0 | I/O | Clock | Clock I/O pins. |
| | SSL20, SSL10, SSL00 | I/O | Slave select | Slave select I/O pins. |
| SPI multi I/O bus controller | QSPI0_SPCLK, QSPI1_SPCLK | O | Clock | Clock output pins. |
| | QSPI0_SSL | O | Slave select | Slave select output pins. |
| | QSPI1_SSL | I/O | Slave select or Data strobe | When serial flash memory is connected: This pin serves as a slave select output pin. When Octal-SPI flash or HyperFlash memory is connected: This pin serves as a data strobe input pin. |
| | QSPI0_IO3 to QSPI0_IO0, QSPI1_IO3 to QSPI1_IO0 | I/O | Data | Data I/O pins. |
| | RPC_RESET# | O | Reset | Reset output pin. |
| | RPC_WP# | O | Write protect | Write protect output pin. |
| | RPC_INT# | I | Interrupt | Interrupt input pin. |
| HyperBus controller | HM_CK | O | Clock | Differential clock output pin. |
| | HM_CK# | O | Clock | Differential clock output pin. |
| | HM_CS0# | O | Chip select 0 | Chip select signal for the external memory. |
| | HM_CS1# | O | Chip select 1 | Chip select signal for the external memory. |
| | HM_RWDS | I/O | Read Write Data Strobe | Read: data strobe pin. Write: data Mask pin. |
| | HM_DQ7 to HM_DQ0 | I/O | Data | Data I/O pin. |
| | HM_RESET# | O | Reset output | Reset signal for the external memory. |
| | HM_RSTO# | I | Reset input | Reset signal from the external memory. |
| | HM_INT# | I | Interrupt input | Interrupt signal from the external memory. |

Table 2.1        List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| Octa memory controller | OM_SCLK | O | Clock | clock output pin. |
| | OM_CS0# | O | Chip select 0 | Chip select signal for the external memory. |
| | OM_CS1# | O | Chip select 1 | Chip select signal for the external memory. |
| | OM_DQS | I/O | Data strobe | Read: data strobe pin. Write: data Mask pin. |
| | OM_SIO7 to OM_SIO0 | I/O | Data | Data I/O pins. |
| | OM_RESET# | O | Reset output | Reset signal for the external memory. |
| | OM_ECS# | I | ECC error detection | ECC error detection pin from the external memory. |
| Ethernet controller | ET1_TXCLK, ET0_TXCLK | I | Transmit clock | MII clock pin for transmission. |
| | ET1_TXEN, ET0_TXCLK | O | Transmit enable | MII transmit data enable pin |
| | ET0_TXD3 to ET0_TXD0, ET1_TXD3 to ET1_TXD0 | O | Transmit data | MII transmit data pins. |
| | ET1_COL, ET0_COL | I | Collision detection | MII collision detection pin. |
| | ET1_TXER, ET0_TXER | O | Transmit error | MII transmit error output pin. |
| | ET1_RXCLK, ET0_RXCLK | I | Receive clock | MII receive clock pin |
| | ET1_RXDV, ET0_RXDV | I | Receive enable | MII receive data enable pin |
| | ET1_RXD3 to ET1_RXD0, ET0_RXD3 to ET0_RXD0 | I | Receive data | MII receive data pins. |
| | ET1_RXER, ET0_RXER | I | Receive error | MII receive error input pin. |
| | ET1_CRS, ET0_CRS | I | Carrier detection | MII carrier detection pin. |
| | REF50CK0, REF50CK1 | I | Reference clock | RMII reference clock pin. |
| | RMII0_CRS_DV, RMII1_CRS_DV | I | Carrier detection and Receive enable | RMII carrier detection and Receive enable pin. |
| | RMII0_TXD1, RMII0_TXD0, RMII1_TXD1, RMII1_TXD0 | O | Transmit data | RMII transmit data pin. |
| | RMII0_TXD_EN, RMII1_TXD_EN | O | Transmit enable | RMII transmit enable pin. |
| | RMII0_RXER, RMII1_RXER | I | Receive error | RMII receive error input pin. |
| | RMII0_RXD1, RMII0_RXD0, RMII1_RXD1, RMII1_RXD0 | I | Receive data | RMII receive data pin. |
| | ET1_MDC, ET0_MDC | O | Management data clock | Clock pin for information transfer via MDIO. |
| | ET1_MDIO, ET0_MDIO | I/O | Management data I/O | Bidirectional pin for exchange of management data. |
| | ET1_LINKSTA, ET0_LINKSTA | I | Status | Link status pin from the PHY-LSI. |
| | ET1_EXOUT, ET0_EXOUT | O | General purpose output | General purpose output pin. |
| | ET1_WOL, ET0_WOL | O | Wake-On-LAN | Indicate the LSI receive a Magic Packet. |
| | ET0_SCLKIN, ET1_SCLKIN | I | SCLKA clock | Clock signal supplied to the statistical time correction algorithm unit. |

Table 2.1          List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| NAND flash controller | NFALE | O | Flash memory address latch enable | Asserted for address output and negated for data I/O. |
| | NFRE# | O | Flash memory read enable | Reads data at falling edge. |
| | NFCE# | O | Flash memory chip enable | Enables the flash memory connected to this LSI. |
| | NFCLE | O | Flash memory command latch enable | Asserted at command output. |
| | NFRB# | I | Flash memory ready/busy | High level indicates ready state and low level indicates busy state. |
| | NFWE# | O | Flash memory write enable | Flash memory latches commands, addresses, and data at falling edge. |
| | NFDATA[7:0] | I/O | Flash memory data | Data I/O pins. |
| USB 2.0 host/function module | DP1, DP0 | I/O | USB 2.0 host/function module D+ data | D+ data pins for USB 2.0 host/function module bus. |
| | DM1, DM0 | I/O | USB 2.0 host/function module D– data | D– data pins for USB 2.0 host/function module bus. |
| | VBUSIN1, VBUSIN0 | I | VBUS input | A pin for monitoring connection of the USB cable. Step down the VBUS voltage to 3.3 V. Connect this pin to the Vbus pin of the USB bus so that it can detect connection and disconnection of the Vbus pin. |
| | VBUSEN1, VBUSEN0 | O | VBUS output | VBUS power supply enable pin. |
| | OVRCUR1, OVRCUR0 | I | Overcurrent input | Overcurrent input pin. |
| | OTG_EXICEN1, OTG_EXICEN0 | O | OTG Power supply IC control | OTG Power supply IC control pin. |
| | OTG_ID1, OTG_ID0 | I | OTG Power supply IC ID | OTG Power supply IC ID pin. |
| | CC1_Rd1, CC1_Ra1, CC2_Rd1, CC2_Ra1, CC1_Rd0, CC1_Ra0, CC2_Rd0, CC2_Ra0 | I | CC input | These pins are used to monitor the state of the resistance on the CC pins of the USB Type-C connector. Check the state of the resistance of the USB Type-C connector and input the result of checking through the CC pins of the RZ/A2M. |
| | RREF1, RREF0 | I | Reference input | Connected to USBVss via 2.2kΩ ± 1% resistance. |
| | USB_X1 | I | Crystal resonator for USB 2.0 host/function module | Connected to a crystal resonator for USB 2.0 host/function module. |
| | USB_X2 | O | | |
| | USBAPVcc1, USBAPVcc0 | I | Power supply for transceiver analog pins | Power supply for pins. |
| | USBDPVcc1, USBDPVcc0 | I | Power supply for transceiver digital pins | Power supply for pins. |
| | USBVss | I | Ground for transceiver pins | Ground for pins. |
| Video display controller 6 | LCD0_DATA23 to LCD0_DATA0 | O | Output data | Data output pins for panel. |
| | LCD0_TCON6 to LCD0_TCON0 | O | Panel timing adjustment output | Output pins for panel timing adjustment. |
| | LCD0_CLK | O | Panel clock | Panel clock output pins. |
| | LCD0_EXTCLK | I | Panel clock source | Panel clock source input pins. |
| | DV0_DATA23 to DV0_DATA0 | I | Input data | Data input pins for graphics data. |
| | DV0_VSYNC | I | VSYNC input | VSYNC input pins. |
| | DV0_HSYNC | I | HSYNC input | HSYNC input pins. |
| | DV0_CLK | I | Input clock | Clock input signal pins for graphics data. |

Table 2.1        List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| LVDS output interface | TXCLKOUTP, TXCLKOUTM | O | Output clock | LVDS differential clock output pins. |
| | TXOUT2P to TXOUT0P, TXOUT2M to TXOUT0M | O | Output data | LVDS differential data output pins. |
| | LVDSAPVcc | I | LVDS analog power supply | Power supply for LVDS output. |
| | LVDSPLLVcc | I | LVDS PLL power supply | Power supply for LVDS PLL. |
| Capture engine unit | VIO_D15 to VIO_D0 | I | Input data | Graphics data input pins. |
| | VIO_CLK | I | Input clock | Graphics data clock input pin. |
| | VIO_VD | I | VSYNC input | VSYNC input pin. |
| | VIO_HD | I | HSYNC input | HSYNC input pin. |
| | VIO_FLD | I | FIELD input | Input pin for field information |
| MIPI CSI-2 interface | CSI_DATA0P | I | Input data | Positive data receive pin for CSI Lane 0 differential input. |
| | CSI_DATA0N | I | Input data | Negative data receive pin for CSI Lane 0 differential input. |
| | CSI_DATA1P | I | Input data | Positive data receive pin for CSI Lane 1 differential input. |
| | CSI_DATA1N | I | Input data | Negative data receive pin for CSI Lane 1 differential input. |
| | CSI_CLKP | I | Input clock | Positive receive pin for CSI clock Lane input. |
| | CSI_CLKN | I | Input clock | Negative receive pin for CSI clock Lane input. |
| | MIPIAVcc18 | I | MIPI analog power supply | Power supply for the MIPI analog circuits. |
| SD/MMC host interface | SD0_CLK, SD1_CLK | O | SD/MMC clock | Output pins for SD/MMC clock. |
| | SD0_CMD, SD1_CMD | I/O | SD/MMC command | SD/MMC command output and response input signals. |
| | SD0_DAT7 to SD0_DAT0, SD1_DAT3 to SD1_DAT0 | I/O | SD/MMC data | SD/MMC data bus signals. |
| | SD0_CD, SD1_CD | I | SD/MMC card detection | SD/MMC card detection. |
| | SD0_WP, SD1_WP | I | SD/MMC write protection | SD/MMC write protection signals. |
| | SD0_RST# | O | SD/MMC reset | SD/MMC reset signal. |
| A/D converter | AN007 to AN000 | I | Analog input pins | Analog input pins. |
| | ADTRG# | I | A/D conversion trigger input | External trigger input pin for starting A/D conversion. |
| | AVcc | I | Analog power supply and reference voltage | Analog power supply and reference voltage pin for A/D converter. |
| | AVss | I | Analog ground | Ground pin for A/D converter. |
| General I/O ports | P0_0 to PK_5 | I/O | General port | General purpose I/O port pins<br>176-pin products: 47 pins<br>256-pin products: 92 pins<br>272-pin products: 92 pins<br>324-pin products: 128 pins |
| | PD_0 to PD_7 | I/O | General port | 8 general input port pins with open-drain output. |
| | P5_0 to P5_7, PL_0 to PL_4, JP0_0 | I | General port | 14 general input port pins |
| | JP0_1 | O | General port | 1 general output port pin |

Table 2.1        List of Pin Functions

| Classification | Symbol | I/O | Name | Function |
|---|---|---|---|---|
| Debugger interface | TCK/SWDCLK | I | Test clock | Test-clock input pin.<br>Also used as the input clock pin for serial wire debugging |
| | TMS/SWDIO | I/O | Test mode select | Test-mode select signal input pin.<br>Also used as the I/O data pin for serial wire debugging |
| | TDI | I | Test data input | Serial input pin for instructions and data. |
| | TDO/SWO | O | Test data output | Serial output pin for instructions and data. |
| | TRST# | I | Test reset | Initialization-signal input pin. |
| | TRACEDATA3 to TRACEDATA0 | O | Data output | Trace data output pins. |
| | TRACECLK | O | Clock output | Trace clock output pin. |
| | TRACECTL | O | Enable output | Trace enable output pin. |
| Dynamic Reconfigurable Processor (DRP)* | DRP31 to DRP00 | I/O | DRP I/O pins | 32 DRP input/output pins |

Note:   * Only in products with a DRP

## 2.1.2 List of Pins

Table 2.2 List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | Vcc | | | | | | | | | | | | | | | | | | |
| A2 | QSPI1_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A3 | QSPI1_SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A4 | RPC_WP# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A5 | QSPI0_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A6 | PVcc_SPI | | | | | | | | | | | | | | | | | | |
| A7 | Vss | | | | | | | | | | | | | | | | | | |
| A8 | PVcc | | | | | | | | | | | | | | | | | | |
| A9 | PF_4 | I(s)/O | - | - | RxD2 | I(s) | DV0_DATA19 | I(s) | LCD0_DATA4 | O | MTIOC6A | I(s)/O | SSIBCK0 | I(s)/O | IRQ1 | I(s) | - | - | (1) |
| A10 | PE_6 | I(s)/O | - | - | ET0_MDIO | I(s)/O | VIO_D2 | I(s) | SSIRxD0 | I(s) | MTIOC0D | I(s)/O | CC2_Rd1 | I(s) | - | - | - | - | (1) |
| A11 | PL_2 | I(s) | MD_BOOT2 | I(s) | - | - | - | - | - | - | - | - | IRQ6 | I(s) | - | - | - | - | (5) |
| A12 | PE_5 | I(s)/O | - | - | ET0_MDC | O | VIO_D3 | I(s) | SSITxD0 | O | MTIOC0C | I(s)/O | CC1_Rd1 | I(s) | - | - | - | - | (1) |
| A13 | P8_4 | I(s)/O | - | - | A4 | O | DRP20* | I(s)/O | DV0_DATA13 | I(s) | SSL00 | I(s)/O | SSIRxD3 | I(s) | - | - | - | - | (1) |
| A14 | P8_6 | I(s)/O | - | - | A6 | O | DRP18* | I(s)/O | DV0_DATA11 | I(s) | MOSI0 | I(s)/O | SSILRCK3 | I(s)/O | - | - | - | - | (1) |
| A15 | PE_4 | I(s)/O | - | - | ET0_CRS | I(s) | VIO_D4 | I(s) | SSILRCK0 | I(s)/O | MTIOC0B | I(s)/O | - | - | - | - | RMII0_CRS_DV | I(s) | (1) |
| A16 | P9_1 | I(s)/O | - | - | A9 | O | DRP15* | I(s)/O | DV0_DATA8 | I(s) | RxD4 | I(s) | SSILRCK2 | I(s)/O | - | - | - | - | (1) |
| A17 | PVcc | | | | | | | | | | | | | | | | | | |
| A18 | Vss | | | | | | | | | | | | | | | | | | |
| A19 | PE_1 | I(s)/O | - | - | ET0_RXD0 | I(s) | VIO_D7 | I(s) | RxD2 | I(s) | POE8# | I(s) | VBUSIN1 | I(s) | IRQ1 | I(s) | RMII0_RXD0 | I(s) | (1) |
| A20 | PA_4 | I(s)/O | - | - | A20 | O | DV0_DATA9 | I(s) | LCD0_DATA14 | O | SCI_TXD0 | I(s)/O | MTIOC0C | I(s)/O | - | - | - | - | (1) |
| A21 | CKIO | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (11) |
| A22 | Vss | | | | | | | | | | | | | | | | - | - | |
| B1 | PK_1 | I(s)/O | - | - | ET1_TXD0 | O | NFDATA4 | I(s)/O | CC1_Ra0 | I(s) | CAN_CLK | I(s) | SSIDATA2 | I(s)/O | - | - | RMII1_TXD0 | O | (1) |
| B2 | Vcc | | | | | | | | | | | | | | | | | | |
| B3 | QSPI1_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B4 | QSPI1_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B5 | RPC_RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B6 | QSPI0_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B7 | QSPI0_SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B8 | PF_5 | I(s)/O | - | - | TxD2 | O | DV0_DATA20 | I(s) | LCD0_DATA3 | O | MTIOC6B | I(s)/O | SSILRCK0 | I(s)/O | - | - | - | - | (1) |
| B9 | P6_3 | I(s)/O | - | - | ET0_TXD1 | O | VIO_HD | I(s) | TxD3 | O | POE0# | I(s) | - | - | - | - | RMII0_TXD1 | O | (1) |
| B10 | PH_0 | I(s)/O | - | - | AUDIO_CLK | I(s) | VIO_D1 | I(s) | GTIOC4A | I(s)/O | MTIOC1A | I(s)/O | CC1_Rd0 | I(s) | IRQ3 | I(s) | - | - | (1) |
| B11 | PL_3 | I(s) | MD_BOOT1 | I(s) | - | - | - | - | - | - | - | - | IRQ7 | I(s) | - | - | - | - | (5) |
| B12 | PL_1 | I(s) | MD_CLK | I(s) | - | - | - | - | - | - | - | - | IRQ5 | I(s) | - | - | - | - | (5) |
| B13 | P8_3 | I(s)/O | - | - | A3 | O | DRP21* | I(s)/O | DV0_DATA14 | I(s) | MTIOC6A | I(s)/O | GTIOC3A | I(s)/O | - | - | - | - | (1) |
| B14 | PF_2 | I(s)/O | - | - | TxD3 | O | DV0_DATA17 | I(s) | LCD0_DATA6 | O | MTIOC7C | I(s)/O | MISO1 | I(s)/O | - | - | - | - | (1) |
| B15 | P8_7 | I(s)/O | - | - | A7 | O | DRP17* | I(s)/O | DV0_DATA10 | I(s) | RSPCK0 | I(s)/O | SSIBCK3 | I(s)/O | - | - | - | - | (1) |
| B16 | PE_3 | I(s)/O | - | - | ET0_RXER | I(s) | VIO_D5 | I(s) | SSIBCK0 | I(s)/O | MTIOC0A | I(s)/O | - | - | - | - | RMII0_RXER | I(s) | (1) |
| B17 | PA_0 | I(s)/O | - | - | A16 | O | DV0_DATA13 | I(s) | LCD0_DATA10 | O | SCI_TXD1 | I(s)/O | MTIOC8C | I(s)/O | - | - | - | - | (1) |
| B18 | PA_3 | I(s)/O | - | - | A19 | O | DV0_DATA10 | I(s) | LCD0_DATA13 | O | SCI_CTS0#/RTS0# | I(s)/O | MTIOC0D | I(s)/O | - | - | - | - | (1) |
| B19 | PA_5 | I(s)/O | - | - | A21 | O | DV0_DATA8 | I(s) | LCD0_DATA15 | O | SCI_RXD0 | I(s)/O | MTIOC0B | I(s)/O | IRQ5 | I(s) | - | - | (1) |

Table 2.2 List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B20 | PA_6 | I(s)/O | - | - | A22 | O | DV0_DATA7 | I(s) | LCD0_DATA16 | O | SCI_SCK0 | I(s)/O | MTIOC0A | I(s)/O | - | - | - | - | (1) |
| B21 | Vss | | | | | | | | | | | | | | | | | | |
| B22 | PVcc | | | | | | | | | | | | | | | | | | |
| C1 | PH_2 | I(s)/O | - | - | CTS2# | I(s)/O | DV0_DATA22 | I(s) | LCD0_DATA1 | O | MTIOC6D | I(s)/O | SSIRxD0 | I(s) | - | - | - | - | (1) |
| C2 | P8_2 | I(s)/O | - | - | A2 | O | DRP22* | I(s)/O | DV0_DATA15 | I(s) | GTIOC5A | I(s)/O | IRQ2 | I(s) | - | - | - | - | (1) |
| C3 | Vcc | | | | | | | | | | | | | | | | | | |
| C4 | QSPI1_SSL | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C5 | RPC_INT# | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C6 | QSPI0_SSL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C7 | QSPI0_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C8 | P6_1 | I(s)/O | - | - | ET0_TXEN | O | VIO_CLK | I(s) | SCK3 | I(s)/O | MTIOC2A | I(s)/O | - | - | - | - | RMII0_TXD_EN | O | (1) |
| C9 | P6_2 | I(s)/O | - | - | ET0_TXD0 | O | VIO_VD | I(s) | RxD3 | I(s) | MTIOC2B | I(s)/O | OTG_EXICEN1 | O | IRQ0 | I(s) | RMII0_TXD0 | O | (1) |
| C10 | PH_1 | I(s)/O | - | - | AUDIO_XOUT | O | VIO_D0 | I(s) | GTIOC4B | I(s)/O | MTIOC1B | I(s)/O | CC2_Rd0 | I(s) | IRQ2 | I(s) | - | - | (1) |
| C11 | PL_4 | I(s) | MD_BOOT0 | I(s) | - | - | - | - | - | - | - | - | IRQ0 | I(s) | - | - | - | - | (5) |
| C12 | PL_0 | I(s) | MD_CLKS | I(s) | - | - | - | - | - | - | - | - | IRQ4 | I(s) | - | - | - | - | (5) |
| C13 | P8_5 | I(s)/O | - | - | A5 | O | DRP19* | I(s)/O | DV0_DATA12 | I(s) | MISO0 | I(s)/O | SSITxD3 | O | - | - | - | - | (1) |
| C14 | PF_1 | I(s)/O | - | - | RxD3 | I(s) | DV0_DATA16 | I(s) | LCD0_DATA7 | O | MTIOC7B | I(s)/O | MOSI1 | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| C15 | P9_0 | I(s)/O | - | - | A8 | O | DRP16* | I(s)/O | DV0_DATA9 | I(s) | TxD4 | O | SSIDATA2 | I(s)/O | - | - | - | - | (1) |
| C16 | PE_2 | I(s)/O | - | - | ET0_RXD1 | I(s) | VIO_D6 | I(s) | TxD2 | O | POE10# | I(s) | - | - | - | - | RMII0_RXD1 | I(s) | (1) |
| C17 | PA_2 | I(s)/O | - | - | A18 | O | DV0_DATA11 | I(s) | LCD0_DATA12 | O | SCI_SCK1 | I(s)/O | MTIOC8A | I(s)/O | - | - | - | - | (1) |
| C18 | PG_0 | I(s)/O | - | - | ET0_TXCLK | I(s) | VIO_D8 | I(s) | RSPCK0 | I(s)/O | MTIOC3A | I(s)/O | HM_RSTO# | I(s) | - | - | - | - | (1) |
| C19 | PB_0 | I(s)/O | - | - | A24 | O | DV0_DATA5 | I(s) | LCD0_DATA18 | O | SSITxD1 | O | POE8# | I(s) | - | - | - | - | (1) |
| C20 | Vss | | | | | | | | | | | | | | | | | | |
| C21 | PD_7 | I(s)/O(o) | - | - | RIIC3SDA | I(s)/O(o) | IRQ7 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| C22 | PD_3 | I(s)/O(o) | - | - | RIIC1SDA | I(s)/O(o) | IRQ3 | I(s) | MTCLKD | I(s) | GTETRGD | I(s) | - | - | - | - | - | - | (4) |
| D1 | PVcc | | | | | | | | | | | | | | | | | | |
| D2 | BSCANP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| D3 | P8_1 | I(s)/O | - | - | A1 | O | DRP23* | I(s)/O | DV0_DATA16 | I(s) | GTIOC5B | I(s)/O | IRQ3 | I(s) | - | - | - | - | (1) |
| D4 | Vcc | | | | | | | | | | | | | | | | | | |
| D5 | QSPI1_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D6 | Vss | | | | | | | | | | | | | | | | | | |
| D7 | QSPI0_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D8 | PK_0 | I(s)/O | - | - | ET1_TXEN | O | NFDATA3 | I(s)/O | CC1_Rd0 | I(s) | MTIOC1B | I(s)/O | SSIBCK2 | I(s)/O | - | - | RMII1_TXD_EN | O | (1) |
| D9 | PF_6 | I(s)/O | - | - | RTS2# | I(s)/O | DV0_DATA21 | I(s) | LCD0_DATA2 | O | MTIOC6C | I(s)/O | SSITxD0 | O | - | - | - | - | (1) |
| D10 | PE_0 | I(s)/O | - | - | ET0_RXCLK | I(s) | VIO_FLD | I(s) | SCK2 | I(s)/O | POE4# | I(s) | - | - | - | - | REF50CK0 | I(s) | (1) |
| D11 | PF_3 | I(s)/O | - | - | SCK2 | I(s)/O | DV0_DATA18 | I(s) | LCD0_DATA5 | O | MTIOC7D | I(s)/O | SSL10 | I(s)/O | - | - | - | - | (1) |
| D12 | PVcc | | | | | | | | | | | | | | | | | | |
| D13 | Vss | | | | | | | | | | | | | | | | | | |
| D14 | PF_0 | I(s)/O | - | - | SCK3 | I(s)/O | DV0_DATA15 | I(s) | LCD0_DATA8 | O | MTIOC7A | I(s)/O | RSPCK1 | I(s)/O | - | - | - | - | (1) |
| D15 | P8_0 | I(s)/O | - | - | A0 | O | DV0_DATA14 | I(s) | LCD0_DATA9 | O | SCI_CTS1#/RTS1# | I(s)/O | MTIOC8D | I(s)/O | - | - | - | - | (1) |
| D16 | PA_1 | I(s)/O | - | - | A17 | O | DV0_DATA12 | I(s) | LCD0_DATA11 | O | SCI_RXD1 | I(s)/O | MTIOC8B | I(s)/O | IRQ6 | I(s) | - | - | (1) |
| D17 | PA_7 | I(s)/O | - | - | A23 | O | DV0_DATA6 | I(s) | LCD0_DATA17 | O | SSIRxD1 | I(s) | POE10# | I(s) | - | - | - | - | (1) |

## Table 2.2    List of Pins (324-Pin BGA)

| Ball Number | Port Function/Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D18 | PVcc | | | | | | | | | | | | | | | | | | |
| D19 | Vss | | | | | | | | | | | | | | | | | | |
| D20 | PD_6 | I(s)/O(o) | - | - | RIIC3SCL | I(s)/O(o) | IRQ6 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D21 | PD_4 | I(s)/O(o) | - | - | RIIC2SCL | I(s)/O(o) | IRQ4 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D22 | PD_1 | I(s)/O(o) | - | - | RIIC0SDA | I(s)/O(o) | IRQ1 | I(s) | MTCLKB | I(s) | GTETRGB | I(s) | - | - | - | - | - | - | (4) |
| E1 | Vss | | | | | | | | | | | | | | | | | | |
| E2 | PH_3 | I(s)/O | - | - | HM_RSTO# | I(s) | RTS2# | I(s)/O | GTIOC6A | I(s)/O | MTIOC2A | I(s)/O | SD0_CD | I(s) | IRQ3 | I(s) | - | - | (1) |
| E3 | PK_3 | I(s)/O | - | - | ET1_RXCLK | I(s) | NFDATA6 | I(s)/O | CC2_Rd0 | I(s) | CAN0RX_DATARATE_EN | O | MOSI0 | I(s)/O | - | - | REF50CK1 | I(s) | (1) |
| E4 | PK_2 | I(s)/O | - | - | ET1_TXD1 | O | NFDATA5 | I(s)/O | VBUSEN1 | O | CAN0RX | I(s) | RSPCK0 | I(s)/O | IRQ5 | I(s) | RMII1_TXD1 | O | (1) |
| E19 | PD_5 | I(s)/O(o) | - | - | RIIC2SDA | I(s)/O(o) | IRQ5 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| E20 | PD_2 | I(s)/O(o) | - | - | RIIC1SCL | I(s)/O(o) | IRQ2 | I(s) | MTCLKC | I(s) | GTETRGC | I(s) | - | - | - | - | - | - | (4) |
| E21 | TCK/SWDCLK | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (7) |
| E22 | JP0_0 | I(s) | - | - | TDI | I | - | - | - | - | - | - | - | - | - | - | - | - | (6) |
| F1 | PVcc_HO | | | | | | | | | | | | | | | | | | |
| F2 | HM_CS0#/OM_CS0# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F3 | HM_CK/OM_SCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F4 | PF_7 | I(s)/O | - | - | GTETRGD | I(s) | DV0_DATA23 | I(s) | LCD0_DATA0 | O | MTCLKD | I(s) | IRQ1 | I(s) | - | - | - | - | (1) |
| F19 | PD_0 | I(s)/O(o) | - | - | RIIC0SCL | I(s)/O(o) | IRQ0 | I(s) | MTCLKA | I(s) | GTETRGA | I(s) | - | - | - | - | - | - | (4) |
| F20 | TRST# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| F21 | TMS/SWDIO | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (9) |
| F22 | PB_1 | I(s)/O | - | - | A25 | O | DV0_DATA4 | I(s) | LCD0_DATA19 | O | SSILRCK1 | I(s)/O | POE4# | I(s) | - | - | - | - | (1) |
| G1 | HM_DQ1/OM_SIO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G2 | HM_RWDS/OM_DQS | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G3 | HM_CS1#/OM_CS1# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G4 | HM_CK# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G19 | JP0_1 | O | - | - | TDO/SWO | O | - | - | - | - | - | - | - | - | - | - | - | - | (8) |
| G20 | PB_2 | I(s)/O | - | - | BS# | O | DV0_DATA3 | I(s) | LCD0_DATA20 | O | SSIBCK1 | I(s)/O | POE0# | I(s) | - | - | - | - | (1) |
| G21 | PB_3 | I(s)/O | - | - | CS0# | O | DV0_DATA2 | I(s) | LCD0_DATA21 | O | SSIDATA2 | I(s)/O | CTS0# | I(s)/O | - | - | - | - | (1) |
| G22 | P9_2 | I(s)/O | - | - | A10 | O | DRP14* | I(s)/O | DV0_DATA7 | I(s) | SCK4 | I(s)/O | SSIBCK2 | I(s)/O | - | - | - | - | (1) |
| H1 | HM_DQ4/OM_SIO4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H2 | HM_DQ2/OM_SIO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H3 | HM_DQ3/OM_SIO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H4 | HM_DQ0/OM_SIO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H19 | PB_4 | I(s)/O | - | - | CS1# | O | DV0_DATA1 | I(s) | LCD0_DATA22 | O | SSILRCK2 | I(s)/O | RTS0# | I(s)/O | - | - | - | - | (1) |
| H20 | P9_3 | I(s)/O | - | - | A11 | O | DRP13* | I(s)/O | DV0_DATA6 | I(s) | - | - | SSIRxD0 | I(s) | - | - | - | - | (1) |
| H21 | PB_5 | I(s)/O | - | - | WAIT# | I(s) | DV0_DATA0 | I(s) | LCD0_DATA23 | O | SSIBCK2 | I(s)/O | TxD0 | O | - | - | - | - | (1) |
| H22 | P9_5 | I(s)/O | - | - | A13 | O | DRP11* | I(s)/O | DV0_DATA4 | I(s) | - | - | SSILRCK0 | I(s)/O | - | - | - | - | (1) |
| J1 | HM_RESET#/OM_RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J2 | HM_DQ6/OM_SIO6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |

Table 2.2 List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J3 | HM_DQ7/ OM_SIO7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J4 | HM_DQ5/ OM_SIO5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J9 | Vcc | | | | | | | | | | | | | | | | | | |
| J10 | Vss | | | | | | | | | | | | | | | | | | |
| J11 | Vss | | | | | | | | | | | | | | | | | | |
| J12 | Vss | | | | | | | | | | | | | | | | | | |
| J13 | Vss | | | | | | | | | | | | | | | | | | |
| J14 | Vcc | | | | | | | | | | | | | | | | | | |
| J19 | P9_4 | I(s)/O | - | - | A12 | O | DRP12* | I(s)/O | DV0_DATA5 | I(s) | - | - | SSITxD0 | O | - | - | - | - | (1) |
| J20 | P7_7 | I(s)/O | - | - | RD# | O | DV0_HSYNC | I(s) | LCD0_TCON0 | O | GTIOC3B | I(s)/O | RxD0 | I(s) | - | - | - | - | (1) |
| J21 | P7_6 | I(s)/O | - | - | AH# | O | DV0_VSYNC | I(s) | LCD0_TCON1 | O | GTIOC3A | I(s)/O | SCK0 | I(s)/O | - | - | - | - | (1) |
| J22 | P9_6 | I(s)/O | - | - | A14 | O | DRP10* | I(s)/O | DV0_DATA3 | I(s) | - | - | SSIBCK0 | I(s)/O | - | - | - | - | (1) |
| K1 | Vss | | | | | | | | | | | | | | | | | | |
| K2 | PJ_6 | I(s)/O | - | - | GTETRGC | I(s) | NFCE# | O | LCD0_CLK | O | MTCLKC | I(s) | IRQ0 | I(s) | - | - | - | - | (1) |
| K3 | PH_4 | I(s)/O | - | - | HM_INT#/ OM_ECS# | I(s) | CTS2# | I(s)/O | GTIOC6B | I(s)/O | MTIOC2B | I(s)/O | SD0_WP | I(s) | IRQ2 | I(s) | - | - | (1) |
| K4 | PJ_0 | I(s)/O | - | - | TRACECLK | O | SPDIF_OUT | O | - | - | SCK1 | I(s)/O | SSIRxD3 | I(s) | - | - | - | - | (1) |
| K9 | Vcc | | | | | | | | | | | | | | | | | | |
| K10 | Vss | | | | | | | | | | | | | | | | | | |
| K11 | Vss | | | | | | | | | | | | | | | | | | |
| K12 | Vss | | | | | | | | | | | | | | | | | | |
| K13 | Vss | | | | | | | | | | | | | | | | | | |
| K14 | Vcc | | | | | | | | | | | | | | | | | | |
| K19 | P9_7 | I(s)/O | - | - | A15 | O | DRP09* | I(s)/O | DV0_DATA2 | I(s) | - | - | SD1_WP | I(s) | - | - | - | - | (1) |
| K20 | PG_1 | I(s)/O | - | - | ET0_TXD2 | O | VIO_D9 | I(s) | MOSI0 | I(s)/O | MTIOC3C | I(s)/O | HM_INT#/ OM_ECS# | I(s) | - | - | - | - | (1) |
| K21 | P7_5 | I(s)/O | - | - | CKE | O | DRP08* | I(s)/O | DV0_DATA1 | I(s) | CTS1# | I(s)/O | OVRCUR1 | I(s) | - | - | - | - | (1) |
| K22 | PG_2 | I(s)/O | - | - | ET0_TXD3 | O | VIO_D10 | I(s) | MISO0 | I(s)/O | MTIOC3B | I(s)/O | GTIOC0A | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| L1 | PVcc | | | | | | | | | | | | | | | | | | |
| L2 | P0_1 | I(s)/O | - | - | D1 | I/O | DRP25* | I(s)/O | DV0_DATA18 | I(s) | MTIOC6C | I(s)/O | GTIOC4A | I(s)/O | - | - | - | - | (2) |
| L3 | P0_0 | I(s)/O | - | - | D0 | I/O | DRP24* | I(s)/O | DV0_DATA17 | I(s) | MTIOC6B | I(s)/O | GTIOC3B | I(s)/O | - | - | - | - | (2) |
| L4 | PJ_7 | I(s)/O | - | - | GTETRGB | I(s) | NFDATA0 | I(s)/O | LCD0_EXTCLK | I(s) | MTCLKB | I(s) | - | - | - | - | - | - | (1) |
| L9 | Vcc | | | | | | | | | | | | | | | | | | |
| L10 | Vss | | | | | | | | | | | | | | | | | | |
| L11 | Vss | | | | | | | | | | | | | | | | | | |
| L12 | Vss | | | | | | | | | | | | | | | | | | |
| L13 | Vss | | | | | | | | | | | | | | | | | | |
| L14 | Vcc | | | | | | | | | | | | | | | | | | |
| L19 | P7_1 | I(s)/O | - | - | RD/WR# | O | DRP05* | I(s)/O | DV0_VSYNC | I(s) | RxD1 | I(s) | CC1_Ra1 | I(s) | - | - | - | - | (1) |
| L20 | P7_4 | I(s)/O | - | - | CAS# | O | DRP07* | I(s)/O | DV0_DATA0 | I(s) | RTS1# | I(s)/O | CC2_Ra1 | I(s) | - | - | - | - | (1) |
| L21 | P7_3 | I(s)/O | - | - | RAS# | O | DRP06* | I(s)/O | DV0_HSYNC | I(s) | TxD1 | O | CC2_Rd1 | I(s) | - | - | - | - | (1) |
| L22 | P7_2 | I(s)/O | - | - | CS4# | O | DV0_CLK | I(s) | LCD0_TCON2 | O | TEND0 | O | CC2_Ra0 | I(s) | - | - | - | - | (1) |
| M1 | P0_2 | I(s)/O | - | - | D2 | I/O | DRP26* | I(s)/O | DV0_DATA19 | I(s) | MTIOC6D | I(s)/O | GTIOC4B | I(s)/O | - | - | - | - | (2) |
| M2 | P0_5 | I(s)/O | - | - | D5 | I/O | DRP29* | I(s)/O | DV0_DATA22 | I(s) | MTIOC7C | I(s)/O | GTIOC7A | I(s)/O | - | - | - | - | (2) |
| M3 | P0_4 | I(s)/O | - | - | D4 | I/O | DRP28* | I(s)/O | DV0_DATA21 | I(s) | MTIOC7B | I(s)/O | GTIOC6B | I(s)/O | - | - | - | - | (2) |
| M4 | P0_3 | I(s)/O | - | - | D3 | I/O | DRP27* | I(s)/O | DV0_DATA20 | I(s) | MTIOC7A | I(s)/O | GTIOC6A | I(s)/O | - | - | - | - | (2) |

Table 2.2        List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function | | Mode Function | | Function 1 | | Function 2 | | Function 3 | | Function 4 | | Function 5 | | Function 6 | | Function 7 | | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | |
| M9 | Vcc | | | | | | | | | | | | | | | | | | |
| M10 | Vss | | | | | | | | | | | | | | | | | | |
| M11 | Vss | | | | | | | | | | | | | | | | | | |
| M12 | Vss | | | | | | | | | | | | | | | | | | |
| M13 | Vss | | | | | | | | | | | | | | | | | | |
| M14 | Vcc | | | | | | | | | | | | | | | | | | |
| M19 | P6_6 | I(s)/ O | - | - | CS2# | O | DRP02* | I(s)/ O | LCD0_ TCON4 | O | DREQ0 | I(s) | CC1_Ra0 | I(s) | - | - | - | - | (1) |
| M20 | P6_0 | I(s)/ O | - | - | ADTRG# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | (1) |
| M21 | P7_0 | I(s)/ O | - | - | WE1#/ DQMU | O | DRP04* | I(s)/ O | DV0_ CLK | I(s) | SCK1 | I(s)/ O | CC1_Rd1 | I(s) | - | - | - | - | (1) |
| M22 | PVcc | | | | | | | | | | | | | | | | | | |
| N1 | PJ_3 | I(s)/ O | - | - | TRACE DATA1 | O | NFDATA0 | I(s)/ O | - | - | RTS1# | I(s)/ O | SSILRCK3 | I(s)/ O | - | - | - | - | (1) |
| N2 | PJ_1 | I(s)/ O | - | - | TRACECTL | O | SPDIF_ IN | I(s) | - | - | RxD1 | I(s) | VBUSIN0 | I(s) | IRQ0 | I(s) | - | - | (1) |
| N3 | P0_6 | I(s)/ O | - | - | D6 | I/O | DRP30* | I(s)/ O | DV0_ DATA23 | I(s) | MTIOC7D | I(s)/ O | GTIOC7B | I(s)/ O | - | - | - | - | (2) |
| N4 | PJ_2 | I(s)/ O | - | - | TRACE DATA0 | O | NFCE# | O | - | - | TxD1 | O | SSITxD3 | O | - | - | - | - | (1) |
| N9 | Vcc | | | | | | | | | | | | | | | | | | |
| N10 | Vss | | | | | | | | | | | | | | | | | | |
| N11 | Vss | | | | | | | | | | | | | | | | | | |
| N12 | Vss | | | | | | | | | | | | | | | | | | |
| N13 | Vss | | | | | | | | | | | | | | | | | | |
| N14 | Vcc | | | | | | | | | | | | | | | | | | |
| N19 | P6_5 | I(s)/ O | - | - | CS3# | O | DRP01* | I(s)/ O | LCD0_ TCON5 | O | AUDIO_ XOUT | O | CC1_Rd0 | I(s) | - | - | - | - | (1) |
| N20 | PG_3 | I(s)/ O | - | - | ET0_COL | I(s) | VIO_D11 | I(s) | SSL00 | I(s)/ O | MTIOC3D | I(s)/ O | GTIOC0B | I(s)/ O | - | - | - | - | (1) |
| N21 | P6_4 | I(s)/ O | - | - | CS5# | O | DRP00* | I(s)/ O | LCD0_ TCON6 | O | AUDIO_ CLK | I(s) | SD1_CD | I(s) | - | - | - | - | (1) |
| N22 | Vss | | | | | | | | | | | | | | | | | | |
| P1 | PH_6 | I(s)/ O | - | - | HM_INT#/ OM_ECS# | I(s) | NFDATA3 | I(s)/ O | ET1_WOL | O | MTIC5V | I(s) | IRQ4 | I(s) | - | - | - | - | (1) |
| P2 | PH_5 | I(s)/ O | - | - | HM_RSTO# | I(s) | NFDATA2 | I(s)/ O | ET1_EXOUT/ ET1_SCLKIN | I(s)/ O | MTIC5U | I(s) | IRQ5 | I(s) | - | - | - | - | (1) |
| P3 | PK_5 | I(s)/ O | - | - | GTETRGA | I(s) | NFDATA1 | I(s)/ O | WDTOVF#/ PERROUT# | O | MTCLKA | I(s) | - | - | - | - | - | - | (1) |
| P4 | PVcc | | | | | | | | | | | | | | | | | | |
| P9 | Vcc | | | | | | | | | | | | | | | | | | |
| P10 | Vss | | | | | | | | | | | | | | | | | | |
| P11 | Vss | | | | | | | | | | | | | | | | | | |
| P12 | Vss | | | | | | | | | | | | | | | | | | |
| P13 | Vss | | | | | | | | | | | | | | | | | | |
| P14 | Vcc | | | | | | | | | | | | | | | | | | |
| P19 | SD0_DAT7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P20 | SD0_RST# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P21 | P6_7 | I(s)/ O | - | - | WE0#/ DQML | O | DRP03* | I(s)/ O | LCD0_ TCON3 | O | DACK0 | O | CC2_Rd0 | I(s) | - | - | - | - | (1) |
| P22 | PVcc_SD0 | | | | | | | | | | | | | | | | | | |
| R1 | PVcc | | | | | | | | | | | | | | | | | | |
| R2 | PJ_4 | I(s)/ O | - | - | TRACE DATA2 | O | NFDATA1 | I(s)/ O | - | - | CTS1# | I(s)/ O | SSIBCK3 | I(s)/ O | - | - | - | - | (1) |
| R3 | PJ_5 | I(s)/ O | - | - | TRACE DATA3 | O | NFDATA2 | I(s)/ O | OVRCUR0 | I(s) | MTIOC1A | I(s)/ O | SSILRCK2 | I(s)/ O | IRQ4 | I(s) | - | - | (1) |
| R4 | Vss | | | | | | | | | | | | | | | | | | |
| R19 | SD0_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R20 | SD0_DAT5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R21 | SD0_DAT4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R22 | SD0_DAT6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T1 | AUDIO_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| T2 | AUDIO_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |

## Table 2.2 List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function | | Mode Function | | Function 1 | | Function 2 | | Function 3 | | Function 4 | | Function 5 | | Function 6 | | Function 7 | | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | |
| T3 | P3_5 | I(s)/O | - | - | ET1_RXD1 | I(s) | NFCLE | O | CC2_Ra0 | I(s) | CAN0TX_DATARATE_EN | O | SSL00 | I(s)/O | - | - | RMII1_RXD1 | I(s) | (1) |
| T4 | P3_2 | I(s)/O | - | - | ET1_CRS | I(s) | NFRE# | O | CC1_Ra1 | I(s) | CAN1RX_DATARATE_EN | O | MOSI2 | I(s)/O | - | - | RMII1_CRS_DV | I(s) | (1) |
| T19 | SD0_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T20 | SD0_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T21 | SD0_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T22 | Vss | | | | | | | | | | | | | | | | | | |
| U1 | Vss | | | | | | | | | | | | | | | | | | |
| U2 | PK_4 | I(s)/O | - | - | ET1_RXD0 | I(s) | NFDATA7 | I(s)/O | OVRCUR1 | I(s) | CAN0TX | O | MISO0 | I(s)/O | IRQ6 | I(s) | RMII1_RXD0 | I(s) | (1) |
| U3 | P3_1 | I(s)/O | - | - | ET1_RXER | I(s) | NFALE | O | VBUSEN0 | I(s) | CAN1RX | I(s) | RSPCK2 | I(s)/O | IRQ6 | I(s) | RMII1_RXER | I(s) | (1) |
| U4 | MIPIAVcc18 | | | | | | | | | | | | | | | | | | |
| U19 | SD1_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| U20 | SD1_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| U21 | SD0_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| U22 | SD0_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| V1 | CSI_CLKP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| V2 | CSI_CLKN | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| V3 | PG_4 | I(s)/O | - | - | ET0_TXER | O | VIO_D15 | I(s) | RSPCK1 | I(s)/O | MTIOC4A | I(s)/O | GTIOC1A | I(s)/O | - | - | - | - | (1) |
| V4 | Vss | | | | | | | | | | | | | | | | | | |
| V19 | P5_4 | I(s) | - | - | AN004 | I(a) | IRQ0 | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | - | - | (3) |
| V20 | SD1_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| V21 | SD1_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| V22 | PVcc_SD1 | | | | | | | | | | | | | | | | | | |
| W1 | CSI_DATA0P | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| W2 | CSI_DATA0N | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| W3 | Vss | | | | | | | | | | | | | | | | | | |
| W4 | PG_6 | I(s)/O | - | - | ET0_RXD2 | I(s) | VIO_D13 | I(s) | MISO1 | I(s)/O | MTIOC4C | I(s)/O | GTIOC2A | I(s)/O | IRQ5 | I(s) | - | - | (1) |
| W5 | P1_0 | I(s)/O | - | - | D7 | I/O | DRP31* | I(s)/O | IRQ0 | I(s) | CAN_CLK | I(s) | VBUSEN0 | O | - | - | - | - | (2) |
| W6 | P1_2 | I(s)/O | - | - | D9 | I/O | MTIOC8B | I(s)/O | IRQ2 | I(s) | CAN0RX_DATARATE_EN | O | VBUSEN1 | O | - | - | - | - | (2) |
| W7 | P2_0 | I(s)/O | - | - | D12 | I/O | GTIOC6A | I(s)/O | IRQ5 | I(s) | CAN1RX | I(s) | OTG_EXICEN0 | O | - | - | - | - | (2) |
| W8 | PC_2 | I(s)/O | - | - | OTG_EXICEN0 | O | NFDATA7 | I(s)/O | ET1_TXD3 | O | MISO2 | I(s)/O | LCD0_TCON5 | O | - | - | - | - | (1) |
| W9 | P4_3 | I(s)/O | - | - | RTS0# | I(s)/O | TXOUT1M | O | SCI_CTS1#/RTS1# | I(s)/O | SSILRCK1 | I(s)/O | MTIOC8D | I(s)/O | IRQ3 | I(s) | - | - | (1) |
| W10 | LVDSAPVcc | | | | | | | | | | | | | | | | | | |
| W11 | Vss | | | | | | | | | | | | | | | | | | |
| W12 | LVDSPLLVcc | | | | | | | | | | | | | | | | | | |
| W13 | USBDPVcc0 | | | | | | | | | | | | | | | | | | |
| W14 | USBVss | | | | | | | | | | | | | | | | | | |
| W15 | Vss | | | | | | | | | | | | | | | | | | |
| W16 | PVcc | | | | | | | | | | | | | | | | | | |
| W17 | Vss | | | | | | | | | | | | | | | | | | |
| W18 | PLLVcc | | | | | | | | | | | | | | | | | | |
| W19 | P5_2 | I(s) | - | - | AN002 | I(a) | IRQ6 | I(s) | VBUSIN0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| W20 | P5_6 | I(s) | - | - | AN006 | I(a) | IRQ2 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| W21 | SD1_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| W22 | Vss | | | | | | | | | | | | | | | | | | |
| Y1 | CSI_DATA1P | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| Y2 | CSI_DATA1N | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |

Table 2.2      List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y3 | Vss | | | | | | | | | | | | | | | | | | |
| Y4 | P3_3 | I(s)/ O | - | - | ET1_MDC | O | NFWE# | O | OTG_ EXICEN0 | O | CAN1TX | O | MISO2 | I(s)/ O | IRQ7 | I(s) | - | - | (1) |
| Y5 | P1_4 | I(s)/ O | - | - | D11 | I/O | MTIOC8D | I(s)/ O | IRQ4 | I(s) | CAN0TX_ DATARATE_ EN | O | VBUSIN0 | I(s) | - | - | - | - | (2) |
| Y6 | PC_0 | I(s)/ O | - | - | VBUSIN1 | I(s) | NFDATA5 | I(s)/ O | ET1_ TXCLK | I(s) | RSPCK2 | I(s)/ O | IRQ2 | I(s) | - | - | - | - | (1) |
| Y7 | P2_2 | I(s)/ O | - | - | D14 | I/O | GTIOC7A | I(s)/ O | IRQ7 | I(s) | CAN1TX | O | VBUSIN1 | I(s) | - | - | - | - | (2) |
| Y8 | P4_2 | I(s)/ O | - | - | TxD0 | O | TXOUT1P | O | SCI_TXD1 | I(s)/ O | SSITxD1 | O | MTIOC8C | I(s)/ O | IRQ2 | I(s) | - | - | (1) |
| Y9 | P4_6 | I(s)/ O | - | - | ET0_EXOUT/ ET0_SCLKIN | I(s)/ O | TXCLK OUTP | O | SCI_TXD0 | I(s)/ O | TxD4 | O | DACK0 | O | - | - | - | - | (1) |
| Y10 | NMI | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| Y11 | Vss | | | | | | | | | | | | | | | | | | |
| Y12 | USBVss | | | | | | | | | | | | | | | | | | |
| Y13 | USBVss | | | | | | | | | | | | | | | | | | |
| Y14 | USBVss | | | | | | | | | | | | | | | | | | |
| Y15 | USBVss | | | | | | | | | | | | | | | | | | |
| Y16 | USBDPVcc1 | | | | | | | | | | | | | | | | | | |
| Y17 | PC_7 | I(s)/ O | - | - | OVRCUR0 | I(s) | NFRB# | I(s) | ET1_RXD3 | I(s) | SD1_WP | I(s) | LCD0_ TCON0 | O | IRQ6 | I(s) | - | - | (1) |
| Y18 | PC_6 | I(s)/ O | - | - | VBUSEN0 | O | NFWE# | O | ET1_RXD2 | I(s) | SD1_CD | I(s) | LCD0_ TCON1 | O | IRQ7 | I(s) | - | - | (1) |
| Y19 | P5_0 | I(s) | - | - | AN000 | I(a) | IRQ4 | I(s) | SD0_CD | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | (3) |
| Y20 | P5_1 | I(s) | - | - | AN001 | I(a) | IRQ5 | I(s) | SD0_WP | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | (3) |
| Y21 | P5_7 | I(s) | - | - | AN007 | I(a) | IRQ3 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| Y22 | SD1_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| AA1 | MIPIAVcc18 | | | | | | | | | | | | | | | | | | |
| AA2 | Vss | | | | | | | | | | | | | | | | | | |
| AA3 | P1_1 | I(s)/ O | - | - | D8 | I/O | MTIOC8A | I(s)/ O | IRQ1 | I(s) | CAN0RX | I(s) | OVRCUR0 | I(s) | - | - | - | - | (2) |
| AA4 | P3_4 | I(s)/ O | - | - | ET1_MDIO | I(s)/ O | NFRB# | I(s) | CC2_Ra1 | I(s) | CAN1TX_ DATARATE_ EN | O | SSL20 | I(s)/ O | - | - | - | - | (1) |
| AA5 | P3_0 | I(s)/ O | - | - | OTG_ EXICEN1 | O | NFDATA4 | I(s)/ O | ET1_ LINKSTA | I(s) | MTIC5W | I(s) | IRQ3 | I(s) | - | - | - | - | (1) |
| AA6 | PC_1 | I(s)/ O | - | - | VBUSIN0 | I(s) | NFDATA6 | I(s)/ O | ET1_TXD2 | O | MOSI2 | I(s)/ O | LCD0_ TCON6 | O | - | - | - | - | (1) |
| AA7 | P4_0 | I(s)/ O | - | - | SCK0 | I(s)/ O | TXOUT0P | O | SCI_SCK1 | I(s)/ O | SSIBCK1 | I(s)/ O | MTIOC8A | I(s)/ O | IRQ0 | I(s) | - | - | (1) |
| AA8 | P4_4 | I(s)/ O | - | - | CTS0# | I(s)/ O | TXOUT2P | O | SCI_CTS0#/ RTS0# | I(s)/ O | WDTOVF#/ PERROUT# | O | OTG_ EXICEN0 | O | - | - | - | - | (1) |
| AA9 | P4_7 | I(s)/ O | - | - | ET0_WOL | O | TXCLK OUTM | O | SCI_SCK0 | I(s)/ O | SCK4 | I(s)/ O | TEND0 | O | - | - | - | - | (1) |
| AA10 | USB_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| AA11 | DP0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| AA12 | USBAPVcc0 | | | | | | | | | | | | | | | | | | |
| AA13 | RREF0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| AA14 | USBVss | | | | | | | | | | | | | | | | | | |
| AA15 | DP1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| AA16 | PVcc | | | | | | | | | | | | | | | | | | |
| AA17 | PC_5 | I(s)/ O | - | - | VBUSEN1 | O | NFRE# | O | ET1_ RXDV | I(s) | SPDIF_ OUT | O | LCD0_ TCON2 | O | IRQ0 | I(s) | - | - | (1) |
| AA18 | XTAL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| AA19 | PC_4 | I(s)/ O | - | - | OTG_ID1 | I(s) | NFALE | O | ET1_ TXER | O | SPDIF_ IN | I(s) | LCD0_ TCON3 | O | IRQ1 | I(s) | - | - | (1) |
| AA20 | RTC_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| AA21 | P5_3 | I(s) | - | - | AN003 | I(a) | IRQ7 | I(s) | OTG_ID0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| AA22 | P5_5 | I(s) | - | - | AN005 | I(a) | IRQ1 | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | - | - | (3) |
| AB1 | Vss | | | | | | | | | | | | | | | | | | |
| AB2 | PG_5 | I(s)/ O | - | - | ET0_RXDV | I(s) | VIO_D14 | I(s) | MOSI1 | I(s)/ O | MTIOC4B | I(s)/ O | GTIOC1B | I(s)/ O | - | - | - | - | (1) |
| AB3 | PG_7 | I(s)/ O | - | - | ET0_RXD3 | I(s) | VIO_D12 | I(s) | SSL10 | I(s)/ O | MTIOC4D | I(s)/ O | GTIOC2B | I(s)/ O | - | - | - | - | (1) |

Table 2.2 List of Pins (324-Pin BGA)

| Ball Number | Port Function/ Dedicated Function | | Mode Function | | Function 1 | | Function 2 | | Function 3 | | Function 4 | | Function 5 | | Function 6 | | Function 7 | | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | |
| AB4 | P1_3 | I(s)/ O | - | - | D10 | I/O | MTIOC8C | I(s)/ O | IRQ3 | I(s) | CAN0TX | O | OTG_ID1 | I(s) | - | - | - | - | (2) |
| AB5 | P2_1 | I(s)/ O | - | - | D13 | I/O | GTIOC6B | I(s)/ O | IRQ6 | I(s) | CAN1RX_ DATARATE_ EN | O | OTG_ID0 | I(s) | - | - | - | - | (2) |
| AB6 | P2_3 | I(s)/ O | - | - | D15 | I/O | GTIOC7B | I(s)/ O | WDTOVF#/ PERROUT# | O | CAN1TX_ DATARATE_ EN | O | OTG_ EXICEN1 | O | - | - | - | - | (2) |
| AB7 | P4_1 | I(s)/ O | - | - | RxD0 | I(s) | TXOUT0M | O | SCI_RXD1 | I(s)/ O | SSIRxD1 | I(s) | MTIOC8B | I(s)/ O | IRQ1 | I(s) | - | - | (1) |
| AB8 | P4_5 | I(s)/ O | - | - | ET0_ LINKSTA | I(s) | TXOUT2M | O | SCI_RXD0 | I(s)/ O | RxD4 | I(s) | DREQ0 | I(s) | - | - | - | - | (1) |
| AB9 | RES# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| AB10 | USB_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| AB11 | DM0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| AB12 | USBA PVcc1 | | | | | | | | | | | | | | | | | | |
| AB13 | RREF1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| AB14 | USBVss | | | | | | | | | | | | | | | | | | |
| AB15 | DM1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| AB16 | PVcc | | | | | | | | | | | | | | | | | | |
| AB17 | PC_3 | I(s)/ O | - | - | OTG_ID0 | I(s) | NFCLE | O | ET1_COL | I(s) | SSL20 | I(s)/ O | LCD0_ TCON4 | O | - | - | - | - | (1) |
| AB18 | EXTAL | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| AB19 | Vss | | | | | | | | | | | | | | | | | | |
| AB20 | RTC_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| AB21 | AVcc | | | | | | | | | | | | | | | | | | |
| AB22 | AVss | | | | | | | | | | | | | | | | | | |

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain

Note: * Only in products with a DRP

Table 2.3         List of Pins (272-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | Vcc | | | | | | | | | | | | | | | | | | |
| A2 | QSPI1_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A3 | QSPI1_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A4 | QSPI1_ SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A5 | QSPI0_SSL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A6 | QSPI0_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A7 | Vss | | | | | | | | | | | | | | | | | | |
| A8 | PVcc | | | | | | | | | | | | | | | | | | |
| A9 | P6_3 | I(s)/ O | - | - | ET0_TXD1 | O | VIO_HD | I(s) | TxD3 | O | POE0# | I(s) | - | - | - | - | RMII0_TXD1 | O | (1) |
| A10 | PE_6 | I(s)/ O | - | - | ET0_MDIO | I(s)/ O | VIO_D2 | I(s) | SSIRxD0 | I(s) | MTIOC0D | I(s)/ O | CC2_Rd1 | I(s) | - | - | - | - | (1) |
| A11 | PL_4 | I(s) | MD_BOOT0 | I(s) | - | - | - | - | - | - | - | - | IRQ0 | I(s) | - | - | - | - | (5) |
| A12 | PL_2 | I(s) | MD_BOOT2 | I(s) | - | - | - | - | - | - | - | - | IRQ6 | I(s) | - | - | - | - | (5) |
| A13 | PL_1 | I(s) | MD_CLK | I(s) | - | - | - | - | - | - | - | - | IRQ5 | I(s) | - | - | - | - | (5) |
| A14 | PF_1 | I(s)/ O | - | - | RxD3 | I(s) | DV0_DATA16 | I(s) | LCD0_DATA7 | O | MTIOC7B | I(s)/ O | MOSI1 | I(s)/ O | IRQ4 | I(s) | - | - | (1) |
| A15 | PE_2 | I(s)/ O | - | - | ET0_RXD1 | I(s) | VIO_D6 | I(s) | TxD2 | O | POE10# | I(s) | - | - | - | - | RMII0_RXD1 | I(s) | (1) |
| A16 | PA_3 | I(s)/ O | - | - | - | - | DV0_DATA10 | I(s) | LCD0_ DATA13 | O | SCI_CTS0#/ RTS0# | I(s)/ O | MTIOC0D | I(s)/ O | - | - | - | - | (1) |
| A17 | PA_6 | I(s)/ O | - | - | - | - | DV0_DATA7 | I(s) | LCD0_ DATA16 | O | SCI_SCK0 | I(s)/ O | MTIOC0A | I(s)/ O | - | - | - | - | (1) |
| A18 | Vss | | | | | | | | | | | | | | | | | | |
| A19 | CKIO | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (11) |
| A20 | Vss | | | | | | | | | | | | | | | | | | |
| B1 | Vss | | | | | | | | | | | | | | | | | | |
| B2 | Vcc | | | | | | | | | | | | | | | | | | |
| B3 | QSPI1_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B4 | RPC_INT# | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B5 | RPC_ RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B6 | QSPI0_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B7 | QSPI0_ SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B8 | P6_1 | I(s)/ O | - | - | ET0_TXEN | O | VIO_CLK | I(s) | SCK3 | I(s)/ O | MTIOC2A | I(s)/ O | - | - | - | - | RMII0_ TXD_EN | O | (1) |
| B9 | PF_5 | I(s)/ O | - | - | TxD2 | O | DV0_DATA20 | I(s) | LCD0_DATA3 | O | MTIOC6B | I(s)/ O | SSILRCK0 | I(s)/ O | - | - | - | - | (1) |
| B10 | PH_1 | I(s)/ O | - | - | AUDIO_XOUT | O | VIO_D0 | I(s) | GTIOC4B | I(s)/ O | MTIOC1B | I(s)/ O | CC2_Rd0 | I(s) | IRQ2 | I(s) | - | - | (1) |
| B11 | PF_3 | I(s)/ O | - | - | SCK2 | I(s)/ O | DV0_DATA18 | I(s) | LCD0_DATA5 | O | MTIOC7D | I(s)/ O | SSL10 | I(s)/ O | - | - | - | - | (1) |
| B12 | PL_0 | I(s) | MD_CLKS | I(s) | - | - | - | - | - | - | - | - | IRQ4 | I(s) | - | - | - | - | (5) |
| B13 | PE_5 | I(s)/ O | - | - | ET0_MDC | O | VIO_D3 | I(s) | SSITxD0 | O | MTIOC0C | I(s)/ O | CC1_Rd1 | I(s) | - | - | - | - | (1) |
| B14 | P8_0 | I(s)/ O | - | - | - | - | DV0_DATA14 | I(s) | LCD0_DATA9 | O | SCI_CTS1#/ RTS1# | I(s)/ O | MTIOC8D | I(s)/ O | - | - | - | - | (1) |
| B15 | PE_3 | I(s)/ O | - | - | ET0_RXER | I(s) | VIO_D5 | I(s) | SSIBCK0 | I(s)/ O | MTIOC0A | I(s)/ O | - | - | - | - | RMII0_RXER | I(s) | (1) |
| B16 | PA_2 | I(s)/ O | - | - | - | - | DV0_DATA11 | I(s) | LCD0_ DATA12 | O | SCI_SCK1 | I(s)/ O | MTIOC8A | I(s)/ O | - | - | - | - | (1) |
| B17 | PA_4 | I(s)/ O | - | - | - | - | DV0_DATA9 | I(s) | LCD0_ DATA14 | O | SCI_TXD0 | I(s)/ O | MTIOC0C | I(s)/ O | - | - | - | - | (1) |
| B18 | PB_0 | I(s)/ O | - | - | - | - | DV0_DATA5 | I(s) | LCD0_ DATA18 | O | SSITxD1 | O | POE8# | I(s) | - | - | - | - | (1) |
| B19 | Vss | | | | | | | | | | | | | | | | | | |
| B20 | PD_6 | I(s)/ O(o) | - | - | RIIC3SCL | I(s)/ O(o) | IRQ6 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| C1 | PH_2 | I(s)/ O | - | - | CTS2# | I(s)/ O | DV0_DATA22 | I(s) | LCD0_DATA1 | O | MTIOC6D | I(s)/ O | SSIRxD0 | I(s) | - | - | - | - | (1) |
| C2 | PK_1 | I(s)/ O | - | - | ET1_TXD0 | O | NFDATA4 | I(s)/ O | CC1_Ra0 | I(s) | CAN_CLK | I(s) | SSIDATA2 | I(s)/ O | - | - | RMII1_TXD0 | O | (1) |

Table 2.3  List of Pins (272-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C3 | Vcc | | | | | | | | | | | | | | | | | | |
| C4 | QSPI1_SSL | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C5 | RPC_WP# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C6 | QSPI0_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C7 | QSPI0_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C8 | PF_6 | I(s)/O | - | - | RTS2# | I(s)/O | DV0_DATA21 | I(s) | LCD0_DATA2 | O | MTIOC6C | I(s)/O | SSITxD0 | O | - | - | - | - | (1) |
| C9 | PE_0 | I(s)/O | - | - | ET0_RXCLK | I(s) | VIO_FLD | I(s) | SCK2 | I(s)/O | POE4# | I(s) | - | - | - | - | REF50CK0 | I(s) | (1) |
| C10 | PF_4 | I(s)/O | - | - | RxD2 | I(s) | DV0_DATA19 | I(s) | LCD0_DATA4 | O | MTIOC6A | I(s)/O | SSIBCK0 | I(s)/O | IRQ1 | I(s) | - | - | (1) |
| C11 | PL_3 | I(s) | MD_BOOT1 | I(s) | - | - | - | - | - | - | - | - | IRQ7 | I(s) | - | - | - | - | (5) |
| C12 | PF_2 | I(s)/O | - | - | TxD3 | O | DV0_DATA17 | I(s) | LCD0_DATA6 | O | MTIOC7C | I(s)/O | MISO1 | I(s)/O | - | - | - | - | (1) |
| C13 | PE_4 | I(s)/O | - | - | ET0_CRS | I(s) | VIO_D4 | I(s) | SSILRCK0 | I(s)/O | MTIOC0B | I(s)/O | - | - | - | - | RMII0_CRS_DV | I(s) | (1) |
| C14 | PA_0 | I(s)/O | - | - | - | - | DV0_DATA13 | I(s) | LCD0_DATA10 | O | SCI_TXD1 | I(s)/O | MTIOC8C | I(s)/O | - | - | - | - | (1) |
| C15 | PE_1 | I(s)/O | - | - | ET0_RXD0 | I(s) | VIO_D7 | I(s) | RxD2 | I(s) | POE8# | I(s) | VBUSIN1 | I(s) | IRQ1 | I(s) | RMII0_RXD0 | I(s) | (1) |
| C16 | PA_5 | I(s)/O | - | - | - | - | DV0_DATA8 | I(s) | LCD0_DATA15 | O | SCI_RXD0 | I(s)/O | MTIOC0B | I(s)/O | IRQ5 | I(s) | - | - | (1) |
| C17 | PG_0 | I(s)/O | - | - | ET0_TXCLK | I(s) | VIO_D8 | I(s) | RSPCK0 | I(s)/O | MTIOC3A | I(s)/O | HM_RSTO# | I(s) | - | - | - | - | (1) |
| C18 | Vss | | | | | | | | | | | | | | | | | | |
| C19 | PD_7 | I(s)/O(o) | - | - | RIIC3SDA | I(s)/O(o) | IRQ7 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| C20 | PD_5 | I(s)/O(o) | - | - | RIIC2SDA | I(s)/O(o) | IRQ5 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D1 | PH_3 | I(s)/O | - | - | HM_RSTO# | I(s) | RTS2# | I(s)/O | GTIOC6A | I(s)/O | MTIOC2A | I(s)/O | SD0_CD | I(s) | IRQ3 | I(s) | - | - | (1) |
| D2 | PK_3 | I(s)/O | - | - | ET1_RXCLK | I(s) | NFDATA6 | I(s)/O | CC2_Rd0 | I(s) | CAN0RX_DATARATE_EN | O | MOSI0 | I(s)/O | - | - | REF50CK1 | I(s) | (1) |
| D3 | PK_2 | I(s)/O | - | - | ET1_TXD1 | O | NFDATA5 | I(s)/O | VBUSEN1 | O | CAN0RX | I(s) | RSPCK0 | I(s)/O | IRQ5 | I(s) | RMII1_TXD1 | O | (1) |
| D4 | Vcc | | | | | | | | | | | | | | | | | | |
| D5 | QSPI1_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D6 | Vss | | | | | | | | | | | | | | | | | | |
| D7 | PVcc_SPI | | | | | | | | | | | | | | | | | | |
| D8 | PK_0 | I(s)/O | - | - | ET1_TXEN | O | NFDATA3 | I(s)/O | CC1_Rd0 | I(s) | MTIOC1B | I(s)/O | SSIBCK2 | I(s)/O | - | - | RMII1_TXD_EN | O | (1) |
| D9 | P6_2 | I(s)/O | - | - | ET0_TXD0 | O | VIO_VD | I(s) | RxD3 | I(s) | MTIOC2B | I(s)/O | OTG_EXICEN1 | O | IRQ0 | I(s) | RMII0_TXD0 | O | (1) |
| D10 | PH_0 | I(s)/O | - | - | AUDIO_CLK | I(s) | VIO_D1 | I(s) | GTIOC4A | I(s)/O | MTIOC1A | I(s)/O | CC1_Rd0 | I(s) | IRQ3 | I(s) | - | - | (1) |
| D11 | PVcc | | | | | | | | | | | | | | | | | | |
| D12 | Vss | | | | | | | | | | | | | | | | | | |
| D13 | PF_0 | I(s)/O | - | - | SCK3 | I(s)/O | DV0_DATA15 | I(s) | LCD0_DATA8 | O | MTIOC7A | I(s)/O | RSPCK1 | I(s)/O | - | - | - | - | (1) |
| D14 | PA_1 | I(s)/O | - | - | - | - | DV0_DATA12 | I(s) | LCD0_DATA11 | O | SCI_RXD1 | I(s)/O | MTIOC8B | I(s)/O | IRQ6 | I(s) | - | - | (1) |
| D15 | PA_7 | I(s)/O | - | - | - | - | DV0_DATA6 | I(s) | LCD0_DATA17 | O | SSIRxD1 | I(s) | POE10# | I(s) | - | - | - | - | (1) |
| D16 | PVcc | | | | | | | | | | | | | | | | | | |
| D17 | Vss | | | | | | | | | | | | | | | | | | |
| D18 | PD_4 | I(s)/O(o) | - | - | RIIC2SCL | I(s)/O(o) | IRQ4 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D19 | PD_3 | I(s)/O(o) | - | - | RIIC1SDA | I(s)/O(o) | IRQ3 | I(s) | MTCLKD | I(s) | GTETRGD | I(s) | - | - | - | - | - | - | (4) |
| D20 | PD_1 | I(s)/O(o) | - | - | RIIC0SDA | I(s)/O(o) | IRQ1 | I(s) | MTCLKB | I(s) | GTETRGB | I(s) | - | - | - | - | - | - | (4) |
| E1 | Vss | | | | | | | | | | | | | | | | | | |
| E2 | BSCANP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |

Table 2.3    List of Pins (272-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E3 | PF_7 | I(s)/O | - | - | GTETRGD | I(s) | DV0_DATA23 | I(s) | LCD0_DATA0 | O | MTCLKD | I(s) | IRQ1 | I(s) | - | - | - | - | (1) |
| E4 | PVcc | | | | | | | | | | | | | | | | | | |
| E17 | PVcc | | | | | | | | | | | | | | | | | | |
| E18 | PD_2 | I(s)/O(o) | - | - | RIIC1SCL | I(s)/O(o) | IRQ2 | I(s) | MTCLKC | I(s) | GTETRGC | I(s) | - | - | - | - | - | - | (4) |
| E19 | TCK/ SWDCLK | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (7) |
| E20 | JP0_0 | I | - | - | TDI | I | - | - | - | - | - | - | - | - | - | - | - | - | (6) |
| F1 | HM_RWDS/ OM_DQS | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F2 | HM_CK# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F3 | HM_CK/ OM_SCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F4 | Vss | | | | | | | | | | | | | | | | | | |
| F17 | TMS/SWDIO | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (9) |
| F18 | PD_0 | I(s)/O(o) | - | - | RIIC0SCL | I(s)/O(o) | IRQ0 | I(s) | MTCLKA | I(s) | GTETRGA | I(s) | - | - | - | - | - | - | (4) |
| F19 | TRST# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| F20 | JP0_1 | O | - | - | TDO/SWO | O | - | - | - | - | - | - | - | - | - | - | - | - | (8) |
| G1 | HM_DQ2/ OM_SIO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G2 | HM_DQ1/ OM_SIO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G3 | HM_CS0#/ OM_CS0# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G4 | PVcc_HO | | | | | | | | | | | | | | | | | | |
| G17 | Vss | | | | | | | | | | | | | | | | | | |
| G18 | PB_1 | I(s)/O | - | - | - | - | DV0_DATA4 | I(s) | LCD0_DATA19 | O | SSILRCK1 | I(s)/O | POE4# | I(s) | - | - | - | - | (1) |
| G19 | PB_2 | I(s)/O | - | - | - | - | DV0_DATA3 | I(s) | LCD0_DATA20 | O | SSIBCK1 | I(s)/O | POE0# | I(s) | - | - | - | - | (1) |
| G20 | PB_3 | I(s)/O | - | - | - | - | DV0_DATA2 | I(s) | LCD0_DATA21 | O | SSIDATA2 | I(s)/O | CTS0# | I(s)/O | - | - | - | - | (1) |
| H1 | HM_DQ3/ OM_SIO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H2 | HM_DQ6/ OM_SIO6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H3 | HM_DQ4/ OM_SIO4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H4 | HM_CS1#/ OM_CS1# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H17 | PVcc | | | | | | | | | | | | | | | | | | |
| H18 | PB_5 | I(s)/O | - | - | - | - | DV0_DATA0 | I(s) | LCD0_DATA23 | O | SSIBCK2 | I(s)/O | TxD0 | O | - | - | - | - | (1) |
| H19 | PB_4 | I(s)/O | - | - | - | - | DV0_DATA1 | I(s) | LCD0_DATA22 | O | SSILRCK2 | I(s)/O | RTS0# | I(s)/O | - | - | - | - | (1) |
| H20 | P7_7 | I(s)/O | - | - | - | - | DV0_HSYNC | I(s) | LCD0_TCON0 | O | GTIOC3B | I(s)/O | RxD0 | I(s) | - | - | - | - | (1) |
| J1 | HM_RESET#/ OM_RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J2 | HM_DQ7/ OM_SIO7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J3 | HM_DQ5/ OM_SIO5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J4 | HM_DQ0/ OM_SIO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J9 | Vcc | | | | | | | | | | | | | | | | | | |
| J10 | Vss | | | | | | | | | | | | | | | | | | |
| J11 | Vss | | | | | | | | | | | | | | | | | | |
| J12 | Vcc | | | | | | | | | | | | | | | | | | |
| J17 | P7_6 | I(s)/O | - | - | - | - | DV0_VSYNC | I(s) | LCD0_TCON1 | O | GTIOC3A | I(s)/O | SCK0 | I(s)/O | - | - | - | - | (1) |
| J18 | PG_2 | I(s)/O | - | - | ET0_TXD3 | O | VIO_D10 | I(s) | MISO0 | I(s)/O | MTIOC3B | I(s)/O | GTIOC0A | I(s)/O | IRQ4 | I(s) | - | - | (1) |

Table 2.3 List of Pins (272-Pin BGA)

| Ball Number | Port Function/Dedicated Function | | Mode Function | | Function 1 | | Function 2 | | Function 3 | | Function 4 | | Function 5 | | Function 6 | | Function 7 | | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | |
| J19 | PG_1 | I(s)/O | - | - | ET0_TXD2 | O | VIO_D9 | I(s) | MOSI0 | I(s)/O | MTIOC3C | I(s)/O | HM_INT#/OM_ECS# | I(s) | - | - | - | - | (1) |
| J20 | P7_2 | I(s)/O | - | - | - | - | DV0_CLK | I(s) | LCD0_TCON2 | O | TEND0 | O | CC2_Ra0 | I(s) | - | - | - | - | (1) |
| K1 | PJ_7 | I(s)/O | - | - | GTETRGB | I(s) | NFDATA0 | I(s)/O | LCD0_EXTCLK | I(s) | MTCLKB | I(s) | - | - | - | - | - | - | (1) |
| K2 | PJ_6 | I(s)/O | - | - | GTETRGC | I(s) | NFCE# | O | LCD0_CLK | O | MTCLKC | I(s) | IRQ0 | I(s) | - | - | - | - | (1) |
| K3 | PH_4 | I(s)/O | - | - | HM_INT#/OM_ECS# | I(s) | CTS2# | I(s)/O | GTIOC6B | I(s)/O | MTIOC2B | I(s)/O | SD0_WP | I(s) | IRQ2 | I(s) | - | - | (1) |
| K4 | PJ_0 | I(s)/O | - | - | TRACECLK | O | SPDIF_OUT | O | - | - | SCK1 | I(s)/O | SSIRxD3 | I(s) | - | - | - | - | (1) |
| K9 | Vcc | | | | | | | | | | | | | | | | | | |
| K10 | Vss | | | | | | | | | | | | | | | | | | |
| K11 | Vss | | | | | | | | | | | | | | | | | | |
| K12 | Vcc | | | | | | | | | | | | | | | | | | |
| K17 | PVcc | | | | | | | | | | | | | | | | | | |
| K18 | PG_3 | I(s)/O | - | - | ET0_COL | I(s) | VIO_D11 | I(s) | SSL00 | I(s)/O | MTIOC3D | I(s)/O | GTIOC0B | I(s)/O | - | - | - | - | (1) |
| K19 | P6_7 | I(s)/O | - | - | - | - | DRP03* | I(s)/O | LCD0_TCON3 | O | DACK0 | O | CC2_Rd0 | I(s) | - | - | - | - | (1) |
| K20 | PVcc | | | | | | | | | | | | | | | | | | |
| L1 | PJ_1 | I(s)/O | - | - | TRACECTL | O | SPDIF_IN | I(s) | - | - | RxD1 | I(s) | VBUSIN0 | I(s) | IRQ0 | I(s) | - | - | (1) |
| L2 | PJ_3 | I(s)/O | - | - | TRACEDATA1 | O | NFDATA0 | I(s)/O | - | - | RTS1# | I(s)/O | SSILRCK3 | I(s)/O | - | - | - | - | (1) |
| L3 | PH_5 | I(s)/O | - | - | HM_RSTO# | I(s) | NFDATA2 | I(s)/O | ET1_EXOUT/ET1_SCLKIN | I(s)/O | MTIC5U | I(s) | IRQ5 | I(s) | - | - | - | - | (1) |
| L4 | PVcc | | | | | | | | | | | | | | | | | | |
| L9 | Vcc | | | | | | | | | | | | | | | | | | |
| L10 | Vss | | | | | | | | | | | | | | | | | | |
| L11 | Vss | | | | | | | | | | | | | | | | | | |
| L12 | Vcc | | | | | | | | | | | | | | | | | | |
| L17 | Vss | | | | | | | | | | | | | | | | | | |
| L18 | P6_0 | I(s)/O | - | - | ADTRG# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | (1) |
| L19 | P6_5 | I(s)/O | - | - | - | - | DRP01* | I(s)/O | LCD0_TCON5 | O | AUDIO_XOUT | O | CC1_Rd0 | I(s) | - | - | - | - | (1) |
| L20 | Vss | | | | | | | | | | | | | | | | | | |
| M1 | PH_6 | I(s)/O | - | - | HM_INT#/OM_ECS# | I(s) | NFDATA3 | I(s)/O | ET1_WOL | O | MTIC5V | I(s) | IRQ4 | I(s) | - | - | - | - | (1) |
| M2 | PJ_2 | I(s)/O | - | - | TRACEDATA0 | O | NFCE# | O | - | - | TxD1 | O | SSITxD3 | O | - | - | - | - | (1) |
| M3 | PK_5 | I(s)/O | - | - | GTETRGA | I(s) | NFDATA1 | I(s)/O | WDTOVF#/PERROUT# | O | MTCLKA | I(s) | - | - | - | - | - | - | (1) |
| M4 | Vss | | | | | | | | | | | | | | | | | | |
| M9 | Vcc | | | | | | | | | | | | | | | | | | |
| M10 | Vss | | | | | | | | | | | | | | | | | | |
| M11 | Vss | | | | | | | | | | | | | | | | | | |
| M12 | Vcc | | | | | | | | | | | | | | | | | | |
| M17 | PVcc_SD0 | | | | | | | | | | | | | | | | | | |
| M18 | P6_4 | I(s)/O | - | - | - | - | DRP00* | I(s)/O | LCD0_TCON6 | O | AUDIO_CLK | I(s) | SD1_CD | I(s) | - | - | - | - | (1) |
| M19 | P6_6 | I(s)/O | - | - | - | - | DRP02* | I(s)/O | LCD0_TCON4 | O | DREQ0 | I(s) | CC1_Ra0 | I(s) | - | - | - | - | (1) |
| M20 | SD0_RST# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| N1 | PVcc | | | | | | | | | | | | | | | | | | |
| N2 | PJ_5 | I(s)/O | - | - | TRACEDATA3 | O | NFDATA2 | I(s)/O | OVRCUR0 | I(s) | MTIOC1A | I(s)/O | SSILRCK2 | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| N3 | PJ_4 | I(s)/O | - | - | TRACEDATA2 | O | NFDATA1 | I(s)/O | - | - | CTS1# | I(s)/O | SSIBCK3 | I(s)/O | - | - | - | - | (1) |
| N4 | PVcc | | | | | | | | | | | | | | | | | | |
| N17 | SD0_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |

Table 2.3 List of Pins (272-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N18 | SD0_DAT5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| N19 | SD0_DAT7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| N20 | SD0_DAT6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P1 | AUDIO_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| P2 | AUDIO_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| P3 | P3_5 | I(s)/O | - | - | ET1_RXD1 | I(s) | NFCLE | O | CC2_Ra0 | I(s) | CAN0TX_ DATARATE_ EN | O | SSL00 | I(s)/O | - | - | RMII1_RXD1 | I(s) | (1) |
| P4 | PK_4 | I(s)/O | - | - | ET1_RXD0 | I(s) | NFDATA7 | I(s)/O | OVRCUR1 | I(s) | CAN0TX | O | MISO0 | I(s)/O | IRQ6 | I(s) | RMII1_RXD0 | I(s) | (1) |
| P17 | PVcc_SD1 | | | | | | | | | | | | | | | | | | |
| P18 | SD0_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P19 | SD0_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P20 | SD0_DAT4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R1 | Vss | | | | | | | | | | | | | | | | | | |
| R2 | P3_1 | I(s)/O | - | - | ET1_RXER | I(s) | NFALE | O | VBUSEN0 | I(s) | CAN1RX | I(s) | RSPCK2 | I(s)/O | IRQ6 | I(s) | RMII1_RXER | I(s) | (1) |
| R3 | PG_4 | I(s)/O | - | - | ET0_TXER | O | VIO_D15 | I(s) | RSPCK1 | I(s)/O | MTIOC4A | I(s)/O | GTIOC1A | I(s)/O | - | - | - | - | (1) |
| R4 | MIPIAVcc18 | | | | | | | | | | | | | | | | | | |
| R17 | Vss | | | | | | | | | | | | | | | | | | |
| R18 | SD0_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R19 | SD0_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R20 | SD0_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T1 | CSI_CLKP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| T2 | CSI_CLKN | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| T3 | P3_2 | I(s)/O | - | - | ET1_CRS | I(s) | NFRE# | O | CC1_Ra1 | I(s) | CAN1RX_ DATARATE_ EN | O | MOSI2 | I(s)/O | - | - | RMII1_ CRS_DV | I(s) | (1) |
| T4 | Vss | | | | | | | | | | | | | | | | | | |
| T17 | AVss | | | | | | | | | | | | | | | | | | |
| T18 | SD1_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T19 | SD1_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T20 | Vss | | | | | | | | | | | | | | | | | | |
| U1 | CSI_DATA0P | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U2 | CSI_DATA0N | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U3 | Vss | | | | | | | | | | | | | | | | | | |
| U4 | PG_6 | I(s)/O | - | - | ET0_RXD2 | I(s) | VIO_D13 | I(s) | MISO1 | I(s)/O | MTIOC4C | I(s)/O | GTIOC2A | I(s)/O | IRQ5 | I(s) | - | - | (1) |
| U5 | PC_0 | I(s)/O | - | - | VBUSIN1 | I(s) | NFDATA5 | I(s)/O | ET1_TXCLK | I(s) | RSPCK2 | I(s)/O | IRQ2 | I(s) | - | - | - | - | (1) |
| U6 | P3_3 | I(s)/O | - | - | ET1_MDC | O | NFWE# | O | OTG_EXICE N0 | O | CAN1TX | O | MISO2 | I(s)/O | IRQ7 | I(s) | - | - | (1) |
| U7 | P4_6 | I(s)/O | - | - | ET0_EXOUT/ ET0_SCLKIN | I(s)/O | TXCLKOUTP | O | SCI_TXD0 | I(s)/O | TxD4 | O | DACK0 | O | - | - | - | - | (1) |
| U8 | LVDSPLLVcc | | | | | | | | | | | | | | | | | | |
| U9 | LVDSAPVcc | | | | | | | | | | | | | | | | | | |
| U10 | USBDPVcc0 | | | | | | | | | | | | | | | | | | |
| U11 | RREF0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U12 | RREF1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U13 | Vss | | | | | | | | | | | | | | | | | | |
| U14 | PLLVcc | | | | | | | | | | | | | | | | | | |
| U15 | PVcc | | | | | | | | | | | | | | | | | | |
| U16 | PC_6 | I(s)/O | - | - | VBUSEN0 | O | NFWE# | O | ET1_RXD2 | I(s) | SD1_CD | I(s) | LCD0_ TCON1 | O | IRQ7 | I(s) | - | - | (1) |
| U17 | AVcc | | | | | | | | | | | | | | | | | | |
| U18 | SD1_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| U19 | SD1_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| U20 | SD1_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |

Table 2.3 List of Pins (272-Pin BGA)

| Ball Number | Port Function/Dedicated Function | | Mode Function | | Function 1 | | Function 2 | | Function 3 | | Function 4 | | Function 5 | | Function 6 | | Function 7 | | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | |
| V1 | CSI_DATA1P | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| V2 | CSI_DATA1N | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| V3 | Vss | | | | | | | | | | | | | | | | | | |
| V4 | P3_4 | I(s)/O | - | - | ET1_MDIO | I(s)/O | NFRB# | I(s) | CC2_Ra1 | I(s) | CAN1TX_DATARATE_EN | O | SSL20 | I(s)/O | - | - | - | - | (1) |
| V5 | PC_2 | I(s)/O | - | - | OTG_EXICEN0 | O | NFDATA7 | I(s)/O | ET1_TXD3 | O | MISO2 | I(s)/O | LCD0_TCON5 | O | - | - | - | - | (1) |
| V6 | P4_2 | I(s)/O | - | - | TxD0 | O | TXOUT1P | O | SCI_TXD1 | I(s)/O | SSITxD1 | O | MTIOC8C | I(s)/O | IRQ2 | I(s) | - | - | (1) |
| V7 | P4_7 | I(s)/O | - | - | ET0_WOL | O | TXCLKOUTM | O | SCI_SCK0 | I(s)/O | SCK4 | I(s)/O | TEND0 | O | - | - | - | - | (1) |
| V8 | Vss | | | | | | | | | | | | | | | | | | |
| V9 | Vss | | | | | | | | | | | | | | | | | | |
| V10 | USBVss | | | | | | | | | | | | | | | | | | |
| V11 | USBVss | | | | | | | | | | | | | | | | | | |
| V12 | USBVss | | | | | | | | | | | | | | | | | | |
| V13 | Vss | | | | | | | | | | | | | | | | | | |
| V14 | PC_3 | I(s)/O | - | - | OTG_ID0 | I(s) | NFCLE | O | ET1_COL | I(s) | SSL20 | I(s)/O | LCD0_TCON4 | O | - | - | - | - | (1) |
| V15 | PC_5 | I(s)/O | - | - | VBUSEN1 | O | NFRE# | O | ET1_RXDV | I(s) | SPDIF_OUT | O | LCD0_TCON2 | O | IRQ0 | I(s) | - | - | (1) |
| V16 | PC_7 | I(s)/O | - | - | OVRCUR0 | I(s) | NFRB# | I(s) | ET1_RXD3 | I(s) | SD1_WP | I(s) | LCD0_TCON0 | O | IRQ6 | I(s) | - | - | (1) |
| V17 | P5_0 | I(s) | - | - | AN000 | I(a) | IRQ4 | I(s) | SD0_CD | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | (3) |
| V18 | P5_6 | I(s) | - | - | AN006 | I(a) | IRQ2 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| V19 | P5_7 | I(s) | - | - | AN007 | I(a) | IRQ3 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| V20 | SD1_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| W1 | MIPIAVcc18 | | | | | | | | | | | | | | | | | | |
| W2 | Vss | | | | | | | | | | | | | | | | | | |
| W3 | PG_5 | I(s)/O | - | - | ET0_RXDV | I(s) | VIO_D14 | I(s) | MOSI1 | I(s)/O | MTIOC4B | I(s)/O | GTIOC1B | I(s)/O | - | - | - | - | (1) |
| W4 | P3_0 | I(s)/O | - | - | OTG_EXICEN1 | O | NFDATA4 | I(s)/O | ET1_LINKSTA | I(s) | MTIC5W | I(s) | IRQ3 | I(s) | - | - | - | - | (1) |
| W5 | P4_1 | I(s)/O | - | - | RxD0 | I(s) | TXOUT0M | O | SCI_RXD1 | I(s)/O | SSIRxD1 | I(s) | MTIOC8B | I(s)/O | IRQ1 | I(s) | - | - | (1) |
| W6 | P4_3 | I(s)/O | - | - | RTS0# | I(s)/O | TXOUT1M | O | SCI_CTS1#/RTS1# | I(s)/O | SSILRCK1 | I(s)/O | MTIOC8D | I(s)/O | IRQ3 | I(s) | - | - | (1) |
| W7 | NMI | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| W8 | USB_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| W9 | USBVss | | | | | | | | | | | | | | | | | | |
| W10 | DP0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| W11 | USBAPVcc0 | | | | | | | | | | | | | | | | | | |
| W12 | USBAPVcc1 | | | | | | | | | | | | | | | | | | |
| W13 | DM1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| W14 | USBDPVcc1 | | | | | | | | | | | | | | | | | | |
| W15 | PC_4 | I(s)/O | - | - | OTG_ID1 | I(s) | NFALE | O | ET1_TXER | O | SPDIF_IN | I(s) | LCD0_TCON3 | O | IRQ1 | I(s) | - | - | (1) |
| W16 | XTAL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| W17 | RTC_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| W18 | P5_4 | I(s) | - | - | AN004 | I(a) | IRQ0 | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | - | - | (3) |
| W19 | P5_3 | I(s) | - | - | AN003 | I(a) | IRQ7 | I(s) | OTG_ID0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| W20 | P5_5 | I(s) | - | - | AN005 | I(a) | IRQ1 | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | - | - | (3) |
| Y1 | Vss | | | | | | | | | | | | | | | | | | |
| Y2 | PG_7 | I(s)/O | - | - | ET0_RXD3 | I(s) | VIO_D12 | I(s) | SSL10 | I(s)/O | MTIOC4D | I(s)/O | GTIOC2B | I(s)/O | - | - | - | - | (1) |
| Y3 | PC_1 | I(s)/O | - | - | VBUSIN0 | I(s) | NFDATA6 | I(s)/O | ET1_TXD2 | O | MOSI2 | I(s)/O | LCD0_TCON6 | O | - | - | - | - | (1) |
| Y4 | P4_0 | I(s)/O | - | - | SCK0 | I(s)/O | TXOUT0P | O | SCI_SCK1 | I(s)/O | SSIBCK1 | I(s)/O | MTIOC8A | I(s)/O | IRQ0 | I(s) | - | - | (1) |

Table 2.3 List of Pins (272-Pin BGA)

| Ball Number | Port Function/Dedicated Function | | Mode Function | | Function 1 | | Function 2 | | Function 3 | | Function 4 | | Function 5 | | Function 6 | | Function 7 | | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | Symbol | I/O | |
| Y5 | P4_4 | I(s)/O | - | - | CTS0# | I(s)/O | TXOUT2P | O | SCI_CTS0#/RTS0# | I(s)/O | WDTOVF#/PERROUT# | O | OTG_EXICEN0 | O | - | - | - | - | (1) |
| Y6 | P4_5 | I(s)/O | - | - | ET0_LINKSTA | I(s) | TXOUT2M | O | SCI_RXD0 | I(s)/O | RxD4 | I(s) | DREQ0 | I(s) | - | - | - | - | (1) |
| Y7 | RES# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| Y8 | USB_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| Y9 | USBVss | | | | | | | | | | | | | | | | | | |
| Y10 | DM0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| Y11 | USBVss | | | | | | | | | | | | | | | | | | |
| Y12 | USBVss | | | | | | | | | | | | | | | | | | |
| Y13 | DP1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| Y14 | USBVss | | | | | | | | | | | | | | | | | | |
| Y15 | EXTAL | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| Y16 | Vss | | | | | | | | | | | | | | | | | | |
| Y17 | RTC_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| Y18 | P5_2 | I(s) | - | - | AN002 | I(a) | IRQ6 | I(s) | VBUSIN0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| Y19 | P5_1 | I(s) | - | - | AN001 | I(a) | IRQ5 | I(s) | SD0_WP | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | (3) |
| Y20 | Vss | | | | | | | | | | | | | | | | | | |

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain

Note: * Only in products with a DRP

Table 2.4         List of Pins (256-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | Vcc | | | | | | | | | | | | | | | | | | |
| A2 | QSPI1_SSL | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A3 | QSPI1_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A4 | QSPI1_ SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A5 | RPC_ RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A6 | PVcc_SPI | | | | | | | | | | | | | | | | | | |
| A7 | Vss | | | | | | | | | | | | | | | | | | |
| A8 | QSPI0_ SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A9 | P6_1 | I(s)/ O | - | - | ET0_TXEN | O | VIO_CLK | I(s) | SCK3 | I(s)/ O | MTIOC2A | I(s)/ O | - | - | - | - | RMII0_ TXD_EN | O | (1) |
| A10 | P6_3 | I(s)/ O | - | - | ET0_TXD1 | O | VIO_HD | I(s) | TxD3 | O | POE0# | I(s) | - | - | - | - | RMII0_TXD1 | O | (1) |
| A11 | PE_6 | I(s)/ O | - | - | ET0_MDIO | I(s)/ O | VIO_D2 | I(s) | SSIRxD0 | I(s) | MTIOC0D | I(s)/ O | CC2_Rd1 | I(s) | - | - | - | - | (1) |
| A12 | PL_4 | I(s) | MD_BOOT0 | I(s) | - | - | - | - | - | - | - | - | IRQ0 | I(s) | - | - | - | - | (5) |
| A13 | PL_0 | I(s) | MD_CLKS | I(s) | - | - | - | - | - | - | - | - | IRQ4 | I(s) | - | - | - | - | (5) |
| A14 | PE_5 | I(s)/ O | - | - | ET0_MDC | O | VIO_D3 | I(s) | SSITxD0 | O | MTIOC0C | I(s)/ O | CC1_Rd1 | I(s) | - | - | - | - | (1) |
| A15 | PE_4 | I(s)/ O | - | - | ET0_CRS | I(s) | VIO_D4 | I(s) | SSILRCK0 | I(s)/ O | MTIOC0B | I(s)/ O | - | - | - | - | RMII0_ CRS_DV | I(s) | (1) |
| A16 | PE_3 | I(s)/ O | - | - | ET0_RXER | I(s) | VIO_D5 | I(s) | SSIBCK0 | I(s)/ O | MTIOC0A | I(s)/ O | - | - | - | - | RMII0_RXER | I(s) | (1) |
| A17 | PA_2 | I(s)/ O | - | - | - | - | DV0_DATA11 | I(s) | LCD0_ DATA12 | O | SCI_SCK1 | I(s)/ O | MTIOC8A | I(s)/ O | - | - | - | - | (1) |
| A18 | PE_1 | I(s)/ O | - | - | ET0_RXD0 | I(s) | VIO_D7 | I(s) | RxD2 | I(s) | POE8# | I(s) | VBUSIN1 | I(s) | IRQ1 | I(s) | RMII0_RXD0 | I(s) | (1) |
| A19 | PA_6 | I(s)/ O | - | - | - | - | DV0_DATA7 | I(s) | LCD0_ DATA16 | O | SCI_SCK0 | I(s)/ O | MTIOC0A | I(s)/ O | - | - | - | - | (1) |
| A20 | CKIO | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (11) |
| A21 | Vss | | | | | | | | | | | | | | | | | | |
| B1 | PK_1 | I(s)/ O | - | - | ET1_TXD0 | O | NFDATA4 | I(s)/ O | CC1_Ra0 | I(s) | CAN_CLK | I(s) | SSIDATA2 | I(s)/ O | - | - | RMII1_TXD0 | O | (1) |
| B2 | Vcc | | | | | | | | | | | | | | | | | | |
| B3 | QSPI1_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B4 | QSPI1_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B5 | RPC_INT# | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B6 | QSPI0_SSL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B7 | QSPI0_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B8 | QSPI0_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B9 | PF_5 | I(s)/ O | - | - | TxD2 | O | DV0_DATA20 | I(s) | LCD0_DATA3 | O | MTIOC6B | I(s)/ O | SSILRCK0 | I(s)/ O | - | - | - | - | (1) |
| B10 | PF_4 | I(s)/ O | - | - | RxD2 | I(s) | DV0_DATA19 | I(s) | LCD0_DATA4 | O | MTIOC6A | I(s)/ O | SSIBCK0 | I(s)/ O | IRQ1 | I(s) | - | - | (1) |
| B11 | PH_1 | I(s)/ O | - | - | AUDIO_XOUT | O | VIO_D0 | I(s) | GTIOC4B | I(s)/ O | MTIOC1B | I(s)/ O | CC2_Rd0 | I(s) | IRQ2 | I(s) | - | - | (1) |
| B12 | PL_1 | I(s) | MD_CLK | I(s) | - | - | - | - | - | - | - | - | IRQ5 | I(s) | - | - | - | - | (5) |
| B13 | PL_2 | I(s) | MD_BOOT2 | I(s) | - | - | - | - | - | - | - | - | IRQ6 | I(s) | - | - | - | - | (5) |
| B14 | P8_0 | I(s)/ O | - | - | - | - | DV0_DATA14 | I(s) | LCD0_DATA9 | O | SCI_CTS1#/ RTS1# | I(s)/ O | MTIOC8D | I(s)/ O | - | - | - | - | (1) |
| B15 | PF_1 | I(s)/ O | - | - | RxD3 | I(s) | DV0_DATA16 | I(s) | LCD0_DATA7 | O | MTIOC7B | I(s)/ O | MOSI1 | I(s)/ O | IRQ4 | I(s) | - | - | (1) |
| B16 | PA_0 | I(s)/ O | - | - | - | - | DV0_DATA13 | I(s) | LCD0_ DATA10 | O | SCI_TXD1 | I(s)/ O | MTIOC8C | I(s)/ O | - | - | - | - | (1) |
| B17 | PA_7 | I(s)/ O | - | - | - | - | DV0_DATA6 | I(s) | LCD0_ DATA17 | O | SSIRxD1 | I(s) | POE10# | I(s) | - | - | - | - | (1) |
| B18 | PA_4 | I(s)/ O | - | - | - | - | DV0_DATA9 | I(s) | LCD0_ DATA14 | O | SCI_TXD0 | I(s)/ O | MTIOC0C | I(s)/ O | - | - | - | - | (1) |
| B19 | PB_0 | I(s)/ O | - | - | - | - | DV0_DATA5 | I(s) | LCD0_ DATA18 | O | SSITxD1 | O | POE8# | I(s) | - | - | - | - | (1) |
| B20 | Vss | | | | | | | | | | | | | | | | | | |
| B21 | PD_3 | I(s)/ O(o) | - | - | RIIC1SDA | I(s)/ O(o) | IRQ3 | I(s) | MTCLKD | I(s) | GTETRGD | I(s) | - | - | - | - | - | - | (4) |
| C1 | PK_3 | I(s)/ O | - | - | ET1_RXCLK | I(s) | NFDATA6 | I(s)/ O | CC2_Rd0 | I(s) | CAN0RX_ DATARATE_ EN | | MOSI0 | I(s)/ O | - | - | REF50CK1 | I(s) | (1) |

## Table 2.4        List of Pins (256-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C2 | PH_2 | I(s)/ O | - | - | CTS2# | I(s)/ O | DV0_DATA22 | I(s) | LCD0_DATA1 | O | MTIOC6D | I(s)/ O | SSIRxD0 | I(s) | - | - | - | - | (1) |
| C20 | PD_7 | I(s)/ O(o) | - | - | RIIC3SDA | I(s)/ O(o) | IRQ7 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| C21 | PD_1 | I(s)/ O(o) | - | - | RIIC0SDA | I(s)/ O(o) | IRQ1 | I(s) | MTCLKB | I(s) | GTETRGB | I(s) | - | - | - | - | - | - | (4) |
| D1 | HM_CK/ OM_SCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D2 | BSCANP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| D4 | Vcc | | | | | | | | | | | | | | | | | | |
| D5 | QSPI1_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D6 | RPC_WP# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D7 | QSPI0_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D8 | PK_0 | I(s)/ O | - | - | ET1_TXEN | O | NFDATA3 | I(s)/ O | CC1_Rd0 | I(s) | MTIOC1B | I(s)/ O | SSIBCK2 | I(s)/ O | - | - | RMII1_ TXD_EN | O | (1) |
| D9 | P6_2 | I(s)/ O | - | - | ET0_TXD0 | O | VIO_VD | I(s) | RxD3 | I(s) | MTIOC2B | I(s)/ O | OTG_ EXICEN1 | O | IRQ0 | I(s) | RMII0_TXD0 | O | (1) |
| D10 | PH_0 | I(s)/ O | - | - | AUDIO_CLK | I(s) | VIO_D1 | I(s) | GTIOC4A | I(s)/ O | MTIOC1A | I(s)/ O | CC1_Rd0 | I(s) | IRQ3 | I(s) | - | - | (1) |
| D11 | PF_3 | I(s)/ O | - | - | SCK2 | I(s)/ O | DV0_DATA18 | I(s) | LCD0_DATA5 | O | MTIOC7D | I(s)/ O | SSL10 | I(s)/ O | - | - | - | - | (1) |
| D12 | PF_2 | I(s)/ O | - | - | TxD3 | O | DV0_DATA17 | I(s) | LCD0_DATA6 | O | MTIOC7C | I(s)/ O | MISO1 | I(s)/ O | - | - | - | - | (1) |
| D13 | PF_0 | I(s)/ O | - | - | SCK3 | I(s)/ O | DV0_DATA15 | I(s) | LCD0_DATA8 | O | MTIOC7A | I(s)/ O | RSPCK1 | I(s)/ O | - | - | - | - | (1) |
| D14 | PE_2 | I(s)/ O | - | - | ET0_RXD1 | I(s) | VIO_D6 | I(s) | TxD2 | O | POE10# | I(s) | - | - | - | - | RMII0_RXD1 | I(s) | (1) |
| D15 | PA_1 | I(s)/ O | - | - | - | - | DV0_DATA12 | I(s) | LCD0_ DATA11 | O | SCI_RXD1 | I(s)/ O | MTIOC8B | I(s)/ O | IRQ6 | I(s) | - | - | (1) |
| D16 | PG_0 | I(s)/ O | - | - | ET0_TXCLK | I(s) | VIO_D8 | I(s) | RSPCK0 | I(s)/ O | MTIOC3A | I(s)/ O | HM_RSTO# | I(s) | - | - | - | - | (1) |
| D17 | PA_5 | I(s)/ O | - | - | - | - | DV0_DATA8 | I(s) | LCD0_ DATA15 | O | SCI_RXD0 | I(s)/ O | MTIOC0B | I(s)/ O | IRQ5 | I(s) | - | - | (1) |
| D18 | Vss | | | | | | | | | | | | | | | | | | |
| D20 | PD_5 | I(s)/ O(o) | - | - | RIIC2SDA | I(s)/ O(o) | IRQ5 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D21 | JP0_0 | I | - | - | TDI | I | - | - | - | - | - | - | - | - | - | - | - | - | (6) |
| E1 | HM_CK# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| E2 | HM_CS0#/ OM_CS0# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| E4 | PK_2 | I(s)/ O | - | - | ET1_TXD1 | O | NFDATA5 | I(s)/ O | VBUSEN1 | O | CAN0RX | I(s) | RSPCK0 | I(s)/ O | IRQ5 | I(s) | RMII1_TXD1 | O | (1) |
| E5 | Vcc | | | | | | | | | | | | | | | | | | |
| E6 | Vss | | | | | | | | | | | | | | | | | | |
| E7 | PVcc | | | | | | | | | | | | | | | | | | |
| E8 | QSPI0_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| E9 | PF_6 | I(s)/ O | - | - | RTS2# | I(s)/ O | DV0_DATA21 | I(s) | LCD0_DATA2 | O | MTIOC6C | I(s)/ O | SSITxD0 | O | - | - | - | - | (1) |
| E10 | PE_0 | I(s)/ O | - | - | ET0_RXCLK | I(s) | VIO_FLD | I(s) | SCK2 | I(s)/ O | POE4# | I(s) | - | - | - | - | REF50CK0 | I(s) | (1) |
| E11 | PL_3 | I(s) | MD_BOOT1 | I(s) | - | - | - | - | - | - | - | - | IRQ7 | I(s) | - | - | - | - | (5) |
| E12 | Vcc | | | | | | | | | | | | | | | | | | |
| E13 | Vss | | | | | | | | | | | | | | | | | | |
| E14 | PVcc | | | | | | | | | | | | | | | | | | |
| E15 | PA_3 | I(s)/ O | - | - | - | - | DV0_DATA10 | I(s) | LCD0_ DATA13 | O | SCI_CTS0#/ RTS0# | I(s)/ O | MTIOC0D | I(s)/ O | - | - | - | - | (1) |
| E16 | Vcc | | | | | | | | | | | | | | | | | | |
| E17 | Vss | | | | | | | | | | | | | | | | | | |
| E18 | TCK/ SWDCLK | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (7) |
| E20 | PD_0 | I(s)/ O(o) | - | - | RIIC0SCL | I(s)/ O(o) | IRQ0 | I(s) | MTCLKA | I(s) | GTETRGA | I(s) | - | - | - | - | - | - | (4) |
| E21 | TRST# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| F1 | HM_DQ1/ OM_SIO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F2 | HM_RWDS/ OM_DQS | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |

### Table 2.4    List of Pins (256-Pin BGA)

| Ball Number | Port Function/Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F4 | PF_7 | I(s)/O | - | - | GTETRGD | I(s) | DV0_DATA23 | I(s) | LCD0_DATA0 | O | MTCLKD | I(s) | IRQ1 | I(s) | - | - | - | - | (1) |
| F5 | Vss | | | | | | | | | | | | | | | | | | |
| F17 | PD_6 | I(s)/O(o) | - | - | RIIC3SCL | I(s)/O(o) | IRQ6 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| F18 | PD_2 | I(s)/O(o) | - | - | RIIC1SCL | I(s)/O(o) | IRQ2 | I(s) | MTCLKC | I(s) | GTETRGC | I(s) | - | - | - | - | - | - | (4) |
| F20 | JP0_1 | O | - | - | TDO/SWO | O | - | - | - | - | - | - | - | - | - | - | - | - | (8) |
| F21 | PB_1 | I(s)/O | - | - | - | - | DV0_DATA4 | I(s) | LCD0_DATA19 | O | SSILRCK1 | I(s)/O | POE4# | I(s) | - | - | - | - | (1) |
| G1 | PVcc_HO | | | | | | | | | | | | | | | | | | |
| G2 | HM_DQ2/OM_SIO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G4 | HM_DQ4/OM_SIO4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G5 | PVcc | | | | | | | | | | | | | | | | | | |
| G17 | PD_4 | I(s)/O(o) | - | - | RIIC2SCL | I(s)/O(o) | IRQ4 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| G18 | TMS/SWDIO | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (9) |
| G20 | PB_3 | I(s)/O | - | - | - | - | DV0_DATA2 | I(s) | LCD0_DATA21 | O | SSIDATA2 | I(s)/O | CTS0# | I(s)/O | - | - | - | - | (1) |
| G21 | PB_5 | I(s)/O | - | - | - | - | DV0_DATA0 | I(s) | LCD0_DATA23 | O | SSIBCK2 | I(s)/O | TxD0 | O | - | - | - | - | (1) |
| H1 | Vss | | | | | | | | | | | | | | | | | | |
| H2 | HM_DQ6/OM_SIO6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H4 | HM_CS1#/OM_CS1# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H5 | PH_3 | I(s)/O | - | - | HM_RSTO# | I(s) | RTS2# | I(s)/O | GTIOC6A | I(s)/O | MTIOC2A | I(s)/O | SD0_CD | I(s) | IRQ3 | I(s) | - | - | (1) |
| H17 | PB_2 | I(s)/O | - | - | - | - | DV0_DATA3 | I(s) | LCD0_DATA20 | O | SSIBCK1 | I(s)/O | POE0# | I(s) | - | - | - | - | (1) |
| H18 | PB_4 | I(s)/O | - | - | - | - | DV0_DATA1 | I(s) | LCD0_DATA22 | O | SSILRCK2 | I(s)/O | RTS0# | I(s)/O | - | - | - | - | (1) |
| H20 | P7_7 | I(s)/O | - | - | - | - | DV0_HSYNC | I(s) | LCD0_TCON0 | O | GTIOC3B | I(s)/O | RxD0 | I(s) | - | - | - | - | (1) |
| H21 | PG_2 | I(s)/O | - | - | ET0_TXD3 | O | VIO_D10 | I(s) | MISO0 | I(s)/O | MTIOC3B | I(s)/O | GTIOC0A | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| J1 | HM_RESET#/OM_RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J2 | PH_4 | I(s)/O | - | - | HM_INT#/OM_ECS# | I(s) | CTS2# | I(s)/O | GTIOC6B | I(s)/O | MTIOC2B | I(s)/O | SD0_WP | I(s) | IRQ2 | I(s) | - | - | (1) |
| J4 | HM_DQ3/OM_SIO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J5 | HM_DQ0/OM_SIO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J17 | PG_1 | I(s)/O | - | - | ET0_TXD2 | O | VIO_D9 | I(s) | MOSI0 | I(s)/O | MTIOC3C | I(s)/O | HM_INT#/OM_ECS# | I(s) | - | - | - | - | (1) |
| J18 | P7_6 | I(s)/O | - | - | - | - | DV0_VSYNC | I(s) | LCD0_TCON1 | O | GTIOC3A | I(s)/O | SCK0 | I(s)/O | - | - | - | - | (1) |
| J20 | P7_2 | I(s)/O | - | - | - | - | DV0_CLK | I(s) | LCD0_TCON2 | O | TEND0 | O | CC2_Ra0 | I(s) | - | - | - | - | (1) |
| J21 | P6_0 | I(s)/O | - | - | ADTRG# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | (1) |
| K1 | PJ_6 | I(s)/O | - | - | GTETRGC | I(s) | NFCE# | O | LCD0_CLK | O | MTCLKC | I(s) | IRQ0 | I(s) | - | - | - | - | (1) |
| K2 | PJ_1 | I(s)/O | - | - | TRACECTL | O | SPDIF_IN | I(s) | - | - | RxD1 | I(s) | VBUSIN0 | I(s) | IRQ0 | I(s) | - | - | (1) |
| K4 | HM_DQ7/OM_SIO7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| K5 | HM_DQ5/OM_SIO5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| K17 | PVcc | | | | | | | | | | | | | | | | | | |
| K18 | PG_3 | I(s)/O | - | - | ET0_COL | I(s) | VIO_D11 | I(s) | SSL00 | I(s)/O | MTIOC3D | I(s)/O | GTIOC0B | I(s)/O | - | - | - | - | (1) |
| K20 | P6_5 | I(s)/O | - | - | - | - | DRP01* | I(s)/O | LCD0_TCON5 | O | AUDIO_XOUT | O | CC1_Rd0 | I(s) | - | - | - | - | (1) |
| K21 | P6_4 | I(s)/O | - | - | - | - | DRP00* | I(s)/O | LCD0_TCON6 | O | AUDIO_CLK | I(s) | SD1_CD | I(s) | - | - | - | - | (1) |
| L1 | PH_5 | I(s)/O | - | - | HM_RSTO# | I(s) | NFDATA2 | I(s)/O | ET1_EXOUT/ET1_SCLKIN | I(s)/O | MTIC5U | I(s) | IRQ5 | I(s) | - | - | - | - | (1) |

Table 2.4 List of Pins (256-Pin BGA)

| Ball Number | Port Function/Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L2 | PJ_3 | I(s)/O | - | - | TRACEDATA1 | O | NFDATA0 | I(s)/O | - | - | RTS1# | I(s)/O | SSILRCK3 | I(s)/O | - | - | - | - | (1) |
| L4 | PJ_0 | I(s)/O | - | - | TRACECLK | O | SPDIF_OUT | O | - | - | SCK1 | I(s)/O | SSIRxD3 | I(s) | - | - | - | - | (1) |
| L5 | Vcc | | | | | | | | | | | | | | | | | | |
| L17 | Vss | | | | | | | | | | | | | | | | | | |
| L18 | P6_7 | I(s)/O | - | - | - | - | DRP03* | I(s)/O | LCD0_TCON3 | O | DACK0 | O | CC2_Rd0 | I(s) | - | - | - | - | (1) |
| L20 | P6_6 | I(s)/O | - | - | - | - | DRP02* | I(s)/O | LCD0_TCON4 | O | DREQ0 | I(s) | CC1_Ra0 | I(s) | - | - | - | - | (1) |
| L21 | SD0_DAT6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| M1 | PH_6 | I(s)/O | - | - | HM_INT#/OM_ECS# | I(s) | NFDATA3 | I(s)/O | ET1_WOL | O | MTIC5V | I(s) | IRQ4 | I(s) | - | - | - | - | (1) |
| M2 | PJ_7 | I(s)/O | - | - | GTETRGB | I(s) | NFDATA0 | I(s)/O | LCD0_EXTCLK | I(s) | MTCLKB | I(s) | - | - | - | - | - | - | (1) |
| M4 | PJ_2 | I(s)/O | - | - | TRACEDATA0 | O | NFCE# | O | - | - | TxD1 | O | SSITxD3 | O | - | - | - | - | (1) |
| M5 | Vss | | | | | | | | | | | | | | | | | | |
| M17 | Vcc | | | | | | | | | | | | | | | | | | |
| M18 | SD0_RST# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| M20 | SD0_DAT7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| M21 | PVcc_SD0 | | | | | | | | | | | | | | | | | | |
| N1 | P3_5 | I(s)/O | - | - | ET1_RXD1 | I(s) | NFCLE | O | CC2_Ra0 | I(s) | CAN0TX_DATARATE_EN | O | SSL00 | I(s)/O | - | - | RMII1_RXD1 | I(s) | (1) |
| N2 | PJ_5 | I(s)/O | - | - | TRACEDATA3 | O | NFDATA2 | I(s)/O | OVRCUR0 | I(s) | MTIOC1A | I(s)/O | SSILRCK2 | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| N4 | PJ_4 | I(s)/O | - | - | TRACEDATA2 | O | NFDATA1 | I(s)/O | - | - | CTS1# | I(s)/O | SSIBCK3 | I(s)/O | - | - | - | - | (1) |
| N5 | PK_5 | I(s)/O | - | - | GTETRGA | I(s) | NFDATA1 | I(s)/O | WDTOVF#/PERROUT# | O | MTCLKA | I(s) | - | - | - | - | - | - | (1) |
| N17 | SD0_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| N18 | SD0_DAT5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| N20 | SD0_DAT4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| N21 | Vss | | | | | | | | | | | | | | | | | | |
| P1 | AUDIO_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| P2 | AUDIO_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| P4 | PK_4 | I(s)/O | - | - | ET1_RXD0 | I(s) | NFDATA7 | I(s)/O | OVRCUR1 | I(s) | CAN0TX | O | MISO0 | I(s)/O | IRQ6 | I(s) | RMII1_RXD0 | I(s) | (1) |
| P5 | PVcc | | | | | | | | | | | | | | | | | | |
| P17 | SD0_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P18 | SD0_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P20 | SD0_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| P21 | SD0_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R1 | PG_4 | I(s)/O | - | - | ET0_TXER | O | VIO_D15 | I(s) | RSPCK1 | I(s)/O | MTIOC4A | I(s)/O | GTIOC1A | I(s)/O | - | - | - | - | (1) |
| R2 | P3_1 | I(s)/O | - | - | ET1_RXER | I(s) | NFALE | O | VBUSEN0 | I(s) | CAN1RX | I(s) | RSPCK2 | I(s)/O | IRQ6 | I(s) | RMII1_RXER | I(s) | (1) |
| R4 | P3_2 | I(s)/O | - | - | ET1_CRS | I(s) | NFRE# | O | CC1_Ra1 | I(s) | CAN1RX_DATARATE_EN | O | MOSI2 | I(s)/O | - | - | RMII1_CRS_DV | I(s) | (1) |
| R5 | Vss | | | | | | | | | | | | | | | | | | |
| R17 | SD1_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R18 | SD1_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R20 | SD1_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| R21 | SD0_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T1 | Vss | | | | | | | | | | | | | | | | | | |
| T2 | Vss | | | | | | | | | | | | | | | | | | |
| T4 | MIPIAVcc18 | | | | | | | | | | | | | | | | | | |
| T5 | Vcc | | | | | | | | | | | | | | | | | | |
| T17 | SD1_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T18 | SD1_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T20 | SD1_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| T21 | PVcc_SD1 | | | | | | | | | | | | | | | | | | |

Table 2.4 List of Pins (256-Pin BGA)

| Ball Number | Port Function/Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U1 | CSI_DATA0P | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U2 | CSI_DATA0N | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U4 | Vss | | | | | | | | | | | | | | | | | | |
| U5 | PVcc | | | | | | | | | | | | | | | | | | |
| U6 | Vss | | | | | | | | | | | | | | | | | | |
| U7 | LVDSAPVcc | | | | | | | | | | | | | | | | | | |
| U8 | P4_3 | I(s)/O | - | - | RTS0# | I(s)/O | TXOUT1M | O | SCI_CTS1#/ RTS1# | I(s)/O | SSILRCK1 | I(s)/O | MTIOC8D | I(s)/O | IRQ3 | I(s) | - | - | (1) |
| U9 | P4_7 | I(s)/O | - | - | ET0_WOL | O | TXCLKOUTM | O | SCI_SCK0 | I(s)/O | SCK4 | I(s)/O | TEND0 | O | - | - | - | - | (1) |
| U10 | USBVss | | | | | | | | | | | | | | | | | | |
| U11 | RREF0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U12 | RREF1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| U13 | USBVss | | | | | | | | | | | | | | | | | | |
| U14 | Vss | | | | | | | | | | | | | | | | | | |
| U15 | PLLVcc | | | | | | | | | | | | | | | | | | |
| U16 | PVcc | | | | | | | | | | | | | | | | | | |
| U17 | Vss | | | | | | | | | | | | | | | | | | |
| U18 | P5_4 | I(s) | - | - | AN004 | I(a) | IRQ0 | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | - | - | (3) |
| U20 | P5_5 | I(s) | - | - | AN005 | I(a) | IRQ1 | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | - | - | (3) |
| U21 | Vss | | | | | | | | | | | | | | | | | | |
| V1 | CSI_CLKP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| V2 | CSI_CLKN | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| V4 | PG_6 | I(s)/O | - | - | ET0_RXD2 | I(s) | VIO_D13 | I(s) | MISO1 | I(s)/O | MTIOC4C | I(s)/O | GTIOC2A | I(s)/O | IRQ5 | I(s) | - | - | (1) |
| V5 | P3_3 | I(s)/O | - | - | ET1_MDC | O | NFWE# | O | OTG_EXICEN0 | O | CAN1TX | O | MISO2 | I(s)/O | IRQ7 | I(s) | - | - | (1) |
| V6 | PC_2 | I(s)/O | - | - | OTG_EXICEN0 | O | NFDATA7 | I(s)/O | ET1_TXD3 | O | MISO2 | I(s)/O | LCD0_TCON5 | O | - | - | - | - | (1) |
| V7 | Vss | | | | | | | | | | | | | | | | | | |
| V8 | P4_2 | I(s)/O | - | - | TxD0 | O | TXOUT1P | O | SCI_TXD1 | I(s)/O | SSITxD1 | O | MTIOC8C | I(s)/O | IRQ2 | I(s) | - | - | (1) |
| V9 | P4_6 | I(s)/O | - | - | ET0_EXOUT/ ET0_SCLKIN | I(s)/O | TXCLKOUTP | O | SCI_TXD0 | I(s)/O | TxD4 | O | DACK0 | O | - | - | - | - | (1) |
| V10 | Vss | | | | | | | | | | | | | | | | | | |
| V11 | USBAPVcc0 | | | | | | | | | | | | | | | | | | |
| V12 | USBAPVcc1 | | | | | | | | | | | | | | | | | | |
| V13 | USBVss | | | | | | | | | | | | | | | | | | |
| V14 | PC_4 | I(s)/O | - | - | OTG_ID1 | I(s) | NFALE | O | ET1_TXER | O | SPDIF_IN | I(s) | LCD0_TCON3 | O | IRQ1 | I(s) | - | - | (1) |
| V15 | PC_6 | I(s)/O | - | - | VBUSEN0 | O | NFWE# | O | ET1_RXD2 | I(s) | SD1_CD | I(s) | LCD0_TCON1 | O | IRQ7 | I(s) | - | - | (1) |
| V16 | PC_3 | I(s)/O | - | - | OTG_ID0 | I(s) | NFCLE | O | ET1_COL | I(s) | SSL20 | I(s)/O | LCD0_TCON4 | O | - | - | - | - | (1) |
| V17 | PVcc | | | | | | | | | | | | | | | | | | |
| V18 | P5_0 | I(s) | - | - | AN000 | I(a) | IRQ4 | I(s) | SD0_CD | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | (3) |
| V20 | P5_6 | I(s) | - | - | AN006 | I(a) | IRQ2 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| V21 | P5_7 | I(s) | - | - | AN007 | I(a) | IRQ3 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| W1 | CSI_DATA1P | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| W2 | CSI_DATA1N | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| W20 | P5_2 | I(s) | - | - | AN002 | I(a) | IRQ6 | I(s) | VBUSIN0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| W21 | P5_3 | I(s) | - | - | AN003 | I(a) | IRQ7 | I(s) | OTG_ID0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| Y1 | Vss | | | | | | | | | | | | | | | | | | |
| Y2 | Vss | | | | | | | | | | | | | | | | | | |
| Y3 | PG_7 | I(s)/O | - | - | ET0_RXD3 | I(s) | VIO_D12 | I(s) | SSL10 | I(s)/O | MTIOC4D | I(s)/O | GTIOC2B | I(s)/O | - | - | - | - | (1) |
| Y4 | PC_0 | I(s)/O | - | - | VBUSIN1 | I(s) | NFDATA5 | I(s)/O | ET1_TXCLK | I(s) | RSPCK2 | I(s)/O | IRQ2 | I(s) | - | - | - | - | (1) |
| Y5 | PC_1 | I(s)/O | - | - | VBUSIN0 | I(s) | NFDATA6 | I(s)/O | ET1_TXD2 | O | MOSI2 | I(s)/O | LCD0_TCON6 | O | - | - | - | - | (1) |
| Y6 | P4_0 | I(s)/O | - | - | SCK0 | I(s)/O | TXOUT0P | O | SCI_SCK1 | I(s)/O | SSIBCK1 | I(s)/O | MTIOC8A | I(s)/O | IRQ0 | I(s) | - | - | (1) |

Table 2.4 List of Pins (256-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y7 | P4_4 | I(s)/O | - | - | CTS0# | I(s)/O | TXOUT2P | O | SCI_CTS0#/ RTS0# | I(s)/O | WDTOVF#/ PERROUT# | O | OTG_ EXICEN0 | O | - | - | - | - | (1) |
| Y8 | LVDSPLLVcc | | | | | | | | | | | | | | | | | | |
| Y9 | NMI | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| Y10 | USB_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| Y11 | USBDPVcc0 | | | | | | | | | | | | | | | | | | |
| Y12 | DP0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| Y13 | USBVss | | | | | | | | | | | | | | | | | | |
| Y14 | DP1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| Y15 | USBDPVcc1 | | | | | | | | | | | | | | | | | | |
| Y16 | Vss | | | | | | | | | | | | | | | | | | |
| Y17 | XTAL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| Y18 | RTC_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| Y19 | AVcc | | | | | | | | | | | | | | | | | | |
| Y20 | PVcc | | | | | | | | | | | | | | | | | | |
| Y21 | P5_1 | I(s) | - | - | AN001 | I(a) | IRQ5 | I(s) | SD0_WP | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | (3) |
| AA1 | Vss | | | | | | | | | | | | | | | | | | |
| AA2 | PG_5 | I(s)/O | - | - | ET0_RXDV | I(s) | VIO_D14 | I(s) | MOSI1 | I(s)/O | MTIOC4B | I(s)/O | GTIOC1B | I(s)/O | - | - | - | - | (1) |
| AA3 | P3_4 | I(s)/O | - | - | ET1_MDIO | I(s)/O | NFRB# | I(s) | CC2_Ra1 | I(s) | CAN1TX_ DATARATE_ EN | O | SSL20 | I(s)/O | - | - | - | - | (1) |
| AA4 | P3_0 | I(s)/O | - | - | OTG_ EXICEN1 | O | NFDATA4 | I(s)/O | ET1_ LINKSTA | I(s) | MTIC5W | I(s) | IRQ3 | I(s) | - | - | - | - | (1) |
| AA5 | Vss | | | | | | | | | | | | | | | | | | |
| AA6 | P4_1 | I(s)/O | - | - | RxD0 | I(s) | TXOUT0M | O | SCI_RXD1 | I(s)/O | SSIRxD1 | I(s) | MTIOC8B | I(s)/O | IRQ1 | I(s) | - | - | (1) |
| AA7 | P4_5 | I(s)/O | - | - | ET0_ LINKSTA | I(s) | TXOUT2M | O | SCI_RXD0 | I(s)/O | RxD4 | I(s) | DREQ0 | I(s) | - | - | - | - | (1) |
| AA8 | Vss | | | | | | | | | | | | | | | | | | |
| AA9 | RES# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| AA10 | USB_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| AA11 | USBVss | | | | | | | | | | | | | | | | | | |
| AA12 | DM0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| AA13 | USBVss | | | | | | | | | | | | | | | | | | |
| AA14 | DM1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| AA15 | USBVss | | | | | | | | | | | | | | | | | | |
| AA16 | PC_5 | I(s)/O | - | - | VBUSEN1 | O | NFRE# | O | ET1_RXDV | I(s) | SPDIF_OUT | O | LCD0_TCON2 | O | IRQ0 | I(s) | - | - | (1) |
| AA17 | PC_7 | I(s)/O | - | - | OVRCUR0 | I(s) | NFRB# | I(s) | ET1_RXD3 | I(s) | SD1_WP | I(s) | LCD0_TCON0 | O | IRQ6 | I(s) | - | - | (1) |
| AA18 | EXTAL | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| AA19 | RTC_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| AA20 | AVss | | | | | | | | | | | | | | | | | | |
| AA21 | PVcc | | | | | | | | | | | | | | | | | | |

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain
Note: * Only in products with a DRP

Table 2.5 List of Pins (176-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | Vss | | | | | | | | | | | | | | | | | | |
| A2 | PK_3 | I(s)/ O | - | - | - | - | NFDATA6 | I(s)/ O | CC2_Rd0 | I(s) | CAN0RX_ DATARATE_ EN | O | MOSI0 | I(s)/ O | - | - | REF50CK1 | I(s) | (1) |
| A3 | QSPI1_ SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A4 | RPC_WP# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A5 | PVcc_SPI | | | | | | | | | | | | | | | | | | |
| A6 | Vss | | | | | | | | | | | | | | | | | | |
| A7 | QSPI0_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| A8 | P6_1 | I(s)/ O | - | - | ET0_TXEN | O | VIO_CLK | I(s) | SCK3 | I(s)/ O | MTIOC2A | I(s)/ O | - | - | - | - | RMII0_ TXD_EN | O | (1) |
| A9 | P6_2 | I(s)/ O | - | - | ET0_TXD0 | O | VIO_VD | I(s) | RxD3 | I(s) | MTIOC2B | I(s)/ O | OTG_ EXICEN1 | O | IRQ0 | I(s) | RMII0_TXD0 | O | (1) |
| A10 | PH_1 | I(s)/ O | - | - | AUDIO_XOUT | O | VIO_D0 | I(s) | GTIOC4B | I(s)/ O | MTIOC1B | I(s)/ O | CC2_Rd0 | I(s) | IRQ2 | I(s) | - | - | (1) |
| A11 | PE_6 | I(s)/ O | - | - | ET0_MDIO | I(s)/ O | VIO_D2 | I(s) | SSIRxD0 | I(s) | MTIOC0D | I(s)/ O | CC2_Rd1 | I(s) | - | - | - | - | (1) |
| A12 | PL_2 | I(s) | MD_BOOT2 | I(s) | - | - | - | - | - | - | - | - | IRQ6 | I(s) | - | - | - | - | (5) |
| A13 | PE_3 | I(s)/ O | - | - | ET0_RXER | I(s) | VIO_D5 | I(s) | SSIBCK0 | I(s)/ O | MTIOC0A | I(s)/ O | - | - | - | - | RMII0_RXER | I(s) | (1) |
| A14 | CKIO | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (11) |
| A15 | Vss | | | | | | | | | | | | | | | | | | |
| B1 | BSCANP | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| B2 | PH_3 | I(s)/ O | - | - | HM_RSTO# | I(s) | RTS2# | I(s)/ O | GTIOC6A | I(s)/ O | MTIOC2A | I(s)/ O | SD0_CD | I(s) | IRQ3 | I(s) | - | - | (1) |
| B3 | QSPI1_SSL | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B4 | QSPI1_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B5 | RPC_RESET # | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B6 | QSPI0_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B7 | QSPI0_IO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| B8 | PK_0 | I(s)/ O | - | - | - | - | NFDATA3 | I(s)/ O | CC1_Rd0 | I(s) | MTIOC1B | I(s)/ O | SSIBCK2 | I(s)/ O | - | - | RMII1_ TXD_EN | O | (1) |
| B9 | P6_3 | I(s)/ O | - | - | ET0_TXD1 | O | VIO_HD | I(s) | TxD3 | O | POE0# | I(s) | - | - | - | - | RMII0_TXD1 | O | (1) |
| B10 | PL_4 | I(s) | MD_BOOT0 | I(s) | - | - | - | - | - | - | - | - | IRQ0 | I(s) | - | - | - | - | (5) |
| B11 | PL_0 | I(s) | MD_CLKS | I(s) | - | - | - | - | - | - | - | - | IRQ4 | I(s) | - | - | - | - | (5) |
| B12 | PE_5 | I(s)/ O | - | - | ET0_MDC | O | VIO_D3 | I(s) | SSITxD0 | O | MTIOC0C | I(s)/ O | CC1_Rd1 | I(s) | - | - | - | - | (1) |
| B13 | PE_1 | I(s)/ O | - | - | ET0_RXD0 | I(s) | VIO_D7 | I(s) | RxD2 | I(s) | POE8# | I(s) | VBUSIN1 | I(s) | IRQ1 | I(s) | RMII0_RXD0 | I(s) | (1) |
| B14 | Vss | | | | | | | | | | | | | | | | | | |
| B15 | PD_7 | I(s)/ O(o) | - | - | RIIC3SDA | I(s)/ O(o) | IRQ7 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| C1 | HM_CK/OM_ SCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C2 | PK_1 | I(s)/ O | - | - | - | - | NFDATA4 | I(s)/ O | CC1_Ra0 | I(s) | CAN_CLK | I(s) | SSIDATA2 | I(s)/ O | - | - | RMII1_TXD0 | O | (1) |
| C3 | QSPI1_IO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C4 | QSPI1_IO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C5 | RPC_INT# | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C6 | QSPI0_SSL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C7 | QSPI0_ SPCLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| C8 | PE_0 | I(s)/ O | - | - | ET0_RXCLK | I(s) | VIO_FLD | I(s) | SCK2 | I(s)/ O | POE4# | I(s) | - | - | - | - | REF50CK0 | I(s) | (1) |
| C9 | PH_0 | I(s)/ O | - | - | AUDIO_CLK | I(s) | VIO_D1 | I(s) | GTIOC4A | I(s)/ O | MTIOC1A | I(s)/ O | CC1_Rd0 | I(s) | IRQ3 | I(s) | - | - | (1) |
| C10 | PL_1 | I(s) | MD_CLK | I(s) | - | - | - | - | - | - | - | - | IRQ5 | I(s) | - | - | - | - | (5) |
| C11 | PE_4 | I(s)/ O | - | - | ET0_CRS | I(s) | VIO_D4 | I(s) | SSILRCK0 | I(s)/ O | MTIOC0B | I(s)/ O | - | - | - | - | RMII0_ CRS_DV | I(s) | (1) |
| C12 | PG_0 | I(s)/ O | - | - | ET0_TXCLK | I(s) | VIO_D8 | I(s) | RSPCK0 | I(s)/ O | MTIOC3A | I(s)/ O | HM_RSTO# | I(s) | - | - | - | - | (1) |
| C13 | Vss | | | | | | | | | | | | | | | | | | |
| C14 | PD_5 | I(s)/ O(o) | - | - | RIIC2SDA | I(s)/ O(o) | IRQ5 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |

Table 2.5     List of Pins (176-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C15 | PD_3 | I(s)/O(o) | - | - | RIIC1SDA | I(s)/O(o) | IRQ3 | I(s) | MTCLKD | I(s) | GTETRGD | I(s) | - | - | - | - | - | - | (4) |
| D1 | HM_CK# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D2 | HM_CS0#/ OM_CS0# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D3 | PK_2 | I(s)/O | - | - | - | - | NFDATA5 | I(s)/O | VBUSEN1 | O | CAN0RX | I(s) | RSPCK0 | I(s)/O | IRQ5 | I(s) | RMII1_TXD1 | O | (1) |
| D4 | Vss | | | | | | | | | | | | | | | | | | |
| D5 | Vcc | | | | | | | | | | | | | | | | | | |
| D6 | QSPI1_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D7 | QSPI0_IO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| D8 | PVcc | | | | | | | | | | | | | | | | | | |
| D9 | PL_3 | I(s) | MD_BOOT1 | I(s) | - | - | - | - | - | - | - | - | IRQ7 | I(s) | - | - | - | - | (5) |
| D10 | PE_2 | I(s)/O | - | - | ET0_RXD1 | I(s) | VIO_D6 | I(s) | TxD2 | O | POE10# | I(s) | - | - | - | - | RMII0_RXD1 | I(s) | (1) |
| D11 | PVcc | | | | | | | | | | | | | | | | | | |
| D12 | Vss | | | | | | | | | | | | | | | | | | |
| D13 | PD_6 | I(s)/O(o) | - | - | RIIC3SCL | I(s)/O(o) | IRQ6 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D14 | PD_4 | I(s)/O(o) | - | - | RIIC2SCL | I(s)/O(o) | IRQ4 | I(s) | - | - | - | - | - | - | - | - | - | - | (4) |
| D15 | PD_1 | I(s)/O(o) | - | - | RIIC0SDA | I(s)/O(o) | IRQ1 | I(s) | MTCLKB | I(s) | GTETRGB | I(s) | - | - | - | - | - | - | (4) |
| E1 | Vss | | | | | | | | | | | | | | | | | | |
| E2 | HM_DQ0/ OM_SIO0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| E3 | HM_RWDS/ OM_DQS | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| E4 | PVcc | | | | | | | | | | | | | | | | | | |
| E12 | PD_2 | I(s)/O(o) | - | - | RIIC1SCL | I(s)/O(o) | IRQ2 | I(s) | MTCLKC | I(s) | GTETRGC | I(s) | - | - | - | - | - | - | (4) |
| E13 | PD_0 | I(s)/O(o) | - | - | RIIC0SCL | I(s)/O(o) | IRQ0 | I(s) | MTCLKA | I(s) | GTETRGA | I(s) | - | - | - | - | - | - | (4) |
| E14 | TCK/ SWDCLK | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (7) |
| E15 | JP0_0 | I(s) | - | - | TDI | I | - | - | - | - | - | - | - | - | - | - | - | - | (6) |
| F1 | PVcc_HO | | | | | | | | | | | | | | | | | | |
| F2 | HM_DQ2/ OM_SIO2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F3 | HM_DQ1/ OM_SIO1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F4 | HM_CS1#/ OM_CS1# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| F12 | TMS/SWDIO | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (9) |
| F13 | JP0_1 | O | - | - | TDO/SWO | O | - | - | - | - | - | - | - | - | - | - | - | - | (8) |
| F14 | TRST# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| F15 | P6_0 | I(s)/O | - | - | ADTRG# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | (1) |
| G1 | HM_DQ4/ OM_SIO4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G2 | HM_DQ7/ OM_SIO7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G3 | HM_DQ5/ OM_SIO5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G4 | HM_DQ3/ OM_SIO3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| G12 | Vcc | | | | | | | | | | | | | | | | | | |
| G13 | PG_3 | I(s)/O | - | - | ET0_COL | I(s) | VIO_D11 | I(s) | SSL00 | I(s)/O | MTIOC3D | I(s)/O | GTIOC0B | I(s)/O | - | - | - | - | (1) |
| G14 | PG_2 | I(s)/O | - | - | ET0_TXD3 | O | VIO_D10 | I(s) | MISO0 | I(s)/O | MTIOC3B | I(s)/O | GTIOC0A | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| G15 | PVcc | | | | | | | | | | | | | | | | | | |
| H1 | HM_DQ6/ OM_SIO6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H2 | HM_RESET#/ OM_RESET# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H3 | PH_4 | I(s)/O | - | - | HM_INT#/ OM_ECS# | I(s) | CTS2# | I(s)/O | GTIOC6B | I(s)/O | MTIOC2B | I(s)/O | SD0_WP | I(s) | IRQ2 | I(s) | - | - | (1) |

Table 2.5 List of Pins (176-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H4 | Vcc | | | | | | | | | | | | | | | | | | |
| H12 | PG_1 | I(s)/O | - | - | ET0_TXD2 | O | VIO_D9 | I(s) | MOSI0 | I(s)/O | MTIOC3C | I(s)/O | HM_INT#/OM_ECS# | I(s) | - | - | - | - | (1) |
| H13 | SD0_DAT5 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H14 | SD0_RST# | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| H15 | Vss | | | | | | | | | | | | | | | | | | |
| J1 | PJ_0 | I(s)/O | - | - | TRACECLK | O | SPDIF_OUT | O | - | - | SCK1 | I(s)/O | SSIRxD3 | I(s) | - | - | - | - | (1) |
| J2 | PJ_1 | I(s)/O | - | - | TRACECTL | O | SPDIF_IN | I(s) | - | - | RxD1 | I(s) | VBUSIN0 | I(s) | IRQ0 | I(s) | - | - | (1) |
| J3 | PJ_2 | I(s)/O | - | - | TRACE DATA0 | O | NFCE# | O | - | - | TxD1 | O | SSITxD3 | O | - | - | - | - | (1) |
| J4 | Vss | | | | | | | | | | | | | | | | | | |
| J12 | SD0_DAT7 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J13 | SD0_DAT2 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J14 | SD0_DAT4 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| J15 | PVcc_SD0 | | | | | | | | | | | | | | | | | | |
| K1 | PJ_5 | I(s)/O | - | - | TRACE DATA3 | O | NFDATA2 | I(s)/O | OVRCUR0 | I(s) | MTIOC1A | I(s)/O | SSILRCK2 | I(s)/O | IRQ4 | I(s) | - | - | (1) |
| K2 | PJ_3 | I(s)/O | - | - | TRACE DATA1 | O | NFDATA0 | I(s)/O | - | - | RTS1# | I(s)/O | SSILRCK3 | I(s)/O | - | - | - | - | (1) |
| K3 | PJ_4 | I(s)/O | - | - | TRACE DATA2 | O | NFDATA1 | I(s)/O | - | - | CTS1# | I(s)/O | SSIBCK3 | I(s)/O | - | - | - | - | (1) |
| K4 | PVcc | | | | | | | | | | | | | | | | | | |
| K12 | SD0_CLK | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| K13 | SD0_DAT3 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| K14 | SD0_DAT0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| K15 | SD0_DAT6 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| L1 | PK_4 | I(s)/O | - | - | - | - | NFDATA7 | I(s)/O | OVRCUR1 | I(s) | CAN0TX | O | MISO0 | I(s)/O | IRQ6 | I(s) | RMII1_RXD0 | I(s) | (1) |
| L2 | P3_5 | I(s)/O | - | - | - | - | NFCLE | O | CC2_Ra0 | I(s) | CAN0TX_DATARATE_EN | O | SSL00 | I(s)/O | - | - | RMII1_RXD1 | I(s) | (1) |
| L3 | Vss | | | | | | | | | | | | | | | | | | |
| L4 | Vcc | | | | | | | | | | | | | | | | | | |
| L12 | PVcc | | | | | | | | | | | | | | | | | | |
| L13 | Vss | | | | | | | | | | | | | | | | | | |
| L14 | SD0_DAT1 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| L15 | SD0_CMD | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (15) |
| M1 | AUDIO_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| M2 | AUDIO_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| M3 | P3_2 | I(s)/O | - | - | - | - | NFRE# | O | CC1_Ra1 | I(s) | CAN1RX_DATARATE_EN | O | MOSI2 | I(s)/O | - | - | RMII1_CRS_DV | I(s) | (1) |
| M4 | Vss | | | | | | | | | | | | | | | | | | |
| M5 | P3_3 | I(s)/O | - | - | ET1_MDC | O | NFWE# | O | OTG_EXICEN0 | O | CAN1TX | O | MISO2 | I(s)/O | IRQ7 | I(s) | - | - | (1) |
| M6 | LVDSAPVcc | | | | | | | | | | | | | | | | | | |
| M7 | LVDSPLLVcc | | | | | | | | | | | | | | | | | | |
| M8 | NMI | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (10) |
| M9 | USBVss | | | | | | | | | | | | | | | | | | |
| M10 | PVcc | | | | | | | | | | | | | | | | | | |
| M11 | Vcc | | | | | | | | | | | | | | | | | | |
| M12 | P5_0 | I(s) | - | - | AN000 | I(a) | IRQ4 | I(s) | SD0_CD | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | (3) |
| M13 | P5_4 | I(s) | - | - | AN004 | I(a) | IRQ0 | I(s) | SD1_CD | I(s) | - | - | - | - | - | - | - | - | (3) |
| M14 | P5_7 | I(s) | - | - | AN007 | I(a) | IRQ3 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| M15 | P5_5 | I(s) | - | - | AN005 | I(a) | IRQ1 | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | - | - | (3) |
| N1 | P3_1 | I(s)/O | - | - | - | - | NFALE | O | VBUSEN0 | I(s) | CAN1RX | I(s) | RSPCK2 | I(s)/O | IRQ6 | I(s) | RMII1_RXER | I(s) | (1) |
| N2 | PG_4 | I(s)/O | - | - | ET0_TXER | O | VIO_D15 | I(s) | RSPCK1 | I(s)/O | MTIOC4A | I(s)/O | GTIOC1A | I(s)/O | - | - | - | - | (1) |
| N3 | Vss | | | | | | | | | | | | | | | | | | |
| N4 | PG_7 | I(s)/O | - | - | ET0_RXD3 | I(s) | VIO_D12 | I(s) | SSL10 | I(s)/O | MTIOC4D | I(s)/O | GTIOC2B | I(s)/O | - | - | - | - | (1) |

Table 2.5 List of Pins (176-Pin BGA)

| Ball Number | Port Function/ Dedicated Function Symbol | I/O | Mode Function Symbol | I/O | Function 1 Symbol | I/O | Function 2 Symbol | I/O | Function 3 Symbol | I/O | Function 4 Symbol | I/O | Function 5 Symbol | I/O | Function 6 Symbol | I/O | Function 7 Symbol | I/O | Simplified Circuit Diagram Figure 2.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N5 | P4_2 | I(s)/O | - | - | TxD0 | O | TXOUT1P | O | SCI_TXD1 | I(s)/O | SSITxD1 | O | MTIOC8C | I(s)/O | IRQ2 | I(s) | - | - | (1) |
| N6 | P4_3 | I(s)/O | - | - | RTS0# | I(s)/O | TXOUT1M | O | SCI_CTS1#/ RTS1# | I(s)/O | SSILRCK1 | I(s)/O | MTIOC8D | I(s)/O | IRQ3 | I(s) | - | - | (1) |
| N7 | P4_6 | I(s)/O | - | - | ET0_EXOUT/ ET0_SCLKIN | I(s)/O | TXCLK OUTP | O | SCI_TXD0 | I(s)/O | TxD4 | O | DACK0 | O | - | - | - | - | (1) |
| N8 | RES# | I(s) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (12) |
| N9 | RREF0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| N10 | Vss | | | | | | | | | | | | | | | | | | |
| N11 | PLLVcc | | | | | | | | | | | | | | | | | | |
| N12 | Vcc | | | | | | | | | | | | | | | | | | |
| N13 | P5_2 | I(s) | - | - | AN002 | I(a) | IRQ6 | I(s) | VBUSIN0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| N14 | P5_3 | I(s) | - | - | AN003 | I(a) | IRQ7 | I(s) | OTG_ID0 | I(s) | - | - | - | - | - | - | - | - | (3) |
| N15 | P5_6 | I(s) | - | - | AN006 | I(a) | IRQ2 | I(s) | - | - | - | - | - | - | - | - | - | - | (3) |
| P1 | PVcc | | | | | | | | | | | | | | | | | | |
| P2 | Vss | | | | | | | | | | | | | | | | | | |
| P3 | PG_6 | I(s)/O | - | - | ET0_RXD2 | I(s) | VIO_D13 | I(s) | MISO1 | I(s)/O | MTIOC4C | I(s)/O | GTIOC2A | I(s)/O | IRQ5 | I(s) | - | - | (1) |
| P4 | P4_0 | I(s)/O | - | - | SCK0 | I(s)/O | TXOUT0P | O | SCI_SCK1 | I(s)/O | SSIBCK1 | I(s)/O | MTIOC8A | I(s)/O | IRQ0 | I(s) | - | - | (1) |
| P5 | P4_4 | I(s)/O | - | - | CTS0# | I(s)/O | TXOUT2P | O | SCI_CTS0#/ RTS0# | I(s)/O | WDTOVF#/ PERROUT# | O | OTG_ EXICEN0 | O | - | - | - | - | (1) |
| P6 | P4_7 | I(s)/O | - | - | ET0_WOL | O | TXCLK OUTM | O | SCI_SCK0 | I(s)/O | SCK4 | I(s)/O | TEND0 | O | - | - | - | - | (1) |
| P7 | USB_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| P8 | USBDPVcc0 | | | | | | | | | | | | | | | | | | |
| P9 | USBAPVcc0 | | | | | | | | | | | | | | | | | | |
| P10 | USBVss | | | | | | | | | | | | | | | | | | |
| P11 | XTAL | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| P12 | RTC_X2 | O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| P13 | AVcc | | | | | | | | | | | | | | | | | | |
| P14 | Vcc | | | | | | | | | | | | | | | | | | |
| P15 | P5_1 | I(s) | - | - | AN001 | I(a) | IRQ5 | I(s) | SD0_WP | I(s) | SD1_WP | I(s) | - | - | - | - | - | - | (3) |
| R1 | Vss | | | | | | | | | | | | | | | | | - | - | |
| R2 | PG_5 | I(s)/O | - | - | ET0_RXDV | I(s) | VIO_D14 | I(s) | MOSI1 | I(s)/O | MTIOC4B | I(s)/O | GTIOC1B | I(s)/O | - | - | - | - | (1) |
| R3 | P3_4 | I(s)/O | - | - | ET1_MDIO | I(s)/O | NFRB# | I(s) | CC2_Ra1 | I(s) | CAN1TX_ DATARATE_ EN | O | SSL20 | I(s)/O | - | - | - | - | (1) |
| R4 | P4_1 | I(s)/O | - | - | RxD0 | I(s) | TXOUT0M | O | SCI_RXD1 | I(s)/O | SSIRxD1 | I(s) | MTIOC8B | I(s)/O | IRQ1 | I(s) | - | - | (1) |
| R5 | P4_5 | I(s)/O | - | - | ET0_LINKSTA | I(s) | TXOUT2M | O | SCI_RXD0 | I(s)/O | RxD4 | I(s) | DREQ0 | I(s) | - | - | - | - | (1) |
| R6 | Vss | | | | | | | | | | | | | | | | | | |
| R7 | USB_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| R8 | DP0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R9 | DM0 | I/O | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| R10 | USBVss | | | | | | | | | | | | | | | | | | |
| R11 | EXTAL | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (13) |
| R12 | Vss | | | | | | | | | | | | | | | | | | |
| R13 | RTC_X1 | I | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | (14) |
| R14 | AVss | | | | | | | | | | | | | | | | | | |
| R15 | Vcc | | | | | | | | | | | | | | | | | | |

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain

P3_0 to P3_5                    PC_0 to PC_7
P4_0 to P4_7 (except LVDS output)    PE_0 to PE_6
P6_0 to P6_7                    PF_0 to PF_7
P7_0 to P7_7                    PG_0 to PG_7
P8_0 to P8_7                    PH_0 to PH_6
P9_0 to P9_7                    PJ_0 to PJ_7
PA_0 to PA_7                    PK_0 to PK_5
PB_0 to PB_5

Internal bus

DSCR[1:0]

PDR[1:0]            2        [0]
                            [1]

PODR

ISEL bit

PMR

PIDR

Input signal of peripheral module/interrupt
Peripheral module output enable signal
Peripheral module output signal
Peripheral module input enable signal
Latch control

Figure 2.1        (1) Input/Output Buffer with Schmitt AND Input and Latch
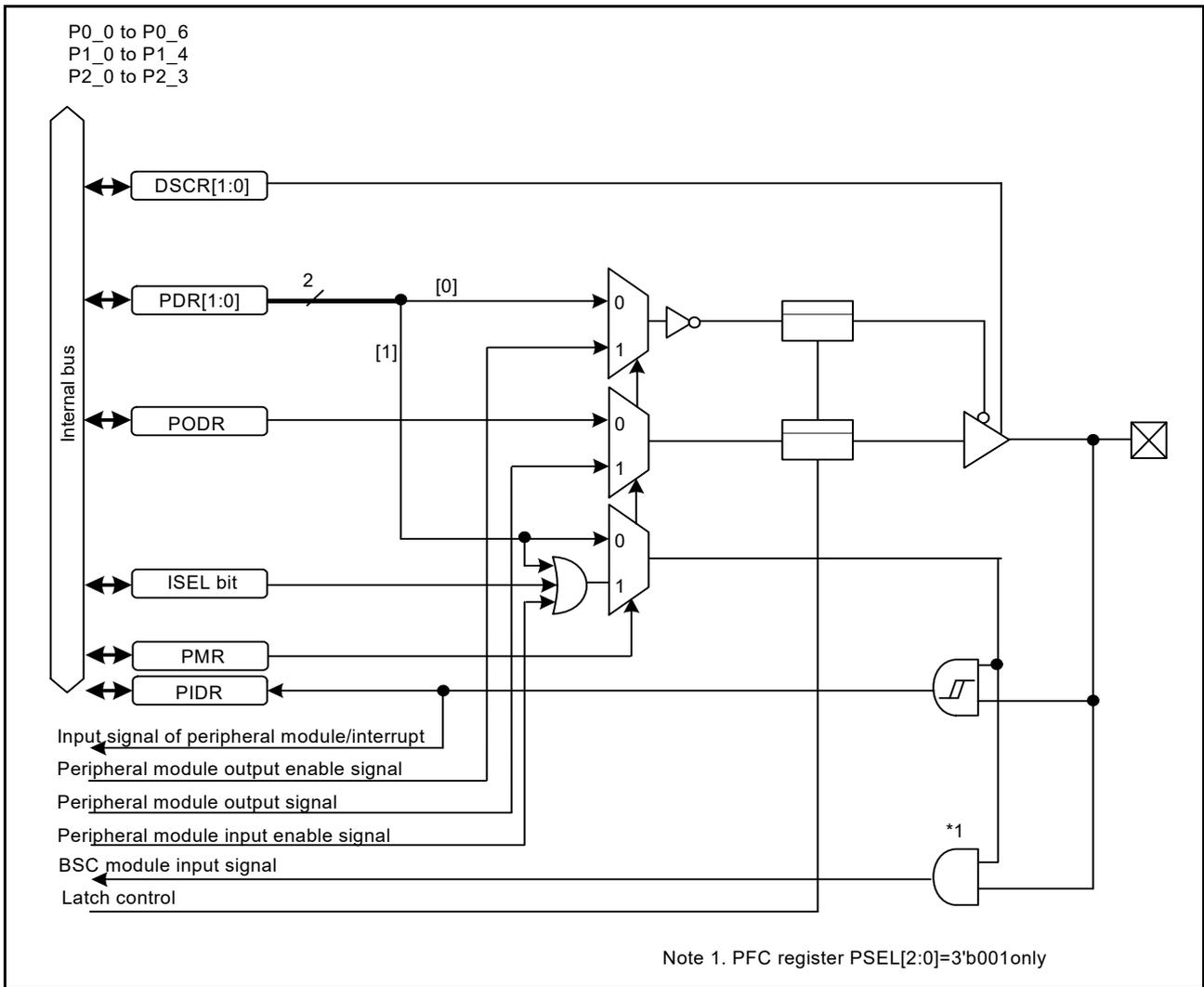
Figure 2.1       (2) Input/Output Buffer with TTL AND Input, Schmitt AND Input, and Latch
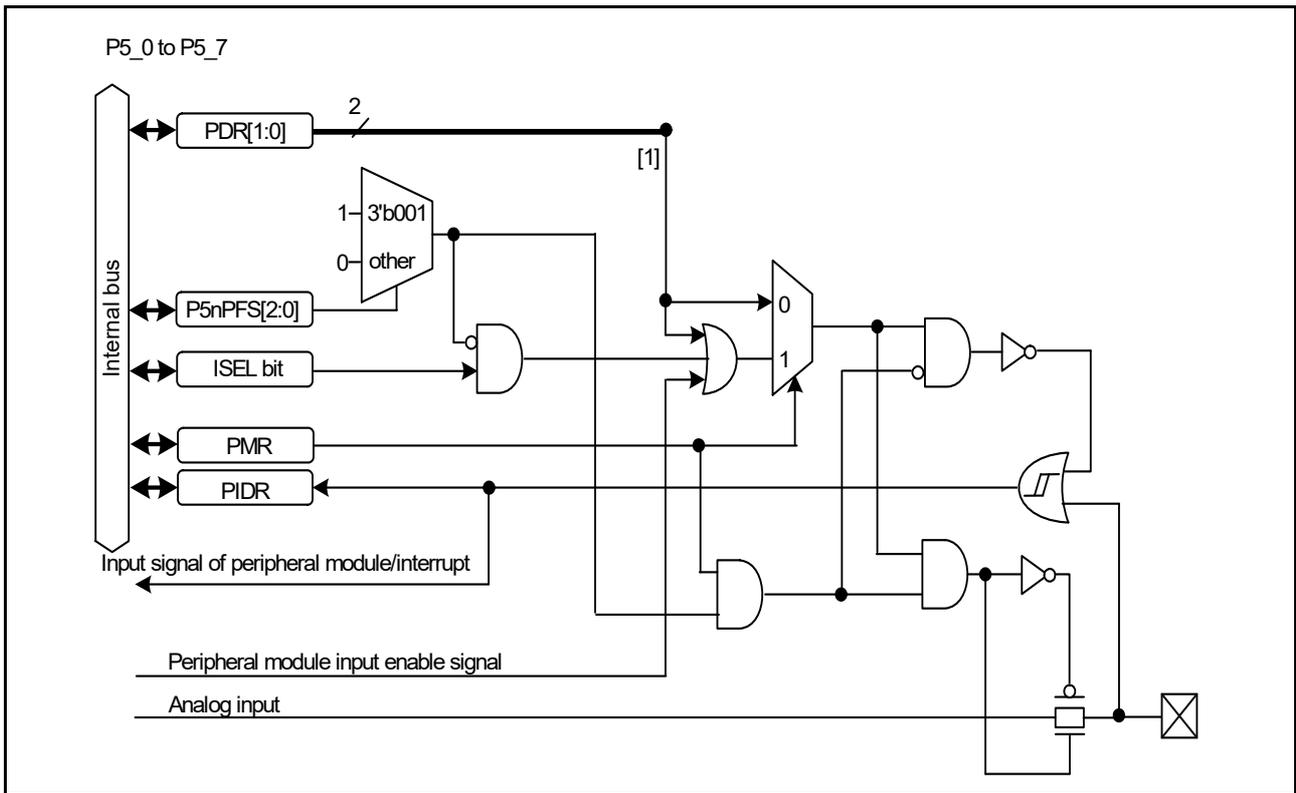
Figure 2.1          (3) Input Buffer Multiplexed with Schmitt OR Input and A/D Input
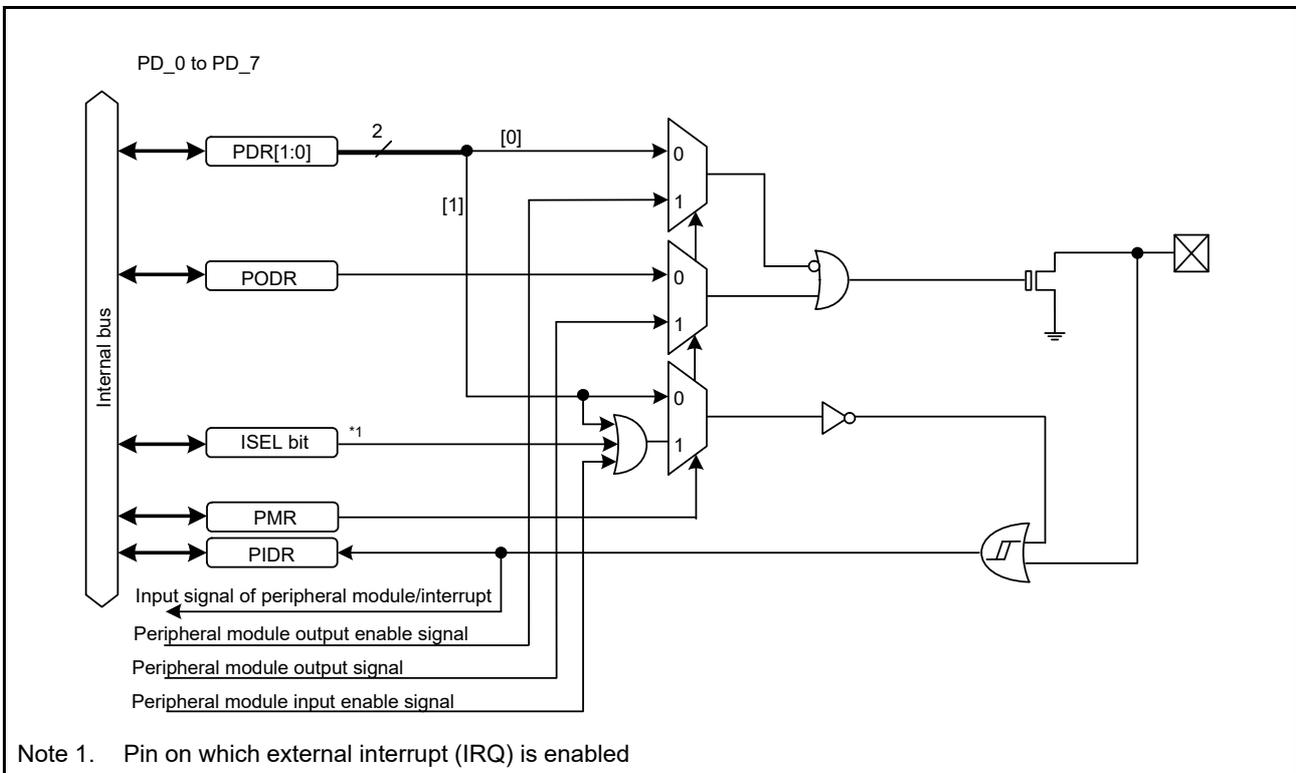


Note 1.     Pin on which external interrupt (IRQ) is enabled

Figure 2.1          (4) Bidirectional Buffer with Schmitt OR Input and Open-Drain Output

Note 1.   Pin on which external interrupt (IRQ) is enabled
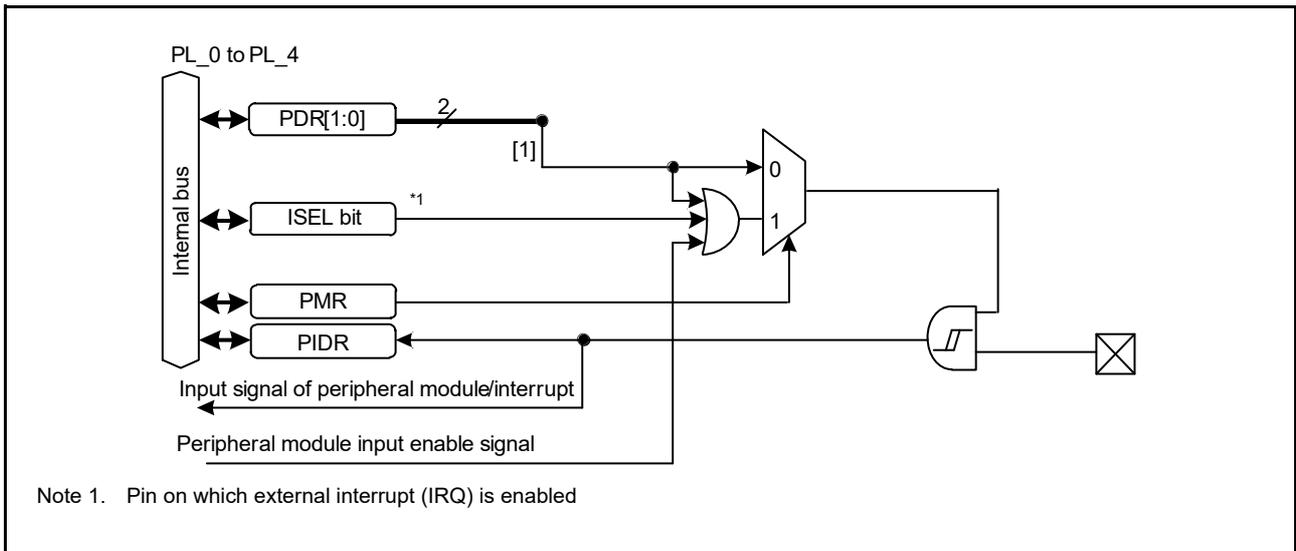
Figure 2.1        (5) Schmitt AND Input Buffer



Note 1.   Pin on which external interrupt (IRQ) is enabled
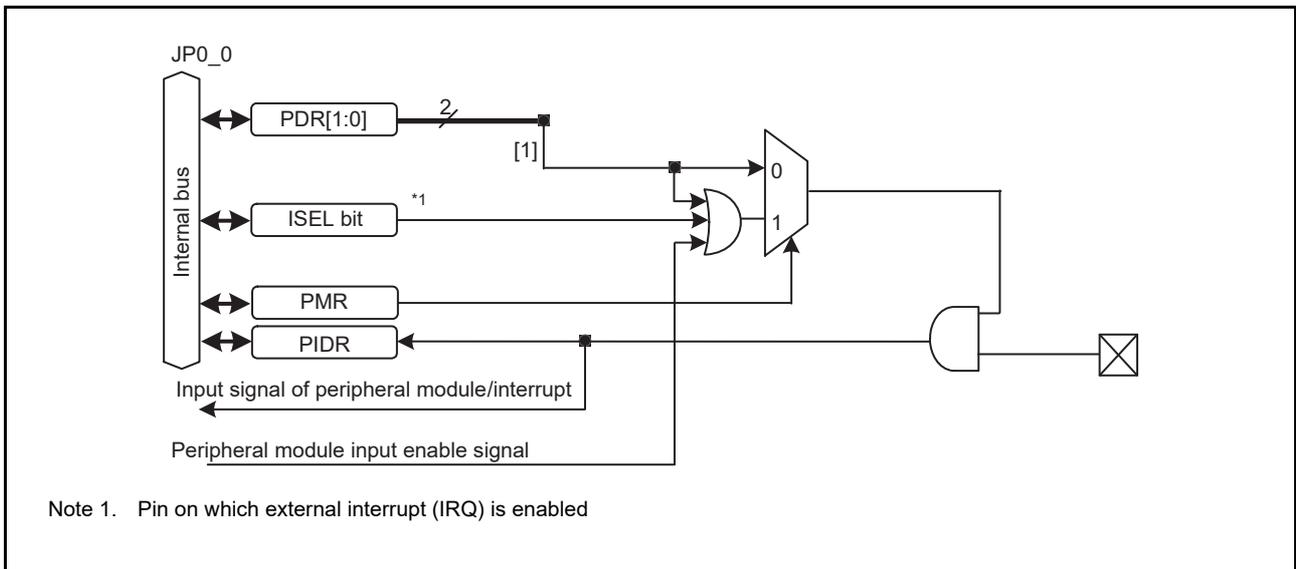
Figure 2.1        (6) TTL AND Input Buffer
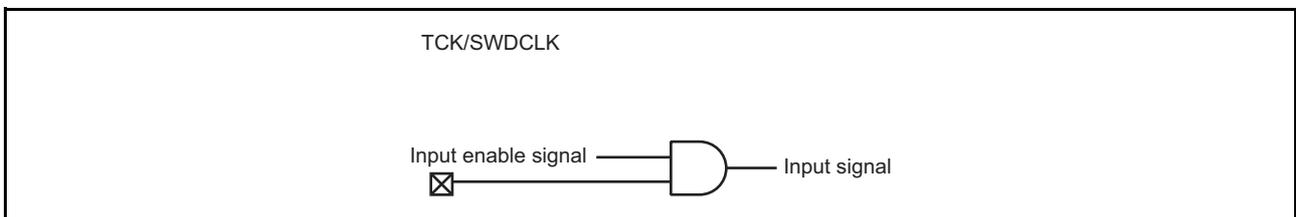


Figure 2.1        (7) TTL AND Input Buffer
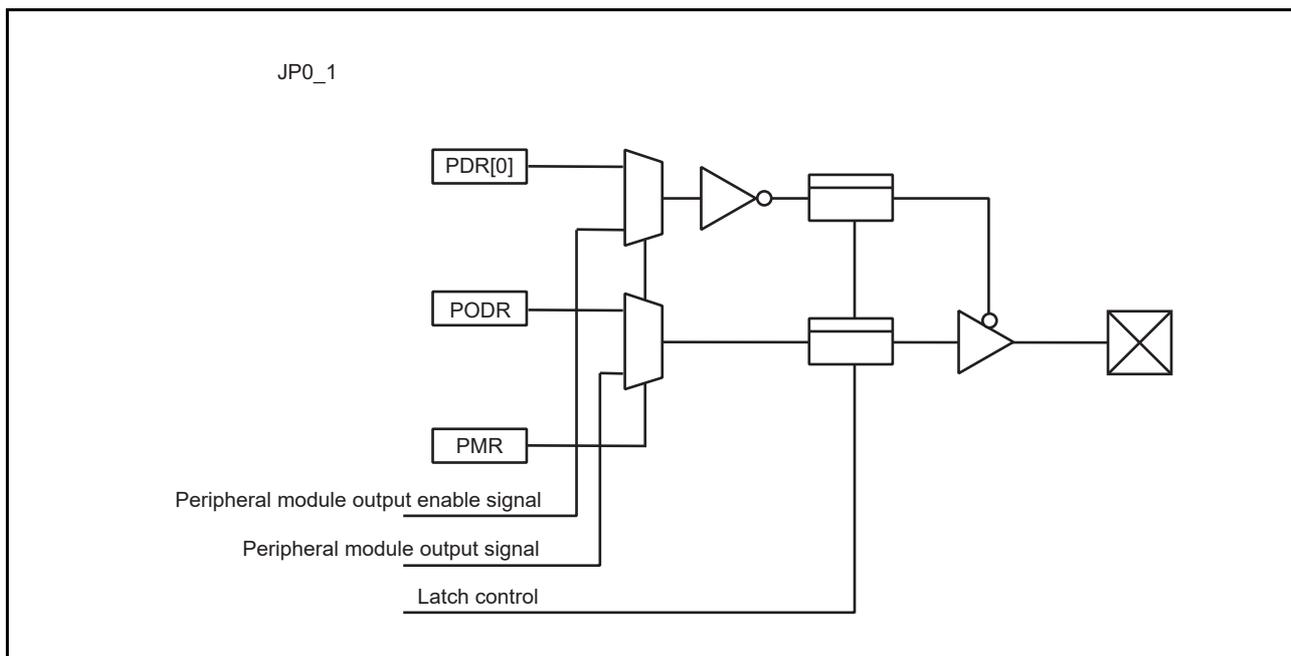
Figure 2.1        (8) Output Buffer with Latch and Enable Signal
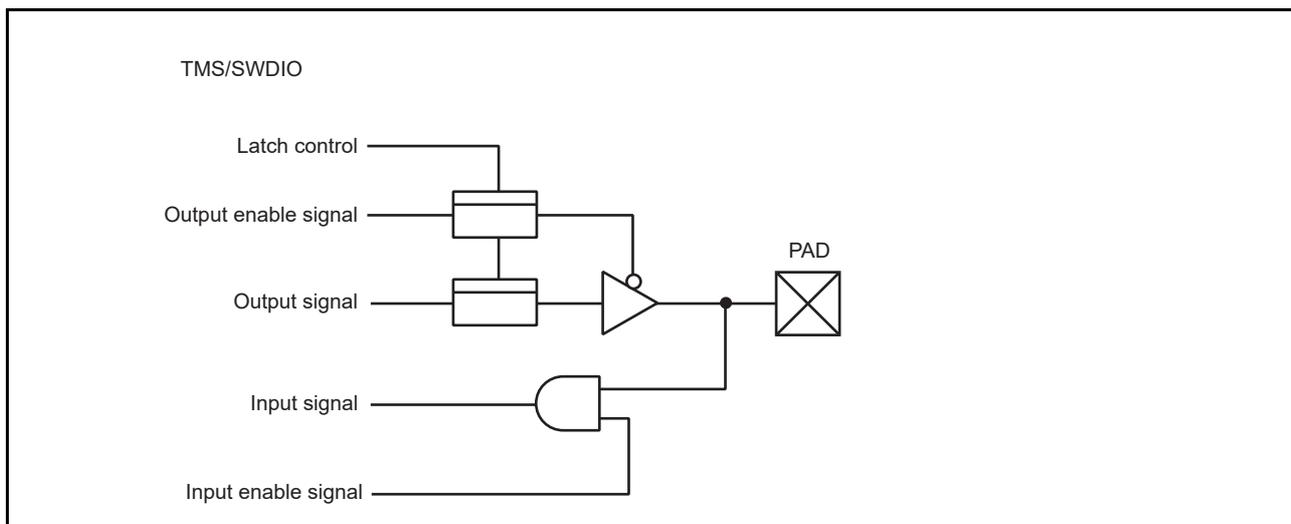


Figure 2.1        (9) Bidirectional Buffer with TTL AND Input and Latch
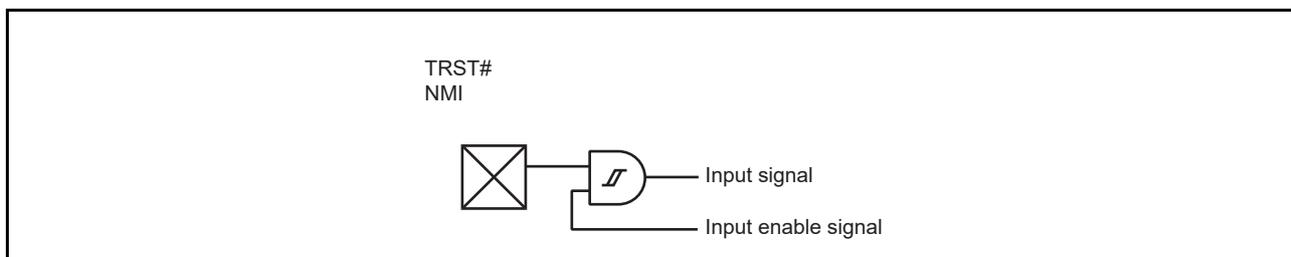


Figure 2.1        (10) Schmitt AND Input Buffer
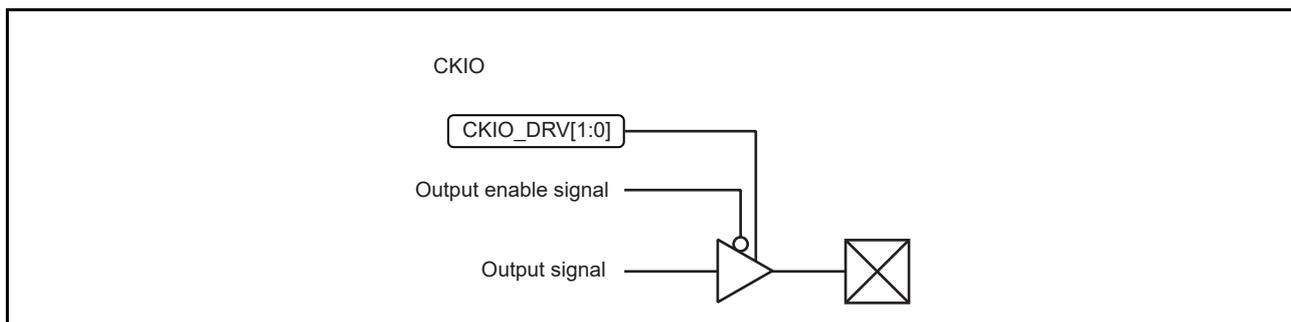
Figure 2.1     (11) Output Buffer with Enable Signal and Controllable Driving Ability
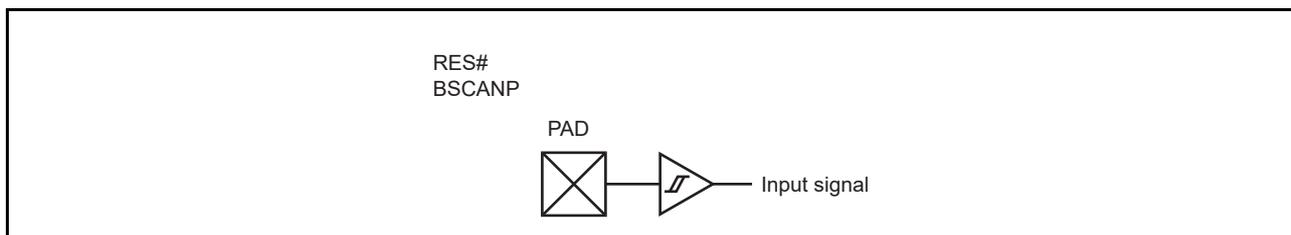


Figure 2.1     (12) Schmitt Input Buffer
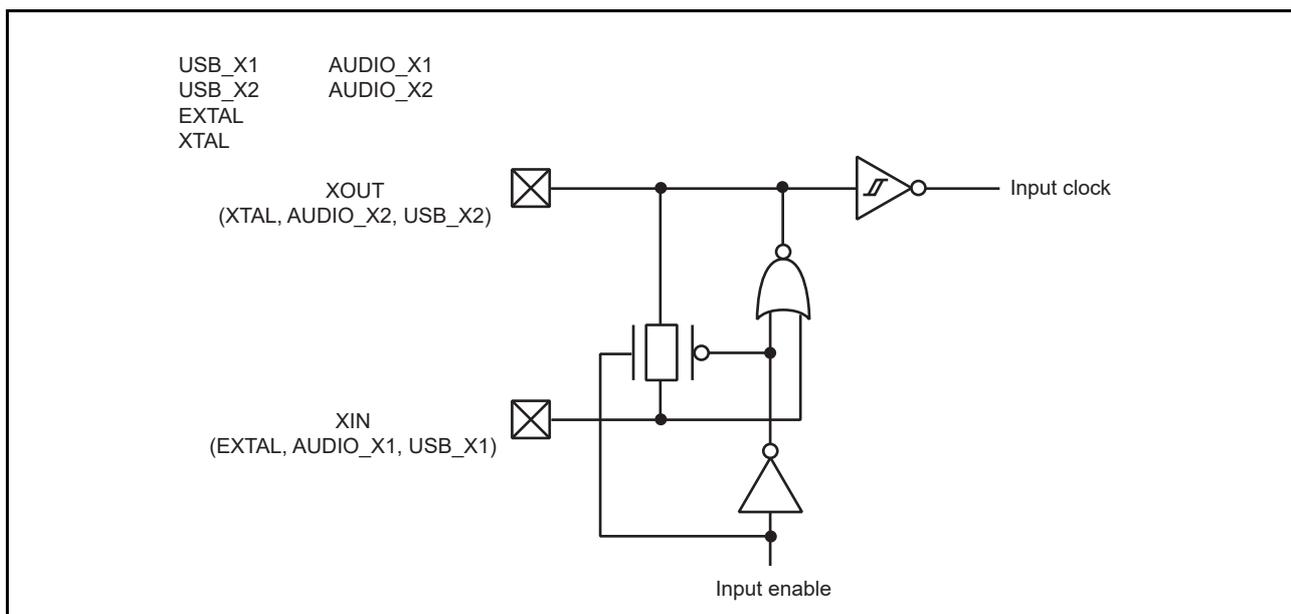


Figure 2.1     (13) Oscillation Buffer (1)

Figure 2.1          (14) Oscillation Buffer (2)

| SD1_CLK | SD0_DAT1 | HM_CK# | HM_DQ5/OM_SIO5 | QSPI0_SSL | QSPI1_SSL |
|---------|----------|--------|----------------|-----------|-----------|
| SD1_CMD | SD0_DAT2 | HM_CS0#/OM_CS0# | HM_DQ6/OM_SIO6 | RPC_RESET# | |
| SD1_DAT0 | SD0_DAT3 | HM_CS1#/OM_CS1# | HM_DQ7/OM_SIO7 | RPC_WP# | |
| SD1_DAT1 | SD0_DAT4 | HM_RWDS/OM_DQS | HM_RESET#/OM_RESET# | RPC_INT# | |
| SD1_DAT2 | SD0_DAT5 | HM_DQ0/OM_SIO0 | QSPI0_SPCLK | QSPI1_SPCLK | |
| SD1_DAT3 | SD0_DAT6 | HM_DQ1/OM_SIO1 | QSPI0_IO0 | QSPI1_IO0 | |
| SD0_CLK | SD0_DAT7 | HM_DQ2/OM_SIO2 | QSPI0_IO1 | QSPI1_IO1 | |
| SD0_CMD | SD0_RST# | HM_DQ3/OM_SIO3 | QSPI0_IO2 | QSPI1_IO2 | |
| SD0_DAT0 | HM_CK/OM_SCLK | HM_DQ4/OM_SIO4 | QSPI0_IO3 | QSPI1_IO3 | |



Figure 2.1          (15) Bidirectional Buffer with AND Input, Controllable Driving Ability, Operating Voltage Selection, and Latch

## 2.2　Pin Assignment

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | Vcc | QSPI1_IO3 | QSPI1_SPCLK | RPC_WP# | QSPI0_IO3 | PVcc_SPI | Vss | PVcc | PF_4 | PE_6 | PL_2 | PE_5 | P8_4 | P8_6 | PE_4 | P9_1 | PVcc | Vss | PE_1 | PA_4 | CKIO | Vss | A |
| B | PK_1 | Vcc | QSPI1_IO1 | QSPI1_IO0 | RPC_RESET# | QSPI0_IO1 | QSPI0_SPCLK | PF_5 | P6_3 | PH_0 | PL_3 | PL_1 | P8_3 | PF_2 | P8_7 | PE_3 | PA_0 | PA_3 | PA_5 | PA_6 | Vss | PVcc | B |
| C | PH_2 | P8_2 | Vcc | QSPI1_SSL | RPC_INT# | QSPI0_SSL | QSPI0_IO0 | P6_1 | P6_2 | PH_1 | PL_4 | PL_0 | P8_5 | PF_1 | P9_0 | PE_2 | PA_2 | PG_0 | PB_0 | Vss | PD_7 | PD_3 | C |
| D | PVcc | BSCANP | P8_1 | Vcc | QSPI1_IO2 | Vss | QSPI0_IO2 | PK_0 | PF_6 | PE_0 | PF_3 | PVcc | Vss | PF_0 | P8_0 | PA_1 | PA_7 | PVcc | Vss | PD_6 | PD_4 | PD_1 | D |
| E | Vss | PH_3 | PK_3 | PK_2 | | | | | | | | | | | | | | | PD_5 | PD_2 | TCK/SWDCLK | JP0_0 | E |
| F | PVcc_HO | HM_CS0#/OM_CS0# | HM_CK/OM_SCLK | PF_7 | | | | | | | | | | | | | | | PD_0 | TRST# | TMS/SWDIO | PB_1 | F |
| G | HM_DQ1/OM_SIO1 | HM_RWDS/OM_DQS | HM_CS1#/OM_CS1# | HM_CK# | | | | | | | | | | | | | | | JP0_1 | PB_2 | PB_3 | P9_2 | G |
| H | HM_DQ4/OM_SIO4 | HM_DQ2/OM_SIO2 | HM_DQ3/OM_SIO3 | HM_DQ0/OM_SIO0 | | | | | | | | | | | | | | | PB_4 | P9_3 | PB_5 | P9_5 | H |
| J | HM_RESET#/OM_RESET# | HM_DQ6/OM_SIO6 | HM_DQ7/OM_SIO7 | HM_DQ5/OM_SIO5 | | | | Vcc | Vss | Vss | Vss | Vss | Vcc | | | | | | P9_4 | P7_7 | P7_6 | P9_6 | J |
| K | Vss | PJ_6 | PH_4 | PJ_0 | | | | Vcc | Vss | Vss | Vss | Vss | Vcc | | | | | | P9_7 | PG_1 | P7_5 | PG_2 | K |
| L | PVcc | P0_1 | P0_0 | PJ_7 | | | | Vcc | Vss | Vss | Vss | Vss | Vcc | | | | | | P7_1 | P7_4 | P7_3 | P7_2 | L |
| M | P0_2 | P0_5 | P0_4 | P0_3 | | | | Vcc | Vss | Vss | Vss | Vss | Vcc | | | | | | P6_6 | P6_0 | P7_0 | PVcc | M |
| N | PJ_3 | PJ_1 | P0_6 | PJ_2 | | | | Vcc | Vss | Vss | Vss | Vss | Vcc | | | | | | P6_5 | PG_3 | P6_4 | Vss | N |
| P | PH_6 | PH_5 | PK_5 | PVcc | | | | Vcc | Vss | Vss | Vss | Vss | Vcc | | | | | | SD0_DAT7 | SD0_RST# | P6_7 | PVcc_SD0 | P |
| R | PVcc | PJ_4 | PJ_5 | Vss | | | | | | | | | | | | | | | SD0_DAT2 | SD0_DAT5 | SD0_DAT4 | SD0_DAT6 | R |
| T | AUDIO_X1 | AUDIO_X2 | P3_5 | P3_2 | | | | | | | | | | | | | | | SD0_DAT0 | SD0_DAT1 | SD0_DAT3 | Vss | T |
| U | Vss | PK_4 | P3_1 | MIPI_AVcc18 | | | | | | | | | | | | | | | SD1_DAT0 | SD1_DAT2 | SD0_CMD | SD0_CLK | U |
| V | CSI_CLKP | CSI_CLKN | PG_4 | Vss | | | | | | | | | | | | | | | P5_4 | SD1_DAT1 | SD1_DAT3 | PVcc_SD1 | V |
| W | CSI_DATA0P | CSI_DATA0N | Vss | PG_6 | P1_0 | P1_2 | P2_0 | PC_2 | P4_3 | LVDS_APVcc | Vss | LVDS_PLLVcc | USB_DPVcc0 | USBVss | Vss | PVcc | Vss | PLLVcc | P5_2 | P5_6 | SD1_CMD | Vss | W |
| Y | CSI_DATA1P | CSI_DATA1N | Vss | P3_3 | P1_4 | PC_0 | P2_2 | P4_2 | P4_6 | NMI | Vss | USBVss | USBVss | USBVss | USBVss | USB_DPVcc1 | PC_7 | PC_6 | P5_0 | P5_1 | P5_7 | SD1_CLK | Y |
| AA | MIPI_AVcc18 | Vss | P1_1 | P3_4 | P3_0 | PC_1 | P4_0 | P4_4 | P4_7 | USB_X2 | DP0 | USB_APVcc0 | RREF0 | USBVss | DP1 | PVcc | PC_5 | XTAL | PC_4 | RTC_X2 | P5_3 | P5_5 | AA |
| AB | Vss | PG_5 | PG_7 | P1_3 | P2_1 | P2_3 | P4_1 | P4_5 | RES# | USB_X1 | DM0 | USB_APVcc1 | RREF1 | USBVss | DM1 | PVcc | PC_3 | EXTAL | Vss | RTC_X1 | AVcc | AVss | AB |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | |

Figure 2.2　　　　Pin Assignment of the 324-Pin BGA (Top Perspective View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | Vcc | QSPI1_IO3 | QSPI1_IO1 | QSPI1_SPCLK | QSPI0_SSL | QSPI0_IO0 | Vss | PVcc | P6_3 | PE_6 | PL_4 | PL_2 | PL_1 | PF_1 | PE_2 | PA_3 | PA_6 | Vss | CKIO | Vss | A |
| B | Vss | Vcc | QSPI1_IO2 | RPC_INT# | RPC_RESET# | QSPI0_IO3 | QSPI0_SPCLK | P6_1 | PF_5 | PH_1 | PF_3 | PL_0 | PE_5 | P8_0 | PE_3 | PA_2 | PA_4 | PB_0 | Vss | PD_6 | B |
| C | PH_2 | PK_1 | Vcc | QSPI1_SSL | RPC_WP# | QSPI0_IO1 | QSPI0_IO2 | PF_6 | PE_0 | PF_4 | PL_3 | PF_2 | PE_4 | PA_0 | PE_1 | PA_5 | PG_0 | Vss | PD_7 | PD_5 | C |
| D | PH_3 | PK_3 | PK_2 | Vcc | QSPI1_IO0 | Vss | PVcc_SPI | PK_0 | P6_2 | PH_0 | PVcc | Vss | PF_0 | PA_1 | PA_7 | PVcc | Vss | PD_4 | PD_3 | PD_1 | D |
| E | Vss | BSCANP | PF_7 | PVcc | | | | | | | | | | | | | PVcc | PD_2 | TCK/SWDCLK | JP0_0 | E |
| F | HM_RWDS/OM_DQS | HM_CK# | HM_CK/OM_SCLK | Vss | | | | | | | | | | | | | TMS/SWDIO | PD_0 | TRST# | JP0_1 | F |
| G | HM_DQ2/OM_SIO2 | HM_DQ1/OM_SIO1 | HM_CS0#/OM_CS0# | PVcc_HO | | | | | | | | | | | | | Vss | PB_1 | PB_2 | PB_3 | G |
| H | HM_DQ3/OM_SIO3 | HM_DQ6/OM_SIO6 | HM_DQ4/OM_SIO4 | HM_CS1#/OM_CS1# | | | | | | | | | | | | | PVcc | PB_5 | PB_4 | P7_7 | H |
| J | HM_RESET#/OM_RESET# | HM_DQ7/OM_SIO7 | HM_DQ5/OM_SIO5 | HM_DQ0/OM_SIO0 | | | | Vcc | Vss | Vss | Vcc | | | | | | P7_6 | PG_2 | PG_1 | P7_2 | J |
| K | PJ_7 | PJ_6 | PH_4 | PJ_0 | | | | Vcc | Vss | Vss | Vcc | | | | | | PVcc | PG_3 | P6_7 | PVcc | K |
| L | PJ_1 | PJ_3 | PH_5 | PVcc | | | | Vcc | Vss | Vss | Vcc | | | | | | Vss | P6_0 | P6_5 | Vss | L |
| M | PH_6 | PJ_2 | PK_5 | Vss | | | | Vcc | Vss | Vss | Vcc | | | | | | PVcc_SD0 | P6_4 | P6_6 | SD0_RST# | M |
| N | PVcc | PJ_5 | PJ_4 | PVcc | | | | | | | | | | | | | SD0_DAT0 | SD0_DAT5 | SD0_DAT7 | SD0_DAT6 | N |
| P | AUDIO_X1 | AUDIO_X2 | P3_5 | PK_4 | | | | | | | | | | | | | PVcc_SD1 | SD0_DAT2 | SD0_DAT3 | SD0_DAT4 | P |
| R | Vss | P3_1 | PG_4 | MIPI AVcc18 | | | | | | | | | | | | | Vss | SD0_CMD | SD0_DAT1 | SD0_CLK | R |
| T | CSI_CLKP | CSI_CLKN | P3_2 | Vss | | | | | | | | | | | | | AVss | SD1_DAT0 | SD1_CLK | Vss | T |
| U | CSI_DATA0P | CSI_DATA0N | Vss | PG_6 | PC_0 | P3_3 | P4_6 | LVDS PLLVcc | LVDS APVcc | USB DPVcc0 | RREF0 | RREF1 | Vss | PLLVcc | PVcc | PC_6 | AVcc | SD1_CMD | SD1_DAT1 | SD1_DAT2 | U |
| V | CSI_DATA1P | CSI_DATA1N | Vss | P3_4 | PC_2 | P4_2 | P4_7 | Vss | Vss | USBVss | USBVss | USBVss | Vss | PC_3 | PC_5 | PC_7 | P5_0 | P5_6 | P5_7 | SD1_DAT3 | V |
| W | MIPI AVcc18 | Vss | PG_5 | P3_0 | P4_1 | P4_3 | NMI | USB_X2 | USBVss | DP0 | USB APVcc0 | USB APVcc1 | DM1 | USB DPVcc1 | PC_4 | XTAL | RTC_X2 | P5_4 | P5_3 | P5_5 | W |
| Y | Vss | PG_7 | PC_1 | P4_0 | P4_4 | P4_5 | RES# | USB_X1 | USBVss | DM0 | USBVss | USBVss | DP1 | USBVss | EXTAL | Vss | RTC_X1 | P5_2 | P5_1 | Vss | Y |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | |

Figure 2.3    Pin Assignment of the 272-Pin BGA (Top Perspective View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | Vcc | QSPI1_SSL | QSPI1_IO3 | QSPI1_SPCLK | RPC_RESET# | PVcc_SPI | Vss | QSPI0_SPCLK | P6_1 | P6_3 | PE_6 | PL_4 | PL_0 | PE_5 | PE_4 | PE_3 | PA_2 | PE_1 | PA_6 | CKIO | Vss | A |
| B | PK_1 | Vcc | QSPI1_IO0 | QSPI1_IO1 | RPC_INT# | QSPI0_SSL | QSPI0_IO3 | QSPI0_IO1 | PF_5 | PF_4 | PH_1 | PL_1 | PL_2 | P8_0 | PF_1 | PA_0 | PA_7 | PA_4 | PB_0 | Vss | PD_3 | B |
| C | PK_3 | PH_2 | | | | | | | | | | | | | | | | | | PD_7 | PD_1 | C |
| D | HM_CK/OM_SCLK | BSCANP | | Vcc | QSPI1_IO2 | RPC_WP# | QSPI0_IO2 | PK_0 | P6_2 | PH_0 | PF_3 | PF_2 | PF_0 | PE_2 | PA_1 | PG_0 | PA_5 | Vss | | PD_5 | JP0_0 | D |
| E | HM_CK# | HM_CS0#/OM_CS0# | | PK_2 | Vcc | Vss | PVcc | QSPI0_IO0 | PF_6 | PE_0 | PL_3 | Vcc | Vss | PVcc | PA_3 | Vcc | Vss | TCK/SWDCLK | | PD_0 | TRST# | E |
| F | HM_DQ1/OM_SIO1 | HM_RWDS/OM_DQS | | PF_7 | Vss | | | | | | | | | | | | PD_6 | PD_2 | | JP0_1 | PB_1 | F |
| G | PVcc_HO | HM_DQ2/OM_SIO2 | | HM_DQ4/OM_SIO4 | PVcc | | | | | | | | | | | | PD_4 | TMS/SWDIO | | PB_3 | PB_5 | G |
| H | Vss | HM_DQ6/OM_SIO6 | | HM_CS1#/OM_CS1# | PH_3 | | | | | | | | | | | | PB_2 | PB_4 | | P7_7 | PG_2 | H |
| J | HM_RESET#/OM_RESET# | PH_4 | | HM_DQ3/OM_SIO3 | HM_DQ0/OM_SIO0 | | | | | | | | | | | | PG_1 | P7_6 | | P7_2 | P6_0 | J |
| K | PJ_6 | PJ_1 | | HM_DQ7/OM_SIO7 | HM_DQ5/OM_SIO5 | | | | | | | | | | | | PVcc | PG_3 | | P6_5 | P6_4 | K |
| L | PH_5 | PJ_3 | | PJ_0 | Vcc | | | | | | | | | | | | Vss | P6_7 | | P6_6 | SD0_DAT6 | L |
| M | PH_6 | PJ_7 | | PJ_2 | Vss | | | | | | | | | | | | Vcc | SD0_RST# | | SD0_DAT7 | PVcc_SD0 | M |
| N | P3_5 | PJ_5 | | PJ_4 | PK_5 | | | | | | | | | | | | SD0_DAT0 | SD0_DAT5 | | SD0_DAT4 | Vss | N |
| P | AUDIO_X1 | AUDIO_X2 | | PK_4 | PVcc | | | | | | | | | | | | SD0_CLK | SD0_DAT2 | | SD0_DAT3 | SD0_DAT1 | P |
| R | PG_4 | P3_1 | | P3_2 | Vss | | | | | | | | | | | | SD1_DAT2 | SD1_DAT0 | | SD1_DAT3 | SD0_CMD | R |
| T | Vss | Vss | | MIPIAVcc18 | Vcc | | | | | | | | | | | | SD1_CLK | SD1_CMD | | SD1_DAT1 | PVcc_SD1 | T |
| U | CSI_DATA0P | CSI_DATA0N | | Vss | PVcc | Vss | LVDS_APVcc | P4_3 | P4_7 | USBVss | RREF0 | RREF1 | USBVss | Vss | PLLVcc | PVcc | Vss | P5_4 | | P5_5 | Vss | U |
| V | CSI_CLKP | CSI_CLKN | | PG_6 | P3_3 | PC_2 | Vss | P4_2 | P4_6 | Vss | USBAPVcc0 | USBAPVcc1 | USBVss | PC_4 | PC_6 | PC_3 | PVcc | P5_0 | | P5_6 | P5_7 | V |
| W | CSI_DATA1P | CSI_DATA1N | | | | | | | | | | | | | | | | | | P5_2 | P5_3 | W |
| Y | Vss | Vss | PG_7 | PC_0 | PC_1 | P4_0 | P4_4 | LVDS_PLLVcc | NMI | USB_X2 | USB_DPVcc0 | DP0 | USBVss | DP1 | USB_DPVcc1 | Vss | XTAL | RTC_X2 | AVcc | PVcc | P5_1 | Y |
| AA | Vss | PG_5 | P3_4 | P3_0 | Vss | P4_1 | P4_5 | Vss | RES# | USB_X1 | USBVss | DM0 | USBVss | DM1 | USBVss | PC_5 | PC_7 | EXTAL | RTC_X1 | AVss | PVcc | AA |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | |

Figure 2.4      Pin Assignment of the 256-Pin BGA (Top Perspective View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | Vss | PK_3 | QSPI1_SPCLK | RPC_WP# | PVcc_SPI | Vss | QSPI0_IO3 | P6_1 | P6_2 | PH_1 | PE_6 | PL_2 | PE_3 | CKIO | Vss | A |
| B | BSCANP | PH_3 | QSPI1_SSL | QSPI1_IO1 | RPC_RESET# | QSPI0_IO2 | QSPI0_IO1 | PK_0 | P6_3 | PL_4 | PL_0 | PE_5 | PE_1 | Vss | PD_7 | B |
| C | HM_CK/OM_SCLK | PK_1 | QSPI1_IO3 | QSPI1_IO2 | RPC_INT# | QSPI0_SSL | QSPI0_SPCLK | PE_0 | PH_0 | PL_1 | PE_4 | PG_0 | Vss | PD_5 | PD_3 | C |
| D | HM_CK# | HM_CS0#/OM_CS0# | PK_2 | Vss | Vcc | QSPI1_IO0 | QSPI0_IO0 | PVcc | PL_3 | PE_2 | PVcc | Vss | PD_6 | PD_4 | PD_1 | D |
| E | Vss | HM_DQ0/OM_SIO0 | HM_RWDS/OM_DQS | PVcc | | | | | | | | PD_2 | PD_0 | TCK/SWDCLK | JP0_0 | E |
| F | PVcc_HO | HM_DQ2/OM_SIO2 | HM_DQ1/OM_SIO1 | HM_CS1#/OM_CS1# | | | | | | | | TMS/SWDIO | JP0_1 | TRST# | P6_0 | F |
| G | HM_DQ4/OM_SIO4 | HM_DQ7/OM_SIO7 | HM_DQ5/OM_SIO5 | HM_DQ3/OM_SIO3 | | | | | | | | Vcc | PG_3 | PG_2 | PVcc | G |
| H | HM_DQ6/OM_SIO6 | HM_RESET#/OM_RESET# | PH_4 | Vcc | | | | | | | | PG_1 | SD0_DAT5 | SD0_RST# | Vss | H |
| J | PJ_0 | PJ_1 | PJ_2 | Vss | | | | | | | | SD0_DAT7 | SD0_DAT2 | SD0_DAT4 | PVcc_SD0 | J |
| K | PJ_5 | PJ_3 | PJ_4 | PVcc | | | | | | | | SD0_CLK | SD0_DAT3 | SD0_DAT0 | SD0_DAT6 | K |
| L | PK_4 | P3_5 | Vss | Vcc | | | | | | | | PVcc | Vss | SD0_DAT1 | SD0_CMD | L |
| M | AUDIO_X1 | AUDIO_X2 | P3_2 | Vss | P3_3 | LVDS APVcc | LVDS PLLVcc | NMI | USBVss | PVcc | Vcc | P5_0 | P5_4 | P5_7 | P5_5 | M |
| N | P3_1 | PG_4 | Vss | PG_7 | P4_2 | P4_3 | P4_6 | RES# | RREF0 | Vss | PLLVcc | Vcc | P5_2 | P5_3 | P5_6 | N |
| P | PVcc | Vss | PG_6 | P4_0 | P4_4 | P4_7 | USB_X2 | USB DPVcc0 | USB APVcc0 | USBVss | XTAL | RTC_X2 | AVcc | Vcc | P5_1 | P |
| R | Vss | PG_5 | P3_4 | P4_1 | P4_5 | Vss | USB_X1 | DP0 | DM0 | USBVss | EXTAL | Vss | RTC_X1 | AVss | Vcc | R |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |

Figure 2.5      Pin Assignment of the 176-Pin BGA (Top Perspective View)

# 3.     Electrical Characteristics

## 3.1     Absolute Maximum Ratings

Table 3.1        Absolute Maximum Ratings

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage (I/O) | | PVcc | −0.3 to 4.2 | V |
| Power supply voltage (1.8-/3.3-V switchable I/O) | | PVcc_SPI<br>PVcc_SD0<br>PVcc_SD1 | −0.3 to 4.2 | V |
| Power supply voltage (1.8-V I/O) | | PVcc_HO | −0.3 to 4.2 | V |
| Power supply voltage (Internal) | | Vcc | −0.3 to 1.6 | V |
| PLL power supply voltage | | PLLVcc | −0.3 to 1.6 | V |
| Analog power supply voltage | | AVcc | −0.3 to 4.2 | V |
| USB transceiver analog power supply voltage (I/O) | | USBAPVcc1<br>USBAPVcc0 | −0.3 to 4.2 | V |
| USB transceiver digital power supply voltage (I/O) | | USBDPVcc1<br>USBDPVcc0 | −0.3 to 4.2 | V |
| LVDS analog power supply voltage | | LVDSAPVcc | −0.3 to 4.2 | V |
| LVDS PLL power supply voltage | | LVDSPLLVcc | −0.3 to 1.6 | V |
| MIPI analog power supply voltage | | MIPIAVcc18 | −0.3 to 2.6 | V |
| Input voltage | 1.8-V I/O input pins | $V_{in}$ | −0.3 to 1.8-V power supply (PVcc_HO, MIPIAVcc18) + 0.3 | V |
| | 1.8-/3.3-V switchable I/O input pins | $V_{in}$ | −0.3 to 1.8-/3.3-V power supply (PVcc_SPI, PVcc_SD0, PVcc_SD1) + 0.3 | V |
| | Other input pins | $V_{in}$ | −0.3 to 3.3-V power supply (PVcc, AVcc, USBAPVcc1, USBAPVcc0, USBDPVcc1, USBDPVcc0, LVDSAPVcc) + 0.3 | V |
| Operating temperature | Ambient temperature | Ta | −40 to +85 | °C |
| | Junction temperature | Tj | −40 to +125 | |
| Storage temperature | | $T_{stg}$ | −55 to +125 | °C |

Caution:  Permanent damage to the LSI may result if absolute maximum ratings are exceeded

## 3.2     Power-On/Power-Off Sequence

The 1.2-V power supply (Vcc, PLLVcc, and LVDSPLLVcc), 1.8-V power supply (PVcc_HO and MIPIAVcc18), 1.8-/3.3-V switchable power supply (PVcc_SPI, PVcc_SD0, PVcc_SD1), and 3.3-V power supply (PVcc, AVcc, USBAPVcc1, USBAPVcc0, USBDPVcc1, USBDPVcc0, and LVDSAPVcc) can be turned on and off in any order. When turning on the power, be sure to drive both the TRST# and RES# pins low; otherwise, the output pins and input/output pins output undefined levels, resulting in system malfunction.
When turning off the power, drive the TRST# and RES# pins low if the undefined output may cause a problem.

## 3.3 DC Characteristics

- Conditions used to obtain DC characteristics (2) in Table 3.2 other than current consumption
  Vcc = 1.14 to 1.26 V, PVcc = USBDPVcc0 = USBDPVcc1 = AVcc = 3.0 to 3.6 V,
  PVcc_SPI = 3.0 to 3.6 V/1.7 to 1.9 V, PVcc_SD0 = 3.0 to 3.6 V/1.7 to 1.9 V,
  PVcc_SD1 = 3.0 to 3.6 V/1.7 to 1.9 V, PLLVcc = 1.14 to 1.26 V,
  USBAPVcc0 = USBAPVcc1 = 3.0 to 3.6 V, LVDSAPVcc = 3.0 to 3.6 V,
  LVDSPLLVcc = 1.14 to 1.26 V, PVcc_HO = MIPIAVcc18 = 1.7 to 1.9 V,
  Vss = AVss = USBVss = 0 V
  Ta = –40 to +85°C, Tj = –40 to +125°C

- Conditions used to obtain DC characteristics (2) in Table 3.2 for current consumption
  Vcc = 1.20 V, PVcc = USBDPVcc0 = USBDPVcc1 = AVcc = 3.3 V,
  PVcc_SPI = 3.3 V/1.8 V, PVcc_SD0 = 3.3 V/1.8 V, PVcc_SD1 = 3.3 V/1.8 V,
  PLLVcc = 1.20 V, USBAPVcc0 = USBAPVcc1 = 3.3 V, LVDSAPVcc = 3.3 V,
  LVDSPLLVcc = 1.20 V, PVcc_HO = MIPIAVcc18 = 1.8 V,
  Vss = AVss = USBVss = 0 V
  Ta = –40 to +85°C, Tj = –40 to +125°C
  Iφ = 528.0 MHz, Gφ = 264.00 MHz, Bφ = 132.00 MHz, P1φ = 66.00 MHz, P0φ = 33.00 MHz

Table 3.2 DC Characteristics (1) [Common Items]

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Power supply voltage | | PVcc | 3.0 | 3.3 | 3.6 | V | |
| | | PVcc_SPI | 1.7 | 1.8 | 1.9 | V | 1.8-V power supply selection |
| | | PVcc_SD0 PVcc_SD1 | 3.0 | 3.3 | 3.6 | V | 3.3-V power supply selection |
| | | PVcc_HO | 1.7 | 1.8 | 1.9 | V | |
| | | Vcc | 1.14 | 1.20 | 1.26 | V | |
| PLL power supply voltage | | PLLVcc | 1.14 | 1.20 | 1.26 | V | |
| Analog power supply voltage | | AVcc | 3.0 | 3.3 | 3.6 | V | |
| USB power supply voltage | | USBAPVcc1 USBAPVcc0 USBDPVcc1 USBDPVcc0 | 3.0 | 3.3 | 3.6 | V | |
| LVDS analog power supply voltage | | LVDSAPVcc | 3.0 | 3.3 | 3.6 | V | |
| LVDS PLL power supply voltage | | LVDSPLLVcc | 1.14 | 1.20 | 1.26 | V | |
| MIPI analog power supply voltage | | MIPIAVcc18 | 1.7 | 1.8 | 1.9 | V | |
| Input leakage current | All input pins (except MIPI CSI-2 interface Related Pins[1] ) | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to PVcc − 0.5 V |
| | MIPI CSI-2 interface Related Pins[1] | | | | 10 | µA | $V_{in}$ = 0.5 to MIPIAVcc18 − 0.5 V |
| Three-state leakage current | All input/output pins, all output pins (except PD_0 to PD_7) (off state) | $\lvert I_{STI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to PVcc − 0.5 V |
| | PD_0 to PD_7 | | — | — | 10 | µA | |
| Input capacitance | USB 2.0 Host/Function Module-Related Pins[2] | $C_{in}$ | — | — | 20 | pF | |
| | All input/output pins and all input pins other than above | | — | — | 10 | pF | |

Note 1. CSI_DATA0P, CSI_DATA0N, CSI_DATA1P, CSI_DATA1N, CSI_CLKP, CSI_CLKN pins
Note 2. DP1, DP0, DM1, DM0 pins

Table 3.2    DC Characteristics (2) [Current Consumption]

| Item | Power Supply | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Current consumption in normal operation | Vcc | Icc | — | 994 | mA | When the DRP is not in use. |
| | | | — | 400 | mA | When the DRP is in use, these values are added to that of the above columns, respectively. |
| | PLLVcc | PLLIcc | — | 21.8 | mA | |
| | LVDSPLLVcc | LVDSPLLIcc | — | 2.1 | mA | |
| | MIPIAVcc18 | MIPIAIcc18 | — | 10 | mA | During MIPI transfer |
| | PVcc_HO | PIcc_HO | 15[*1] | — | mA | PVcc_HO = 1.8 V HM_CK, HM_CK# / OM_SCLK = 132 MHz |
| | PVcc_SPI | PIcc_SPI | 15[*1] | — | mA | PVcc_SPI = 3.3 V QSPI0_SPCLK, QSPI1_SPCLK = 66 MHz |
| | | | 15[*1] | — | mA | PVcc_SPI = 1.8 V QSPI0_SPCLK, QSPI1_SPCLK = 132 MHz |
| | PVcc_SD0 | PIcc_SD0 | 15[*1] | — | mA | PVcc_SD0 = 3.3 V SD0_CLK = 33 MHz |
| | | | 11[*1] | — | mA | PVcc_SD0 = 1.8 V SD0_CLK = 132 MHz |
| | PVcc_SD1 | PIcc_SD1 | 15[*1] | — | mA | PVcc_SD1 = 3.3 V SD1_CLK = 33 MHz |
| | | | 11[*1] | — | mA | PVcc_SD1 = 1.8 V SD1_CLK = 132 MHz |
| | PVcc | PIcc | 100[*1] | — | mA | |
| | USBDPVcc0 + USBDPVcc1 | UDPIcc | 52[*1] | — | mA | In USB high-speed operation (1ch) |
| | | | 93[*1] | — | mA | In USB high-speed operation (2ch) |
| | | | 19[*1] | — | mA | In USB full-speed operation (1ch) |
| | | | 29[*1] | — | mA | In USB full-speed operation (2ch) |
| | USBAPVcc0 + USBAPVcc1 | UAPIcc | — | 11 | mA | When 1-ch is in use |
| | | | — | 18 | mA | When 2-ch is in use |
| | LVDSAPVcc | LVDSAPIcc | — | 30 | mA | During LVDS transfer |
| | AVcc | AIcc | — | 1 | mA | During A/D conversion |
| Current consumption in sleep mode | Vcc | $I_{sleep}$ | — | 850 | mA | |
| | For the other power supply, the current consumption is the same as in normal operation. | | | | | |
| Current consumption in software standby mode | Vcc + PLLVcc + LVDSPLLVcc | $I_{sstby}$ | 30 | 500 | mA | |
| | MIPIAVcc18 + PVcc_SPI + PVcc_HO + PVcc_SD0 + PVcc_SD1 | $PI_{sstby18\_33}$ | 0.4 | 3.4 | µA | |
| | PVcc + AVcc + USBAPVcc1 + USBAPVcc0 + USBDPVcc1 + USBDPVcc0 + LVDSAPVcc | $PI_{sstby}$ | 3 | 20 | µA | When the USB host/function is not in use |
| | | | 4.5 | 5 | mA | When the USB host/function is in use |

| Item | Power Supply | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Current consumption in deep standby mode | Vcc + PLLVcc + LVDSPLLVcc | $I_{dstby}$ | 16 | 155 | µA | RAM 0 Kbytes retained |
| | | | 22 | 170 | µA | RAM 16 Kbytes retained |
| | | | 28 | 185 | µA | RAM 32 Kbytes retained |
| | | | 40 | 215 | µA | RAM 64 Kbytes retained |
| | | | 64 | 275 | µA | RAM 128 Kbytes retained |
| | MIPIAVcc18 + PVcc_SPI + PVcc_HO + PVcc_SD0 + PVcc_SD1 | $PI_{dstby18\_33}$ | 0.4 | 2.1 | µA | |
| | PVcc + AVcc + USBAPVcc1 + USBAPVcc0 + USBDPVcc1 + USBDPVcc0 + LVDSAPVcc | $PI_{dstby}$ | 2.4 | 7 | µA | RTC is not operating |
| | | | 7.7 | 12.5 | µA | RTC_X1 selected |
| | | | 1.3 | — | mA | EXTAL 12 MHz selected, small gain |
| | | | 1.5 | — | mA | EXTAL 24 MHz selected, small gain |

Note 1.  Reference value. The actual operating current greatly depends on the system (such as slow rising/falling edges caused by IO load and toggle frequency). Be sure to determine the value using the actual system.

Table 3.2    DC Characteristics (3) [Except 1.8-/3.3-V Switchable I/O Interface, I$^2$C Bus Interface, and USB 2.0 Host/ Function Module-Related Pins]

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input high voltage*[1] | | $V_{IH}$ | 2.2 | — | PVcc + 0.3 | V | |
| Input low voltage*[1] | | $V_{IL}$ | –0.3 | — | 0.8 | V | |
| Schmitt trigger input characteristics | | $VT^+$ | PVcc × 0.665 | — | PVcc + 0.3 | V | |
| | | $VT^-$ | –0.3 | — | 0.8 | V | |
| | | $VT^+- VT^-$ | 0.2 | — | — | V | |
| Output high voltage | | $V_{OH}$ | PVcc – 0.5 | — | — | V | $I_{OH}$ = –8.0 mA*[2], –2.0 mA*[3] |
| Output low voltage | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8.0 mA*[2], 2.0 mA*[3] |
| RAM standby voltage | Software standby mode (large-capacity on-chip RAM) | $V_{RAMS}$ | 0.85 | — | — | V | Measured with Vcc as parameter |
| | Deep standby mode (only the on-chip RAM for data retention) | $V_{RAMD}$ | 1.14 | — | — | V | |

Note 1.  Except for Schmitt trigger function
Note 2.  This is the value when high driving ability is set with a pin for which high driving ability is selectable.
Note 3.  This is the value when normal driving ability is set with a pin for which high driving ability is selectable or the value of the pin to which normal driving ability is fixed.

Table 3.2    DC Characteristics (4) [1.8-/3.3-V Switchable I/O Interface*]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 1.27 | — | PVcc_* + 0.3 | V | PVcc_SPI with 1.8-V power supply selection |
| | | | | 2 | | PVcc_SD0 and PVcc_SD1 with 1.8-V power supply selection |
| | | PVcc_* × 0.625 | — | PVcc_* + 0.3 | V | 3.3-V power supply selection |
| Input low voltage | $V_{IL}$ | −0.3 | — | 0.58 | V | 1.8-V power supply selection |
| | | −0.3 | — | PVcc_* × 0.25 | V | 3.3-V power supply selection |
| Output high voltage | $V_{OH}$ | 1.4 | — | — | V | 1.8-V power supply selection, $I_{OH}$ = −2.0 mA |
| | | PVcc_* × 0.75 | — | — | V | 3.3-V power supply selection, $I_{OH}$ = −2.0 mA |
| Output low voltage | $V_{OL}$ | — | — | 0.45 | V | 1.8-V power supply selection, $I_{OL}$ = 2.0 mA |
| | | — | — | PVcc_* × 0.125 | V | 3.3-V power supply selection, $I_{OL}$ = 2.0 mA |

Note:  PVcc_SPI, PVcc_SD0, PVcc_SD1

Table 3.2    DC Characteristics (5) [1.8-V I/O Interface*]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 1.27 | — | PVcc_* + 0.3 | V | |
| Input low voltage | $V_{IL}$ | −0.3 | — | 0.58 | V | |
| Output high voltage | $V_{OH}$ | 1.4 | — | — | V | $I_{OH}$ = −2.0 mA |
| Output low voltage | $V_{OL}$ | — | — | 0.45 | V | $I_{OL}$ = 2.0 mA |

Note:  PVcc_HO

Table 3.2    DC Characteristics (6) [I$^2$C Bus Interface-Related Pins*]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | PVcc × 0.7 | — | PVcc + 0.3 | V | |
| Input low voltage | $V_{IL}$ | −0.3 | — | PVcc × 0.3 | V | |
| Schmitt trigger input characteristics | $V_{IH} - V_{IL}$ | PVcc × 0.05 | — | — | V | |
| Output low voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 3.0 mA (RIICnFER.FMPE = 0) |
| | | — | — | 0.4 | V | $I_{OL}$ = 20.0 mA (RIICnFER.FMPE = 1) |

Note:  The PD_0 to PD_7 pins are open-drain pins.

Table 3.2    DC Characteristics (7) [USB 2.0 Host/Function Module-Related Pins*]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Reference resistance | $R_{REF}$ | 2.2 kΩ ± 1% | | | | |

Note:  RREF0, RREF1 pins.

Table 3.2    DC Characteristics (8) [USB 2.0 Host/Function Module-Related Pins* (Low-Speed, Full-Speed, and High-Speed Common Items)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DP pull-up resistance (when function is selected) | $R_{pu}$ | 0.900 | — | 1.575 | kΩ | In idle mode |
| | | 1.425 | — | 3.090 | kΩ | In transmit/receive mode |
| DP and DM pull-down resistance (when host is selected) | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | |

Note:  DP1, DP0, DM1, and DM0 pins

Table 3.2    DC Characteristics (9) [USB 2.0 Host/Function Module-Related Pins* (Low-Speed and Full-Speed)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2.0 | — | — | V | |
| Input low voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | $\mid$(DP) – (DM)$\mid$ |
| Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Output high voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 µA |
| Output low voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| Output signal crossover voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | $C_L$ = 50 pF (full-speed) $C_L$ = 200 to 600 pF (low-speed) |

Note:  DP1, DP0, DM1, and DM0 pins

Table 3.2    DC Characteristics (10) [USB 2.0 Host/Function Module-Related Pins* (High-Speed)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Squelch detection threshold voltage (differential voltage) | $V_{HSSQ}$ | 100 | — | 150 | mV | |
| Common mode voltage range | $V_{HSCM}$ | –50 | — | 500 | mV | |
| Idle state | $V_{HSOI}$ | –10.0 | — | 10.0 | mV | |
| Output high voltage | $V_{HSOH}$ | 360 | — | 440 | mV | |
| Output low voltage | $V_{HSOL}$ | –10.0 | — | 10.0 | mV | |
| Chirp J output voltage (difference) | $V_{CHIRPJ}$ | 700 | — | 1100 | mV | |
| Chirp K output voltage (difference) | $V_{CHIRPK}$ | –900 | — | –500 | mV | |

Note:  DP1, DP0, DM1, and DM0 pins

Table 3.2    DC Characteristics (11) [LVDS-Related Pins*]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Differential Output Voltage | VOD | 250 | 350 | 450 | mV | $R_L$ = 100Ω |
| Difference VOD between 'H' and 'L' | ΔVOD | — | — | 50 | mV | $R_L$ = 100Ω |
| Offset (Common Mode) Voltage | VOS | 1.125 | 1.25 | 1.375 | V | $R_L$ = 100Ω |
| Difference VOS between 'H' and 'L' | ΔVOS | — | — | 50 | mV | $R_L$ = 100Ω |

Note:  TXCLKOUTP, TXCLKOUTM, TXOUT2P to TXOUT0P, and TXOUT2M to TXOUT0M pins
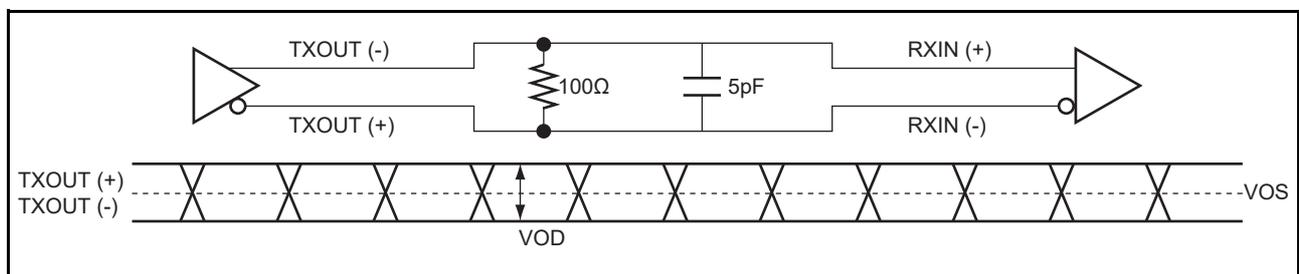


Figure 3.1        LVDS output waveform

Table 3.2     DC Characteristics (12) [MIPI CSI-2 interface-Related Pins[*] ]

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input signal voltage range | $V_{PIN}$ | −50 | — | 1350 | mV | |
| Ground shift | $V_{GNDSH}$ | −50 | — | 50 | mV | |
| transient pin voltage level | $V_{PIN(absmax)}$ | −0.15 | — | 1.45 | V | |
| Differential input high threshold | $V_{IDTH}$ | — | — | 70 | mV | HS Receiver |
| Differential input low threshold | $V_{IDTL}$ | −70 | — | — | mV | HS Receiver |
| Single-ended input high voltage | $V_{IHHS}$ | — | — | 460 | mV | HS Receiver |
| Single-ended input low voltage | $V_{ILHS}$ | −40 | — | — | mV | HS Receiver |
| Input common mode voltage | $V_{CMRX(DC)}$ | 70 | — | 330 | mV | HS Receiver |
| Differential input impedance | $Z_{ID}$ | 80 | — | 125 | Ω | HS Receiver |
| Input high voltage | $V_{IH}$ | 880 | — | — | mV | LP Receiver |
| Input low voltage | $V_{IL}$ | — | — | 550 | mV | LP Receiver |
| Input hysteresis | $V_{HYST}$ | — | 50 | — | mV | LP Receiver, Reference value |

Note: CSI_DATA0P, CSI_DATA0N, CSI_DATA1P, CSI_DATA1N, CSI_CLKP, CSI_CLKN pins

Table 3.3      Permissible Output Currents

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | PD_0 to PD_7 | High-speed mode | IOL | — | — | 20 | mA |
| | | Normal mode | | | | 6 | mA |
| | The CKIO, SD0_CLK, and SD1_CLK output pins, and output pins driven by the PVcc_SPI, or PVcc_HO power supply pin | High drive | | | | 12 | mA |
| | | Normal drive | | | | 8 | mA |
| | SD0_CMD, SD0_DAT7 to SD0_DAT0, SD1_CMD, SD1_DAT3 to SD1_DAT0 | | | | | 6 | mA |
| | Output pins other than above | High drive[*1] | | | | 8 | mA |
| | | Normal drive[*2] | | | | 2 | mA |
| Permissible output high current (per pin) | The CKIO, SD0_CLK, and SD1_CLK output pins, and output pins driven by the PVcc_SPI, or PVcc_HO power supply pin | High drive | − IOH | — | — | 12 | mA |
| | | Normal drive | | | | 8 | mA |
| | SD0_CMD, SD0_DAT7 to SD0_DAT0, SD1_CMD, SD1_DAT3 to SD1_DAT0 | | | | | 6 | mA |
| | Output pins other than above | High drive[*1] | | | | 8 | mA |
| | | Normal drive[*2] | | | | 2 | mA |
| Permissible output current (total) | | | Σ IO | — | — | 150 | mA |

Caution: To protect the LSI's reliability, the output current values should not exceed the values in Table 3.3.

Note 1. This is the value when high driving ability is set with a pin for which high driving ability is selectable.

Note 2. This is the value when normal driving ability is set with a pin for which high driving ability is selectable or the value of the pin to which normal driving ability is fixed.

## 3.4　AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. The setup and hold times for input pins must be followed.

Conditions for AC characteristics: Vcc = 1.14 to 1.26 V, PVcc = USBDPVcc0 = USBDPVcc1 = AVcc = 3.0 to 3.6 V, PVcc_SPI = 3.0 to 3.6 V/1.7 to 1.9 V, PVcc_SD0 = 3.0 to 3.6 V/1.7 to 1.9 V, PVcc_SD1 = 3.0 to 3.6 V/1.7 to 1.9 V, PLLVcc = 1.14 to 1.26 V, USBAPVcc0 = USBAPVcc1 = 3.0 to 3.6 V, LVDSAPVcc = 3.0 to 3.6 V, LVDSPLLVcc = 1.14 to 1.26 V, PVcc_HO = MIPIAVcc18 = 1.7 to 1.9 V, Vss = AVss = USBVss = 0 V, Ta = –40 to +85℃, Tj = –40 to +125℃

Table 3.4　　　Operating Frequency

| Item | | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Operating frequency | CPU clock (Iφ) | f | 55 | 528 | MHz | |
| | Image processing clock (Gφ) | | 55 | 264 | MHz | |
| | Internal bus clock (Bφ) | | 27.5 | 132 | MHz | |
| | Peripheral clock 1 (P1φ) | | 27.5 | 66 | MHz | |
| | Peripheral clock 0 (P0φ) | | 27.5 | 33 | MHz | |

## 3.4.1 Clock Timing

Table 3.5 Clock Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| EXTAL clock input frequency (when the clock is supplied to USB 2.0 host/function module) | $f_{EX}$ | 12MHz ± 100ppm<br>24MHz ± 100ppm | | | Figure 3.2 |
| EXTAL clock input frequency (when the clock isn't supplied to USB 2.0 host/function module) | | 10<br>20 | 12<br>24 | MHz | |
| EXTAL clock input cycle time (when the clock isn't supplied to USB 2.0 host/function module) | $t_{EXcyc}$ | 83.34<br>41.67 | 100<br>50 | ns | |
| AUDIO_X1 clock input frequency (crystal resonator connected) | $f_{EX}$ | 10.00 | 50.00 | MHz | |
| AUDIO_X1 clock input cycle time (crystal resonator connected) | $t_{EXcyc}$ | 20.00 | 100.00 | ns | |
| AUDIO_X1, AUDIO_CLK clock input frequency (external clock input) | $f_{EX}$ | 1.00 | 50.00 | MHz | |
| AUDIO_X1, AUDIO_CLK clock input cycle time (external clock input) | $t_{EXcyc}$ | 20.00 | 1000.00 | ns | |
| USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module) | $f_{EX}$ | 48MHz ± 100ppm | | | |
| EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1 clock input low pulse width | $t_{EXL}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |
| EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1 clock input high pulse width | $t_{EXH}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |
| EXTAL, AUDIO_X1, AUDIO_CLK, USB_ X1 clock input rise time | $t_{EXr}$ | — | 4 | ns | |
| EXTAL, AUDIO_X1, AUDIO_CLK, USB_ X1 clock input fall time | $t_{EXf}$ | — | 4 | ns | |
| CKIO clock output frequency | $f_{OP}$ | 27.5[1] | 132[1] | MHz | |
| CKIO clock output cycle time | $t_{cyc}$ | 7.58[1] | 36.36[1] | ns | Figure 3.3 (1),<br>Figure 3.3 (2) |
| CKIO clock output low pulse width 1 | $t_{CKOL1}$ | $t_{cyc} / 2 - t_{CKOr1}$ | — | ns | Figure 3.3 (1) |
| CKIO clock output high pulse width 1 | $t_{CKOH1}$ | $t_{cyc} / 2 - t_{CKOf1}$ | — | ns | |
| CKIO clock output rise time 1 | $t_{CKOr1}$ | — | 3 | ns | |
| CKIO clock output fall time 1 | $t_{CKOf1}$ | — | 3 | ns | |
| CKIO clock output low pulse width 2 | $t_{CKOL2}$ | $t_{cyc} / 2 - t_{CKOr2}$ | — | ns | Figure 3.3 (2) |
| CKIO clock output high pulse width 2 | $t_{CKOH2}$ | $t_{cyc} / 2 - t_{CKOf2}$ | — | ns | |
| CKIO clock output rise time 2 | $t_{CKOr2}$ | — | 2 | ns | |
| CKIO clock output fall time 2 | $t_{CKOf2}$ | — | 2 | ns | |
| CKIO clock output low pulse width 3 | $t_{CKOL3}$ | $t_{cyc} / 2 - t_{CKOr3}$ | — | ns | Figure 3.3 (3) |
| CKIO clock output high pulse width 3 | $t_{CKOH3}$ | $t_{cyc} / 2 - t_{CKOf3}$ | — | ns | |
| CKIO clock output rise time 3 | $t_{CKOr3}$ | — | 1[2] | ns | |
| CKIO clock output fall time 3 | $t_{CKOf3}$ | — | 1[2] | ns | |
| On-chip PLL circuit oscillation settling time | $t_{POSC}$ | 1 | — | ms | Figure 3.4,<br>Figure 3.5 |
| On-chip oscillation circuit oscillation settling time (RTC_X1) | $t_{ROSC}$ | — | 3[3] | s | Figure 3.7 |
| On-chip oscillation circuit oscillation settling time (other than above) | | — | 4[3] | ms | Figure 3.4,<br>Figure 3.5 ,<br>Figure 3.7 |
| Mode hold time | $t_{MDH}$ | 200 | — | ns | Figure 3.4,<br>Figure 3.5 |

Note 1. The range of CKIO clock output frequency and cycle time is determined by register settings. See Table 6.4 and Table 6.5 in Section 6, Clock Pulse Generator, of the RZ/A2M Group User's Manual.

Note 2.  Output load: 15 pF

Note 3.  Settings for values smaller than the above specifications may be possible, as long as the values are confirmed through evaluation by the manufacturer of the oscillator.
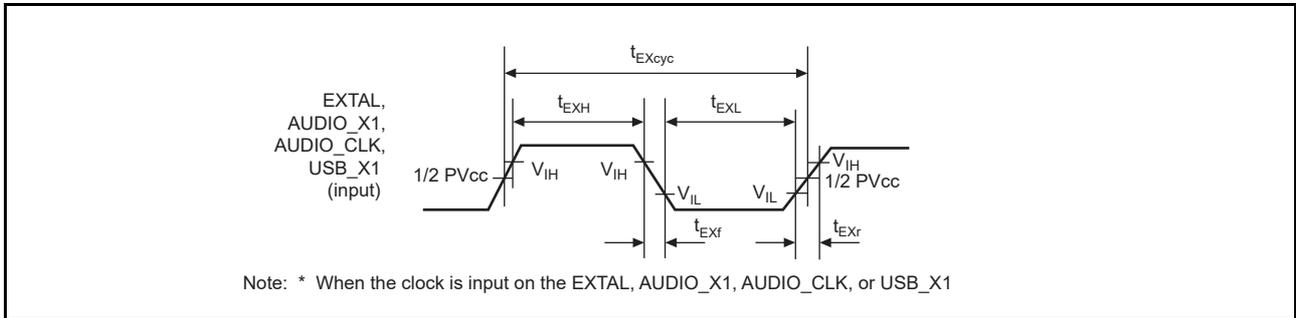


Figure 3.2        EXTAL, AUDIO_X1, AUDIO_CLK, and USB_X1 Clock Input Timing
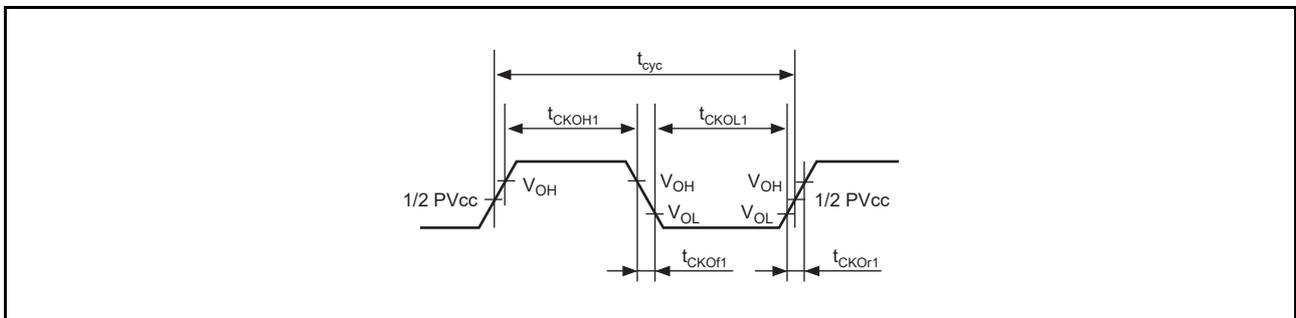


Figure 3.3        (1) CKIO Clock Output Timing 1
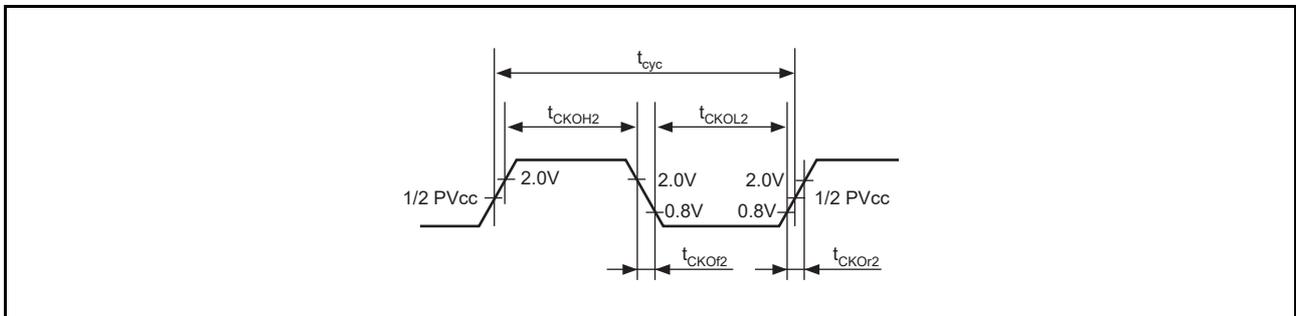


Figure 3.3        (2) CKIO Clock Output Timing 2
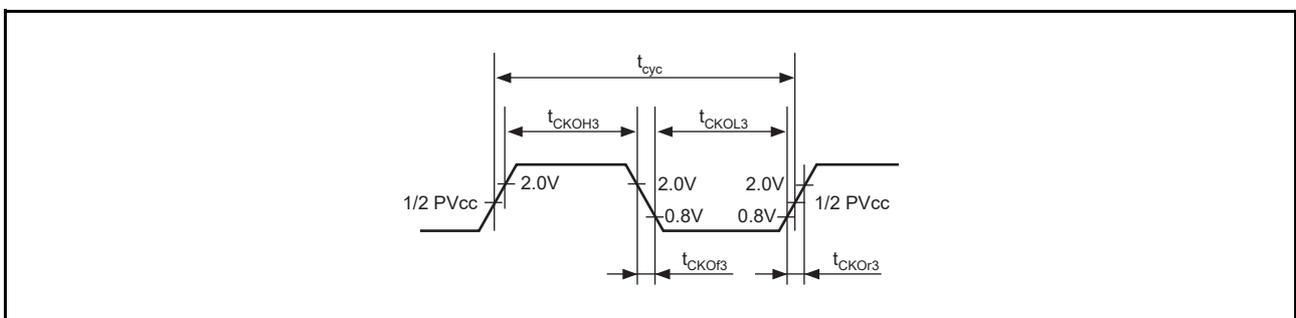


Figure 3.3        (3) CKIO Clock Output Timing 3
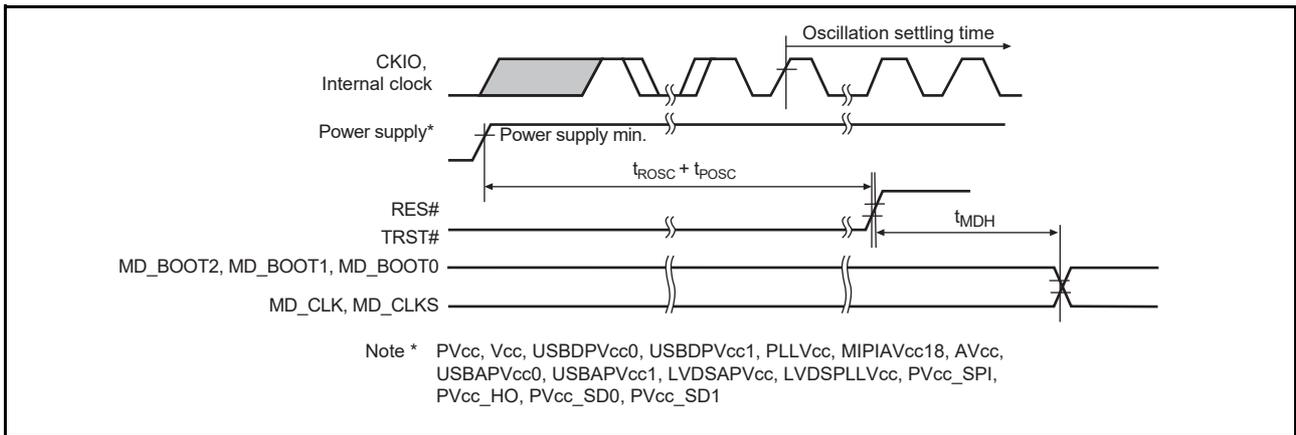
Figure 3.4 Power-On Oscillation Settling Time
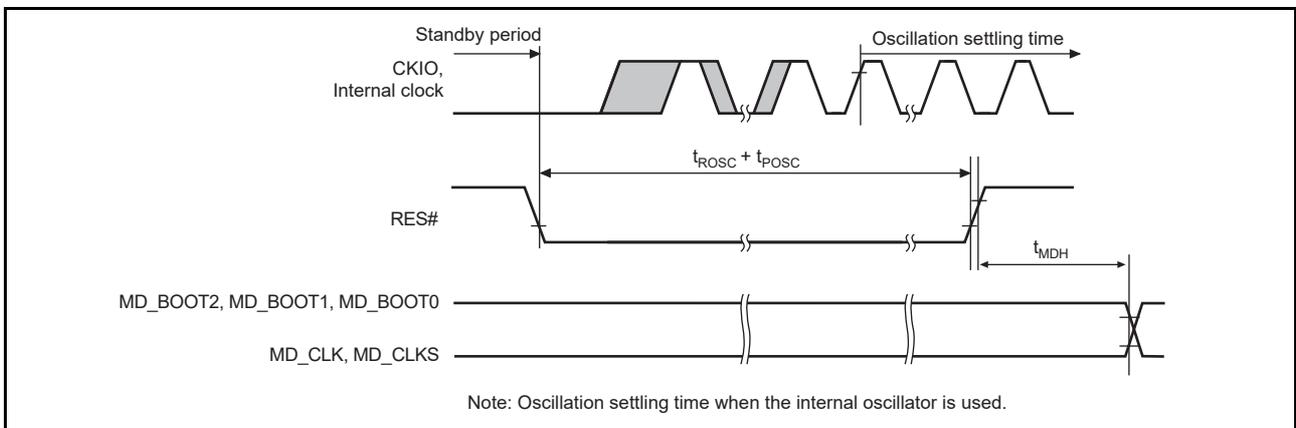


Figure 3.5 Oscillation Settling Time on Return from Standby (Return by Reset)
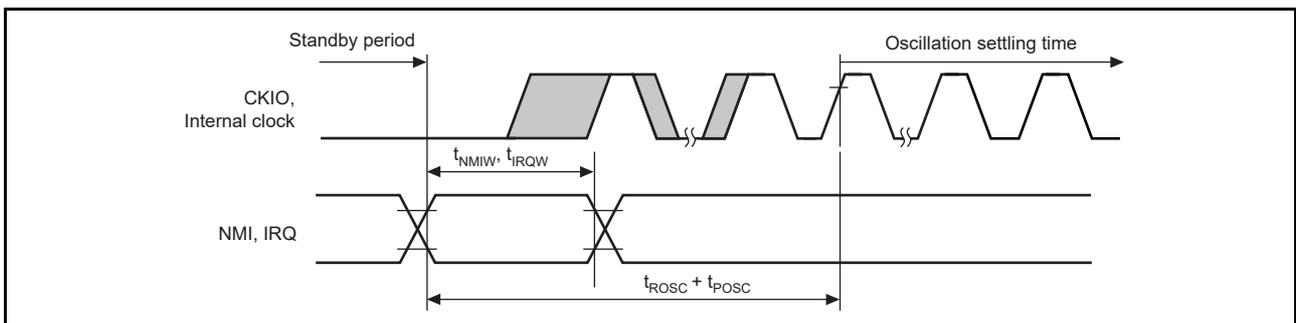


Figure 3.6 Oscillation Settling Time on Return from Standby (Return by NMI or IRQ)
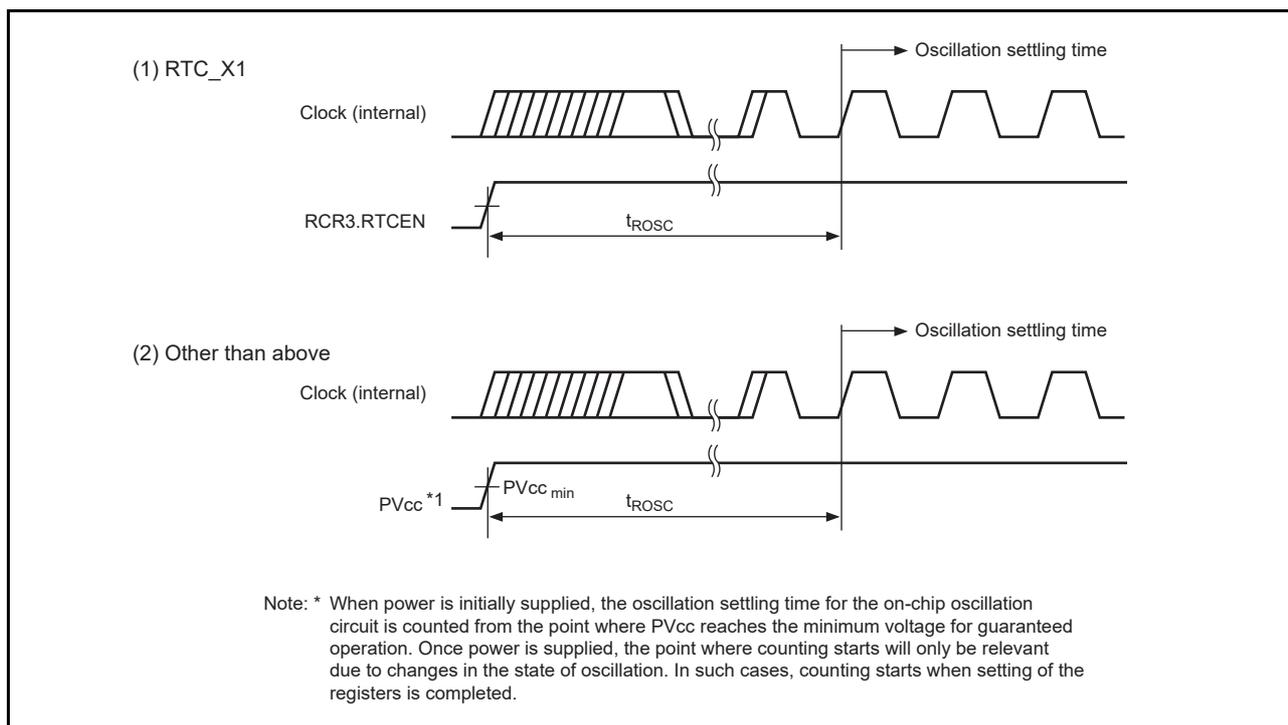
Figure 3.7      On-chip Oscillation Circuit Oscillation Settling Time

## 3.4.2      Control Signal Timing

Table 3.6        Control Signal Timing

| Item | | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|---|
| RES# pulse width | Exit from standby mode | $t_{RESW}$ | 10 | — | ms | Figure 3.8 (1) |
| | Other than above | | 20 | — | tcyc[*2] | |
| TRST# pulse width | | $t_{TRSW}$ | 20 | — | tcyc[*2] | |
| NMI pulse width | | $t_{NMIW}$ | 20 | — | tcyc[*2] | Figure 3.3 (2) , Figure 3.6 |
| IRQ pulse width | | $t_{IRQW}$ | 20 | — | tcyc[*2] | |
| TINT pulse width | | $t_{TINTW}$ | 20 | — | tcyc[*2] | |
| TINT input wait timing in the same group[*1] | | $t_{TINTGW}$ | 20 | — | tcyc[*2] | Figure 3.8 (2) |
| RES# input rise time | | $t_{RSr}$ | — | 500 | µs | Figure 3.8 (3) |

Note 1.  This restriction applies only to the same group of pin interrupts. For details, see section 51.4.4.2, Restriction on the Input from Pins in the Same Group, in the RZ/A2M Group User's Manual.
Note 2.  tcyc indicates the cycle when the setting of the CKIOSEL bits in the CKIO select register is 2'b01 (initial value).
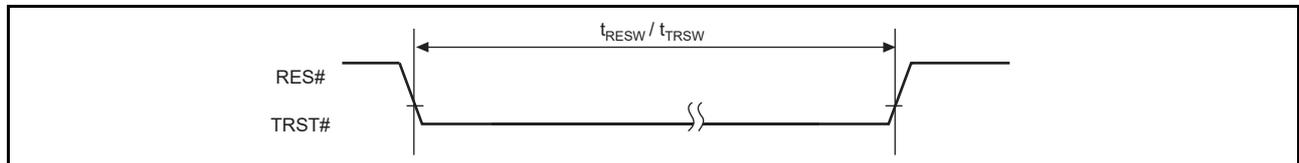


Figure 3.8        (1) Reset Input Timing 1
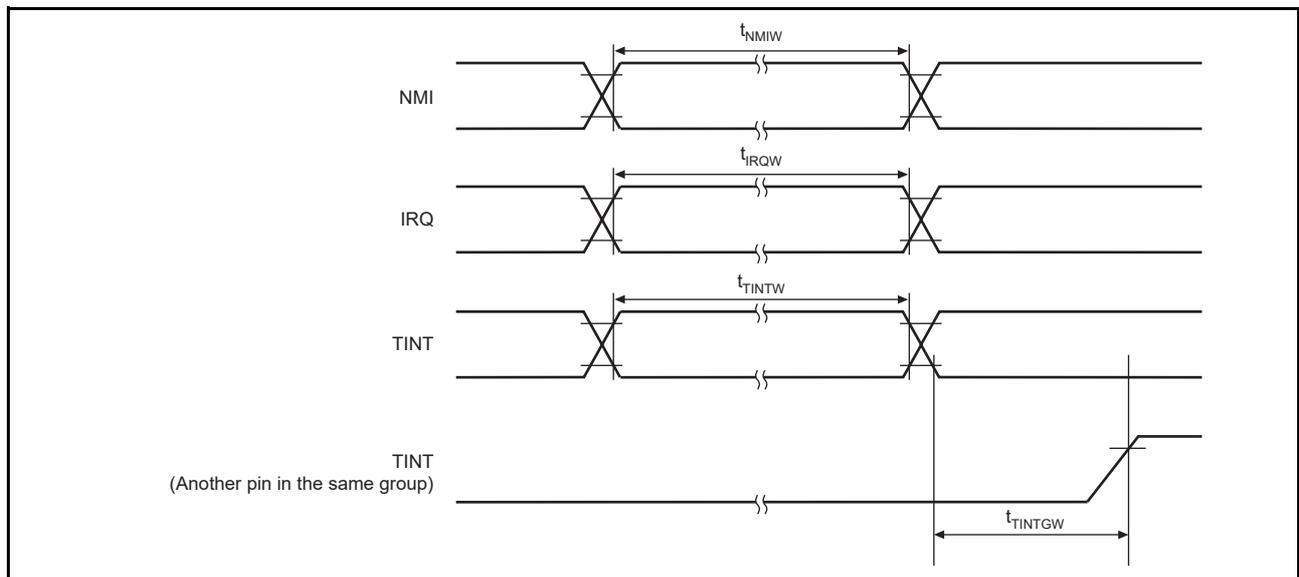


Figure 3.8        (2) Interrupt Signal Input Timing
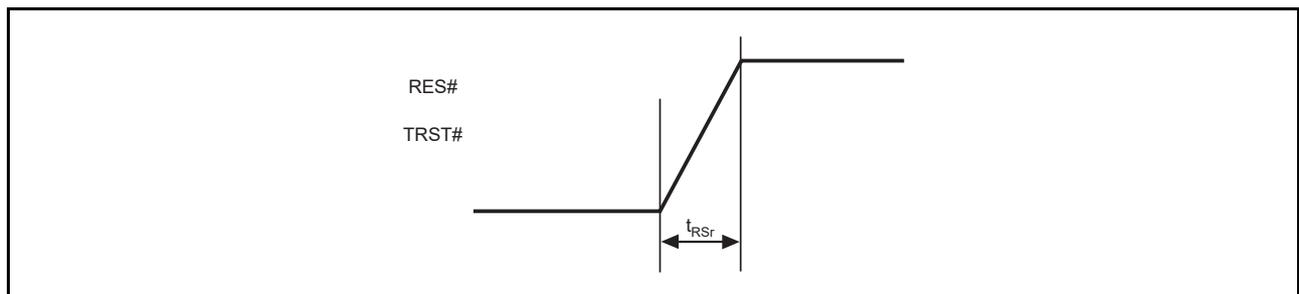


Figure 3.8        (3) Reset Input Timing 2

### 3.4.3   SPI Multi I/O Bus Controller, Octa Memory/HyperBus™ Controller Reset Output Timing

Table 3.7        SPI Multi I/O Bus Controller,Octa Memory/HyperBus™ Controller Reset Output Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| Memory reset pulse width | $t_{RP}$ | 2500 | — | $t_{p0cyc}$ | Figure 3.9 to Figure 3.12 |
| Memory reset (negate) to memory access time | $t_{RH}$ | 500 | — | $t_{p0cyc}$ | |

Note:  $t_{p0cyc}$ indicates the peripheral clock 0 (P0φ) cycle.
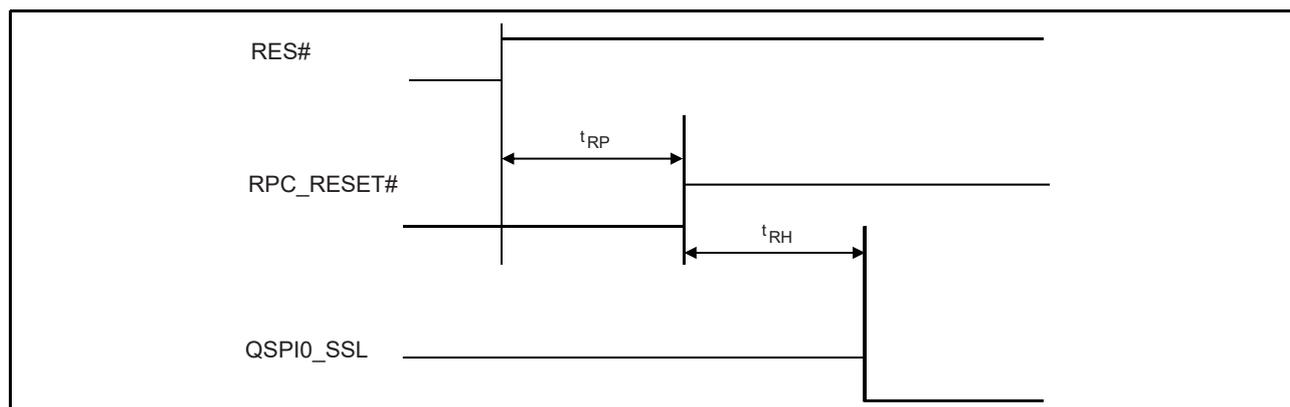


Figure 3.9        SPI Multi I/O Bus Controller Reset Output Timing after a power-on reset (Boot Modes 3, 4, and 5)
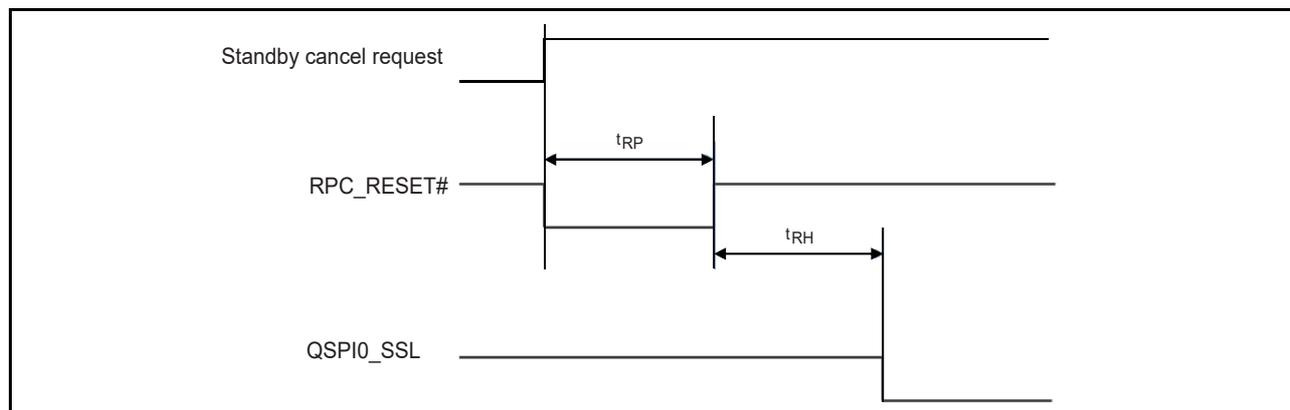


Figure 3.10      SPI Multi I/O Bus Controller Reset Output Timing after recovery from deep standby (Boot Modes 3, 4, and 5)
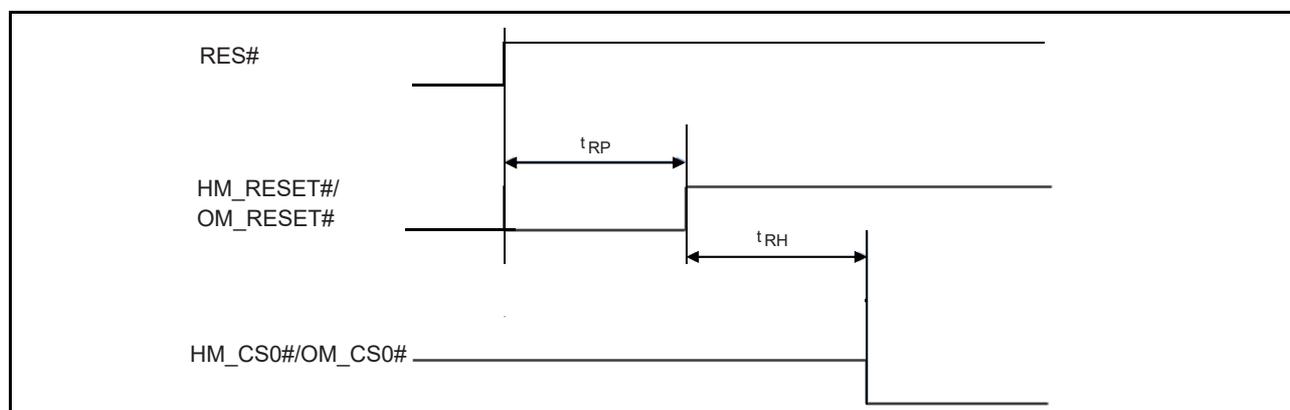


Figure 3.11      Octa Memory/HyperBus™ Controller Reset Output Timing after a power-on reset (Boot Modes 6 and 7)
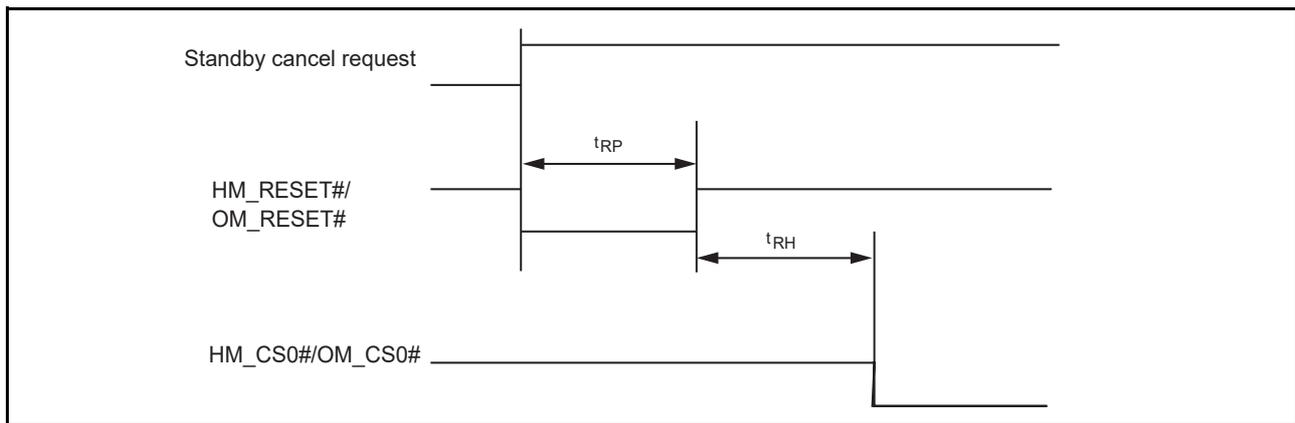
Figure 3.12      Octa Memory/HyperBus™ Controller Reset Output Timing after recovery from deep standby (Boot Modes 6 and 7)

### 3.4.4 Bus Timing

Table 3.8 Bus Timing

| Item | Symbol | CKIO = 132 MHz[1] Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| Address delay time 1 | $t_{AD1}$ | 2.0 | 4.8 | ns | Figure 3.13 to Figure 3.37 |
| Address delay time 2 | $t_{AD2}$ | $1/2\ t_{cyc}$ | $1/2\ t_{cyc} + 8$ [3] | ns | Figure 3.20 |
| Address setup time | $t_{AS}$ | 0 | — | ns | Figure 3.13 to Figure 3.16, Figure 3.20 |
| Chip enable setup time | $t_{cs}$ | 0 | — | ns | Figure 3.13 to Figure 3.16, Figure 3.20 |
| Address hold time | $t_{AH}$ | 0 | — | ns | Figure 3.13 to Figure 3.16 |
| BS delay time | $t_{BSD}$ | — | 4.8 | ns | Figure 3.13 to Figure 3.34 |
| CS delay time 1 | $t_{CSD1}$ | 2.0 | 4.8 | ns | Figure 3.13 to Figure 3.37 |
| Read write delay time 1 | $t_{RWD1}$ | 2.0 | 4.8 | ns | Figure 3.13 to Figure 3.37 |
| Read strobe delay time | $t_{RSD}$ | $1/2\ t_{cyc}$ | $1/2\ t_{cyc} + 12$ [3] | ns | Figure 3.13 to Figure 3.20 |
| Read data setup time 1 | $t_{RDS1}$ | $1/2\ t_{cyc} + 5$ [3] | — | ns | Figure 3.13 to Figure 3.19 |
| Read data setup time 2 | $t_{RDS2}$ | 2.0 | — | ns | Figure 3.21 to Figure 3.24, Figure 3.29 to Figure 3.31 |
| Read data setup time 3 | $t_{RDS3}$ | $1/2\ t_{cyc} + 5$ [3] | — | ns | Figure 3.20 |
| Read data hold time 1 | $t_{RDH1}$ | 0 | — | ns | Figure 3.13 to Figure 3.19 |
| Read data hold time 2 | $t_{RDH2}$ | 2.5 | — | ns | Figure 3.21 to Figure 3.24, Figure 3.29 to Figure 3.31 |
| Read data hold time 3 | $t_{RDH3}$ | 0 | — | ns | Figure 3.20 |
| Write enable delay time 1 | $t_{WED1}$ | $1/2\ t_{cyc}$ | $1/2\ t_{cyc} + 12$ [3] | ns | Figure 3.13 to Figure 3.18 |
| Write enable delay time 2 | $t_{WED2}$ | — | 4.8 | ns | Figure 3.19 |
| Write data delay time 1 | $t_{WDD1}$ | — | 4.8 | ns | Figure 3.13 to Figure 3.19 |
| Write data delay time 2 | $t_{WDD2}$ | — | 4.8 | ns | Figure 3.25 to Figure 3.28, Figure 3.32 to Figure 3.34 |
| Write data hold time 1 | $t_{WDH1}$ | 2.0 | — | ns | Figure 3.13 to Figure 3.19 |
| Write data hold time 2 | $t_{WDH2}$ | 2.0 | — | ns | Figure 3.25 to Figure 3.28, Figure 3.32 to Figure 3.34 |
| Write data hold time 4 | $t_{WDH4}$ | 0 | — | ns | Figure 3.13 to Figure 3.17 |
| WAIT setup time | $t_{WTS}$ | $1/2\ t_{cyc} + 5.0$ [3] | — | ns | Figure 3.14 to Figure 3.20 |
| WAIT hold time | $t_{WTH}$ | $1/2\ t_{cyc} + 3.5$ [3] | — | ns | Figure 3.14 to Figure 3.20 |
| RAS delay time 1 | $t_{RASD1}$ | 2.0 | 4.8 | ns | Figure 3.21 to Figure 3.37 |
| CAS delay time 1 | $t_{CASD1}$ | 2.0 | 4.8 | ns | Figure 3.21 to Figure 3.37 |
| DQM delay time 1 | $t_{DQMD1}$ | 2.0 | 4.8 | ns | Figure 3.21 to Figure 3.34 |
| CKE delay time 1 | $t_{CKED1}$ | 2.0 | 4.8 | ns | Figure 3.36 |
| AH delay time | $t_{AHD}$ | $1/2\ t_{cyc}$ | $1/2\ t_{cyc} + 12$ [3] | ns | Figure 3.17 |
| Multiplexed address delay time | $t_{MAD}$ | — | 12[3] | ns | Figure 3.17 |
| Multiplexed address hold time | $t_{MAH}$ | 1.0[3] | — | ns | Figure 3.17 |
| Address setup time for AH | $t_{AVVH}$ | $1/2\ t_{cyc} - 2$ | — | ns | Figure 3.17 |
| DACK, TEND delay time | $t_{DACD}$ | Refer to the direct memory access controller timing | | ns | Figure 3.13 to Figure 3.34 |

Note 1. The maximum value ($f_{max}$) of CKIO (external bus clock) depends on the number of wait cycles and the system configuration of your board.

Note 2. $1/2\ t_{cyc}$ indicated in minimum and maximum values for the item of delay, setup, and hold times represents a half cycle from the rising edge with a clock. That is, $1/2$ tcyc describes a reference of the falling edge with a clock.

Note 3. These values specified are for 66 MHz max operation. For CKIO = 110 to 132 MHz operation, some wait cycle insertion and input timing design are required depending on the system configuration.
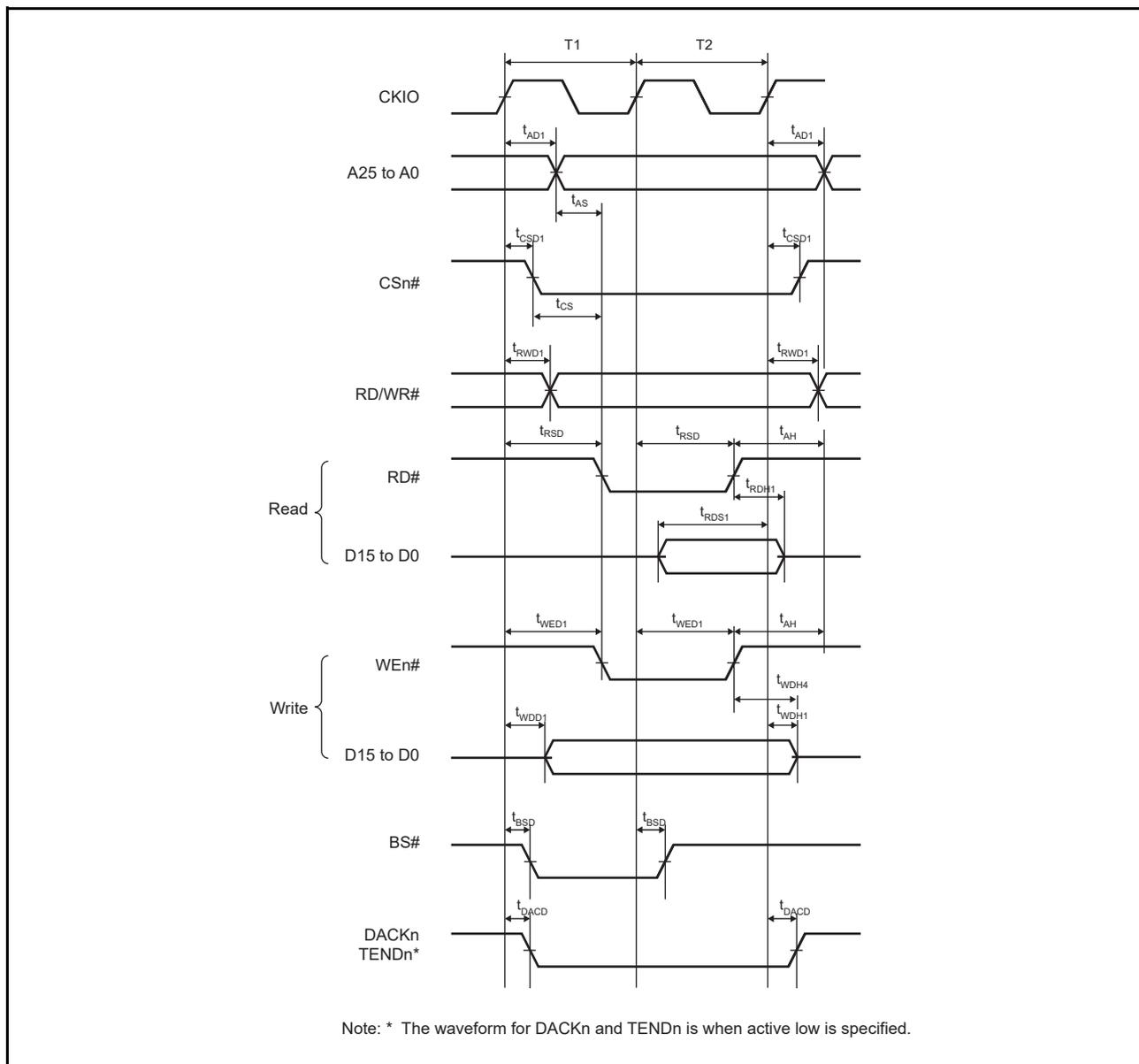
Figure 3.13      Basic Bus Timing for Normal Space (No Wait)
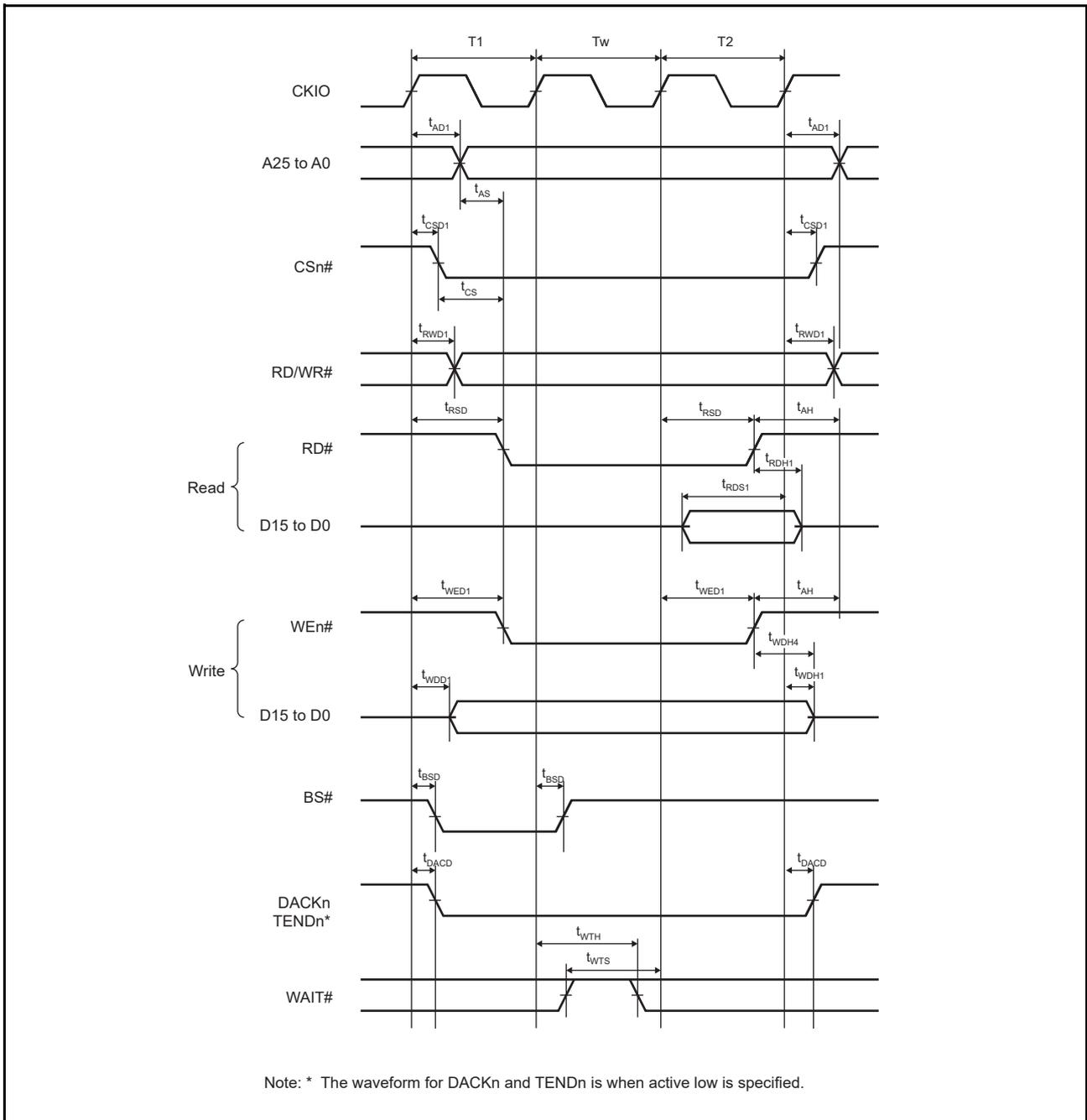
Figure 3.14        Basic Bus Timing for Normal Space (One Software Wait Cycle)
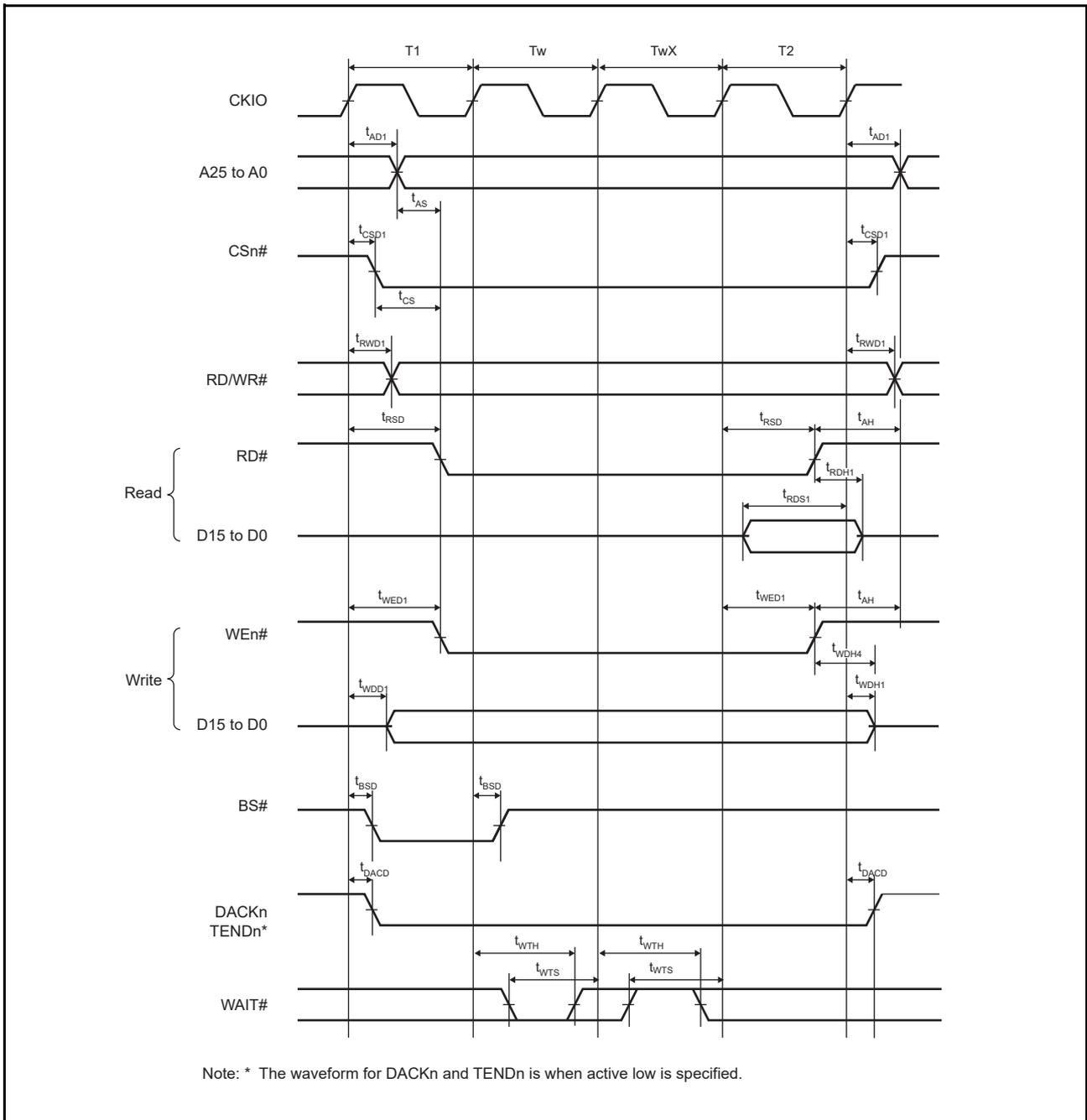
Figure 3.15      Basic Bus Timing for Normal Space (One Software Wait Cycle, One External Wait Cycle)
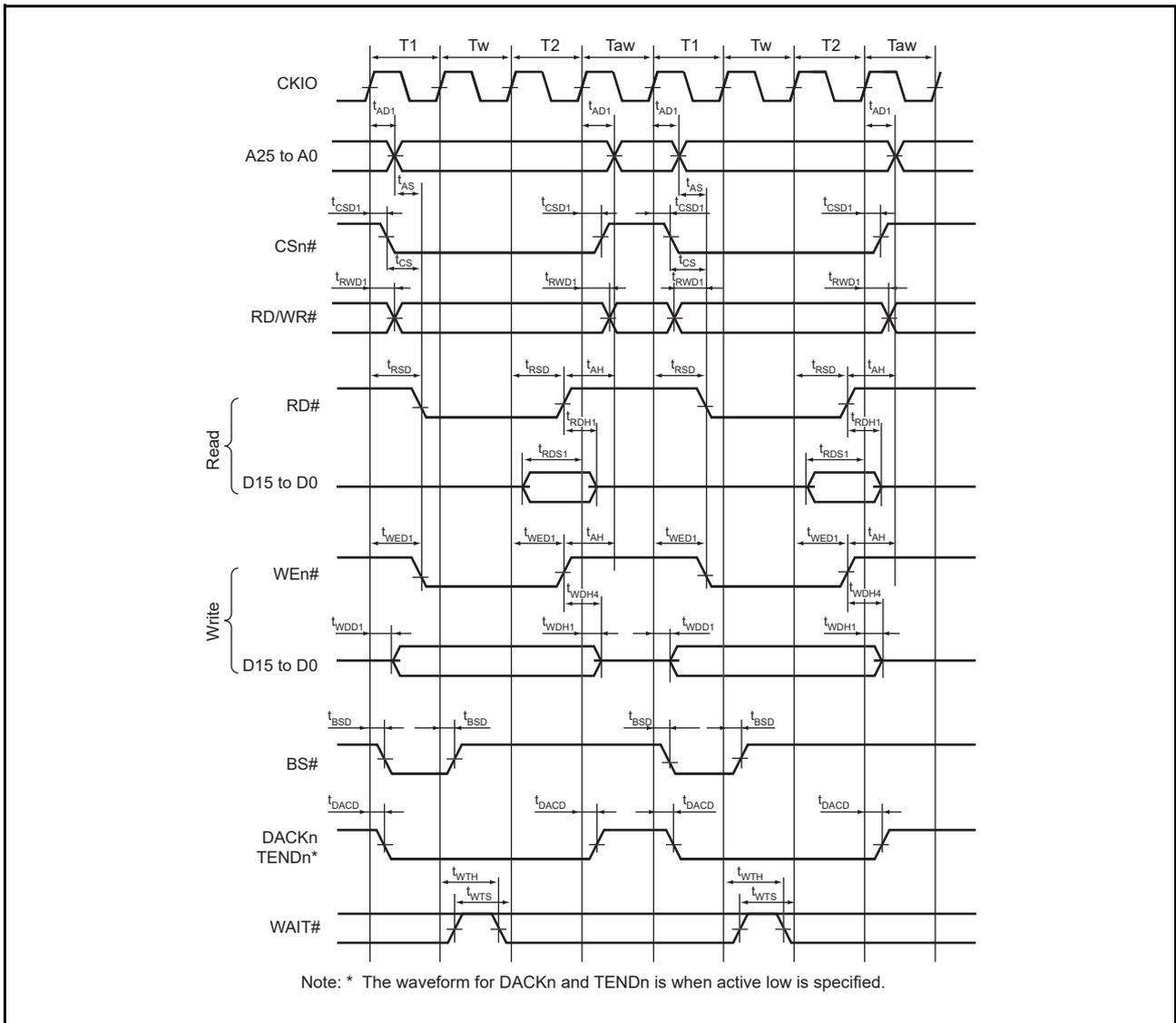
Figure 3.16    Basic Bus Timing for Normal Space (One Software Wait Cycle, External Wait Cycle Valid (WM Bit = 0), No Idle Cycle)
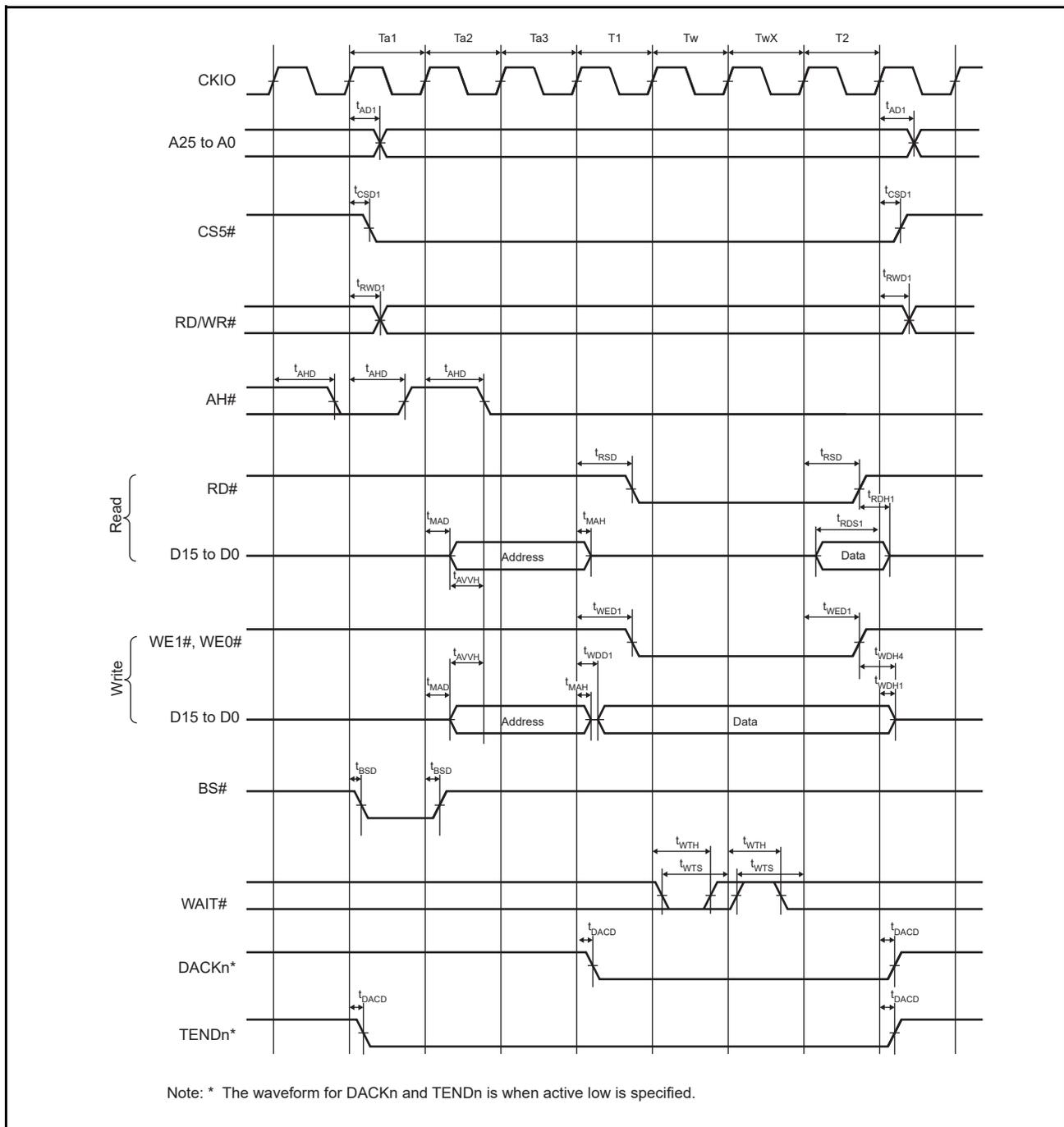
Figure 3.17    MPX-I/O Interface Bus Cycle (Three Address Cycles, One Software Wait Cycle, One External Wait Cycle)
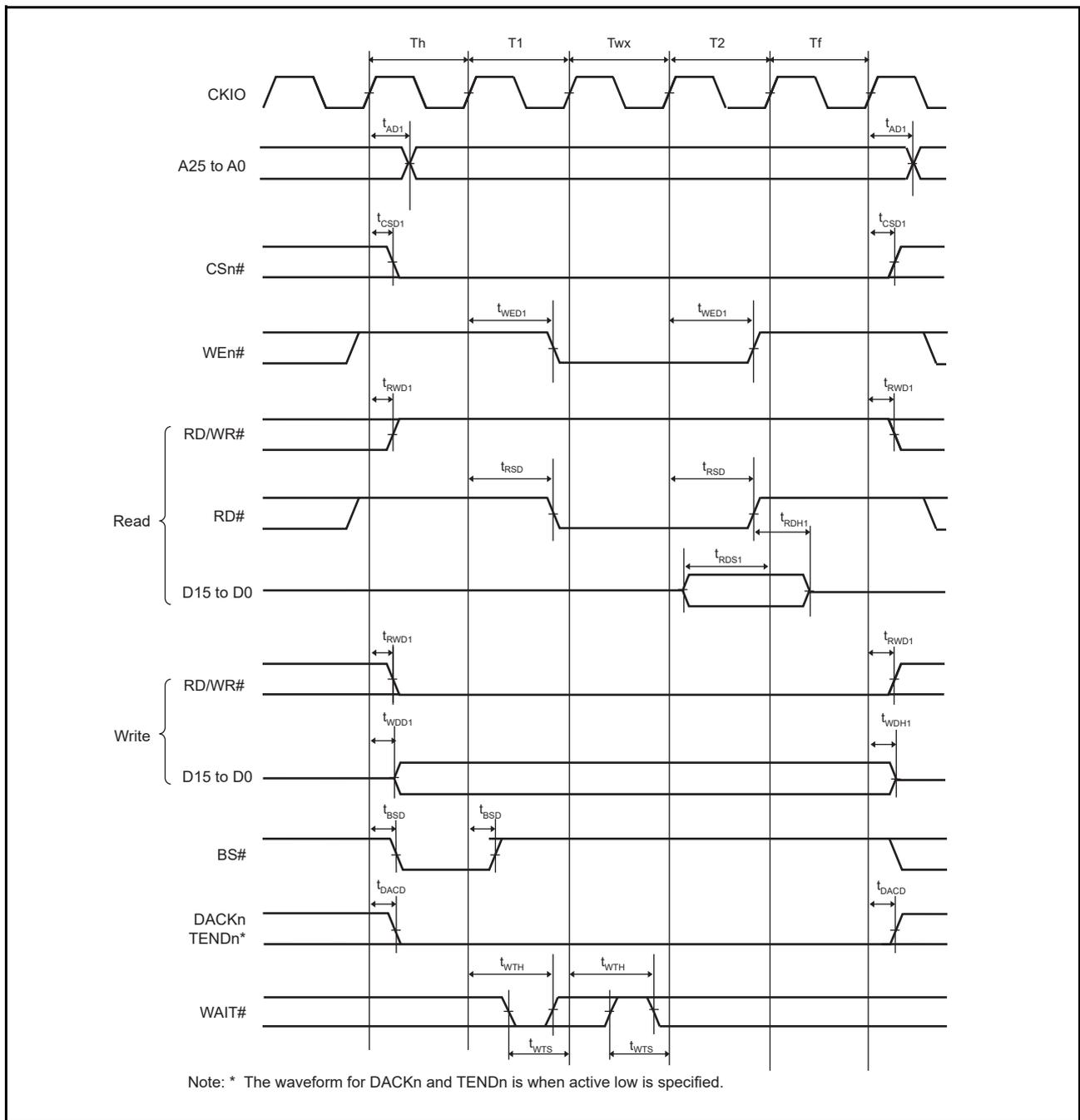
Figure 3.18   Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 0 (Write Cycle UB#/LB# Control))
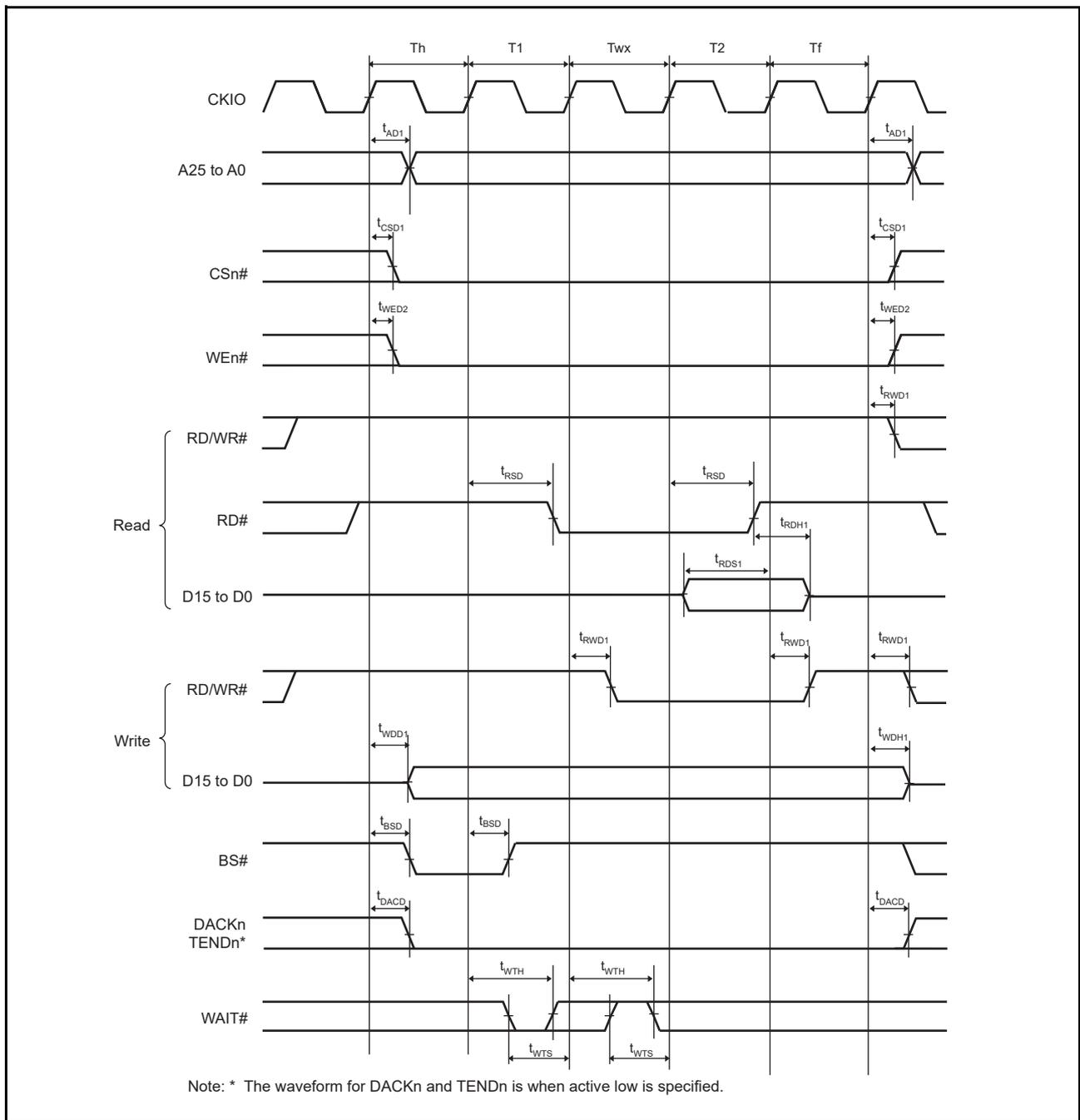
Figure 3.19     Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 1 (Write Cycle WE# Control))
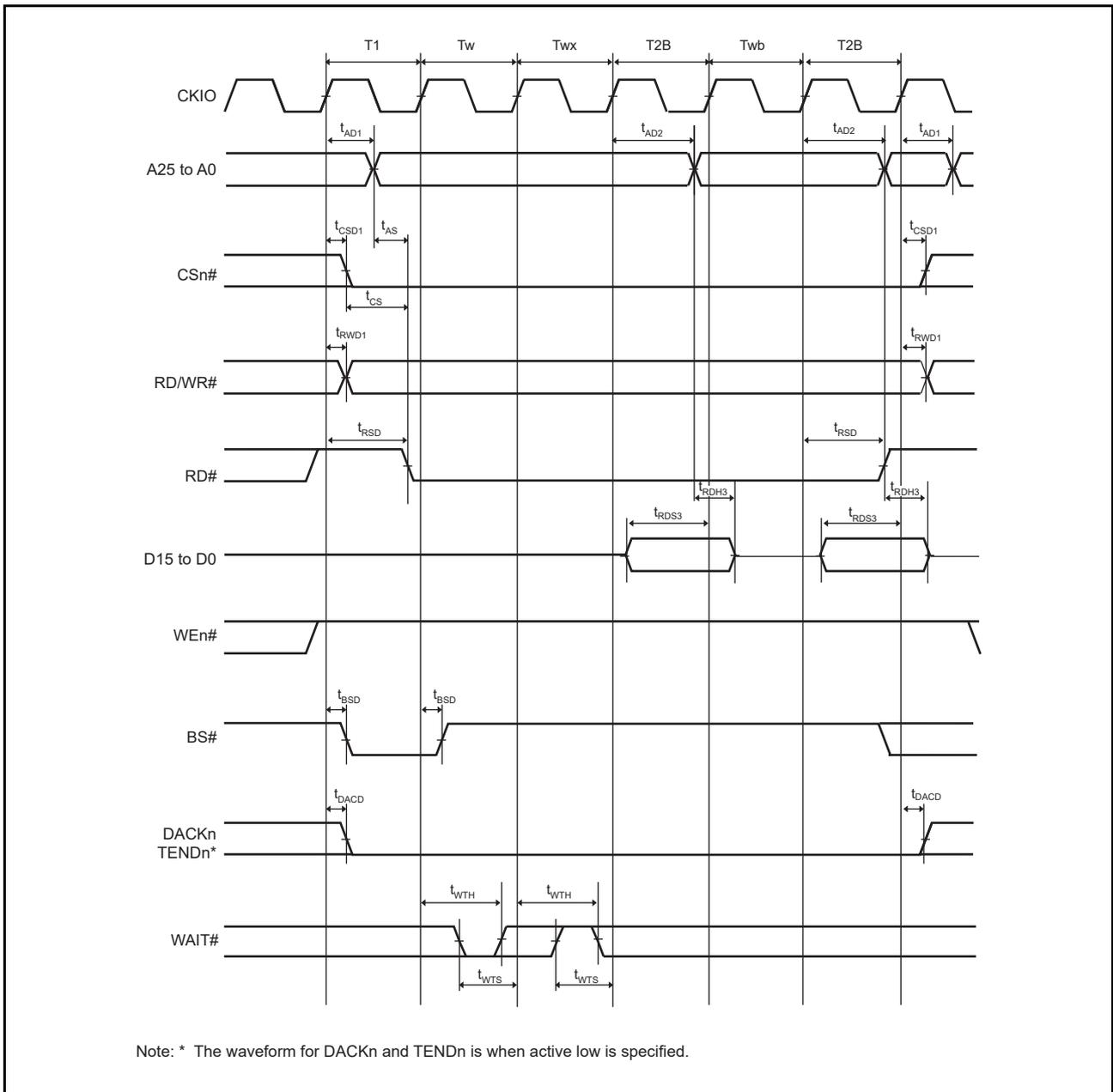
Figure 3.20    Burst ROM Read Cycle (One Software Wait Cycle, One Asynchronous External Burst Wait Cycle, Two Burst)

Notes:  1.   An address pin to be connected to pin A10 of SDRAM.
        2.   The waveform for DACKn and TENDn is when active low is specified.
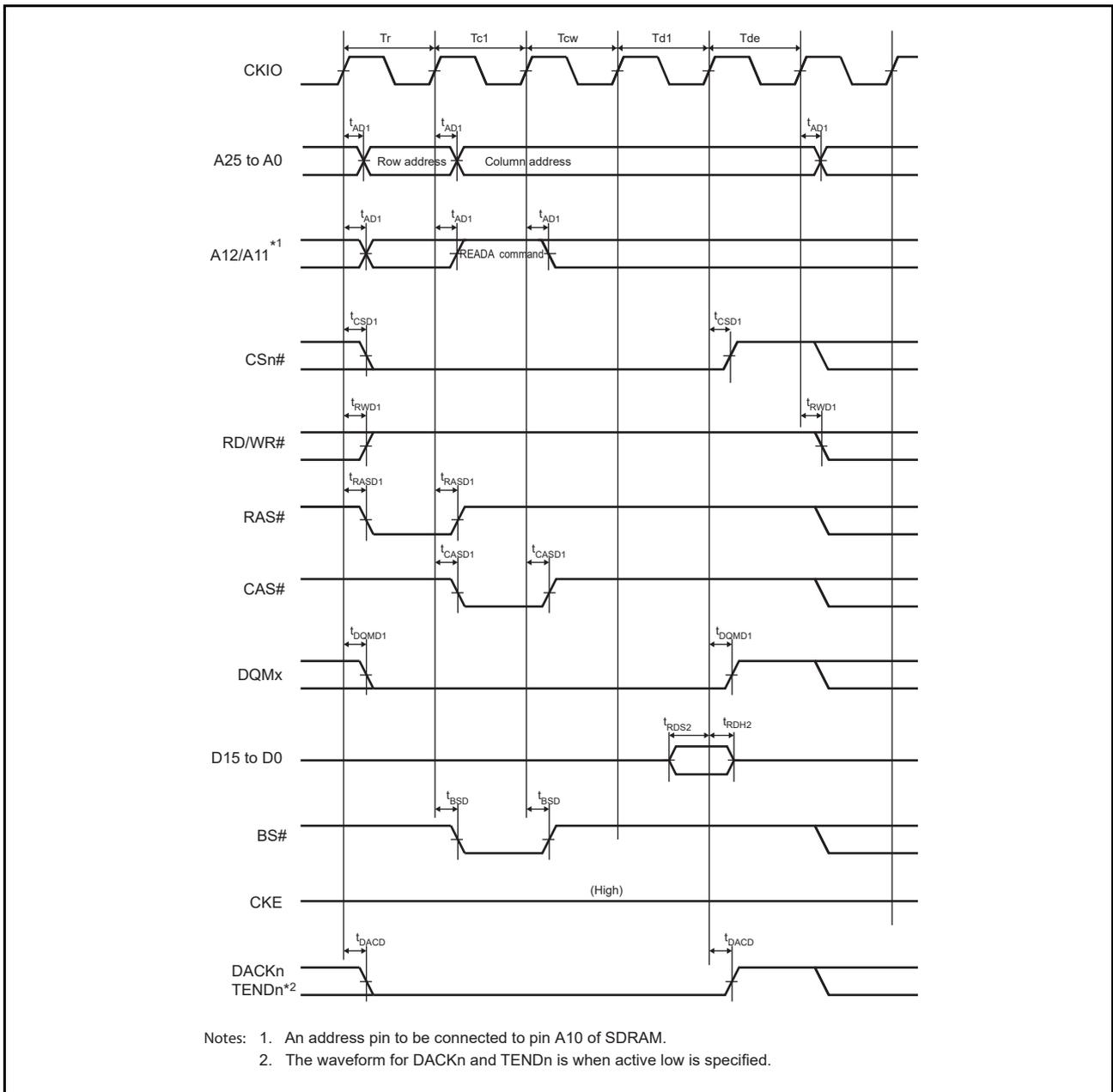
Figure 3.21    Synchronous DRAM Single Read Bus Cycle (Auto Precharge, CAS Latency 2, WTRCD = 0 Cycle, WTRP = 0 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.
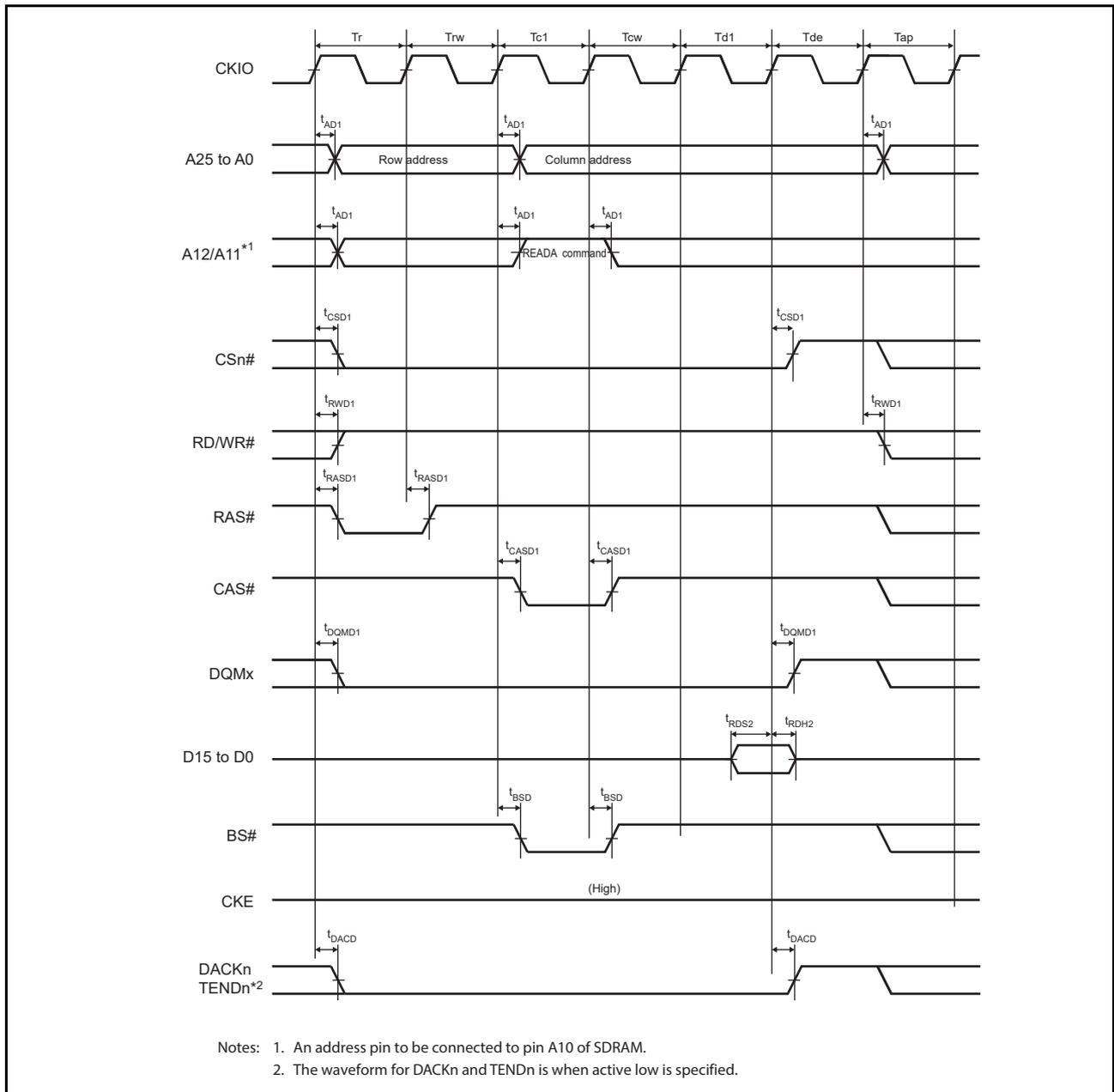
Figure 3.22 Synchronous DRAM Single Read Bus Cycle (Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)
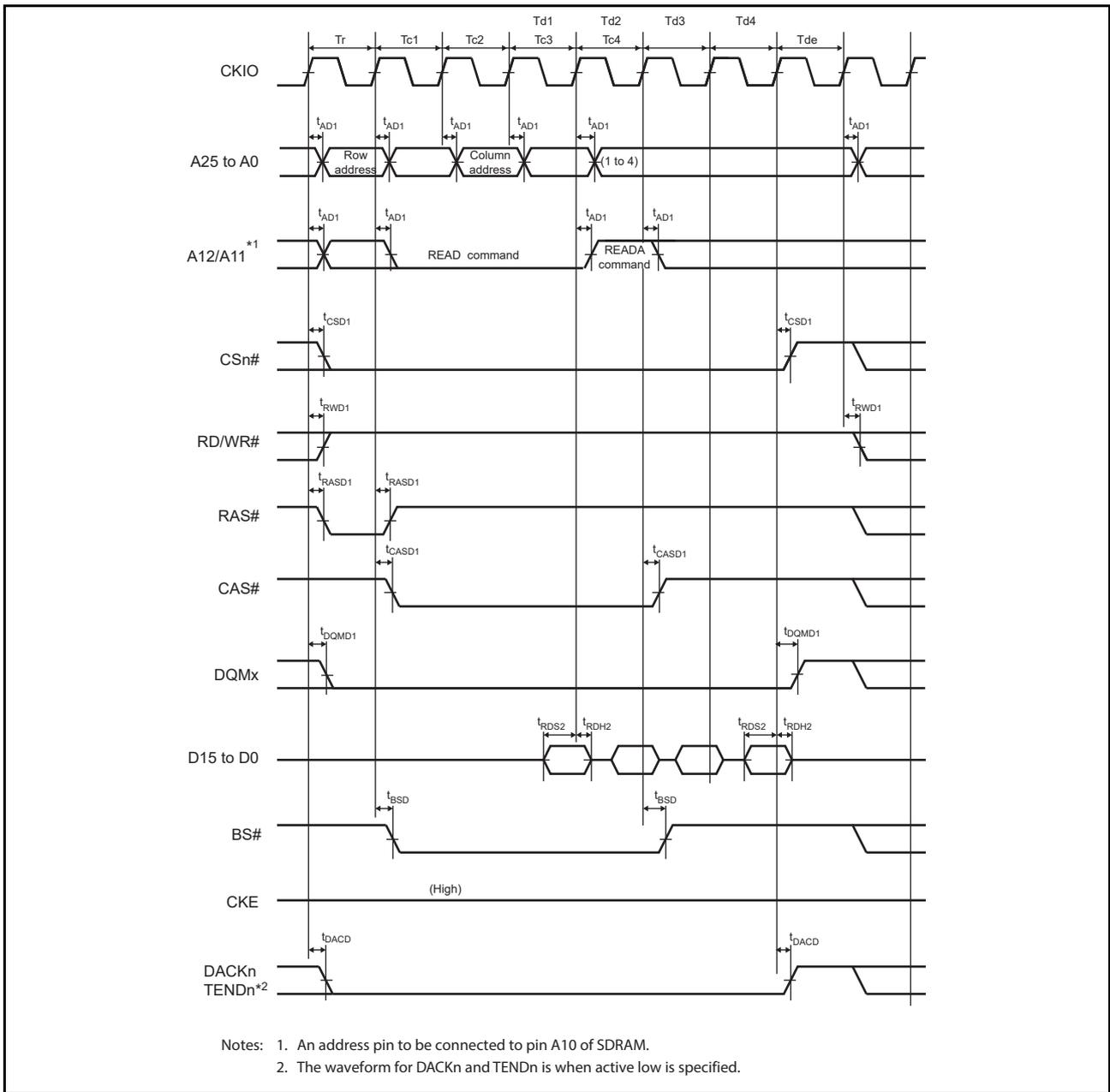
Figure 3.23    Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Auto Precharge, CAS Latency 2, WTRCD = 0 Cycle, WTRP = 1 Cycle)
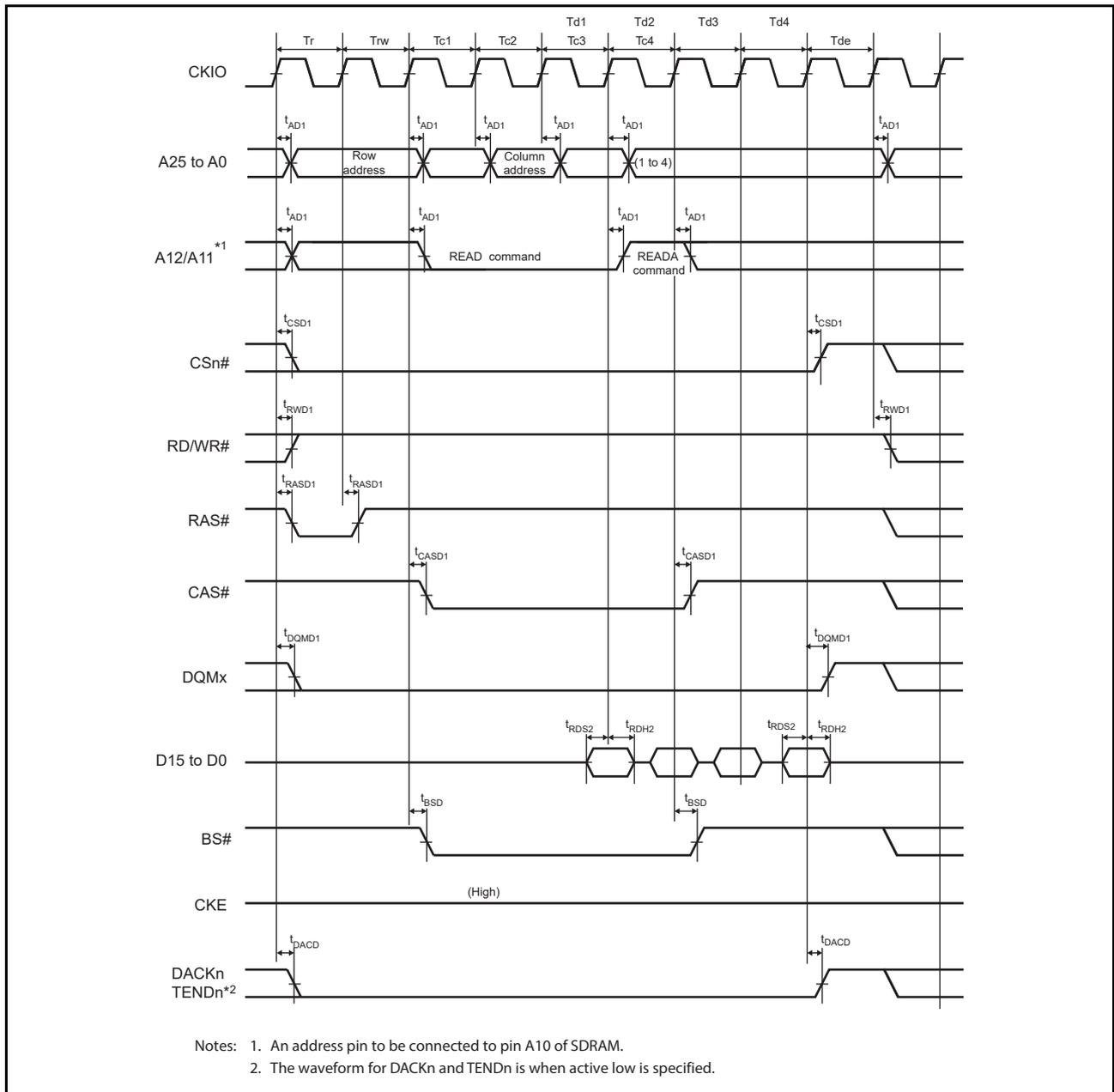
Figure 3.24    Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 0 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.
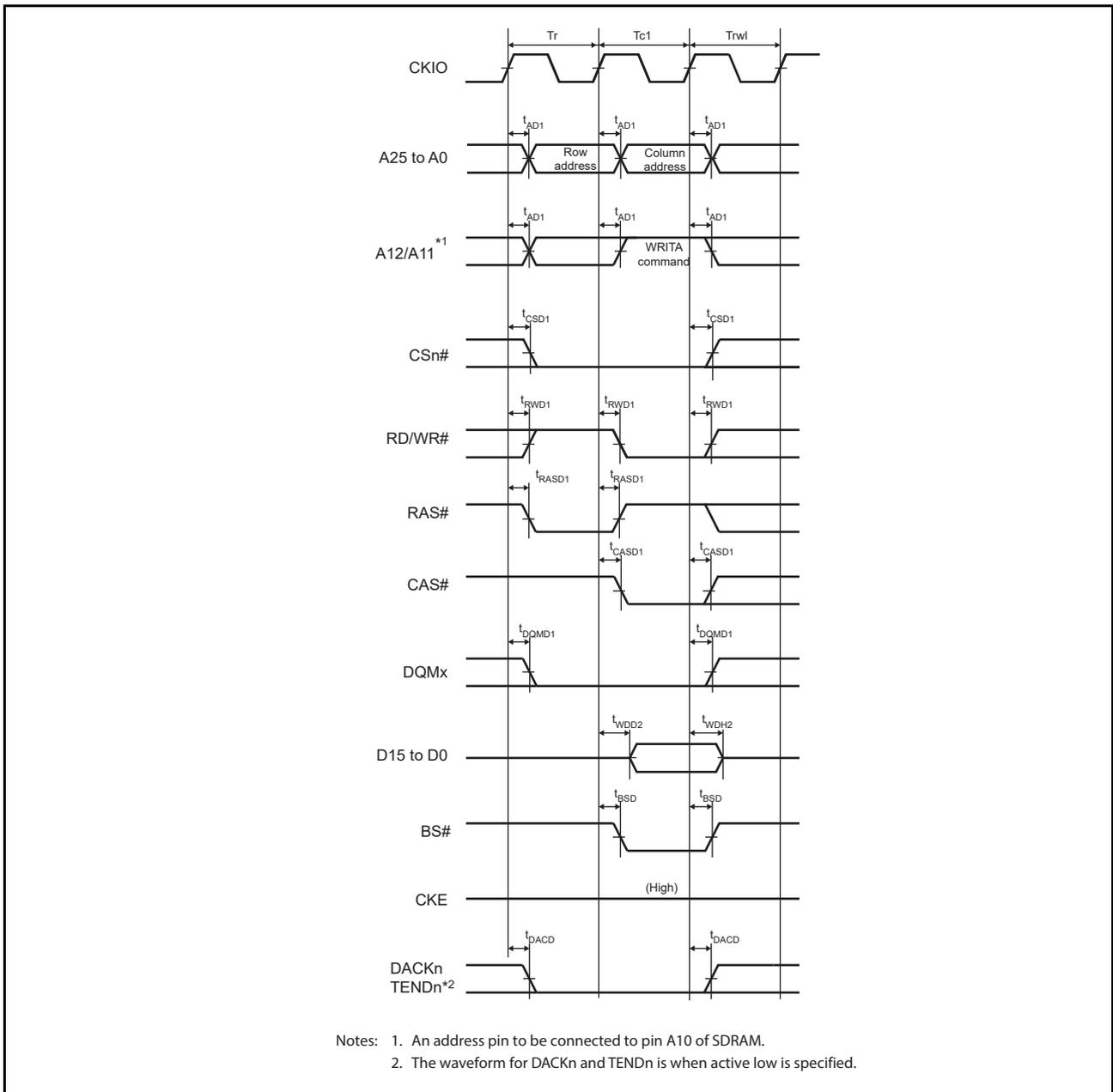
Figure 3.25        Synchronous DRAM Single Write Bus Cycle (Auto Precharge, TRWL = 1 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.
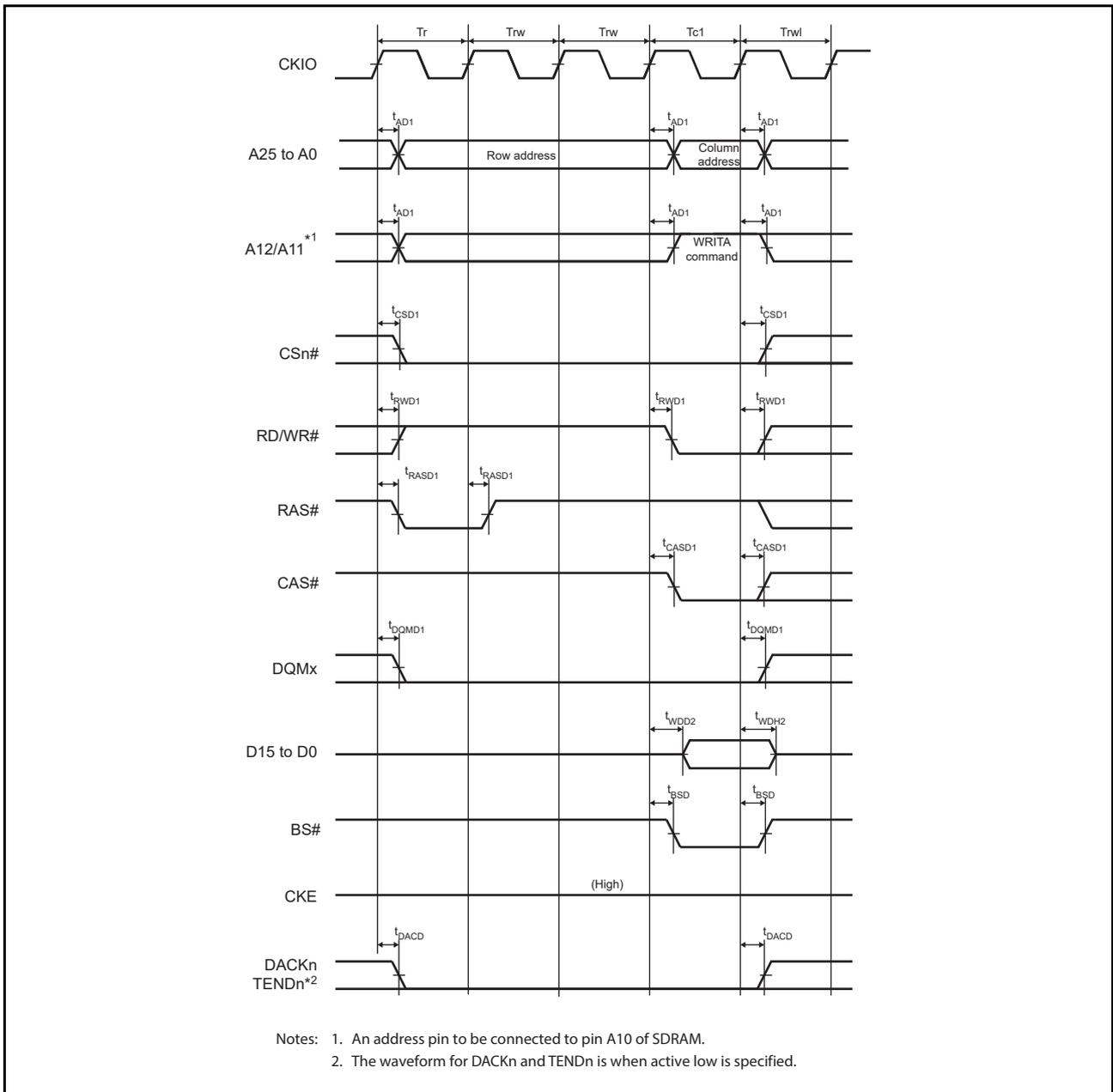
Figure 3.26    Synchronous DRAM Single Write Bus Cycle (Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)
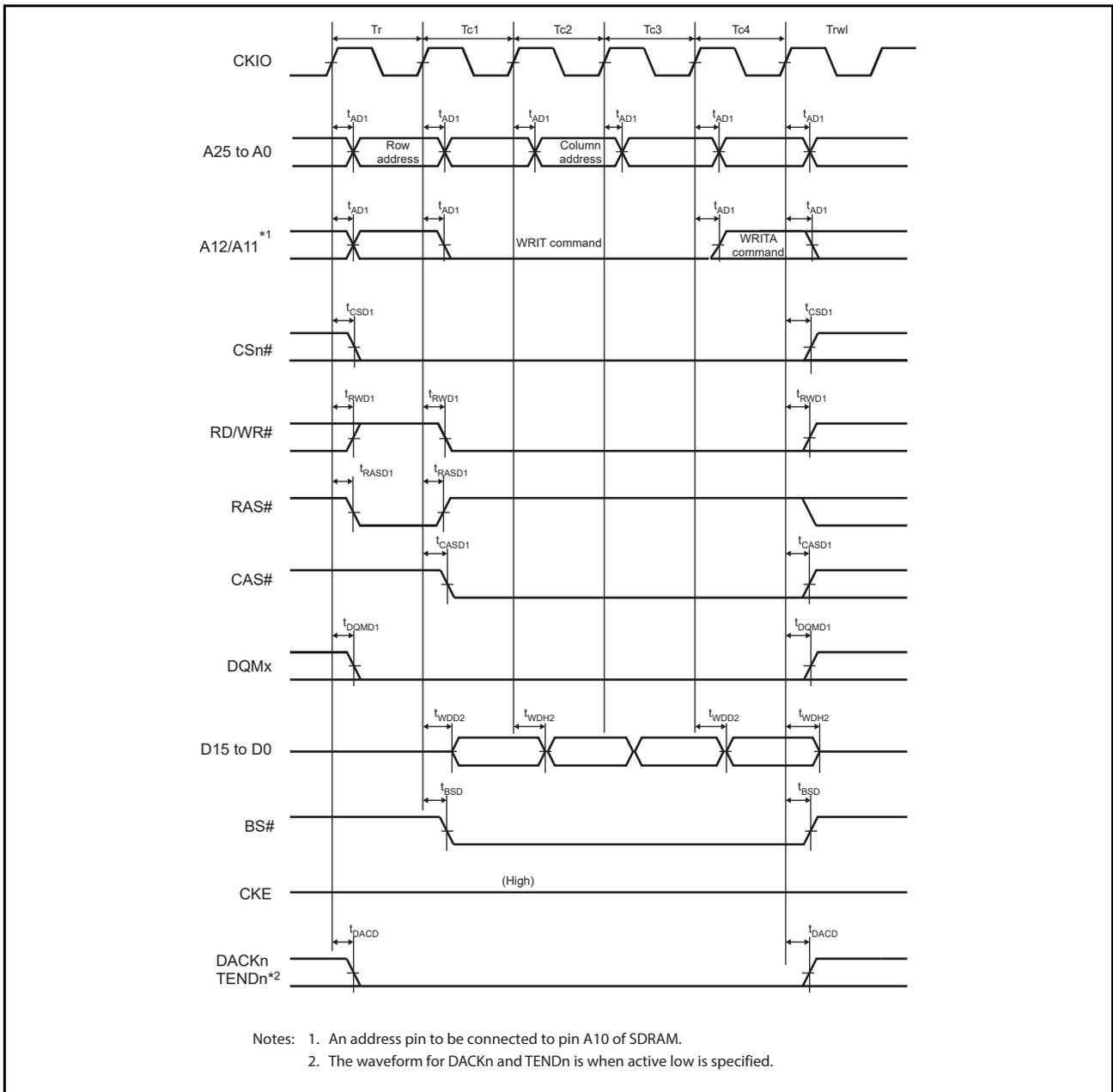
Figure 3.27    Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Auto Precharge, WTRCD = 0 Cycle, TRWL = 1 Cycle)

Notes:  1.  An address pin to be connected to pin A10 of SDRAM.
        2.  The waveform for DACKn and TENDn is when active low is specified.
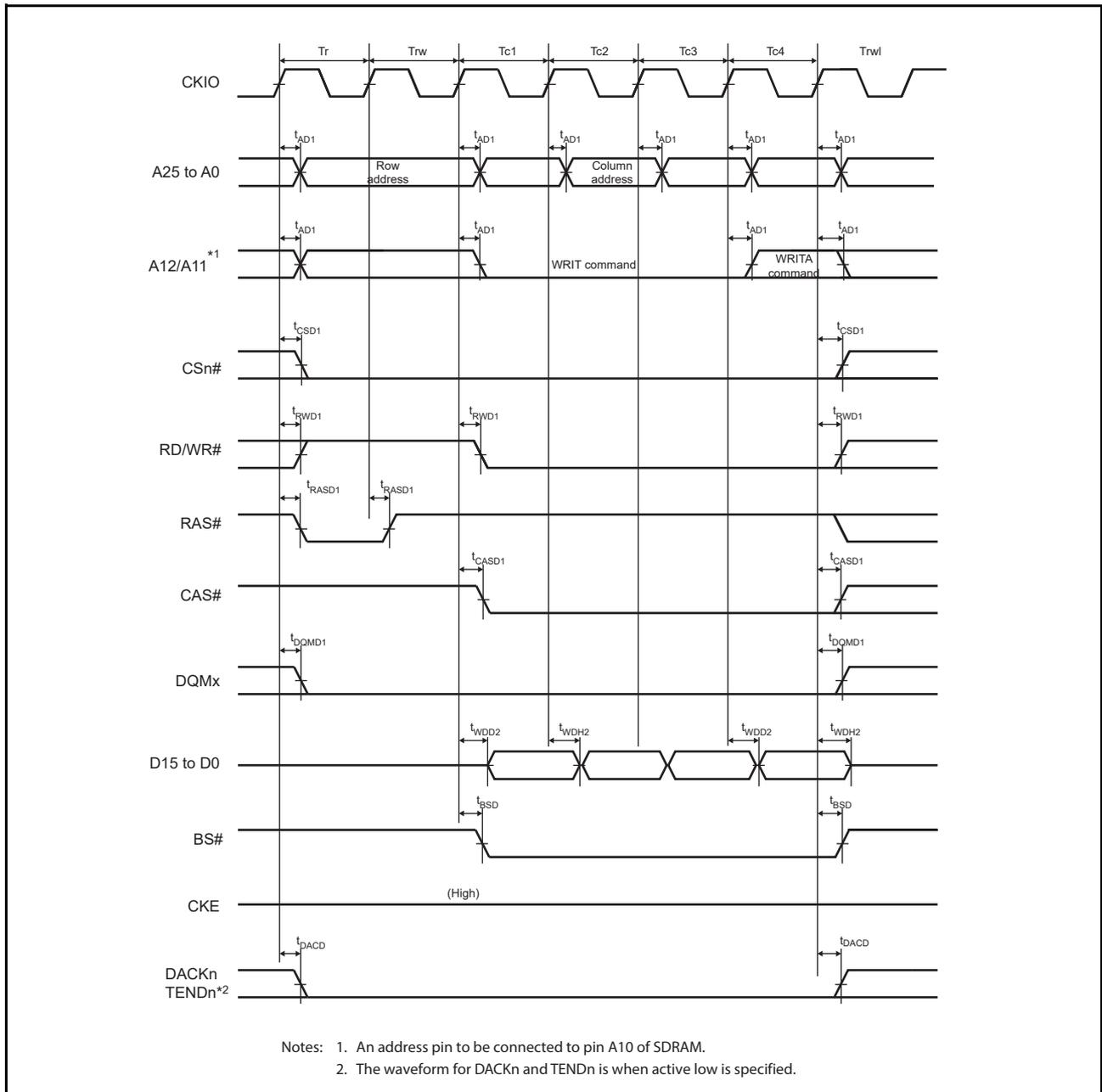
Figure 3.28	Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Auto Precharge, WTRCD = 1 Cycle, TRWL = 1 Cycle)
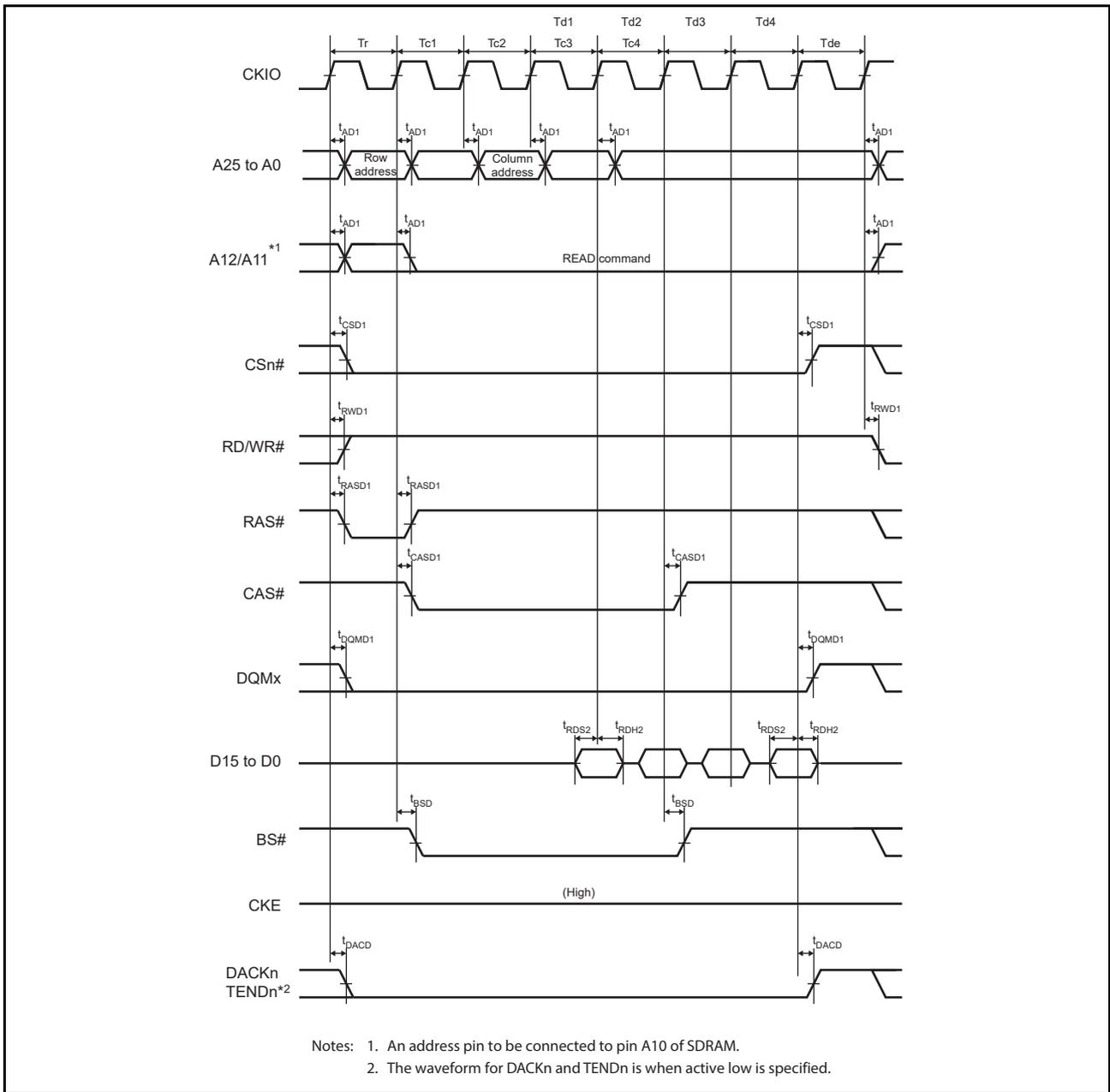
Figure 3.29 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: ACT + READ Commands, CAS Latency 2, WTRCD = 0 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.
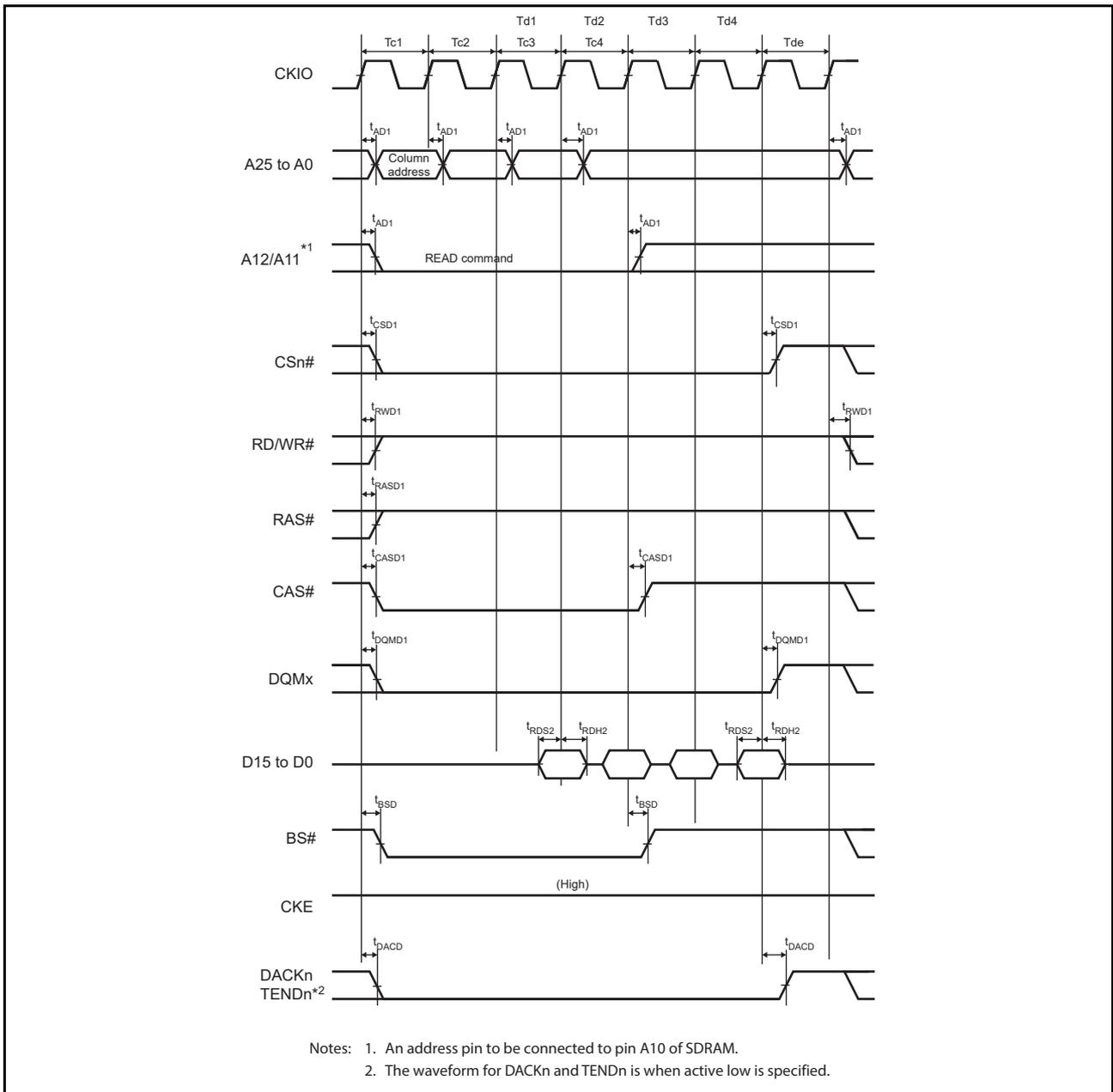
Figure 3.30    Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: READ Command, Same Row Address, CAS Latency 2, WTRCD = 0 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
       2. The waveform for DACKn and TENDn is when active low is specified.
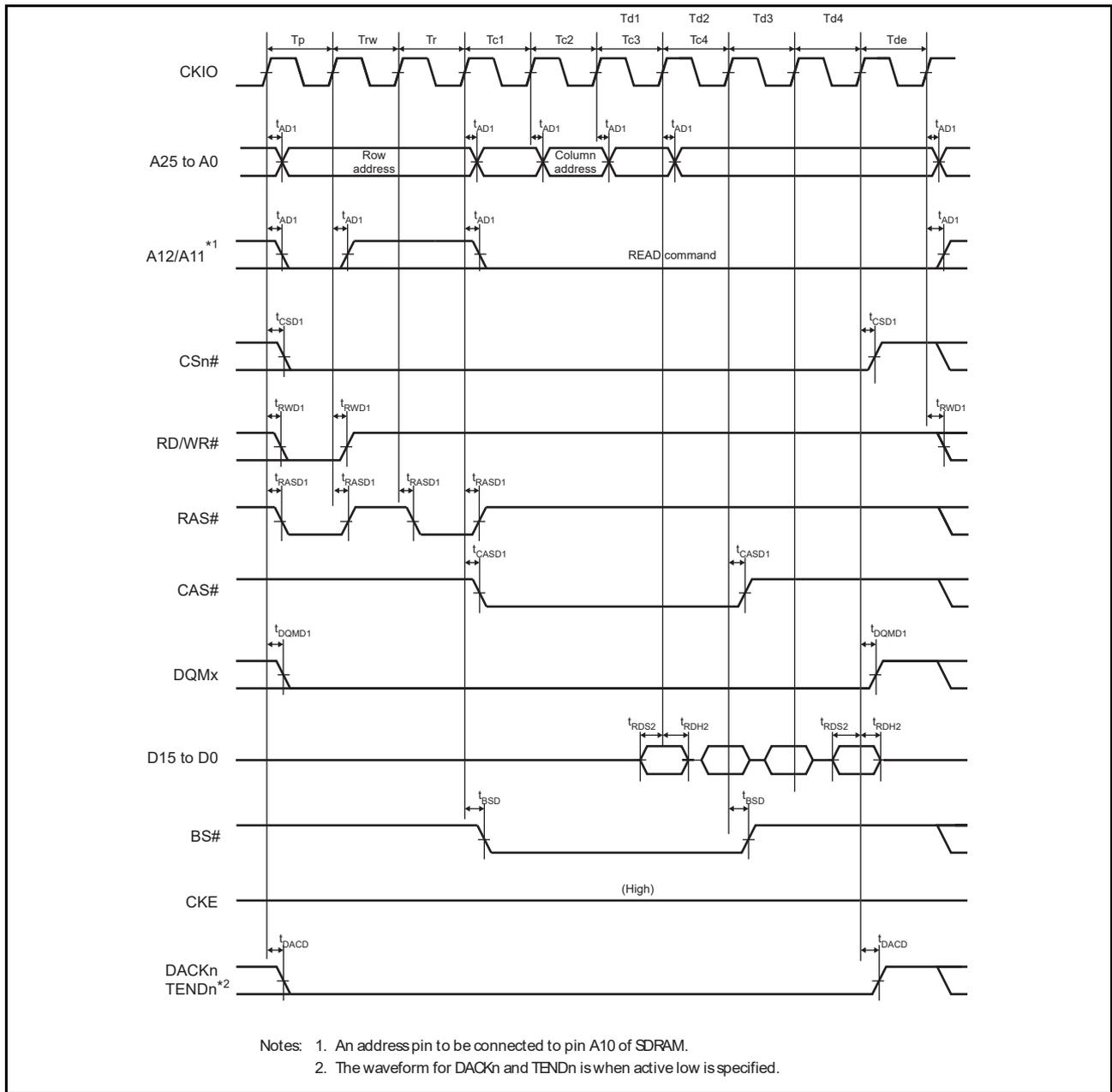
Figure 3.31    Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: PRE + ACT + READ Commands, Different Row Addresses, CAS Latency 2, WTRCD = 0 Cycle)
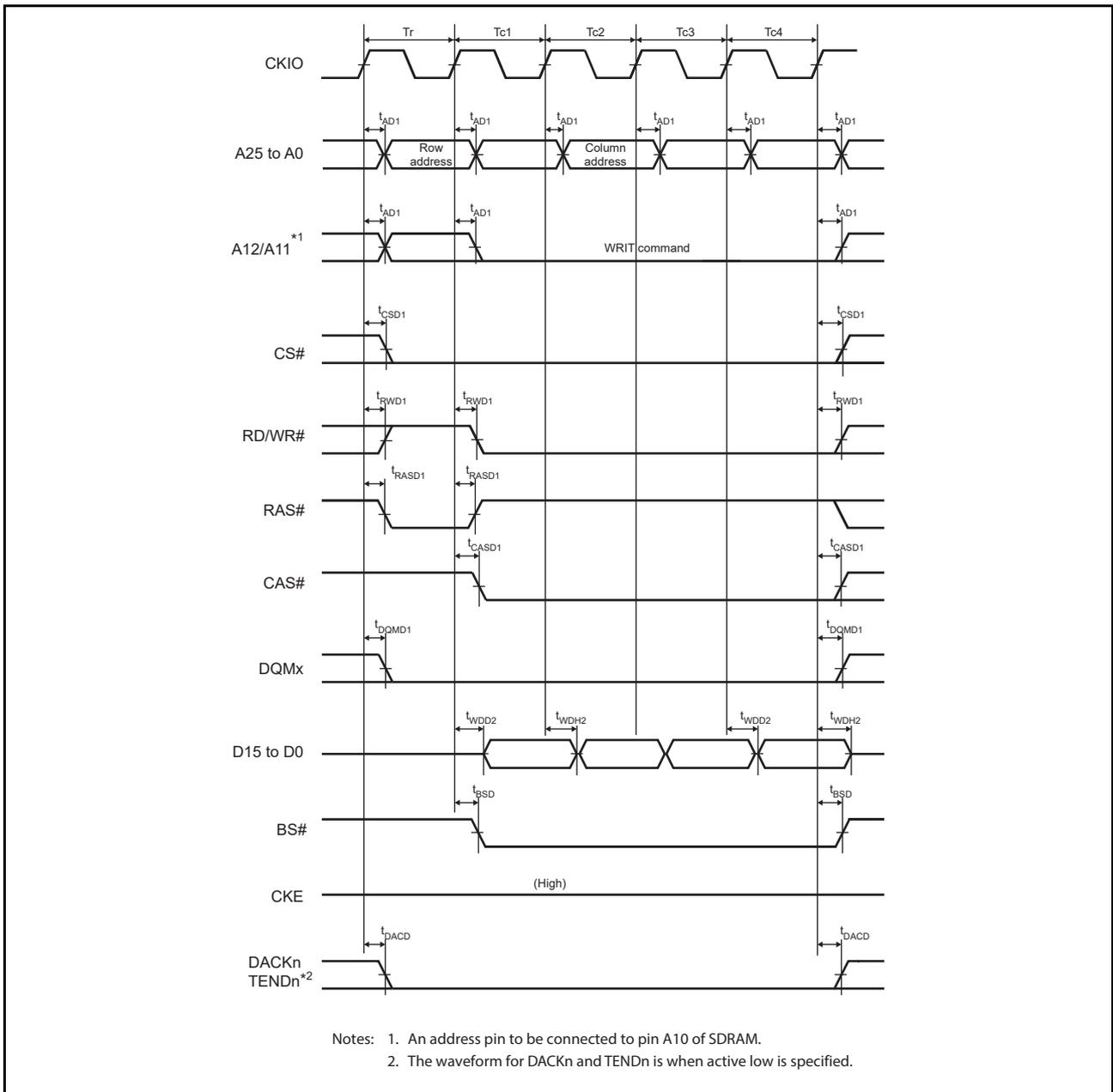
Figure 3.32    Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: ACT + WRITE
               Commands, WTRCD = 0 Cycle, TRWL = 0 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.
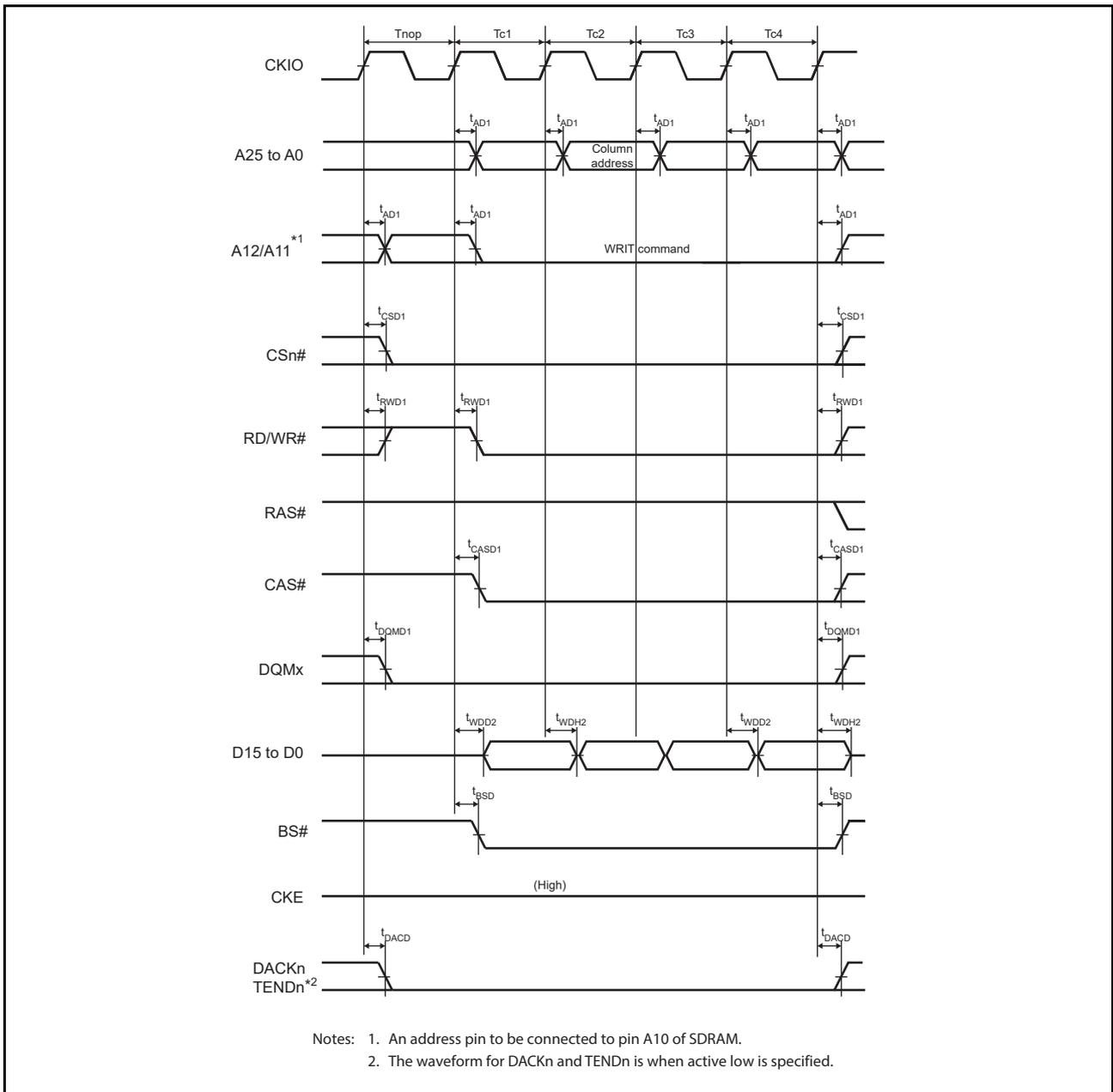
Figure 3.33    Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: WRITE Command, Same Row Address, WTRCD = 0 Cycle, TRWL = 0 Cycle)
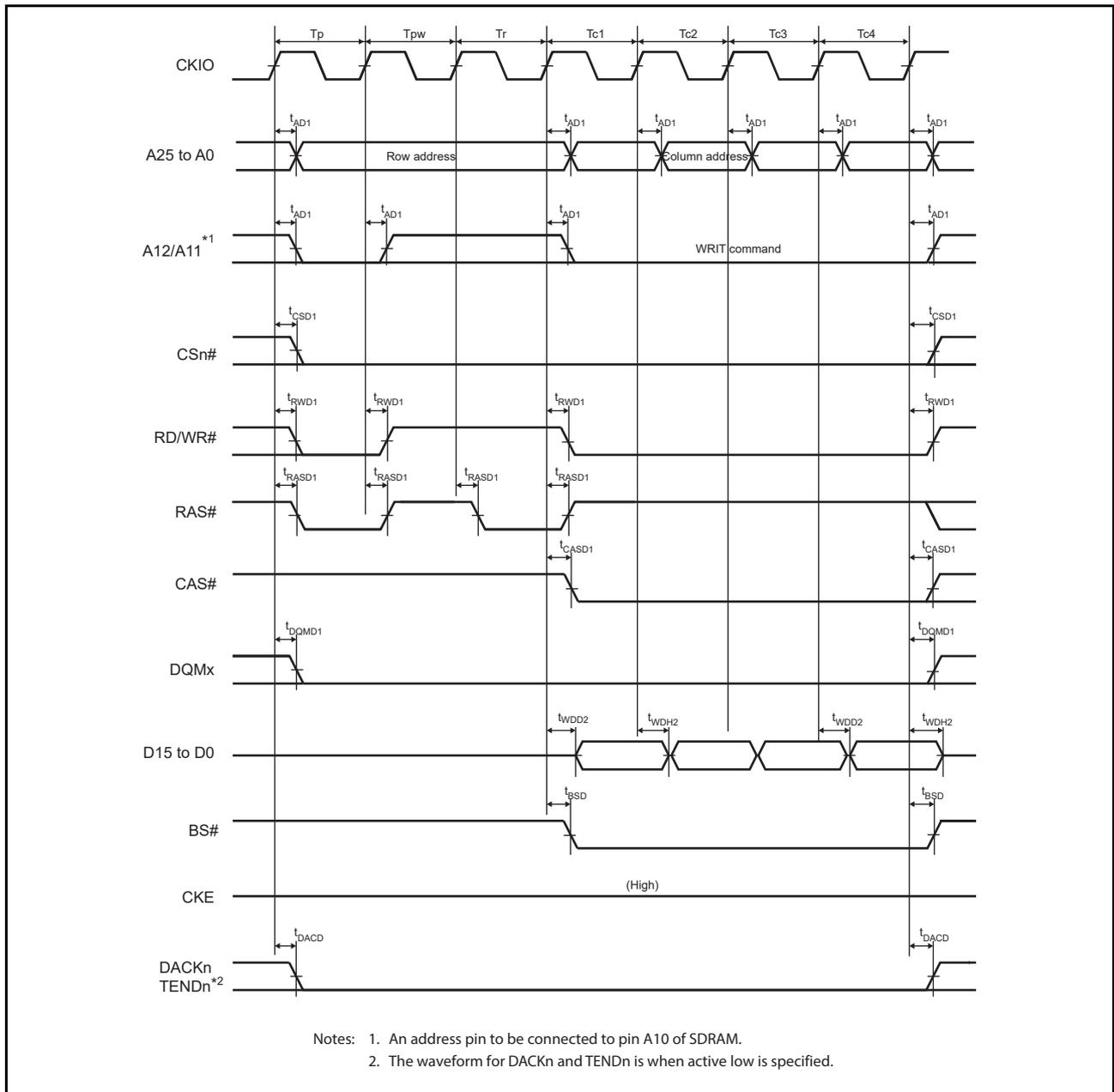
Figure 3.34	Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: PRE + ACT + WRITE Commands, Different Row Addresses, WTRCD = 0 Cycle, TRWL = 0 Cycle)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
       2. The waveform for DACKn and TENDn is when active low is specified.
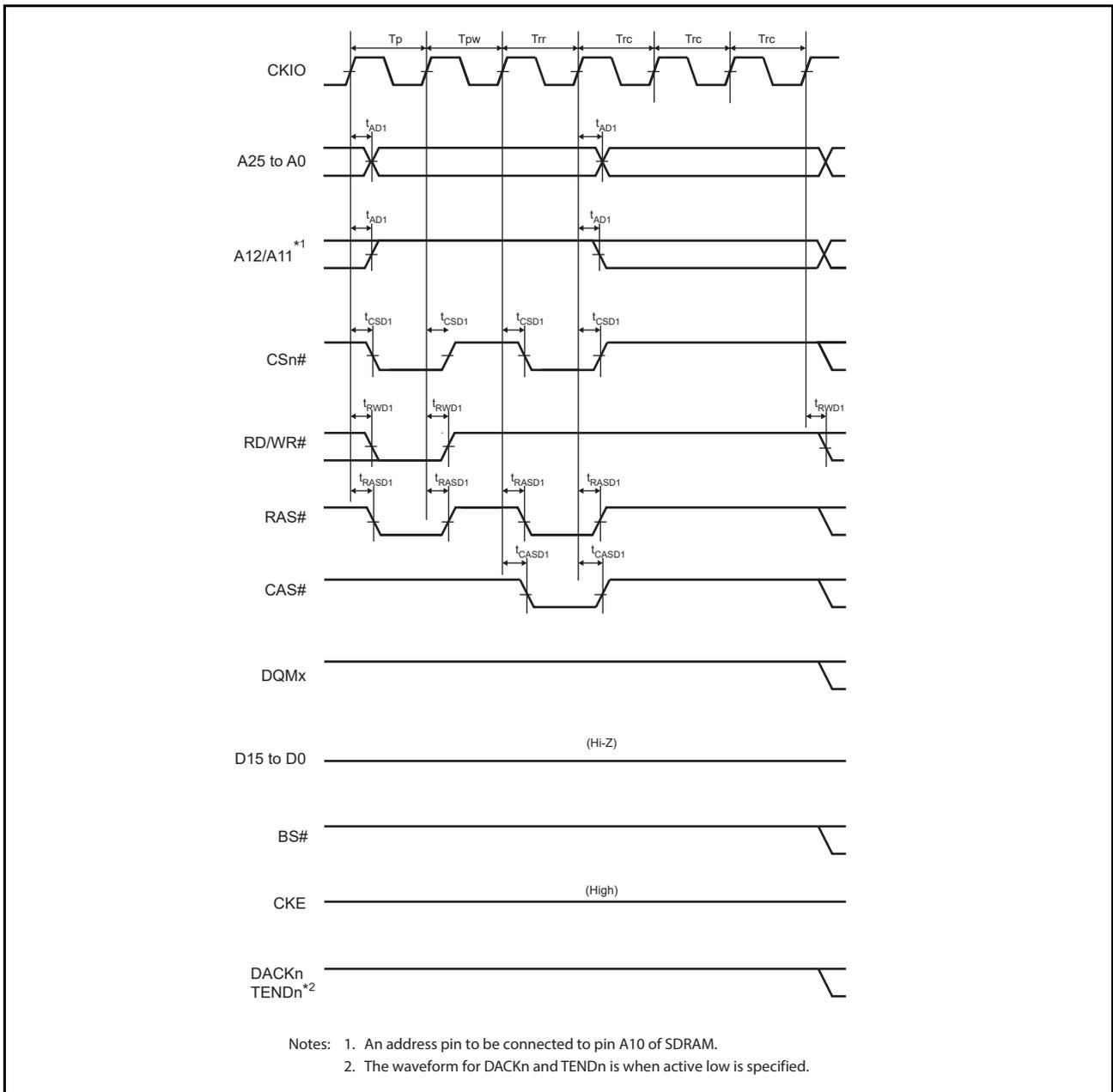
Figure 3.35    Synchronous DRAM Auto-Refreshing Timing (WTRP = 1 Cycle, WTRC = 3 Cycles)

Notes: 1. An address pin to be connected to pin A10 of SDRAM.
           2. The waveform for DACKn and TENDn is when active low is specified.
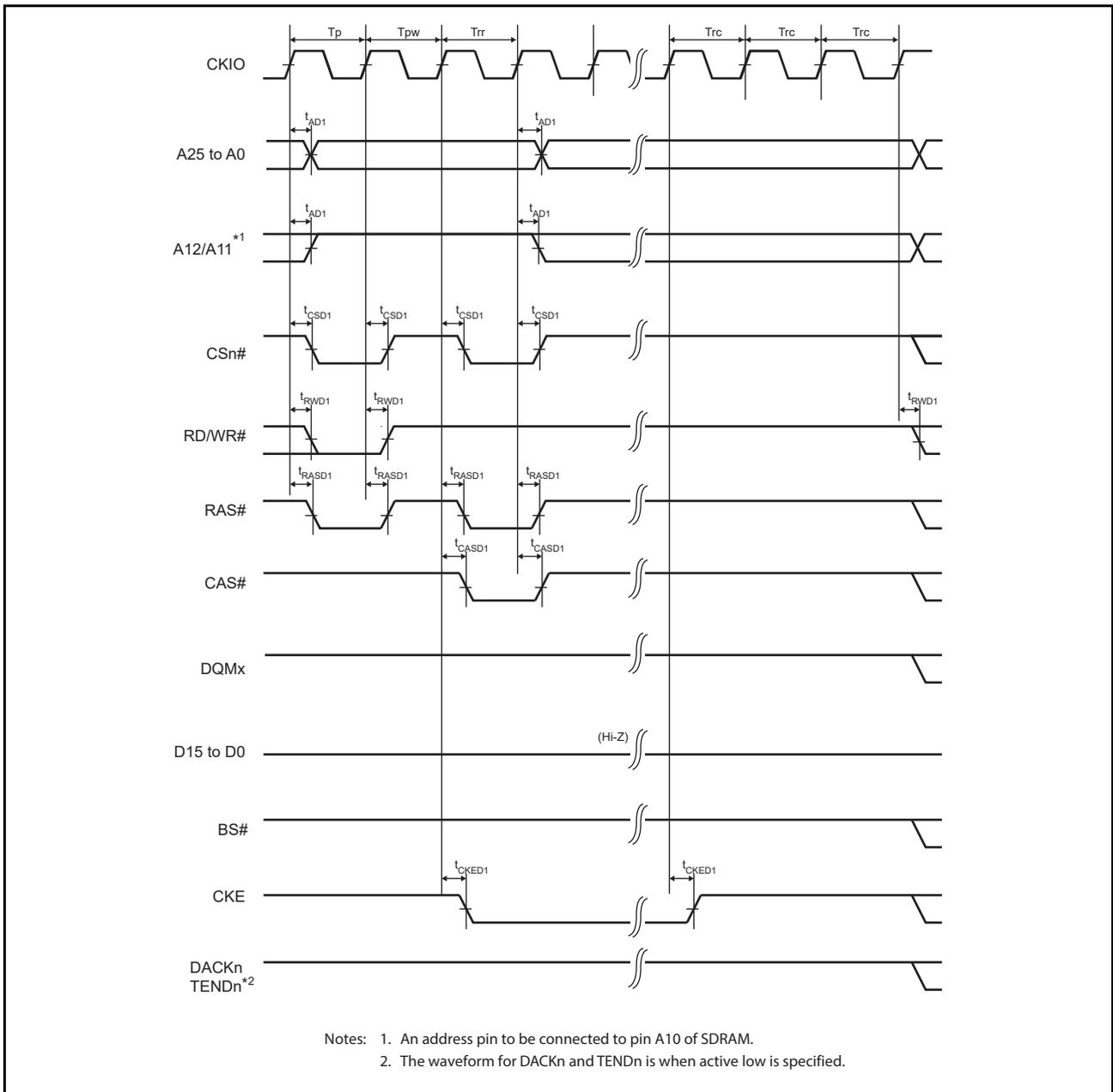
Figure 3.36      Synchronous DRAM Self-Refreshing Timing (WTRP = 1 Cycle)

Notes:  1.  An address pin to be connected to pin A10 of SDRAM.
        2.  The waveform for DACKn and TENDn is when active low is specified.
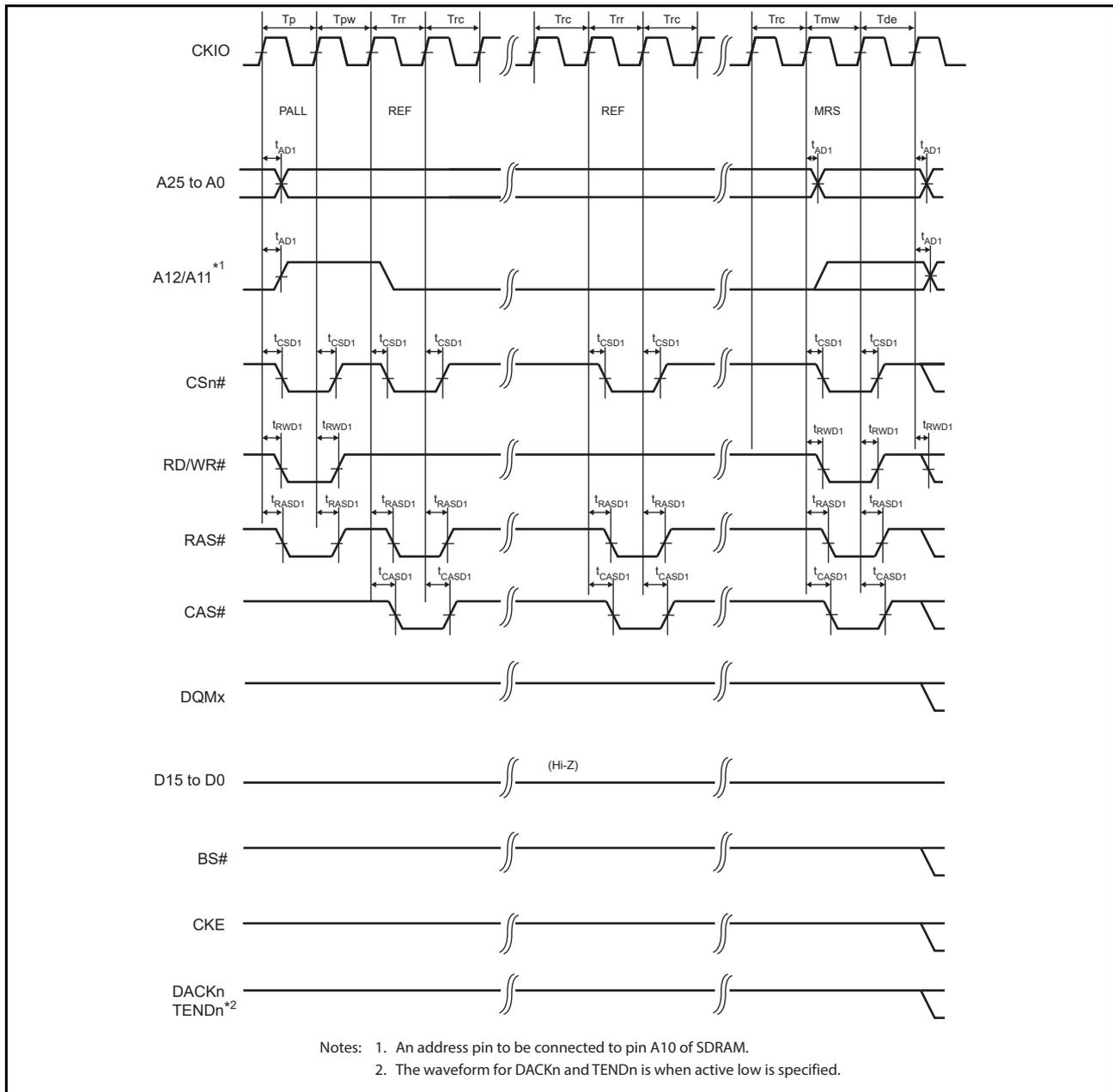
Figure 3.37     Synchronous DRAM Mode Register Write Timing (WTRP = 1 Cycle)

## 3.4.5        Direct Memory Access Controller Timing

Table 3.9        Direct Memory Access Controller Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|------|--------|------|------|------|--------|
| DREQ setup time | $t_{DRQS}$ | 4.0 | — | ns | Figure 3.38 |
| DREQ hold time | $t_{DRQH}$ | 0.5 | — | | |
| DACK, TEND delay time | $t_{DACD}$ | 0 | 12 | | Figure 3.39 |
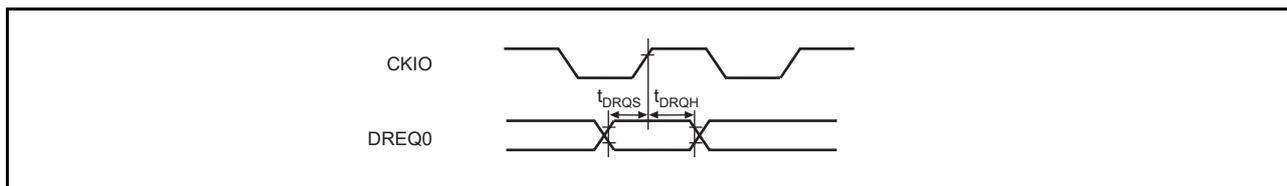


Figure 3.38        DREQ Input Timing
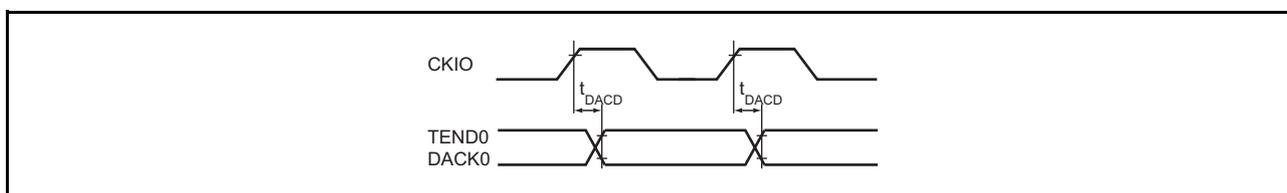


Figure 3.39        DACK, TEND Output Timing

### 3.4.6 Multi-Function Timer Pulse Unit 3 (MTU3a) Timing

Table 3.10 MTU3a Timing

| Item | | | Symbol | Min. | Max. | Unit[*1] | Test Conditions |
|---|---|---|---|---|---|---|---|
| MTU3a | Input capture input pulse width | Single-edge setting | $t_{MTICW}$ | 1.5 | — | $t_{p1cyc}$ | Figure 3.40 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{MTCKWH}$, $t_{MTCKWL}$ | 1.5 | — | $t_{p1cyc}$ | Figure 3.41 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{p1cyc}$ indicates peripheral clock 1C (P1φ) cycle.
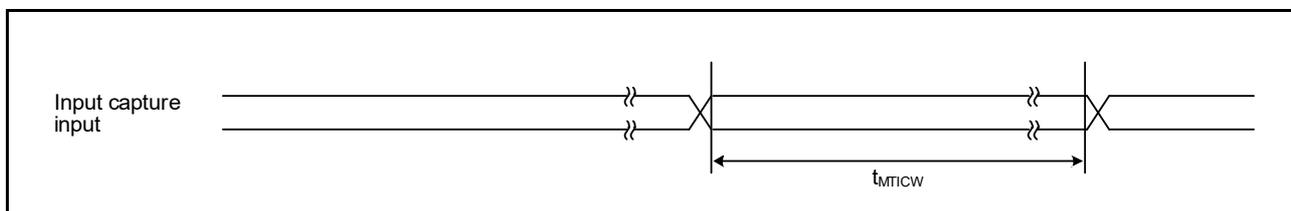


Figure 3.40 MTU3a Input Capture Input Timing
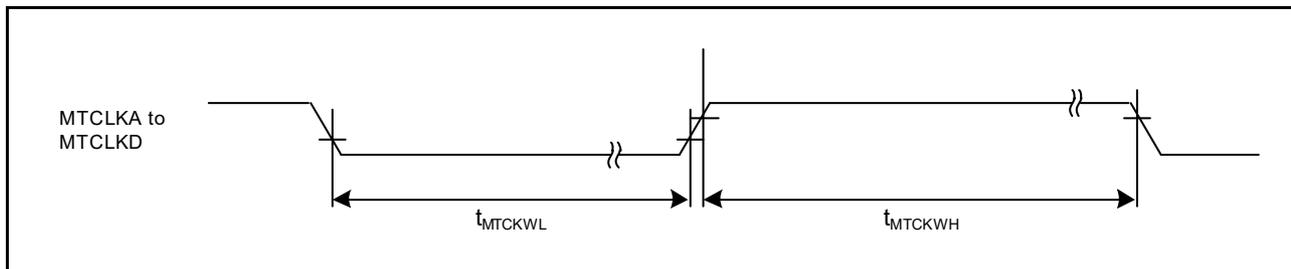


Figure 3.41 MTU3a Clock Input Timing

## 3.4.7　Port Output Enable 3 (POE3) Timing

Table 3.11　POE3 Timing

| Item | | Symbol | Min. | Max. | Unit[*1] | Test Conditions |
|------|---|--------|------|------|---------|-----------------|
| POE3 | POEn# input pulse width | $t_{POE3W}$ | 1.5 | — | $t_{p1cyc}$ | Figure 3.42 |

Note 1.　$t_{p1cyc}$ indicates peripheral clock 1C (P1φ) cycle.
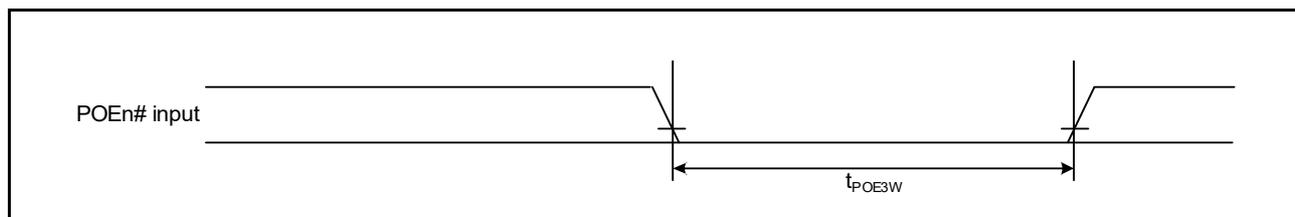


Figure 3.42　POEn# input pulse Timing

## 3.4.8    General PWM Timer (GPT) Timing

Table 3.12    GPT Timing

| Item | | | Symbol | Min. | Max. | Unit[*1] | Test Conditions |
|---|---|---|---|---|---|---|---|
| GPT | Input capture input pulse width | Single-edge setting | $t_{GTICW}$ | 1.5 | — | $t_{p1cyc}$ | Figure 3.43 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1.  $t_{p1cyc}$ indicates peripheral clock 1C (P1φ) cycle.
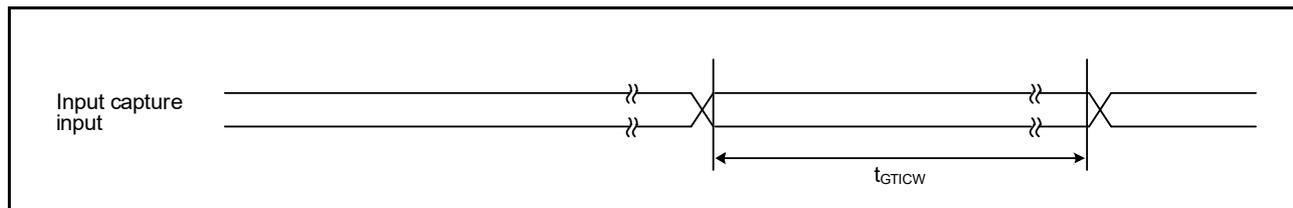


Figure 3.43    GPT Input Capture Input Timing

## 3.4.9　　　Port Output Enable for GPT (POEG) Timing

Table 3.13　　　POEG Timing

| Item | | Symbol | Min. | Max. | Unit[*1] | Test Conditions |
|---|---|---|---|---|---|---|
| POEG | POEG input trigger pulse width | $t_{POEGW}$ | 3 | — | $t_{p1cyc}$ | Figure 3.44 |

Note 1.　$t_{p1cyc}$ indicates peripheral clock 1C (P1φ) cycle.
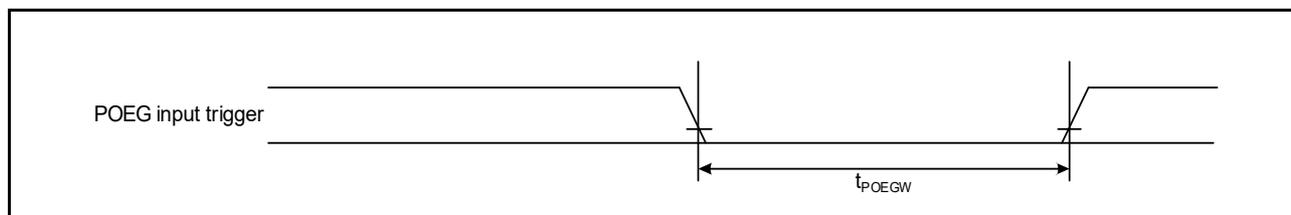


Figure 3.44　　　POEG Input Trigger Timing

## 3.4.10    Watchdog Timer Timing

Table 3.14      Watchdog Timer Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|------|--------|------|------|------|--------|
| WDTOVF# delay time | $t_{WOVD}$ | — | 100 | ns | Figure 3.45 |
| PERROUT# delay time | $t_{PEOD}$ | — | 100 | ns | |
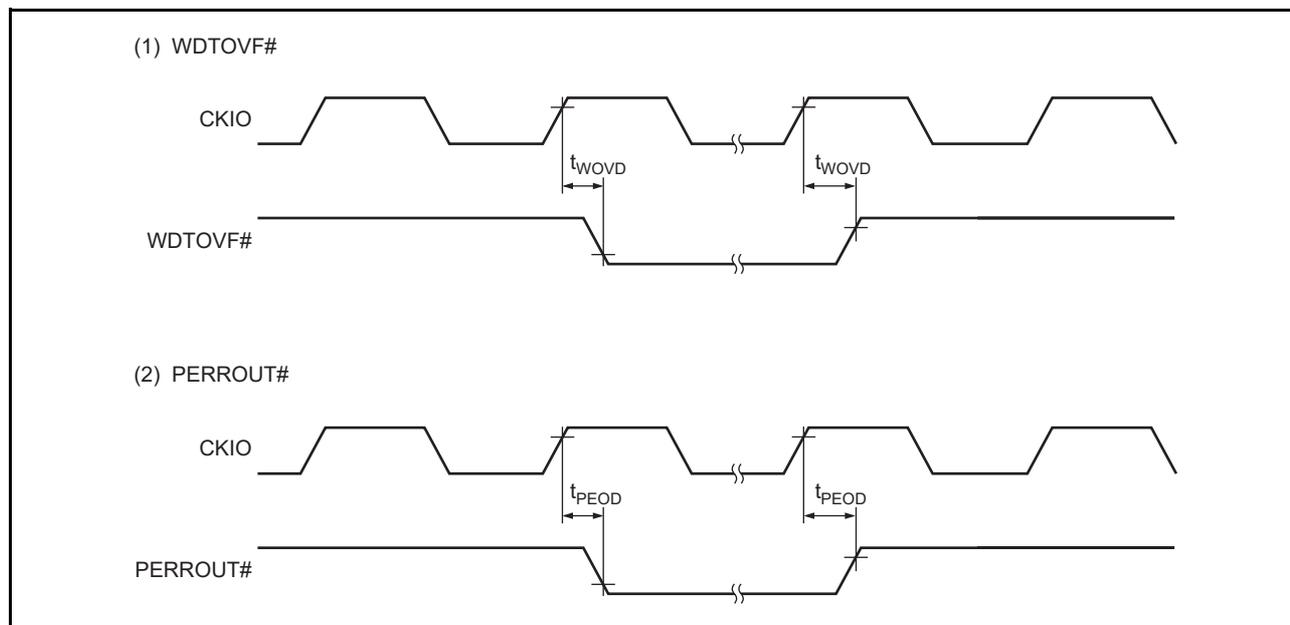


Figure 3.45      Watchdog Timer Output Timing

## 3.4.11     Serial Communications Interface with FIFO (SCIFA) Timing

Table 3.15     SCIFA Timing

| Item | | | Symbol | Min.[*1] | Max.[*1] | Unit[*1] | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCIFA | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{p1cyc}$ | Figure 3.46 |
| | | Clocked synchronous | | 12 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous[*2] | $t_{Scyc}$ | 8 | — | $t_{p1cyc}$ | |
| | | Clocked synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 9 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 9 | ns | |
| | Transmit data delay time | Internal clock | $t_{TXD}$ | −10 | 10 | ns | Figure 3.47 |
| | | External clock | | $3 \times t_{p1cyc}$ | $4 \times t_{p1cyc} + 20$ | | |
| | Receive data setup time | Internal clock | $t_{RXS}$ | $3 \times t_{p1cyc} + 20$ | — | ns | |
| | | External clock | | $t_{p1cyc} + 10$ | — | | |
| | Receive data hold time | Internal clock | $t_{RXH}$ | $- 3 \times t_{p1cyc}$ | — | ns | |
| | | External clock | | $2 \times t_{p1cyc} + 10$ | — | | |

Note 1.  $t_{p1cyc}$ indicates peripheral clock 1C (P1φ) cycle.
Note 2.  When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1
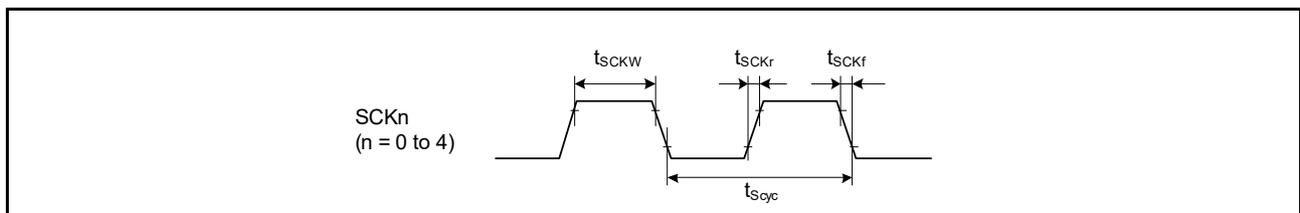


Figure 3.46     SCK Input Clock Timing
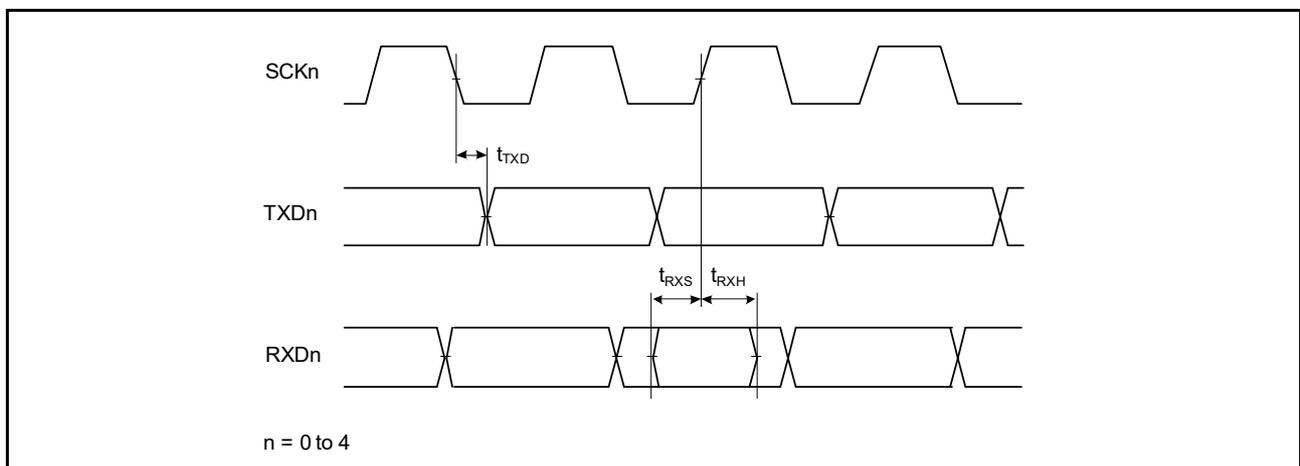


Figure 3.47     SCIFA Input/Output Timing in Clocked Synchronous Mode

## 3.4.12    Serial Communications Interface (SCI) Timing

Table 3.16    SCI Timing

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$[*1] | Figure 3.48 |
| | | clocked synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | asynchronous[*2] | $t_{Scyc}$ | 8 | — | $t_{Pcyc}$[*1] | |
| | | clocked synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | clocked synchronous | $t_{TXD}$ | — | 28 | ns | Figure 3.49 |
| | Receive data setup time | clocked synchronous | $t_{RXS}$ | 15 | — | ns | |
| | Receive data hold time | clocked synchronous | $t_{RXH}$ | 5 | — | ns | |

Note 1.  $t_{Pcyc}$ indicates the peripheral clock 1 (P1φ) cycle.
Note 2.  When the SEMR.ABCS and SEMR.BGDM bits are set to 1
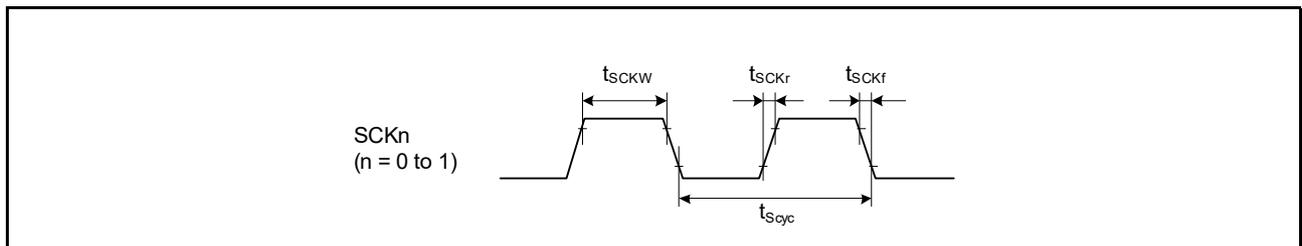


Figure 3.48    SCK Input Clock Timing
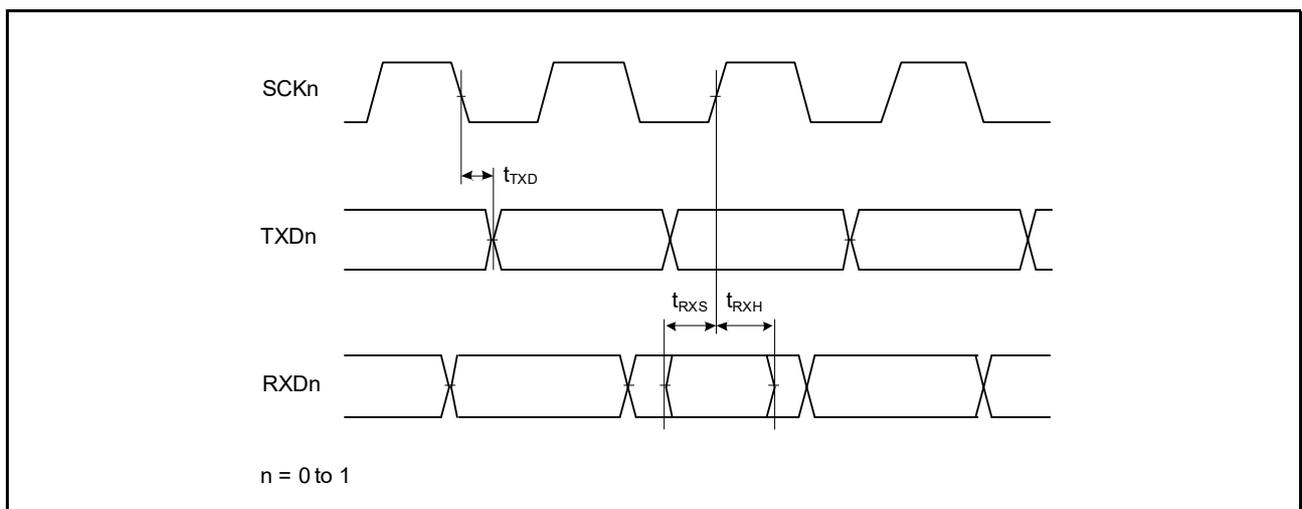


Figure 3.49    SCI Input/Output Timing in Clocked Synchronous Mode

### 3.4.13 Renesas Serial Peripheral Interface Timing

Table 3.17 Renesas Serial Peripheral Interface Timing

| Item | | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|---|
| RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 | 4096 | $t_{p1cyc}$ | Figure 3.50 |
| | Slave | | 8 | 4096 | | |
| RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | 0.4 | — | $t_{SPcyc}$ | |
| | Slave | | 0.4 | — | | |
| RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | 0.4 | — | $t_{SPcyc}$ | |
| | Slave | | 0.4 | — | | |
| Data input setup time | Master | $t_{SU}$ | 15 | — | ns | Figure 3.51 to Figure 3.54 |
| | Slave | | 0 | — | $t_{p1cyc}$ | |
| Data input hold time | Master | $t_H$ | 0 | — | ns | |
| | Slave | | 4 | — | $t_{p1cyc}$ | |
| SSL setup time | Master | $t_{LEAD}$ | $1 \times t_{SPcyc} - 20$ | $8 \times t_{SPcyc}$ | ns | |
| | Slave | | 4 | — | $t_{p1cyc}$ | |
| SSL hold time | Master | $t_{LAG}$ | $1 \times t_{SPcyc}$ | $8 \times t_{SPcyc} + 20$ | ns | |
| | Slave | | 4 | — | $t_{p1cyc}$ | |
| Data output delay time | Master | $t_{OD}$ | — | 21 | ns | |
| | Slave | | — | 4 | $t_{p1cyc}$ | |
| Data output hold time | Master | $t_{OH}$ | 5 | — | ns | |
| | Slave | | 3 | — | $t_{p1cyc}$ | |
| Continuous transmission delay time | Master | $t_{TD}$ | $1 \times t_{SPcyc} + 2 \times t_{cyc}$ | $8 \times t_{SPcyc} + 2 \times tcyc$ | ns | |
| | Slave | | $4 \times tcyc$ | — | | |
| Slave access time | | $t_{SA}$ | — | 4 | $t_{p1cyc}$ | Figure 3.53, Figure 3.54 |
| Slave out release time | | $t_{REL}$ | — | 3 | $t_{p1cyc}$ | |

Note: tp1cyc indicates the period of a cycle of the peripheral clock 1 (P1φ).
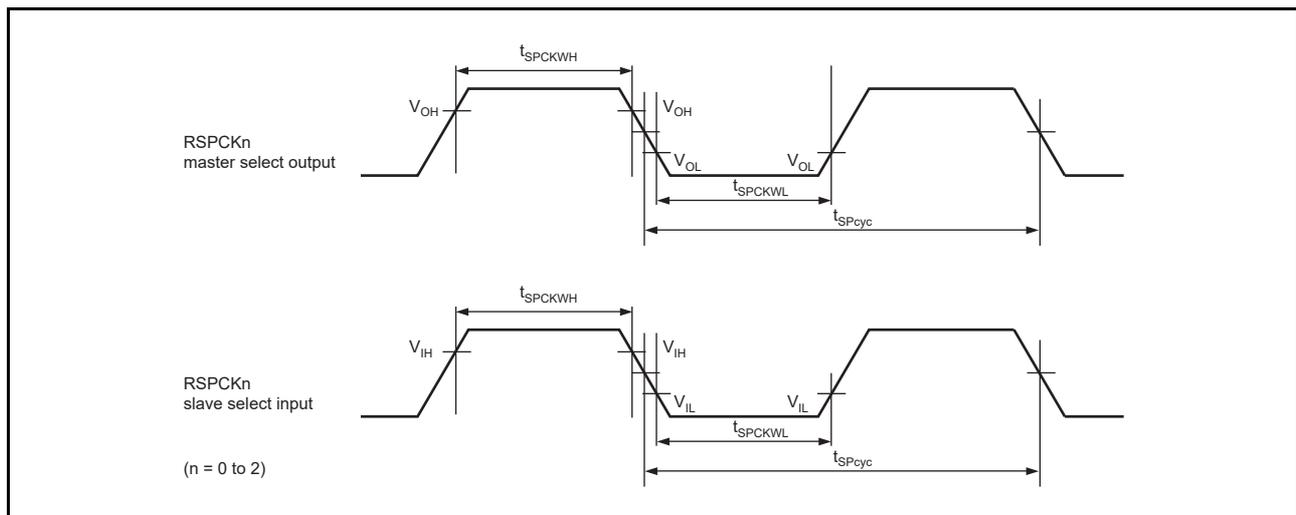


Figure 3.50      Clock Timing
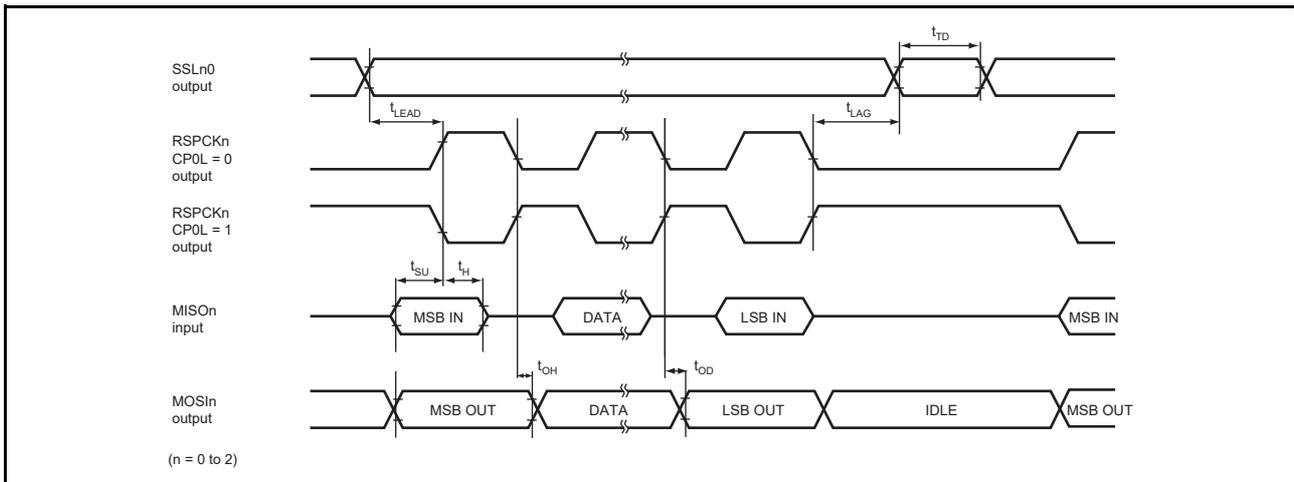
Figure 3.51        Transmission and Reception Timing (Master, CPHA = 0)
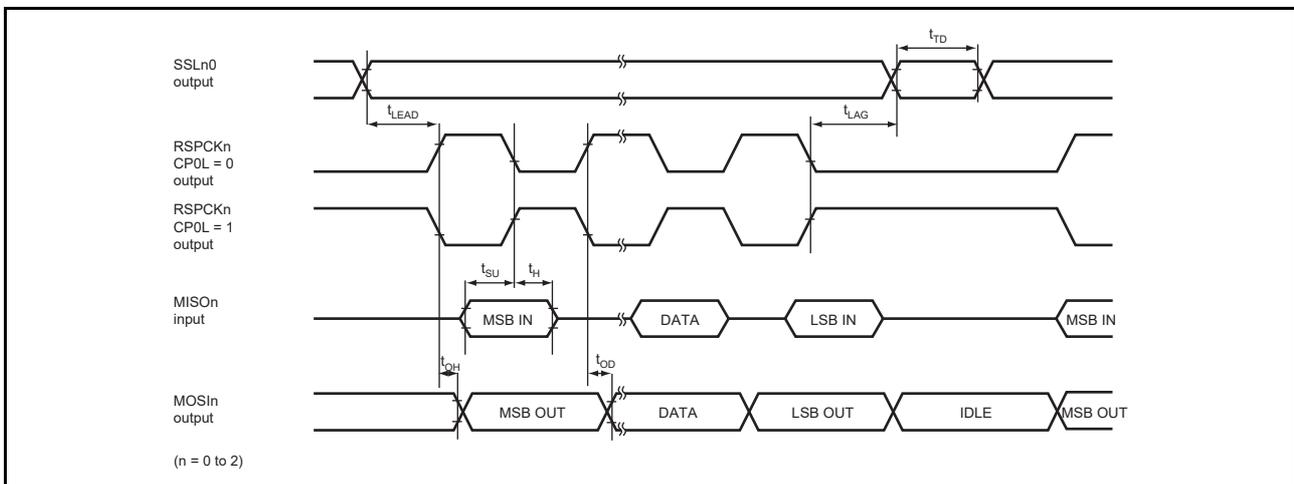


Figure 3.52        Transmission and Reception Timing (Master, CPHA = 1)
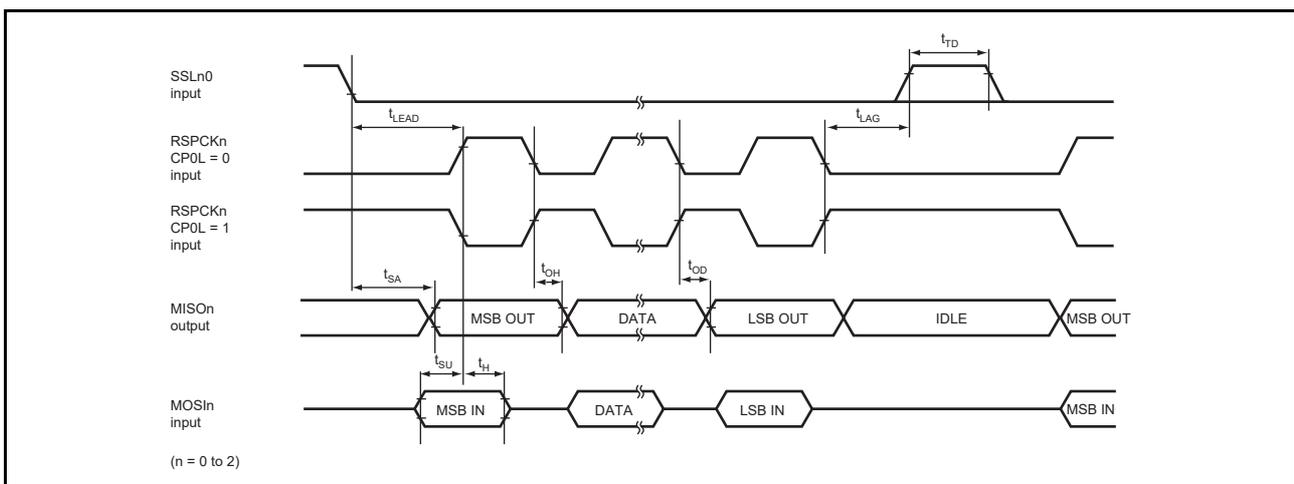


Figure 3.53        Transmission and Reception Timing (Slave, CPHA = 0)
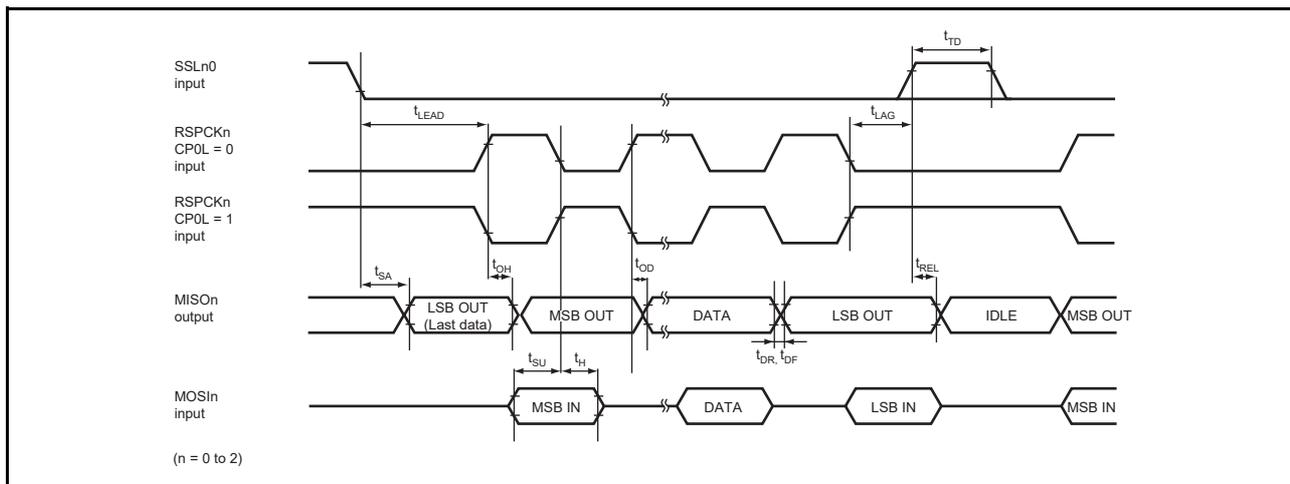
Figure 3.54        Transmission and Reception Timing (Slave, CPHA = 1)

## 3.4.14 SPI Multi I/O Bus Controller Timing

Table 3.18 SPI Multi I/O Bus Controller Timing [1]

| Item | | Symbol | 1.8 V (Octal-SPI flash memory/ HyperFlash connected) | | 3.3 V (Serial flash connected) | | Unit | Figure |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| Clock cycle | | $t_{SPBcyc}$ | 7.58 | — | 15.15 | — | ns | Figure 3.55, Figure 3.59 |
| CLK high pulse width | | $t_{SPBWH}$ | 0.475 | 0.525 | 0.475 | 0.525 | $t_{SPBcyc}$ | Figure 3.55, Figure 3.59 |
| CLK low pulse width | | $t_{SPBWL}$ | 0.475 | 0.525 | 0.475 | 0.525 | $t_{SPBcyc}$ | Figure 3.55, Figure 3.59 |
| CLK rise time | | $t_{SPBR}$ | — | 1.0 | — | 2.0 | ns | Figure 3.55, Figure 3.59 |
| CLK fall time | | $t_{SPBF}$ | — | 1.0 | — | 2.0 | ns | Figure 3.55, Figure 3.59 |
| Data input setup time | QSPI0_SPCLK base point (SDR mode timing adjusted) | $t_{SU}$ | — | — | 5.0 | — | ns | Figure 3.56 |
| | QSPI0_SPCLK base point (DDR mode timing adjusted) | | — | — | 2.0 | — | ns | Figure 3.57 |
| | QSPI1_SSL base point | | − 0.9 [2] | — | — | — | ns | Figure 3.60 |
| Data input hold time | QSPI0_SPCLK base point (SDR mode timing adjusted) | $t_{H}$ | — | — | 0.0 | — | ns | Figure 3.56 |
| | QSPI0_SPCLK base point (DDR mode timing adjusted) | | — | — | 1.0 | — | ns | Figure 3.57 |
| | QSPI1_SSL base point | | 2.69 [2] | — | — | — | ns | Figure 3.60 |
| SSL setup time | | $t_{LEAD}$ | 1.5 × tSPBcyc − 3 | 8.5 × $t_{SPBcyc}$ + 3 | 1.5 × $t_{SPBcyc}$ − 3 | 8.5 × $t_{SPBcyc}$ + 3 | ns | Figure 3.56, Figure 3.57, Figure 3.60 |
| SSL hold time | | $t_{LAG}$ | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | ns | Figure 3.56, Figure 3.57, Figure 3.60 |
| Continuous transfer delay time | | $t_{TD}$ | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | ns | Figure 3.56, Figure 3.57, Figure 3.60 |
| Data output delay time | SDR | $t_{OD}$ | — | 1.4 | — | 5.0 | ns | Figure 3.56 |
| | DDR | | — | 2.69 [2] | — | 5.0 [3] | ns | Figure 3.57, Figure 3.60 |
| Data output hold time | SDR | $t_{OH}$ | − 1.4 | — | − 5.0 | — | ns | Figure 3.56 |
| | DDR | | 0.9 [2] | — | 2.1 [3] | — | ns | Figure 3.57, Figure 3.60 |
| Skew of Clock to Data Strobe | | $t_{CKDS}$ | — | 7 | — | — | ns | Figure 3.60 |
| Data output buffer off time | SDR | $t_{BOFF}$ | − 1.7 | — | − 5.5 | 2 | ns | Figure 3.58 |
| | DDR | | 1 × $t_{SPBcyc}$ − 1.7 | — | 1 × $t_{SPBcyc}$ − 5.5 | — | ns | |

| Item | Symbol | 1.8 V (Octal-SPI flash memory/ HyperFlash connected) | | 3.3 V (Serial flash connected) | | Unit | Figure |
| | | Min. | Max. | Min. | Max. | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| AC differential crossing voltage | $V_{OX}$ | PVcc_SPI × 0.4 | PVcc_SPI × 0.6 | — | — | V | Figure 3.59 |

Note 1. Output load: 15 pF
Note 2. QSPI0_SPCLK frequency: 132 MHz
Note 3. QSPI0_SPCLK frequency: 66 MHz
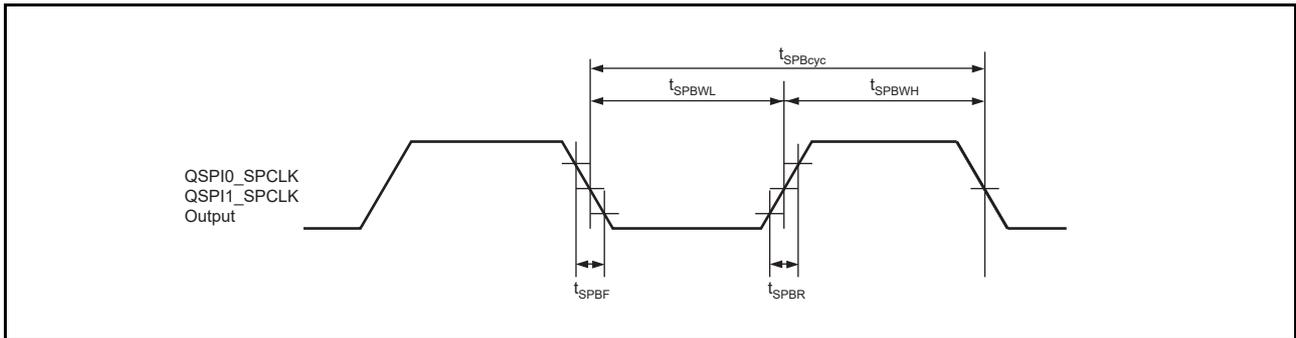


Figure 3.55        Clock Timing
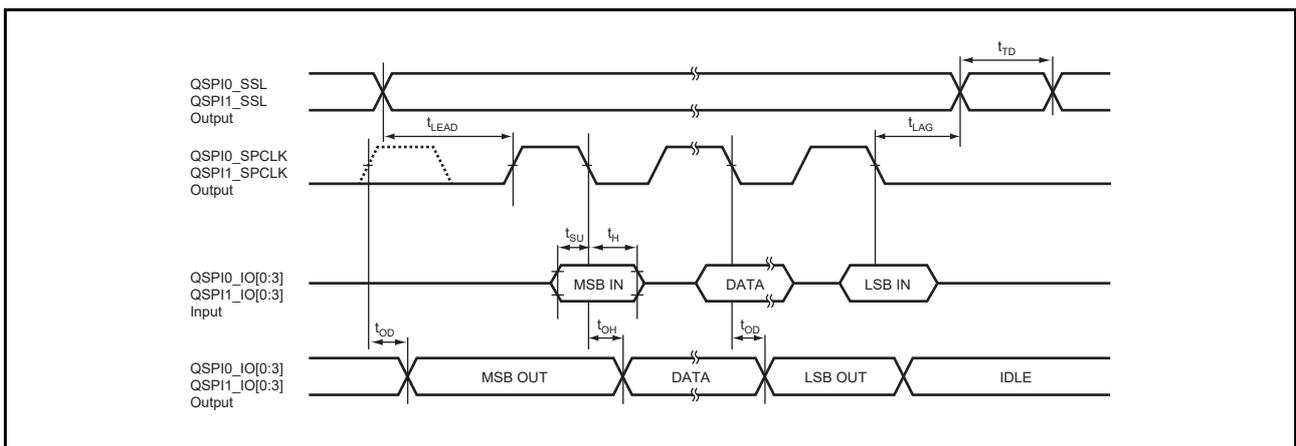


Figure 3.56        SDR Transfer Format Transmission and Reception Timing
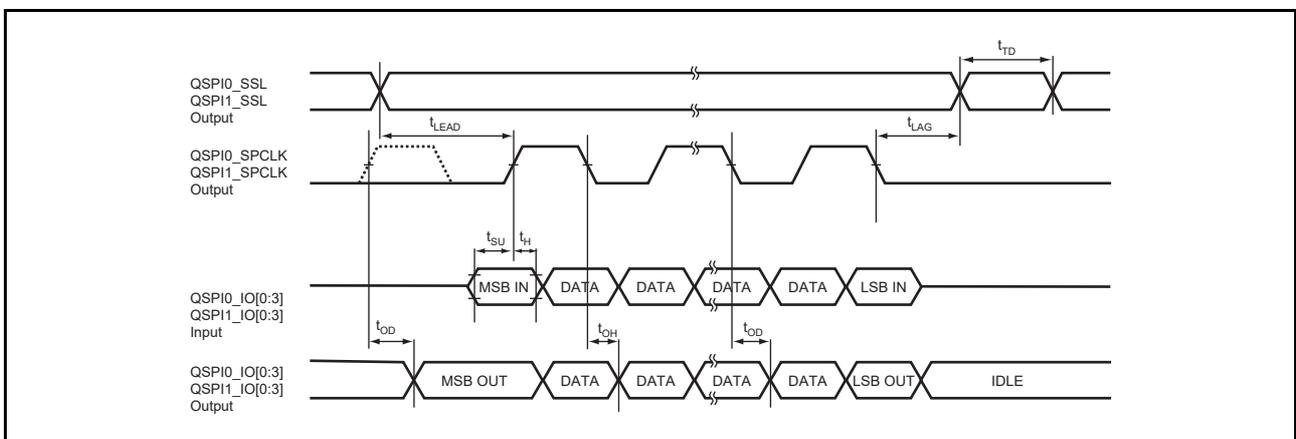


Figure 3.57        DDR Transfer Format Transmission and Reception Timing
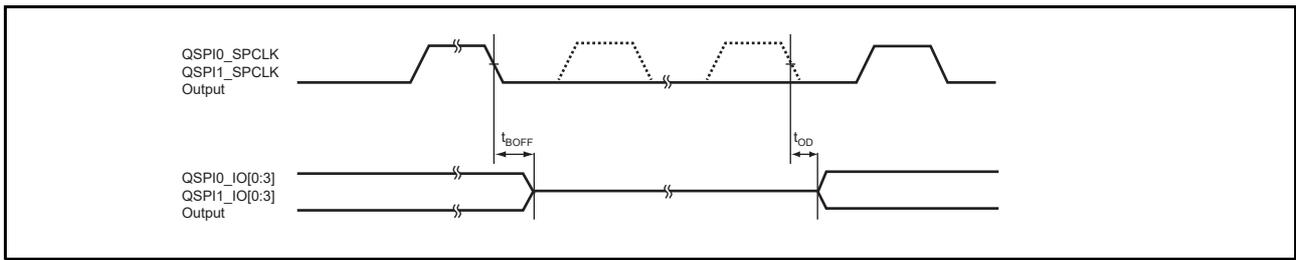
Figure 3.58          Timing for Switching the Buffers on and off
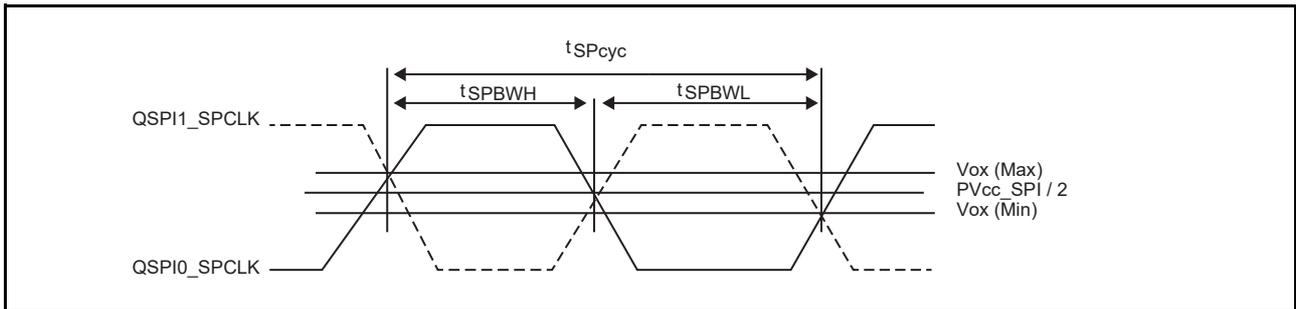


Figure 3.59          AC Differential Crossing Voltage
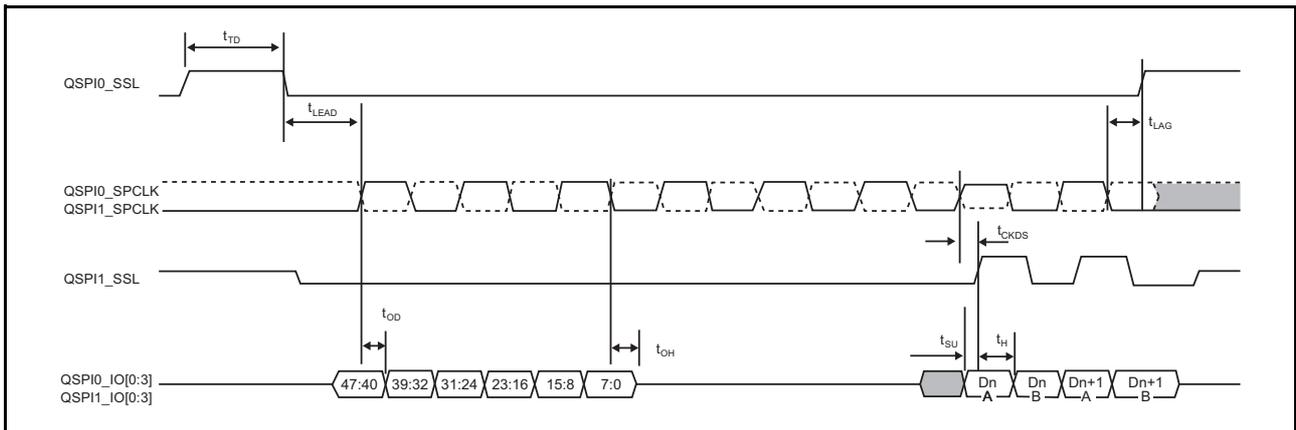


Figure 3.60          Transmit/Receive Timing with Octal-SPI flash memory or HyperFlash™ Connected

## 3.4.15 HyperBus™ Controller Timing

Table 3.19 HyperBus™ Controller Timing [1][2]

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| HM_CK, HM_CK# clock frequency | $f_{HY}$ | 13.75 | 132 | MHz | Figure 3.61, Figure 3.62 |
| HM_CK, HM_CK# clock pulse width | $t_{HYW}$ | 0.475 | 0.525 | $t_{HYcyc}$ | |
| HM_CK, HM_CK# rise time | $t_{HYr}$ | — | 1 | ns | |
| HM_CK, HM_CK# fall time | $t_{HYf}$ | — | 1 | ns | |
| HM_CK, HM_CK# differential cross point voltage | $V_{OX}$ | PVcc_HO × 0.4 | PVcc_HO × 0.6 | V | |
| HM_CS setup time | $t_{CSSHY}$ | $1 \times t_{HYcyc} - 3$ (Minimum register settings[3]) | $16 \times t_{HYcyc} + 3$ (Maximum register settings[3]) | ns | Figure 3.63, Figure 3.64 |
| HM_CS hold time | $t_{CSHHY}$ | $1 \times t_{HYcyc} - 3$ (Minimum register settings[4]) | $16 \times t_{HYcyc} + 3$ (Maximum register settings[4]) | ns | |
| HM_CS High time (Continuous transfer) | $t_{CSHIHY}$ | $1.5 \times t_{HYcyc} - 3$ (Minimum register settings[5]) | $16.5 \times t_{HYcyc} + 3$ (Maximum register settings[5]) | ns | |
| Data input setup time | $t_{SU}$ | − 0.9 [7] | — | ns | |
| Data input hold time | $t_H$ | 2.69 [7] | — | ns | |
| Skew of clock to data strobe | $t_{CKDS}$ | — | $(N + 1) \times t_{HYcyc} - 3$ [6] | ns | |
| Data output delay time | $t_{OD}$ | — | 2.69 [7] | ns | |
| Data output hold time | $t_{OH}$ | 0.9 [7] | — | ns | |
| RWDS refresh input setup time | $t_{RWDSS}$ | 12.5 | — | ns | Figure 3.65 |
| RWDS refresh input hold time | $t_{RWDSH}$ | $0.5 \times t_{HYcyc}$ | — | ns | |

Note 1. $t_{HYcyc}$ indicates the HM_CK (HM_CK#) cycle.
Note 2. Output load: 15 pF
Note 3. The value of HM_CS0# is set by the WCSS bits and RCSS bits of the MTR0 register. The value of HM_CS1# is set by the WCSS bits and RCSS bits of the MTR1 register.
Note 4. The value of HM_CS0# is set by the WCSH bits and RCSH bits of the MTR0 register. The value of HM_CS1# is set by the WCSH bits and RCSH bits of the MTR1 register.
Note 5. The value of HM_CS0# is set by the WCSHI bits and RCSHI bits of the MTR0 register. The value of HM_CS1# is set by the WCSHI bits and RCSHI bits of the MTR1 register.
Note 6. N is RCSH bits value of the MTR0 or MTR1 register (N = 0 to 15).
Note 7. HM_CK frequency: 132 MHz
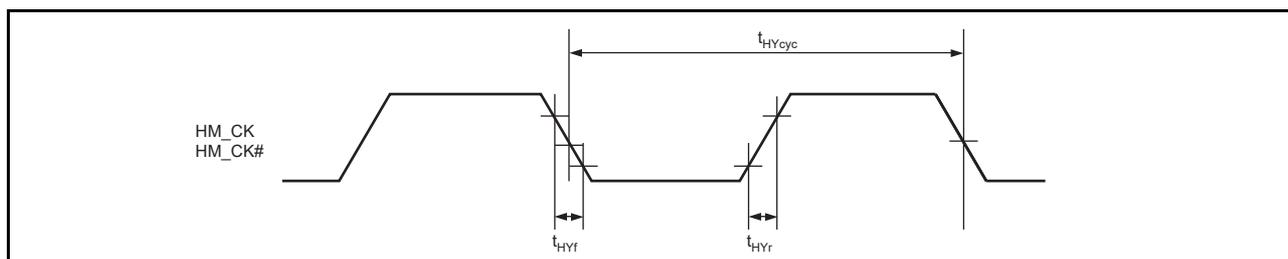


Figure 3.61 Clock Timing
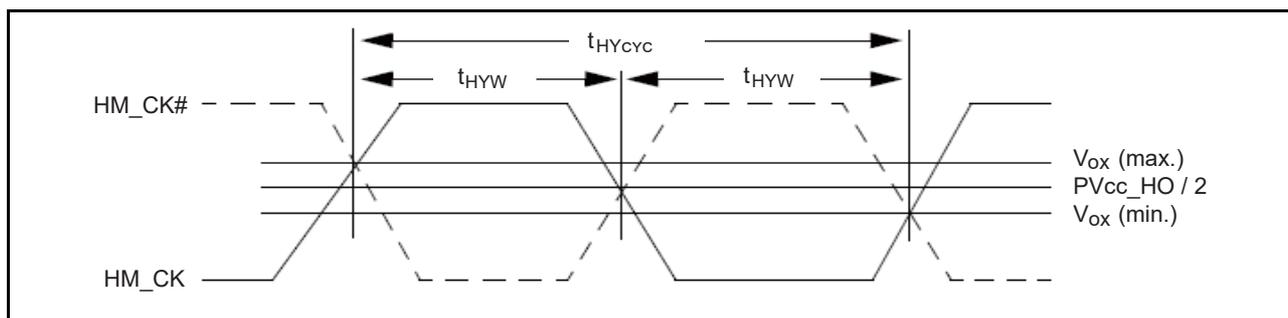


Figure 3.62 AC Differential Crossing Voltage
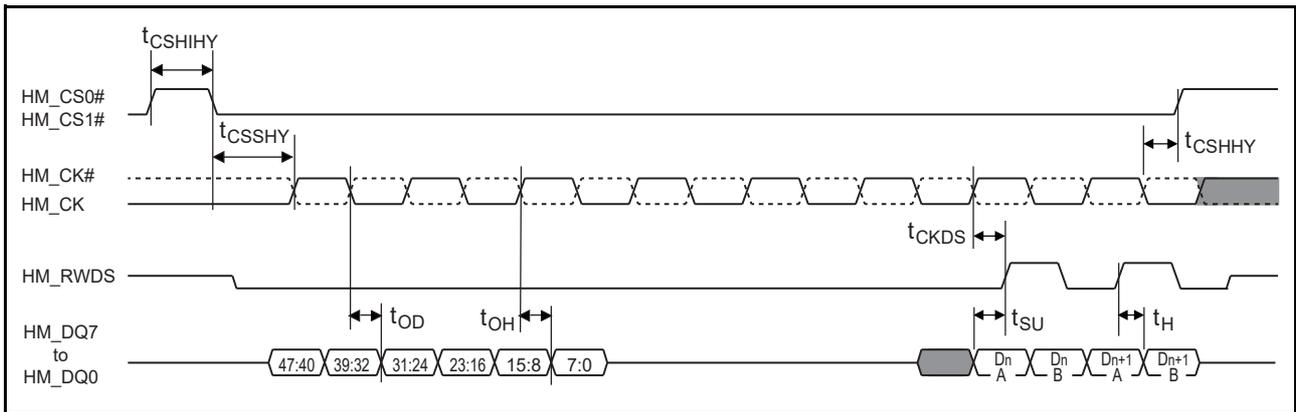
Figure 3.63        HyperBus™ Read Timing
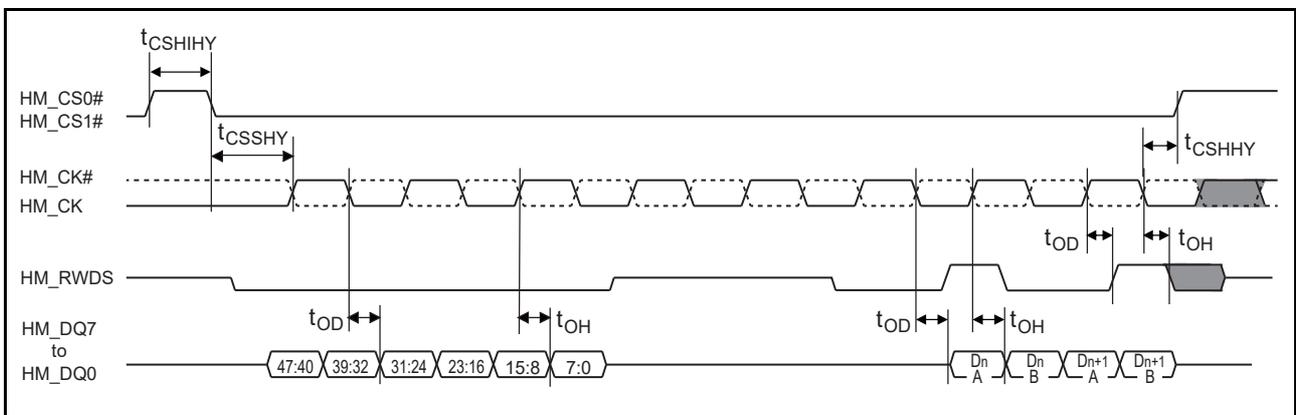


Figure 3.64        HyperBus™ Write Timing
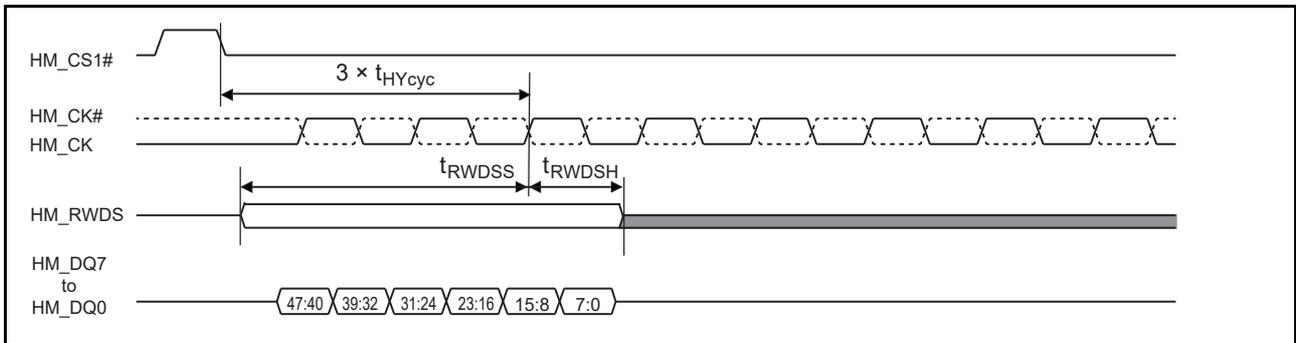


Figure 3.65        RWDS Refresh input Timing (HyperRAM™ Read/Write)

### 3.4.16    Octa Memory Controller Timing

Table 3.20    Octa Memory Controller Timing [*1][*2]

| Item | | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|---|
| OM_SCLK clockfrequency | | $f_{OCcyc}$ | — | 132 | MHz | Figure 3.66 |
| OM_SCLK high pulse width | | $t_{OCwh}$ | 0.475 | 0.525 | $t_{OCcyc}$ | |
| OM_SCLK low pulse width | | $t_{OCwl}$ | 0.475 | 0.525 | $t_{OCcyc}$ | |
| OM_SCLK rise time | | $t_{OCr}$ | — | 1 | ns | |
| OM_SCLK fall time | | $t_{OCf}$ | — | 1 | ns | |
| OM_CS setup time | SPI/SOPI | $t_{OCLEAD}$ | $1 \times t_{OCcyc} - 3$ (Minimum register settings) | $2.5 \times t_{OCcyc} + 3$ (Maximum register settings) | ns | Figure 3.67, Figure 3.68 |
| | DOPI | $t_{OCLEAD}$ | $0.75 \times t_{OCcyc} - 3$ (Minimum register settings) | $2.25 \times t_{OCcyc} + 3$ (Maximum register settings) | ns | Figure 3.69 |
| OM_CS hold time | SPI/SOPI | $t_{OCLAG}$ | $1 \times t_{OCcyc} - 3$ (Minimum register settings) | $4.5 \times t_{OCcyc} + 3$ (Maximum register settings) | ns | Figure 3.67, Figure 3.68 |
| | DOPI read | $t_{OCLAG}$ | $3.25 \times t_{OCcyc} - 3$ (Minimum register settings) | $4.25 \times t_{OCcyc} + 3$ (Maximum register settings) | ns | Figure 3.69 |
| | DOPI write | $t_{OCLAG}$ | $0.75 \times t_{OCcyc} - 3$ (Minimum register settings) | $4.25 \times t_{OCcyc} + 3$ (Maximum register settings) | ns | |
| Continuous transfer delay time | | $t_{OCTD}$ | $1 \times t_{OCcyc} - 3$ (Minimum register settings) | $8.5 \times t_{OCcyc} + 3$ (Maximum register settings) | ns | Figure 3.67, Figure 3.68, Figure 3.69 |
| Data input setup time | SPI SCLK base point | $t_{SU}$ | 9.6 | — | ns | Figure 3.67 |
| Data input hold time | | $t_H$ | 0.5 | — | ns | |
| Data input setup time | SOPI/DOPI DQS base point [*3] | $t_{SU}$ | − 0.7 | — | ns | Figure 3.68, Figure 3.69 |
| Data input hold time | | $t_H$ | 2.69 | — | ns | |
| Skew of Clock to Data Strobe | | $t_{CKDS}$ | — | 20 | ns | |
| Data output delay time | SPI/SOPI | $t_{OD}$ | — | 1.4 | ns | Figure 3.67, Figure 3.68 |
| Data output hold time | | $t_{OH}$ | − 1.4 | — | ns | |
| Data output buffer off time | SOPI | $t_{BOFF}$ | 2 | — | ns | Figure 3.68 |
| Data output delay time | DOPI [*3] | $t_{OD}$ | — | 2.69 | ns | Figure 3.69, Figure 3.70 |
| Data output hold time | | $t_{OH}$ | 0.9 | — | ns | |
| Data output buffer off time | DOPI | $t_{BOFF}$ | 0.9 | — | ns | Figure 3.69 |
| DQS refresh input setup time | | $t_{DQSS}$ | 12 | — | ns | Figure 3.71 |
| DQS refresh input hold time | | $t_{DQSH}$ | $0.5 \times t_{OCcyc}$ | — | ns | |

Note 1.  $t_{OCcyc}$ indicates the OM_SCLK cycle.
Note 2.  Maximum load capacitance: 15 pF
Note 3.  OM_SCLK frequency: 132 MHz
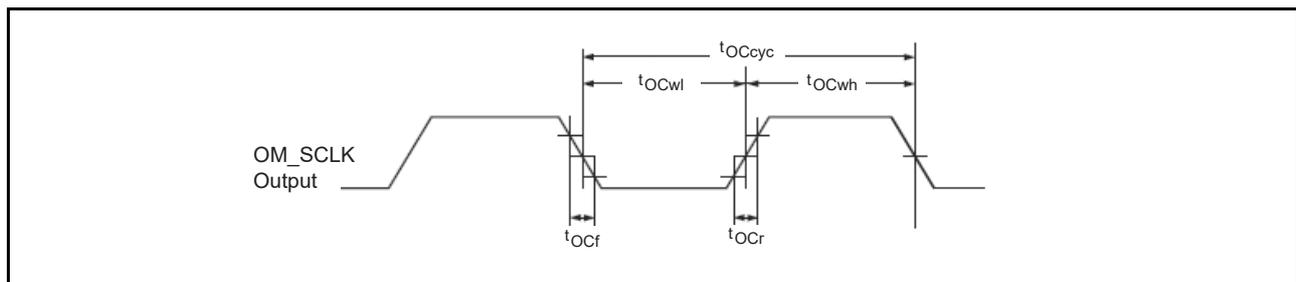


Figure 3.66        Clock Timing
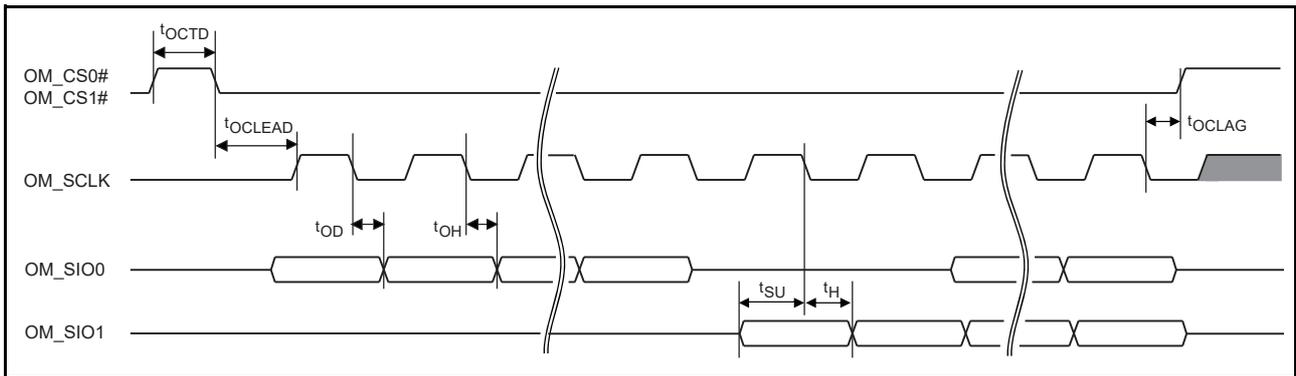
Figure 3.67        SPI Transfer Format Transmission and Reception Timing
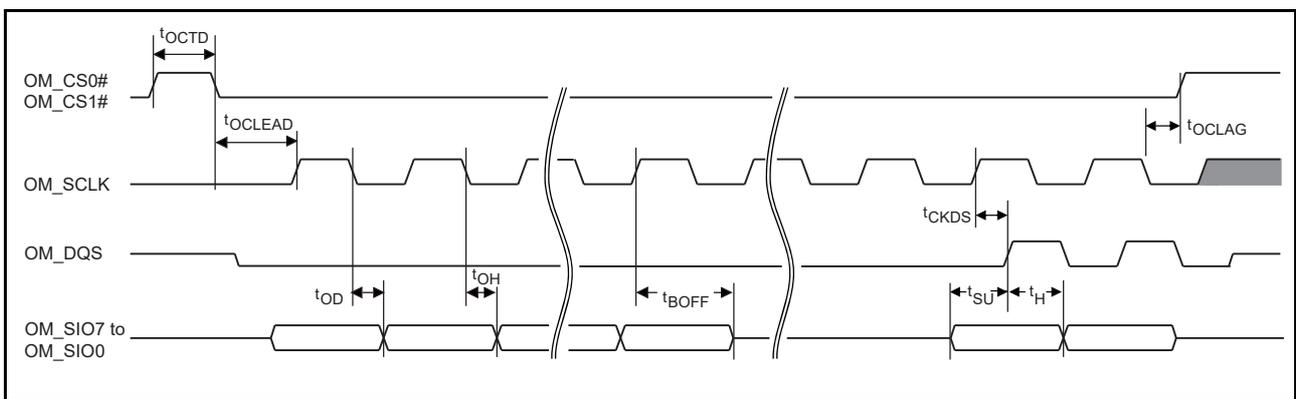


Figure 3.68        SOPI Transfer Format Transmission and Reception Timing
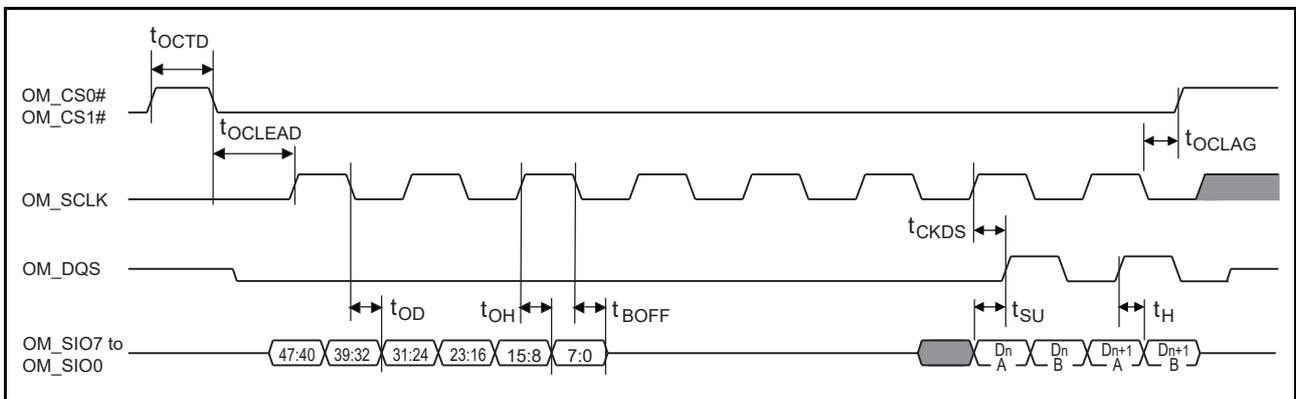


Figure 3.69        DOPI Transfer Format Transmission and Reception Timing
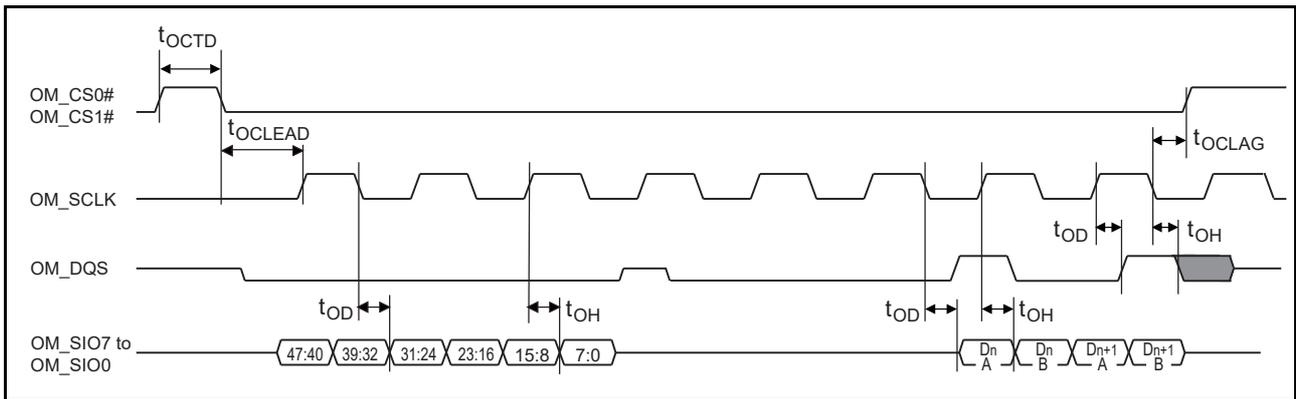
Figure 3.70     DOPI Transfer Format Transmission Timing
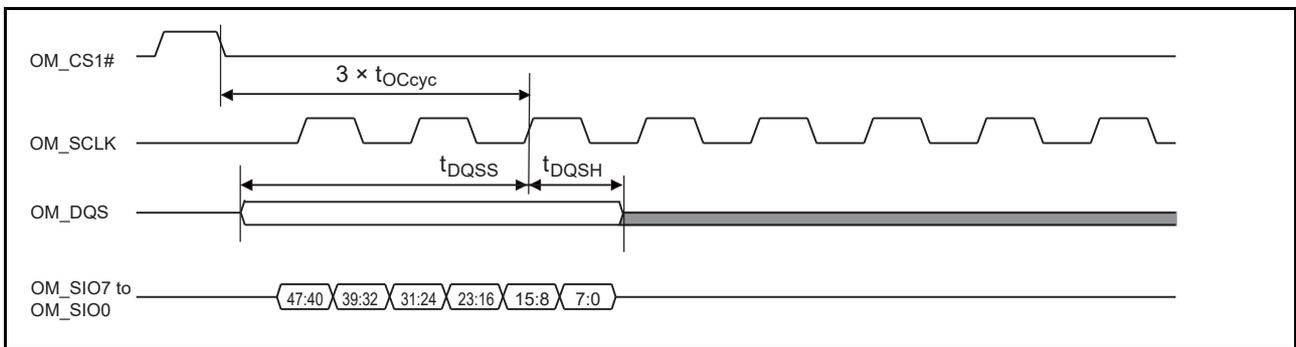


Figure 3.71     DQS Refresh input Timing (OctaRAM™ Read/Write)

## 3.4.17 I²C Bus Interface Timing

Table 3.21 I2C Bus Interface Timing

| Item | Symbol | I/O | Standard mode (Sm) Min. | Max. | Fast mode (Fm) Min. | Max. | Fast mode plus (Fm+) Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| SCL clock frequency | $f_{CLK}$ | I/O | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| Bus free time (between stop and start condition) | $t_{BUF}$ | I/O | 4.7 | — | 1.3 | — | 0.5 | — | µs |
| Hold time[1] | $t_{HD:STA}$ | I/O | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| Low period of SCL clock | $t_{LOW}$ | I/O | 4.7 | — | 1.3 | — | 0.5 | — | µs |
| High period of SCL clock | $t_{HIGH}$ | I/O | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| Setup time for start/restart condition | $t_{SU:STA}$ | I/O | 4.7 | — | 0.6 | — | 0.26 | — | µs |
| Data hold time (I2C bus device) | $t_{HD:DAT}$ | I/O | 0[2] | — | 0[2] | — | 0 | — | µs |
| Data setup time | $t_{SU:DAT}$ | I/O | 250 | — | 100[3] | — | 50 | — | ns |
| SDA and SCL signal rise time | $t_R$ | Input | — | 1000 | 20 | 300 | — | 120 | ns |
| SDA and SCL signal fall time[3] | $t_F$ | Input | — | 300 | 20 × (PVcc / 5.5 V) | 300 | 20 × (PVcc / 5.5 V) | 120 | ns |
| | | Output | — | 250 | 20 × (PVcc / 5.5 V) | 250 | 20 × (PVcc / 5.5 V) | 120 | ns |
| Setup time for STOP condition | $t_{SU:STO}$ | I/O | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| Capacitive load for each bus line | $C_b$ | — | — | — | 400[4] | 400[4] | — | 550[4] | pF |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | Input | — | — | 0 | 50[5] | 0 | 50[5] | ns |

In the above table and subsequently, SCL and SDA refer to the RIICnSCL and RIICnSDA signals, respectively.

Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.

Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the CnSCL signal reaches $V_{IL}$ (max.) from $V_{IH}$ (min.) ).

Note 3. The fast-mode I2C bus device can be used in the standard mode I2C bus system. In this case, the minimum value of the data setup time ($t_{SU:DAT (min.)}$ 250 [ns]) must be satisfied.
If the system does not extend the low period of SCL clock ($t_{LOW}$), this condition is automatically satisfied. If the system extends the low period of SCL clock ($t_{LOW}$), transmit the subsequent data bit to the SDA line before the SCL line is released ($t_{R (max.)}$ + $t_{SU:DAT (min.)}$ = 1000 + 250 = 1250 [ns]: (standard mode I2C bus specification)).

Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I2C bus specification provided by NXP Semiconductors.

Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICφ) and the NF[1:0] bits in RIICnMR3. For details, refer to section 23, I2C Bus Interface, in the RZ/A2M Group User's Manual.
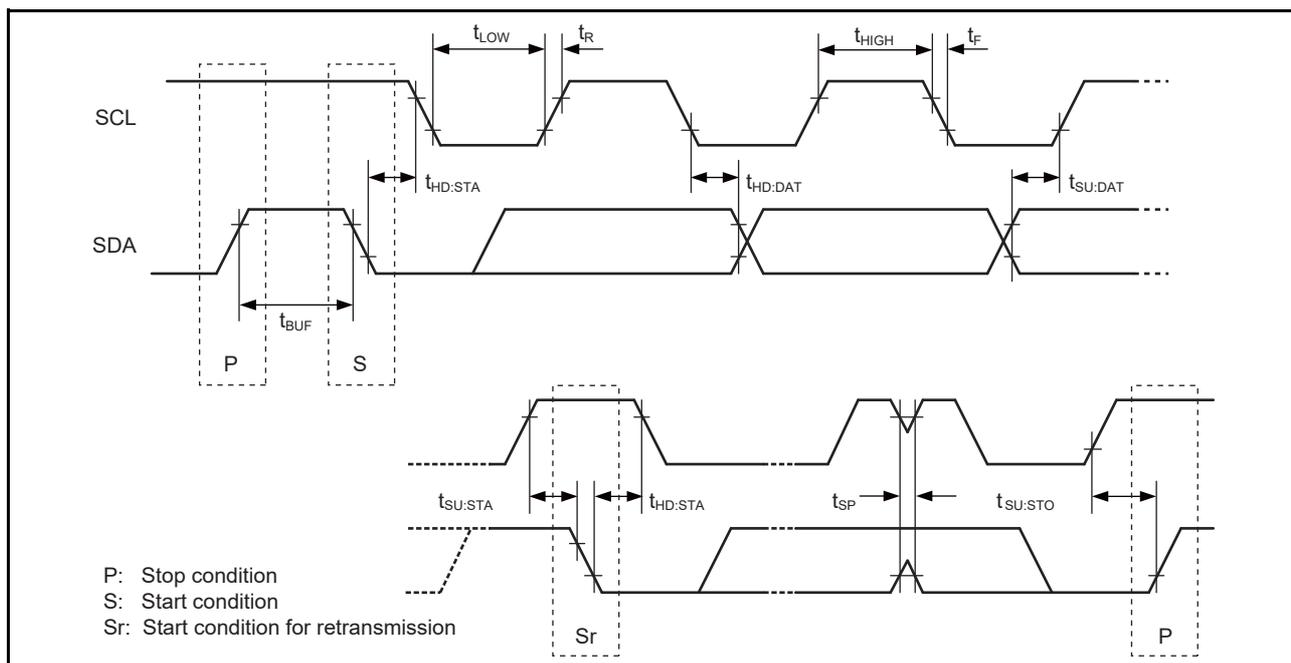
Figure 3.72      Input/Output Timing

## 3.4.18      Serial Sound Interface (SSIF-2) Timing

Table 3.22      SSIF-2 Timing

| Item | Remarks | Symbol | Target Specification Min. | Target Specification Max. | Unit | Figure |
|------|---------|--------|------|------|------|--------|
| Output clock cycle | Output | $t_O$ | 80 | 64000 | ns | Figure 3.73 |
| Input clock cycle | Input | $t_I$ | 80 | 64000 | ns | |
| Clock high | Bidirectional | $t_{HC}$ | 32 | — | ns | |
| Clock low | | $t_{LC}$ | 32 | — | ns | |
| Clock rise time/Clock fall time | Output | $t_{RC}/t_{FC}$ | — | 25 | ns | |
| Setup time | | $t_{SR}$ | 25 | — | ns | Figure 3.74, Figure 3.75, Figure 3.76 |
| Hold time | | $t_{HR}$ | 5 | — | ns | |
| SSILRCK output delay time | | $t_{DTR}$ | −5 | 15 | ns | |
| Data output delay time (Noise canceler not in use) | | $t_{DTR}$ | −5 | 25 | ns | |
| Data output delay time (Noise canceler in use) | | $t_{DTR}$ | 10 | 45 | ns | |
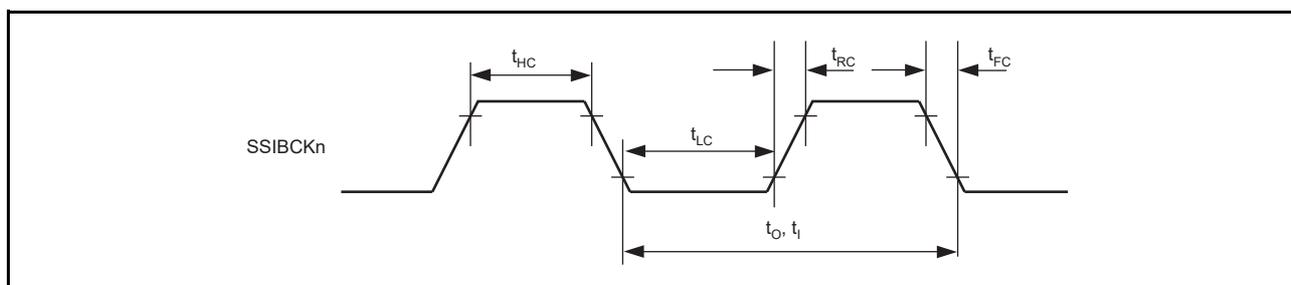


Figure 3.73        Bit Clock Input/Output Timing
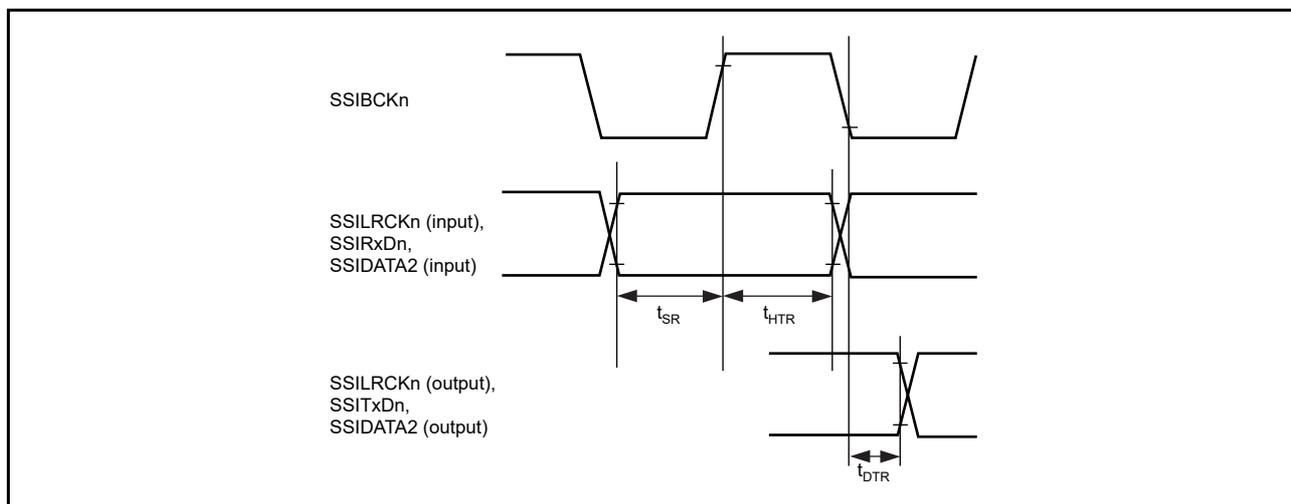


Figure 3.74        Transmission and Reception Timing (SSIBCK Falling Output)
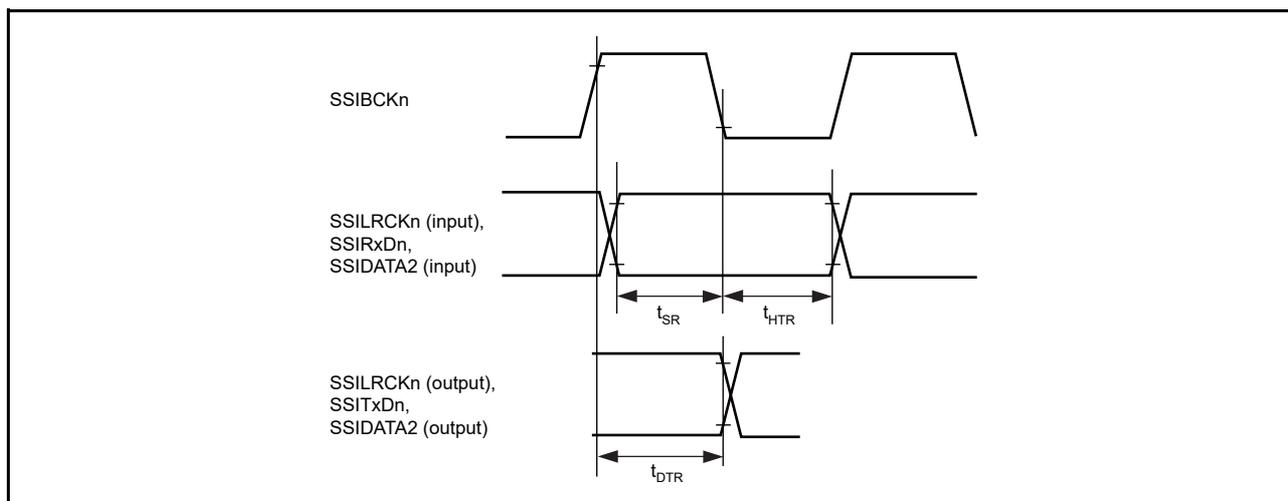
Figure 3.75　　　　Transmission and Reception Timing (SSIBCK Rising Output)



Note.  Output timing of the MSB when slave transmission satisfies the following condition a) or b)
　　　　a) SSICR.DEL=1, SSICR.SDTA=0
　　　　b) SSICR.DEL=1, SSICR.SDTA=1, without Padding
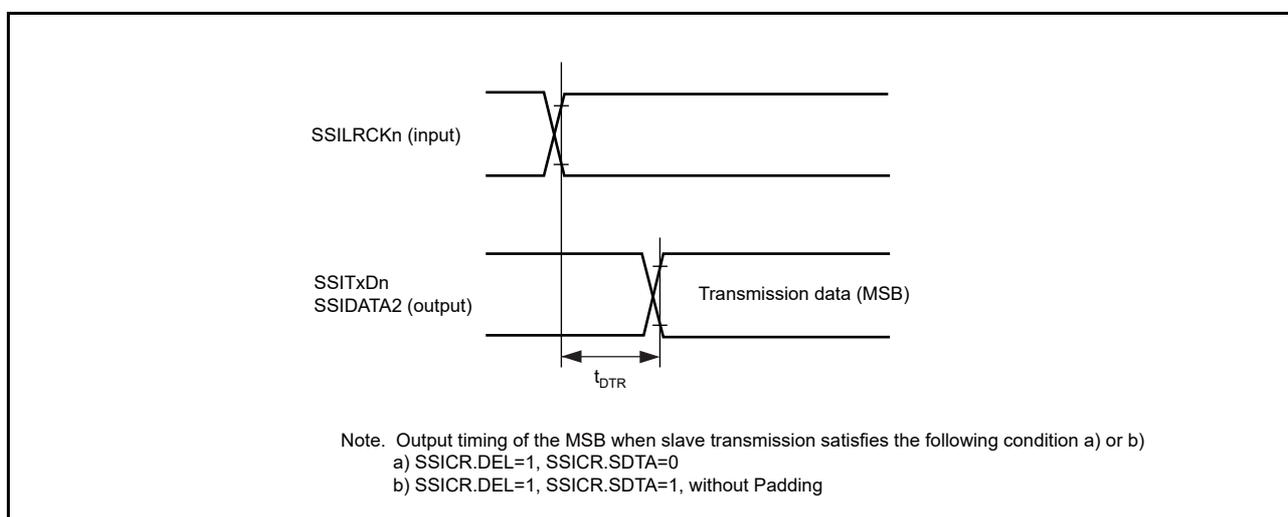
Figure 3.76　　　　Transmission Timing (Slave, in Synchronization with SSILRCK)

### 3.4.19    CANFD Interface Timing

Table 3.23    CANFD Interface Timing

| Item | Symbol | CAN | | CANFD | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Internal delay time | $t_{node}$ | — | 100 | — | 75 | ns | Figure 3.77 |
| Transmission rate | | — | 1 | — | 4.125 | Mbps | |

Internal delay time ($t_{node}$) = Internal transfer delay time ($t_{output}$) + Internal receive delay time ($t_{input}$)
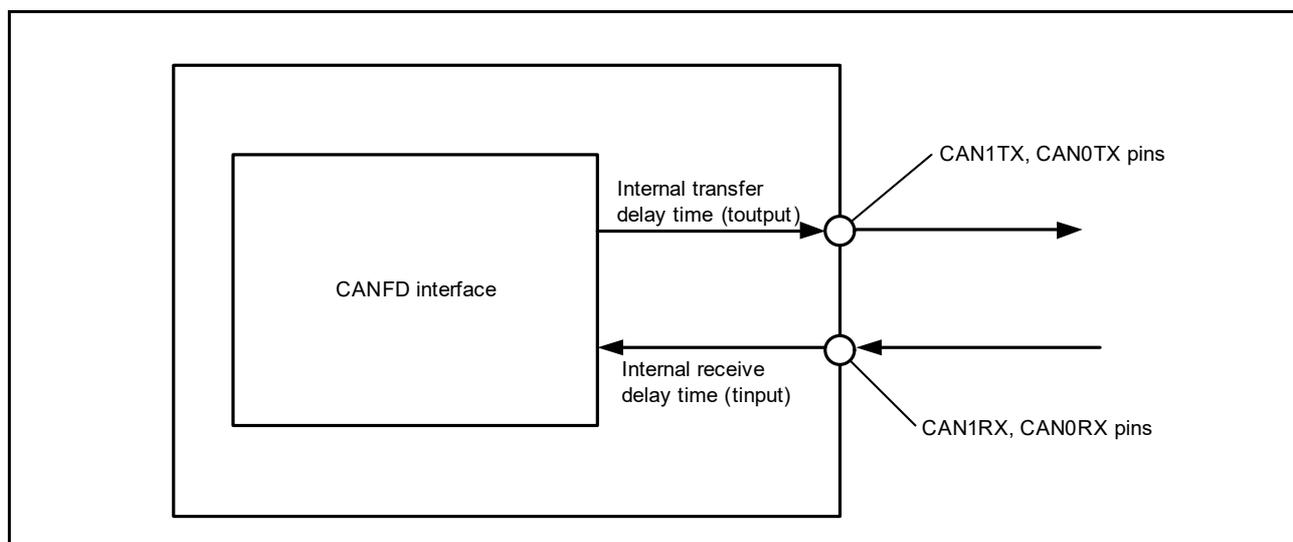


Figure 3.77    CANFD Interface Condition

## 3.4.20  Ethernet Controller (ETHERC) Timing

Table 3.24    ETHERC Timing

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC (RMII) | REF50CK cycle time | $T_{ck}$ | 20 | — | ns | Figure 3.78 to Figure 3.81 |
| | REF50CK frequency Typ. 50 MHz | — | — | 50 + 100ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII_xxxx[1] output delay time | $T_{co}$ | 2.5 | 15.0 | ns | |
| | RMII_xxxx[2] setup time | $T_{su}$ | 3 | — | ns | |
| | RMII_xxxx[2] hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII_xxxx[1][2] rise/fall time | $T_r/T_f$ | 0.5 | 6 | ns | |
| ETHERC (MII) | ET_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET_TX_EN output delay time | $t_{TENd}$ | 1 | 20 | ns | Figure 3.82 |
| | ET_ETXD0 to ET_ETXD3 output delay time | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 3.83 |
| | ET_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET_RX_DV setup time | $t_{RDVs}$ | 10 | — | ns | Figure 3.84 |
| | ET_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 3.85 |
| | ET_RX_ER hold time | $t_{RERh}$ | 10 | — | ns | |

Note 1.  RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2.  RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
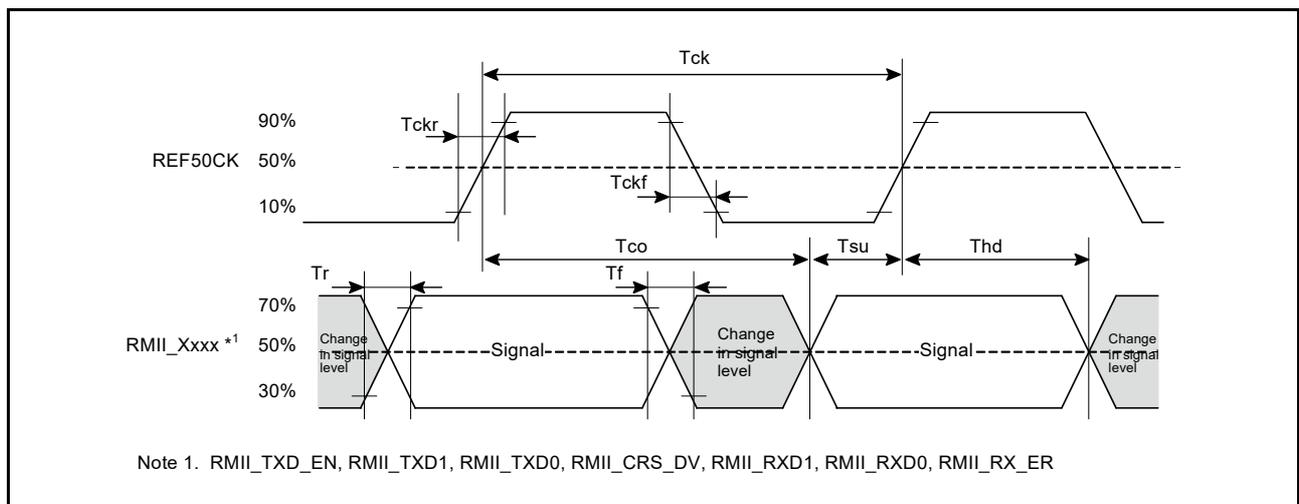


Figure 3.78    Timing with the REF50CK and RMII Signals
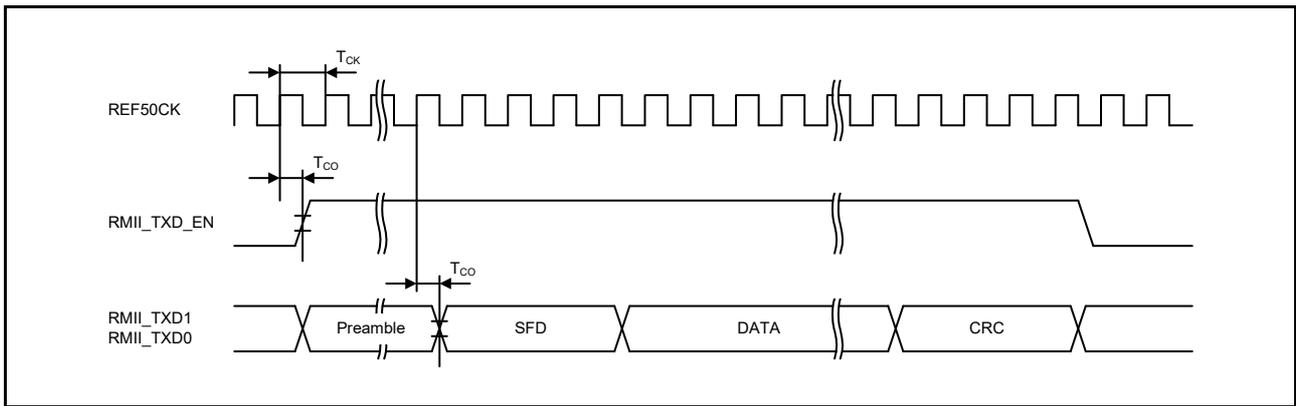
Figure 3.79        RMII Transmission Timing
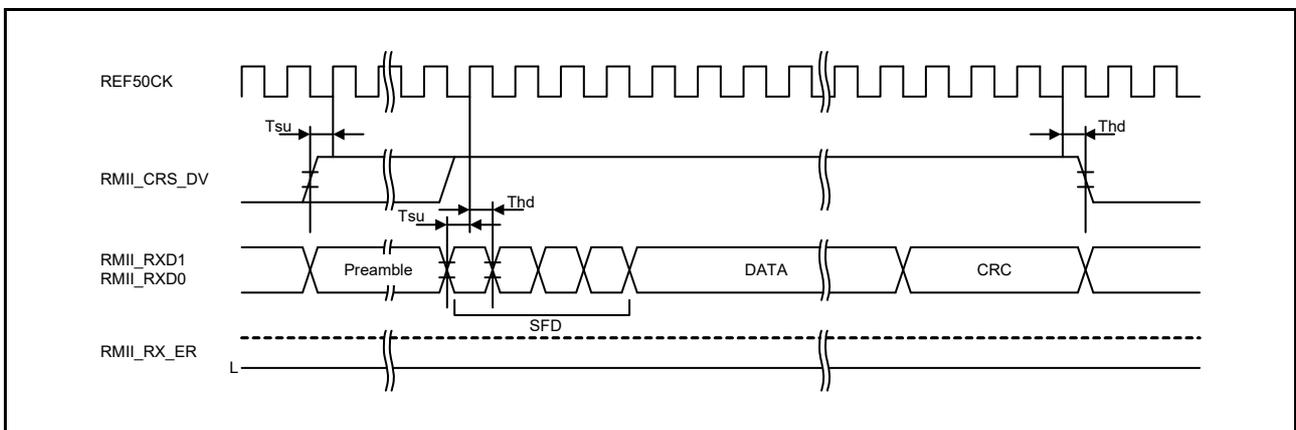


Figure 3.80        RMII Reception Timing (Normal Operation)
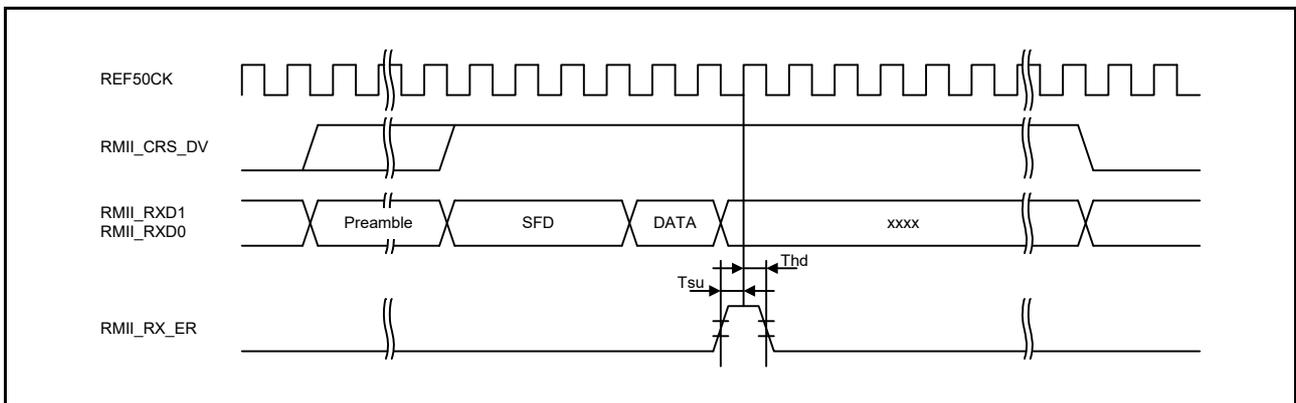


Figure 3.81        RMII Reception Timing (Error Occurrence)
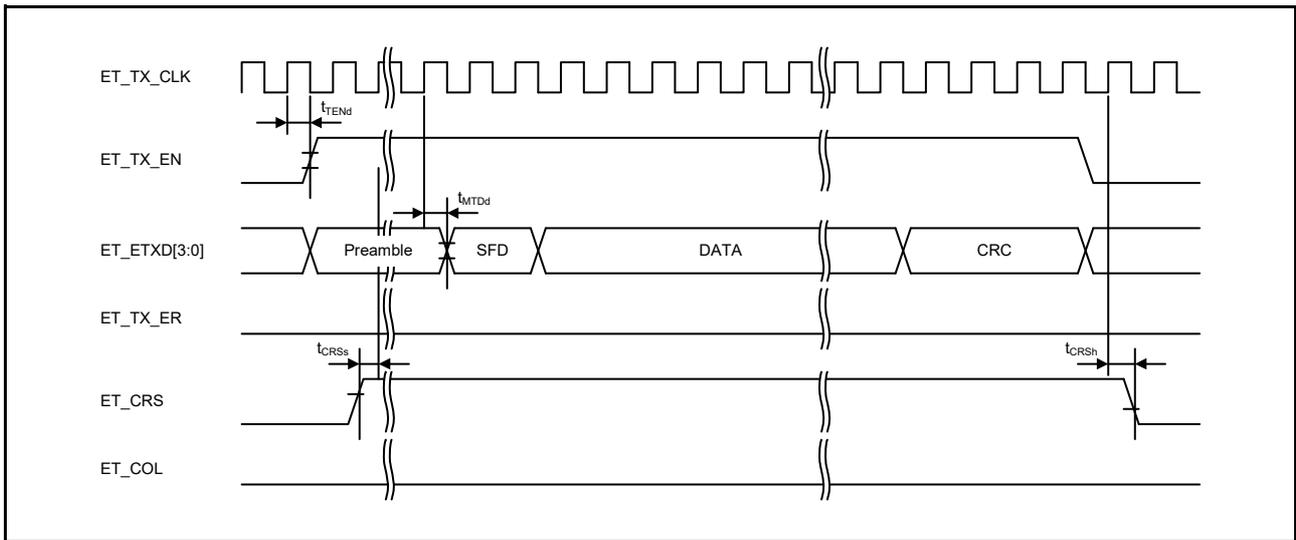
Figure 3.82        MII Transmission Timing (Normal Operation)
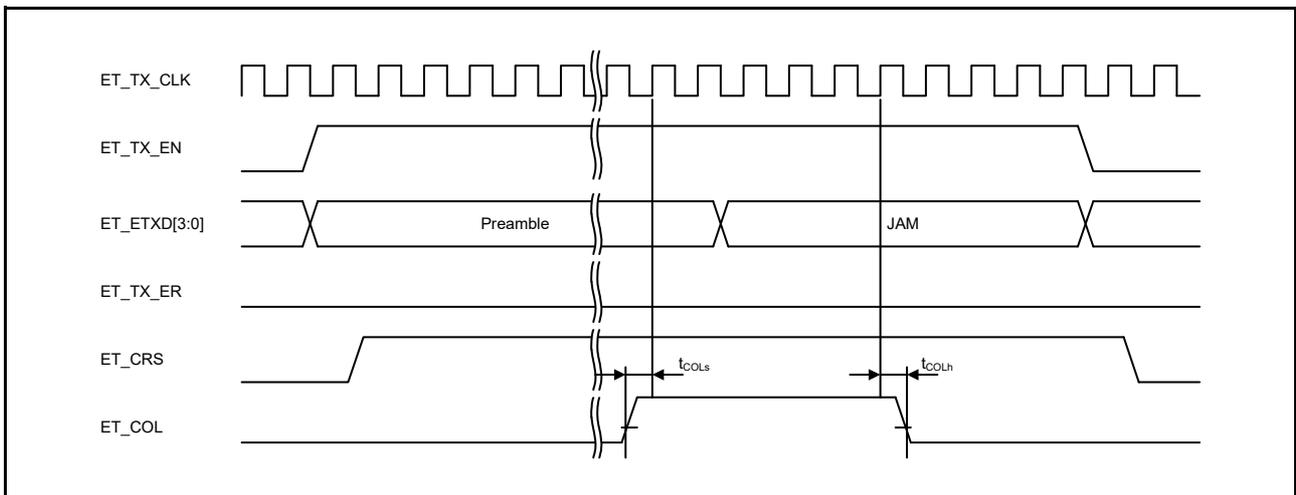


Figure 3.83        MII Transmission Timing (Conflict Occurrence)
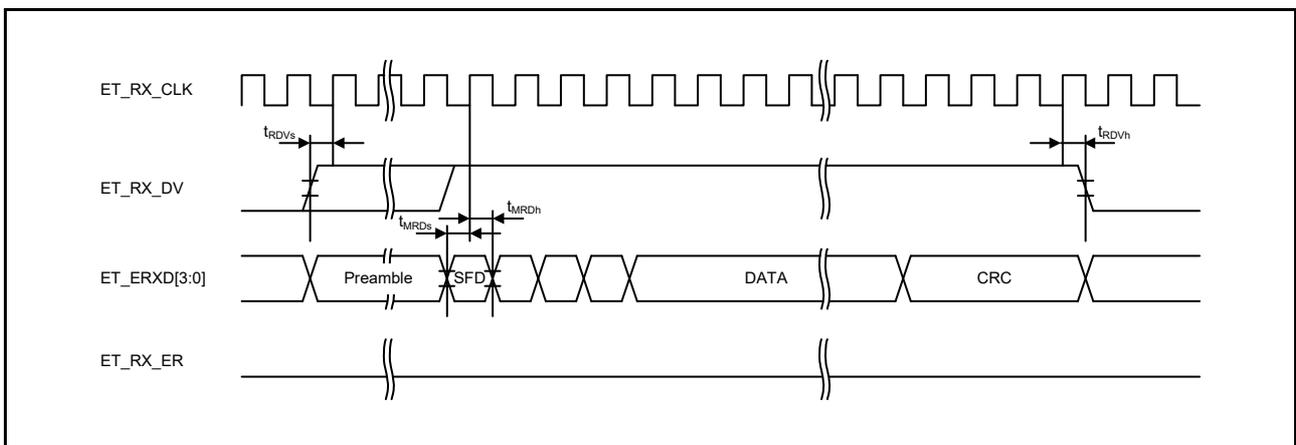


Figure 3.84        MII Reception Timing (Normal Operation)
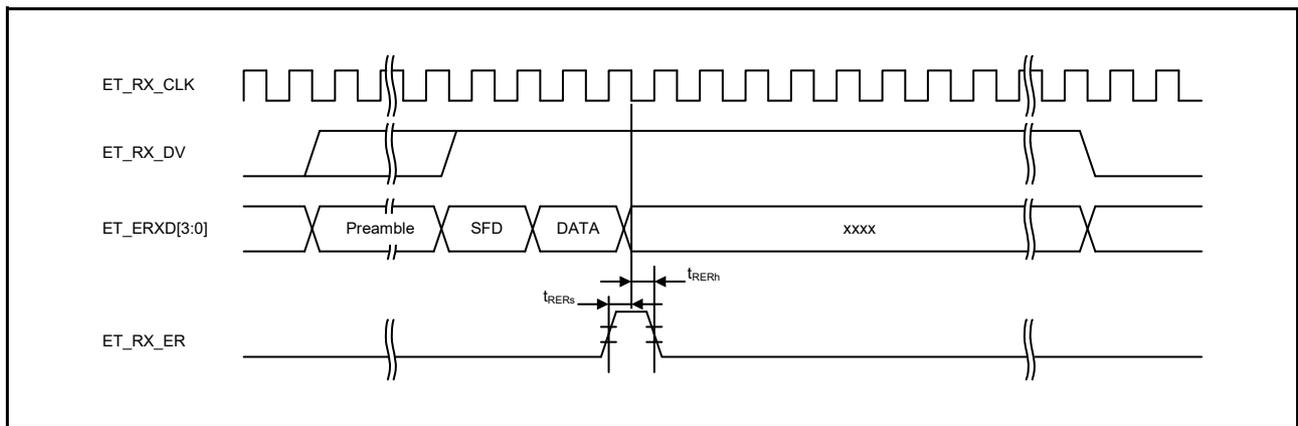
Figure 3.85        MII Reception Timing (Error Occurrence)

## 3.4.21    A/D Converter Timing

Table 3.25    A/D Converter Timing

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|------|--|--------|------|------|------|-----------------|
| ADC12 | ADC12 Trigger Input Pulse Width | $t_{TRGW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 3.86 |
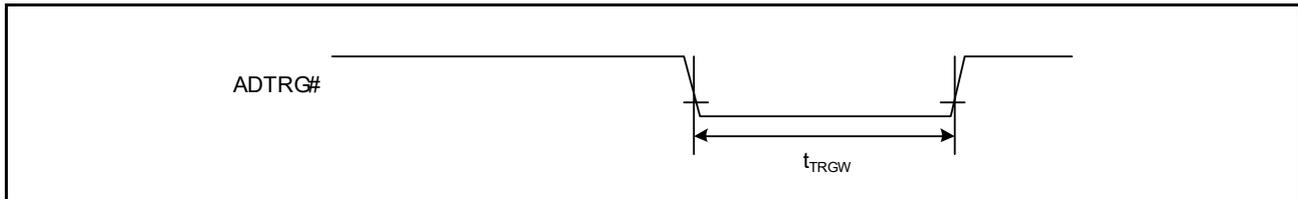


Figure 3.86    ADC12 Trigger Input Timing

## 3.4.22    NAND Flash Controller Timing

Table 3.26      NAND Flash Controller Timing

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|------|--------|------|------|------|-----------------|
| Delay time between output signals ($t_{OD}$ delay difference of each output signals) | $t_{RFD}$ | — | 5 | ns | |
| Read data setup time (based on the rising edge of NFRE#) | $t_{SD}$ | 12 | — | ns | Figure 3.87 |
| Read data hold time (based on the rising edge of NFRE#) | $t_{HD}$ | 0 | — | ns | |
| Time of NFWE# rising edge to NFRB# falling edge (NFRB# Capture start time) | $t_{WB}$ | $N \times t_{p1cyc}$[1][2] | — | ns | |
| Time of Ready to NFRE# falling edge | $t_{RR}$ | $M \times t_{p1cyc}$[1][3] | — | ns | |

Note 1.  $t_{p1cyc}$ indicates the peripheral clock 1 (P1φ) cycle.
Note 2.  N is TWB bits value of the TIME_SEQ_1 register.
Note 3.  M is TRR bits value of the TIME_SEQ_1 register.
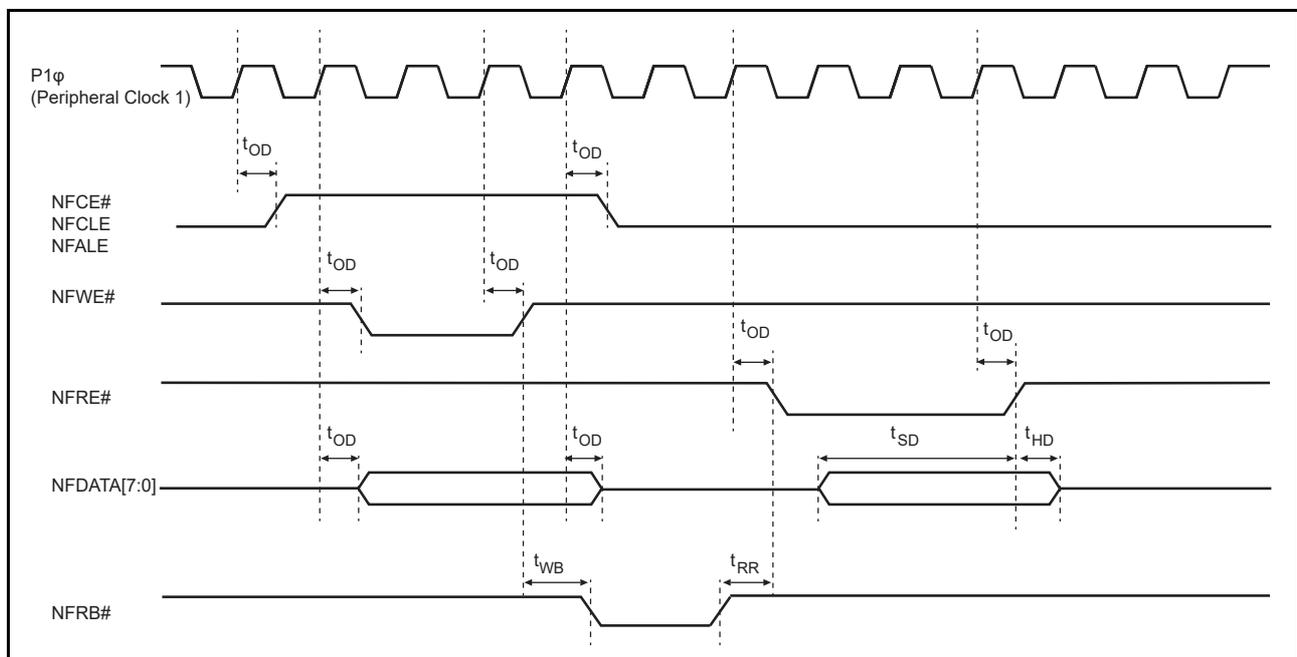


Figure 3.87      NAND Flash Controller Timing

## 3.4.23    USB 2.0 Host/Function Module Timing

Table 3.27    USB Transceiver Timing (Low-Speed)

| Item | Symbol | Min. | Max. | Unit | Figure |
|------|--------|------|------|------|--------|
| Rise time | $t_{LR}$ | 75 | 300 | ns | Figure 3.88 |
| Fall time | $t_{LF}$ | 75 | 300 | ns | |
| Rise/fall time lag | $t_{LR}/t_{LF}$ | 80 | 125 | % | |
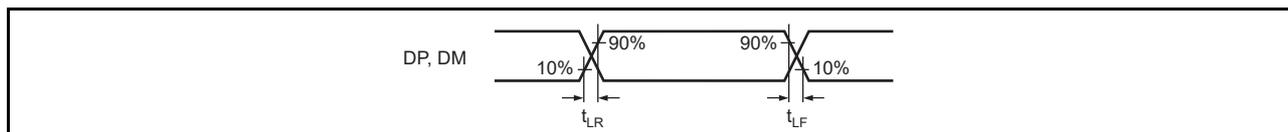


Figure 3.88    DP1, DP0, DM1, and DM0 Output Timing (Low-Speed)
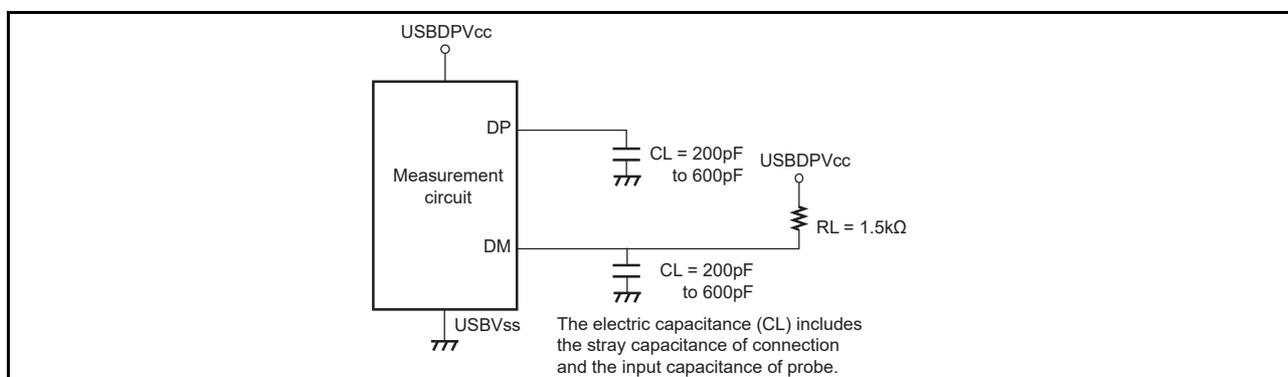


Figure 3.89    Measurement Circuit (Low-Speed)

Table 3.28    USB Transceiver Timing (Full-Speed)

| Item | Symbol | Min. | Max. | Unit | Figure |
|------|--------|------|------|------|--------|
| Rise time | $t_{FR}$ | 4 | 20 | ns | Figure 3.90 |
| Fall time | $t_{FF}$ | 4 | 20 | ns | |
| Rise/fall time lag | $t_{FR}/t_{FF}$ | 90 | 111.11 | % | |
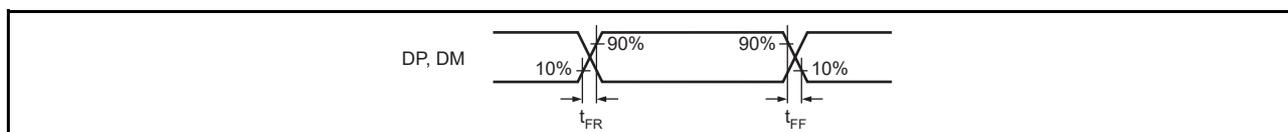


Figure 3.90    DP1, DP0, DM1, and DM0 Output Timing (Full-Speed)
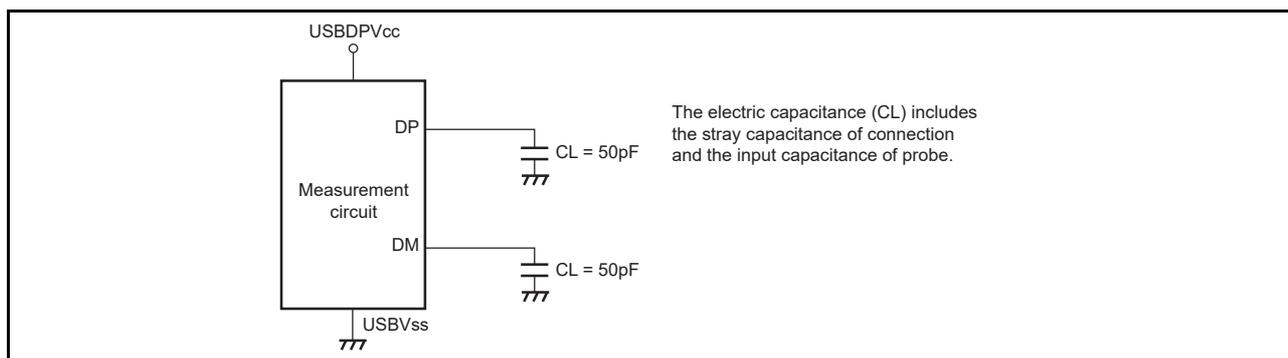


Figure 3.91    Measurement Circuit (Full-Speed)

Table 3.29      USB Transceiver Timing (Hi-Speed)

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| Rise time | $t_{HSR}$ | 500 | — | ps | Figure 3.92 |
| Fall time | $t_{HSF}$ | 500 | — | ps | |
| Output driver resistance | $Z_{HSDRV}$ | 40.5 | 49.5 | Ω | |
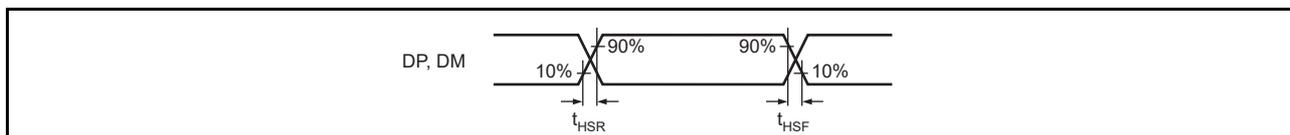


Figure 3.92      DP1, DP0, DM1, and DM0 Output Timing (Hi-Speed)
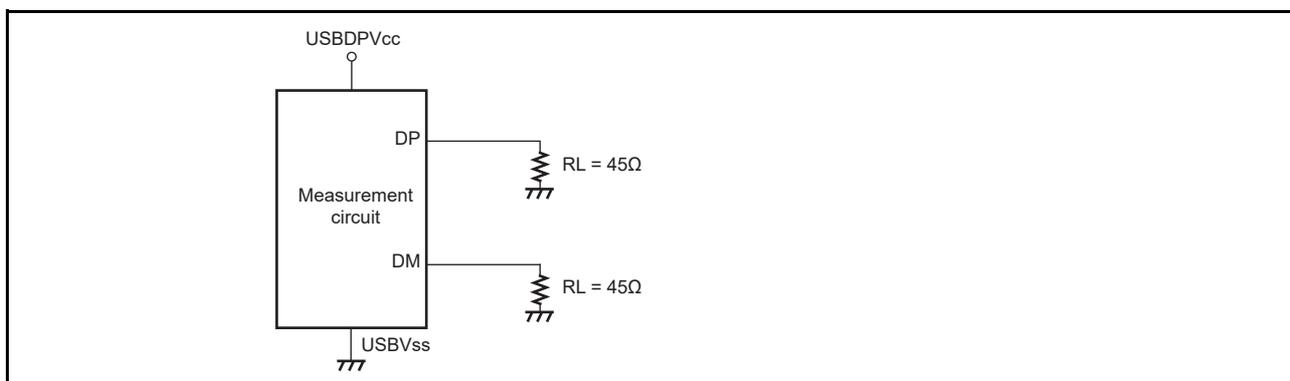


Figure 3.93      Measurement Circuit (Hi-Speed)

## 3.4.24　Video Display Controller 6 Timing

Table 3.30　Video Display Controller 6 Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| DV0_CLK input clock cycle | $t_{Dcyc}$ | 11.50 | — | ns | Figure 3.94 |
| DV0_CLK input clock low pulse width | $t_{WIL}$ | 0.4 | — | $t_{Dcyc}$ | |
| DV0_CLK input clock high pulse width | $t_{WIH}$ | 0.4 | — | | |
| LCD0_EXTCLK input clock cycle | $t_{Ecyc}$ | 11.50 | — | ns | |
| LCD0_EXTCLK input clock low pulse width | $t_{WIL}$ | 0.4 | — | $t_{Ecyc}$ | |
| LCD0_EXTCLK input clock high pulse width | $t_{WIH}$ | 0.4 | — | | |
| LCD0_CLK output clock cycle | $t_{Lcyc}$ | 11.50 | — | ns | Figure 3.95 |
| LCD0_CLK clock output low pulse width[*1] | $t_{LOL}$ | $t_{WIL} - 0.95$ | $t_{WIL} + 0.95$ | ns | |
| LCD0_CLK clock output high pulse width[*1] | $t_{LOH}$ | $t_{WIH} - 0.95$ | $t_{WIH} + 0.95$ | ns | |
| LCD0_CLK clock output low pulse width[*2] | $t_{LOL}$ | $t_{Lcyc} / 2 - 1.06$ | $t_{Lcyc} / 2 + 1.06$ | ns | |
| LCD0_CLK clock output high pulse width[*2] | $t_{LOH}$ | $t_{Lcyc} / 2 - 1.06$ | $t_{Lcyc} / 2 + 1.06$ | ns | |
| LCD0_CLK clock output rise time | $t_{LOR}$ | — | 3 | ns | |
| LCD0_CLK clock output fall time | $t_{LOF}$ | — | 3 | ns | |
| Input data setup time | $t_{VS}$ | 2 | — | ns | Figure 3.96 |
| Input data hold time | $t_{VH}$ | 4 | — | ns | |
| Output data delay time | $t_{DD}$ | −3 | 3[*3] | ns | Figure 3.97 |
| | | | 4[*4] | | |

Note 1.　This is the case when the video image clock or an external clock is selected as the clock for frequency division and the division ratio is set to 1/1.
Note 2.　This is for cases other than when the video image clock or an external clock is selected as the clock for frequency division and the division ratio is set to 1/1.
Note 3.　This is the case when normal driving ability is set with LCD0_CLK pin.
Note 4.　This is the case when high driving ability is set with LCD0_CLK pin.
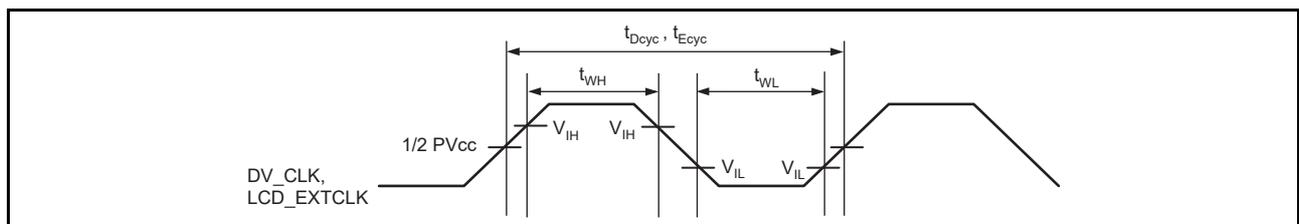


Figure 3.94　DV0_CLK and LCD0_EXTCLK Clock Input Timing
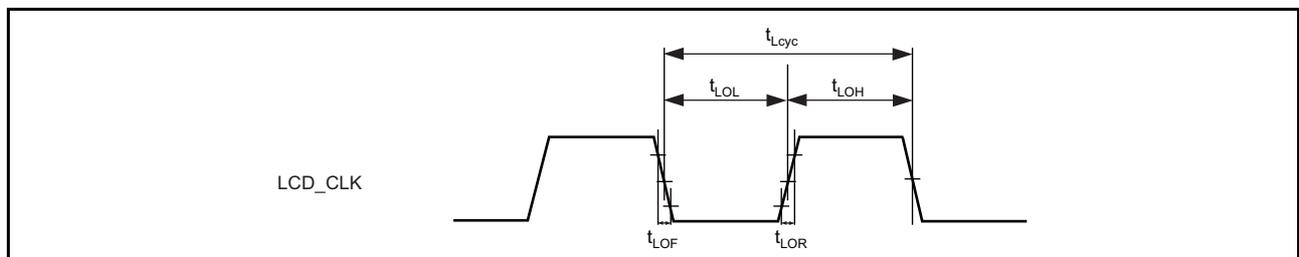


Figure 3.95　LCD0_CLK Clock Output Timing
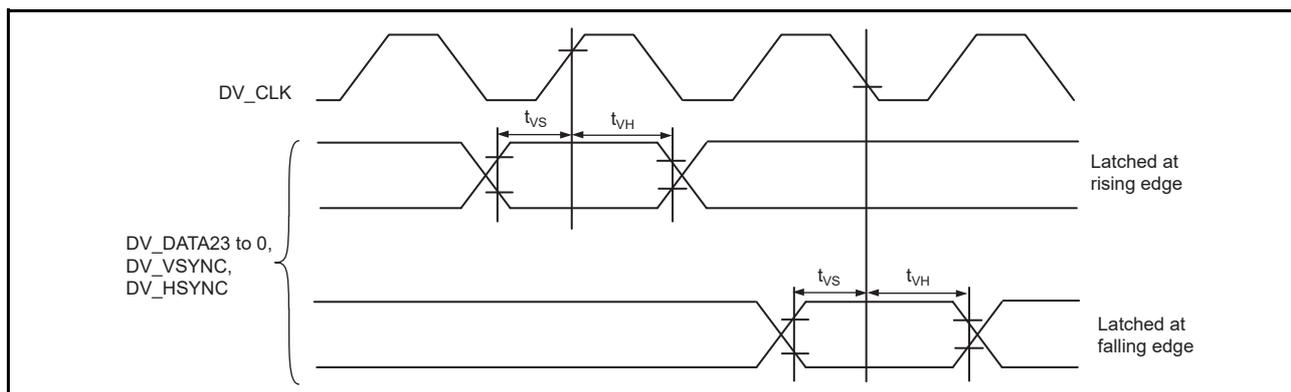
Figure 3.96        Video Input Timing
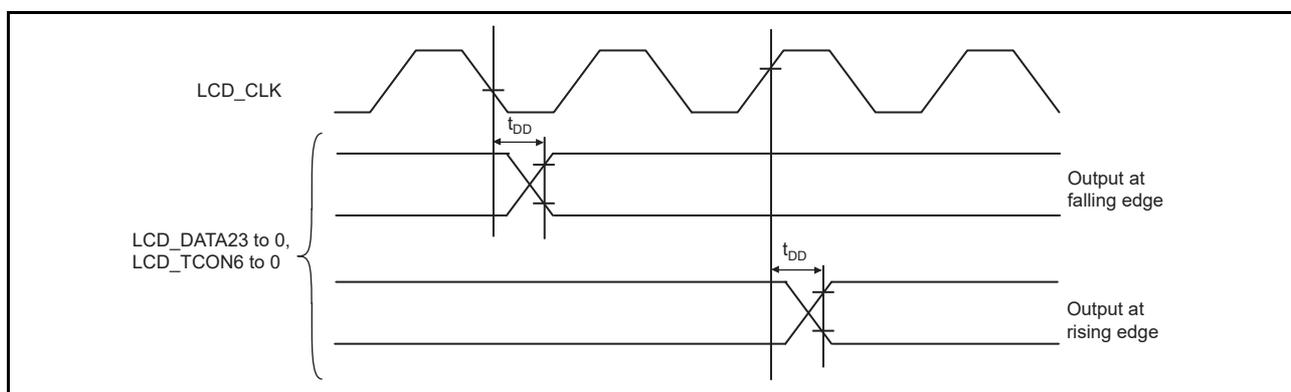


Figure 3.97        Display Output Timing

## 3.4.25      LVDS Output Interface Timing

Table 3.31      LVDS Timing

| Item | Symbol | Min. | Typ. | Max. | Unit | Figure |
|------|--------|------|------|------|------|--------|
| Panel clock for LVDS output (LSI internal signal) | T | 11.49 (87 MHz) | — | 24.1 (41.43 MHz) | ns | Figure 3.98 |
| Transmitter Output Pulse Position for Bit1 | TPPos1 | −0.20 | 0 | 0.20 | ns | |
| Transmitter Output Pulse Position for Bit0 | TPPos0 | $T / 7 - 0.20$ | $T / 7$ | $T / 7 + 0.20$ | ns | |
| Transmitter Output Pulse Position for Bit6 | TPPos6 | $T \times 2 / 7 - 0.20$ | $T \times 2 / 7$ | $T \times 2 / 7 + 0.20$ | ns | |
| Transmitter Output Pulse Position for Bit5 | TPPos5 | $T \times 3 / 7 - 0.20$ | $T \times 3 / 7$ | $T \times 3 / 7 + 0.20$ | ns | |
| Transmitter Output Pulse Position for Bit4 | TPPos4 | $T \times 4 / 7 - 0.20$ | $T \times 4 / 7$ | $T \times 4 / 7 + 0.20$ | ns | |
| Transmitter Output Pulse Position for Bit3 | TPPos3 | $T \times 5 / 7 - 0.20$ | $T \times 5 / 7$ | $T \times 5 / 7 + 0.20$ | ns | |
| Transmitter Output Pulse Position for Bit2 | TPPos2 | $T \times 6 / 7 - 0.20$ | $T \times 6 / 7$ | $T \times 6 / 7 + 0.20$ | ns | |
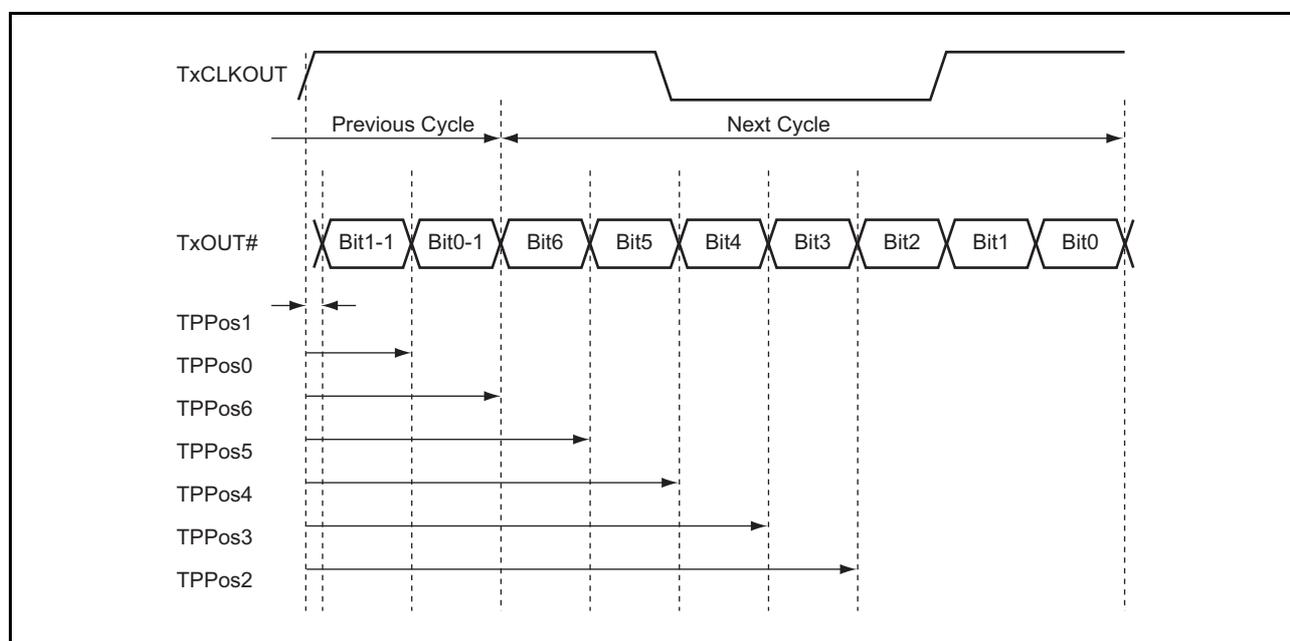


Figure 3.98      Transmitter LVDS Output Pulse Position Measurement

## 3.4.26    Capture Engine Unit Timing

Table 3.32    Capture Engine Unit Signal Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| Vertical sync (VIO_VD) setup time (Camera clock rising) | $t_{VVDS}$ | 2 | — | ns | Figure 3.99 (1) , Figure 3.99 (2) |
| Vertical sync (VIO_VD) setup time (Camera clock falling) | $t_{VVDS}$ | 2.5 | — | ns | |
| Vertical sync (VIO_VD) hold time | $t_{VVDH}$ | 3.5 | — | ns | |
| Horizontal sync (VIO_HD) setup time (Camera clock rising) | $t_{VHDS}$ | 2 | — | ns | |
| Horizontal sync (VIO_HD) setup time (Camera clock falling) | $t_{VHDS}$ | 2.5 | — | ns | |
| Horizontal sync (VIO_HD) hold time | $t_{VHDH}$ | 3.5 | — | ns | |
| Capture image data (VIO_D) setup time (Camera clock rising) | $t_{VDTS}$ | 2 | — | ns | |
| Capture image data (VIO_D) setup time (Camera clock falling) | $t_{VDTS}$ | 2.5 | — | ns | |
| Capture image data (VIO_D) hold time | $t_{VDTH}$ | 3.5 | — | ns | |
| Camera clock cycle | $t_{VCYC}$ | 11.50 | — | ns | |
| Camera clock high level width | $t_{VHW}$ | $0.4 \times t_{VCYC}$ | — | ns | |
| Camera clock low level width | $t_{VLW}$ | $0.4 \times t_{VCYC}$ | — | ns | |
| Field identification signal (VIO_FLD) setup time (Camera clock rising) | $t_{VFDS}$ | 2 | — | ns | |
| Field identification signal (VIO_FLD) setup time (Camera clock falling) | $t_{VFDS}$ | 2.5 | — | ns | |
| Field identification signal (VIO_FLD) hold time | $t_{VFDH}$ | 3.5 | — | ns | |
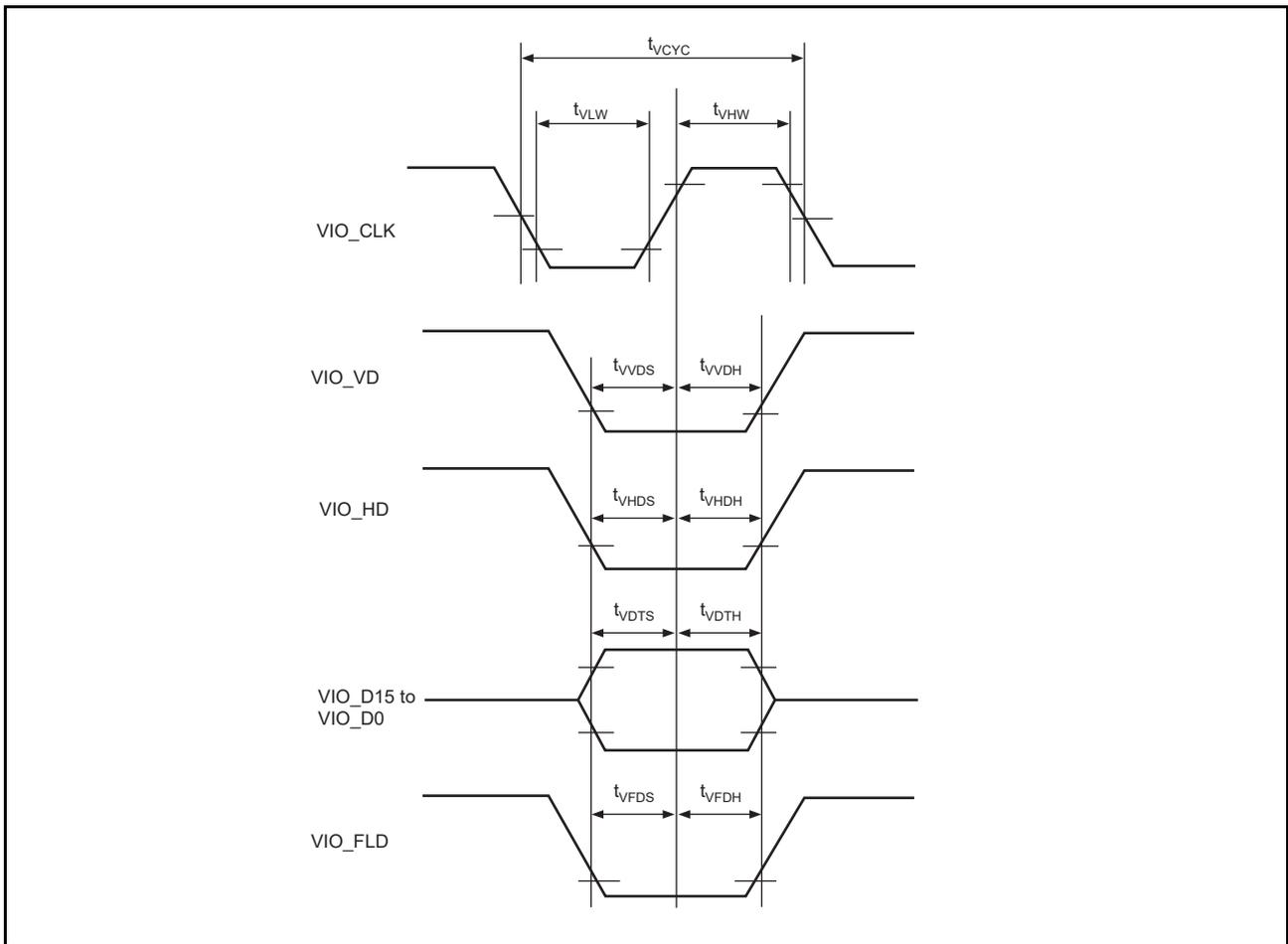
Figure 3.99          (1) Capture Engine Unit Module Signal Timing of data capturing on the rising edge of VIO_CLK
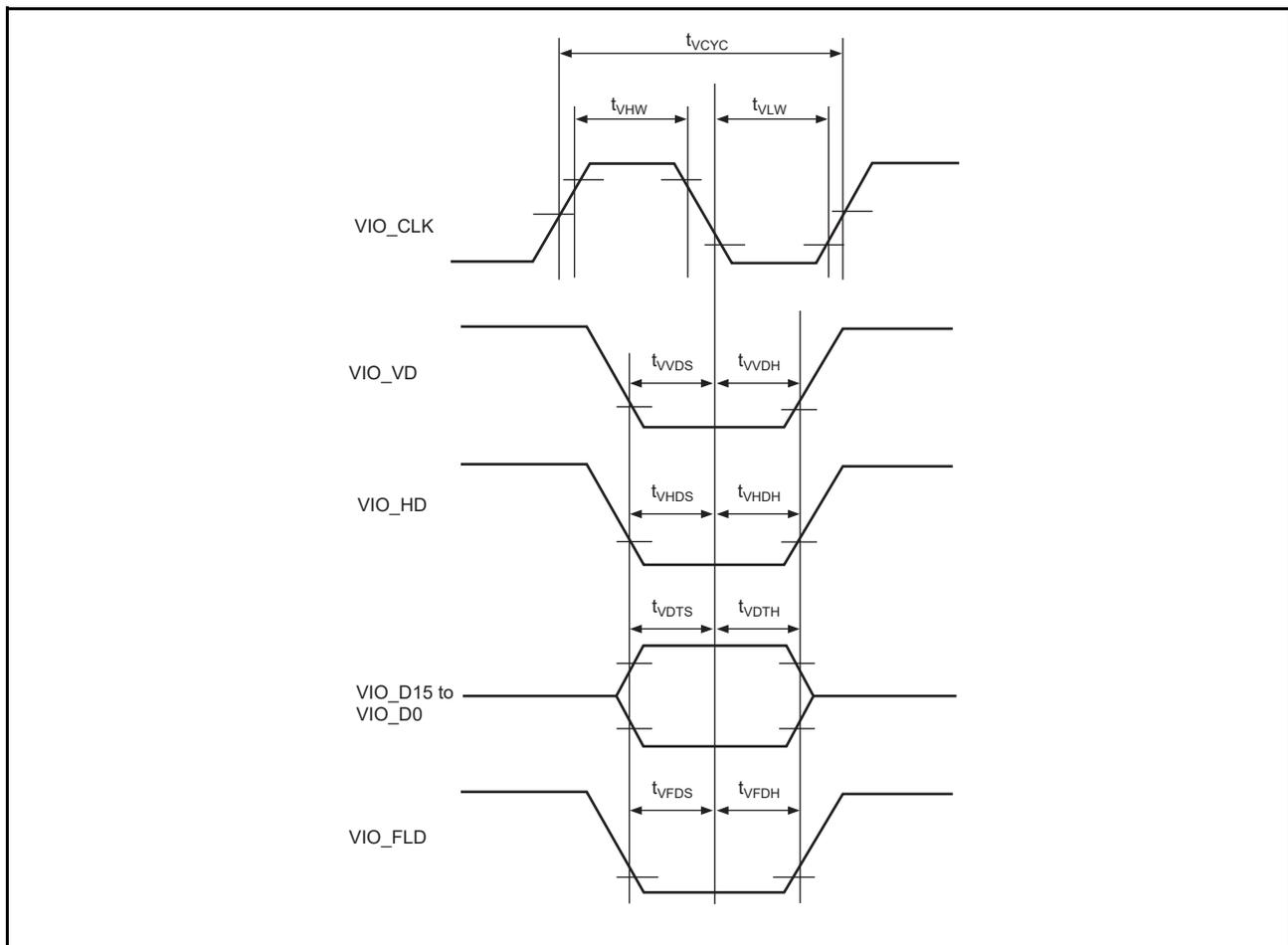
Figure 3.99        (2) Capture Engine Unit Module Signal Timing of data capturing on the falling edge of VIO_CLK

## 3.4.27    MIPI CSI-2 Interface Timing

Table 3.33    MIPI CSI-2 Interface Timing

| Item | Symbol | Min. | Max. | Unit | Remarks | Figure |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | 1 | 12.5 | ns | | Figure 3.100 |
| Common–mode interference beyond 450 MHz | $\Delta V_{CMRX(HF)}$ | — | 100 | mV | HS Receiver | |
| Common–mode interference 50MHz – 450MHz | $\Delta V_{CMRX(LF)}$ | –50 | 50 | mV | HS Receiver | |
| Setup time | $T_{CDS}$ | 0.15 | — | UI | HS Receiver | Figure 3.100 |
| Hold time | $T_{CDH}$ | 0.15 | — | UI | HS Receiver | Figure 3.100 |
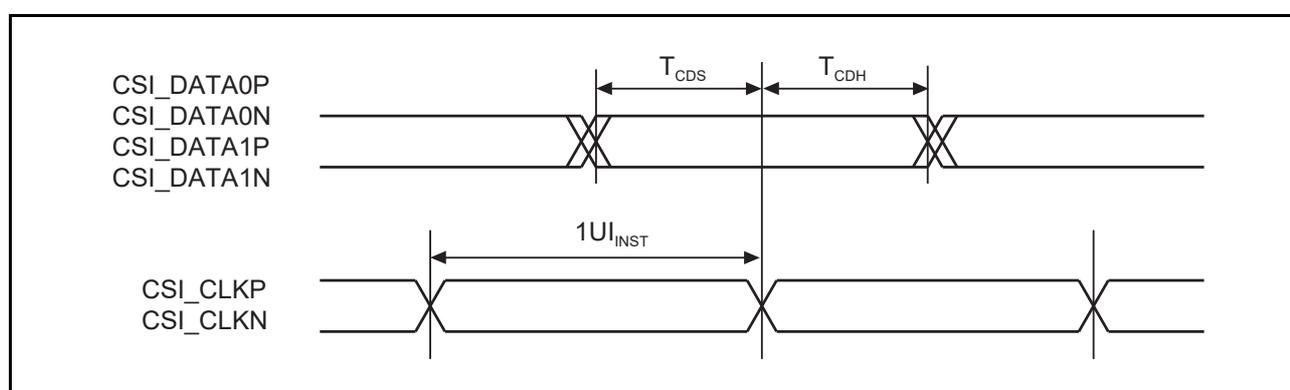


Figure 3.100    MIPI CSI-2 Interface Timing

## 3.4.28    SD/MMC Host Interface Timing

### 3.4.28.1    SD Interface

Table 3.34      SD/MMC Host Interface Timing (SD Default/High Speed mode 3.3-V power supply selection)

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| SD_CLK clock cycle | $t_{SDPP}$ | $4 \times t_{bcyc}$ | — | ns | Figure 3.101 |
| SD_CLK clock high level width | $t_{SDWH}$ | $0.4 \times t_{SDPP}$ | — | ns | |
| SD_CLK clock low level width | $t_{SDWL}$ | $0.4 \times t_{SDPP}$ | — | ns | |
| SD_CLK clock rise time | $t_{SDLH}$ | — | 3 | ns | |
| SD_CLK clock fall time | $t_{SDHL}$ | — | 3 | ns | |
| SD_CMD, SD_D7 to SD_D0 output data delay time | $t_{SDODLY}$ | −8 | 4 | ns | |
| SD_CMD, SD_D7 to SD_D0 input data setup time | $t_{SDISU}$ | 4.5 | — | ns | |
| SD_CMD, SD_D7 to SD_D0 input data hold time | $t_{SDIH}$ | 2 | — | ns | |

Note:   $t_{bcyc}$ indicates internal bus clock (Bφ) cycle.
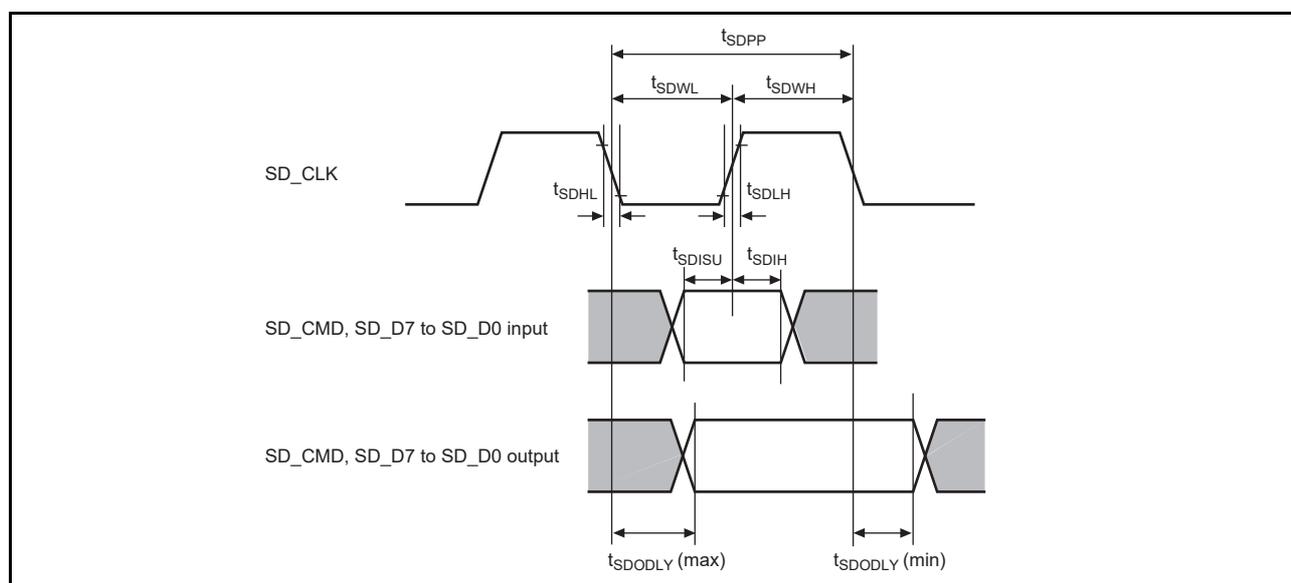


Figure 3.101      SD/MMC Host Interface (SD Interface)

Other characteristics of the SD interface are available upon non-disclosure agreement.
For details, contact your local sales representatives.

## 3.4.28.2 MMC Interface Timing

Table 3.35 SD/MMC Host Interface Timing (MMC Default/High Speed mode 3.3-V power supply selection)

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| SD_CLK clock cycle | $t_{MMCPP}$ | $4 \times t_{bcyc}$ | — | ns | Figure 3.102 |
| SD_CLK clock high level width | $t_{MMCWH}$ | $0.4 \times t_{MMCPP}$ | — | ns | |
| SD_CLK clock low level width | $t_{MMCWL}$ | $0.4 \times t_{MMCPP}$ | — | ns | |
| SD_CLK clock rise time | $t_{MMCLH}$ | — | 3 | ns | |
| SD_CLK clock fall time | $t_{MMCHL}$ | — | 3 | ns | |
| SD_CMD, SD_D7 to SD_D0 output data delay time | $t_{MMCODLY}$ | −7 | 4 | ns | |
| SD_CMD, SD_D7 to SD_D0 input data setup time | $t_{MMCISU}$ | 4.5 | — | ns | |
| SD_CMD, SD_D7 to SD_D0 input data hold time | $t_{MMCIH}$ | 2 | — | ns | |

Note: $t_{bcyc}$ indicates internal bus clock (Bφ) cycle.
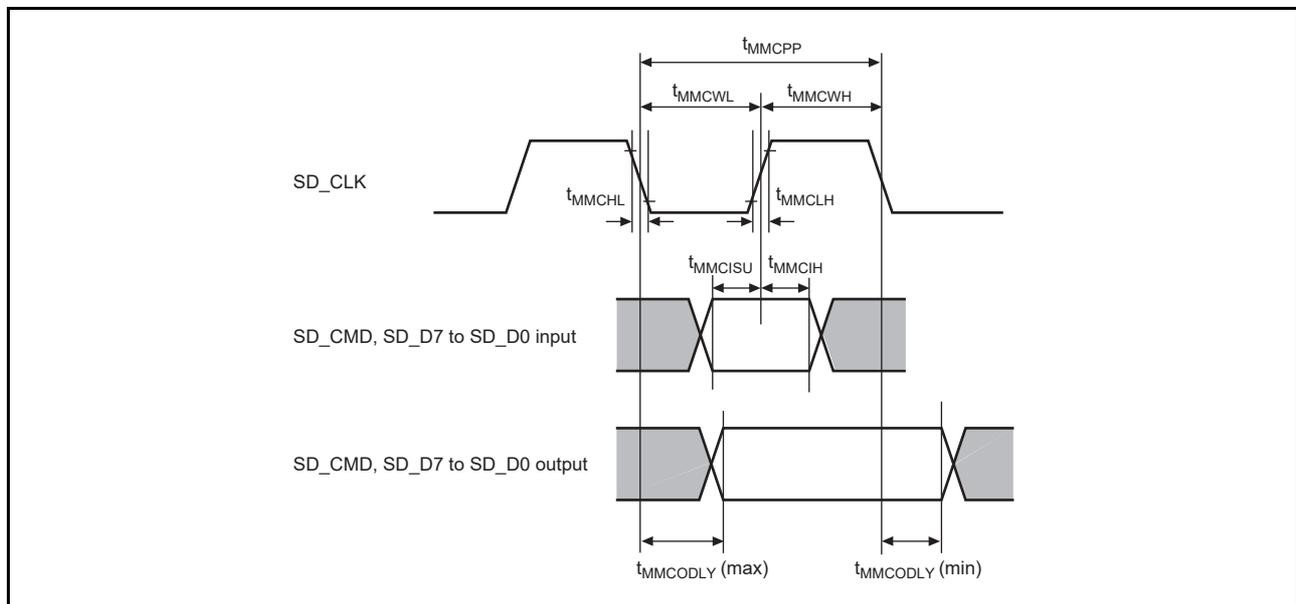


Figure 3.102 SD/MMC Host Interface (MMC Interface Default/High Speed mode 3.3-V power supply selection)

Table 3.36 SD/MMC Host Interface Timing (MMC HS-DDR mode 3.3-/1.8-V power supply selection)

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| SD_CLK clock cycle | $t_{MMCPP}$ | $4 \times t_{bcyc}$ | — | ns | Figure 3.103, Figure 3.104 |
| SD_CLK clock high level width | $t_{MMCWH}$ | $0.45 \times t_{MMCPP}$ | — | ns | |
| SD_CLK clock low level width | $t_{MMCWL}$ | $0.45 \times t_{MMCPP}$ | — | ns | |
| SD_CLK clock rise time | $t_{MMCLH}$ | — | 3 | ns | |
| SD_CLK clock fall time | $t_{MMCHL}$ | — | 3 | ns | |
| SD_CMD output data delay time | $t_{MMCODLY}$ | −6.6 | 6.6 | ns | Figure 3.103 |
| SD_CMD input data setup time | $t_{MMCISU}$ | 5.5 | — | ns | |
| SD_CMD input data hold time | $t_{MMCIH}$ | 2.5 | — | ns | |
| SD_D7 to SD_D0 output data delay time | $t_{MMCODLYddr}$ | 2.5 | $0.5 \times t_{bcyc} + 3$ | ns | Figure 3.104 |
| SD_D7 to SD_D0 input data setup time | $t_{MMCISUddr}$ | 2.6 | — | ns | |
| SD_D7 to SD_D0 input data hold time | $t_{MMCIHddr}$ | 1.5 | — | ns | |

Note: $t_{bcyc}$ indicates internal bus clock (Bφ) cycle.
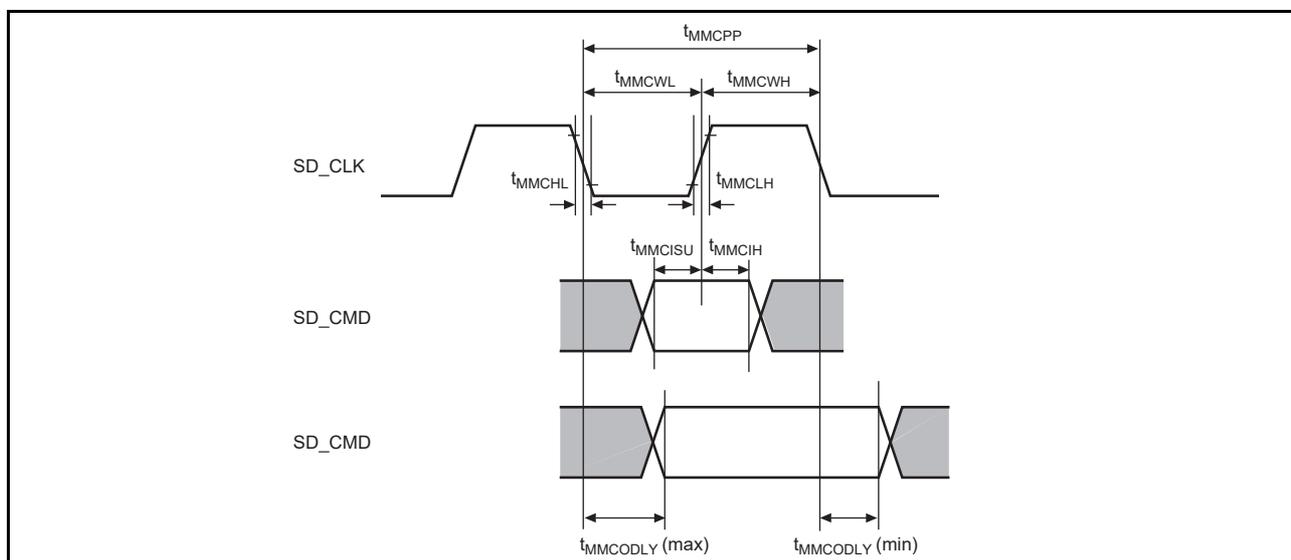


Figure 3.103 SD_CMD, SD/MMC Host Interface (MMC Interface HS-DDR mode 3.3-/1.8-V power supply selection)
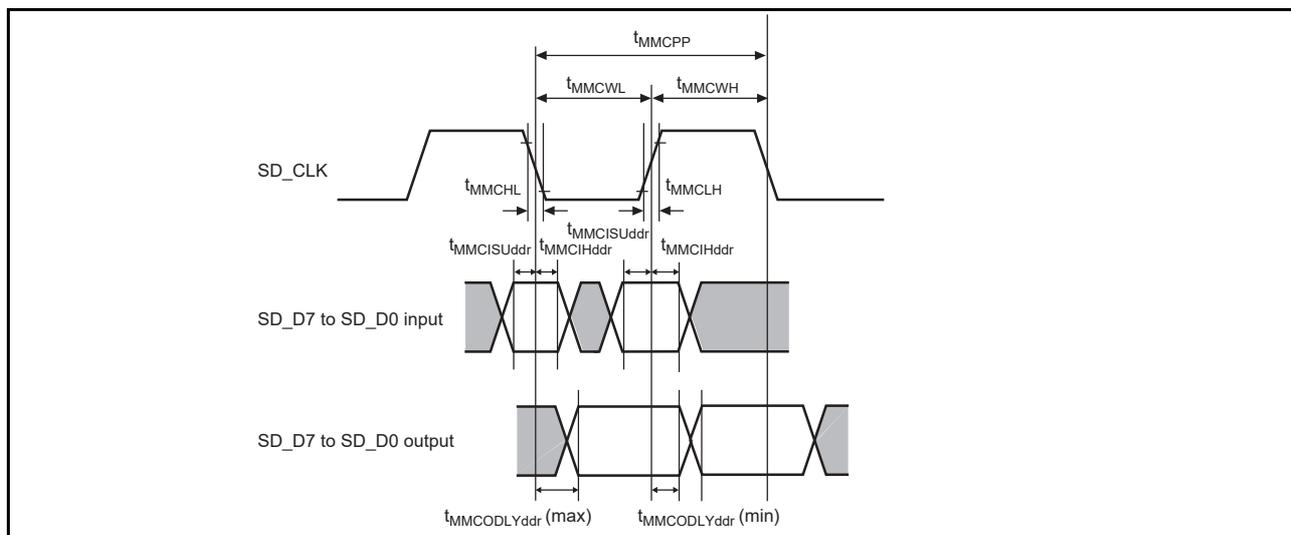


Figure 3.104 SD_D7 to SD_D0, SD/MMC Host Interface (MMC Interface HS-DDR mode 3.3-/1.8-V power supply selection)

Table 3.37   SD/MMC Host Interface Timing (MMC HS200 mode 1.8-V power supply selection, Output load: 15pF)

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| SD_CLK clock cycle | $t_{MMCPP}$ | $1 \times t_{bcyc}$[1] | — | ns | Figure 3.105 |
| SD_CLK clock high level width | $t_{MMCWH}$ | $0.35 \times t_{MMCPP}$ | — | ns | |
| SD_CLK clock low level width | $t_{MMCWL}$ | $0.35 \times t_{MMCPP}$ | — | ns | |
| SD_CLK clock rise time | $t_{MMCLH}$ | — | 1.5 | ns | |
| SD_CLK clock fall time | $t_{MMCHL}$ | — | 1.5 | ns | |
| SD_CMD, SD_D7 to SD_D0 output data delay time | $t_{MMCODLY}$ | −1.7 | 1.1 | ns | |
| SD_CMD, SD_D7 to SD_D0 input data setup time[2] | $t_{MMCISU}$ | — | — | ns | |
| SD_CMD, SD_D7 to SD_D0 input data hold time[2] | $t_{MMCIH}$ | — | — | ns | |
| SD_CMD, SD_D7 to SD_D0 input data width[2] | $t_{MMCIDW}$ | 3.6 | — | ns | |

Note 1.   $t_{bcyc}$ indicates internal bus (Bφ) cycle.
Note 2.   In HS200 mode, tuning by SCC is required. For details, see section 49.6, Sampling Clock Controller (SCC), in the RZ/A2M Group User's Manual.
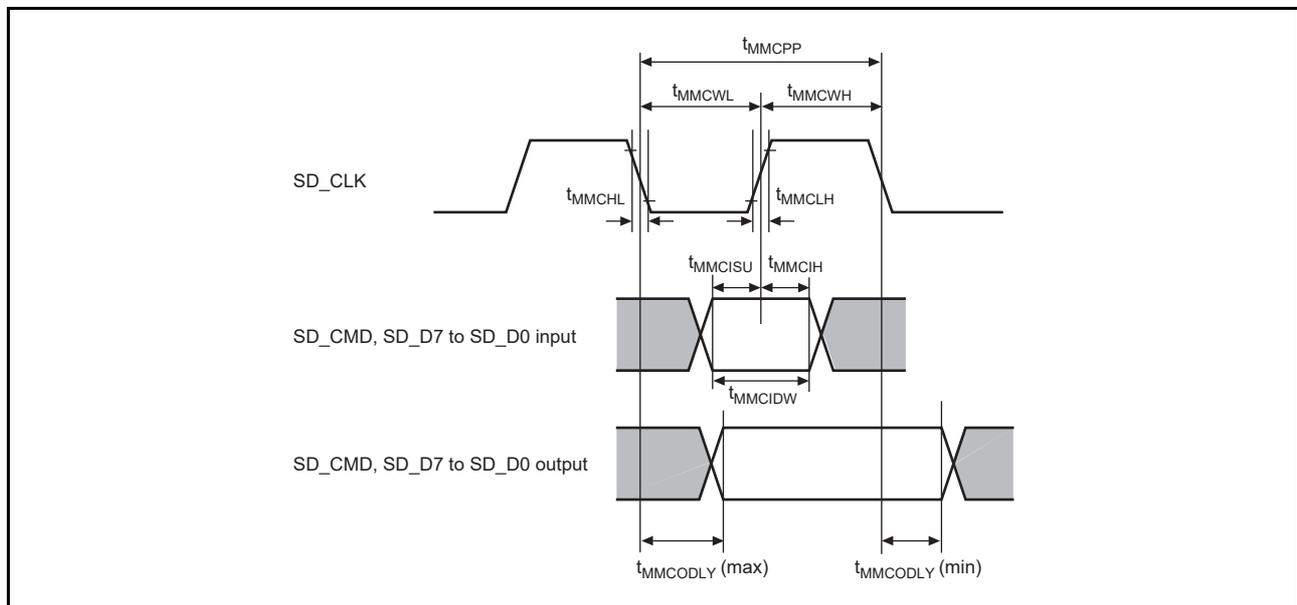


Figure 3.105   SD/MMC Host Interface (MMC Interface HS200 mode 1.8-V power supply selection)

## 3.4.29     General Purpose I/O Ports Timing

Table 3.38     General Purpose I/O Ports Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|------|--------|------|------|------|--------|
| Output data delay time | $t_{PORTD}$ | — | 100 | ns | Figure 3.106 |
| Input data setup time | $t_{PORTS}$ | 100 | — | | |
| Input data hold time | $t_{PORTH}$ | 100 | — | | |
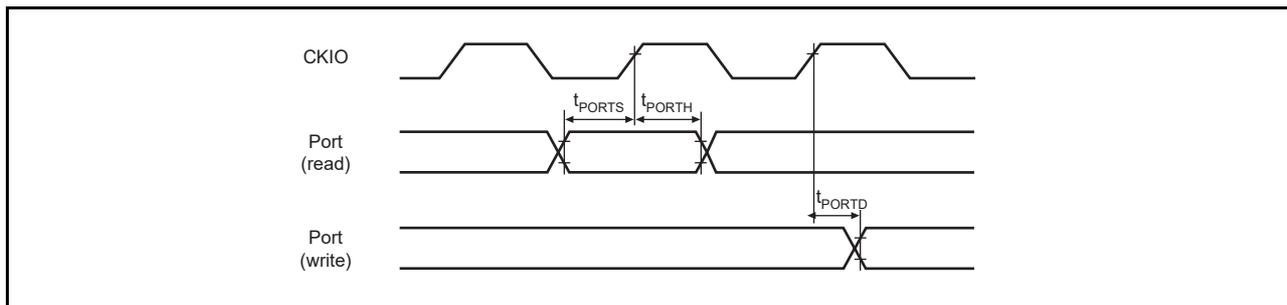


Figure 3.106     General I/O Ports Timing

## 3.4.30    Debugger Interface Timing

Table 3.39    Debugger Interface Timing

| Item | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| TCK cycle time | $t_{TCKcyc}$ | 50[*1] | — | ns | Figure 3.107 |
| TCK high pulse width | $t_{TCKH}$ | 0.4 | 0.6 | $t_{TCKcyc}$ | |
| TCK low pulse width | $t_{TCKL}$ | 0.4 | 0.6 | $t_{TCKcyc}$ | |
| TDI setup time | $t_{TDIS}$ | 10 | — | ns | Figure 3.108 |
| TDI hold time | $t_{TDIH}$ | 10 | — | ns | |
| TMS/SWDIO setup time | $t_{TMSS}$ | 10 | — | ns | |
| TMS/SWDIO hold time | $t_{TMSH}$ | 10 | — | ns | |
| SWDIO delay time | $t_{SWDO}$ | — | 16 | ns | |
| TDO delay time | $t_{TDOD}$ | — | 16 | ns | |
| Capture register setup time | $t_{CAPTS}$ | 10 | — | ns | Figure 3.109 |
| Capture register hold time | $t_{CAPTH}$ | 10 | — | ns | |
| Update register delay time | $t_{UPDATED}$ | — | 20 | ns | |
| Trace clock cycle | $t_{TCYC}$ | 7.57 | — | ns | Figure 3.110 |
| Trace clock high level | $t_{THC}$ | 2.5 | — | ns | Output load: 15 pF |
| Trace clock low level | $t_{TLC}$ | 2.5 | — | ns | |
| Trace data delay time | $t_{TDT}$ | $0.1 \times t_{TCYC} - 0.1$ | $0.4 \times t_{TCYC} - 0.2$ | ns | |

Note 1.  Should be greater than the peripheral clock 0 (P0φ) cycle time.
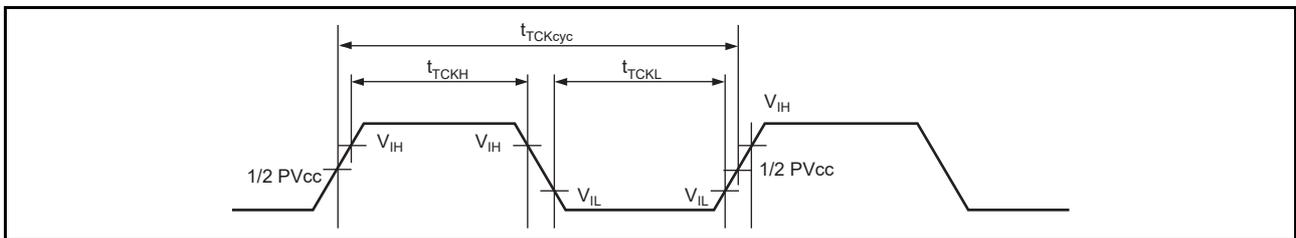


Figure 3.107    TCK Input Timing
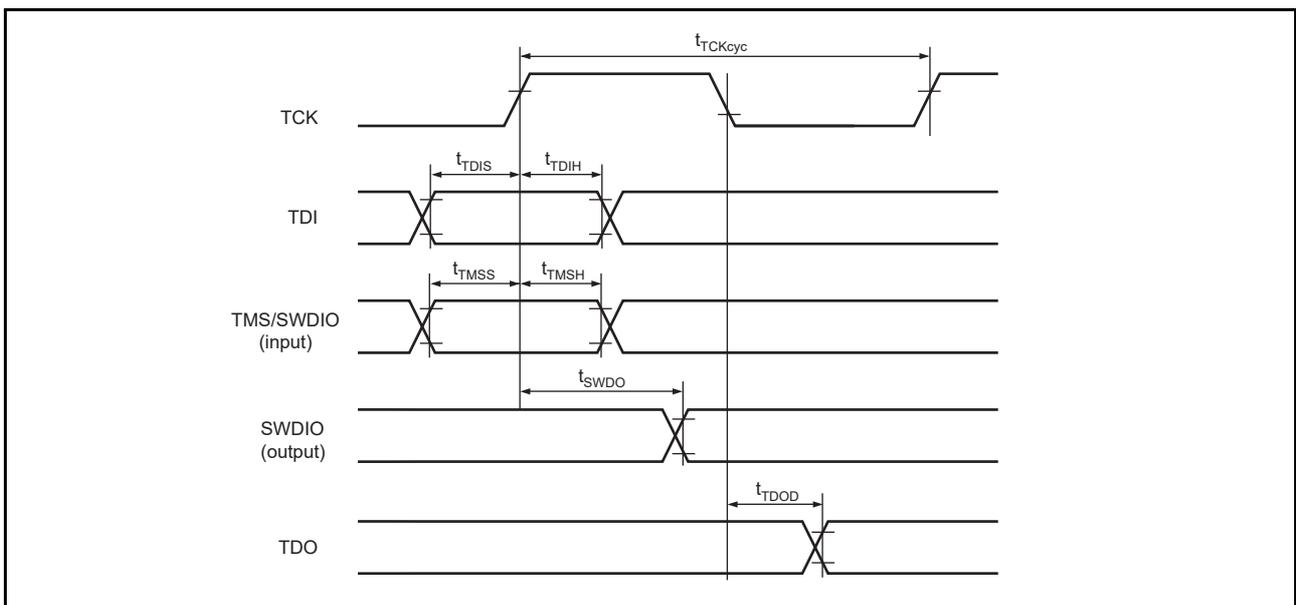


Figure 3.108    Data Transfer Timing
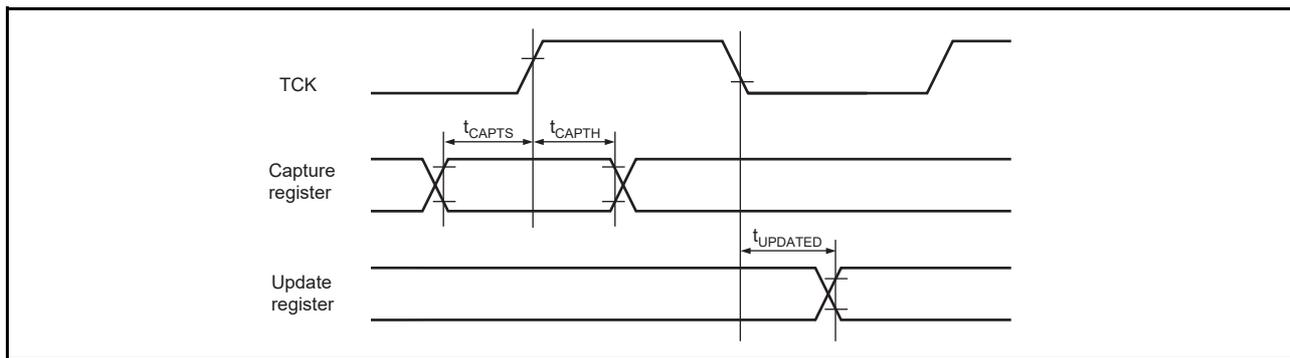
Figure 3.109    Boundary Scan Input/Output I/O Timing
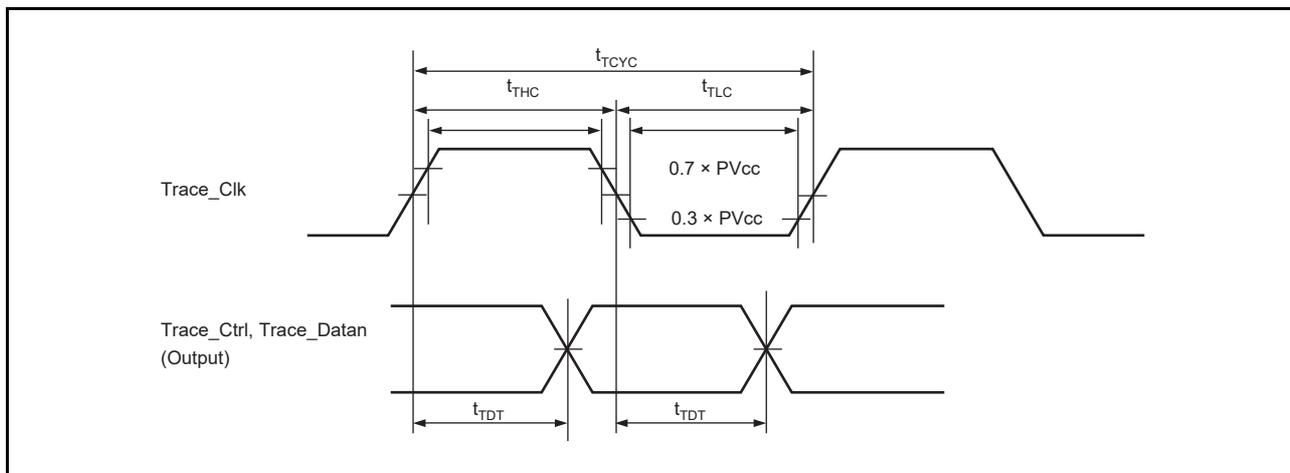


Figure 3.110    Trace Interface Timing

### 3.4.31   AC Characteristics Measurement Conditions

- I/O signal reference level: PVcc/2, PVcc_SPI/2, PVcc_HO/2, PVcc_SD0/2, PVcc_SD1/2, the minimum values of $V_{IH}$, $V_{T+}$, and $V_{OH}$, and the maximum values of $V_{IL}$, $V_{T-}$, and $V_{OL}$ (refer to the individual timing chart)

- Input pulse level: PVcc, PVcc_SPI, PVcc_HO, PVcc_SD0, and PVcc_SD1

- Input rise and fall times: 1 ns
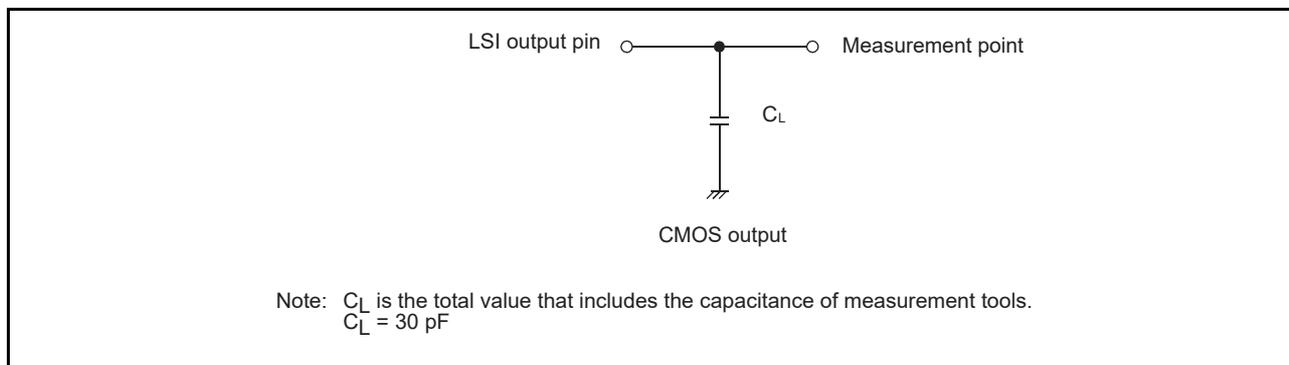


Figure 3.111    Output Load Circuit

## 3.5    A/D Converter Characteristics

Conditions: Vcc = 1.14 to 1.26 V, PVcc = USBDPVcc0 = USBDPVcc1 = AVcc = 3.0 to 3.6 V,

PVcc_SPI = 3.0 to 3.6 V/1.7 to 1.9 V, PVcc_SD0 = 3.0 to 3.6 V/1.7 to 1.9 V, PVcc_SD1 = 3.0 to 3.6V/1.7 to

1.9V, PLLVcc = 1.14 to 1.26 V, USBAPVcc0 = USBAPVcc1 = 3.0 to 3.6 V,  LVDSAPVcc = 3.0 to 3.6 V,

LVDSPLLVcc = 1.14 to 1.26 V, PVcc_HO = MIPIAVcc18 = 1.7 to 1.9 V,

Vss = AVss = USBVss = 0 V

Ta = −40 to +85℃, Tj = −40 to +125℃

Table 3.40    A/D Converter Characteristics

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 8 | — | 12 | bits | |
| Analog input capacitance | — | — | 30 | pF | |
| Conversion time[1] (P1$\varphi$ = 66 MHz, P0$\varphi$ = 33 MHz) | 1 | — | — | us | Sampling in 20 states |
| Permissible signal-source impedance | — | — | 1 | kΩ | |
| DNL | — | — | ± 3 | LSB | |
| INL | — | — | ± 4 | LSB | |
| Offset error | — | — | ± 5.5 | LSB | |
| Full-scale error | — | — | ± 5.5 | LSB | |
| Absolute accuracy | — | — | ± 7 | LSB | |

Note:    The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds
during A/D conversion, values may not fall within the above ranges.

Note 1.  The conversion time includes the sampling time and the comparison time ($t_{SPL}$ + $t_{SAM}$).
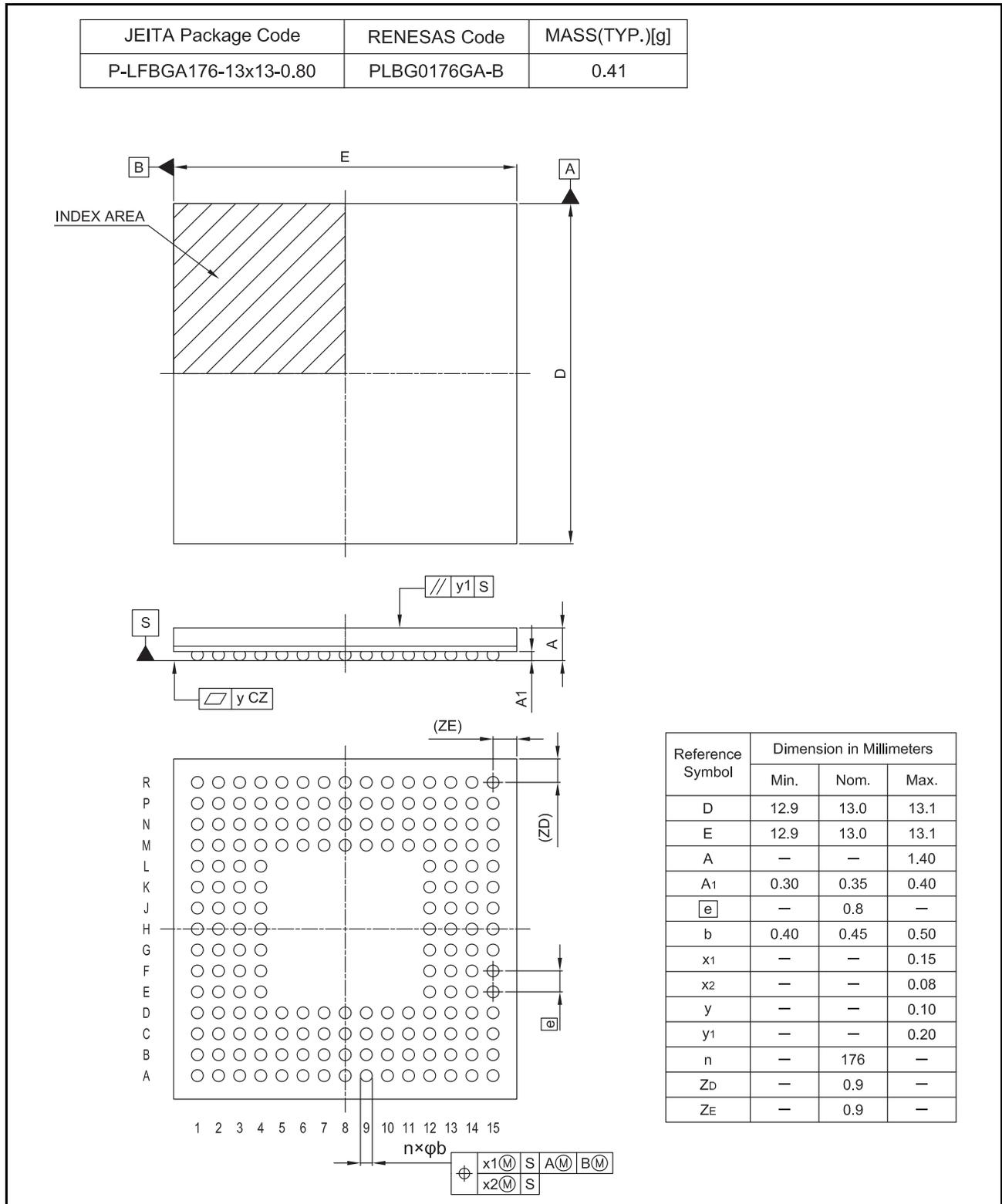
# 4.    Package Dimensions

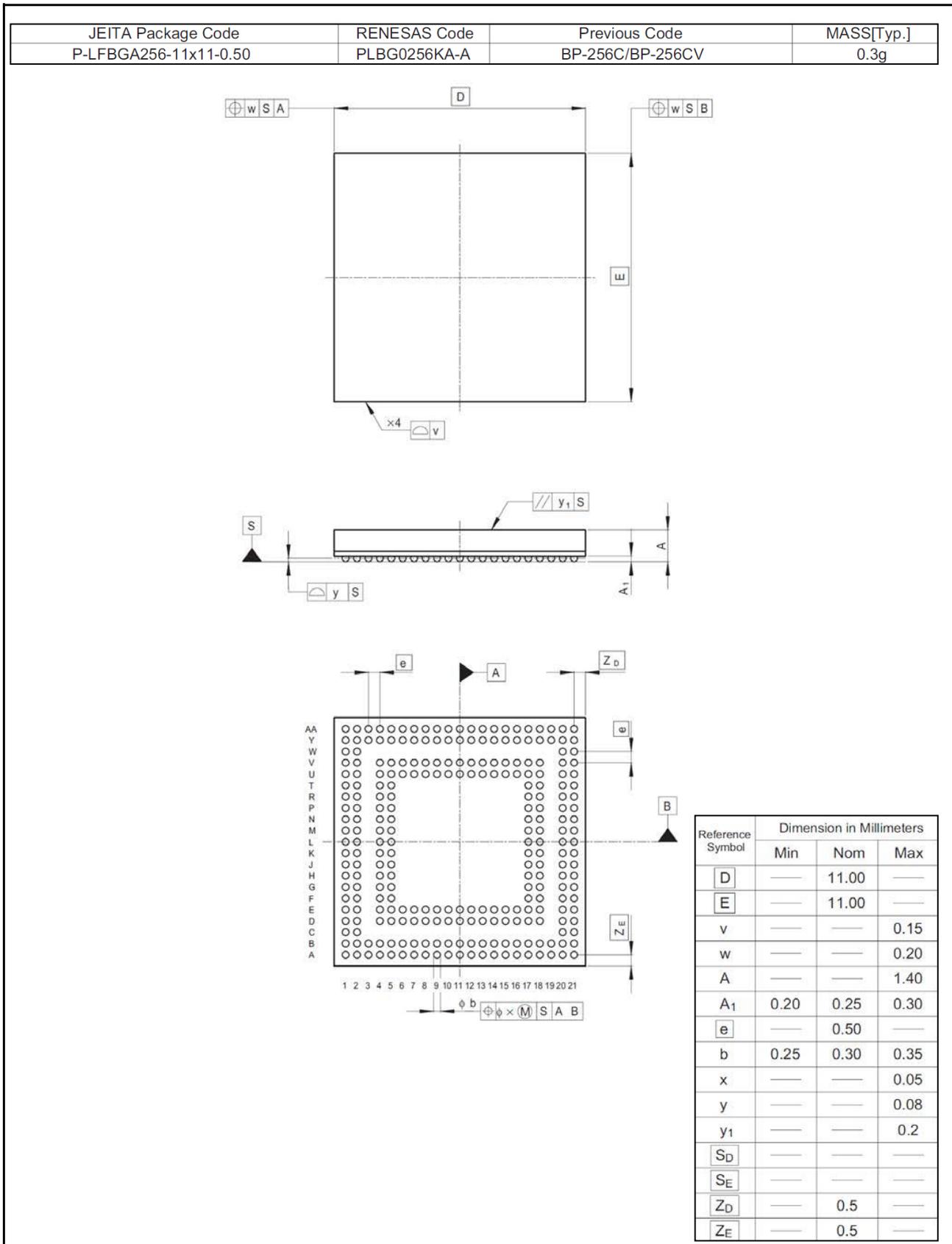| JEITA Package Code | RENESAS Code | MASS(TYP.)[g] |
|---|---|---|
| P-LFBGA176-13x13-0.80 | PLBG0176GA-B | 0.41 |

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| D | 12.9 | 13.0 | 13.1 |
| E | 12.9 | 13.0 | 13.1 |
| A | — | — | 1.40 |
| A1 | 0.30 | 0.35 | 0.40 |
| e | — | 0.8 | — |
| b | 0.40 | 0.45 | 0.50 |
| x1 | — | — | 0.15 |
| x2 | — | — | 0.08 |
| y | — | — | 0.10 |
| y1 | — | — | 0.20 |
| n | — | 176 | — |
| ZD | — | 0.9 | — |
| ZE | — | 0.9 | — |

Figure 4.1    Dimensions of 176-Pin BGA Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA256-11x11-0.50 | PLBG0256KA-A | BP-256C/BP-256CV | 0.3g |



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | —— | 11.00 | —— |
| E | —— | 11.00 | —— |
| v | —— | —— | 0.15 |
| w | —— | —— | 0.20 |
| A | —— | —— | 1.40 |
| A₁ | 0.20 | 0.25 | 0.30 |
| e | —— | 0.50 | —— |
| b | 0.25 | 0.30 | 0.35 |
| x | —— | —— | 0.05 |
| y | —— | —— | 0.08 |
| y₁ | —— | —— | 0.2 |
| S_D | —— | —— | —— |
| S_E | —— | —— | —— |
| Z_D | —— | 0.5 | —— |
| Z_E | —— | 0.5 | —— |

Figure 4.2    Dimensions of 256-Pin BGA Package

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-FBGA272-17x17-0.80 | PRBG0272GA-A | - | 0.90 |



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| D | – | 17.00 | – |
| E | – | 17.00 | – |
| v | – | – | 0.15 |
| w | – | – | 0.30 |
| A | – | – | 1.90 |
| $A_1$ | 0.35 | 0.40 | 0.45 |
| e | – | 0.80 | – |
| b | 0.45 | 0.50 | 0.55 |
| x | – | – | 0.08 |
| y | – | – | 0.10 |
| $y_1$ | – | – | 0.20 |
| $S_D$ | – | 0.40 | – |
| $S_E$ | – | 0.40 | – |
| $Z_D$ | – | 0.90 | – |
| $Z_E$ | – | 0.90 | – |
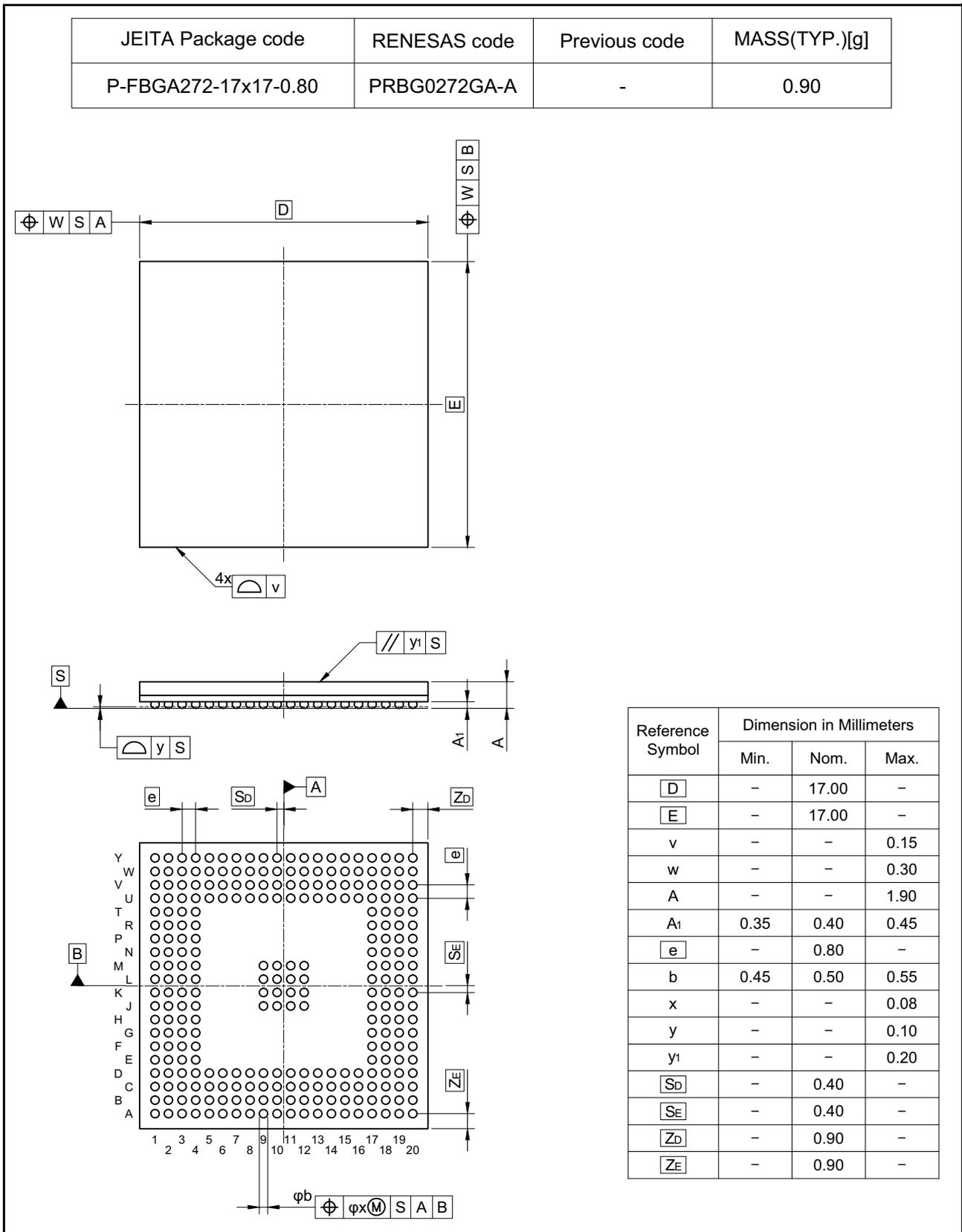
Figure 4.3    Dimensions of 272-Pin BGA Package

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P−FBGA324−19x19−0.80 | PRBG0324GA−A | − | 1.2 |

Unit:mm
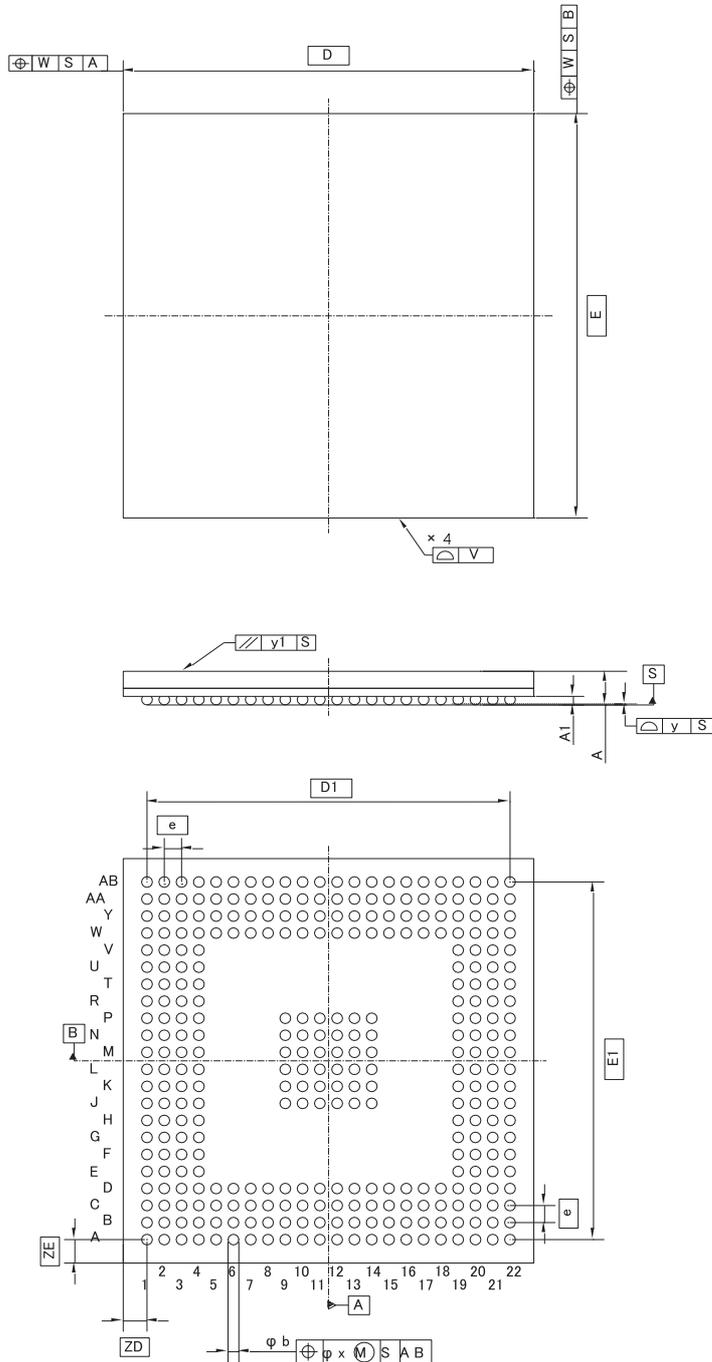
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Mon | Max |
| D | — | 19.00 | — |
| D1 | — | 16.80 | — |
| E | — | 19.00 | — |
| E1 | — | 16.80 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| e | — | 0.80 | — |
| A | — | 1.76 | 2.10 |
| A1 | 0.35 | 0.40 | 0.45 |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| y1 | — | — | 0.20 |
| ZD | — | 1.10 | — |
| ZE | — | 1.10 | — |

Figure 4.4    Dimensions of 324-Pin BGA Package

| REVISION HISTORY | | RZ/A2M Group Datasheet | |
|---|---|---|---|

| | | Description | |
|---|---|---|---|
| Rev. | Date | Page | Summary |
| 1.00 | Dec. 25, 2024 | — | First edition, issued |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1.  Precaution against Electrostatic Discharge (ESD)

    A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2.  Processing at power-on

    The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3.  Input of signal during power-off state

    Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4.  Handling of unused pins

    Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5.  Clock signals

    After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6.  Voltage application waveform at input pin

    Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7.  Prohibition of access to reserved addresses

    Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8.  Differences between products

    Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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