

## Features

This LSI has following features.

### ■ CPU

- Arm® Cortex®-A55, single-core  
Max. operating frequency: 1.0 GHz

### ■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (128-Kbytes on-chip SRAM with ECC)
- External DDR memory interface [option]  
1-channel memory controller for DDR3L-1333 or DDR4-1600 with a 16-bit bus width
- SPI Multi I/O Bus Controller × 1 channel (4-bit Double data rate)
- Octa Memory Controller × 1 channel  
OctaFlash™ and OctaRAM™ are supported
- SD card host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

### ■ Video and Graphics

- Image Scaling Unit

### ■ Camera and display interfaces

- Video input interface  
MIPI CSI-2 × 1 channel
- Video display interface  
Digital parallel output × 1 channel

### ■ Various communication/storage/network interfaces

- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- Gigabit Ethernet controller × 2 channels
- CANFD interface × 2 channels
- I<sup>2</sup>C bus interface × 4 channels
- Serial communication interface (SCI) × 2 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial Peripheral Interface (RSPI) × 3 channels

### ■ Extended-function timers

- Multi-Function Timer Pulse Unit  
32-bit × 1 channel, 16-bit × 8 channels

### ■ Audio

- Serial sound interface × 4 channels

### ■ Analog/Digital converter (ADC) and sensor

- 12-bit A/D converter × 2 channels
- Thermal Sensor Unit × 1 channel

# 1. Overview

## 1.1 Outline of Specification

### 1.1.1 CPU Core

| Item                  | Description  |
|-----------------------|--|
| System CPU Cortex-A55 | [RZ/A3UL] <ul style="list-style-type: none"> <li>• Arm Cortex-A55 Single MPCore 1.0 GHz</li> <li>• L1 I-cache 32 Kbytes (Parity) / D-cache 32 Kbytes (ECC)</li> <li>• L2 cache 0 Kbyte</li> <li>• L3 cache 256 Kbytes (ECC)</li> <li>• Arm® NEON™ / FPU supported</li> <li>• Cryptographic Extension supported</li> <li>• Arm® v8.2-A architecture</li> </ul>  |
| Boot                  | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 6 boot modes               <ul style="list-style-type: none"> <li>Boot Mode 0: Booting from eSD</li> <li>Boot Mode 1: Booting from eMMC (1.8 V)</li> <li>Boot Mode 2: Booting from eMMC (3.3 V)</li> <li>Boot Mode 3: Booting from a serial flash memory (Single / Quad / Octa) connected to the SPI Multi I/O or Octa I/F bus space (1.8 V)</li> <li>Boot Mode 4: Booting from a serial flash memory (Single / Quad) connected to the SPI Multi I/O bus space (3.3 V)</li> <li>Boot Mode 5: Booting from SCIF download</li> </ul> </li> </ul> <p><i>Note:</i> Boot Mode 0, 1, 2 and 5 are not supported.</p> |
| Debug Interface       | [RZ/A3UL] <ul style="list-style-type: none"> <li>• Arm® CoreSight™ architecture</li> <li>• JTAG / SWD interface supported</li> <li>• ETF 16 Kbytes for program flow trace (each cluster)</li> <li>• JTAG Disable supported</li> </ul>  |

### 1.1.2 CPU Peripheral

| Item                                   | Description  |
|--|--|
| Clock Pulse Generator (CPG)            | [RZ/A3UL] <ul style="list-style-type: none"> <li>Generates the clocks from external clock (EXCLK 24 MHz). <ul style="list-style-type: none"> <li>Maximum Arm Cortex-A55 clock: 1.0 GHz</li> <li>Maximum DDR clock: 666 MHz (DDR3L-1333), 800 MHz (DDR4-1600)</li> <li>Maximum AXI-bus clock: 200 MHz</li> <li>Maximum APB-bus clock: 100 MHz</li> </ul> </li> <li>SSC (Spread Spectrum Clock) supported</li> </ul> |
| Direct Memory Access Controller (DMAC) | [RZ/A3UL] <ul style="list-style-type: none"> <li>2 modules, 16 channels per module</li> <li>Transfer request: On-chip peripheral request / auto request (software trigger)</li> <li>A specific DMA transfer interval can be specified to adjust the bus occupancy.</li> <li>LINK mode (DMA transfer under descriptor control) supported</li> <li>Transfer information can be automatically reloaded</li> </ul>     |
| Interrupt Controller                   | [RZ/A3UL] <ul style="list-style-type: none"> <li>Arm® CoreLink™ Generic Interrupt Controller (GIC-600) for Arm Cortex-A55</li> <li>External Interrupt pins (NMI, IRQ7 to IRQ0, TINT31-0)</li> <li>On-chip peripheral Interrupts: Priority level set for each module</li> </ul>   |
| General-purpose I/O (GPIO)             | [RZ/A3UL] <ul style="list-style-type: none"> <li>General-purpose I/O ports</li> </ul>  |
| Thermal Sensor Unit (TSU)              | [RZ/A3UL] <ul style="list-style-type: none"> <li>1 channel</li> </ul>  |

### 1.1.3 Internal Memory

| Item        | Description   |
|-------------|---|
| On-chip RAM | [RZ/A3UL] <ul style="list-style-type: none"> <li>RAM of 128 Kbytes (ECC)</li> </ul> |

### 1.1.4 External Memory Interface

| Item  | Description   |
|---|---|
| External Bus Controller for DDR3L / DDR4 SDRAM (DDR) [option] | [RZ/A3UL] <ul style="list-style-type: none"> <li>• Support DDR3L-1333 / DDR4-1600</li> <li>• Bus Width: 16-bit</li> <li>• In line ECC supported (Support error detection interrupt)</li> <li>• Memory Size: Up to 4 Gbytes</li> <li>• Auto Refresh supported</li> </ul>   |
| SPI Multi I/O Bus Controller                                  | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 1 channel (4-bit Double data rate)</li> <li>• 1 serial flash memory with multiple I/O bus sizes (single / quad) can be connected</li> <li>• External address space read mode (built-in read cache)</li> <li>• SPI operation mode</li> <li>• Maximum Clock Frequency:               <ul style="list-style-type: none"> <li>– 50 MHz (Quad-SPI DDR)</li> <li>– 66 MHz (Quad-SPI SDR)</li> </ul> </li> </ul>  |
| Octa Memory Controller  | [RZ/A3UL] <ul style="list-style-type: none"> <li>• Macronix Serial Multi I/O (MXSMIO®) Octa Peripheral Interface (OPI) for high-end consumer applications is supported.</li> <li>• One each of an OctaFlash device and an OctaRAM device compliant with the OPI specifications are connectable.</li> <li>• A chip select signal is assigned to each memory device (OM_CS0#: OctaFlash; OM_CS1#: OctaRAM).</li> <li>• Supported device interfaces               <ul style="list-style-type: none"> <li>– SPI: Serial peripheral interface (OctaFlash, SPI mode)</li> <li>– SOPI: Single Octa I/O (8 bits) (OctaFlash, single data rate)</li> <li>– DOPI: Double Octa I/O (8 bits) (OctaFlash and OctaRAM, double data rate)</li> </ul> </li> </ul> |
| SD Card Host Interface / Multimedia Card Interface (SD/MMC)   | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 2 channels</li> <li>• Channel 0 supports SDHI / e-MMC (boot supported)</li> <li>• Channel 1 supports SDHI</li> <li>• SD memory I/O card interface (1-bit / 4-bit SD bus)</li> <li>• SD, SDHC and SDXC SD memory card access supported</li> <li>• Compliant with SD 3.0</li> <li>• Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported</li> <li>• Error check function: CRC7 (Command), CRC16 (Data)</li> <li>• Card detection function, write protect supported</li> <li>• MMC interface (1-bit / 4-bit / 8-bit MMC bus)</li> <li>• e-MMC device access supported</li> <li>• Compliant with eMMC 4.51</li> <li>• High-speed, HS200 transfer modes supported</li> </ul>           |

### 1.1.5 Video Processing Unit

| Item                     | Description  |
|--------------------------|--|
| Image Scaling Unit (ISU) | [RZ/A3UL] <ul style="list-style-type: none"> <li>• Scaling down function with bilinear interpolation</li> <li>• Input image Size (max): 5M (2800 × 2047)</li> <li>• Output image Size (max): Full HD (1920 × 1080)</li> <li>• Support Color format Conversion</li> <li>• RGB / ARGB / YcbCr422 / YcbCr420 / RAW (Grayscale)</li> </ul> |

## 1.1.6 Camera Interfaces

| Item                            | Description   |
|---------------------------------|---|
| MIPI CSI-2 Interface            | <p>[RZ/A3UL]</p> <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• The number of Lane: 1-/2-/4-lane</li> <li>• Support 5MP, 30 fps (RAW12)</li> <li>• Maximum Bandwidth: 1.5 Gbps per lane</li> <li>• Select 1 VC from 4 VC (virtual channel) supported</li> <li>• Support Input Image Data Formats: <ul style="list-style-type: none"> <li>– YUV420 8-bit / 10-bit</li> <li>– Legacy YUV420 8-bit</li> <li>– YUV420 8-bit / 10-bit (Chroma Shifted Pixel Sampling)</li> <li>– YUV422 8-bit / 10-bit</li> <li>– RGB444 / RGB555 / RGB565 / RGB666 / RGB888</li> <li>– RAW6 / RAW7 / RAW8 / RAW10 / RAW12 / RAW14 / RAW16 / RAW20</li> </ul> </li> <li>• Generic short packet data type 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8</li> <li>• Generic long packet data type 1 / 2 / 3 / 4</li> <li>• User Defined 8-bit data type 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8</li> </ul>  |
| MIPI CSI-2 to AXI Bridge Module | <p>[RZ/A3UL]</p> <ul style="list-style-type: none"> <li>• 1 channel (MIPI CSI-2 Input)</li> <li>• Support Image Processing: <ul style="list-style-type: none"> <li>– Clipping</li> <li>– Frame Sampling</li> <li>– LUT</li> <li>– Color format conversion</li> <li>– Color space conversion</li> <li>– Demosaicing</li> <li>– Linear Matirix</li> <li>– Statistics</li> </ul> </li> <li>• Support Color Formats for Image Processing: <ul style="list-style-type: none"> <li>– YUV422 8-/10-bit</li> <li>– RGB565 / RGB666 / RGB888</li> <li>– RAW8 / 10 / 12 / 14 / 16 (Clipping and Frame Sampling only)</li> </ul> </li> <li>• Support Output Data Formats: <ul style="list-style-type: none"> <li>– YCbCr422 8-bit (Interleave/Semi planar, Progressive)</li> <li>– Y-Only</li> <li>– RGB888 / ARGB8888</li> <li>– RAW8 / 10 / 12 / 14 / 16 (without Image Processing)</li> <li>– MIPI CSI-2 V2.1 Recommended Memory storage data (without Image Processing)</li> </ul> </li> </ul> |

### 1.1.7 Display Interface

| Item                      | Description   |
|---------------------------|---|
| LCD Controller            | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 1 channel (Parallel output)</li> <li>• 2 planes blending (can blend 2 different size images)</li> <li>• Support Image Processing:               <ul style="list-style-type: none"> <li>– Dither processing (RGB666)</li> <li>– Clipping</li> <li>– RGB Gamma Correction LUT</li> </ul> </li> <li>• Support Input Data Format:               <ul style="list-style-type: none"> <li>– RGB565 / RGB666 / RGB888</li> <li>– ARGB1555 / ARGB4444 / ARGB8888</li> <li>– YcbCr444 8-bit / YcbCr422 8-bit / YcbCr420 8-bit</li> </ul> </li> </ul> |
| Parallel Output Interface | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Support WXGA (1280 × 800), 60 fps</li> <li>• Support Output Data Format:               <ul style="list-style-type: none"> <li>– RGB666 / RGB888</li> </ul> </li> <li>• CLK / HD / VD timing signal supported</li> </ul>   |

### 1.1.8 Sound Interface

| Item                         | Description   |
|------------------------------|---|
| Serial Sound Interface (SSI) | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 4 channels bidirectional serial transfer</li> <li>• 2 external clock sources available</li> <li>• Duplex communication (channel 0, 1, and 3)</li> <li>• Support of I2S / Monaural / TDM audio formats</li> <li>• Support of master and slave functions</li> <li>• Generation of programmable word clock and bit clock</li> <li>• Multi-channel formats</li> <li>• Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats</li> <li>• Support of 32-stage FIFO for transmission and reception</li> <li>• Support of LR-clock continue function in which the LR-clock signal is not stopped</li> </ul> |

## 1.1.9 Storage and Network

| Item                                | Description  |
|-------------------------------------|--|
| USB2.0 Host / Function<br>(USB)     | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 2 channels (ch0: Host-Function ch1: Host only)</li> <li>• Compliance with USB2.0</li> <li>• Supports On-The-Go (OTG) Function</li> <li>• Supports Battery Charging Function</li> <li>• Internal dedicated DMA</li> </ul>  |
| Gigabit Ethernet Interface<br>(GbE) | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 2 channels</li> <li>• Supports transfer at 1000 Mbps and 100 Mbps, 10 Mbps</li> <li>• Supports filtering of Ethernet frames</li> <li>• Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface)</li> <li>• Supports interface conforming to IEEE802.3 PHYMII (Media Independent Interface)</li> </ul> |
| CANFD Interface<br>(RS-CANFD)       | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 2 channels</li> <li>• ISO 11898-1 (2003) compliant</li> <li>• CAN-FD ISO 11898-1 (CD2014) compliant</li> <li>• Message buffer               <ul style="list-style-type: none"> <li>– Up to 64 × 2-channel receive message buffer: Shared among all channels</li> <li>– 16 transmit message buffers per channel</li> </ul> </li> </ul>           |

### 1.1.10 Timer

| Item                                      | Description   |
|---|---|
| Multi-function Timer Pulse Unit 3 (MTU3a) | <p>[RZ/A3UL]</p> <ul style="list-style-type: none"> <li>• 9 channels (16 bits × 8 channels, 32 bits × 1 channel)</li> <li>• Module clock frequency (P0φ): 100 MHz</li> <li>• Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs</li> <li>• 14 types of count clocks selectable</li> <li>• Input capture function</li> <li>• 39 outputs compare and input capture registers</li> <li>• Counter clear operation (Simultaneous counter clearing by Compare match or Input capture is available)</li> <li>• Simultaneous writing to multiple timer counters (TCNT)</li> <li>• Synchronous input/output of each register due to synchronous operation of the counter</li> <li>• Buffered operation</li> <li>• Cascade-connected operation</li> <li>• 43 types of interrupt sources</li> <li>• Automatic transfer of register data</li> <li>• Pulse output modes <ul style="list-style-type: none"> <li>Toggle, PWM, complementary PWM, and reset-synchronized PWM modes</li> </ul> </li> <li>• Synchronization of multiple counters</li> <li>• Phase counting mode <ul style="list-style-type: none"> <li>– 16-bit mode (channel 1 and 2)</li> <li>– 32-bit mode (channel 1 and 2)</li> </ul> </li> <li>• Counter function of dead time compensation</li> <li>• Digital filter functions for the input capture and external count clock pin</li> </ul> |
| Port Output Enable 3 (POE3)               | <p>[RZ/A3UL]</p> <ul style="list-style-type: none"> <li>• Control of the high-impedance state of the MTU3a waveform output pins</li> <li>• Activation with four input pins</li> <li>• Activation on detection of short-circuited outputs</li> <li>• Activation by register write</li> <li>• Additional programming of output control target pins is possible.</li> </ul>  |
| Watchdog Timer (WDT)                      | <p>[RZ/A3UL]</p> <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• A counter overflow can reset the LSI</li> <li>• CPU parity error can reset the LSI</li> </ul>  |
| General Timer (GTM)                       | <p>[RZ/A3UL]</p> <ul style="list-style-type: none"> <li>• 32 bits × 3 channels</li> <li>• Two operating modes <ul style="list-style-type: none"> <li>– Interval timer mode</li> <li>– Free-running comparison mode</li> </ul> </li> </ul>   |

### 1.1.11 Peripheral Module

| Item   | Description  |
|--|--|
| I2C Bus Interface<br>(I2C)                             | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 4 channels (ch0,1 = Dedicated pin, ch2,3 = Multiplexed pin)</li> <li>• Master mode and slave mode supported</li> <li>• Support for 7-bit and 10-bit slave address formats</li> <li>• Support for multi-master operation</li> <li>• Timeout detection</li> </ul>   |
| Serial Communication Interface<br>with FIFO<br>(SCIFA) | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 5 channels</li> <li>• Clock synchronous mode or asynchronous mode selectable</li> <li>• Simultaneous transmission and reception (full-duplex communication) supported</li> <li>• Dedicated baud rate generator</li> <li>• Separate 16-byte FIFO registers for transmission and reception</li> <li>• Modem control function (channel 0, 1, and 2 in asynchronous mode)</li> </ul>  |
| Serial Communication Interface<br>(SCIg)               | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 2 channels</li> <li>• Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable</li> <li>• Simultaneous transmission and reception (full-duplex communication) supported</li> <li>• Dedicated baud rate generator</li> <li>• LSB first / MSB first selectable</li> <li>• Modem control function</li> <li>• Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)</li> </ul> |
| Renesas Serial Peripheral<br>Interface (RSPI)          | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 3 channels</li> <li>• SPI operation</li> <li>• Master mode and slave mode supported</li> <li>• Programmable bit length, clock polarity, clock phase can be selected</li> <li>• Consecutive transfers</li> <li>• LSB first / MSB first selectable</li> </ul>   |

### 1.1.12 Analog

| Item                   | Description   |
|------------------------|---|
| A/D Converter<br>(ADC) | [RZ/A3UL] <ul style="list-style-type: none"> <li>• 2 channels</li> <li>• Resolution: 12-bit</li> <li>• Input Range: 0 V ~ 1.8 V</li> <li>• Conversion Time: 1 <math>\mu</math>s</li> <li>• Operation Mode: Single Scan / Continuous Scan</li> <li>• Condition for A/D conversion start <ul style="list-style-type: none"> <li>– Software trigger</li> <li>– Asynchronous trigger: External trigger supported</li> <li>– Synchronous trigger: MTU timer</li> </ul> </li> </ul> |

### 1.1.13 Others

| Item          | Description  |
|---------------|--|
| Boundary Scan | [RZ/A3UL] <ul style="list-style-type: none"> <li>Boundary scan based on IEEE 1149.1 via JTAG interface is supported.</li> </ul> <p>Note that some module pins are not available on this boundary scan.</p> |

### 1.1.14 Power Supply Voltage

| Item                 | Description  |
|----------------------|--|
| Power supply voltage | [RZ/A3UL] <ul style="list-style-type: none"> <li>V<sub>DD</sub>, PLLn_DV<sub>DD11</sub> (n = 23, 5): 1.05 to 1.15 V</li> <li>DDR_V<sub>DDQ</sub>: 1.14 to 1.26 V (DDR4) / 1.283 to 1.45 V (DDR3L)</li> <li>V<sub>DD18</sub>, ADC_AV<sub>DD18</sub>, PLLn_AV<sub>DD18</sub> (n = 1, 23, 4, 5, 6): 1.62 to 1.98 V</li> <li>OTP_V<sub>DD18</sub>, USB_V<sub>DD18</sub>, CSI_V<sub>DD18</sub>: 1.65 to 1.95 V</li> <li>PV<sub>DD</sub>: 2.97 to 3.63 V</li> <li>USB_V<sub>DD33</sub>: 3.00 to 3.60 V</li> <li>SDn_PV<sub>DD</sub> (n = 0, 1), SPI_PV<sub>DD</sub>: 2.97 to 3.63 V / 1.70 to 1.95 V</li> <li>PV<sub>DD182533</sub>: 2.97 to 3.63 V / 2.25 to 2.75 V / 1.62 to 1.98 V</li> </ul> |

### 1.1.15 Temperature Range

| Item              | Description   |
|-------------------|---|
| Temperature range | [RZ/A3UL] <ul style="list-style-type: none"> <li>T<sub>a</sub>: -40°C to +85°C*1</li> <li>T<sub>j</sub>: -40°C to +125°C</li> </ul> |

Note 1. If wider temp is required than this range, use case has to be investigated.

### 1.1.16 Quality level

| Item          | Description  |
|---------------|--|
| Quality level | [RZ/A3UL] <ul style="list-style-type: none"> <li>Industrial usage, etc.</li> </ul> |

### 1.1.17 Package

| Item    | Description   |
|---------|---|
| Package | [RZ/A3UL] <ul style="list-style-type: none"> <li>361-pin LFBGA, 13-mm square, 0.5-mm pitch</li> </ul> |

## 1.2 Block Diagram

The LSI internal bus of this LSI consists of the ACPU bus, MCPU bus, and system bus. **Figure 1.1** shows the configuration of the buses.

### **ACPU bus:**

A bus connected to Cortex-A55, DDR memory controllers, image processing units, and Storage and Network

### **MCPU bus:**

A bus connected to serial interface units

### **System bus:**

A bus connected to the control registers of each unit

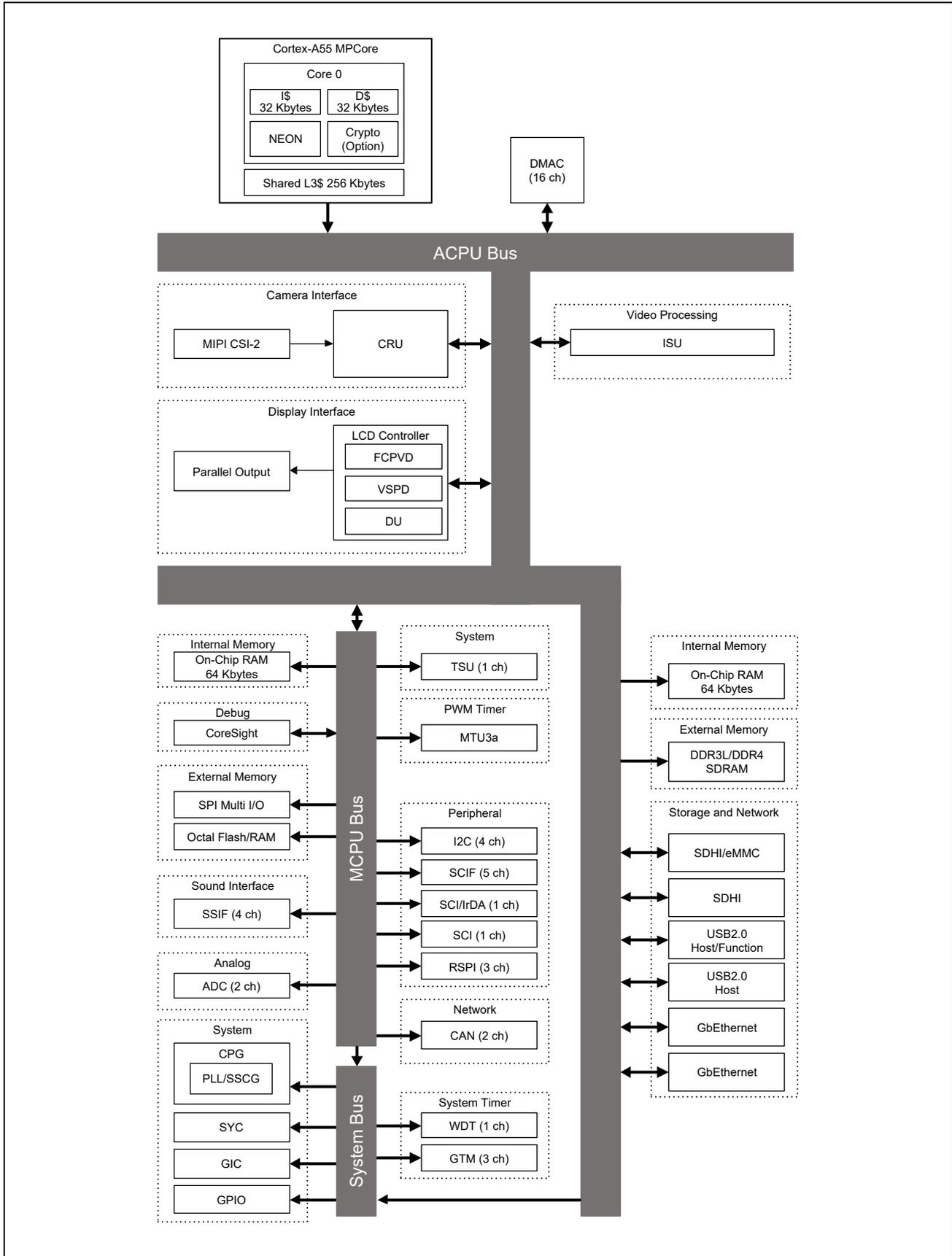


Figure 1.1 Configuration of LSI Internal Bus

## 1.3 Product Lineup

Table 1.1 Product Lineup

| Group   | Package   | Part Number     | DDR SDRAM Interface | Security      |
|---------|-----------|-----------------|---------------------|---------------|
| RZ/A3UL | 13 mm BGA | R9A07G063U02GBG | Available           | Not supported |
|         |           | R9A07G063U01GBG | Not supported       |               |

## 2. Pin

### 2.1 Pin Assignment

Refer to attached excel file for the “ball view” about pin assignment of this LSI.

(Please double-click the icon on the right side)



### 2.2 External Pins and Multiplexed Functional Pins

Refer to attached excel file for the “pn function list” about information of external pins and multiplexed functional pins of this LSI.

(Please double-click the icon on the right side)



## 3. Electrical Characteristics

### 3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

| Item  | Symbol                                      | Value            | Unit  |    |
|---|---|------------------|---|----|
| Power supply voltage (3.3 V)                          | PV <sub>DD</sub>                            | -0.5 to +3.8     | V   |    |
|   | USB_V <sub>DD33</sub>                       |                  |   |    |
| Power supply voltage (1.8-V/3.3-V switchable)         | SD0_PV <sub>DD</sub>                        | -0.5 to +3.8     | V   |    |
|   | SD1_PV <sub>DD</sub>                        |                  |   |    |
|   | SPI_PV <sub>DD</sub>                        |                  |   |    |
| Power supply voltage (1.8-V/ 2.5-V/ 3.3-V switchable) | PV <sub>DD182533_0/1</sub>                  | -0.5 to +3.8     | V   |    |
| Power supply voltage (1.8 V)                          | V <sub>DD18</sub>                           | -0.5 to +2.5     | V   |    |
|   | PLL1_AV <sub>DD18</sub>                     |                  |   |    |
|   | PLL23_AV <sub>DD18</sub>                    |                  |   |    |
|   | PLL4_AV <sub>DD18</sub>                     |                  |   |    |
|   | PLL5_AV <sub>DD18</sub>                     |                  |   |    |
|   | PLL6_AV <sub>DD18</sub>                     |                  |   |    |
|   | CSI_V <sub>DD18</sub>                       |                  |   |    |
|   | USB_V <sub>DD18</sub>                       |                  |   |    |
|   | ADC_AV <sub>DD18</sub>                      |                  |   |    |
|   | OTP_V <sub>DD18</sub>                       |                  |   |    |
| DDR power supply voltage (DDR4/ DDR3L switchable)     | DDR_V <sub>DDQ</sub>                        | -0.5 to +2.5     | V   |    |
| Power supply voltage (1.1-V)                          | V <sub>DD</sub>                             | -0.5 to +1.5     | V   |    |
|   | PLL23_DV <sub>DD11</sub>                    |                  |   |    |
|   | PLL5_DV <sub>DD11</sub>                     |                  |   |    |
| Input voltage   | 3.3-V I/O input pins                        | —                | -0.3 to 3.3-V power supply (PV <sub>DD</sub> , USB_V <sub>DD33</sub> ) + 0.3  | V  |
|   | 1.8-V/3.3-V switchable I/O input pins       | —                | -0.3 to 1.8-V/3.3-V switchable power supply (SD0_PV <sub>DD</sub> , SD1_PV <sub>DD</sub> , SPI_PV <sub>DD</sub> ) + 0.3 | V  |
|   | 1.8-V/2.5-V/3.3-V switchable I/O input pins | —                | -0.3 to 1.8-V/2.5-V/3.3-V switchable power supply (PV <sub>DD182533_0,1</sub> ) + 0.3                                   | V  |
|   | 1.8-V I/O input pins                        | —                | -0.3 to 1.8-V power supply (V <sub>DD18</sub> , CSI_V <sub>DD18</sub> , USB_V <sub>DD18</sub> ) + 0.3                   | V  |
| Operating temperature                                 | Ambient temperature                         | T <sub>a</sub>   | -40°C to +85°C*1  | °C |
|   | Junction temperature                        | T <sub>j</sub>   | -40°C to +125°C   | °C |
| Storage temperature                                   | Ambient temperature                         | T <sub>stg</sub> | -40°C to +150°C   | °C |

Note 1. If wider temp is required than this range, use case has to be investigated.

## 3.2 Power Supply

Table 3.2 Power Supply

| Item                         | Symbol                                     | Min.  | Typ. | Max. | Unit | Remarks                |
|------------------------------|--|-------|------|------|------|------------------------|
| Power supply voltage (3.3 V) | PV <sub>DD</sub>                           | 2.97  | 3.30 | 3.63 | V    | —                      |
| Power supply voltage (1.8 V) | V <sub>DD18</sub> , ADC_AV <sub>DD18</sub> | 1.62  | 1.80 | 1.98 | V    | —                      |
|                              | OTP_V <sub>DD18</sub>                      | 1.65  | 1.80 | 1.95 | V    | —                      |
| Power supply voltage (1.1 V) | V <sub>DD</sub>                            | 1.05  | 1.10 | 1.15 | V    | —                      |
| Power supply voltage (USB)   | USB_V <sub>DD33</sub>                      | 3.00  | 3.30 | 3.60 | V    | —                      |
|                              | USB_V <sub>DD18</sub>                      | 1.65  | 1.80 | 1.95 | V    | —                      |
| Power supply voltage (SD)    | SD0_PV <sub>DD</sub> ,                     | 2.97  | 3.30 | 3.63 | V    | When 3.3 V is supplied |
|                              | SD1_PV <sub>DD</sub>                       | 1.70  | 1.80 | 1.95 | V    | When 1.8 V is supplied |
| Power supply voltage (SPI)   | SPI_PV <sub>DD</sub>                       | 2.97  | 3.30 | 3.63 | V    | When 3.3 V is supplied |
|                              |  | 1.70  | 1.80 | 1.95 | V    | When 1.8 V is supplied |
| Power supply voltage (Ether) | PV <sub>DD182533_0/1</sub>                 | 2.97  | 3.30 | 3.63 | V    | When 3.3 V is supplied |
|                              |  | 2.25  | 2.50 | 2.75 | V    | When 2.5 V is supplied |
|                              |  | 1.62  | 1.80 | 1.98 | V    | When 1.8 V is supplied |
| Power supply voltage (CSI)   | CSI_V <sub>DD18</sub>                      | 1.65  | 1.80 | 1.95 | V    | —                      |
| Power supply voltage (DDR)   | DDR_V <sub>DDQ</sub>                       | 1.14  | 1.20 | 1.26 | V    | When using DDR4        |
|                              |  | 1.283 | 1.35 | 1.45 | V    | When using DDR3L       |
| Power supply voltage (PLL)   | PLL1_AV <sub>DD18</sub> ,                  | 1.62  | 1.80 | 1.98 | V    | —                      |
|                              | PLL23_AV <sub>DD18</sub> ,                 |       |      |      |      |                        |
|                              | PLL4_AV <sub>DD18</sub> ,                  |       |      |      |      |                        |
|                              | PLL5_AV <sub>DD18</sub> ,                  |       |      |      |      |                        |
|                              | PLL6_AV <sub>DD18</sub>                    |       |      |      |      |                        |
|                              | PLL23_DV <sub>DD11</sub> ,                 | 1.05  | 1.10 | 1.15 | V    | —                      |
|                              | PLL5_DV <sub>DD11</sub>                    |       |      |      |      |                        |

### 3.3 Power-On/Power-Off Sequence

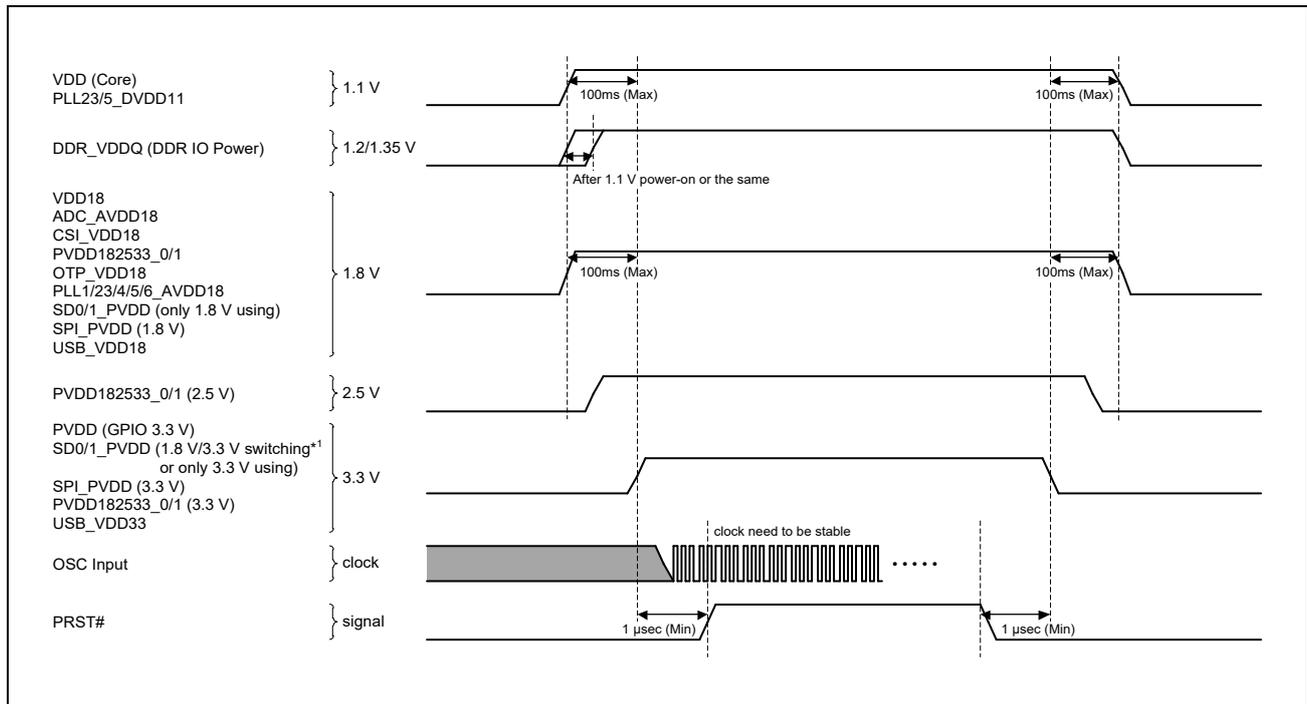


Figure 3.1 Power-On/Power-Off Sequence

#### NOTES

- Turn on 3.3 V after 1.1 V/1.8 V.
 

*Note 1.* About SD0/1\_PV<sub>DD</sub>, especially in the case of switching between 1.8 V and 3.3 V at same power rail, 1.8-V power-on/off timing can also follow 3.3-V power rail sequence as shown in the **Figure 3.1**.
- Turn on the DDR IO power supply at the same time as or after the 1.1-V power supply.
- From first power rising start to last power rising end must be within 100 ms.
- The power-off sequence is the reverse of the power-on sequence (PRST# → Low ⇒ 3.3 V = OFF ⇒ Other = OFF)
- PRST# should be changed from Low to High after the 3.3-V power supply is turned on, after 1 μsec, and after the input clock from the oscillator stabilizes.
- Refer to SD0/1\_PV<sub>DD</sub> when connecting eMMC.

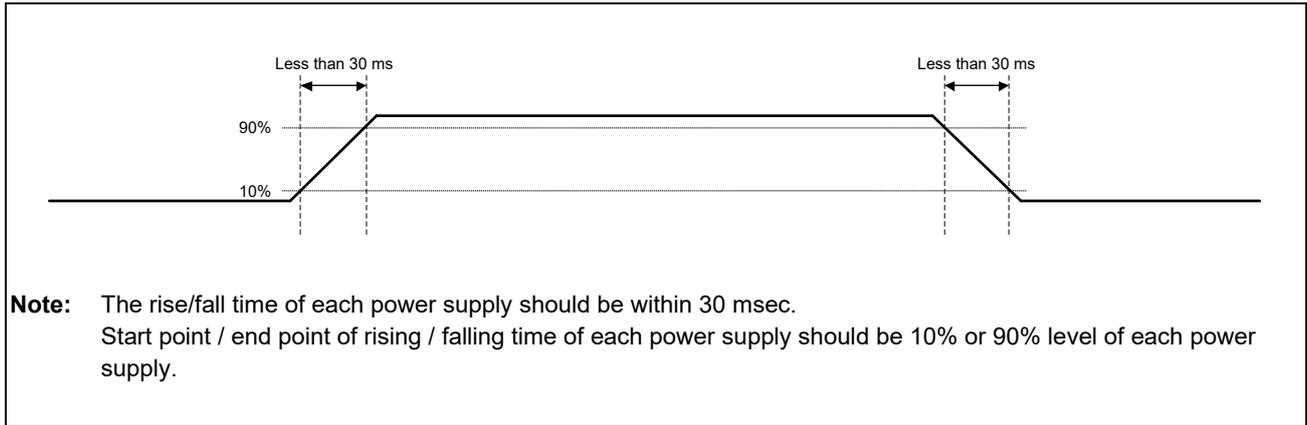


Figure 3.2 Power Up Time/Power Down Time (1)

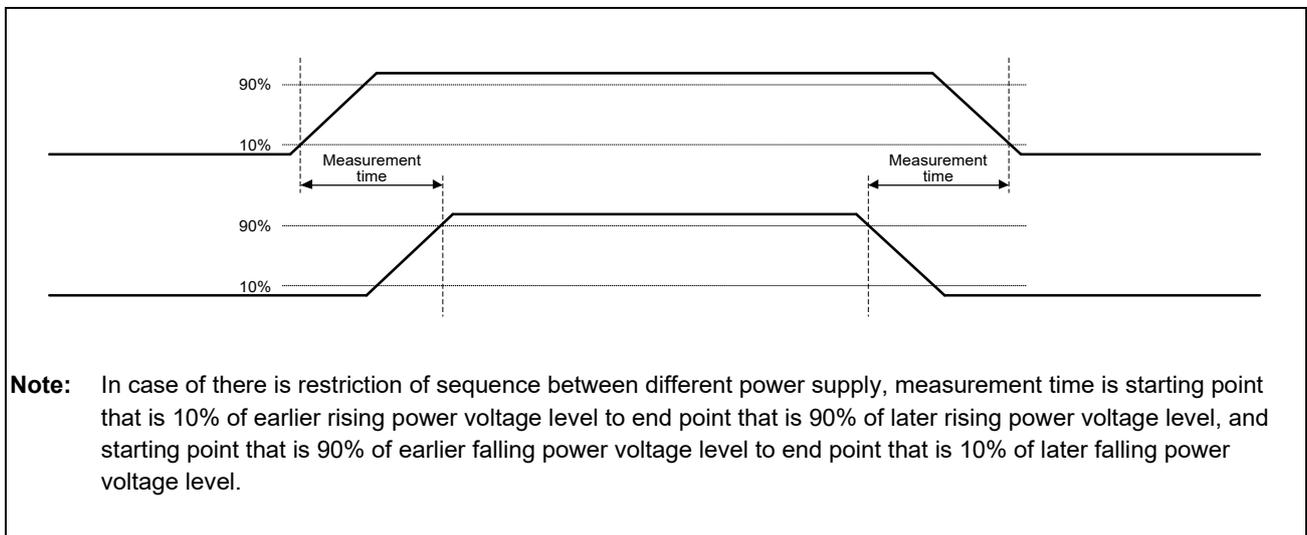


Figure 3.3 Power Up Time/Power Down Time (2)

### 3.4 DC Characteristics

Table 3.3 DC Characteristics (1) [3.3-V I/O]

| Item                                 | Symbol               | Min.            | Typ. | Max.            | Unit     | Remarks   |
|--------------------------------------|----------------------|-----------------|------|-----------------|----------|---|
| High-level input voltage             | $V_{IH}$             | 2               | —    | $PV_{DD} + 0.3$ | V        |   |
| Low-level input voltage              | $V_{IL}$             | -0.3            | —    | 0.8             | V        |   |
| Hysteresis threshold ↑               | $V_{T+}$             | 0.9             | —    | 2.1             | V        |   |
| Hysteresis threshold ↓               | $V_{T-}$             | 0.7             | —    | 1.9             | V        |   |
| Input hysteresis voltage             | $V_{HYS}$            | 0.306           | —    | 0.420           | V        |   |
| Output logic high voltage            | $V_{OH}$             | $PV_{DD} - 0.4$ | —    | $PV_{DD}$       | V        |   |
|                                      | ( $I_{OH} = -2mA$ )  |                 |      |                 |          |   |
|                                      | ( $I_{OH} = -4mA$ )  |                 |      |                 |          |   |
|                                      | ( $I_{OH} = -8mA$ )  |                 |      |                 |          |   |
|                                      | ( $I_{OH} = -12mA$ ) |                 |      |                 |          |   |
| Output logic low voltage             | $V_{OL}$             | 0               | —    | 0.4             | V        |   |
|                                      | ( $I_{OL} = 2mA$ )   |                 |      |                 |          |   |
|                                      | ( $I_{OL} = 4mA$ )   |                 |      |                 |          |   |
|                                      | ( $I_{OL} = 8mA$ )   |                 |      |                 |          |   |
|                                      | ( $I_{OL} = 12mA$ )  |                 |      |                 |          |   |
| Weak pull-up resistor (input mode)   | $R_{UP}$             | 7K              | —    | 100K            | $\Omega$ |   |
| Weak pull-down resistor (input mode) | $R_{DN}$             | 7K              | —    | 100K            | $\Omega$ |   |
| Input leakage current                | $I_{LI}$             | —               | —    | 5               | $\mu A$  | $0V \leq V_{in} \leq PV_{DD}$<br>In case of 3state<br>buffer, the leak<br>current when<br>output mode OFF |

**Note:**  $V_{in}$  means input voltage of external input pin.

**Note:** Schmitt can be used at only RIIC mode.

Table 3.4 DC Characteristics (2) [1.8-V I/O]

| Item                      | Symbol               | Min.                   | Typ. | Max.                   | Unit | Remarks |
|---------------------------|----------------------|------------------------|------|------------------------|------|---------|
| High-level input voltage  | $V_{IH}$             | $0.65 \times V_{DD18}$ | —    | $V_{DD18} + 0.3$       | V    |         |
| Low-level input voltage   | $V_{IL}$             | -0.3                   | —    | $0.35 \times V_{DD18}$ | V    |         |
| Output logic high voltage | $V_{OH}$             | $V_{DD18} - 0.4$       | —    | $V_{DD18}$             | V    |         |
|                           | ( $I_{OH} = -2mA$ )  |                        |      |                        |      |         |
|                           | ( $I_{OH} = -4mA$ )  |                        |      |                        |      |         |
|                           | ( $I_{OH} = -8mA$ )  |                        |      |                        |      |         |
|                           | ( $I_{OH} = -12mA$ ) |                        |      |                        |      |         |
| Output logic low voltage  | $V_{OL}$             | 0                      | —    | 0.4                    | V    |         |
|                           | ( $I_{OL} = 2mA$ )   |                        |      |                        |      |         |
|                           | ( $I_{OL} = 4mA$ )   |                        |      |                        |      |         |
|                           | ( $I_{OL} = 8mA$ )   |                        |      |                        |      |         |
|                           | ( $I_{OL} = 12mA$ )  |                        |      |                        |      |         |

Table 3.5 DC Characteristics (3) [3.3-V Input]

| Item                     | Symbol    | Min.  | Typ. | Max.            | Unit | Remarks |
|--------------------------|-----------|-------|------|-----------------|------|---------|
| High-level input voltage | $V_{IH}$  | 2.3   | —    | $PV_{DD} + 0.3$ | V    |         |
| Low-level input voltage  | $V_{IL}$  | -0.3  | —    | 0.8             | V    |         |
| Hysteresis threshold ↑   | $V_{T+}$  | 0.9   | —    | 2.1             | V    |         |
| Hysteresis threshold ↓   | $V_{T-}$  | 0.7   | —    | 1.9             | V    |         |
| Input hysteresis voltage | $V_{HYS}$ | 0.306 | —    | 0.420           | V    |         |

Table 3.6 DC Characteristics (4) [1.8-V Input]

| Item                     | Symbol   | Min.                   | Typ. | Max.                   | Unit | Remarks |
|--------------------------|----------|------------------------|------|------------------------|------|---------|
| High-level input voltage | $V_{IH}$ | $0.65 \times V_{DD18}$ | —    | $V_{DD18} + 0.3$       | V    |         |
| Low-level input voltage  | $V_{IL}$ | -0.3                   | —    | $0.35 \times V_{DD18}$ | V    |         |

Table 3.7 DC Characteristics (5) [RGMII/MII]

| Item                                     | Symbol             | Min.                           | Typ. | Max.                           | Unit | Remarks         |
|--|--------------------|--------------------------------|------|--------------------------------|------|-----------------|
| Power supply voltage                     | $PV_{DD182533\_n}$ | 2.97                           | 3.3  | 3.63                           | V    | 3.3-V RGMII/MII |
| Input logic high                         | $V_{IH}$           | 2.6                            | —    | —                              | V    |                 |
| Input logic low                          | $V_{IL}$           | —                              | —    | 0.7                            | V    |                 |
| Output logic high voltage @ 7.7 mA       | $V_{OH}$           | 2.1                            | —    | 3.6                            | V    |                 |
| Output logic low voltage @ 9.3 mA        | $V_{OL}$           | 0                              | —    | 0.5                            | V    |                 |
| Power supply voltage                     | $PV_{DD182533\_n}$ | 2.25                           | 2.5  | 2.75                           | V    | 2.5-V RGMII/MII |
| Input logic high                         | $V_{IH}$           | 1.9                            | —    | —                              | V    |                 |
| Input logic low                          | $V_{IL}$           | —                              | —    | 0.7                            | V    |                 |
| Output logic high voltage                | $V_{OH}$           | 2.0                            | —    | $PV_{DD182533\_n}$             | V    |                 |
| Output logic low voltage                 | $V_{OL}$           | $V_{SS}$                       | —    | 0.4                            | V    |                 |
| Power supply voltage                     | $PV_{DD182533\_n}$ | 1.62                           | 1.8  | 1.98                           | V    | 1.8-V RGMII/MII |
| Input logic high                         | $V_{IH}$           | $0.7 \times PV_{DD182533\_n}$  | —    | $PV_{DD182533\_n} + 0.3$       | V    |                 |
| Input logic low                          | $V_{IL}$           | $V_{SS} - 0.3$                 | —    | $0.3 \times PV_{DD182533\_n}$  | V    |                 |
| Output logic high @ $I_{OH} = 100 \mu A$ | $V_{OH}$           | $0.85 \times PV_{DD182533\_n}$ | —    | $PV_{DD182533\_n}$             | V    |                 |
| Output logic low @ $I_{OL} = 100 \mu A$  | $V_{OL}$           | $V_{SS}$                       | —    | $0.15 \times PV_{DD182533\_n}$ | V    |                 |

**Note:** n = 0, 1

Table 3.8 DC Characteristics (6) [3.3 V I/O (SD, QSPI)]

| Item                      | Symbol   | Min.                        | Typ. | Max.                        | Unit | Remarks |
|---------------------------|----------|-----------------------------|------|-----------------------------|------|---------|
| High-level input voltage  | $V_{IH}$ | $0.625 \times SDn\_PV_{DD}$ | —    | $SDn\_PV_{DD} + 0.3$        | V    |         |
| Low-level input voltage   | $V_{IL}$ | $SDn\_PV_{DD} - 0.3$        | —    | $0.25 \times SDn\_PV_{DD}$  | V    |         |
| Output logic high voltage | $V_{OH}$ | $0.75 \times SDn\_PV_{DD}$  | —    | $SDn\_PV_{DD}$              | V    |         |
|                           | (× 0.5)  |                             |      |                             |      |         |
|                           | (× 0.75) |                             |      |                             |      |         |
|                           | (× 1.0)  |                             |      |                             |      |         |
|                           | (× 1.5)  |                             |      |                             |      |         |
| Output logic low voltage  | $V_{OL}$ | 0                           | —    | $0.125 \times SDn\_PV_{DD}$ | V    |         |
|                           | (× 0.5)  |                             |      |                             |      |         |
|                           | (× 0.75) |                             |      |                             |      |         |
|                           | (× 1.0)  |                             |      |                             |      |         |
|                           | (× 1.5)  |                             |      |                             |      |         |

Table 3.9 DC Characteristics (7) [1.8 V I/O (SD, QSPI)]

| Item                      | Symbol            | Min.                      | Typ. | Max.                      | Unit | Remarks |
|---------------------------|-------------------|---------------------------|------|---------------------------|------|---------|
| High-level input voltage  | $V_{IH}$          | 1.27                      | —    | 2.00                      | V    |         |
| Low-level input voltage   | $V_{IL}$          | $SDn\_PV_{DD} - 0.3$      | —    | 0.58                      | V    |         |
| Output logic high voltage | $V_{OH}$          | $0.8 \times SDn\_PV_{DD}$ | —    | $SDn\_PV_{DD}$            | V    |         |
|                           | ( $\times 0.5$ )  |                           |      |                           |      |         |
|                           | ( $\times 0.75$ ) |                           |      |                           |      |         |
|                           | ( $\times 1.0$ )  |                           |      |                           |      |         |
|                           | ( $\times 1.5$ )  |                           |      |                           |      |         |
| Output logic low voltage  | $V_{OL}$          | 0                         | —    | $0.2 \times SDn\_PV_{DD}$ | V    |         |
|                           | ( $\times 0.5$ )  |                           |      |                           |      |         |
|                           | ( $\times 0.75$ ) |                           |      |                           |      |         |
|                           | ( $\times 1.0$ )  |                           |      |                           |      |         |
|                           | ( $\times 1.5$ )  |                           |      |                           |      |         |

Table 3.10 DC Characteristics(8) [I<sup>2</sup>C Open Drain 3.3 V I/O]

| Item                     | Symbol     | Min.                  | Typ. | Max.                  | Unit | Remarks          |
|--------------------------|------------|-----------------------|------|-----------------------|------|------------------|
| External pull-up supply  | $V_{VDDP}$ | 2.7                   | —    | $PV_{DD}$             | V    |                  |
| Input high voltage       | $V_{IH}$   | $0.7 \times V_{VDDP}$ | —    | $V_{VDDP} + 0.5$      | V    |                  |
| Input Low Voltage        | $V_{IL}$   | -0.5                  | —    | $0.3 \times V_{VDDP}$ | V    |                  |
| Low level output current | $I_{OL}$   | 20                    | —    | —                     | mA   | $V_{OL} = 0.4$ V |
| Low level output voltage | $V_{OL}$   | —                     | —    | 0.4                   | V    | $V_{VDDP} > 2$ V |
| Input hysteresis         | $V_{HYST}$ | $0.1 \times V_{VDDP}$ | —    | —                     | mV   |                  |

Table 3.11 DC Characteristics (9) [1.2-V Input (DDR4)]

| Item   | Symbol           | Min.                              | Typ. | Max.                              | Unit | Remarks |
|--|------------------|-----------------------------------|------|-----------------------------------|------|---------|
| DC input high level  | $V_{IH}(DC)$     | $V_{REF} + 0.068$                 | —    | —                                 | V    |         |
| DC input low level   | $V_{IL}(DC)$     | —                                 | —    | $V_{REF} - 0.068$                 | V    |         |
| AC input high level  | $V_{IH}(AC)$     | $V_{REF} + 0.093$                 | —    | —                                 | V    |         |
| AC input Low level   | $V_{IL}(AC)$     | —                                 | —    | $V_{REF} - 0.093$                 | V    |         |
| DC differential input high   | $V_{IHdiff}$     | 0.136                             | —    | —                                 | V    |         |
| DC differential input low  | $V_{ILdiff}$     | —                                 | —    | -0.136                            | V    |         |
| AC differential input high   | $V_{IHdiff}(AC)$ | $2 \times (V_{IH}(AC) - V_{REF})$ | —    | —                                 | V    |         |
| AC differential input low  | $V_{ILdiff}(AC)$ | —                                 | —    | $2 \times (V_{REF} - V_{IL}(AC))$ | V    |         |
| Differential input cross point voltage relative to $0.8 \times V_{DDIO}$ for DQS | $V_{IX}(DQS)$    | -0.15                             | —    | 0.06                              | V    |         |

Table 3.12 DC Characteristics (10) [1.35-V Input (DDR3L)]

| Item   | Symbol           | Min.                                   | Typ. | Max.                                   | Unit | Remarks                                  |
|--|------------------|--|------|--|------|--|
| DC input high level  | $V_{IH}(DC)$     | $V_{REF} + 0.09$                       | —    | —                                      | V    |  |
| DC input low level   | $V_{IL}(DC)$     | —                                      | —    | $V_{REF} - 0.09$                       | V    | $V_{REF} = 0.5 \times$<br>$DDR\_V_{DDQ}$ |
| AC input high level  | $V_{IH}(AC)$     | $V_{REF} + 0.135$                      | —    | —                                      | V    |  |
| AC input low level   | $V_{IL}(AC)$     | —                                      | —    | $V_{REF} - 0.135$                      | V    | $V_{REF} = 0.5 \times$<br>$DDR\_V_{DDQ}$ |
| DC differential input high   | $V_{IHdiff}$     | 0.18                                   | —    | —                                      | V    |  |
| DC differential input low  | $V_{ILdiff}$     | —                                      | —    | -0.18                                  | V    |  |
| AC differential input high   | $V_{IHdiff}(AC)$ | $2 \times$<br>$(V_{IH}(AC) - V_{REF})$ | —    | —                                      | V    |  |
| AC differential input low  | $V_{ILdiff}(AC)$ | —                                      | —    | $2 \times$<br>$(V_{REF} - V_{IL}(AC))$ | V    | $V_{REF} = 0.5 \times$<br>$DDR\_V_{DDQ}$ |
| Differential input cross point voltage relative to $0.5 \times DDR\_V_{DDQ}$ for DQS | $V_{IX}(DQS)$    | -0.075                                 | —    | 0.075                                  | V    |  |

Table 3.13 DC Characteristics (11) [1.2-V Output (DDR4)]

| Item  | Symbol       | Min. | Typ.                            | Max. | Unit | Remarks  |
|---|--------------|------|---------------------------------|------|------|--|
| DC output high measurement level (for IV curve linearity) | $V_{OH}(DC)$ | —    | $1.1 \times DDR\_V_{DDQ}$       | —    | V    | The swing of $\pm 0.15 \times$<br>$DDR\_V_{DDQ}$ is based on<br>approximately 50% of<br>the static single-ended<br>output peak-to-peak<br>swing with a driver<br>impedance of $40\Omega$ and<br>an effective test load of<br>$50\Omega$ to $V_{TT} = DDR\_V_{DDQ}$ . |
| DC output mid measurement level (for IV curve linearity)  | $V_{OM}(DC)$ | —    | $0.8 \times DDR\_V_{DDQ}$       | —    | V    |  |
| DC output low measurement level (for IV curve linearity)  | $V_{OL}(DC)$ | —    | $0.5 \times DDR\_V_{DDQ}$       | —    | V    |  |
| AC output high measurement level (for output slew rate)   | $V_{OH}(AC)$ | —    | $0.85 \times$<br>$DDR\_V_{DDQ}$ | —    | V    |  |
| AC output low measurement level (for output slew rate)    | $V_{OL}(AC)$ | —    | $0.55 \times$<br>$DDR\_V_{DDQ}$ | —    | V    |  |

Table 3.14 DC Characteristics (12) [1.35-V Output (DDR3L)]

| Item  | Symbol       | Min. | Typ.                                    | Max. | Unit | Remarks  |
|---|--------------|------|---|------|------|--|
| DC output high measurement level (for IV curve linearity) | $V_{OH}(DC)$ | —    | $0.8 \times DDR\_V_{DDQ}$               | —    | V    | The swing of $\pm 0.1 \times$<br>$DDR\_V_{DDQ}$ is based on<br>approximately 50% of<br>the static single-ended<br>output high or low swing<br>with a driver impedance<br>of $40\Omega$ and an effective<br>test load of $25\Omega$ to $V_{TT} =$<br>$DDR\_V_{DDQ}/2$ . |
| DC output mid measurement level (for IV curve linearity)  | $V_{OM}(DC)$ | —    | $0.5 \times DDR\_V_{DDQ}$               | —    | V    |  |
| DC output low measurement level (for IV curve linearity)  | $V_{OL}(DC)$ | —    | $0.2 \times DDR\_V_{DDQ}$               | —    | V    |  |
| AC output high measurement level (for output slew rate)   | $V_{OH}(AC)$ | —    | $V_{TT} + 0.1 \times$<br>$DDR\_V_{DDQ}$ | —    | V    |  |
| AC output low measurement level (for output slew rate)    | $V_{OL}(AC)$ | —    | $V_{TT} - 0.1 \times$<br>$DDR\_V_{DDQ}$ | —    | V    |  |

Table 3.15 DC Characteristics (13) [DDR4 Cross Point Voltage for Differential Output Signals (CK/DQS)]

| Item   | Symbol           | Min.  | Typ. | Max. | Unit | Remarks |
|--|------------------|-------|------|------|------|---------|
| Differential output cross point voltage relative to $0.67 \times DDR\_V_{DDQ}$ | $V_{OX}(CK/DQS)$ | -0.06 | —    | 0.06 | V    |         |

Table 3.16 DC Characteristics (14) [DDR3L Cross Point Voltage For Differential Output Signals (CK/DQS)]

| Item  | Symbol                  | Min. | Typ. | Max. | Unit | Remarks |
|---|-------------------------|------|------|------|------|---------|
| Differential output cross point voltage relative to $0.5 \times \text{DDR\_VDDQ}$ | $V_{OX}(\text{CK/DQS})$ | -0.1 | —    | 0.1  | V    |         |

Table 3.17 DC Characteristics (15) [USB 2.0]

| Item   | Symbol       | Min.  | Typ. | Max. | Unit | Remarks |
|--|--------------|-------|------|------|------|---------|
| Input levels for low/full speed  |              |       |      |      |      |         |
| High (driven)  | $V_{IH}$     | 2.0   | —    | —    | V    |         |
| Low  | $V_{IL}$     | —     | —    | 0.8  | V    |         |
| Differential input sensitivity   | $V_{DI}$     | 0.2   | —    | —    | V    |         |
| Differential common mode range   | $V_{CM}$     | 0.8   | —    | 2.5  | V    |         |
| Input levels for high speed  |              |       |      |      |      |         |
| High-speed squelch detection threshold (differential signal amplitude)       | $V_{HSSQ}$   | 100   | —    | 150  | mV   |         |
| High-speed data signaling common mode voltage range (guideline for receiver) | $V_{HSCM}$   | -50   | —    | 500  | mV   |         |
| Output levels for low/full speed   |              |       |      |      |      |         |
| Low  | $V_{OL}$     | 0.0   | —    | 0.3  | V    |         |
| High (driven)  | $V_{OH}$     | 2.8   | —    | 3.6  | V    |         |
| Output signal crossover voltage  | $V_{CRS}$    | 1.3   | —    | 2.0  | V    |         |
| Output levels for high-speed   |              |       |      |      |      |         |
| High-speed idle level  | $V_{HSOI}$   | -10.0 | —    | 10.0 | mV   |         |
| High-speed data signaling high   | $V_{HSOH}$   | 360   | —    | 440  | mV   |         |
| High-speed data signaling low  | $V_{HSOL}$   | -10.0 | —    | 10.0 | mV   |         |
| Chirp J level (differential voltage)   | $V_{CHIRPJ}$ | 700   | —    | 1100 | mV   |         |
| Chirp K level (differential voltage)   | $V_{CHIRPK}$ | -900  | —    | -500 | mV   |         |

Table 3.18 DC Characteristics (16) [ADC]

| Item                       | Symbol    | Min.     | Typ.     | Max.                    | Unit     | Remarks |
|----------------------------|-----------|----------|----------|-------------------------|----------|---------|
| Resolution                 | —         | —        | 12       | —                       | Bit      |         |
| Analog input channel       | —         | —        | —        | 2                       | Channel  |         |
| Analog input range         | $A_{IN}$  | $V_{SS}$ | —        | $\text{ADC\_AV}_{DD18}$ | V        |         |
| Differential non-linearity | DNL       | —        | —        | $\pm 3.0$               | LSB      |         |
| Integral non-linearity     | INL       | —        | —        | $\pm 6.0$               | LSB      |         |
| Full-scale error           | —         | —        | $\pm 10$ | $\pm 20$                | LSB      |         |
| Offset error               | —         | —        | $\pm 10$ | $\pm 20$                | LSB      |         |
| Analog input capacitance   | $C_{IN}$  | —        | —        | 12.6                    | pF       |         |
| Analog input resistance    | $R_{IN}$  | —        | —        | 1780                    | $\Omega$ |         |
| External capacitance       | $C_{EXT}$ | —        | —        | (*)                     | pf       |         |
| External resistance        | $R_{EXT}$ | —        | —        | (*)                     | $\Omega$ |         |

Note 1. Refer to **Figure 3.4** for  $C_{ext}$  and  $R_{ext}$ .

The  $C_{ext}$  and  $R_{ext}$  need to satisfy the sampling time.

A/D conversion time = sampling time (6T to 2800T) + 14T.

T stands for the cycle of ADIVCLK (20 MHz).

If A/D conversion is performed with the minimum conversion time, the sampling time must be 6T.

(Minimum conversion time per channel is 1  $\mu$ s when A/D conversion clock ADIVCLK is 20 MHz.)

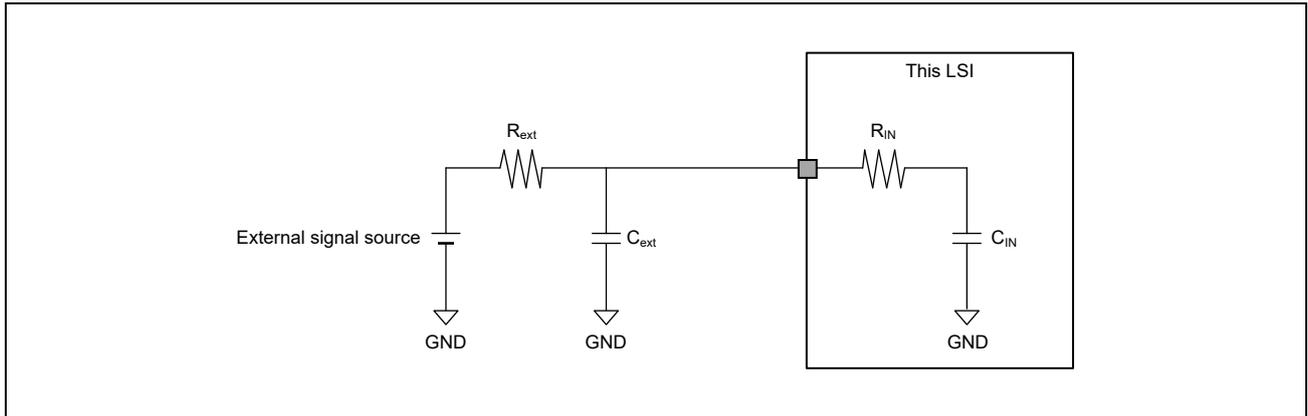


Figure 3.4 Analog Input Equivalent Circuit

Table 3.19 DC Characteristics (17) [Current Consumption]

| Item                              | Power rail symbol        | Max Current | Unit | Remarks   |
|-----------------------------------|--------------------------|-------------|------|---|
| Power Supply voltage(3.3V)        | PV <sub>DD</sub>         | 620         | mA   | PV <sub>DD</sub> =3.6V  |
| Power Supply voltage(1.8V)        | V <sub>DD18</sub>        | 20          | mA   | V <sub>DD18</sub> =1.98V                                      |
|                                   | OTP_AV <sub>DD18</sub>   | 20          | mA   | OTP_V <sub>DD18</sub> =1.95V                                  |
|                                   | ADC_AV <sub>DD18</sub>   | 10          | mA   | ADC_AV <sub>DD18</sub> =1.98V                                 |
| Power Supply voltage(1.1V)        | V <sub>DD</sub>          | 2170        | mA   | V <sub>DD</sub> =1.15V, Condition: Cortex-A55, Dhrystone      |
| Power supply voltage (USB/3.3V)   | USB_V <sub>DD33</sub>    | 20          | mA   | USB_V <sub>DD33</sub> =3.6V                                   |
| Power supply voltage (USB/1.8V)   | USB_V <sub>DD18</sub>    | 140         | mA   | USB_V <sub>DD18</sub> =1.95V                                  |
| Power supply voltage (SD/3.3V)    | SD0_PV <sub>DD</sub>     | 260         | mA   | SD0_PV <sub>DD</sub> =3.63V                                   |
|                                   | SD1_PV <sub>DD</sub>     | 170         | mA   | SD1_PV <sub>DD</sub> =3.63V                                   |
| Power supply voltage (SD/1.8V)    | SD0_PV <sub>DD</sub>     | 110         | mA   | SD0_PV <sub>DD</sub> =1.95V                                   |
|                                   | SD1_PV <sub>DD</sub>     | 70          | mA   | SD1_PV <sub>DD</sub> =1.95V                                   |
| Power supply voltage (SPI/3.3V)   | SPI_PV <sub>DD</sub>     | 50          | mA   | SPI_PV <sub>DD</sub> =3.63V                                   |
| Power supply voltage (SPI/1.8V)   | SPI_PV <sub>DD</sub>     | 100         | mA   | SPI_PV <sub>DD</sub> =1.95V                                   |
| Power supply voltage (Ether/3.3V) | PV <sub>DD182533_n</sub> | 380         | mA   | PV <sub>DD182533_n</sub> =3.63V<br>when 2 channels are in use |
| Power supply voltage (Ether/2.5V) | PV <sub>DD182533_n</sub> | 240         | mA   | PV <sub>DD182533_n</sub> =2.75V<br>when 2 channels are in use |
| Power supply voltage (Ether/1.8V) | PV <sub>DD182533_n</sub> | 140         | mA   | PV <sub>DD182533_n</sub> =1.98V<br>when 2 channels are in use |
| Power supply voltage (CSI/1.8V)   | CSI_V <sub>DD18</sub>    | 100         | mA   | CSI_V <sub>DD18</sub> =1.95V                                  |
| Power supply voltage (DDR/1.2V)   | DDR_V <sub>DDQ</sub>     | 220         | mA   | DDR_V <sub>DDQ</sub> =1.26V                                   |
| Power supply voltage (DDR/1.35V)  | DDR_V <sub>DDQ</sub>     | 210         | mA   | DDR_V <sub>DDQ</sub> =1.45V                                   |
| Power supply voltage (PLL/1.8V)   | PLL1_AV <sub>DD18</sub>  | 10          | mA   | PLL1_AV <sub>DD18</sub> =1.98V                                |
|                                   | PLL23_AV <sub>DD18</sub> | 20          | mA   | PLL23_AV <sub>DD18</sub> =1.98V                               |
|                                   | PLL4_AV <sub>DD18</sub>  | 10          | mA   | PLL4_AV <sub>DD18</sub> =1.98V                                |
|                                   | PLL5_AV <sub>DD18</sub>  | 10          | mA   | PLL5_AV <sub>DD18</sub> =1.98V                                |
|                                   | PLL6_AV <sub>DD18</sub>  | 10          | mA   | PLL6_AV <sub>DD18</sub> =1.98V                                |
| Power supply voltage (PLL/1.1V)   | PLL23_DV <sub>DD11</sub> | 20          | mA   | PLL23_DV <sub>DD11</sub> =1.15V                               |
|                                   | PLL5_DV <sub>DD11</sub>  | 10          | mA   | PLL5_DV <sub>DD11</sub> =1.15V                                |

**Note:** T<sub>j</sub> = 125°C, n = 0, 1

### 3.5 AC Characteristics

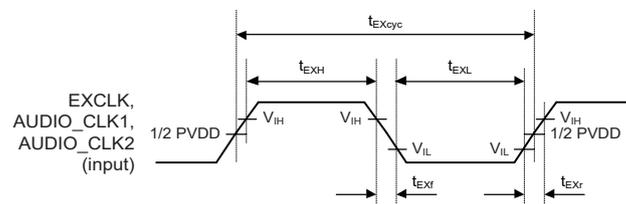
Conditions:  $V_{DD} = PLL23\_DV_{DD11} = PLL5\_DV_{DD11} = 1.1 \pm 0.05$  V,  
 $PLL1\_AV_{DD18} = PLL23\_AV_{DD18} = PLL4\_AV_{DD18} = PLL6\_AV_{DD18} = 1.8 \pm 0.18$  V,  
 $ADC\_AV_{DD18} = V_{DD18} = 1.8 \pm 0.18$  V,  $OTP\_V_{DD18} = 1.8$  V  $\pm$  0.15 V,  
 $USB\_V_{DD18} = CSI\_V_{DD18} = 1.8 \pm 0.15$  V,  
 $PV_{DD} = 3.3 \pm 0.33$  V,  $USB\_V_{DD33} = 3.3 \pm 0.3$  V,  $DDR\_V_{DDQ} = 1.2 \pm 0.06$  V/1.283 to 1.45 V,  
 $SPI\_PV_{DD} = SDn\_PV_{DD}$  (n = 0, 1) =  $3.3 \pm 0.33$  V/1.70 to 1.95 V,  
 $PV_{DD182533\_n}$  (n = 0, 1) =  $3.3 \pm 0.33$  V/2.5  $\pm$  0.25 V/1.8  $\pm$  0.18 V,  $V_{SS} = 0$  V,  
 $T_a = -40$  to  $+85^\circ\text{C}$ ,  $T_j = -40$  to  $+125^\circ\text{C}$

#### 3.5.1 Clock Timing

Table 3.20 Clock Timing Table

| Item   | Symbol      | Min.         | Max.         | Unit        | Figures            |
|--|-------------|--------------|--------------|-------------|--------------------|
| EXCLK clock input frequency  | $f_{EX}$    | 24 – 50ppm*1 | 24 + 50ppm*1 | MHz         | <b>Figure 3.5</b>  |
| EXCLK clock input cycle time   | $t_{EXcyc}$ | 41.67        | 41.67        | ns          |                    |
| AUDIO_CLK1, AUDIO_CLK2 clock input frequency<br>(external clock is input)  | $f_{EX}$    | 10           | 50           | MHz         |                    |
| AUDIO_CLK1, AUDIO_CLK2 clock input cycle time<br>(external clock is input) | $t_{EXcyc}$ | 20           | 100          | ns          |                    |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2<br>clock input low level pulse width         | $t_{EXL}$   | 0.4          | 0.6          | $t_{EXcyc}$ |                    |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2<br>clock input high level pulse width        | $t_{EXH}$   | 0.4          | 0.6          | $t_{EXcyc}$ |                    |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2<br>clock input rise time                     | $t_{EXr}$   | —            | 4            | ns          |                    |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2<br>clock input fall time                     | $t_{EXf}$   | —            | 4            | ns          |                    |
| Oscillator stabilization time  | $t_{OSC}$   | —            | 1            | ms          | <b>Figure 3.6,</b> |
| Mode hold time   | $t_{MDH}$   | —            | 100          | ns          | <b>Figure 3.7</b>  |
| Mode setup time  | $t_{MDS}$   | —            | 100          | ns          |                    |

Note 1. When using RGMII interface. If not using RGMII mode, this spec is  $\pm 100$  ppm.



**Note:** When the clock is input on the EXCLK, AUDIO\_CLK1 or AUDIO\_CLK2

Figure 3.5 EXCLK, AUDIO\_CLK1 and AUDIO\_CLK2 Clock Input Timing

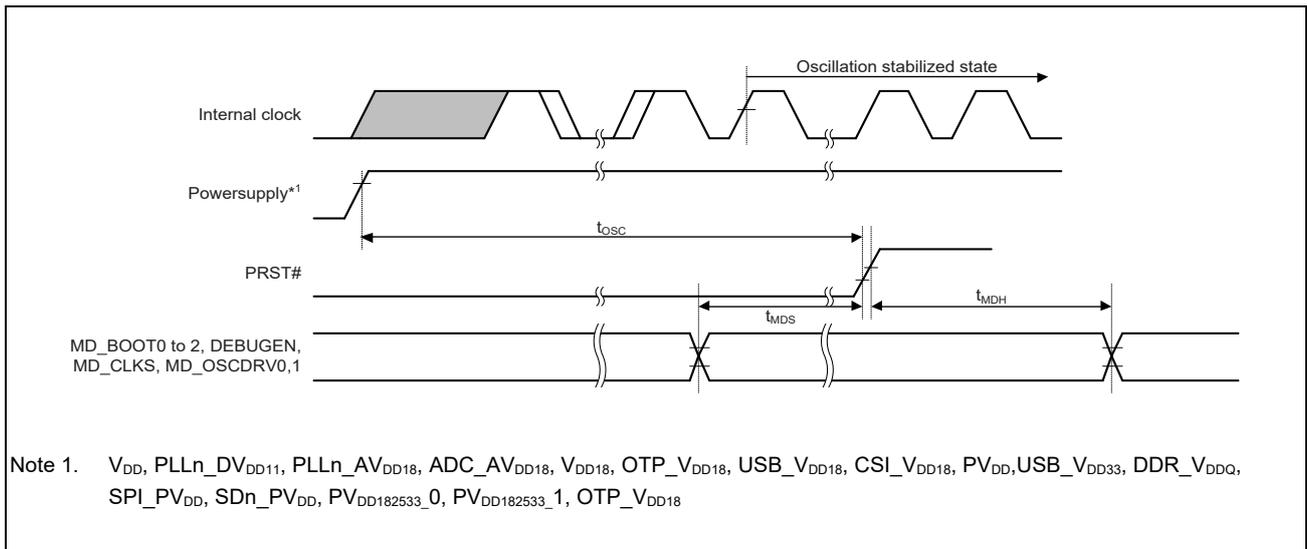


Figure 3.6 Power-On Oscillation Settling Time

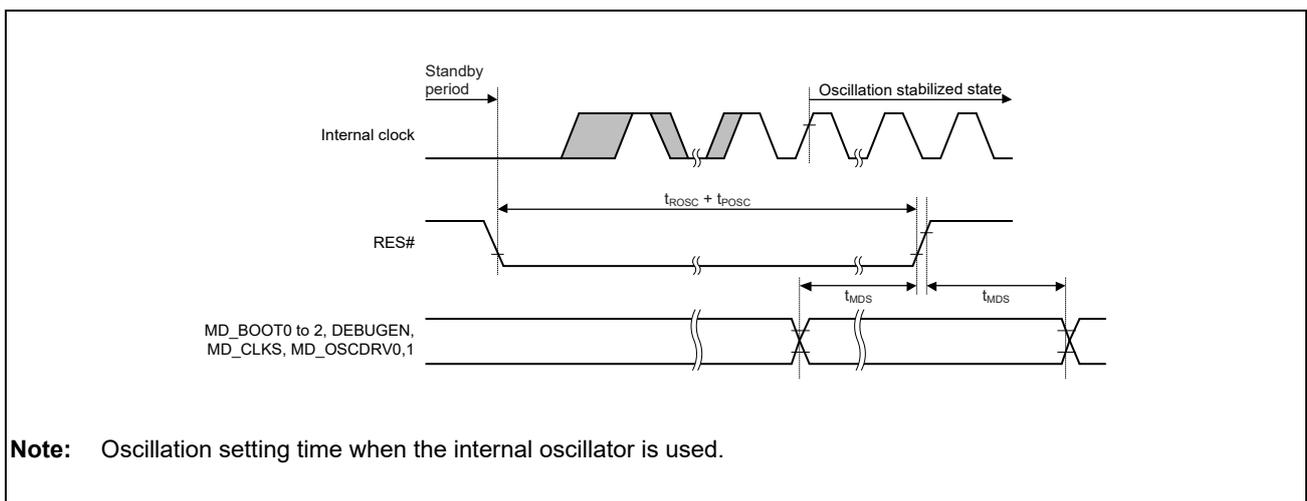


Figure 3.7 Oscillation Settling Time on Return from Standby (Return by Reset)

### 3.5.2 SDHI Access Timing

#### 3.5.2.1 SDHI Access Timing (SDR 3.3-V)

Table 3.21 SDHC AC Access Timing (SDR at 3.3-V Operation)

| Item                             | Symbol       | Default Speed Mode<br>(16.67 MHz) |      | High Speed Mode<br>(33.33 MHz) |      | Unit | Figures           |
|----------------------------------|--------------|-----------------------------------|------|--------------------------------|------|------|-------------------|
|                                  |              | Min.                              | Max. | Min.                           | Max. |      |                   |
| SD_CLK clock cycle               | $t_{SDCYC}$  | 60.00                             | —    | 30.0                           | —    | ns   | <b>Figure 3.8</b> |
| SD_CLK clock high level width    | $t_{SDWH}$   | 23.50                             | —    | 13.50                          | —    | ns   |                   |
| SD_CLK clock low level width     | $t_{SDWL}$   | 23.50                             | —    | 13.50                          | —    | ns   |                   |
| SD_CLK clock rise time           | $t_{SDLH}$   | —                                 | 10   | —                              | 3    | ns   |                   |
| SD_CLK clock fall time           | $t_{SDHL}$   | —                                 | 10   | —                              | 3    | ns   |                   |
| SD_CMD,SD_DATA output delay      | $t_{SDODLY}$ | -4.50                             | 4.0  | -4.50                          | 4.0  | ns   |                   |
| SD_CMD,SD_DATA input set up time | $t_{SDIS}$   | 5.5                               | —    | 5.5                            | —    | ns   |                   |
| SD_CMD,SD_DATA input hold time   | $t_{SDIH}$   | 2.0                               | —    | 2.0                            | —    | ns   |                   |
| SD_CMD,SD_DATA input data width  | $t_{SDIDW}$  | —                                 | —    | —                              | —    | ns   |                   |

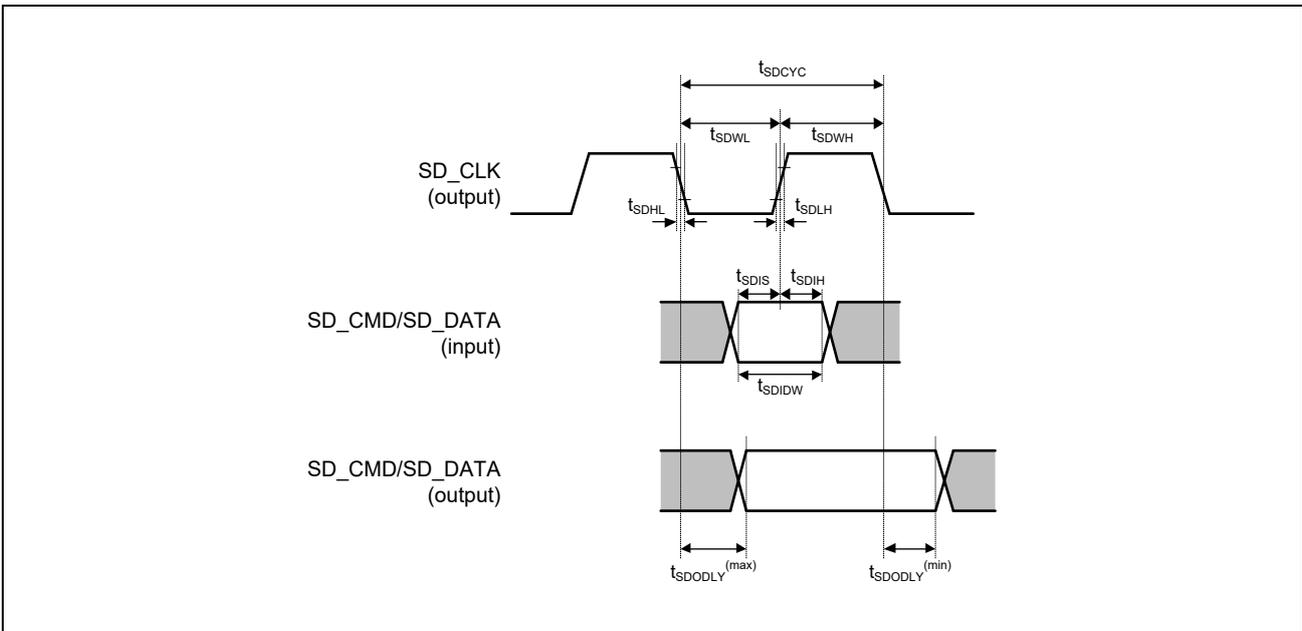


Figure 3.8 SDHC Interface Timing (SDR 3.3-V Power Supply)

**NOTE**

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact your local sales representatives.

### 3.5.3 eMMC Access Timing

#### 3.5.3.1 eMMC Host Interface Timing (Default)

Table 3.22 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

| Item                            | Symbol        | Min.  | Max. | Unit | Figures           |
|---------------------------------|---------------|-------|------|------|-------------------|
| SD0_CLK clock cycle             | $t_{MMCPP}$   | 40.00 | —    | ns   | <b>Figure 3.9</b> |
| SD0_CLK clock high level width  | $t_{MMCWH}$   | 18.50 | —    | ns   |                   |
| SD0_CLK clock low level width   | $t_{MMCWL}$   | 18.50 | —    | ns   |                   |
| SD0_CLK clock rise time         | $t_{MMCLH}$   | —     | 3    | ns   |                   |
| SD0_CLK clock fall time         | $t_{MMCHL}$   | —     | 3    | ns   |                   |
| SD0_CMD/SDDAT output delay      | $t_{MMCODLY}$ | -4.50 | 4.0  | ns   |                   |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$  | 5.5   | —    | ns   |                   |
| SD0_CMD/SDDAT input hold time   | $t_{MMCIH}$   | 2.0   | —    | ns   |                   |
| SD0_CMD/SDDAT input data width  | $t_{MMCIDW}$  | —     | —    | ns   |                   |

Table 3.23 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

| Item                            | Symbol        | Min.  | Max. | Unit | Figures           |
|---------------------------------|---------------|-------|------|------|-------------------|
| SD0_CLK clock cycle             | $t_{MMCPP}$   | 40.00 | —    | ns   | <b>Figure 3.9</b> |
| SD0_CLK clock high level width  | $t_{MMCWH}$   | 19.25 | —    | ns   |                   |
| SD0_CLK clock low level width   | $t_{MMCWL}$   | 19.25 | —    | ns   |                   |
| SD0_CLK clock rise time         | $t_{MMCLH}$   | —     | 2.45 | ns   |                   |
| SD0_CLK clock fall time         | $t_{MMCHL}$   | —     | 2.45 | ns   |                   |
| SD0_CMD/SDDAT output delay      | $t_{MMCODLY}$ | -2.00 | 2.50 | ns   |                   |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$  | 4.00  | —    | ns   |                   |
| SD0_CMD/SDDAT input hold time   | $t_{MMCIH}$   | 1.40  | —    | ns   |                   |
| SD0_CMD/SDDAT input data width  | $t_{MMCIDW}$  | —     | —    | ns   |                   |

### 3.5.3.2 eMMC host interface timing (HS-SDR)

Table 3.24 eMMC Host Interface Timing (MMC HS-SDR 3.3-V Power Supply)

| Item                            | Symbol       | Min.  | Max. | Unit | Figures           |
|---------------------------------|--------------|-------|------|------|-------------------|
| SD0_CLK clock cycle             | $t_{MMCPP}$  | 30.00 | —    | ns   | <b>Figure 3.9</b> |
| SD0_CLK clock high level width  | $t_{MMCWH}$  | 13.50 | —    | ns   |                   |
| SD0_CLK clock low level width   | $t_{MMCWL}$  | 13.50 | —    | ns   |                   |
| SD0_CLK clock rise time         | $t_{MMCLH}$  | —     | 3    | ns   |                   |
| SD0_CLK clock fall time         | $t_{MMCHL}$  | —     | 3    | ns   |                   |
| SD0_CMD/SDDAT output delay      | $t_{MMCODY}$ | -4.50 | 4.0  | ns   |                   |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | 5.5   | —    | ns   |                   |
| SD0_CMD/SDDAT input hold time   | $t_{MMCIH}$  | 2.0   | —    | ns   |                   |
| SD0_CMD/SDDAT input data width  | $t_{MMCIDW}$ | —     | —    | ns   |                   |

Table 3.25 eMMC Host Interface Timing (MMC HS-SDR 1.8-V Power Supply)

| Item                            | Symbol       | Min.  | Max. | Unit | Figures           |
|---------------------------------|--------------|-------|------|------|-------------------|
| SD0_CLK clock cycle             | $t_{MMCPP}$  | 20.00 | —    | ns   | <b>Figure 3.9</b> |
| SD0_CLK clock high level width  | $t_{MMCWH}$  | 9.25  | —    | ns   |                   |
| SD0_CLK clock low level width   | $t_{MMCWL}$  | 9.25  | —    | ns   |                   |
| SD0_CLK clock rise time         | $t_{MMCLH}$  | —     | 2.45 | ns   |                   |
| SD0_CLK clock fall time         | $t_{MMCHL}$  | —     | 2.45 | ns   |                   |
| SD0_CMD/SDDAT output delay      | $t_{MMCODY}$ | -2.00 | 2.50 | ns   |                   |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | 4.00  | —    | ns   |                   |
| SD0_CMD/SDDAT input hold time   | $t_{MMCIH}$  | 1.40  | —    | ns   |                   |
| SD0_CMD/SDDAT input data width  | $t_{MMCIDW}$ | —     | —    | ns   |                   |

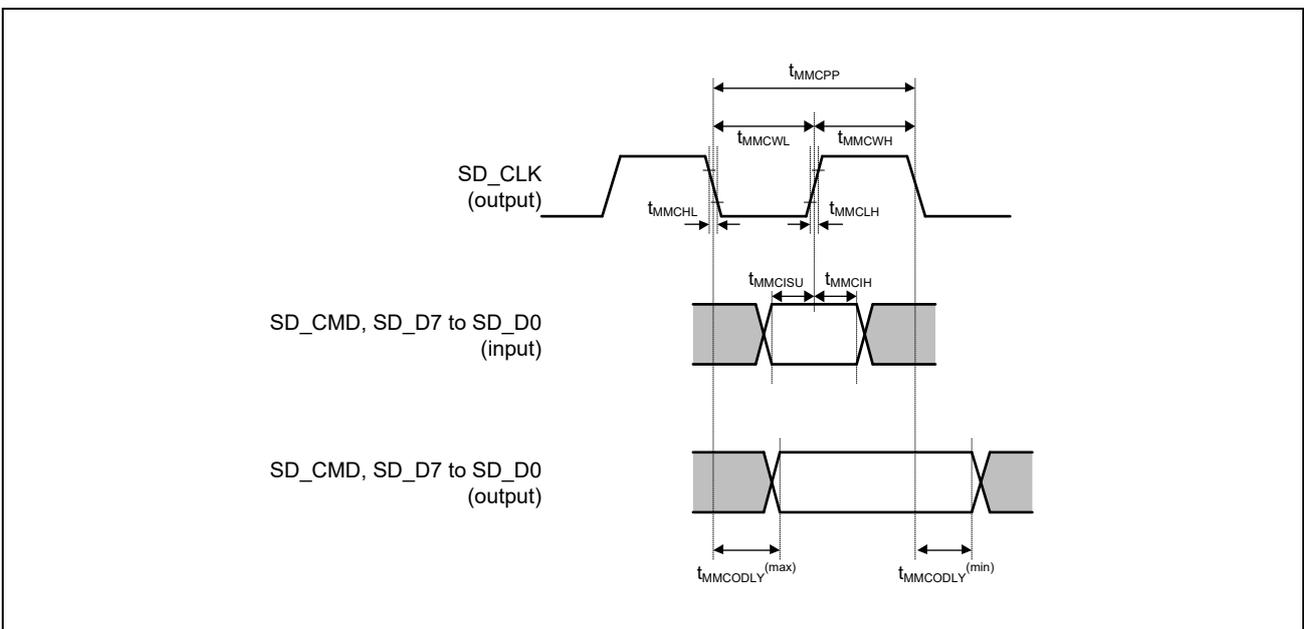


Figure 3.9 eMMC Host Interface Timing (MMC Default/HS-SDR 1.8-V/3.3-V Power Supply)

### 3.5.3.3 eMMC host interface timing (HS200)

Table 3.26 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

| Item                            | Symbol       | Min.  | Max. | Unit | Figures            |
|---------------------------------|--------------|-------|------|------|--------------------|
| SD0_CLK clock cycle             | $t_{MMCPP}$  | 7.50  | 15.0 | ns   | <b>Figure 3.10</b> |
| SD0_CLK clock high level width  | $t_{MMCWH}$  | 3.20  | —    | ns   |                    |
| SD0_CLK clock low level width   | $t_{MMCWL}$  | 3.20  | —    | ns   |                    |
| SD0_CLK clock rise time         | $t_{MMCLH}$  | —     | 1.22 | ns   |                    |
| SD0_CLK clock fall time         | $t_{MMCHL}$  | —     | 1.22 | ns   |                    |
| SD0_CMD/SDDAT output delay      | $t_{MMCODY}$ | -1.50 | 1.75 | ns   |                    |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | —     | —    | ns   |                    |
| SD0_CMD/SDDAT input hold time   | $t_{MMCIH}$  | —     | —    | ns   |                    |
| SD0_CMD/SDDAT input data width  | $t_{MMCIDW}$ | 4.31  | —    | ns   |                    |

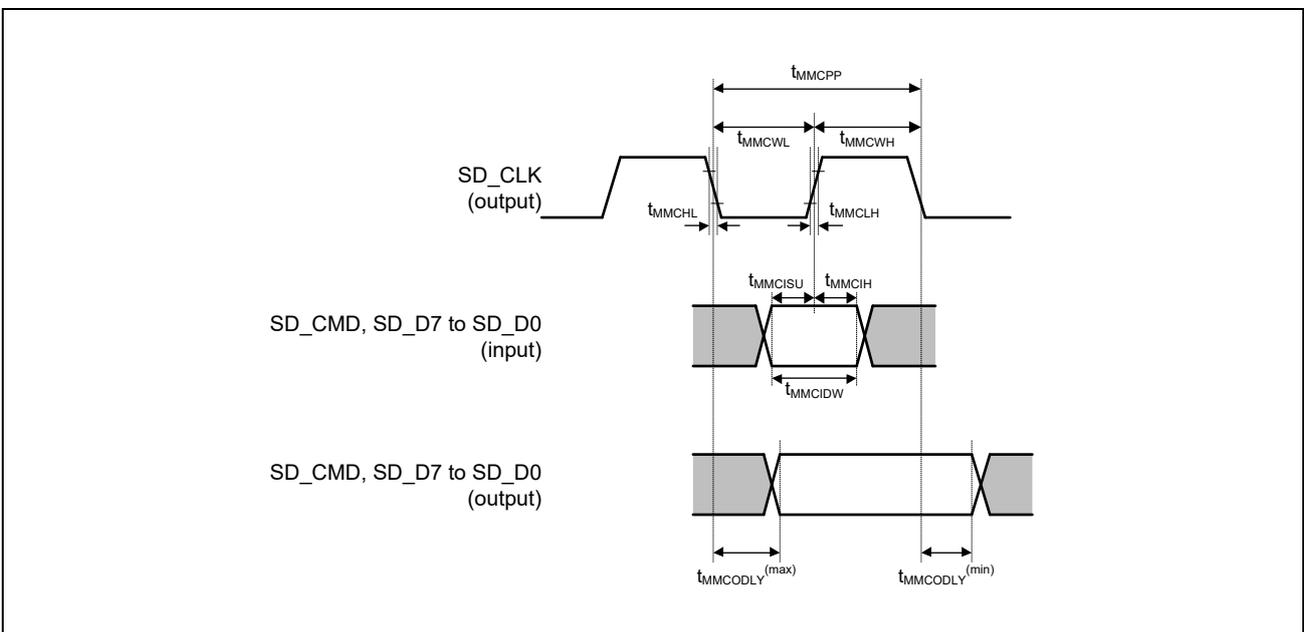


Figure 3.10 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

### 3.5.4 LCDC Access Timing

Table 3.27 LCDC AC Access Timing

| Item                  | Symbol     | Min.                | Max.                | Unit | Figures            |
|-----------------------|------------|---------------------|---------------------|------|--------------------|
| DCLK period           | $t_{Lcyc}$ | 11.5                | 172.33              | ns   | <b>Figure 3.11</b> |
| DCLK low pulse width  | $t_{LOL}$  | $t_{Lcyc}/2 - 1.06$ | $t_{Lcyc}/2 + 1.06$ | ns   |                    |
| DCLK high pulse width | $t_{LOH}$  | $t_{Lcyc}/2 - 1.06$ | $t_{Lcyc}/2 + 1.06$ | ns   |                    |
| DCLK rise time        | $t_{LOR}$  | —                   | 3                   | ns   |                    |
| DCLK fall time        | $t_{LOF}$  | —                   | 3                   | ns   |                    |
| Data output dealy     | $t_{DD}$   | -1.5                | 1.5                 | ns   |                    |

**Note:** AC access timing condition: SR = 1 (fast) / Drive capacity setting 12 mA / Load capacity 30 pF.

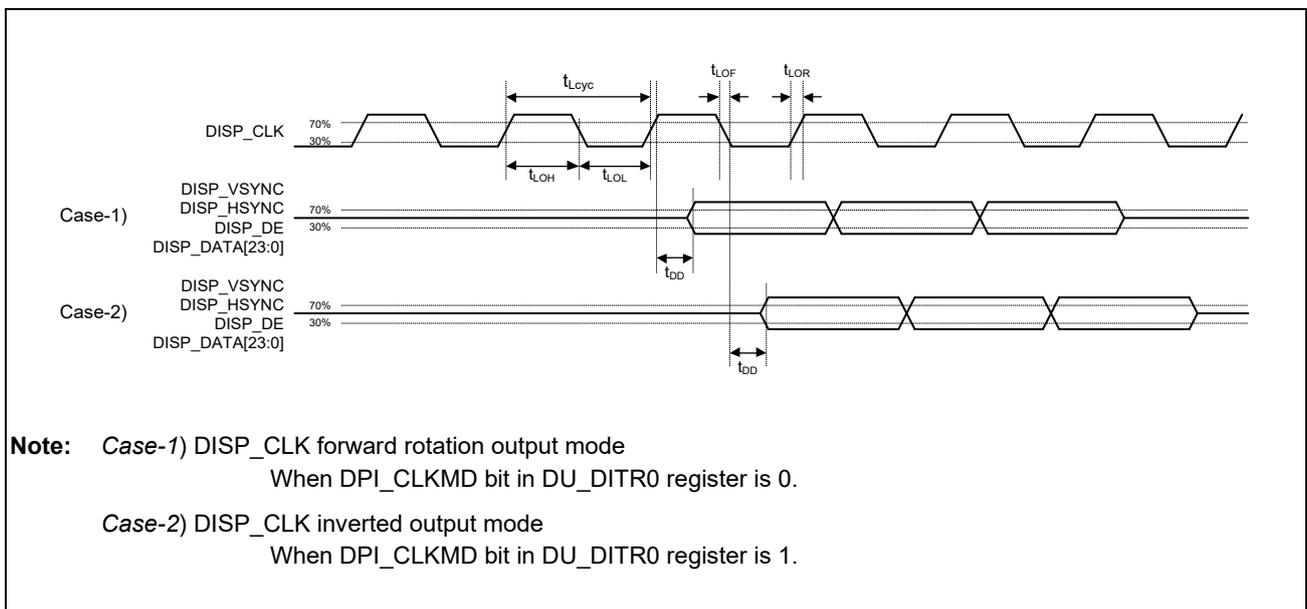


Figure 3.11 LCDC AC Access Timing

### 3.5.5 USB 2.0 Host/Function Module Access Timing

#### 3.5.5.1 USB 2.0 Low-Speed Access Timing

Table 3.28 USB Transceiver Timing (Low-Speed)

| Item               | Symbol          | Min. | Max. | Unit | Figures            |
|--------------------|-----------------|------|------|------|--------------------|
| Rise time          | $t_{LR}$        | 75   | 300  | ns   | <b>Figure 3.12</b> |
| Fall time          | $t_{LF}$        | 75   | 300  | ns   |                    |
| Rise/fall time lag | $t_{LR}/t_{LF}$ | 80   | 125  | %    |                    |

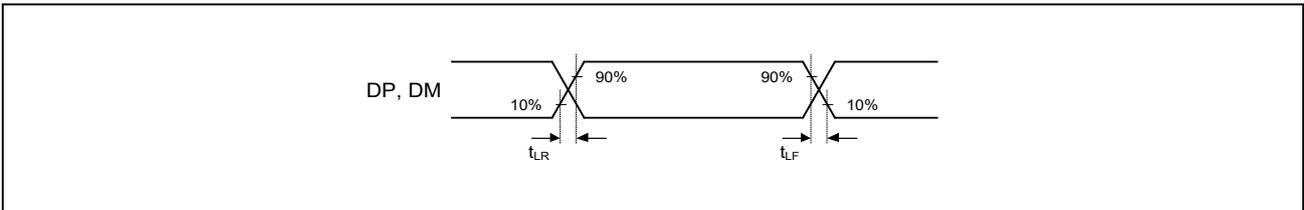


Figure 3.12 USB0\_DP, USB1\_DP, USB0\_DM, and USB1\_DM Output Timing (Low-Speed)

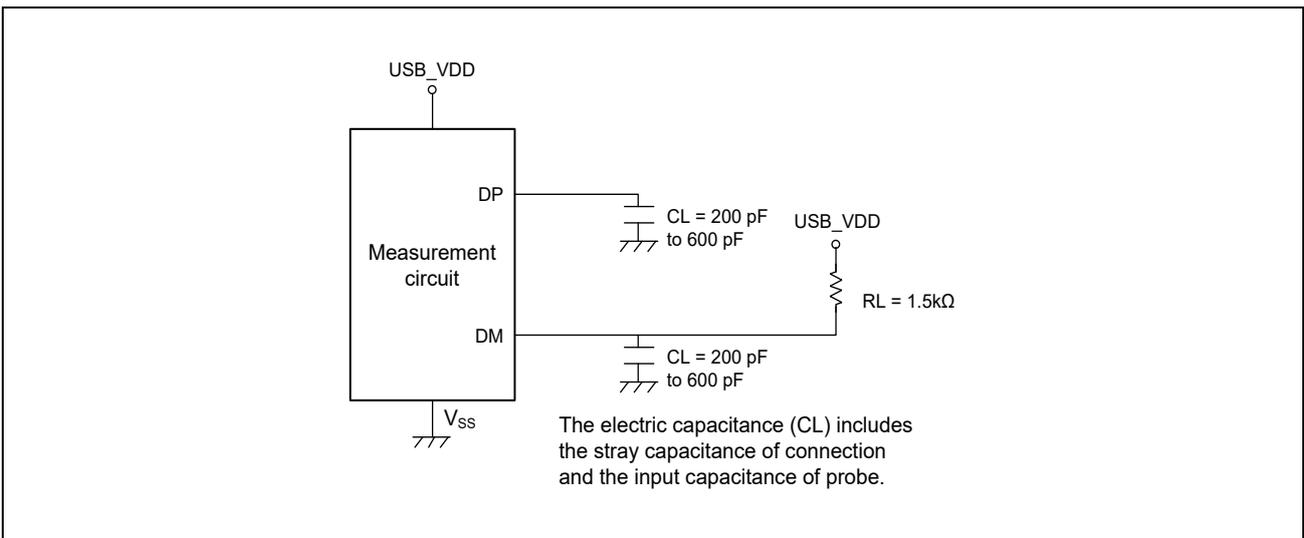


Figure 3.13 Measurement Circuit (Low-Speed)

### 3.5.5.2 USB 2.0 Full-Speed Access Timing

Table 3.29 USB Transceiver Timing (Full-Speed)

| Item               | Symbol          | Min. | Max.   | Unit | Figures            |
|--------------------|-----------------|------|--------|------|--------------------|
| Rise time          | $t_{FR}$        | 4    | 20     | ns   | <b>Figure 3.14</b> |
| Fall time          | $t_{FF}$        | 4    | 20     | ns   |                    |
| Rise/fall time lag | $t_{FR}/t_{FF}$ | 90   | 111.11 | %    |                    |

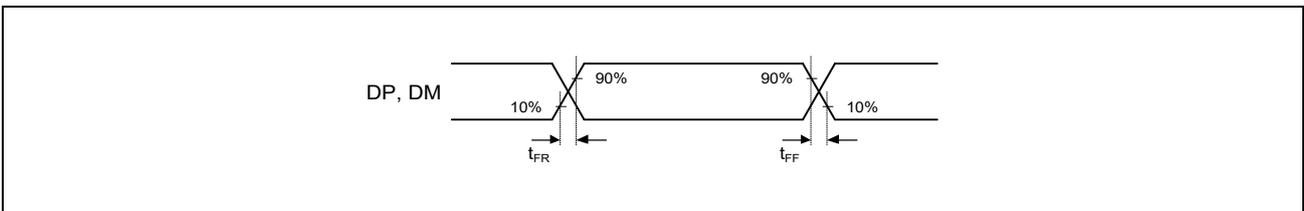


Figure 3.14 USB0\_DP, USB1\_DP, USB0\_DM, and USB1\_DM Output Timing (Full-Speed)

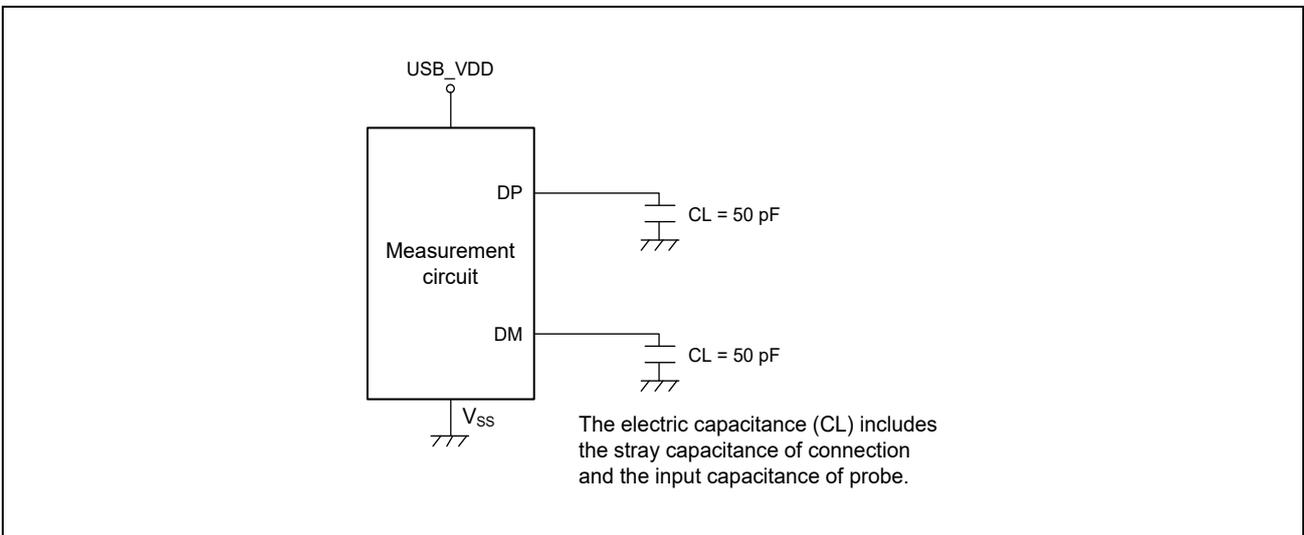


Figure 3.15 Measurement Circuit (Full-Speed)

### 3.5.5.3 USB 2.0 Hi-Speed Access Timing

Table 3.30 USB Transceiver Timing (Hi-Speed)

| Item                     | Symbol      | Min. | Max. | Unit       | Figures            |
|--------------------------|-------------|------|------|------------|--------------------|
| Rise edge rate           | $t_{HSR}$   | —    | 2133 | V/ $\mu$ s | <b>Figure 3.16</b> |
| Fall edge rate           | $t_{HSF}$   | —    | 2133 | V/ $\mu$ s |                    |
| Output driver resistance | $Z_{HSDRV}$ | 40.5 | 49.5 | $\Omega$   |                    |

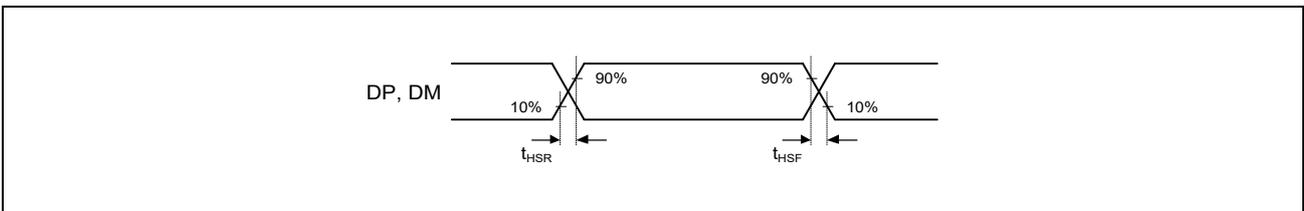


Figure 3.16 USB0\_DP, USB1\_DP, USB0\_DM, and USB1\_DM Output Timing (Hi-Speed)

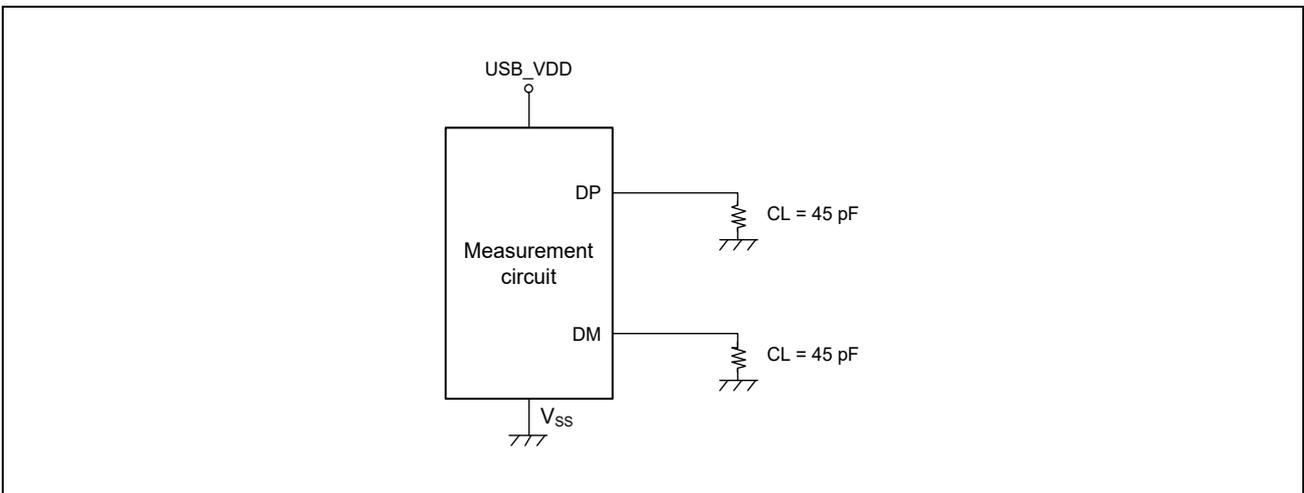


Figure 3.17 Measurement Circuit (Hi-Speed)

### 3.5.6 Ethernet Interface Access Timing

Table 3.31 Ethernet Interface Access Timing

| Item           | Symbol         | Min. | Max. | Unit | Figures            |
|----------------|----------------|------|------|------|--------------------|
| MDC half cycle | $t_{MDC}$      | 0    | 300  | ns   | <b>Figure 3.18</b> |
| MDI setup time | $t_{MDIsetup}$ | 10   | —    | ns   |                    |
| MDI hold time  | $t_{MDIhold}$  | 10   | —    | ns   |                    |

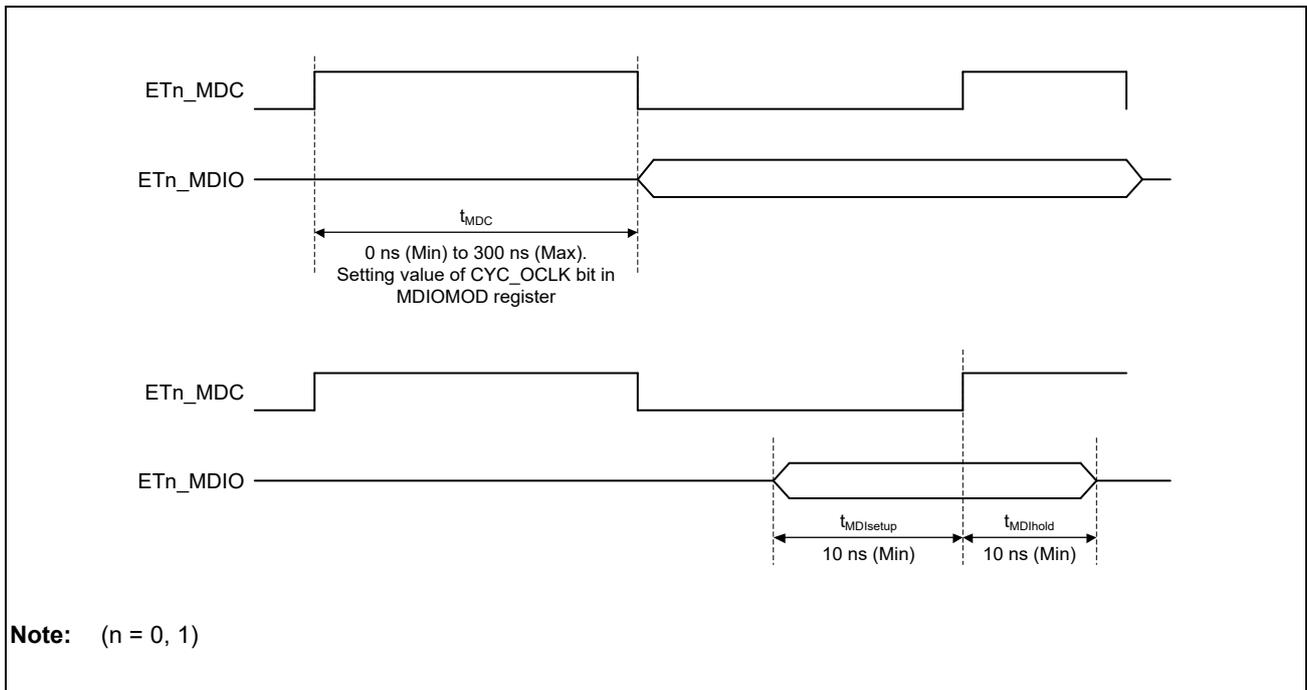


Figure 3.18 Management Interface

### 3.5.6.1 Ethernet-IF (Ether MII)

Table 3.32 Ethernet-IF Access Timing (Ether MII)

| Item      | Symbol                  | Min.       | Max. | Unit | Figures |                    |
|-----------|-------------------------|------------|------|------|---------|--------------------|
| Ether MII | ETH_GTXTXC_TXC period   | $t_{Tcyc}$ | 40   | —    | ns      | <b>Figure 3.19</b> |
|           | ETH_TXCTL output delay  | $t_{TEND}$ | 0    | 25   | ns      |                    |
|           | ETH_TXD3-0 output delay | $t_{MTDd}$ | 0    | 25   | ns      |                    |
|           | ETH_RXC period          | $t_{Rcyc}$ | 40   | —    | ns      |                    |
|           | ETH_RXDV setup time     | $t_{RDVs}$ | 10   | —    | ns      |                    |
|           | ETH_RXDV hold time      | $t_{RDVh}$ | 10   | —    | ns      |                    |
|           | ETH_RXD3-0 setup time   | $t_{MRDs}$ | 10   | —    | ns      |                    |
|           | ETH_RXD3-0 hold time    | $t_{MRDh}$ | 10   | —    | ns      |                    |
|           | ETH_RXER setup time     | $t_{RERs}$ | 10   | —    | ns      |                    |
|           | ETH_RXER hold time      | $t_{RERh}$ | 10   | —    | ns      |                    |

**Note:** I/O driving ability: 8 mA  
CL = 8 pF

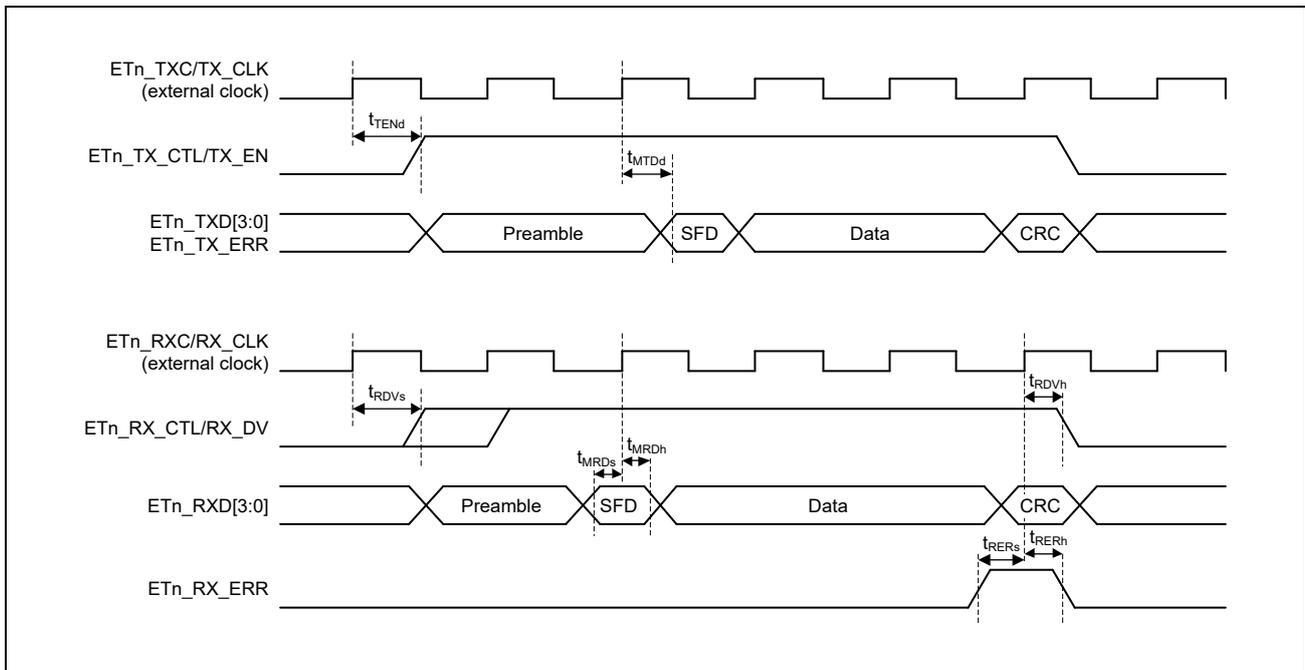


Figure 3.19 MII Transmission Timing

Validated with IEEE802.3 regulation.

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns.

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns.

### 3.5.6.2 Ethernet-IF (Ether RGMII)

Table 3.33 Ethernet-IF Access Timing (Ether RGMII)

| Item        | Symbol   | Min.         | Typ. | Max. | Unit | capaci-<br>tance | Remarks | Figures     |                    |
|-------------|--|--------------|------|------|------|------------------|---------|-------------|--------------------|
| Ether RGMII | Data to clock output skew @ transmitter                    | $T_{skewT}$  | -500 | 0    | 500  | ps               | 8 pF    | Tx RGMII    | <b>Figure 3.20</b> |
|             | Data to clock input skew @ receiver                        | $T_{skewR}$  | 1    | 1.8  | 2.6  | ns               | 8 pF    |             |                    |
|             | Data to clock output setup @ transmitter integrated delay  | $T_{setupT}$ | 1.2  | 2.0  | —    | ns               | 8 pF    | Rx RGMII-ID | <b>Figure 3.21</b> |
|             | Clock to data output hold @ transmitter integrated delay   | $T_{holdT}$  | 1.2  | 2.0  | —    | ns               | 8 pF    |             |                    |
|             | Data to clock input setup @ receiver integrated delay      | $T_{setupR}$ | 1.0  | 2.0  | —    | ns               | 8 pF    | Rx RGMII-ID | <b>Figure 3.21</b> |
|             | Data to clock input setup hold @ receiver integrated delay | $T_{holdR}$  | 1.0  | 2.0  | —    | ns               | 8 pF    |             |                    |
|             | Clock cycle duration* <sup>1</sup>                         | $T_{cyc}$    | 7.2  | 8    | 8.8  | ns               | 8 pF    | —           | —                  |
|             | Duty cycle for gigabit                                     | Duty_G       | 45   | 50   | 55   | %                | 8 pF    |             |                    |
|             | Duty cycle for 10/100T                                     | Duty_T       | 40   | 50   | 60   | %                | 8 pF    |             |                    |
|             | Rise/fall time (20-80%)                                    | $T_r/T_f$    | —    | —    | 0.75 | ns               | 8 pF    |             |                    |

Note 1. For 10 Mbps and 100 Mbps,  $T_{cyc}$  will scale to 400ns  $\pm$ 40ns and 40ns  $\pm$ 4ns respectively.

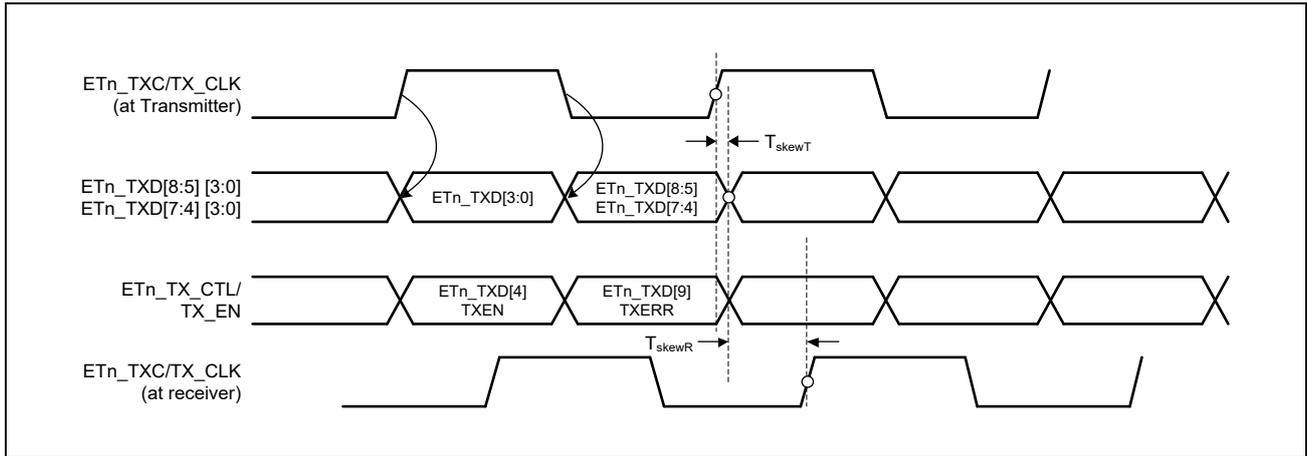


Figure 3.20 Multiplexing & Timing Diagram — RGMII (Transmitter)

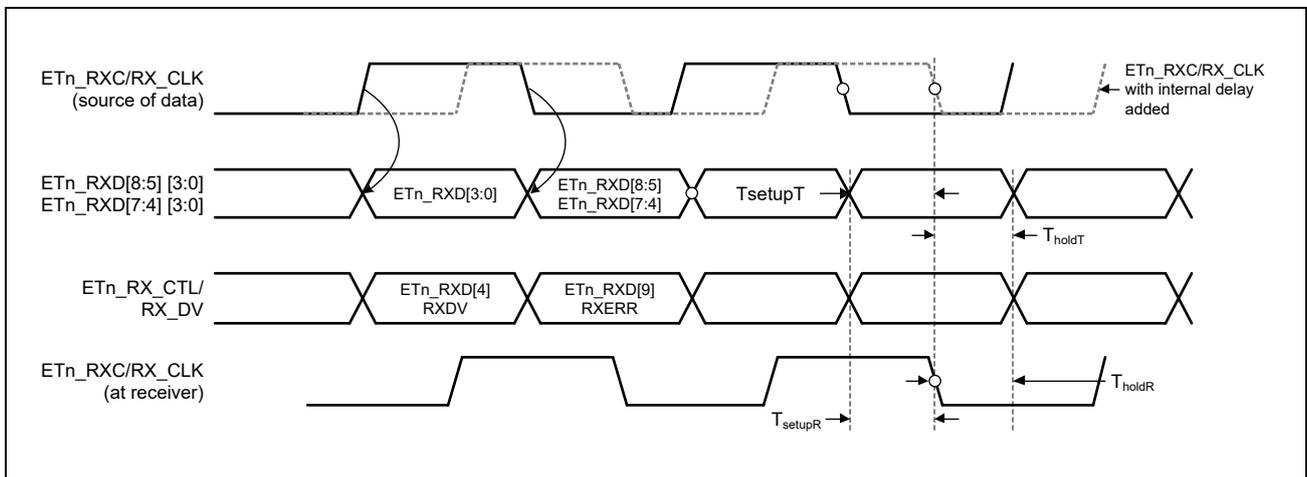


Figure 3.21 Multiplexing & Timing Diagram — RGMII-ID (Receiver)

### 3.5.7 JTAG Debugger Interface Access Timing

Table 3.34 Debugger IF Timing

| Item                        | Symbol        | Min. | Max. | Unit | Figures            |
|-----------------------------|---------------|------|------|------|--------------------|
| TCK_SWCLK cycle time        | $t_{TCKcyc}$  | 50   | —    | ns   | <b>Figure 3.22</b> |
| TCK_SWCLK high pulse width  | $t_{TCKH}$    | 20   | —    | ns   | <b>Figure 3.23</b> |
| TCK_SWCLK low pulse width   | $t_{TCKL}$    | 20   | —    | ns   |                    |
| TDI setup time              | $t_{TDIS}$    | 15   | —    | ns   |                    |
| TDI hold time               | $t_{TDIH}$    | 15   | —    | ns   |                    |
| TMS_SWDIO setup time        | $t_{TMSS}$    | 15   | —    | ns   |                    |
| TMS_SWDIO hold time         | $t_{TMSh}$    | 15   | —    | ns   |                    |
| SWDIO delay time            | $t_{SWDO}$    | —    | 14   | ns   |                    |
| TDO delay time              | $t_{TDOD}$    | —    | 14   | ns   |                    |
| Capture register setup time | $t_{CAPTS}$   | 10   | —    | ns   | <b>Figure 3.24</b> |
| Capture register hold time  | $t_{CAPTH}$   | 10   | —    | ns   |                    |
| Update register delay time  | $t_{UPDATED}$ | —    | 20   | ns   |                    |

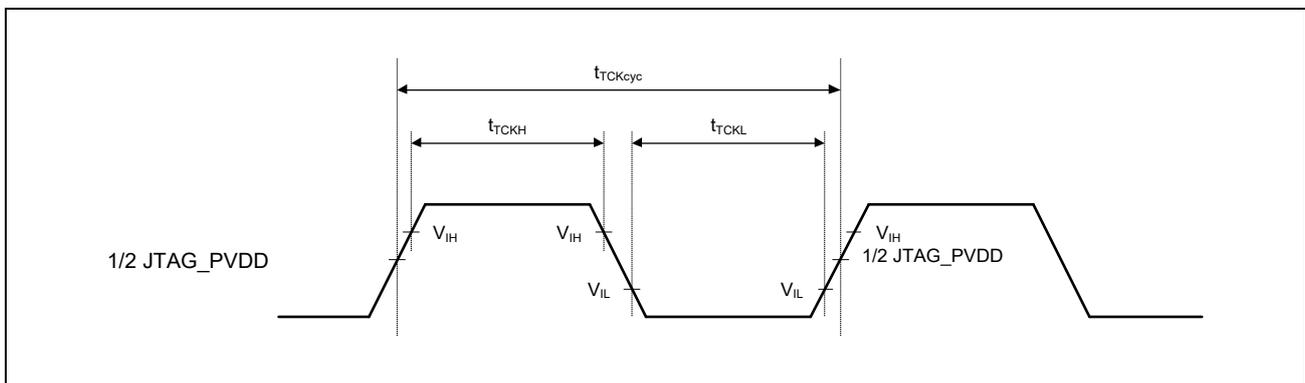


Figure 3.22 TCK\_SWCLK Input Timing

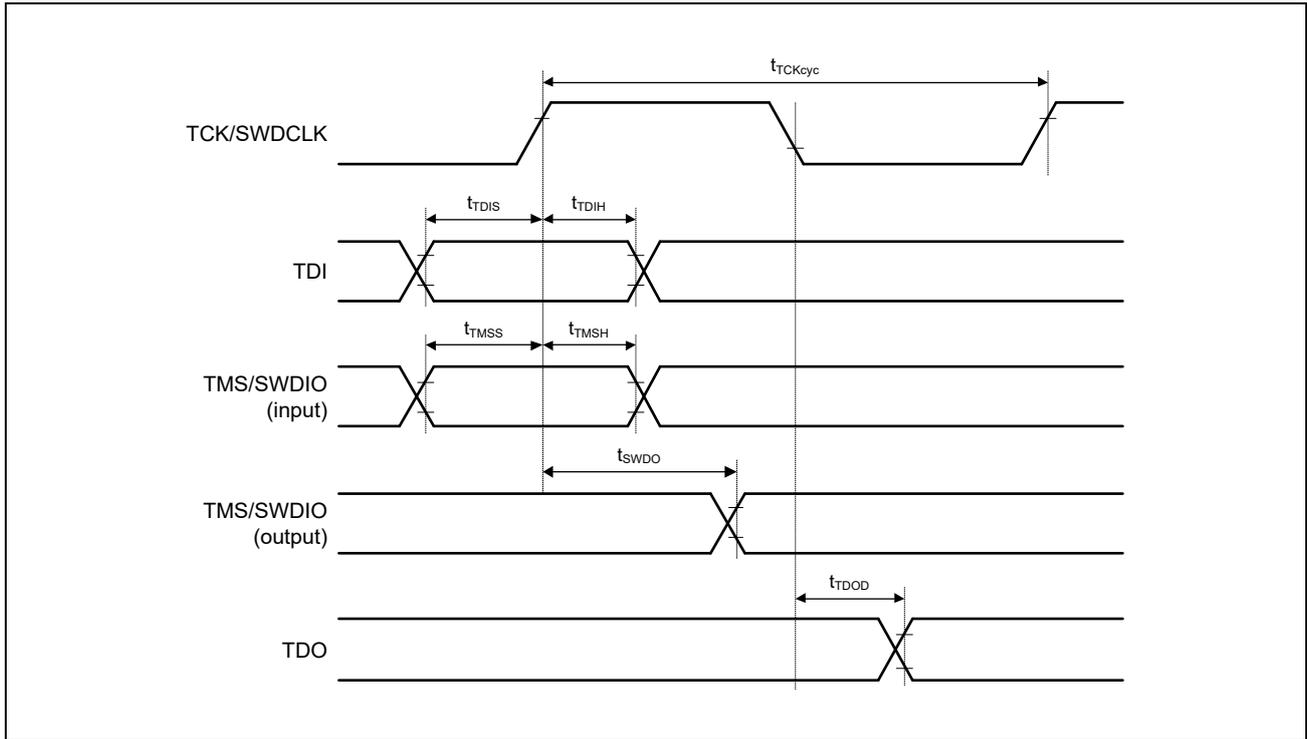


Figure 3.23 Data Transfer Timing

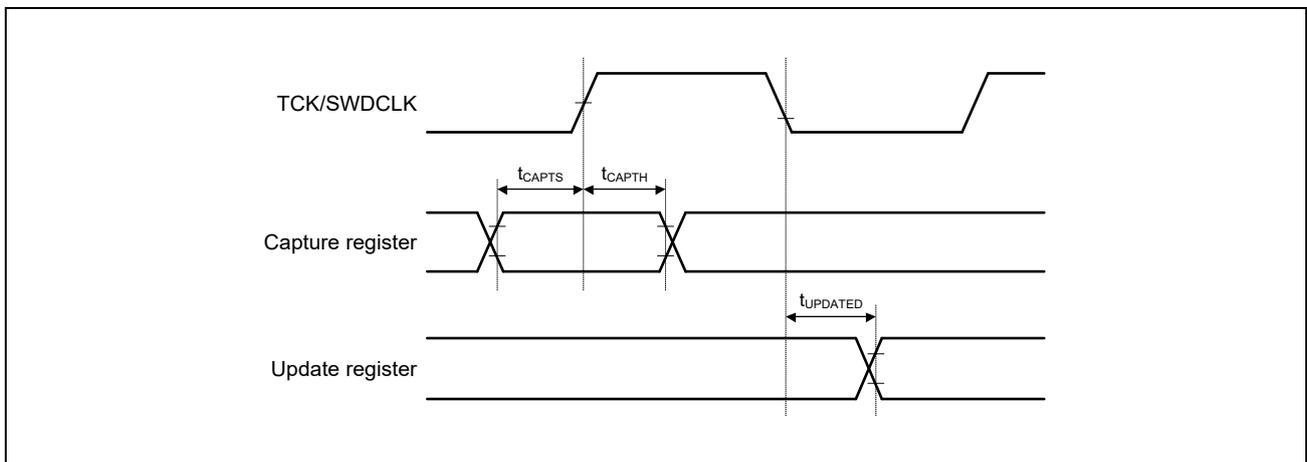


Figure 3.24 Boundary Scan Input/Output I/O Timing

### 3.5.8 SPI Multi I/O Bus Controller Access Timing

Table 3.35 SPI Multi I/O Bus Controller Access Timing

| Item                           | Symbol  | 1.8 V                                    |                             | 3.3 V                       |                             | Unit         | Figures                  |             |
|--------------------------------|---|--|-----------------------------|-----------------------------|-----------------------------|--------------|--------------------------|-------------|
|                                |   | (Serial flash/octal-SPI flash connected) |                             | (Serial flash connected)    |                             |              |                          |             |
|                                |   | Min.                                     | Max.                        | Min.                        | Max.                        |              |                          |             |
| Clock cycle                    | $t_{SPBcyc}$                                      | 15.0                                     | —                           | 15.0                        | —                           | ns           | Figure 3.25              |             |
| CLK high pulse width           | $t_{SPBWH}$                                       | 0.45                                     | 0.55                        | 0.45                        | 0.55                        | $t_{SPBcyc}$ | Figure 3.25              |             |
| CLK low pulse width            | $t_{SPBWL}$                                       | 0.45                                     | 0.55                        | 0.45                        | 0.55                        | $t_{SPBcyc}$ | Figure 3.25              |             |
| CLK rise time                  | $t_{SPBR}$  | —  | 1.0                         | —                           | 3.2                         | ns           | Figure 3.25              |             |
| CLK fall time                  | $t_{SPBF}$  | —  | 1.0                         | —                           | 3.2                         | ns           | Figure 3.25              |             |
| Data input setup time          | QSPI0_SPCLK base point (SDR mode timing adjusted) | $t_{SU}$                                 | 6.7                         | —                           | 7.5                         | —            | ns                       | Figure 3.26 |
|                                | QSPI0_SPCLK base point (DDR mode timing adjusted) |  | 4.5                         | —                           | 4.5                         | —            | ns                       | Figure 3.27 |
| Data input hold time           | QSPI0_SPCLK base point (SDR mode timing adjusted) | $t_{H}$                                  | 0.5                         | —                           | 0.5                         | —            | ns                       | Figure 3.26 |
|                                | QSPI0_SPCLK base point (DDR mode timing adjusted) |  | 1.0                         | —                           | 1.0                         | —            | ns                       | Figure 3.27 |
| SSL setup time                 | $t_{LEAD}$  | $1.5 \times t_{SPBcyc} - 3$              | $8.5 \times t_{SPBcyc} + 3$ | $1.5 \times t_{SPBcyc} - 3$ | $8.5 \times t_{SPBcyc} + 3$ | ns           | Figure 3.26, Figure 3.27 |             |
| SSL hold time                  | $t_{LAG}$   | $1 \times t_{SPBcyc} - 3$                | $8 \times t_{SPBcyc} + 3$   | $1 \times t_{SPBcyc} - 3$   | $8 \times t_{SPBcyc} + 3$   | ns           | Figure 3.26, Figure 3.27 |             |
| Continuous transfer delay time | $t_{TD}$  | $1 \times t_{SPBcyc} - 3$                | $8 \times t_{SPBcyc} + 3$   | $1 \times t_{SPBcyc} - 3$   | $8 \times t_{SPBcyc} + 3$   | ns           | Figure 3.26, Figure 3.27 |             |
| Data output delay time         | SDR   | $t_{OD}$                                 | —                           | 2.0                         | —                           | 5.0          | ns                       | Figure 3.26 |
|                                | DDR   |  | —                           | $6.5^{*2}$                  | —                           | $7.5^{*3}$   | ns                       | Figure 3.27 |
| Data output hold time          | SDR   | $t_{OH}$                                 | -2.0                        | —                           | -5.0                        | —            | ns                       | Figure 3.26 |
|                                | DDR   |  | $1.0^{*2}$                  | —                           | $2.1^{*3}$                  | —            | ns                       | Figure 3.27 |
| Data output buffer off time    | SDR   | $t_{BOFF}$                               | —                           | 2.0                         | —                           | 3.0          | ns                       | Figure 3.28 |
|                                | DDR   |  | —                           | 2.0                         | —                           | 3.0          | ns                       | Figure 3.28 |

Note 1. Output load: 15 pF/driving ability: 12 mA

Note 2. QSPI0\_SPCLK frequency: 100 MHz.

Note 3. QSPI0\_SPCLK frequency: 66 MHz

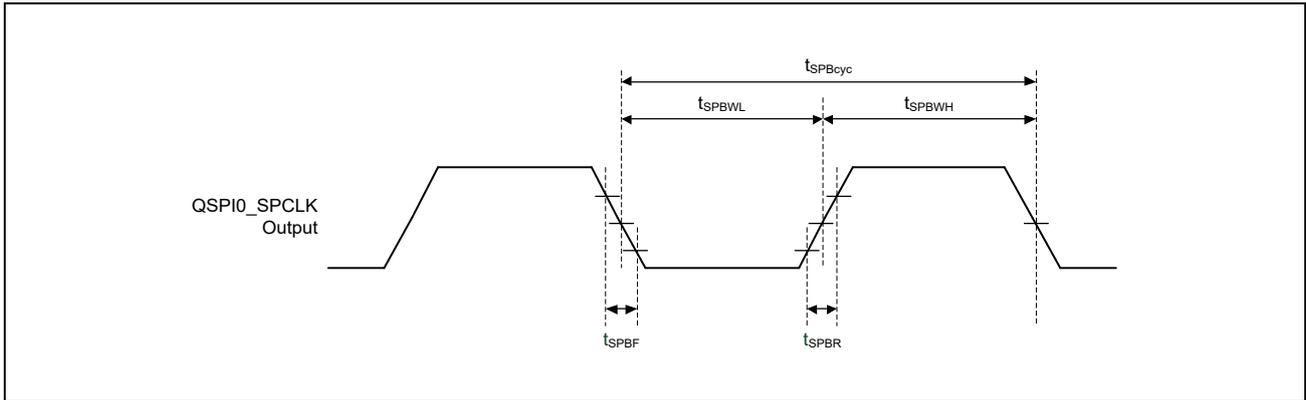


Figure 3.25 Clock Timing

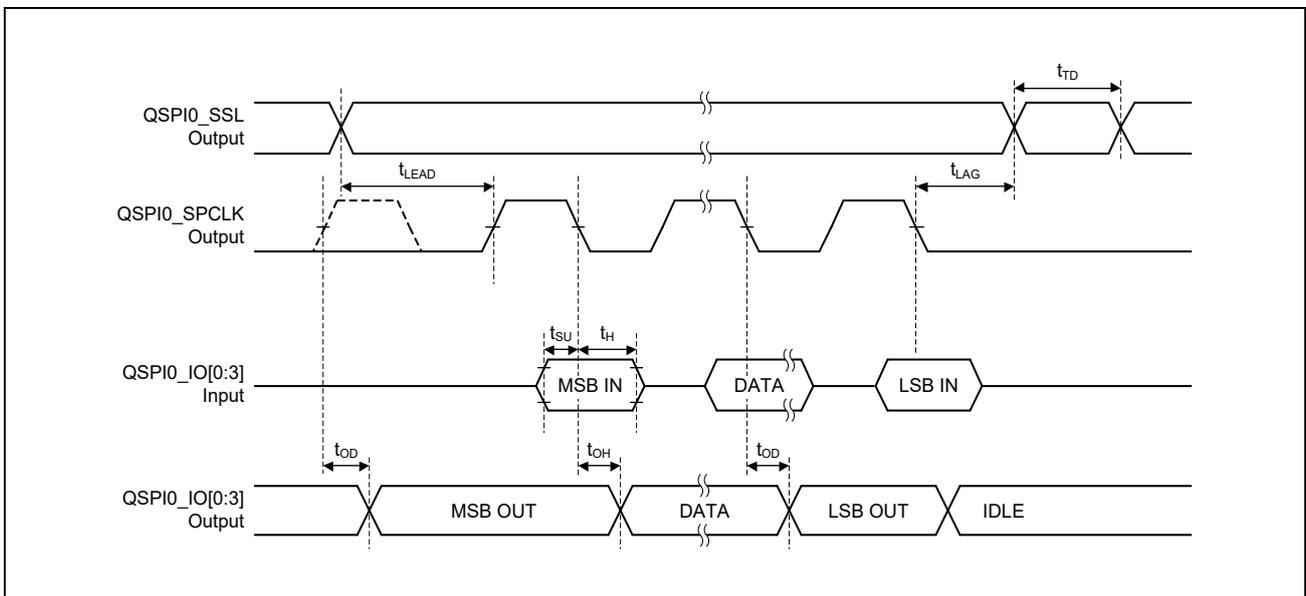


Figure 3.26 SDR Transfer Format Transmission and Reception Timing

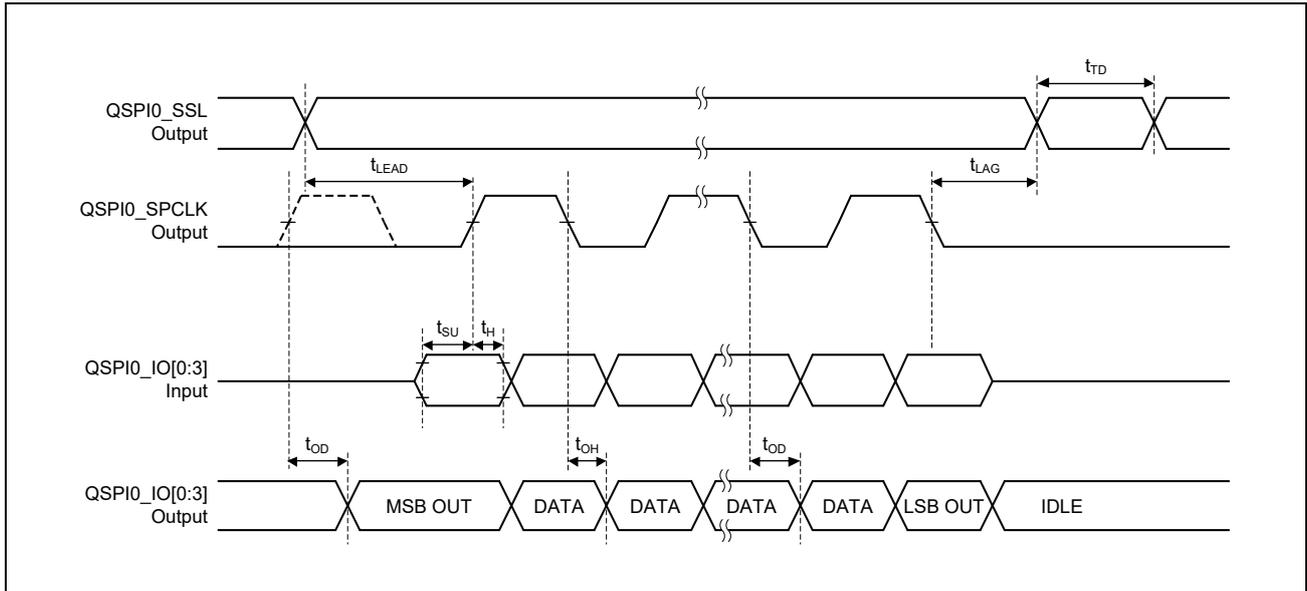


Figure 3.27 DDR Transfer Format Transmission and Reception Timing

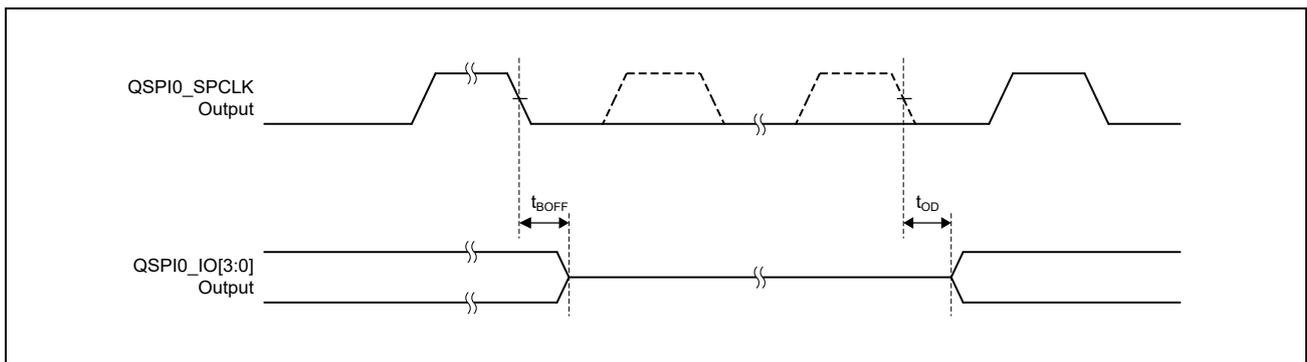


Figure 3.28 Timing for Switching the Buffers On and Off

### 3.5.9 Control Signal Access Timing

Table 3.36 Control Signal Timing

| Item                  | Symbol      | Min. | Max. | Unit           | Figures            |
|-----------------------|-------------|------|------|----------------|--------------------|
| PRST# pulse width     | $t_{RESW}$  | 20   | —    | $t_{cyc}^{*1}$ | <b>Figure 3.29</b> |
| TRST# pulse width     | $t_{TRSW}$  | 20   | —    | $t_{cyc}^{*1}$ |                    |
| NMI pulse width       | $t_{NMIW}$  | 20   | —    | $t_{cyc}^{*1}$ | <b>Figure 3.31</b> |
| IRQ pulse width       | $t_{IRQW}$  | 20   | —    | $t_{cyc}^{*1}$ |                    |
| TINT pulse width      | $t_{TINTW}$ | 20   | —    | $t_{cyc}^{*1}$ |                    |
| PRST# input rise time | $t_{RSr}$   | —    | 500  | $\mu s$        | <b>Figure 3.30</b> |

Note 1.  $t_{cyc} = 41.666 \text{ ns}$  (24 MHz)

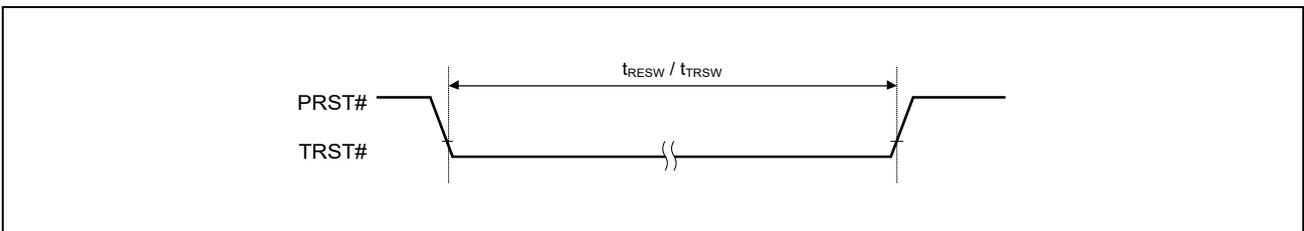


Figure 3.29 Reset Input Timing 1

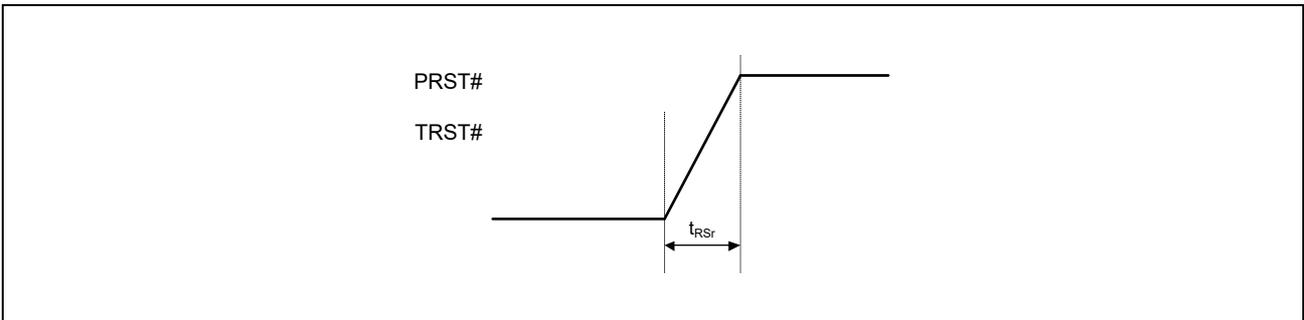


Figure 3.30 Reset Input Timing 2

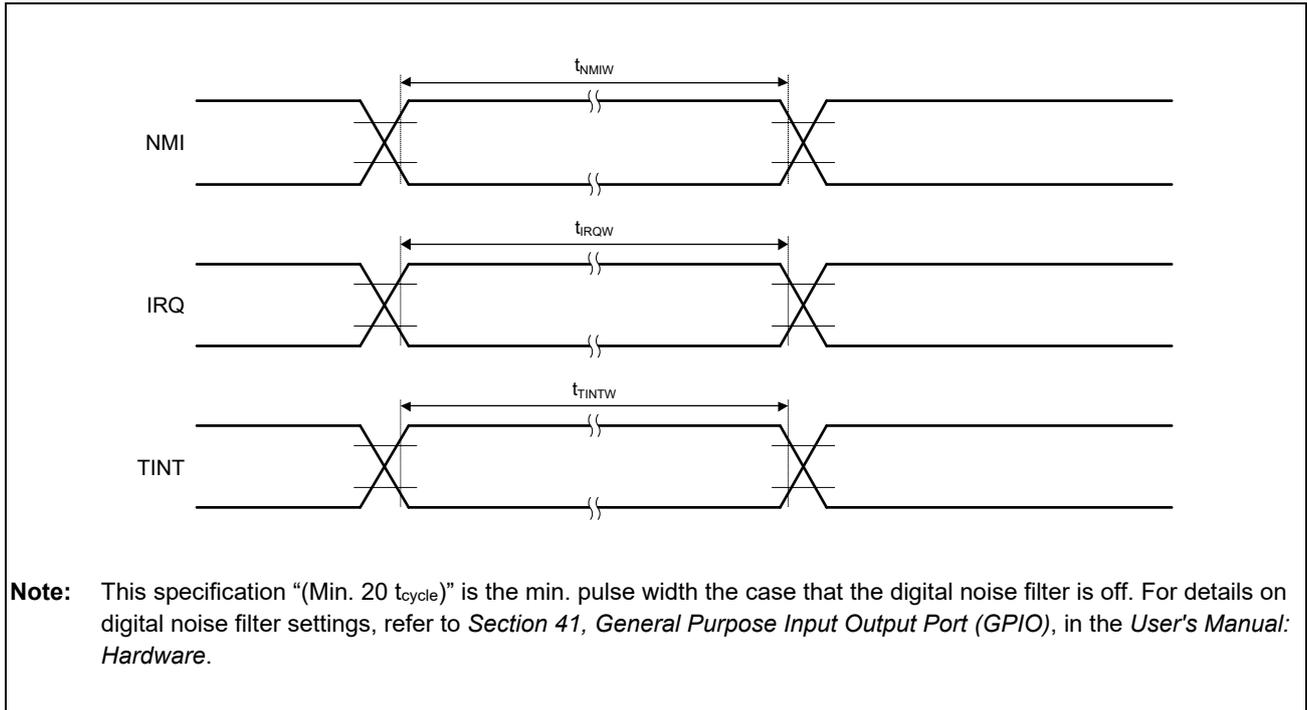


Figure 3.31 Interrupt Signal Input Timing

### 3.5.10 Serial Sound Interface (SSIF-2) Access Timing

Table 3.37 SSIF-2 Timing

| Item  | I/O           | Symbol          | Min. | Max.  | Unit | Figures      |
|---|---------------|-----------------|------|-------|------|--------------|
| Output clock cycle                                    | Output        | $t_O$           | 80   | 64000 | ns   | Figure 3.32  |
| Input clock cycle                                     | Input         | $t_I$           | 80   | —     | ns   |              |
| Clock high  | Bidirectional | $t_{HC}$        | 32   | —     | ns   |              |
| Clock low   |               | $t_{LC}$        | 32   | —     | ns   |              |
| Clock rise time/clock fall time                       | Output        | $t_{RC}/t_{FC}$ | —    | 25    | ns   |              |
| Setup time  | Input         | $t_{SR}$        | 25   | —     | ns   | Figure 3.33, |
| Hold time   |               | $t_{HR}$        | 5    | —     | ns   | Figure 3.34, |
| SILRCK output delay time                              | Output        | $t_{DTR}$       | -5   | 25    | ns   | Figure 3.35  |
| Data output delay time<br>(Noise canceler not in use) |               | $t_{DTR}$       | -5   | 25    | ns   |              |
| Data output delay time<br>(Noise canceler in use)     |               | $t_{DTR}$       | 10   | 50    | ns   |              |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

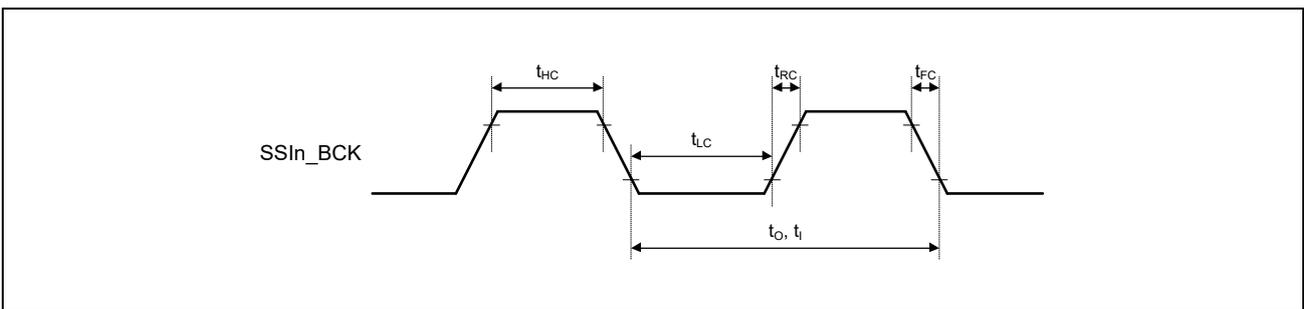


Figure 3.32 Bit Clock Input/Output Timing

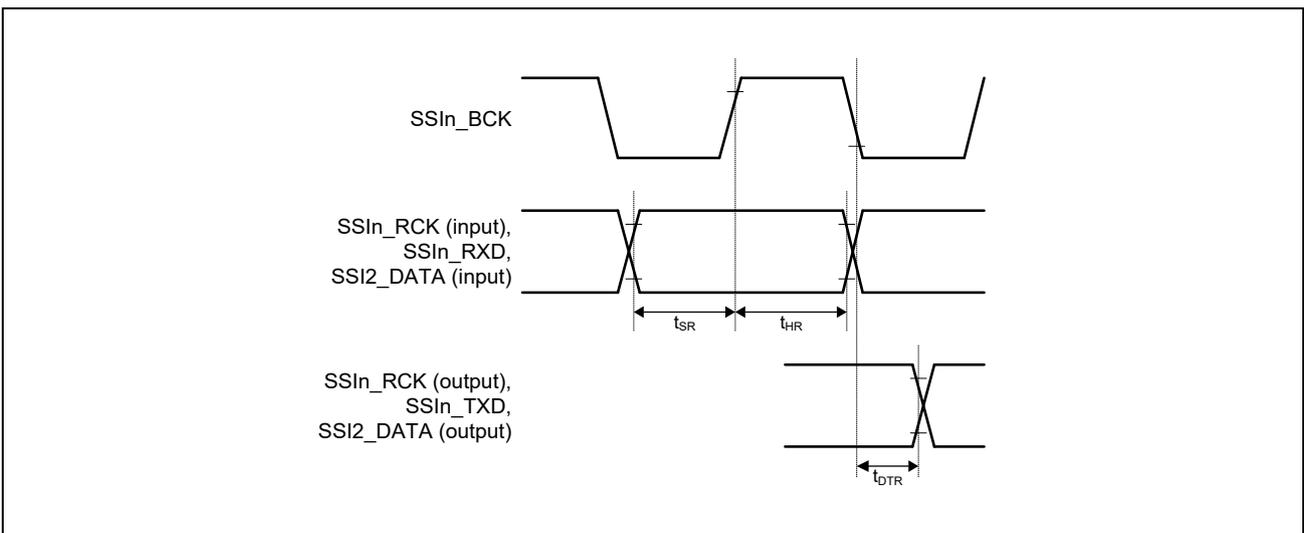


Figure 3.33 Transmission and Reception Timing (SSIBCK Falling Output)

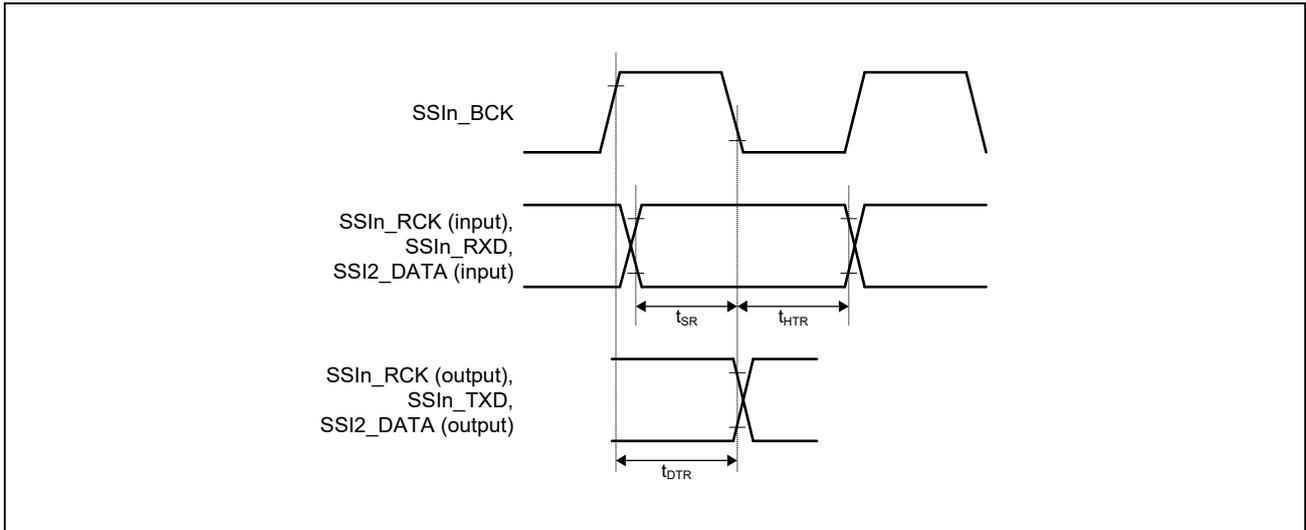


Figure 3.34 Transmission and Reception Timing (SSIBCK Rising Output)

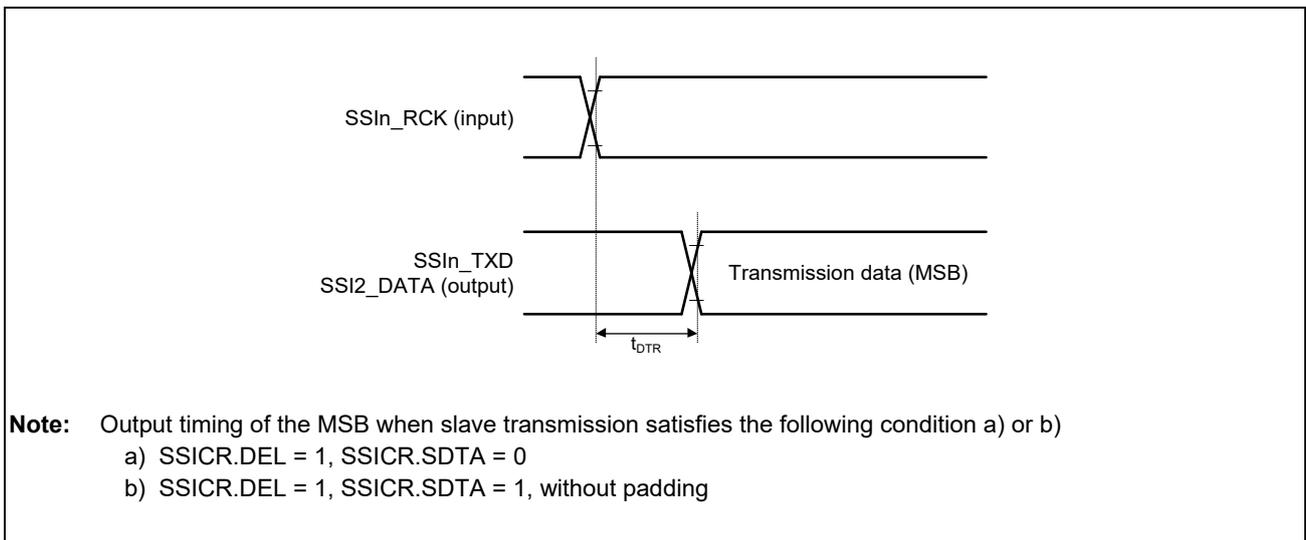


Figure 3.35 Transmission Timing (Slave, in Synchronization with SSILRCK)

### 3.5.11 CAN-FD Interface Access Timing

Table 3.38 CAN-FD Interface Timing

| Item                | Symbol          | CAN  |      | CAN-FD |      | Unit | Figures            |
|---------------------|-----------------|------|------|--------|------|------|--------------------|
|                     |                 | Min. | Max. | Min.   | Max. |      |                    |
| Internal delay time | $t_{node}^{*1}$ | —    | 100  | —      | 75   | ns   | <b>Figure 3.36</b> |
| Transmission rate   | —               | —    | 1    | —      | 4    | Mbps |                    |

**Note:** AC access timing condition: drive ability 12mA, output load 15pF, slew rate = fast

Note 1. Internal delay time ( $t_{node}$ ) = Internal transfer delay time ( $t_{output}$ ) + Internal receive delay time ( $t_{input}$ )

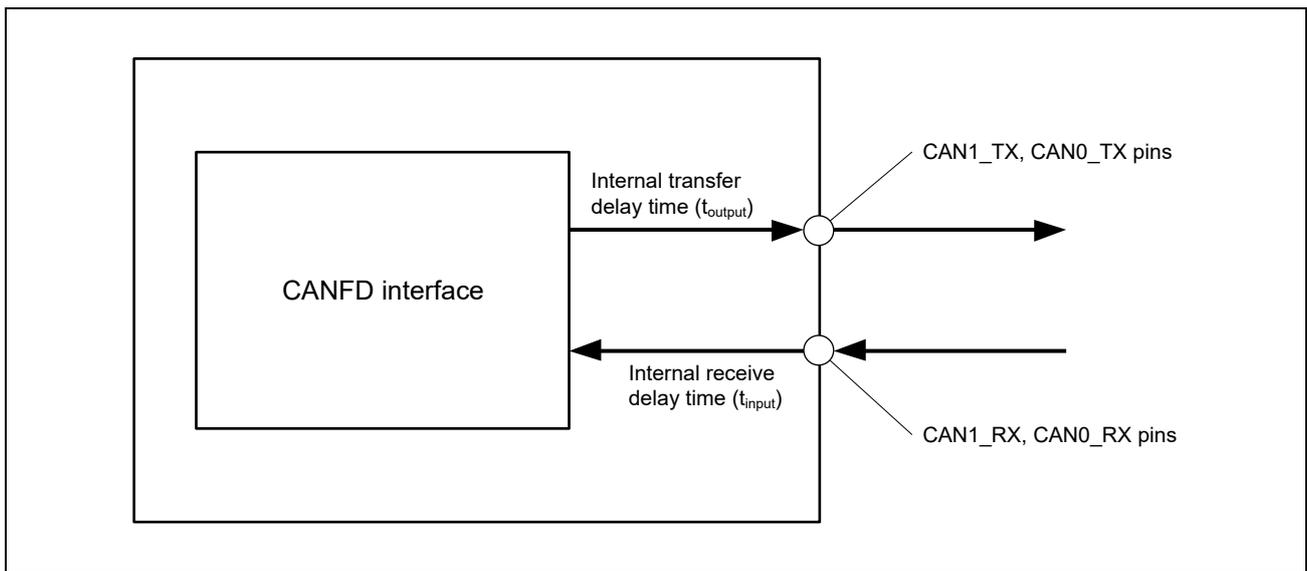


Figure 3.36 CAN-FD Interface Condition

### 3.5.12 Multi-Function Timer Pulse Unit 3 (MTU3a) Access Timing

Table 3.39 MTU3a Timing

| Item  |                                 |                     | Symbol       | Min. | Max. | Unit*1           | Figures     |
|-------|---------------------------------|---------------------|--------------|------|------|------------------|-------------|
| MTU3a | Input capture input pulse width | Single-edge setting | $t_{MTICW}$  | 1.5  | —    | $t_{p1cyc}^{*1}$ | Figure 3.37 |
|       |                                 | Both-edge setting   |              | 2.5  | —    |                  |             |
| MTU3a | Timer clock pulse width         | Single-edge setting | $t_{MTCKWH}$ | 1.5  | —    | $t_{p1cyc}^{*1}$ | Figure 3.38 |
|       |                                 | Both-edge setting   | $t_{MTCKWL}$ | 2.5  | —    |                  |             |
|       |                                 | Phase counting mode |              | 2.5  | —    |                  |             |

**Note:** AC access timing condition: drive ability 4mA, output load 30pF, slew rate = fast

Note 1.  $t_{p1cyc}$  indicates peripheral clock means MTU\_X\_MCLK\_MTU3 (P0φ).

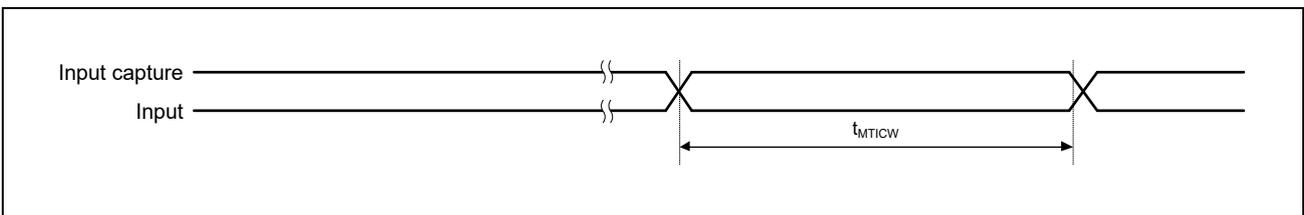


Figure 3.37 MTU3a Input Capture Input Timing

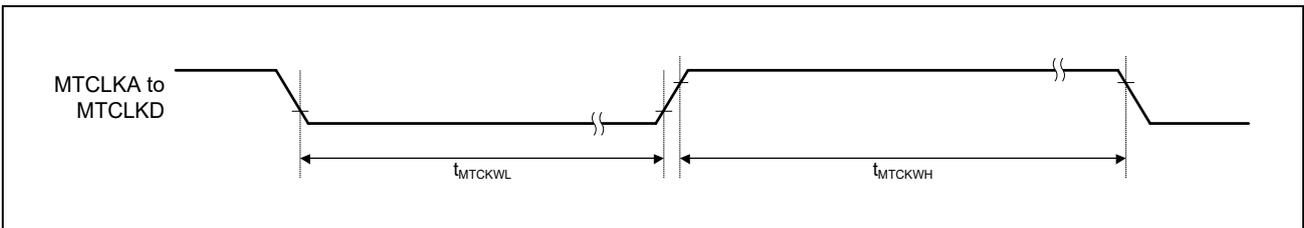


Figure 3.38 MTU3a Clock Input Timing

### 3.5.13 Port Output Enable 3 (POE3) Access Timing

Table 3.40 POE3 Timing

| Item | Symbol                  | Min.        | Max. | Unit | Figures                            |
|------|-------------------------|-------------|------|------|------------------------------------|
| POE3 | POEn# input pulse width | $t_{POE3W}$ | 1.5  | —    | $t_{p1cy}^{*1}$ <b>Figure 3.39</b> |

Note 1.  $t_{p1cy}$  indicates peripheral clock means POE3\_CLKM\_POE (P0 $\phi$ ).

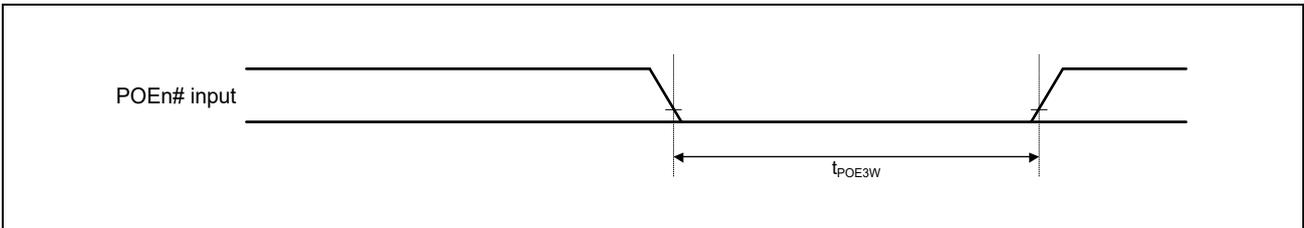


Figure 3.39 POEn# Input Pulse Timing

### 3.5.14 I<sup>2</sup>C Bus Interface Access Timing

Table 3.41 I<sup>2</sup>C Bus Interface Timing

| Item  | Symbol              | I/O    | Standard Mode (Sm) |       | Fast Mode (Fm)                   |       | Fast Mode Plus (Fm+)             |       | Unit |
|---|---------------------|--------|--------------------|-------|----------------------------------|-------|----------------------------------|-------|------|
|   |                     |        | Min.               | Max.  | Min.                             | Max.  | Min.                             | Max.  |      |
| SCL clock frequency   | f <sub>CLK</sub>    | I/O    | 0                  | 100   | 0                                | 400   | 0                                | 1000  | kHz  |
| Bus free time (between stop and start condition)                  | t <sub>BUF</sub>    | I/O    | 4.7                | —     | 1.3                              | —     | 0.5                              | —     | μs   |
| Hold time*1   | t <sub>HD:STA</sub> | I/O    | 4.0                | —     | 0.6                              | —     | 0.26                             | —     | μs   |
| Low period of SCL clock   | t <sub>LOW</sub>    | I/O    | 4.7                | —     | 1.3                              | —     | 0.5                              | —     | μs   |
| High period of SCL clock  | t <sub>HIGH</sub>   | I/O    | 4.0                | —     | 0.6                              | —     | 0.26                             | —     | μs   |
| Setup time for start / restart condition                          | t <sub>SU:STA</sub> | I/O    | 4.7                | —     | 0.6                              | —     | 0.26                             | —     | μs   |
| Data hold time (I <sup>2</sup> C bus device)                      | t <sub>HD:DAT</sub> | I/O    | 0*2                | —     | 0*2                              | —     | 0                                | —     | μs   |
| Data setup time   | t <sub>SU:DAT</sub> | I/O    | 250                | —     | 100*3                            | —     | 50                               | —     | ns   |
| SDA and SCL signal rise time                                      | t <sub>R</sub>      | Input  | —                  | 1000  | 20                               | 300   | —                                | 120   | ns   |
| SDA and SCL signal fall time*3                                    | t <sub>F</sub>      | Input  | —                  | 300   | 20 × (P <sub>VDD</sub> /5.5 V)   | 300   | 20 × (P <sub>VDD</sub> /5.5 V)   | 120   | ns   |
|   |                     | Output | —                  | 300   | 20 × (P <sub>VDD</sub> /5.5 V)*6 | 300*6 | 20 × (P <sub>VDD</sub> /5.5 V)*7 | 120*7 | ns   |
| Setup time for STOP condition                                     | t <sub>SU:STO</sub> | I/O    | 4.0                | —     | 0.6                              | —     | 0.26                             | —     | μs   |
| Capacitive load for each bus line                                 | C <sub>b</sub>      | —      | —                  | 400*4 | —                                | 400*4 | —                                | 550*4 | pF   |
| Pulse width of spikes that must be suppressed by the input filter | t <sub>SP</sub>     | Input  | —                  | —     | 0                                | 50*5  | 0                                | 50*5  | ns   |

**Note:** In the above table and subsequently, SCL and SDA refer to the RIICnSCL and RIICnSDA signals, respectively.

**Note:** AC access timing condition: drive ability 4mA, output load 400pF, slew rate = slow

- Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.
- Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the CnSCL signal reaches V<sub>IL</sub> (max.) from V<sub>IH</sub> (min.)).
- Note 3. The fast-mode I<sup>2</sup>C bus device can be used in the standard mode I<sup>2</sup>C bus system. In this case, the minimum value of the data setup time (t<sub>SU:DAT</sub> (min.) 250 [ns]) must be satisfied.  
If the system does not extend the low period of SCL clock (t<sub>LOW</sub>), this condition is automatically satisfied. If the system extends the low period of SCL clock (t<sub>LOW</sub>), transmit the subsequent data bit to the SDA line before the SCL line is released (t<sub>R</sub> (max.) + t<sub>SU:DAT</sub> (min.) = 1000 + 250 = 1250 [ns]; (standard mode I<sup>2</sup>C bus specification)).
- Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I<sup>2</sup>C bus specification provided by NXP Semiconductors.
- Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICφ) and the NF[1:0] bits in RIICnMR3. For details, refer to *Section 26, I<sup>2</sup>C Bus Interface*, in the *User's Manual: Hardware*.
- Note 6. External pull-up resistor is required 1077Ω to 1770Ω when using RIIC ch2 or RIIC ch3.
- Note 7. External pull-up resistor is required 240Ω to 257Ω when using RIIC ch2 or RIIC ch3.

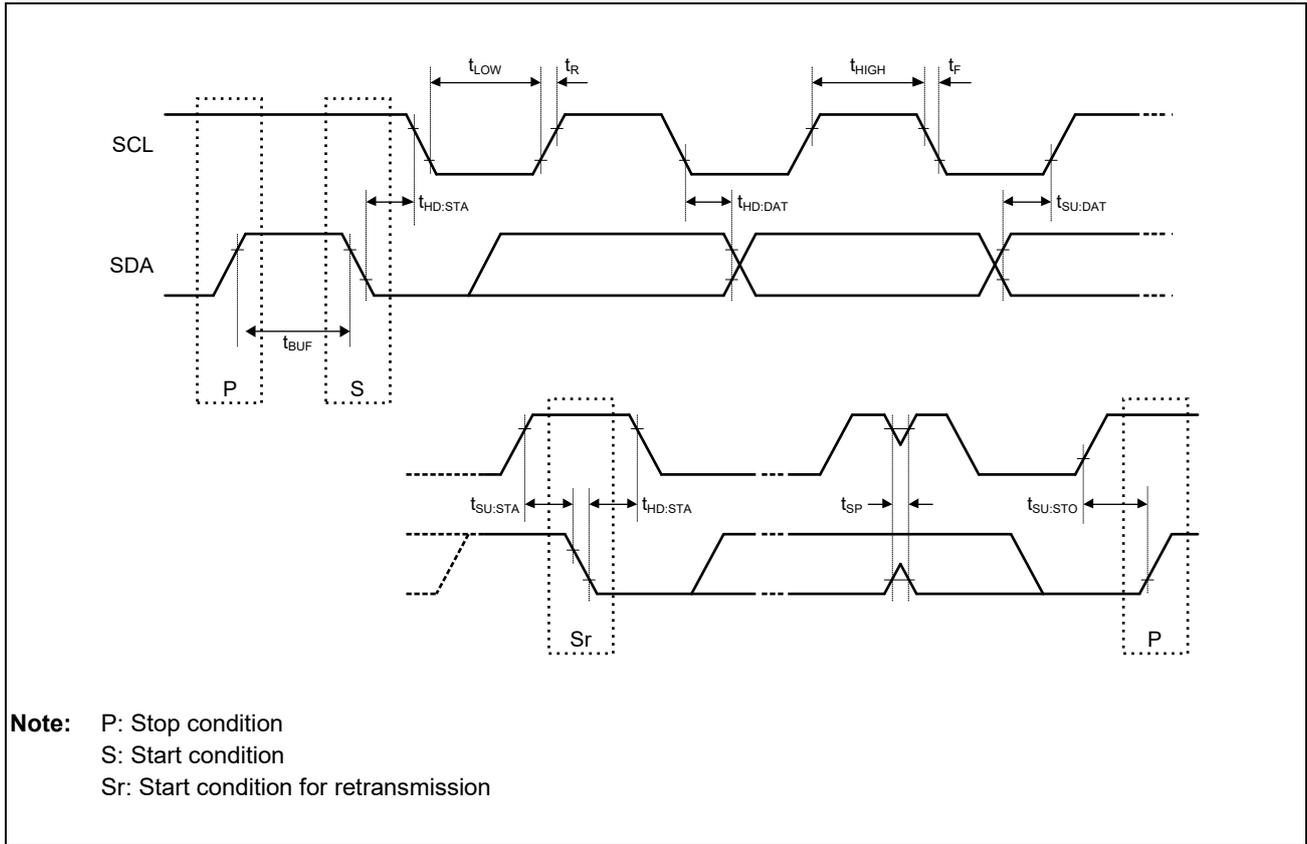


Figure 3.40 Input/Output Timing

### 3.5.15 Serial Communications Interface with FIFO (SCIFA) Access Timing

Table 3.42 SCIFA Timing

| Item                     |                          |                     | Symbol                         | Min.                           | Max. | Unit               | Figures            |
|--------------------------|--------------------------|---------------------|--------------------------------|--------------------------------|------|--------------------|--------------------|
| SCIFA                    | Input clock cycle        | Asynchronous        | $t_{Syc}$                      | 4                              | —    | $t_{p1cyc}^{*1}$   | <b>Figure 3.41</b> |
|                          |                          | Clocked synchronous |                                | 12                             | —    |                    |                    |
|                          | Input clock pulse width  |                     | $t_{SCKW}$                     | 0.4                            | 0.6  | $t_{p1cyc}^{*1}$   |                    |
|                          | Input clock rise time    |                     | $t_{SCKr}$                     | —                              | 5    | ns                 |                    |
|                          | Input clock fall time    |                     | $t_{SCKf}$                     | —                              | 5    | ns                 |                    |
|                          | Output clock cycle       | Asynchronous*2      | $t_{Syc}$                      | 8                              | —    | $t_{p1cyc}^{*1}$   |                    |
|                          |                          | Clocked synchronous |                                | 4                              | —    |                    |                    |
|                          | Output clock pulse width |                     | $t_{SCKW}$                     | 0.4                            | 0.6  | $t_{p1cyc}^{*1}$   |                    |
|                          | Output clock rise time   |                     | $t_{SCKr}$                     | —                              | 9    | ns                 |                    |
|                          | Output clock fall time   |                     | $t_{SCKf}$                     | —                              | 9    | ns                 |                    |
| Transmit data delay time | Internal clock           | $t_{TXD}$           | -10                            | 10                             | ns   | <b>Figure 3.42</b> |                    |
|                          | External clock           |                     | $3 \times t_{p1cyc}^{*1}$      | $4 \times t_{p1cyc}^{*1} + 20$ |      |                    |                    |
| Receive data setup time  | Internal clock           | $t_{RXS}$           | $3 \times t_{p1cyc}^{*1} + 20$ | —                              | ns   |                    |                    |
|                          | External clock           |                     | $t_{p1cyc}^{*1} + 10$          | —                              |      |                    |                    |
| Receive data hold time   | Internal clock           | $t_{RXH}$           | $-3 \times t_{p1cyc}^{*1}$     | —                              | ns   |                    |                    |
|                          | External clock           |                     | $2 \times t_{p1cyc}^{*1} + 10$ | —                              |      |                    |                    |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

Note 1.  $t_{p1cyc}$  indicates peripheral clock means SCIFn\_CLK\_PCK (P0φ) (n = 0 to 4).

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.

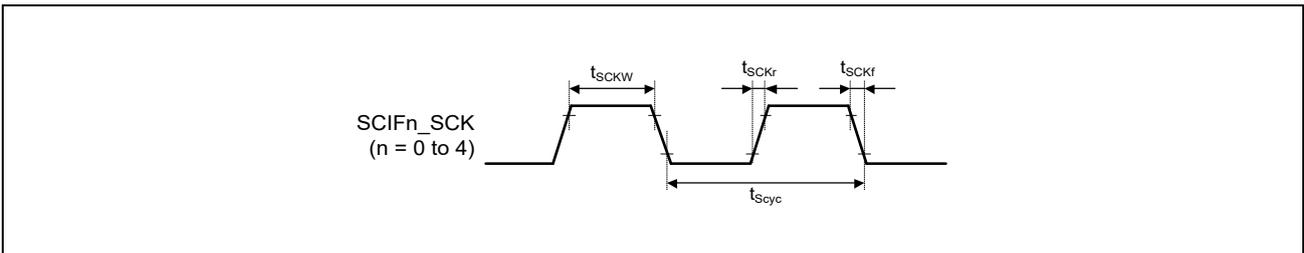


Figure 3.41 SCK Input Clock Timing

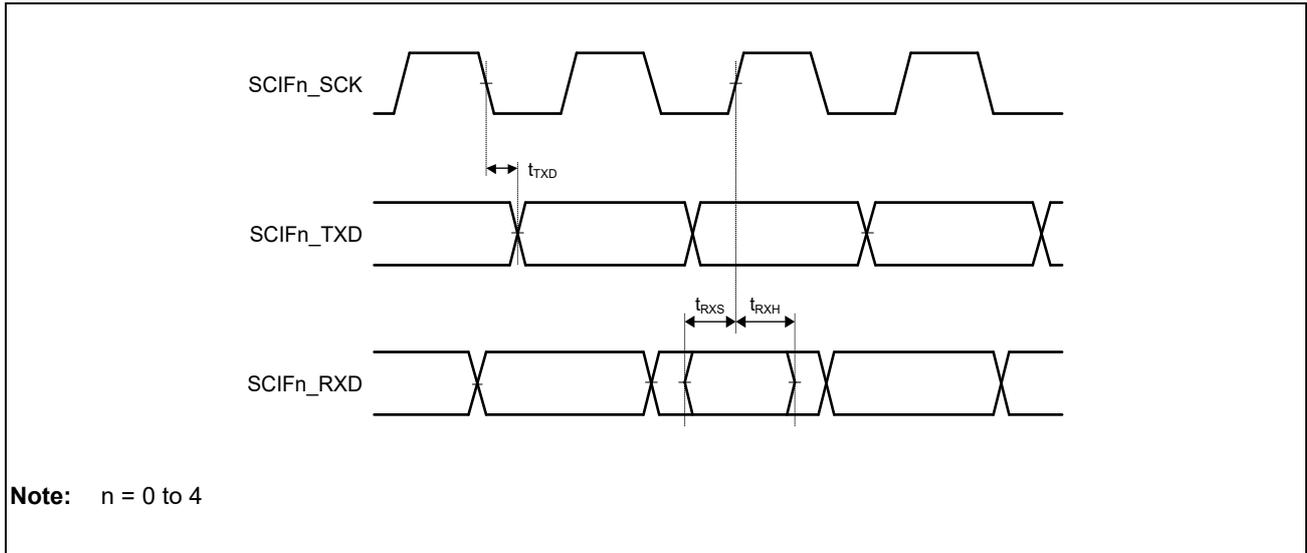


Figure 3.42 SCIFA Input/Output Timing in Clocked Synchronous Mode

### 3.5.16 Serial Communications Interface (SClG) Access Timing

Table 3.43 SClG Timing

| Item                     |                          | Symbol              | Min.       | Max. | Unit             | Figures            |                  |
|--------------------------|--------------------------|---------------------|------------|------|------------------|--------------------|------------------|
| SClG                     | Input clock cycle        | Asynchronous        | 4          | —    | $t_{p1cyc}^{*1}$ | <b>Figure 3.43</b> |                  |
|                          |                          | Clocked synchronous |            |      |                  |                    | 6                |
|                          | Input clock pulse width  |                     | $t_{SCKW}$ | 0.4  | 0.6              |                    | $t_{p1cyc}^{*1}$ |
|                          | Input clock rise time    |                     | $t_{SCKr}$ | —    | 5                |                    | ns               |
|                          | Input clock fall time    |                     | $t_{SCKf}$ | —    | 5                |                    | ns               |
|                          | Output clock cycle       | Asynchronous*2      | $t_{Syc}$  | 8    | —                |                    | $t_{p1cyc}^{*1}$ |
|                          |                          | Clocked synchronous |            |      |                  |                    |                  |
|                          | Output clock pulse width |                     | $t_{SCKW}$ | 0.4  | 0.6              |                    | $t_{p1cyc}^{*1}$ |
|                          | Output clock rise time   |                     | $t_{SCKr}$ | —    | 5                |                    | ns               |
|                          | Output clock fall time   |                     | $t_{SCKf}$ | —    | 5                |                    | ns               |
| Transmit data delay time | Clocked synchronous      | $t_{TXD}$           | —          | 28   | ns               | <b>Figure 3.44</b> |                  |
| Receive data setup time  | Clocked synchronous      | $t_{RXS}$           | 15         | —    | ns               |                    |                  |
| Receive data hold time   | Clocked synchronous      | $t_{RXH}$           | 5          | —    | ns               |                    |                  |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

Note 1.  $t_{p1cyc}$  indicates peripheral clock means SCl<sub>n</sub>\_CLKP (P0φ) (n = 0 to 1).

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.

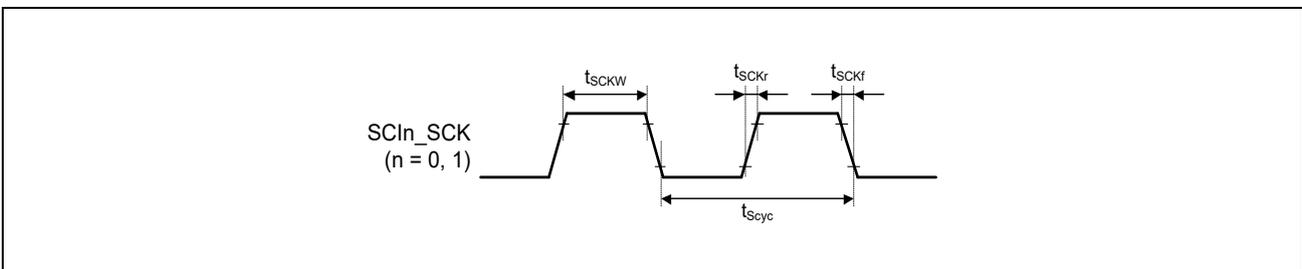


Figure 3.43 SCK Input Clock Timing

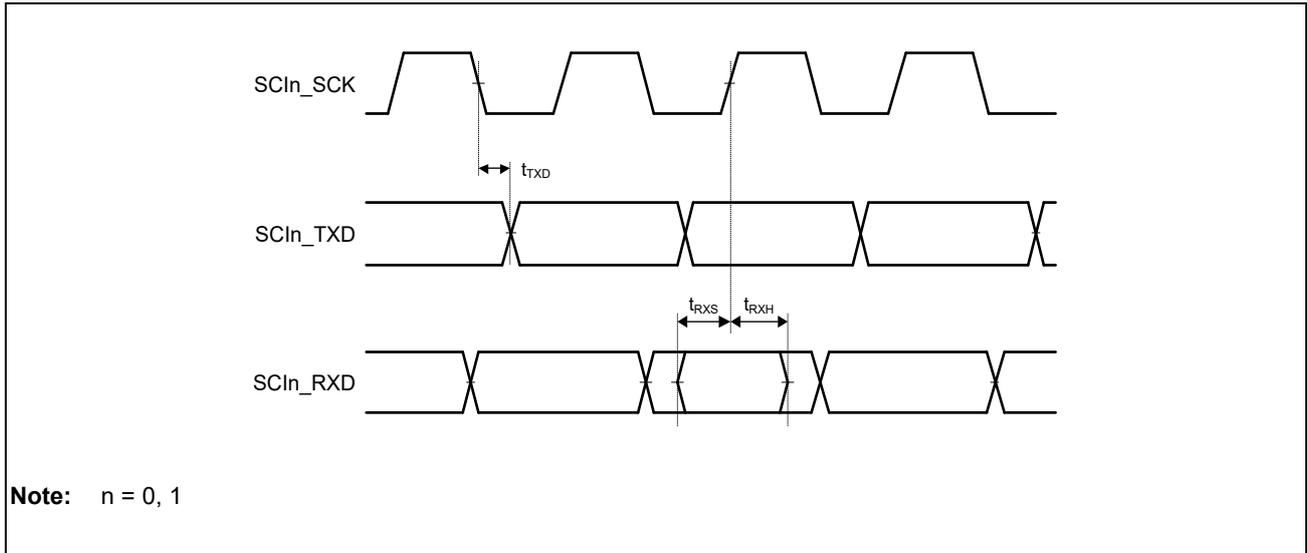


Figure 3.44 SCIFA Input/Output Timing in Clocked Synchronous Mode

### 3.5.17 Renesas Serial Peripheral Interface (RSPI) Access Timing

Table 3.44 Renesas Serial Peripheral Interface Timing

| Item                               |        | Symbol       | Min.                                    | Max.                                    | Unit             | Figure                     |
|------------------------------------|--------|--------------|---|---|------------------|----------------------------|
| RSPCK clock cycle                  | Master | $t_{SPcyc}$  | 2                                       | 4096                                    | $t_{p1cyc}^{*1}$ | Figure 3.45                |
|                                    | Slave  |              | 8                                       | 4096                                    |                  |                            |
| RSPCK clock high pulse width       | Master | $t_{SPCKWH}$ | 0.4                                     | —                                       | $t_{SPcyc}^{*1}$ | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 0.4                                     | —                                       |                  |                            |
| RSPCK clock low pulse width        | Master | $t_{SPCKWL}$ | 0.4                                     | —                                       | $t_{SPcyc}^{*1}$ | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 0.4                                     | —                                       |                  |                            |
| Data input setup time              | Master | $t_{SU}$     | 10                                      | —                                       | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 0                                       | —                                       | $t_{p1cyc}^{*1}$ |                            |
| Data input hold time               | Master | $t_H$        | 0                                       | —                                       | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 4                                       | —                                       | $t_{p1cyc}^{*1}$ |                            |
| SSL setup time                     | Master | $t_{LEAD}$   | $1 \times t_{SPcyc} - 20$               | $8 \times t_{SPcyc}$                    | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 4                                       | —                                       | $t_{p1cyc}^{*1}$ |                            |
| SSL hold time                      | Master | $t_{LAG}$    | $1 \times t_{SPcyc}$                    | $8 \times t_{SPcyc} + 20$               | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 4                                       | —                                       | $t_{p1cyc}^{*1}$ |                            |
| Data output delay time             | Master | $t_{OD}$     | —                                       | 19                                      | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | —                                       | 4                                       | $t_{p1cyc}^{*1}$ |                            |
| Data output hold time              | Master | $t_{OH}$     | 5                                       | —                                       | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | 2                                       | —                                       | $t_{p1cyc}^{*1}$ |                            |
| Continuous transmission delay time | Master | $t_{TD}$     | $1 \times t_{SPcyc} + 2 \times t_{cyc}$ | $8 \times t_{SPcyc} + 2 \times t_{cyc}$ | ns               | Figure 3.46 to Figure 3.49 |
|                                    | Slave  |              | $4 \times t_{cyc}$                      | —                                       |                  |                            |
| Slave access time                  |        | $t_{SA}$     | —                                       | 4                                       | $t_{p1cyc}^{*1}$ | Figure 3.48,               |
| Slave out release time             |        | $t_{REL}$    | —                                       | 3                                       | $t_{p1cyc}^{*1}$ | Figure 3.49                |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

Note 1.  $t_{p1cyc}$  indicates peripheral clock means RSPIn\_CLKB (P0φ) (0 to 2).

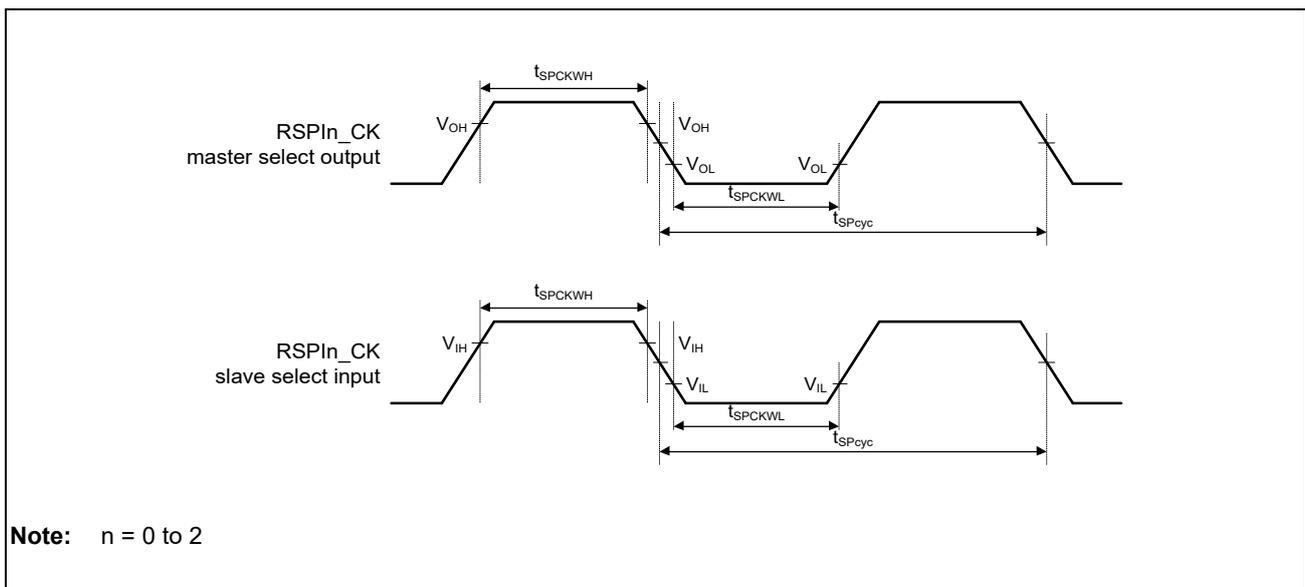


Figure 3.45 Clock Timing

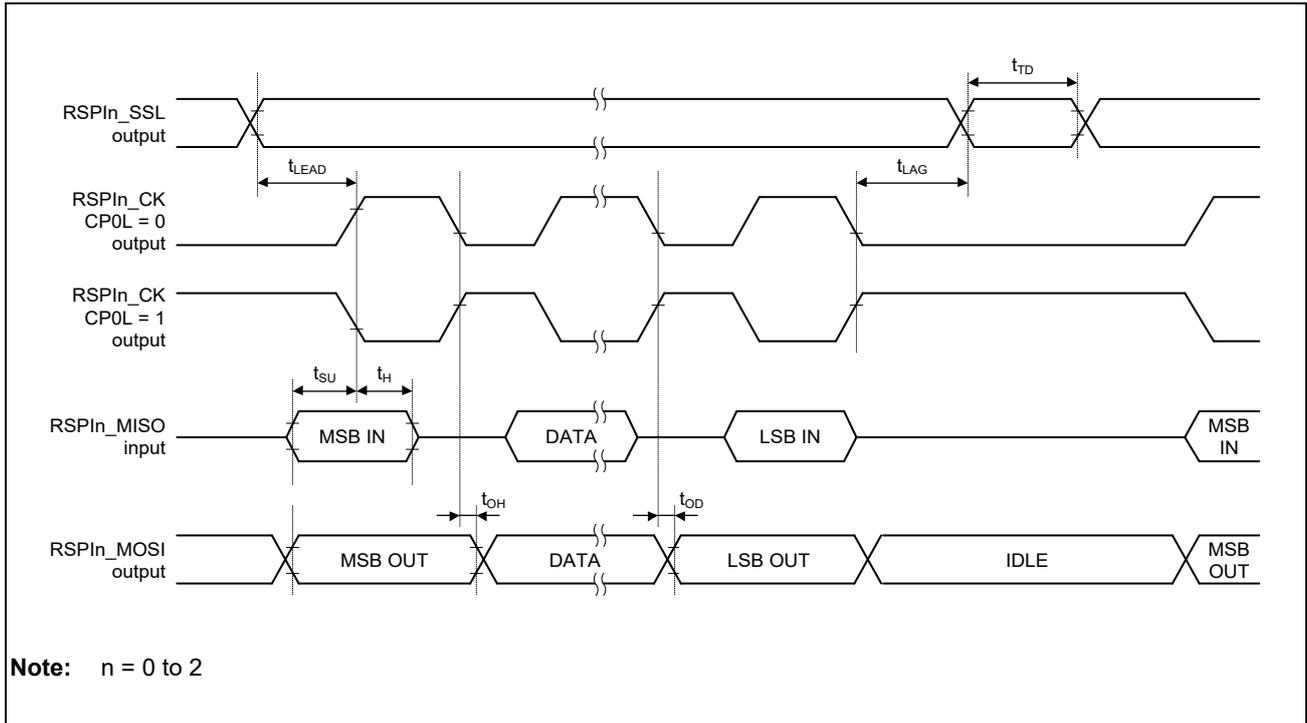


Figure 3.46 Transmission and Reception Timing (Master, CPHA = 0)

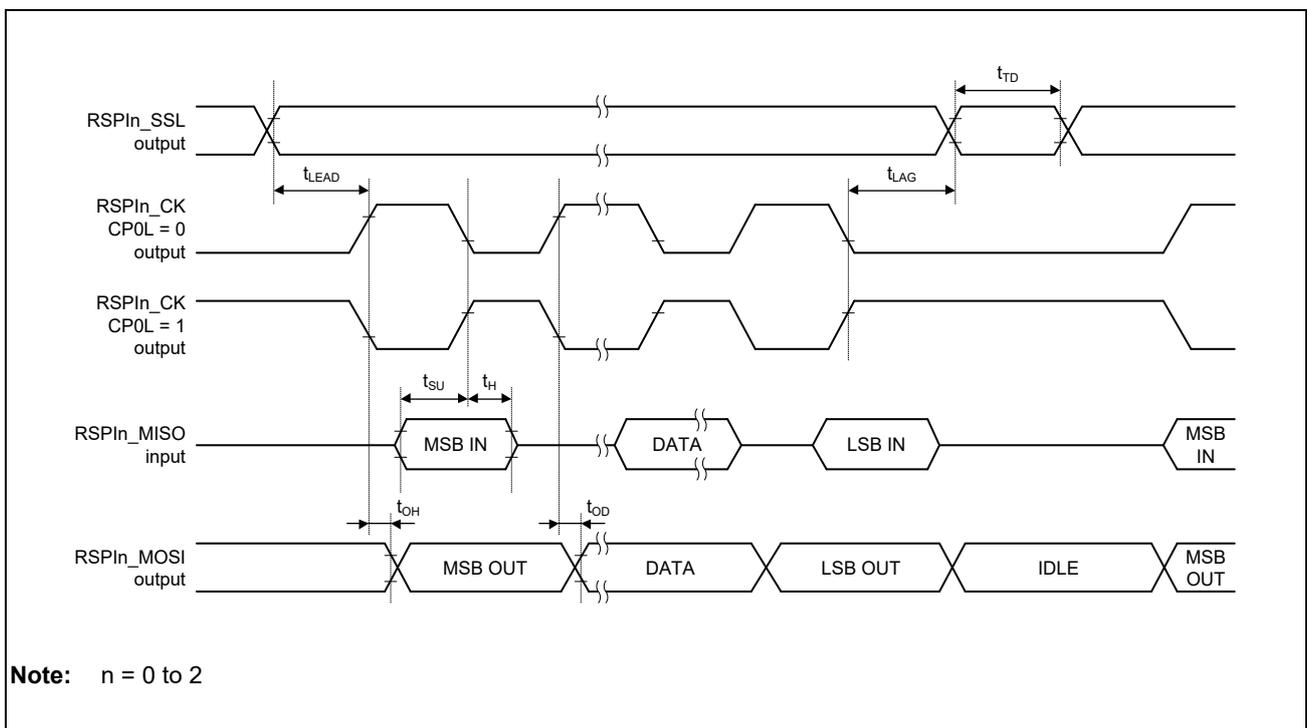


Figure 3.47 Transmission and Reception Timing (Master, CPHA = 1)

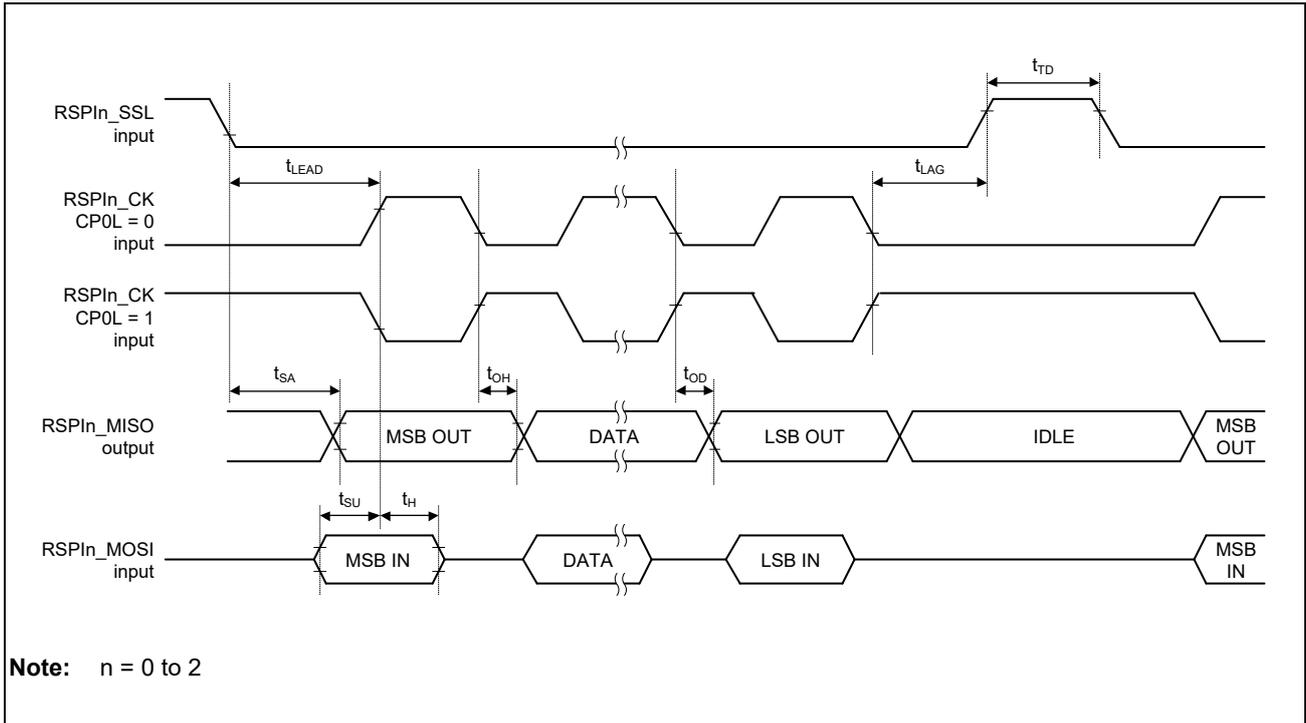


Figure 3.48 Transmission and Reception Timing (Slave, CPHA = 0)

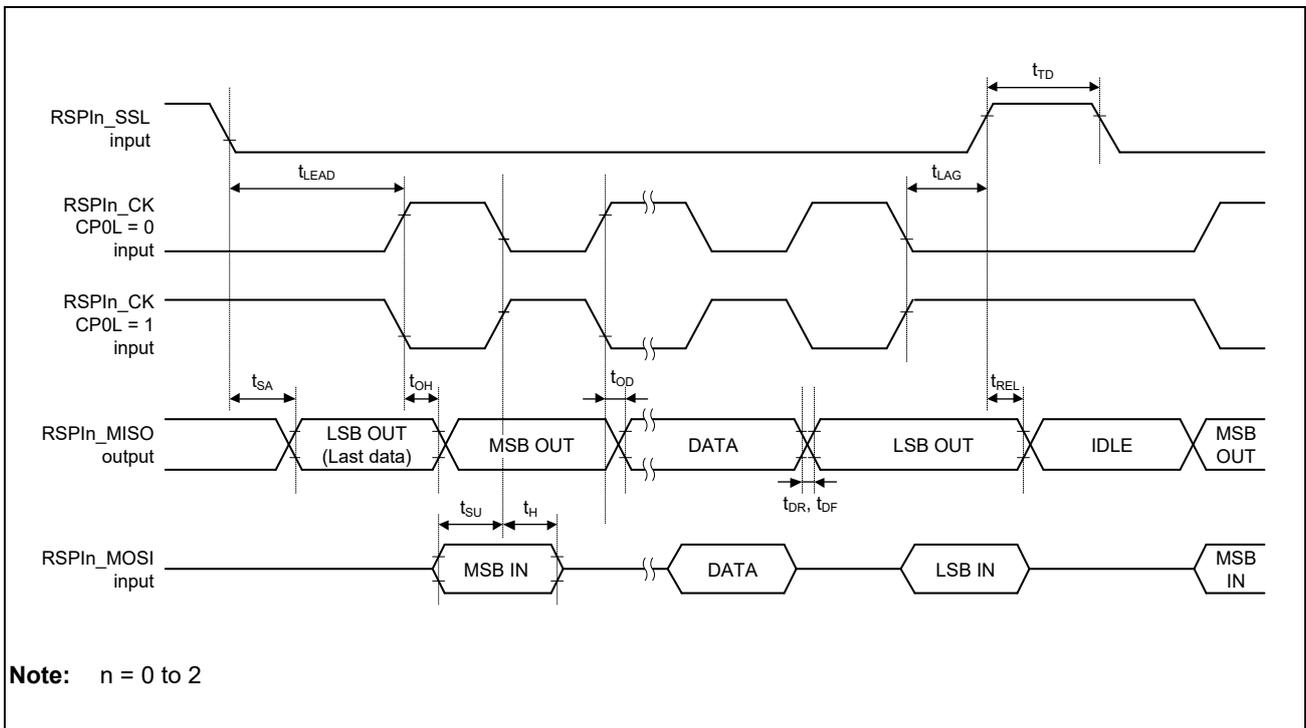


Figure 3.49 Transmission and Reception Timing (Slave, CPHA = 1)

### 3.5.18 A/D Converter Access Timing

Table 3.45 A/D Converter Timing

| Item                          | Symbol     | Min.  | Max. | Unit             | Figures            |
|-------------------------------|------------|-------|------|------------------|--------------------|
| ADC Trigger Input Pulse Width | $t_{TRGW}$ | 1.5*2 |      | $t_{P1cyc}^{*1}$ | <b>Figure 3.50</b> |

Note 1.  $t_{P1cyc}$  indicates peripheral clock means ADC\_ADCLK (TSU $\phi$ ).

Note 2. When a noise filter in ADC is off.

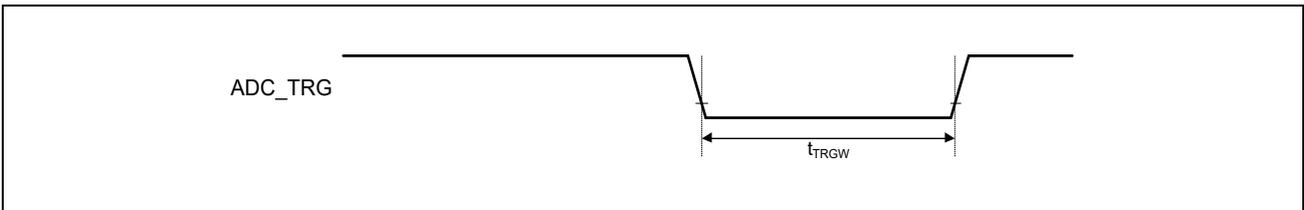


Figure 3.50 ADC Trigger Input Timing

### 3.5.19 Watchdog Timer Access Timing

Table 3.46 Watchdog Timer Timing

| Item                        | Symbol | Min. | Max. | Unit             | Figures            |
|-----------------------------|--------|------|------|------------------|--------------------|
| WDTOVF_PERROUT# Output Time | $t_L$  | 64   | 64   | $t_{P1cyc}^{*1}$ | <b>Figure 3.51</b> |

Note 1.  $t_{P1cyc}$  indicates peripheral clock means WDTn\_CLK (OSCCLK) (n = 0).

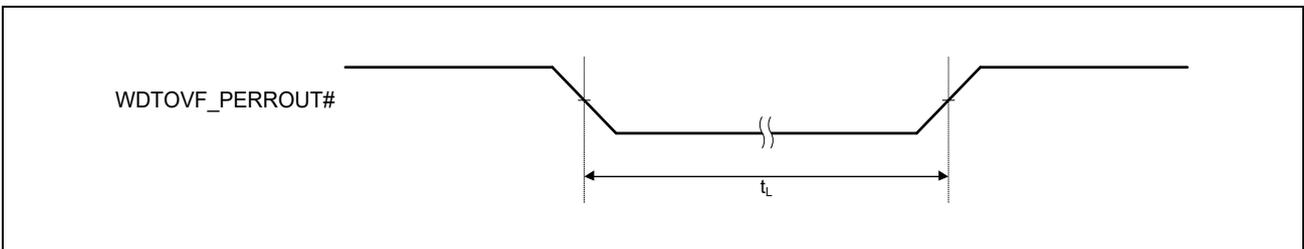


Figure 3.51 Watchdog Timer Output Timing

### 3.5.20 Octa Memory Controller Timing

Table 3.47 Octa Memory Controller Timing\*1,\*2

| Item                           | Symbol                     | Min.   | Max.  | Unit  | Figures                                     |                             |
|--------------------------------|----------------------------|--|---|---|---|-----------------------------|
| QSPIO_SPCLK clock frequency    | $f_{OCyc}$                 | —  | 100   | MHz   | Figure 3.52                                 |                             |
| QSPIO_SPCLK high pulse width   | $t_{OCwh}$                 | 0.475  | 0.525   | $t_{OCyc}$  |   |                             |
| QSPIO_SPCLK low pulse width    | $t_{OCwl}$                 | 0.475  | 0.525   | $t_{OCyc}$  |   |                             |
| QSPIO_SPCLK rise time          | $t_{OCr}$                  | —  | 1   | ns  |   |                             |
| QSPIO_SPCLK fall time          | $t_{OCf}$                  | —  | 1   | ns  |   |                             |
| OM_CS1#, QSPIO_SSL setup time  | SPI/SOPI                   | $t_{OCLEAD}$   | $1 \times t_{OCyc} - 3$<br>(Minimum register settings)    | $2.5 \times t_{OCyc} + 3$<br>(Maximum register settings)  | ns  | Figure 3.53,<br>Figure 3.54 |
|                                | DOPI                       | $t_{OCLEAD}$   | $0.75 \times t_{OCyc} - 3$<br>(Minimum register settings) | $2.25 \times t_{OCyc} + 3$<br>(Maximum register settings) | ns  | Figure 3.55                 |
| OM_CS1#, QSPIO_SSL hold time   | SPI/SOPI                   | $t_{OCLAG}$  | $1 \times t_{OCyc} - 3$<br>(Minimum register settings)    | $4.5 \times t_{OCyc} + 3$<br>(Maximum register settings)  | ns  | Figure 3.53,<br>Figure 3.54 |
|                                | DOPI read                  | $t_{OCLAG}$  | $3.25 \times t_{OCyc} - 3$<br>(Minimum register settings) | $4.25 \times t_{OCyc} + 3$<br>(Maximum register settings) | ns  | Figure 3.55                 |
|                                | DOPI write                 | $t_{OCLAG}$  | $0.75 \times t_{OCyc} - 3$<br>(Minimum register settings) | $4.25 \times t_{OCyc} + 3$<br>(Maximum register settings) | ns  |                             |
| Continuous transfer delay time | $t_{OCTD}$                 | $1 \times t_{OCyc} - 3$<br>(Minimum register settings) | $8.5 \times t_{OCyc} + 3$<br>(Maximum register settings)  | ns  | Figure 3.53,<br>Figure 3.54,<br>Figure 3.55 |                             |
| Data input setup time          | QSPIO_SPCLK base point     | $t_{SU}$   | 9.6   | —   | ns  | Figure 3.53                 |
| Data input hold time           |                            | $t_{H}$  | 0.5   | —   | ns  |                             |
| Data input setup time          | SOPI/DOPI DQS base point*3 | $t_{SU}$   | -0.7  | —   | ns  | Figure 3.54,<br>Figure 3.55 |
| Data input hold time           |                            | $t_{H}$  | 2.69  | —   | ns  |                             |
| Skew of Clock to Data Strobe   | $t_{CKDS}$                 | —  | 20  | ns  |   |                             |
| Data output delay time         | SPI/SOPI                   | $t_{OD}$   | —   | 1.4   | ns  | Figure 3.53,<br>Figure 3.54 |
| Data output hold time          |                            | $t_{OH}$   | -1.4  | —   | ns  |                             |
| Data output buffer off time    | SOPI                       | $t_{BOFF}$   | 2   | —   | ns  | Figure 3.54                 |
| Data output delay time         | DOPI*3                     | $t_{OD}$   | —   | 2.69  | ns  | Figure 3.55,<br>Figure 3.56 |
| Data output hold time          |                            | $t_{OH}$   | 0.9   | —   | ns  |                             |
| Data output buffer off time    | DOPI                       | $t_{BOFF}$   | 0.9   | —   | ns  | Figure 3.55                 |
| DQS refresh input setup time   | $t_{DQSS}$                 | 12   | —   | ns  | Figure 3.57                                 |                             |
| DQS refresh input hold time    | $t_{DQSH}$                 | $0.5 \times t_{OCyc}$                                  | —   | ns  |   |                             |

Note 1.  $t_{OCyc}$  indicates the QSPIO\_SPCLK cycle.

Note 2. Maximum load capacitance: 15 pF

Note 3. QSPIO\_SPCLK frequency: 100 MHz

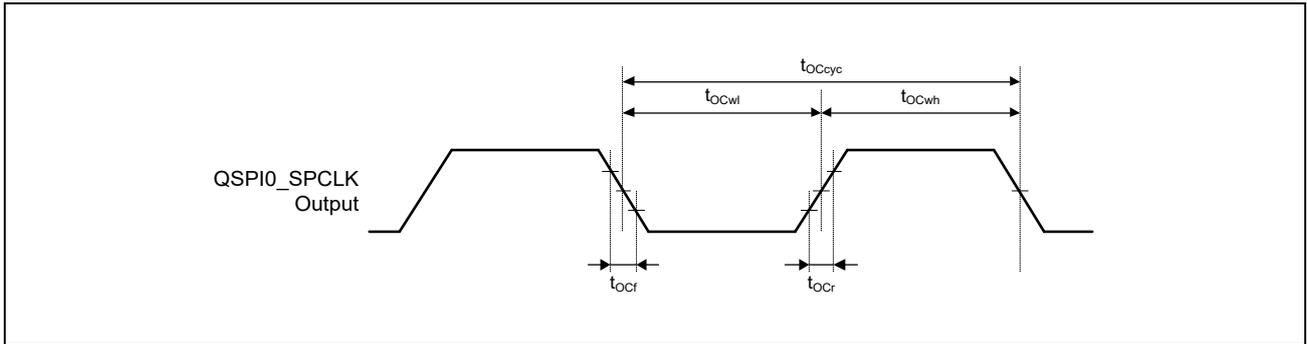


Figure 3.52 Clock Timing

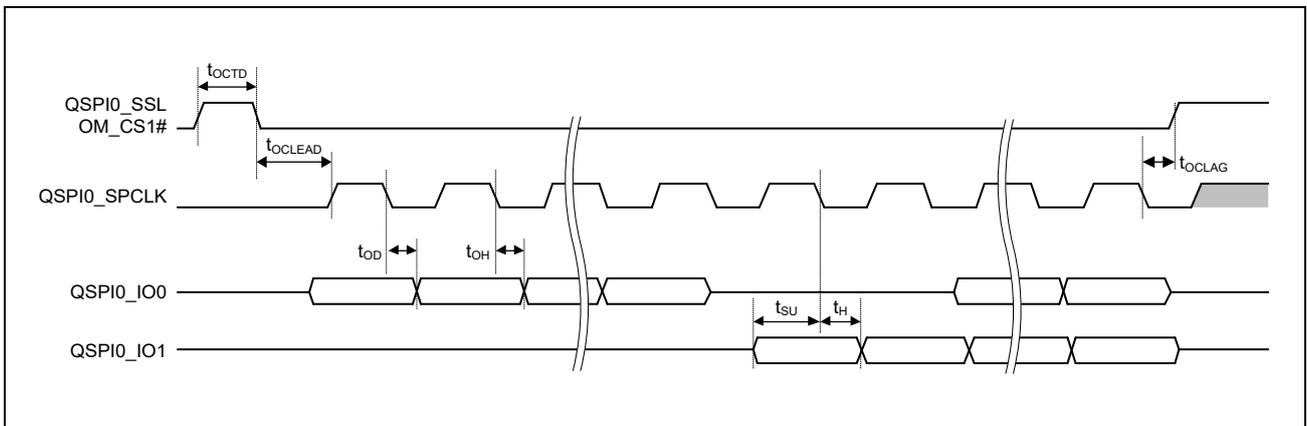


Figure 3.53 SPI Transferring Format Transmission and Receiving Timing

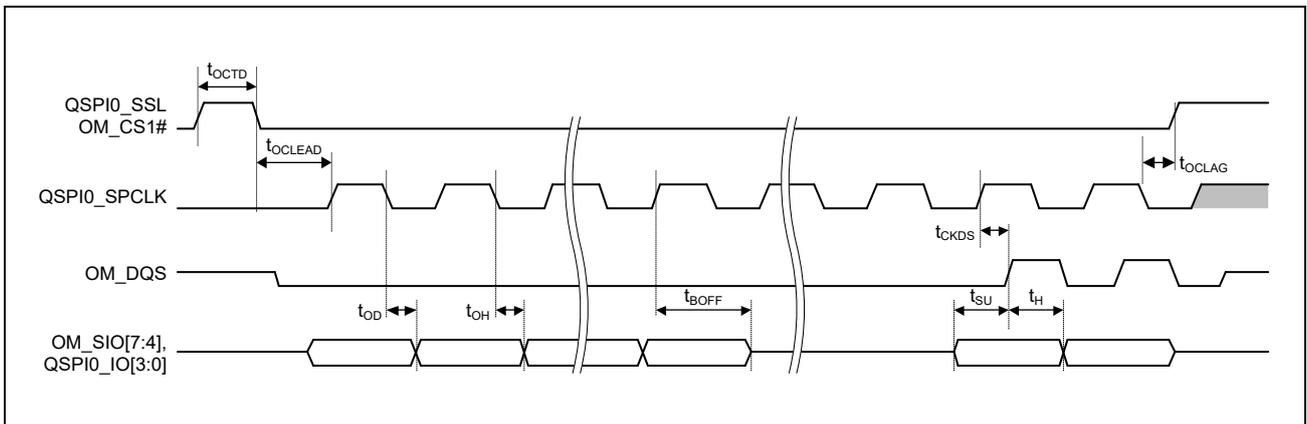


Figure 3.54 SOPI Transferring Format Transmission and Receiving Timing

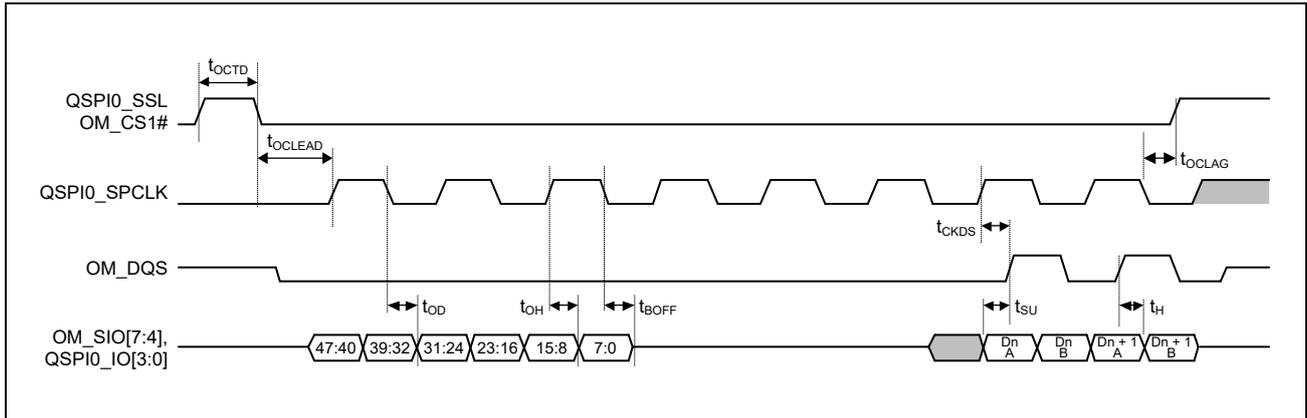


Figure 3.55 DOPI Transferring Format Transmission and Receiving Timing

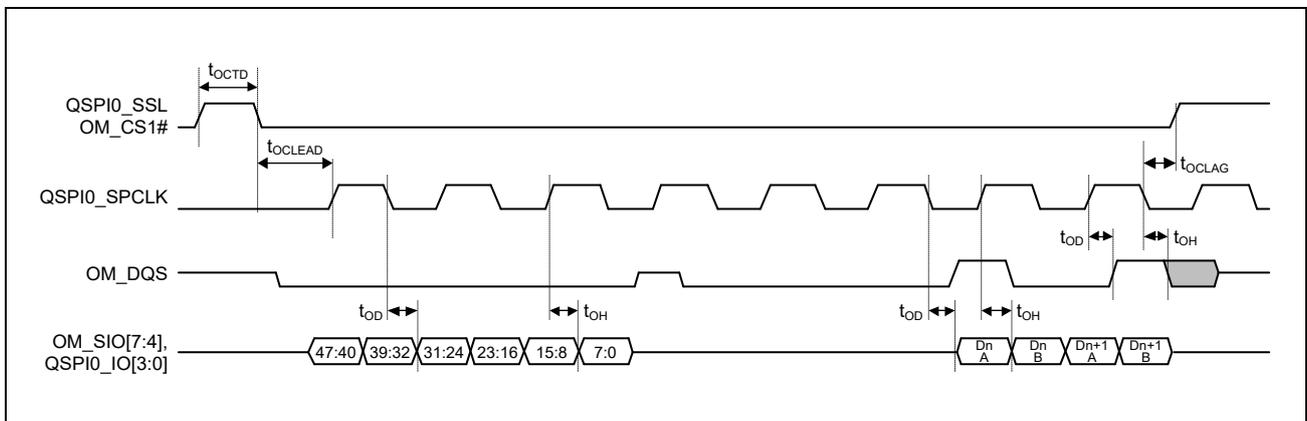


Figure 3.56 DOPI Transferring Format Transmission Timing

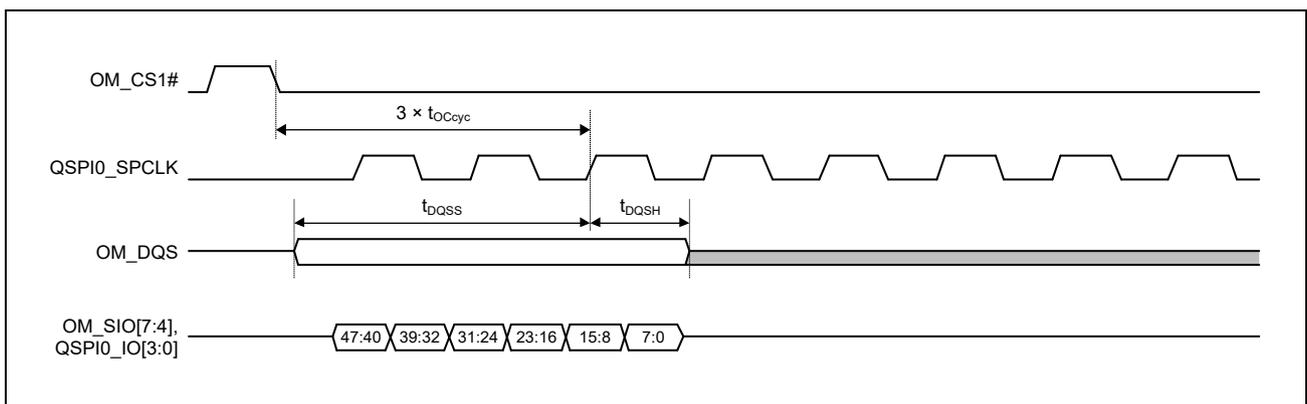
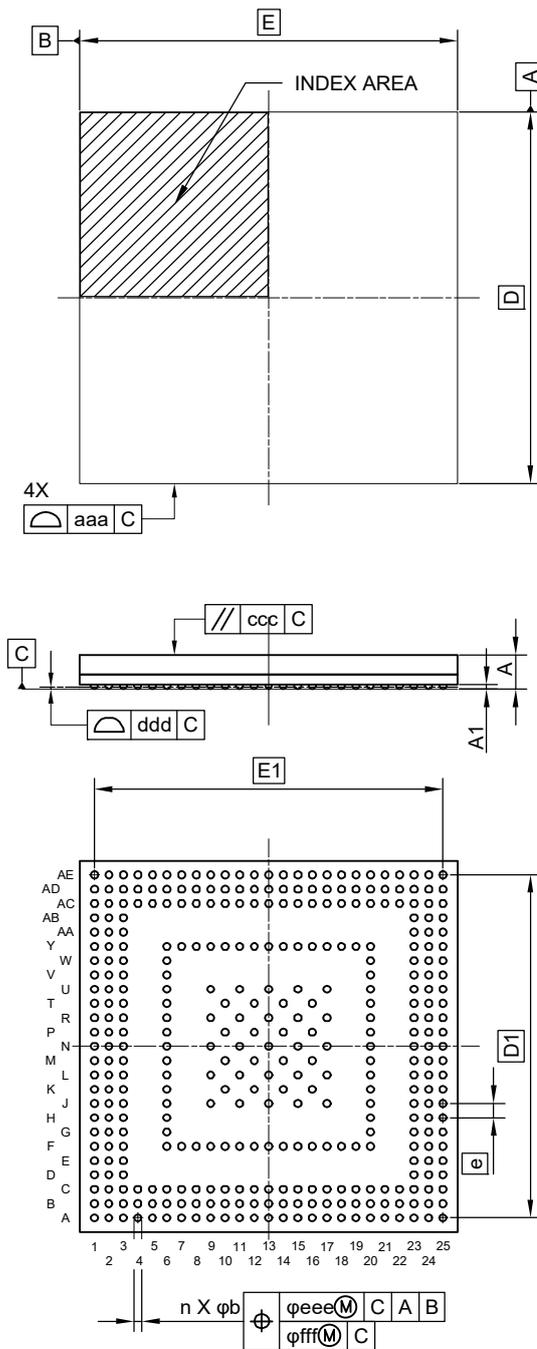


Figure 3.57 DQS Refresh Input Timing (OctaRAM Read and Write)

# 4. Package Dimensions

|                       |              |               |
|-----------------------|--------------|---------------|
| JEITA Package code    | RENESAS code | MASS(TYP.)[g] |
| P-LFBGA361-13x13-0.50 | PLBG0361KB-A | 0.40          |



| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min.                     | Nom.  | Max. |
| D                | —                        | 13.00 | —    |
| E                | —                        | 13.00 | —    |
| D1               | —                        | 12.00 | —    |
| E1               | —                        | 12.00 | —    |
| A                | —                        | —     | 1.40 |
| A1               | 0.11                     | —     | —    |
| b                | 0.20                     | 0.25  | 0.30 |
| e                | —                        | 0.50  | —    |
| aaa              | —                        | —     | 0.15 |
| ccc              | —                        | —     | 0.20 |
| ddd              | —                        | —     | 0.08 |
| eee              | —                        | —     | 0.15 |
| fff              | —                        | —     | 0.08 |
| n                | —                        | 361   | —    |

Figure 4.1 Package Dimensions for LFBGA 13 mm□/0.5 mm pitch/361 pin

|                  |                         |
|------------------|-------------------------|
| REVISION HISTORY | RZ/A3UL Group DATASHEET |
|------------------|-------------------------|

| Rev. | Date   | Description                   |  |
|------|--|-------------------------------|--|
|      |  | Page                          | Summary  |
| 1.00 | Dec 25, 2024   | —                             | First edition issued   |
| 1.10 | Jun 16, 2025   | 1. Overview                   |  |
|      |  | 2                             | 1.1.1 CPU Core<br>Boot: The description, modified (Note, modified)   |
|      |  | 12                            | Figure 1.1 Configuration of LSI Internal Bus<br>Text, modified (MPU Bus → MCPMU Bus)   |
|      |  | 3. Electrical Characteristics |  |
|      |  | 19                            | Table 3.3 DC Characteristics (1) [3.3-V I/O]<br>Input leakage current, added   |
|      |  | 20                            | Table 3.7 DC Characteristics (5) [RGMII/MII]<br>Input logic low (Remarks: 1.8-V RGMII/MII): The Min value, modified  |
|      |  | 21                            | Table 3.9 DC Characteristics (7) [1.8 V I/O (SD, QSPI)]<br>Output logic high voltage: The Min value, modified<br>Output logic low voltage: The Max value, modified   |
|      |  | 23                            | Table 3.18 DC Characteristics (16) [ADC]<br>Full-scale error, Offset error, Analog input capacitance, Analog input resistance, External capacitance, and External resistance, added<br>Note 1, added   |
|      |  | 24                            | Figure 3.4 Analog Input Equivalent Circuit, added  |
|      |  | 28                            | Table 3.21 SDHC AC Access Timing (SDR at 3.3-V Operation)<br>SD_CLK clock high level width, SD_CLK clock low level width, SD_CMD,SD_DATA output delay: The Min values, modified  |
|      |  | 29                            | Table 3.22 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)<br>SD0_CLK clock cycle, SD0_CLK clock high level width, SD0_CLK clock low level width, SD0_CMD/SDDAT output delay: The Min values, modified                                       |
|      |  | 29                            | Table 3.23 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)<br>SD0_CLK clock cycle, SD0_CLK clock high level width, SD0_CLK clock low level width: The Min values, modified<br>SD0_CMD/SDDAT output delay: The Min and Max values, modified   |
|      |  | 30                            | 3.5.3.2 eMMC host interface timing (HS-SDR), modified  |
|      |  | 31                            | Table 3.26 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)<br>SD0_CLK clock high level width, SD0_CLK clock low level width: The Min values, modified<br>SD0_CMD/SDDAT output delay: The Min and Max values, modified |
| 38   | Table 3.33 Ethernet-IF Access Timing (Ether RGMII)<br>Duty cycle for gigabit: The Min and Max values, modified<br>Note, modified |                               |  |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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