Features

This LSI has following features.

■ CPU

- Arm® Cortex®-A55, single-core

  Max. operating frequency: 1.1 GHz
- Arm® Cortex®-M33 core × 2

  Max. operating frequency: 250 MHz

  One core supports Floating Extension

■ Boot

- Selectable boot CPU from Arm® Cortex®-M33 or Arm® Cortex®-A55

■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (1-Mbyte on-chip SRAM with ECC)
- External DDR memory interface

  1-channel memory controller for DDR4-1600 or LPDDR4-1600 with a 16-bit bus width
- eXpanded Serial Peripheral Interface (xSPI) × 1 channel
- Octa memory controller × 1 channel

  OctaFlash™ and OctaRAM™ are supported
- SD card host interface × 3 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

■ Various communication/storage/network interfaces

- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- PCI Express Gen2 (1-lane, Root Complex only) [option]
- Gigabit Ethernet controller × 2 channels
- CANFD interface × 2 channels
- I^2C bus interface × 4 channels
- I3C bus interface × 1 channel
- Serial communication interface (SCI) × 2 channels
- Serial communication interface with FIFO (SCIF) × 6 channels
- Serial Peripheral Interface (RSPI) × 5 channels

■ Extended-function timers

- General PWM timer

  32-bit × 8 channels
- Multi-Function Timer Pulse Unit

  32-bit × 1 channel, 16-bit × 8 channels
- Realtime clock (RTC) × 1 channel

■ Audio

- Serial sound interface × 4 channels
- Pulse Density Modulated (PDM) interface × 3 channels
- SPDIF × 1 channel

■ Analog/Digital converter (ADC) and sensor

- 12-bit A/D converter × 8 channels
- Thermal Sensor Unit × 1 channel

■ Security

- Hardware cryptographic engine [option]
- On-The-Fly Decryption/Encryption (OTFDE) for external memory (DDR, xSPI, Octa)

1. Overview

1.1 Outline of Specification

1.1.1 CPU Core

Item	Description
System CPU Cortex-A55	• Arm Cortex-A55 Single Core 1.1 GHz • L1 I-cache: 32 Kbytes (Parity) / D-cache : 32 Kbytes (ECC) • L2 cache: Not included • L3 cache: 256 Kbytes (ECC) • NEON™ / FPU supported • Cryptographic Extension supported • Arm® v8.2-A architecture
System CPU Cortex-M33	• Arm Cortex-M33 Processor 250 MHz × 2 cores • Security Extension supported • Floating Extension supported*1 • Arm® v8-M architecture
Boot	• Bootable CPU: Cortex-A55, Cortex-M33*4 • Boot device: Boot Mode 0: Booting from eSD Boot Mode 1: Booting from eMMC Boot Mode 2: Booting from a serial flash memory (Single / Quad /Octal)*3 Boot Mode 3: Booting from SCIF download • Boot device voltage: 1.8 V*2, 3.3 V
Debug Interface	• Arm® CoreSight™ architecture • JTAG / SWD interface supported • ETF 16 Kbytes for program flow trace (each cluster) • JTAG Disable supported

Note 1. One core supports Floating Extension

Note 2. 1.8 V is supported in booting from eMMC and serial flash memory.

Note 3. A serial flash memory (Octal) is supported when Boot device voltage is 1.8 V.

Note 4. Cortex-M33 booting is supported from a serial flash memory and SCIF download.

1.1.2 CPU Peripheral

Item	Description
Clock Pulse Generator (CPG)	• Generates the clocks from external clock (EXCLK 24 MHz). Maximum Arm Cortex-A55 clock: 1.1 GHz Maximum Arm Cortex-M33 clock: 250 MHz Maximum DDR clock: 800 MHz (DDR4-1600 / LPDDR4-1600) Maximum AXI-bus clock: 200 MHz Maximum APB-bus clock: 100 MHz • SSC (Spread Spectrum Clock) supported
Direct Memory Access Controller (DMAC)	• 2 modules, 16 channels per module • Transfer request: On-chip peripheral request / auto request (software trigger) • A specific DMA transfer interval can be specified to adjust the bus occupancy. • LINK mode (DMA transfer under descriptor control) supported • Transfer information can be automatically reloaded
Interrupt Controller	• Arm® CoreLink™ Generic Interrupt Controller (GIC-600) for Arm Cortex-A55 • Nested Vectored Interrupt Controller (NVIC) for Arm Cortex-M33 • External Interrupt pins (NMI, IRQ7 to IRQ0, TINT31-0) • On-chip peripheral Interrupts: Priority level set for each module
Message Handling Unit (MHU)	• Message handling function between Arm Cortex-A55 and Arm Cortex-M33 • Assert interrupt to inform message and response from/to Arm Cortex-A55, Cortex-M33
General-purpose I/O (GPIO)	• General-purpose I/O ports
Thermal Sensor Unit (TSU)	• 1 channel

1.1.3 Internal Memory

Item	Description
On-chip RAM	• RAM of 1 Mbytes (ECC)

1.1.4 External Memory Interface

Item	Description
External Bus Controller for DDR4 / LPDDR4 SDRAM (DDR)	• Support DDR4-1600 / LPDDR4-1600 • Bus Width: 16-bit • In line ECC supported (Support error detection interrupt) • Memory Size: Up to 4 Gbytes (DDR4), 1 Gbytes (LPDDR4) • Auto Refresh / Self Refresh supported • On-The-Fly Decryption / Encryption supported
eXpanded Serial Peripheral Interface (xSPI)	• 1 channel • Up to 2 serial flash memories can be connected • Connectable with 2 Quad-SPI flash memories • Connectable with 2 Octal-SPI flash memories • Connectable with 2 Octal-RAMs • External address space read mode (built-in read cache) • SPI operation mode • Maximum Clock Frequency: 66 MHz (Single-SPI / Quad-SPI, SDR, 1.8 V / 3.3 V), 133 MHz (Octal-SPI / OctaFlash / OctaRAM, DDR, 1.8 V) • On-The-Fly Decryption / Encryption supported
Octa Memory Controller	• Macronix Serial Multi I/O (MXSMIO®) Octa Peripheral Interface (OPI) for high-end consumer applications is supported. • One each of an OctaFlash device and an OctaRAM device compliant with the OPI specifications are connectable. • A chip select signal is assigned to each memory device (OM_CS0#: OctaFlash; OM_CS1#: OctaRAM). • Supported device interfaces SPI: Serial peripheral interface (OctaFlash, SPI mode) SOPI: Single Octa I/O (8 bits) (OctaFlash, single data rate) DOPI: Double Octa I/O (8 bits) (OctaFlash and OctaRAM, double data rate) • On-The-Fly Decryption / Encryption supported
SD Card Host Interface / Multimedia Card Interface (SD/MMC)	• 3 channels • Channel 0 supports SDHI / e-MMC (boot supported) • Channel 1 and 2 support SDHI (Channel 1: Dedicated pin, Channel 2: Multiplexed pin, 3.3 V only) • SD memory I/O card interface (1-bit/4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD 3.0 • Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported • Error check function: CRC7 (Command/response), CRC16 (Data) • Card detection function, write protect supported • MMC interface (1-bit/4-bit/8-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 transfer modes supported (SD clock (SD_CLK) frequency: Up to 125 MHz)

1.1.5 Sound Interface

Item	Description
Serial Sound Interface (SSI)	• 4 channels bidirectional serial transfer • 2 external clock sources available • Full Duplex communication • Support of I2S / Monaural / TDM audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of 32-stage FIFO for transmission and reception • Support of LR-clock continue function in which the LR-clock signal is not stopped
Pulse Density Modulated (PDM) Interface	• 3 channels • Capable of filtering 1-bit digital input data PDM_DATn (n = 0,..,2) and converting them into 20-bit or 16-bit digital data. • Support of stereo microphone (L/R sampling by rising/falling clock edge). • Support of sound activity detector. • Support of programmable filters: 4th order sinc filter, high-pass filter (for suppression of DC bias), correction filter (for sinc passband distortion), half-band decimation filter (for aliasing distortion). • Internal buffer: Capable of storing voice data during low power mode
SPDIF	• Supports the IEC 60958 standard (stereo and consumer use modes only). • Supports sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz. • Supports audio word sizes of 16 to 24 bits per sample. • Biphase mark encoding. • Double buffered data. • Parity encoded serial data. • Simultaneous transmit and receive • Receiver autodetects IEC 61937 compressed mode data

1.1.6 Storage and Network

Item	Description
USB2.0 Host / Function (USB)	• 2 channels (ch0: Host-Function ch1: Host only) • Compliance with USB2.0 • Supports On-The-Go (OTG) Function • Supports Battery Charging Function • Internal dedicated DMA
Gigabit Ethernet Interface (GbE)	• 2 channels • Supports transfer at 1000 Mbps and 100 Mbps, 10 Mbps • Supports filtering of Ethernet frames • Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface) • Supports interface conforming to IEEE802.3 PHY MII (Media Independent Interface)
Controller Area Network Interface (CAN)	• 2 channels • CAN-FD ISO 11898-1 (CD2015) compliant • Up to 1 Mbps for arbitration phase and up to 8 Mbps for data phase • Message buffer – Up to 64 × 2-channel receive message buffer: Shared among all channels – 16 transmit message buffers per channel
PCI Express Gen2 (option)	• PCI Express Base Specification 4.0 compliant • PCI Express Gen1(2.5[GT/s])/Gen2(5.0[GT/s]) • Root Complex, Type1 Configuration Register • Lane implementation ×1 • Support Polarity inversion • Maximum data payload of 256 bytes, Maximum read request size 512 bytes • Not support for Virtual channels (support VC0 only) • Number of outstanding 1-8 • Dynamic control of speed/width up/down configuration • Not support for Clock Power Management (not support P1.CPM, P2.CPM) • Power Management (ASPM L1-Substate Support (Support Power Down Sequence only)) • Error handling/logging (AER Support) • Replay FIFO with ECC • Internal Memory without Parity • Number of Support Functions 1

1.1.7 Timer

Item	Description
Multi-function Timer Pulse Unit 3 (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Module clock frequency: 100 MHz • Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs • 14 types of count clocks selectable • Input capture function • 39 outputs compare and input capture registers • Counter clear operation (Simultaneous counter clearing by Compare match or Input capture is available) • Simultaneous writing to multiple timer counters (TCNT) • Synchronous input/output of each register due to synchronous operation of the counter • Buffered operation • Cascade-connected operation • 43 types of interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Phase counting mode – 16-bit mode (channel 1 and 2) – 32-bit mode (channel 1 and 2) • Counter function of dead time compensation • Digital filter functions for the input capture and external count clock pin
Port Output Enable 3 (POE3)	• Control of the high-impedance state of the MTU3a waveform output pins • Activation with four input pins • Activation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Activation by register write • Additional programming of output control target pins is possible.
General PWM Timer (GPT)	• 32 bits × 8 channels • Counting up or down (sawtooth wave), counting up and down (triangular wave) selectable for all channels • Independent selectable for each channel • 2 input/output pins per channel • 2 output compare / input capture registers per channel • For the 2 output compare / input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Synchronous start / stop / clear of counters on arbitrary channels • Starting, stopping, and clearing up/down counters in response to a maximum of eight events • Starting, stopping, and clearing up/down counters in response to input level comparison • Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers • Output pin invalidation functions due to dead time error or detection of short circuit between output pins • Digital filter functions for the input capture and external trigger pins
Port Output Enable for GPT (POEG)	• Output prohibition control of the GPT waveform output pin • Activation with up to four input pins • Activation by dead time error detection or output short detection • Activation by register write

Item	Description
Watchdog Timer (WDT)	• 3 channels • A counter overflow can reset the LSI • CPU parity error can reset the LSI
General Timer (GTM)	• 32 bits × 8 channels • Two operating modes – Interval timer mode – Free-running comparison mode
RTC	• Clock sources: 32 kHz clock (RTXIN) • Count mode: Calendar count mode / binary count mode • Interrupt sources: Alarm interrupt, periodic interrupt and carry interrupt • Time capture function

1.1.8 Peripheral Module

Item	Description
I2C Bus Interface (I2C)	• 4 channels (ch0,1 = Dedicated pin, ch2,3 = Multiplexed pin) • Master mode and slave mode supported • Support for 7-bit and 10-bit slave address formats • Support for multi-master operation • Timeout detection
I3C Bus Interface (I3C)	• 1 channel • Master (Main Master/Secondary Master) mode and Slave mode selectable • SDR (I3C Single Data Rate) Mode – Private Message – Broadcast Message (Common Command Code) – Direct Message (Common Command Code) • Legacy I2C Message – Fast-mode (Fm): Up to 400 kbit/s – Fast-mode Plus (Fm+): Up to 1 Mbit/s • Slave Interrupt Request • Master Ship Request (Secondary Master only) • Support for 7-bit slave address formats • Synchronous Timing Control – Sync Mode: Synchronous Basic Mode • Asynchronous Timing Control – Async Mode 0: Asynchronous Basic Mode – Async Mode 1: Asynchronous Advanced Mode • Error Detection
Serial Communication Interface with FIFO (SCIFA)	• 6 channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • Separate 16-byte FIFO registers for transmission and reception • Modem control function (channel 0, 1 and 2 in asynchronous mode)
Serial Communication Interface (SCIg)	• 2 channels • Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • LSB first / MSB first selectable • Modem control function • Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)
Renesas Serial Peripheral Interface (RSPI)	• 5 channels • SPI operation • Master mode and slave mode supported • Programmable bit length, clock polarity, clock phase can be selected • Consecutive transfers • LSB first / MSB first selectable

1.1.9 Security

Item	Description
Renesas Security IP (RSIP-E01B) [option]	• Security algorism – Common key encryption: AES (compliant with NIST FIPS PUB 197) – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-224, SHA-256 – Support of Unique ID
One Time Programmable memory (OTP)	• A nonvolatile memory that can be written only once • Security setting, authentication setting are possible • Support one time read function (128 bytes)
Battery Backup Function	• Realtime clock • Backup register • Tamper detection

1.1.10 Analog

Item	Description
A/D Converter (ADC)	• 8 channels • Resolution: 12-bit • Input Range: 0 V to 1.8 V • Conversion Time: 1.0 µs • Operation Mode: Select mode / scan mode • Conversion Mode: Single mode / repeat mode • Condition for A/D conversion start – Software trigger – Asynchronous trigger: External trigger supported – Synchronous trigger: MTU and PWM timer

1.1.11 Others

Item	Description
Boundary Scan	• Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

1.1.12 Power Supply Voltage

Item	Description
Power supply voltage	• VBATT_VDD: 1.50 to 1.95 V • VDD, PLL16_AVDD, PLL23_AVDD, PLL4_AVDD: 0.905 to 0.99 V • PVDD33: 3.0 to 3.6 V • PVDD18, ADC_AVDD18, OTP_AVDD18: 1.65 to 1.95 V • JTAG_PVDD: 1.65 to 1.95 V • XSPI_PVDD: 1.65 to 1.95 V / 3.0 to 3.6 V • I3C_PVDD: 1.1 to 1.3 V / 1.65 to 1.95 V • VDD_ISO, PCIE_VDD09: 0.905 to 0.99 V • SDn_PVDD (n = 0, 1): 1.65 to 1.95 V / 3.0 to 3.6 V • PVDD182533_n (n = 0, 1): 1.65 to 1.95 V / 2.3 to 2.7 V / 3.0 to 3.6 V • USB_VDD33: 3.0 to 3.6 V • USB_AVDD18, USB_VDD18, PCIE_VDD18: 1.65 to 1.95 V • DDR_VAA: 1.65 to 1.95 V • DDR_VDDQ: 1.06 to 1.17 V(LPDDR4) / 1.14 to 1.26 V (DDR4)

1.1.13 Temperature Range

Item	Description
Temperature range	• T_a: −40°C to +85°C*1 • T_j: −40°C to +125°C

Note 1. If wider temp is required than this range, use case has to be investigated.

1.1.14 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

1.1.15 Package

Item	Description
Package	• 361-pin LFBGA, 13-mm square, 0.5mm pitch (w/o PCIe) • 359-pin LFBGA, 14-mm square, 0.5mm pitch (w/ PCIe)

1.2 Block Diagram

The LSI internal bus of this LSI consists of the ACPU bus, MCPU bus, and system bus. **Figure 1.1** shows the configuration of the buses.

ACPU bus:

A bus connected to Cortex-A55, Cortex-M33_FPU, DDR memory controllers and Storage and Network

MCPU bus:

A bus connected to Cortex-M33 and serial interface units

System bus:

A bus connected to the control registers of each unit

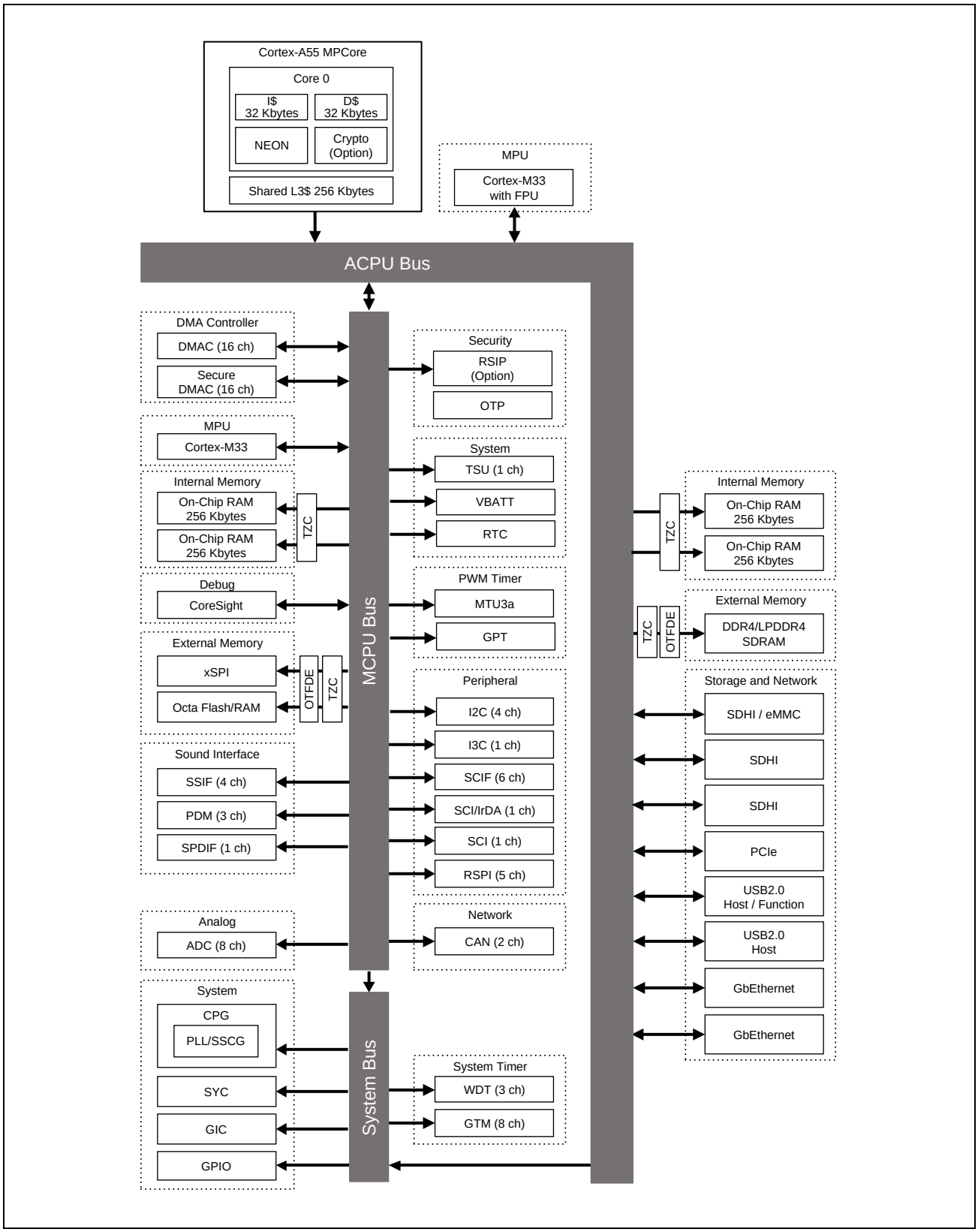


Figure 1.1 Configuration of LSI Internal Bus

1.3 Product Lineup

Table 1.1 Product Lineup

Group	Package	Part Number	CPU	Security	PCIe
RZ/G3S	14 mm BGA	R9A08G045S37GBG	1 × Cortex-A55, 2 × Cortex-M33	Available	Available
		R9A08G045S17GBG	1 × Cortex-A55, 1 × Cortex-M33*1		
		R9A08G045S33GBG	1 × Cortex-A55, 2 × Cortex-M33	Not supported	
		R9A08G045S13GBG	1 × Cortex-A55, 1 × Cortex-M33*1		
	13 mm BGA	R9A08G045S35GBG	1 × Cortex-A55, 2 × Cortex-M33	Available	Not supported
		R9A08G045S15GBG	1 × Cortex-A55, 1 × Cortex-M33*1		
		R9A08G045S31GBG	1 × Cortex-A55, 2 × Cortex-M33	Not supported	
		R9A08G045S11GBG	1 × Cortex-A55, 1 × Cortex-M33*1		

Note 1. Cortex-M33 without FPU is available.

2. Pin

This section describes the pins of this LSI.

2.1 Pin Assignment

Refer to attached excel file for the “ball view” about pin assignment of this LSI.
(Please double-click the icon on the right side)

2.2 External Pins and Multiplexed Functional Pins

Refer to attached excel file for the “pin function list” about information of external pins and multiplexed functional pins of this LSI.
(Please double-click the icon on the right side)

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power Supply voltage (0.94 V)		V_{DD}	−0.3 to +1.26	V
		$PLL16\_AV_{DD}$		
		$PLL23\_AV_{DD}$		
		$PLL4\_AV_{DD}$		
		V_{DD_ISO}		
		$PCIE\_V_{DD09}$		
Power Supply voltage (1.8 V)		$VBATT\_V_{DD}$	−0.3 to +2.5	V
		ADC_AV_{DD18}		
		OTP_AV_{DD18}		
		USB_AV_{DD18}		
		USB_V_{DD18}		
		$PCIE\_V_{DD18}$		
		DDR_V_{AA}		
Power Supply voltage (1.8 V)		PV_{DD18}	−0.3 to +2.45	V
		$JTAG\_PV_{DD}$		
Power Supply voltage (3.3 V)		PV_{DD33}	−0.3 to +4.1	V
		USB_V_{DD33}		
Power Supply Voltage (1.8 V/3.3 V switchable)		$XSPI\_PV_{DD}$	−0.3 to +2.45 (1.8 V mode)	V
		SDn_PV_{DD} (n = 0, 1)	−0.3 to +4.1 (3.3 V mode)	V
Power Supply Voltage (1.2 V/1.8 V switchable)		$I3C\_PV_{DD}$	−0.3 to +2.45 (1.8 V mode)	V
			−0.3 to +1.8 (1.2 V mode)	V
Power Supply Voltage (1.8 V/2.5 V/3.3 V switchable)		$PV_{DD182533\_n}$ (n = 0, 1)	−0.3 to +2.45 (1.8 V mode)	V
			−0.3 to +3.2 (2.5 V mode)	V
			−0.3 to +4.1 (3.3 V mode)	V
Power Supply Voltage (DDR)		DDR_V_{DDQ}	−0.3 to +1.68	V
Input voltage	3.3 V I/O input signal	—	−0.5 to 3.3 V power supply + 0.5	V
	2.5 V I/O input signal	—	−0.5 to 2.5 V power supply + 0.5	V
	1.8 V I/O input signal	—	−0.5 to 1.8 V power supply + 0.5	V
Operating temperature	Ambient temperature	T_a	−40 to +85*1	°C
	Junction temperature	T_j	−40 to +125	°C
Storage temperature	Ambient temperature	T_{stg}	−40 to +150	°C

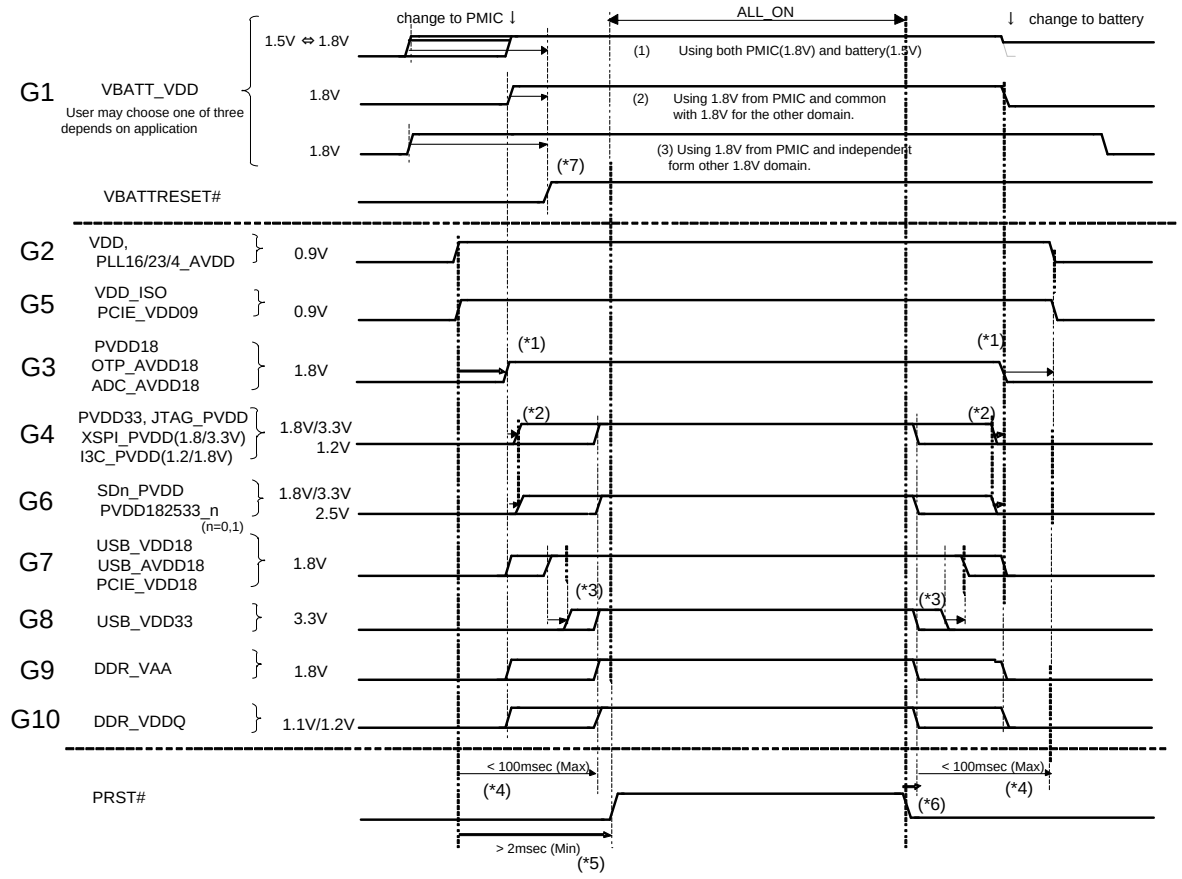
Note 1. If wider temp is required than this range, use case has to be investigated.

3.2 Power Supply

Table 3.2 Power Supply

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage (VBATT)	VBATT_V_{DD}	1.50	1.8	1.95	V	
Power Supply Voltage (Core)	V_{DD}	0.905	0.94	0.99	V	
Power Supply Voltage (PLL)	PLL16_AV_{DD}	0.905	0.94	0.99	V	
	PLL23_AV_{DD}	0.905	0.94	0.99	V	
	PLL4_AV_{DD}	0.905	0.94	0.99	V	
Power Supply Voltage (I/O)	PV_{DD33}	3.0	3.3	3.6	V	
	PV_{DD18}	1.65	1.8	1.95	V	
Power Supply Voltage (ADC/TSU)	ADC_AV_{DD18}	1.65	1.8	1.95	V	
Power Supply Voltage (OTP)	OTP_AV_{DD18}	1.65	1.8	1.95	V	
Power Supply Voltage (JTAG)	JTAG_PV_{DD}	1.65	1.8	1.95	V	
Power Supply Voltage (XSPI)	XSPI_PV_{DD}	1.65	1.8	1.95	V	1.8 V mode
		3.0	3.3	3.6	V	3.3 V mode
Power Supply Voltage (I3C)	I3C_PV_{DD}	1.65	1.8	1.95	V	1.8 V mode
		1.1	1.2	1.3	V	1.2 V mode
Power Supply Voltage (ISO)	V_{DD_ISO}	0.905	0.94	0.99	V	
Power Supply Voltage (SD)	SDn_PV_{DD}	1.65	1.8	1.95	V	1.8 V mode
	(n = 0, 1)	3.0	3.3	3.6	V	3.3 V mode
Power Supply Voltage (Ether)	$PV_{DD182533\_n}$	1.65	1.8	1.95	V	1.8 V mode
	(n = 0, 1)	2.3	2.5	2.7	V	2.5 V mode
		3.0	3.3	3.6	V	3.3 V mode
Power Supply Voltage (USB)	USB_V_{DD33}	3.0	3.3	3.6	V	
	USB_AV_{DD18}	1.65	1.8	1.95	V	
	USB_V_{DD18}	1.65	1.8	1.95	V	
Power Supply Voltage (PCIe)	PCIE_V_{DD18}	1.65	1.8	1.95	V	
	PCIE_V_{DD09}	0.905	0.94	0.99	V	
Power Supply Voltage (DDR)	DDR_V_{AA}	1.65	1.8	1.95	V	
	DDR_V_{DDQ}	1.14	1.2	1.26	V	DDR4 mode
		1.06	1.1	1.17	V	LPDDR4 mode

3.3 Power-On/Power-Off Sequence



Note 1. G3 must be powered on after G2, G5 and powered off before G2, G5. G3 and G7 may be powered on / off at the same time.

Note 2. G4, G6 must be powered on after G3 and powered off before G3.

Note 3. G8 must be powered on after G7 and powered off before G7.

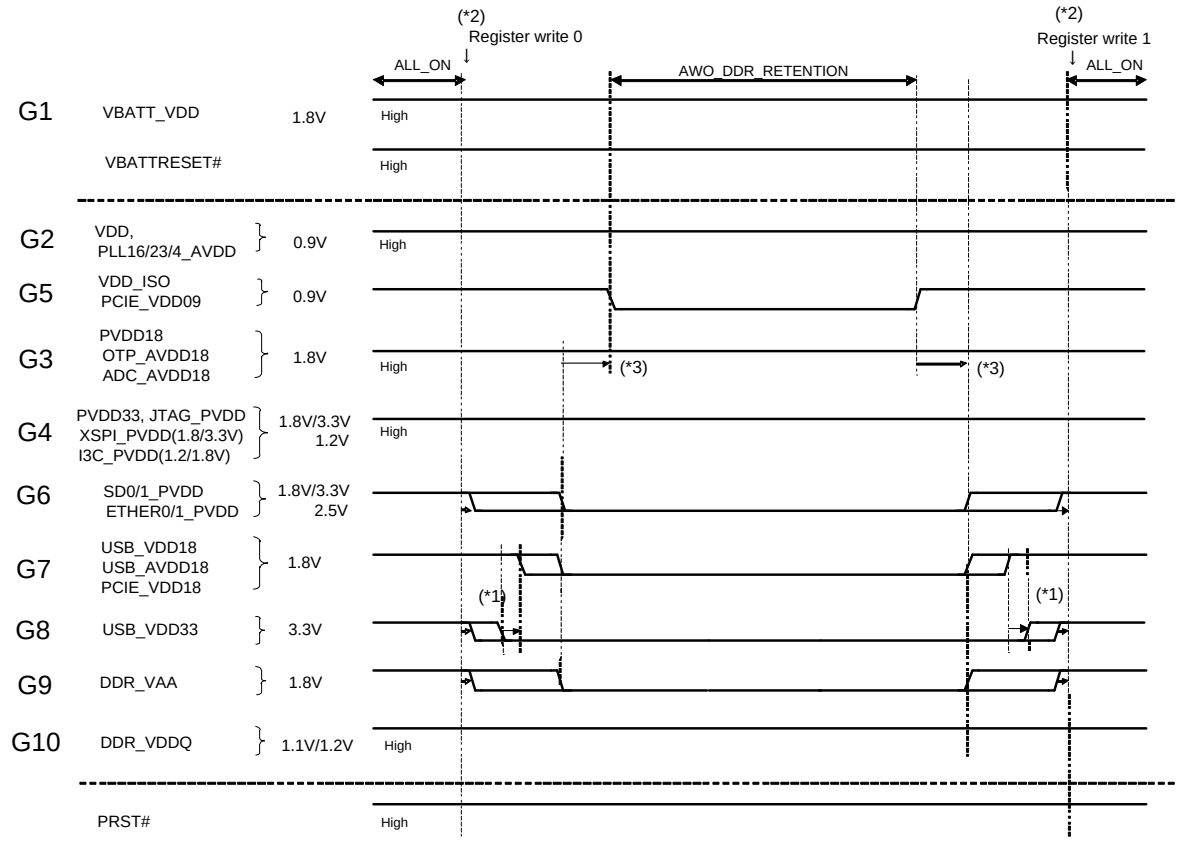
Note 4. It is recommended that all the power domains are powered on or off within approximately 100 msec.

Note 5. PRST# must be High after 2 msec from VDD (G2) power on.

Note 6. PRST# must be changed to Low before powered off.

Note 7. VBATTRESET# must be High after 50 µsec from VBATT_VDD (G1) power on.

Figure 3.1 Power-On/Power-Off Sequence 1 (All_OFF to ALL_ON, ALL_ON to ALL_OFF)

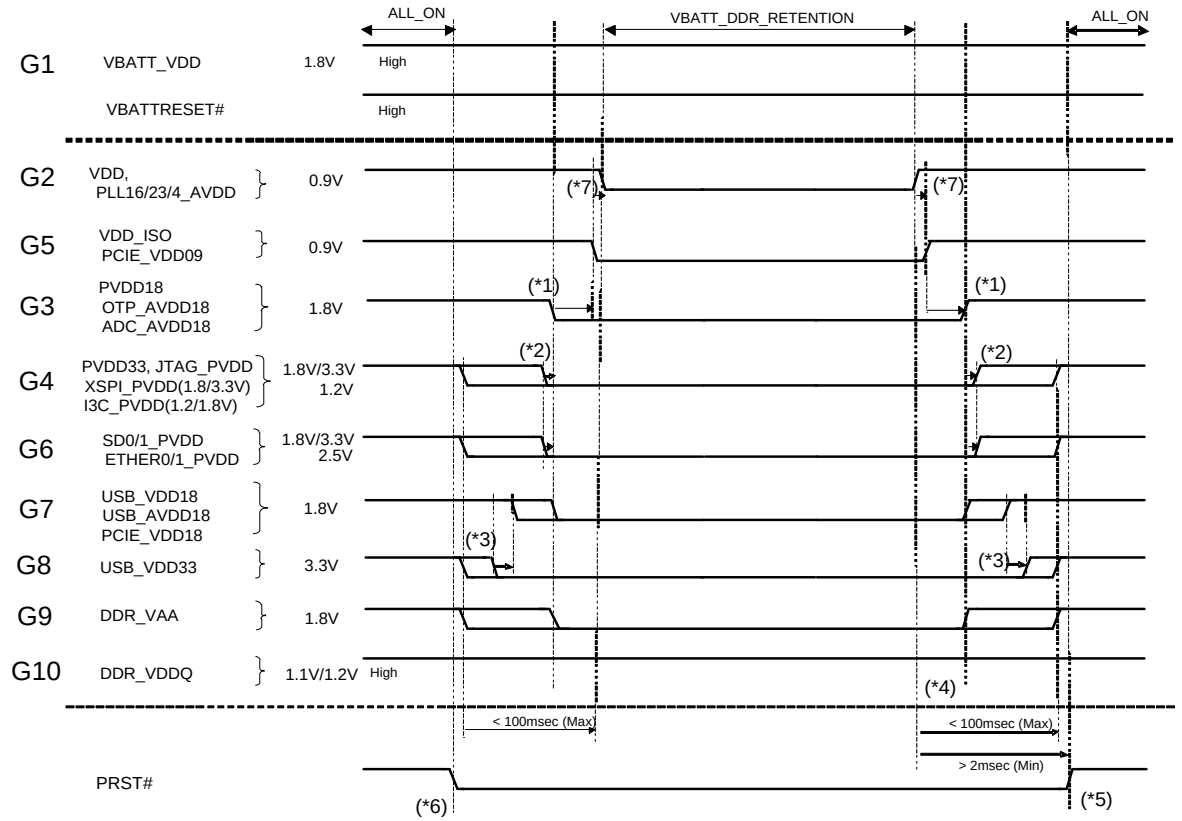


Note 1. G8 must be powered off before G7 and powered on after G7.

Note 2. The following registers must be written before G6, G7, G8, G9 are powered off or after G6, G7, G8, G9 are powered on.
- ISO_IOBUF_SE18_CTRL
- SYS_USB_PWRRDY
- CPG_RST_PCI (in CPG) or SYS_PCIE_RST_RSM_B (in SYSC)

Note 3. G5 must be powered off after G6 to G9 are powered off and powered on before G6 to G9 are powered on.

Figure 3.2 Power-On/Power-Off Sequence 2 (ALL_ON to AWO_DDR_RETENTION, AWO_DDR_RETENTION to ALL_ON)



Note 1. G3 must be powered off before G2, G5 and powered on after G2, G5. G3 and G7 can be powered on/off at the same time.

Note 2. G4, G6 must be powered off before G3 and powered on after G3.

Note 3. G8 must be powered off before G7 and powered on after G7.

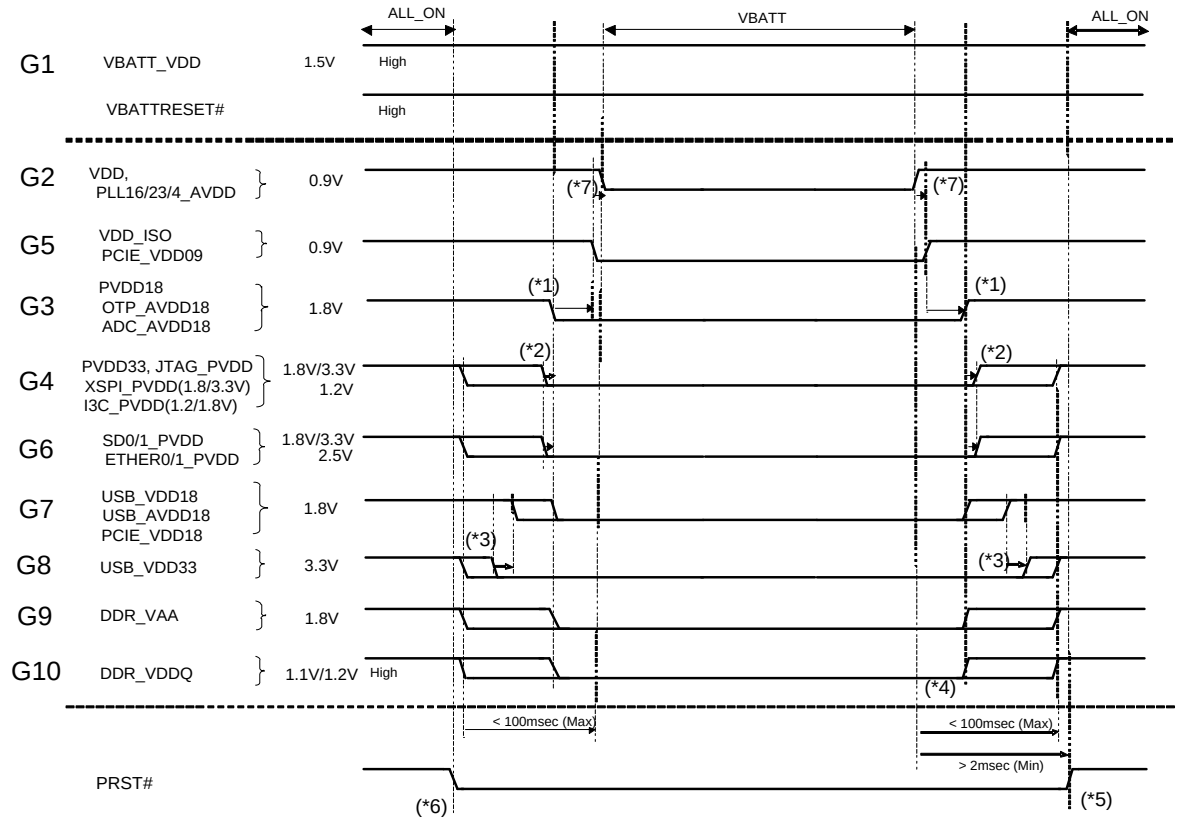
Note 4. It is recommended that all the power domains are powered on or off within approximately 100 msec.

Note 5. PRST# must be High after 2 msec from VDD (G2) power on.

Note 6. PRST# must be changed to Low before powered off.

Note 7. G5 must be powered off before G2 and powered on after G2.

Figure 3.3 Power-On/Power-Off Sequence 3 (ALL_ON to VBATT_DDR_RETENTION, VBATT_DDR_RETENTION to ALL_ON)



Note 1. G3 must be powered off before G2, G5 and powered on after G2, G5. G3 and G7 can be powered on/off at the same time.

Note 2. G4, G6 must be powered off before G3 and powered on after G3.

Note 3. G8 must be powered off before G7 and powered on after G7.

Note 4. It is recommended that all the power domains are powered on or off within approximately 100 msec.

Note 5. PRST# must be High after 2 msec from VDD (G2) power on.

Note 6. PRST# must be changed to Low before powered off.

Note 7. G5 must be powered off before G2 and powered on after G2.

Figure 3.4 Power-On/Power-Off Sequence 4 (ALL_ON to VBATT, VBATT to ALL_ON)

3.4 DC Characteristics

Table 3.3 DC Characteristics (1) [GP I/O (3.3 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	2	—	—	V	
Low-level input voltage		V_{IL}	—	—	0.8	V	
Hysteresis threshold ↑		V_T+	2.1	—	—	V	
Hysteresis threshold ↓		V_T-	—	—	0.7	V	
Output logic high voltage	(I_{OH} = –1.9 mA)	V_{OH}	V_{CCQ} – 0.4	—	—	V	
	(I_{OH} = –4 mA)						
	(I_{OH} = –8 mA)						
	(I_{OH} = –9 mA)						
Output logic low voltage	(I_{OL} = 1.9 mA)	V_{OL}	—	—	0.4	V	
	(I_{OL} = 4 mA)						
	(I_{OL} = 8 mA)						
	(I_{OL} = 9 mA)						
Weak pull-up resistor (input mode)		R_{UP}	10 K	50 K	90 K	Ω	
Weak pull-down resistor (input mode)		R_{DN}	10 K	50 K	90 K	Ω	
Input leakage current		I_{LI}	—	—	10	µA	0V ≤ V_{in} ≤ PV_{DD33} In case of 3state buffer, the leak current when output mode OFF

Note: V_{in} means input voltage of external input pin.

Table 3.4 DC Characteristics (2) [SD I/O (1.8/3.3 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	V_{DDQ} × 0.625	—	—	V	3.3 V mode
Low-level input voltage		V_{IL}	—	—	V_{DDQ} × 0.25	V	
Output logic high voltage	(I_{OH} = –4 mA)	V_{OH}	V_{CCQ} – 0.4	—	—	V	
	(I_{OH} = –6 mA)						
	(I_{OH} = –8 mA)						
	(I_{OH} = –9 mA)						
Output logic low voltage	(I_{OL} = 4 mA)	V_{OL}	—	—	0.4	V	
	(I_{OL} = 6 mA)						
	(I_{OL} = 8 mA)						
	(I_{OL} = 9 mA)						
High-level input voltage		V_{IH}	1.27	—	—	V	1.8 V mode
Low-level input voltage		V_{IL}	—	—	0.58	V	
Output logic high voltage	(I_{OH} = –7 mA)	V_{OH}	V_{CCQ} – 0.45	—	—	V	
	(I_{OH} = –8 mA)						
	(I_{OH} = –9 mA)						
	(I_{OH} = –10 mA)						
Output logic low voltage	(I_{OL} = 7 mA)	V_{OL}	—	—	0.45	V	
	(I_{OL} = 8 mA)						
	(I_{OL} = 9 mA)						
	(I_{OL} = 10 mA)						
Weak pull-up resistor (input mode)		R_{UP}	10 K	50 K	90 K	Ω	3.3 V/1.8 V mode
Weak pull-down resistor (input mode)		R_{DN}	10 K	50 K	90 K	Ω	

Table 3.5 DC Characteristics (3) [RGMII (1.8/2.5/3.3 V)]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage	V_{IH}	V_{CCQ} × 0.65	—	—	V	3.3 V mode
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.35	V	
Output logic high voltage	V_{OH}	V_{CCQ} – 0.4	—	—	V	
Output logic low voltage	V_{OL}	—	—	0.4	V	
High-level input voltage	V_{IH}	1.7	—	—	V	2.5 V mode
Low-level input voltage	V_{IL}	—	—	0.7	V	
Output logic high voltage	V_{OH}	V_{CCQ} – 0.4	—	—	V	
Output logic low voltage	V_{OL}	—	—	0.4	V	
High-level input voltage	V_{IH}	V_{CCQ} × 0.65	—	—	V	1.8 V mode
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.35	V	
Output logic high voltage	V_{OH}	V_{CCQ} – 0.45	—	—	V	
Output logic low voltage	V_{OL}	—	—	0.45	V	

Table 3.6 DC Characteristics (4) [I3C (1.2/1.8 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.8 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I3C Open Drain mode
Output logic low voltage	IOL = 3 mA	V_{OL}	—	—	0.27	V	
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.8 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I2C Open Drain mode*1
Output logic low voltage	IOL = 20 mA	V_{OL}	—	—	0.4	V	
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.8 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I3C CMOS mode
Output logic high voltage	IOL= −3 mA	V_{OH}	V_{CCQ} − 0.27	—		V	
Output logic low voltage	IOL= 3 mA	V_{OL}	—	—	0.27	V	
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.2 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I3C CMOS mode
Output logic high voltage	IOL = −2 mA	V_{OH}	V_{CCQ} − 0.18	—		V	
Output logic low voltage	IOL = 2 mA	V_{OL}	—	—	0.18	V	

Note 1. fast-mode, fast-mode plus

Table 3.7 DC Characteristics (5) [I2C (1.8 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	
Output logic low voltage	IOL = 20 mA	V_{OL}	—	—	0.4	V	

Table 3.8 DC Characteristics (6) [Input (Schmitt/1.8 V)]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage	V_{IH}	V_{CCQ} × 0.75	—	—	V	
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.25	V	

Table 3.9 DC Characteristics (7) [Input (3.3 V tolerant/Schmitt)]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage	V_{IH}	V_{CCQ} × 0.75	—	—	V	
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.25	V	

Table 3.10 DC Characteristics (8) [USB 2.0]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input levels for low/full speed						
High (driven)	V_{IH}	2.0	—	—	V	
Low	V_{IL}	—	—	0.8	V	
Differential input sensitivity	V_{DI}	0.2	—	—	V	
Differential common mode range	V_{CM}	0.8	—	2.5	V	
Input levels for high speed						
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}	100	—	150	mV	
High-speed data signaling common mode voltage range (guideline for receiver)	V_{HSCM}	−50	—	500	mV	
Output levels for low/full speed						
Low	V_{OL}	0.0	—	0.3	V	
High (driven)	V_{OH}	2.8	—	3.6	V	
Output signal crossover voltage	V_{CRS}	1.3	—	2.0	V	
Output levels for high-speed						
High-speed idle level	V_{HSOI}	−10.0	—	10.0	mV	
High-speed data signaling high	V_{HSOH}	360	—	440	mV	
High-speed data signaling low	V_{HSOL}	−10.0	—	10.0	mV	
Chirp J level (differential voltage)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K level (differential voltage)	V_{CHIRPK}	−900	—	−500	mV	

Table 3.11 DC Characteristics (9) [ADC]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Resolution	—	—	12	—	Bit	
Analog input channel	—	—	—	8	Channel	
Analog input range	AIN	V_{SS}	—	ADC_AV_{DD18}	V	
Differential non-linearity	DNL	—	—	±3.0	LSB	
Integral non-linearity	INL	—	—	±6.0	LSB	
Full-scale error	—	—	±10	±20	LSB	
Offset error	—	—	±10	±20	LSB	
Analog input capacitance	C_{IN}	—	—	6.9	pF	
Analog input resistance	R_{IN}	—	—	1733	Ω	
External capacitance	C_{EXT}	—	—	(*1)	pf	
External resistance	R_{EXT}	—	—	(*1)	Ω	

Note 1. Refer to **Figure 3.5** for Cext and Rext.
The Cext and Rext need to satisfy the sampling time.
A/D conversion time = sampling time (71T to 255T) + 29T.
T stands for the cycle of ADIVCLK (100 MHz).
If A/D conversion is performed with the minimum conversion time, the sampling time must be 71T.
(Minimum conversion time per channel is 1 µs when A/D conversion clock ADIVCLK is 100 MHz.)

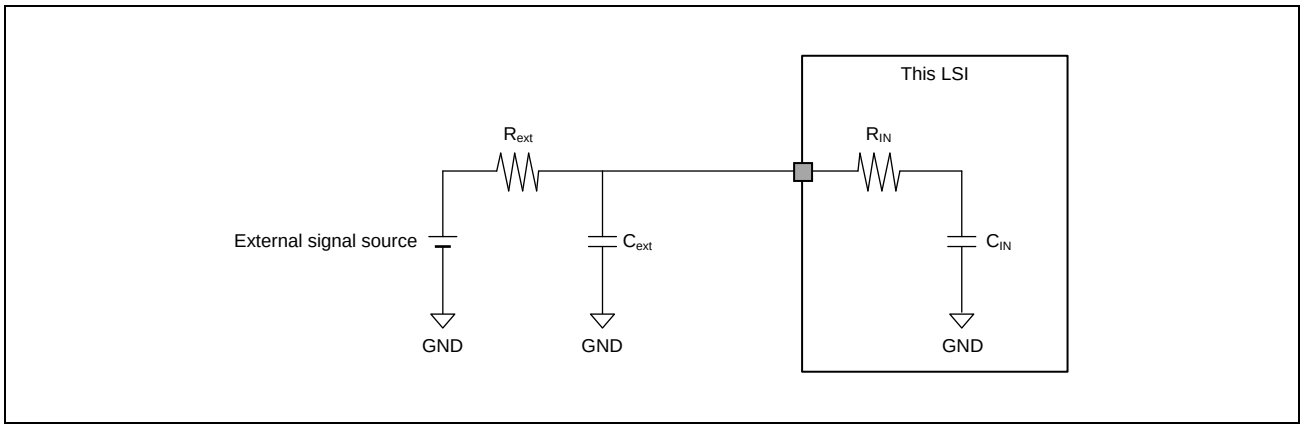


Figure 3.5 Analog Input Equivalent Circuit

Table 3.12 DC Characteristics (10) [Current Consumption]

Item	Power Rail Symbol	Max Current	Unit	Remarks
Power Supply Voltage (VBATT)	VBATT_V_{DD}	10	mA	
Power Supply Voltage (Core)	V_{DD}	450	mA	
Power Supply Voltage (ISO)	V_{DD_ISO}	2350	mA	Condition: Cortex-A55, Dhrystone
Power Supply Voltage (PLL)	PLL16_AV_{DD}	10	mA	
	PLL23_AV_{DD}	10	mA	
	PLL4_AV_{DD}	10	mA	
Power Supply Voltage (I/O)	PV_{DD33}	300	mA	
	PV_{DD18}	10	mA	
Power Supply Voltage (ADC/TSU)	ADC_AV_{DD18}	10	mA	
Power Supply Voltage (OTP)	OTP_AV_{DD18}	10	mA	
Power Supply Voltage (JTAG)	JTAG_PV_{DD}	10	mA	
Power Supply Voltage (XSPI) (1.8 V)	XSPI_PV_{DD}	110	mA	Clock Frequency = 133 MHz, Cload = 10 pF
		150	mA	Clock Frequency = 133 MHz, Cload = 15 pF
Power Supply Voltage (XSPI) (3.3 V)	XSPI_PV_{DD}	100	mA	Clock Frequency = 66 MHz, Cload = 15 pF
Power Supply Voltage (I3C) (1.8 V)	I3C_PV_{DD}	10	mA	
Power Supply Voltage (I3C) (1.2 V)	I3C_PV_{DD}	10	mA	
Power Supply Voltage (SD) (1.8 V)	SD0_PV_{DD}	100	mA	Clock Frequency = 125 MHz, Cload = 15 pF, eMMC: HS200
	SD1_PV_{DD}	100	mA	Clock Frequency = 125 MHz, Cload = 20 pF, SD: SDR104
Power Supply Voltage (SD) (3.3 V)	SD0_PV_{DD}	100	mA	Clock Frequency = 31.25 MHz, Cload = 30 pF, eMMC: High speed SDR
	SD1_PV_{DD}	100	mA	Clock Frequency = 31.25 MHz, Cload = 40 pF, SD: High speed
Power Supply Voltage (Ether) (1.8 V)	$PV_{DD182533\_0}$	100	mA	Clock Frequency = 125 MHz, Cload = 8 pF
	$PV_{DD182533\_1}$	100	mA	Clock Frequency = 125 MHz, Cload = 8 pF
Power Supply Voltage (Ether) (2.5 V)	$PV_{DD182533\_0}$	100	mA	Clock Frequency = 125 MHz, Cload = 8 pF
	$PV_{DD182533\_1}$	100	mA	Clock Frequency = 125 MHz, Cload = 8 pF
Power Supply Voltage (Ether) (3.3 V)	$PV_{DD182533\_0}$	100	mA	Clock Frequency = 125 MHz, Cload = 8 pF
	$PV_{DD182533\_1}$	100	mA	Clock Frequency = 125 MHz, Cload = 8 pF
Power Supply Voltage (USB)	USB_V_{DD33}	100	mA	
	USB_AV_{DD18}	200	mA	
	USB_V_{DD18}	200	mA	
Power Supply Voltage (PCIe)	PCIE_V_{DD18}	50	mA	
	PCIE_V_{DD09}	100	mA	
Power Supply Voltage (DDR)	DDR_V_{AA}	10	mA	
Power Supply Voltage (DDR) (DDR4)	DDR_V_{DDQ}	300	mA	
Power Supply Voltage (DDR) (LPDDR4)	DDR_V_{DDQ}	400	mA	

Note: T_j = 125°C, Power supply voltage = Max.

3.5 AC Characteristics

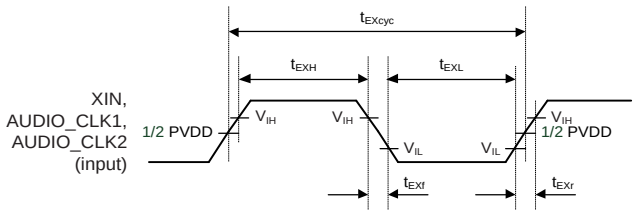
Conditions: VBATT_V_{DD} = 1.50 to 1.95 V, V_{DD} = PLL16/23/4_AV_{DD} = 0.905 to 0.99 V,
PV_{DD33} = 3.0 to 3.6 V, PV_{DD18} = ADC_AV_{DD18} = OTP_AV_{DD18} = 1.65 to 1.95 V,
JTAG_PV_{DD} = 1.65 to 1.95 V, XSPI_PV_{DD} = 1.65 to 1.95 V / 3.0 to 3.6 V,
I3C_PV_{DD} = 1.1 to 1.3 V / 1.65 to 1.95 V, V_{DD_ISO} = PCIE_V_{DD09} = 0.905 to 0.99 V,
SDn_PV_{DD} (n = 0, 1) = 1.65 to 1.95 V / 3.0 to 3.6 V,
$PV_{DD182533\_n}$ (n = 0, 1) = 1.65 to 1.95 V / 2.3 to 2.7 V / 3.0 to 3.6 V,
USB_V_{DD33} = 3.0 to 3.6 V, USB_AV_{DD18} = USB_V_{DD18} = PCIE_V_{DD18} = 1.65 to 1.95 V,
DDR_V_{AA} = 1.65 to 1.95 V, DDR_V_{DDQ} = 1.06 to 1.17 V (LPDDR4) / 1.14 to 1.26 V (DDR4),
USB_V_{SS} = 0 V, V_{SS} = 0 V, T_a = −40 to +85°C, T_j = −40 to +125°C

3.5.1 Clock Timing

Table 3.13 Clock Timing Table

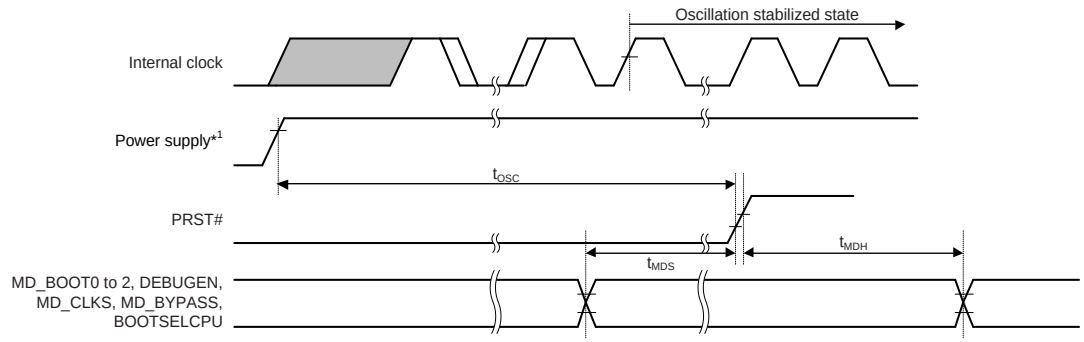
Item	Symbol	Min.	Max.	Unit	Figures
XIN clock input frequency	f_{EX}	24 – 50ppm*1	24 + 50ppm*1	MHz	**Figure 3.6**
XIN clock input cycle time	t_{EXcyc}	41.67	41.67	ns	
AUDIO_CLK1, AUDIO_CLK2 clock input frequency (external clock is input)	f_{EX}	10	50	MHz	
AUDIO_CLK1, AUDIO_CLK2 clock input cycle time (external clock is input)	t_{EXcyc}	20	100	ns	
XIN, AUDIO_CLK1, AUDIO_CLK2 clock input low level pulse width	t_{EXL}	0.4	0.6	t_{EXcyc}	
XIN, AUDIO_CLK1, AUDIO_CLK2 clock input high level pulse width	t_{EXH}	0.4	0.6	t_{EXcyc}	
XIN, AUDIO_CLK1, AUDIO_CLK2 clock input rise time	t_{EXr}	—	4	ns	
XIN, AUDIO_CLK1, AUDIO_CLK2 clock input fall time	t_{EXf}	—	4	ns	
Oscillator stabilization time	t_{OSC}	—	2	ms	**Figure 3.7**, **Figure 3.8**
Mode hold time	t_{MDH}	—	12	µs	
Mode setup time	t_{MDS}	—	0	µs	

Note 1. When using RGMII interface. If not using RGMII mode, this spec is ±100 ppm.



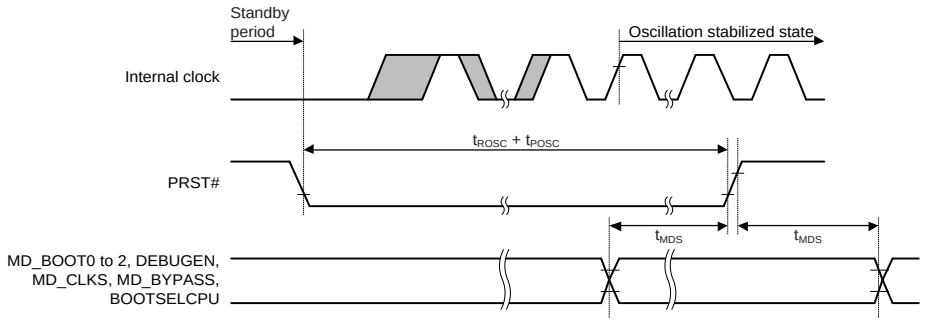
Note: When the clock is input on the EXCLK, AUDIO_CLK1 or AUDIO_CLK2

Figure 3.6 EXCLK, AUDIO_CLK1 and AUDIO_CLK2 Clock Input Timing



Note 1. V_{DD}, PLLn_DV_{DD11}, PLLn_AV_{DD18}, ADC_AV_{DD18}, V_{DD18}, OTP_V_{DD18}, USB_V_{DD18}, CSI_V_{DD18}, PV_{DD},USB_V_{DD33}, DDR_V_{DDQ}, SPI_PV_{DD}, SDn_PV_{DD}, $PV_{DD182533\_0}$, $PV_{DD182533\_1}$, OTP_V_{DD18}

Figure 3.7 Power-On Oscillation Settling Time



Note: Oscillation setting time when the internal oscillator is used.

Figure 3.8 Oscillation Settling Time on Return from Standby (Return by Reset)

Table 3.14 32-kHz Clock Oscillator Timing Table

Item	Symbol	Min.	Max.	Unit	Figures
32-kHz clock oscillator stabilization time	t_{ROSC}	—	2.5	sec	

Note: Oscillation stabilization time after enabling the oscillation of the 32-kHz OSC implemented in the VBATTB region

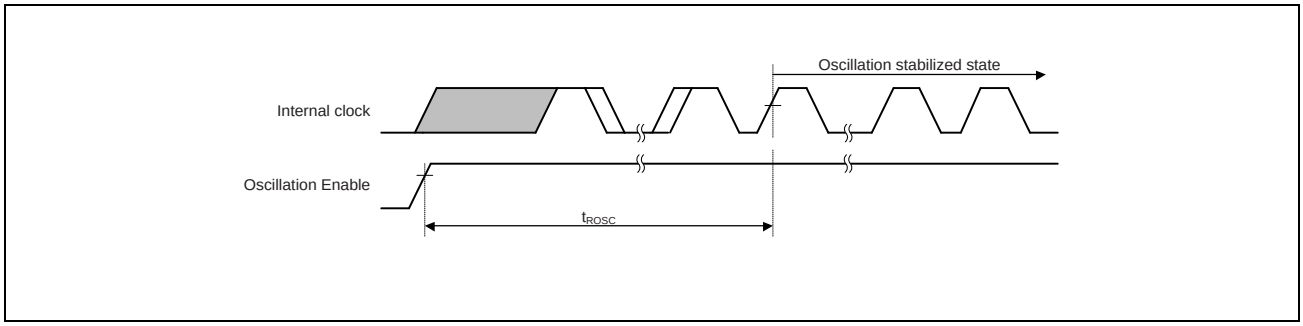


Figure 3.9 32-kHz Clock Oscillator Stabilization Time

3.5.2 Control Signal Access Timing

Table 3.15 Control Signal Timing

Item	Symbol	Min.	Max.	Unit	Figures
PRST# pulse width	t_{RESW}	20	—	t_{cyc}*1	**Figure 3.10**
TRST# pulse width	t_{TRSW}	20	—	t_{cyc}*1	
NMI pulse width	t_{NMIW}	20	—	t_{cyc}*1	**Figure 3.12**
IRQ pulse width	t_{IRQW}	20	—	t_{cyc}*1	
TINT pulse width	t_{TINTW}	20	—	t_{cyc}*1	
PRST# input rise time	t_{RSr}	—	500	µs	**Figure 3.11**

Note 1. t_{cyc} = 41.666 ns (24 MHz)

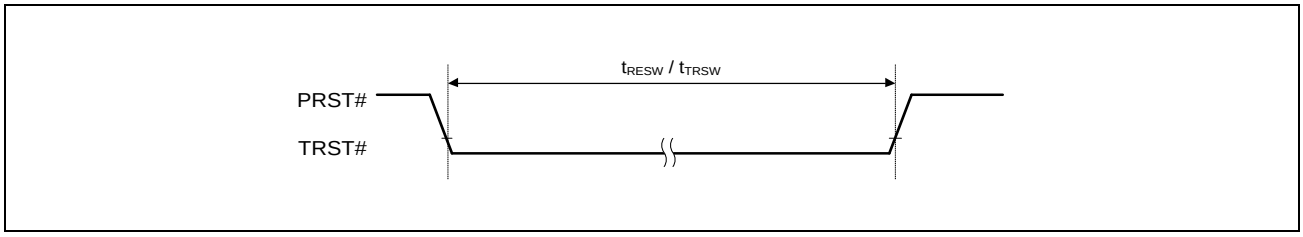


Figure 3.10 Reset Input Timing 1

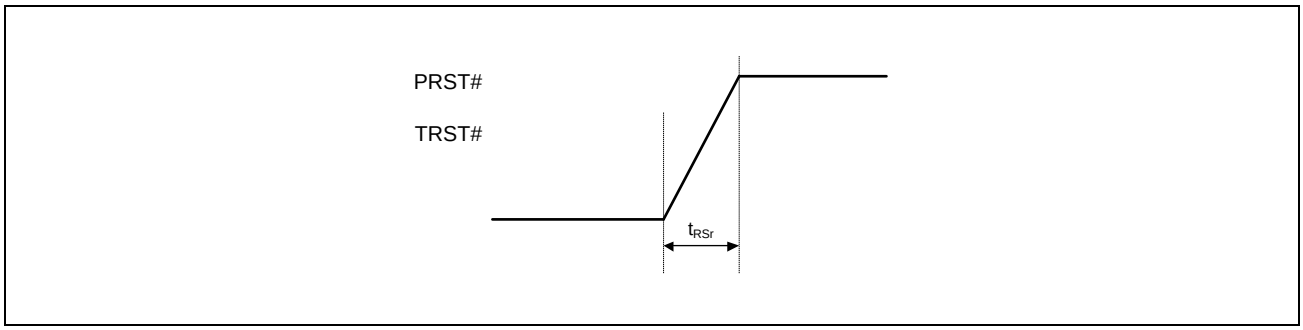
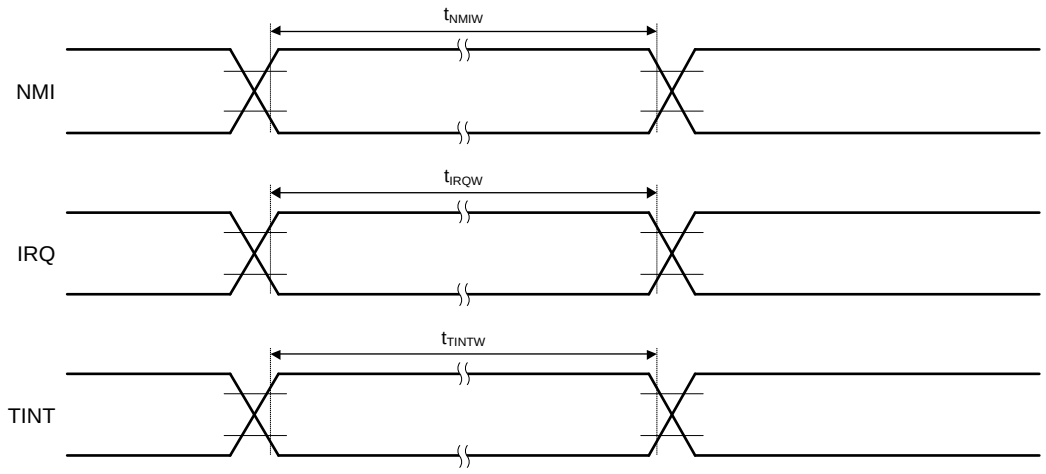


Figure 3.11 Reset Input Timing 2



Note: This specification “(Min. 20 t_{cycle})” is the min. pulse width the case that the digital noise filter is off. For details on digital noise filter settings, refer to *Section 45, General Purpose Input Output Port (GPIO)*, in the *User's Manual: Hardware*.

Figure 3.12 Interrupt Signal Input Timing

3.5.3 SDHI Access Timing

3.5.3.1 SDHI Access Timing (SDR 3.3-V)

Table 3.16 SDHC AC Access Timing (SDR at 3.3-V Operation)

Item	Symbol	Default Speed Mode (15.625 MHz)		High Speed Mode (31.25 MHz)		Unit	Figures
		Min.	Max.	Min.	Max.		
SD_CLK clock cycle	t_{SDCYC}	64.00	—	32.0	—	ns	**Figure 3.13**
SD_CLK clock high level width	t_{SDWH}	23.50	—	13.50	—	ns	
SD_CLK clock low level width	t_{SDWL}	23.50	—	13.50	—	ns	
SD_CLK clock rise time	t_{SDLH}	—	10	—	3	ns	
SD_CLK clock fall time	t_{SDHL}	—	10	—	3	ns	
SD_CMD,SD_DATA output delay	t_{SDODLY}	−4.50	4.0	−4.50	4.0	ns	
SD_CMD,SD_DATA input set up time	t_{SDIS}	5.5	—	5.5	—	ns	
SD_CMD,SD_DATA input hold time	t_{SDIH}	2.0	—	2.0	—	ns	
SD_CMD,SD_DATA input data width	t_{SDIDW}	—	—	—	—	ns	

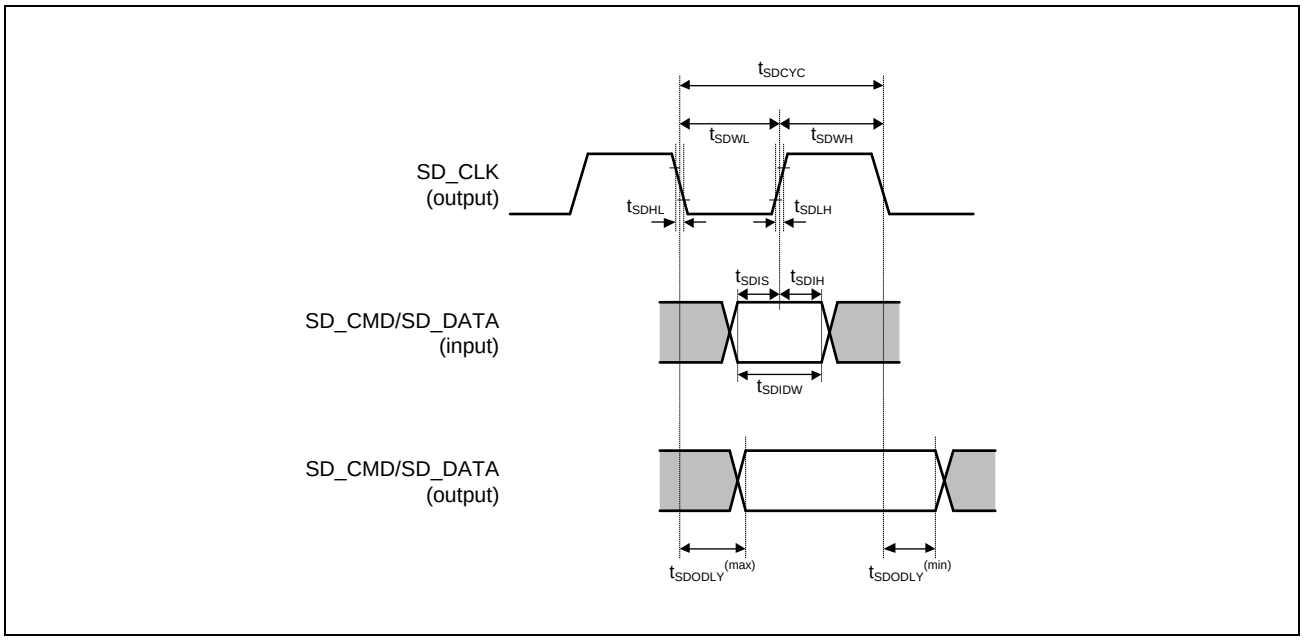


Figure 3.13 SDHC Interface Timing (SDR 3.3-V Power Supply)

NOTE

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact your local sales representatives.

3.5.4 eMMC Access Timing

3.5.4.1 eMMC Host Interface Timing (Default)

Table 3.17 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SD0_CLK clock cycle	t_{MMCPP}	40.00	—	ns	**Figure 3.14**
SD0_CLK clock high level width	t_{MMCWH}	18.50	—	ns	
SD0_CLK clock low level width	t_{MMCWL}	18.50	—	ns	
SD0_CLK clock rise time	t_{MMCLH}	—	3	ns	
SD0_CLK clock fall time	t_{MMCHL}	—	3	ns	
SD0_CMD/SDDAT output delay	$t_{MMCODLY}$	−4.50	4.0	ns	
SD0_CMD/SDDAT input set up time	t_{MMCISU}	5.5	—	ns	
SD0_CMD/SDDAT input hold time	t_{MMCIH}	2.0	—	ns	
SD0_CMD/SDDAT input data width	t_{MMCIDW}	—	—	ns	

Table 3.18 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SD0_CLK clock cycle	t_{MMCPP}	40.00	—	ns	**Figure 3.14**
SD0_CLK clock high level width	t_{MMCWH}	19.25	—	ns	
SD0_CLK clock low level width	t_{MMCWL}	19.25	—	ns	
SD0_CLK clock rise time	t_{MMCLH}	—	2.45	ns	
SD0_CLK clock fall time	t_{MMCHL}	—	2.45	ns	
SD0_CMD/SDDAT output delay	$t_{MMCODLY}$	−2.00	2.50	ns	
SD0_CMD/SDDAT input set up time	t_{MMCISU}	5.00	—	ns	
SD0_CMD/SDDAT input hold time	t_{MMCIH}	1.40	—	ns	
SD0_CMD/SDDAT input data width	t_{MMCIDW}	—	—	ns	

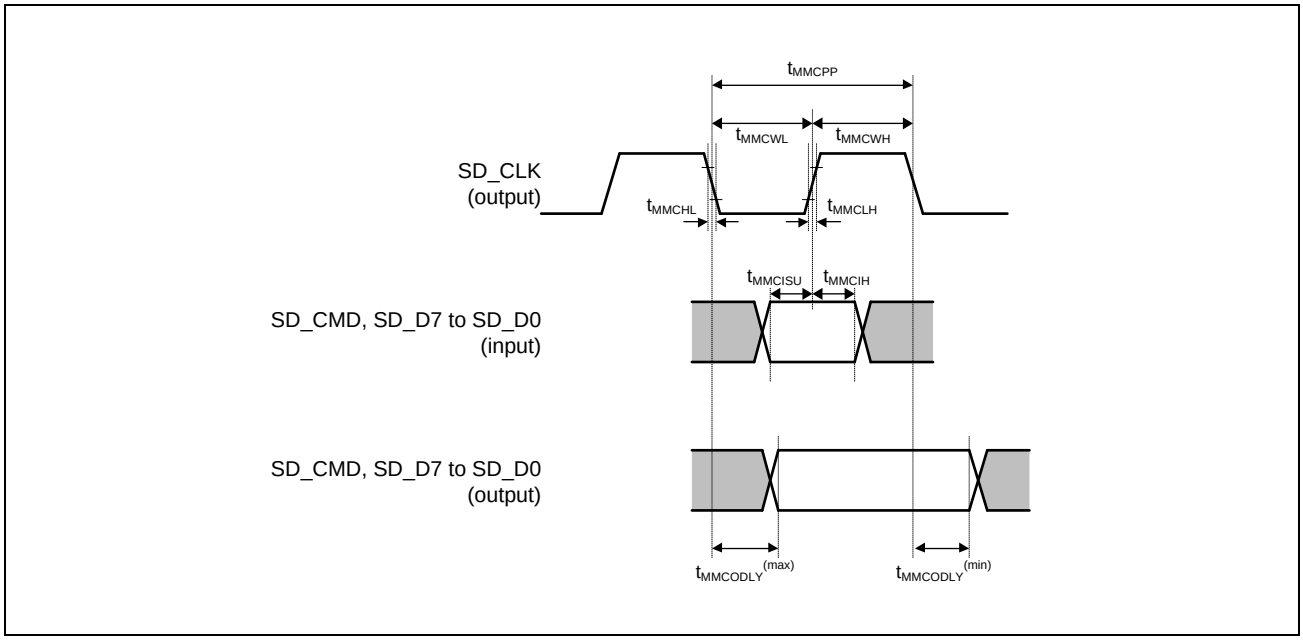


Figure 3.14 eMMC Host Interface Timing (MMC Default 1.8-V/3.3-V Power Supply)

3.5.4.2 eMMC Host Interface Timing (HS-SDR)

Table 3.19 eMMC Host Interface Timing (MMC HS-SDR 3.3-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SD0_CLK clock cycle	t_{MMCPP}	32.00	—	ns	**Figure 3.14**
SD0_CLK clock high level width	t_{MMCWH}	13.50	—	ns	
SD0_CLK clock low level width	t_{MMCWL}	13.50	—	ns	
SD0_CLK clock rise time	t_{MMCLH}	—	3	ns	
SD0_CLK clock fall time	t_{MMCHL}	—	3	ns	
SD0_CMD/SDDAT output delay	$t_{MMCODLY}$	−4.50	4.0	ns	
SD0_CMD/SDDAT input set up time	t_{MMCISU}	5.5	—	ns	
SD0_CMD/SDDAT input hold time	t_{MMCIH}	2.0	—	ns	
SD0_CMD/SDDAT input data width	t_{MMCIDW}	—	—	ns	

Table 3.20 eMMC Host Interface Timing (MMC HS-SDR 1.8-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SD0_CLK clock cycle	t_{MMCPP}	20.00	—	ns	**Figure 3.14**
SD0_CLK clock high level width	t_{MMCWH}	9.25	—	ns	
SD0_CLK clock low level width	t_{MMCWL}	9.25	—	ns	
SD0_CLK clock rise time	t_{MMCLH}	—	2.45	ns	
SD0_CLK clock fall time	t_{MMCHL}	—	2.45	ns	
SD0_CMD/SDDAT output delay	$t_{MMCODLY}$	−2.00	2.50	ns	
SD0_CMD/SDDAT input set up time	t_{MMCISU}	5.00	—	ns	
SD0_CMD/SDDAT input hold time	t_{MMCIH}	1.40	—	ns	
SD0_CMD/SDDAT input data width	t_{MMCIDW}	—	—	ns	

3.5.4.3 eMMC Host Interface Timing (HS200)

Table 3.21 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

Item	Symbol	Min.	Max.	Unit	Figures
SD0_CLK clock cycle	t_{MMCPP}	8.00	16.00	ns	**Figure 3.15**
SD0_CLK clock high level width	t_{MMCWH}	3.30	—	ns	
SD0_CLK clock low level width	t_{MMCWL}	3.30	—	ns	
SD0_CLK clock rise time	t_{MMCLH}	—	1.22	ns	
SD0_CLK clock fall time	t_{MMCHL}	—	1.22	ns	
SD0_CMD/SDDAT output delay	$t_{MMCODLY}$	−2.20	1.80	ns	
SD0_CMD/SDDAT input set up time	t_{MMCISU}	—	—	ns	
SD0_CMD/SDDAT input hold time	t_{MMCIH}	—	—	ns	
SD0_CMD/SDDAT input data width	t_{MMCIDW}	4.31	—	ns	

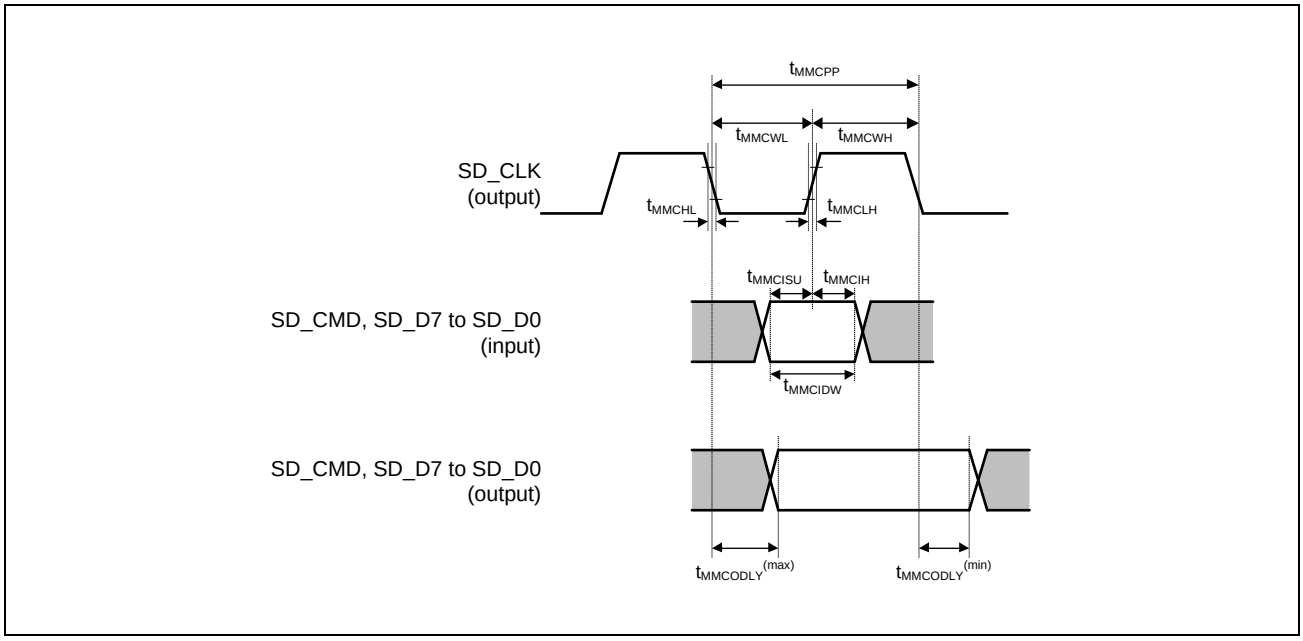


Figure 3.15 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

3.5.5 USB 2.0 Host/Function Module Access Timing

3.5.5.1 USB 2.0 Low-Speed Access Timing

Table 3.22 USB Transceiver Timing (Low-Speed)

Item	Symbol	Min.	Max.	Unit	Figures
Rise time	t_{LR}	75	300	ns	**Figure 3.16**
Fall time	t_{LF}	75	300	ns	
Rise/fall time lag	t_{LR}/t_{LF}	80	125	%	

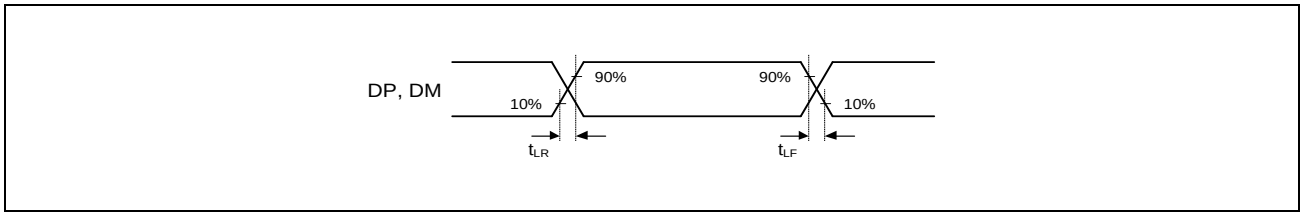


Figure 3.16 USB0_DP, USB1_DP, USB0_DM, and USB1_DM Output Timing (Low-Speed)

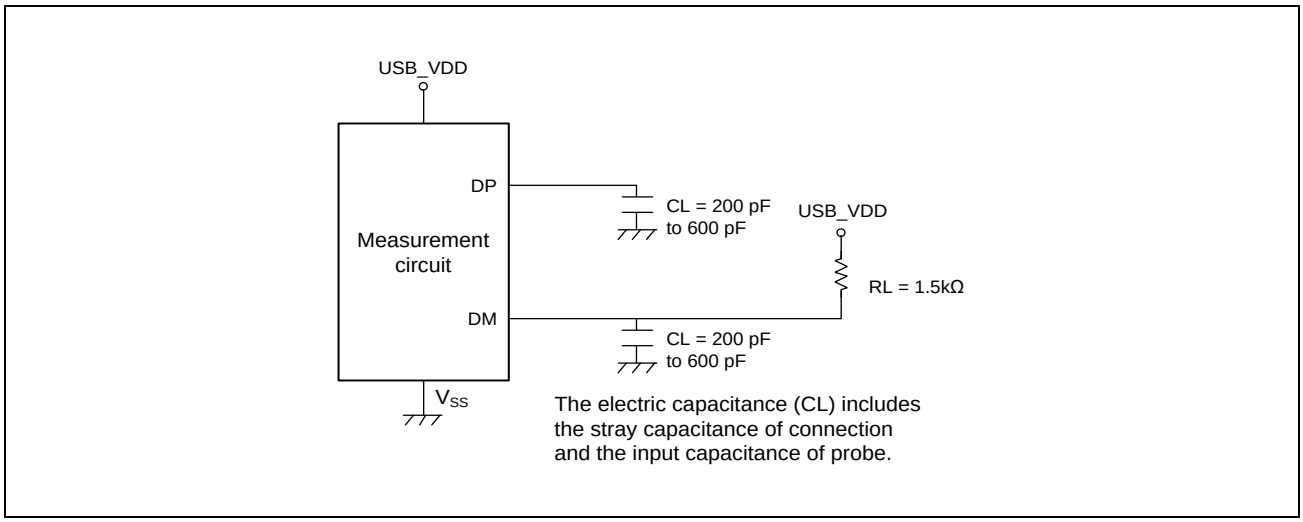


Figure 3.17 Measurement Circuit (Low-Speed)

3.5.5.2 USB 2.0Full-Speed Access Timing

Table 3.23 USB Transceiver Timing (Full-Speed)

Item	Symbol	Min.	Max.	Unit	Figures
Rise time	t_{FR}	4	20	ns	**Figure 3.18**
Fall time	t_{FF}	4	20	ns	
Rise/fall time lag	t_{FR}/t_{FF}	90	111.11	%	

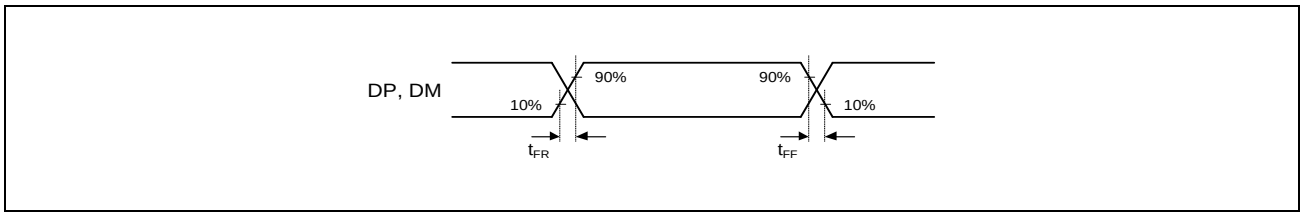


Figure 3.18 USB0_DP, USB1_DP, USB0_DM, and USB1_DM Output Timing (Full-Speed)

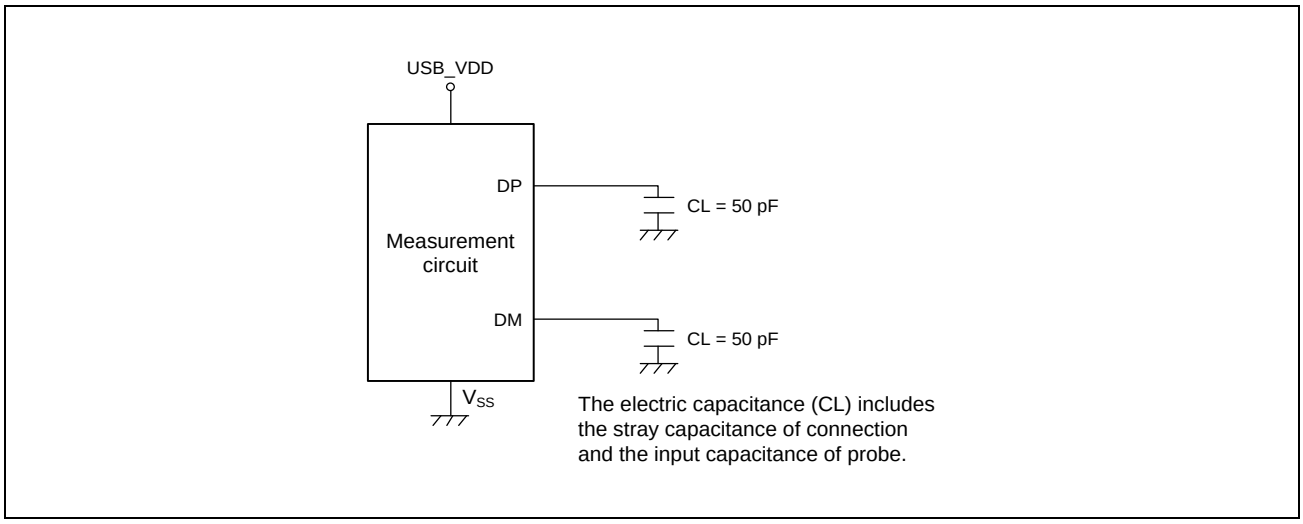


Figure 3.19 Measurement Circuit (Full-Speed)

3.5.5.3 USB 2.0 Hi-Speed Access Timing

Table 3.24 USB Transceiver Timing (Hi-Speed)

Item	Symbol	Min.	Max.	Unit	Figures
Rise edge rate	t_{HSR}	—	2133	V/µs	**Figure 3.20**
Fall edge rate	t_{HSF}	—	2133	V/µs	
Output driver resistance	Z_{HSDRV}	40.5	49.5	Ω	

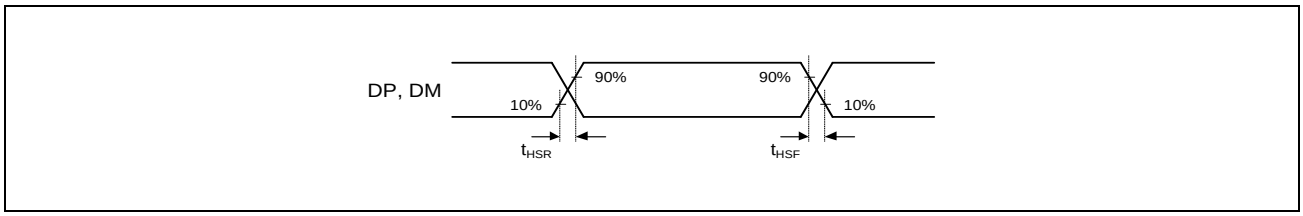


Figure 3.20 USB0_DP, USB1_DP, USB0_DM, and USB1_DM Output Timing (Hi-Speed)

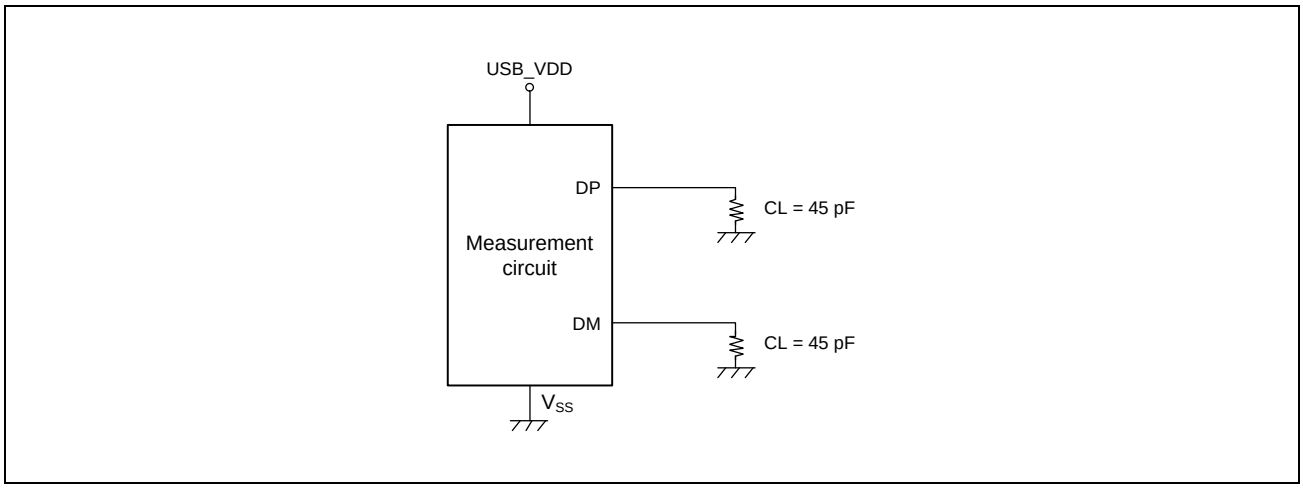
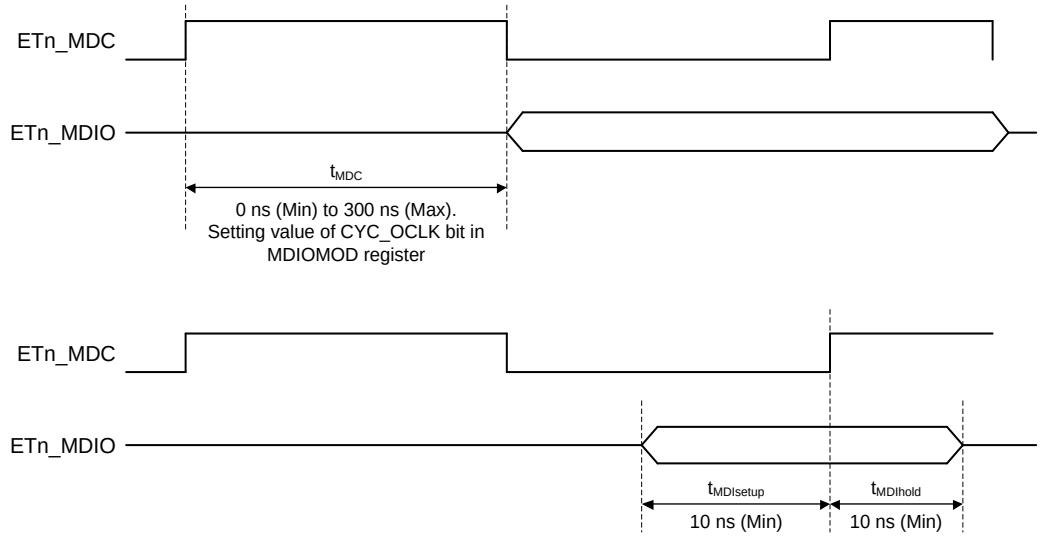


Figure 3.21 Measurement Circuit (Hi-Speed)

3.5.6 Ethernet Interface Access Timing

Table 3.25 Ethernet Interface Access Timing

Item	Symbol	Min.	Max.	Unit	Figures
MDC half cycle	t_{MDC}	0	300	ns	**Figure 3.22**
MDI setup time	$t_{MDIsetup}$	10	—	ns	
MDI hold time	$t_{MDIhold}$	10	—	ns	



Note: (n = 0, 1)

Figure 3.22 Management Interface

3.5.6.1 Ethernet-IF (Ether MII)

Table 3.26 Ethernet-IF Access Timing (Ether MII)

Item		Symbol	Min.	Max.	Unit	Figures
Ether MII	ETH_GTXTXC_TXC period	t_{Tcyc}	40	—	ns	**Figure 3.23**
	ETH_TXCTL output delay	t_{TENd}	0	25	ns	
	ETH_TXD3-0 output delay	t_{MTDd}	0	25	ns	
	ETH_RXC period	t_{Rcyc}	40	—	ns	
	ETH_RXDV setup time	t_{RDVs}	10	—	ns	
	ETH_RXDV hold time	t_{RDVh}	10	—	ns	
	ETH_RXD3-0 setup time	t_{MRDs}	10	—	ns	
	ETH_RXD3-0 hold time	t_{MRDh}	10	—	ns	
	ETH_RXER setup time	t_{RERs}	10	—	ns	
	ETH_RXER hold time	t_{RERh}	10	—	ns	

Note: I/O driving ability: IOLH_xx[1:0] = 11b
CL = 8 pF

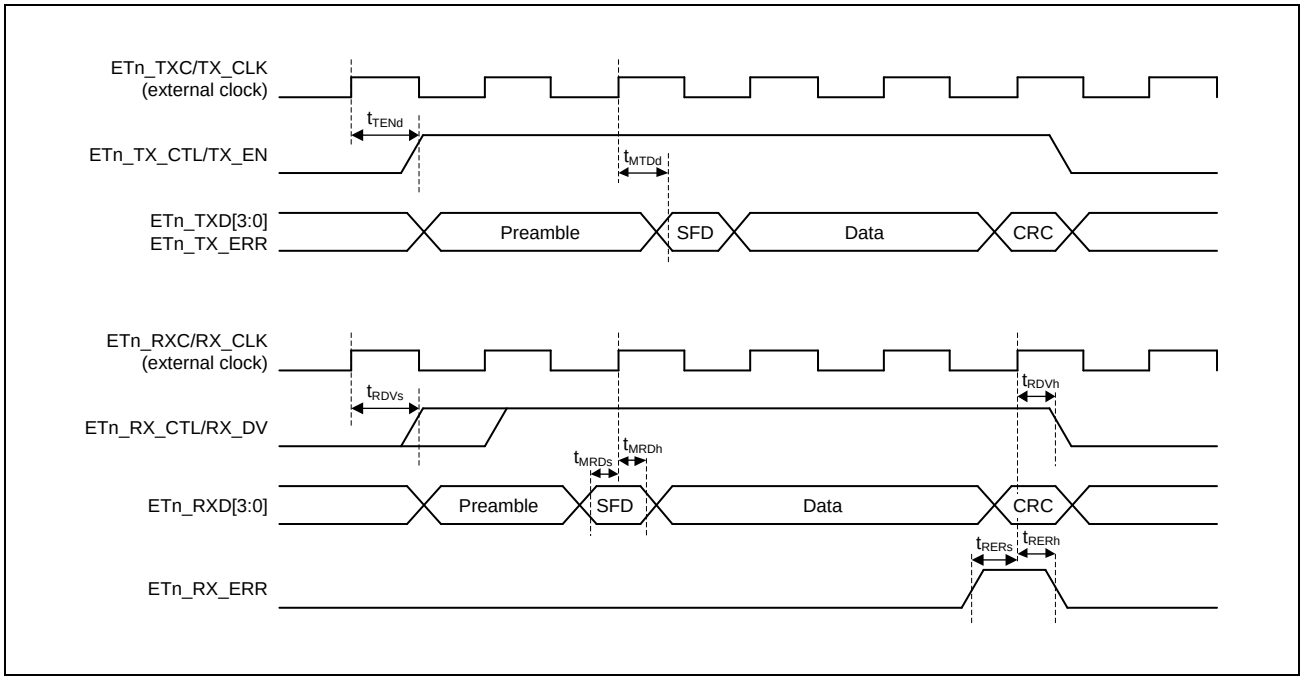


Figure 3.23 MII Transmission Timing

Validated with IEEE802.3 regulation.

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns.

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns.

3.5.6.2 Ethernet-IF (Ether RGMII)

Table 3.27 Ethernet-IF Access Timing (Ether RGMII)

Item		Symbol	Min.	Typ.	Max.	Unit	capaci-tance	Remarks	Figures
Ether RGMII	Data to clock output skew @ transmitter	T_{skewT}	−500	0	500	ps	8 pF	Tx RGMII	**Figure 3.24**
	Data to clock input skew @ receiver	T_{skewR}	1	1.8	2.6	ns	8 pF		
	Data to clock output setup @ transmitter integrated delay	T_{setupT}	1.2	2.0	—	ns	8 pF	Rx RGMII-ID	**Figure 3.25**
	Clock to data output hold @ transmitter integrated delay	T_{holdT}	1.2	2.0	—	ns	8 pF		
	Data to clock input setup setup @ receiver integrated delay	T_{setupR}	1.0	2.0	—	ns	8 pF	Rx RGMII-ID	**Figure 3.25**
	Data to clock input setup hold @ receiver integrated delay	T_{holdR}	1.0	2.0	—	ns	8 pF		
	Clock cycle duration*1	T_{cyc}	7.2	8	8.8	ns	8 pF	—	—
	Duty cycle for gigabit	Duty_G	45	50	55	%	8 pF		
	Duty cycle for 10/100T	Duty_T	40	50	60	%	8 pF		
	Rise/fall time (20 - 80%)	T_r/T_f	—	—	0.75	ns	8 pF		

Note 1. For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ± 40 ns and 40 ns ± 4 ns respectively.

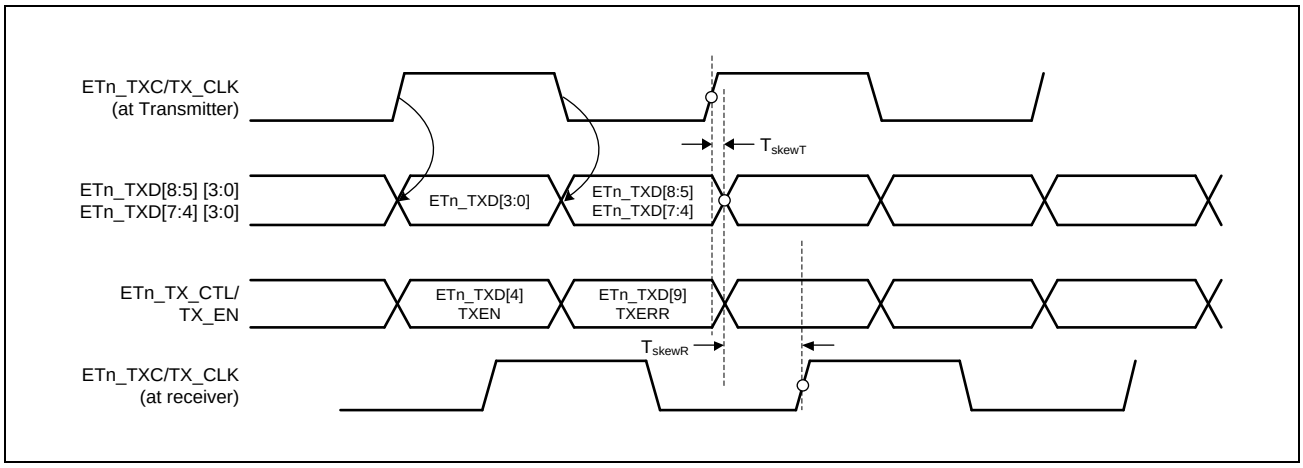


Figure 3.24 Multiplexing & Timing Diagram — RGMII (Transmitter)

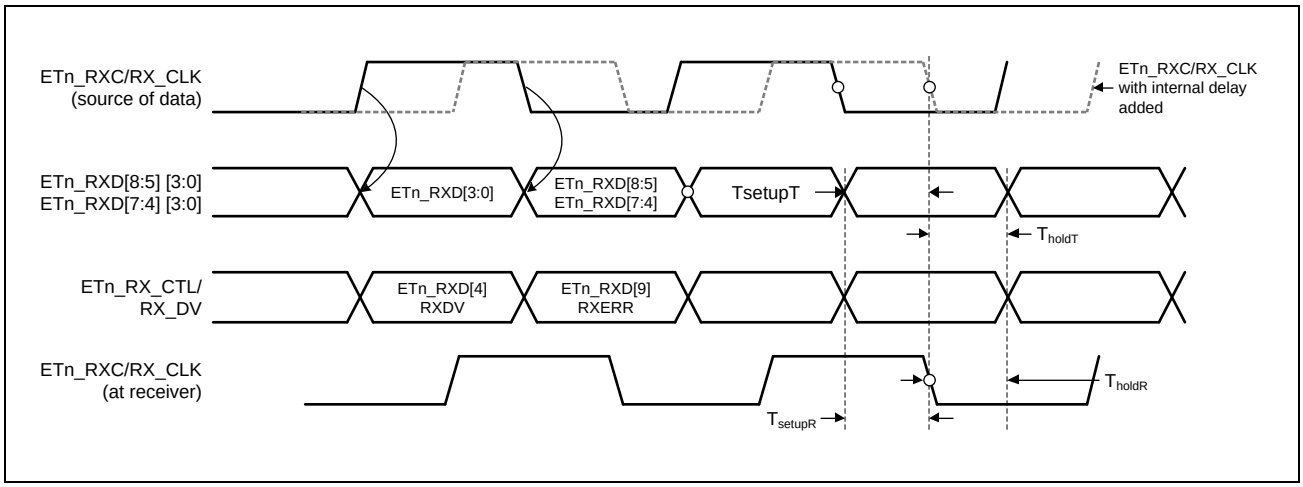


Figure 3.25 Multiplexing & Timing Diagram — RGMII-ID (Receiver)

3.5.7 JTAG Debugger Interface Access Timing

Table 3.28 Debugger IF Timing

Item	Symbol	Min.	Max.	Unit	Figures
TCK_SWCLK cycle time	t_{TCKcyc}	50	—	ns	**Figure 3.26**
TCK_SWCLK high pulse width	t_{TCKH}	20	—	ns	**Figure 3.27**
TCK_SWCLK low pulse width	t_{TCKL}	20	—	ns	
TDI setup time	t_{TDIS}	15	—	ns	
TDI hold time	t_{TDIH}	15	—	ns	
TMS_SWDIO setup time	t_{TMSS}	15	—	ns	
TMS_SWDIO hold time	t_{TMSH}	15	—	ns	
SWDIO delay time	t_{SWDO}	—	14	ns	
TDO delay time	t_{TDOD}	—	14	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	**Figure 3.28**
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	

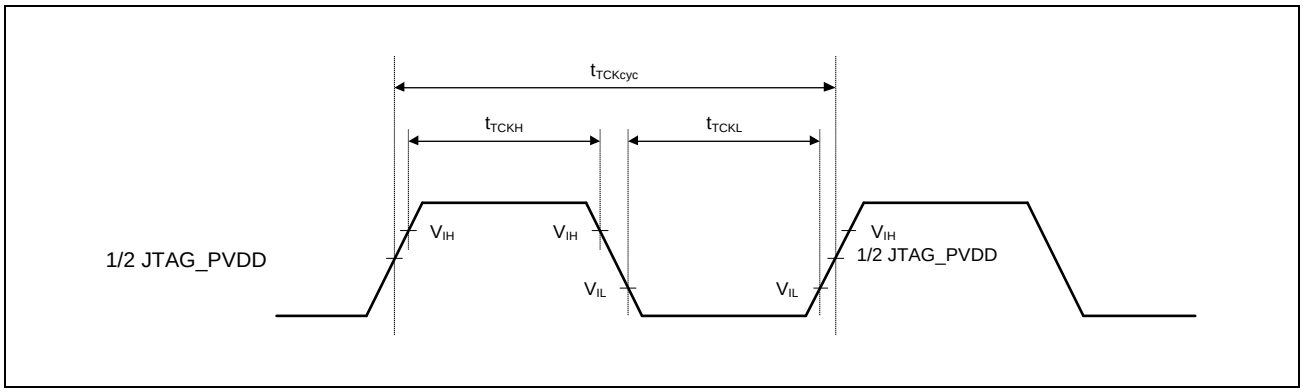


Figure 3.26 TCK_SWDCLK Input Timing

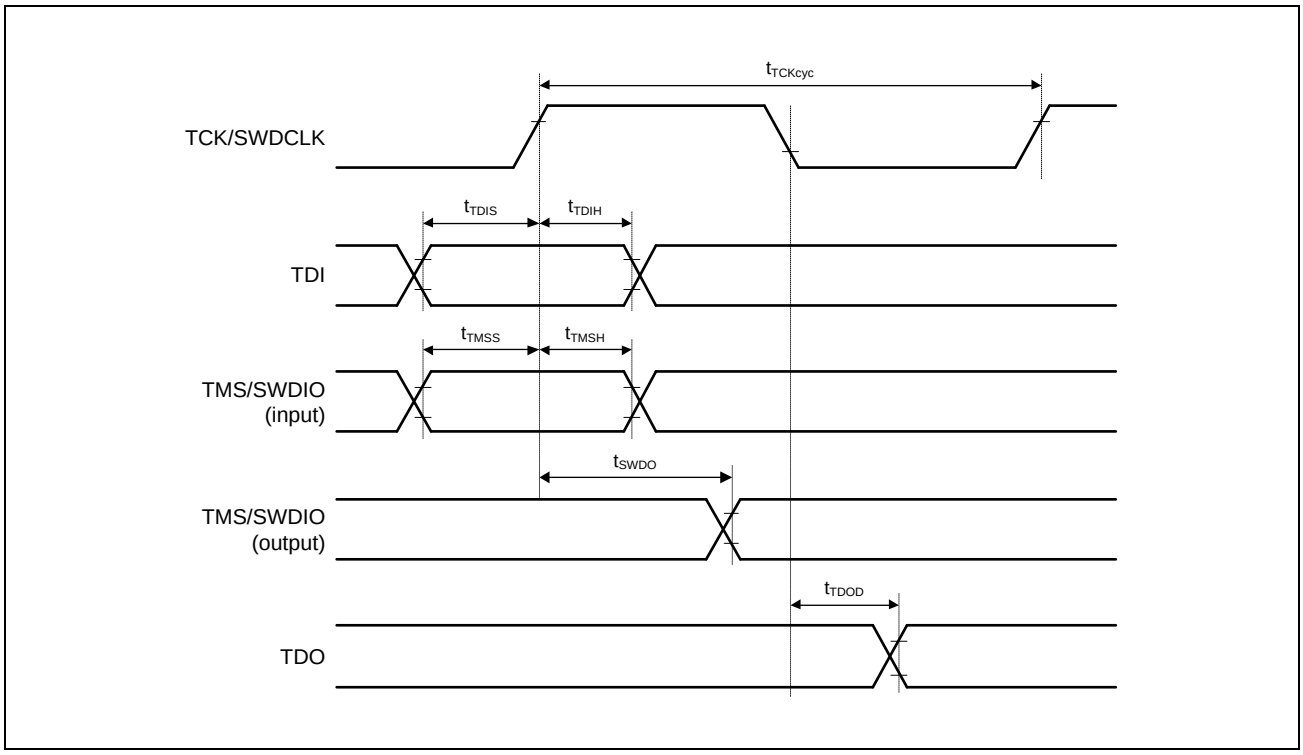


Figure 3.27 Data Transfer Timing

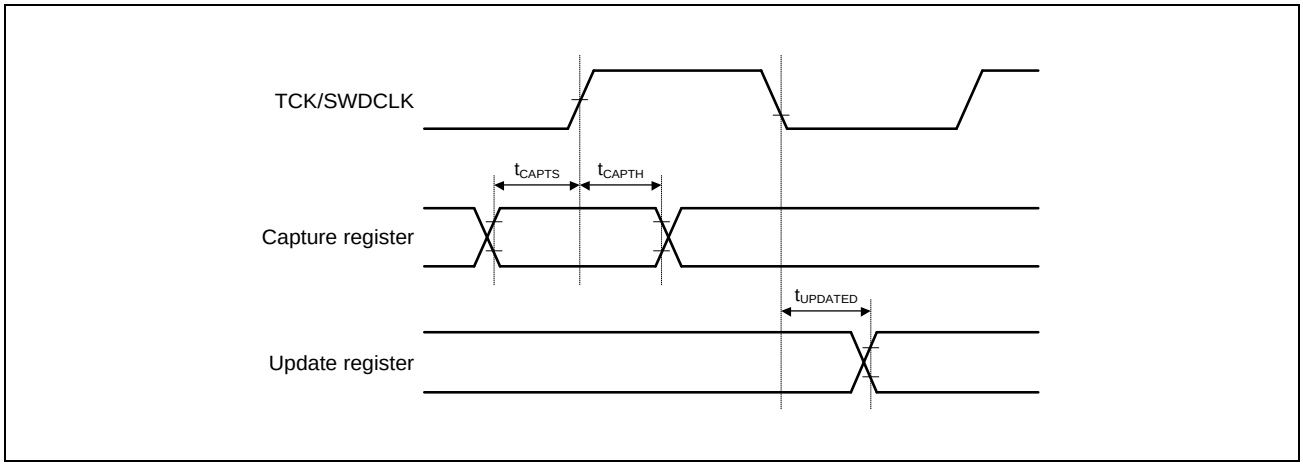


Figure 3.28 Boundary Scan Input/Output I/O Timing

3.5.8 xSPI Timing

Table 3.29 xSPI Timing

Item		Symbol	1.8 V		3.3 V		Unit	Figures
			Min.	Max.	Min.	Max.		
Clock cycle	SDR	t_{SPBcyc}	15	—	15	—	ns	**Figure 3.29**
	DDR		7.5	—	—	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*2	—	1.03*6	—	V/ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	1.03*6	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	5.0	—	5.0	—	ns	**Figure 3.30**
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time	SDR	t_{OD}	—	8.32*3	—	8.32*3	ns	
	DDR		—	1	—	—	ns	
Data output hold time	SDR	t_{OH}	4.8	—	4.8	—	ns	
	DDR		−1	—	—	—	ns	
Data output buffer off time	SDR	t_{BOFF}	4.8	—	4.8	—	ns	
	DDR		−1	—	—	—	ns	
Data input setup time (to DS)	DDR*1,*3	t_{SU}	−0.6/−0.8	—	−0.6/−0.8	—	ns	**Figure 3.31**
Data input hold time (to DS)		t_{H}	t_{PERIOD} × 0.41 − 0.6/0.8	—	t_{PERIOD} × 0.41 – 0.6/0.8	—	ns	
Data output setup time (to CK)		t_{SUO}	0.6*5	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	0.6*5	—	1.0	—	ns	
CS low to clock high		t_{CSLCKH}	6.0/8.0*2,*4	—	8.0*4	—	ns	**Figure 3.30**, **Figure 3.31**
Clock low to CS high		t_{CKLCSH}	6.0/8.0*2	—	8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS low to CS high		t_{DSLCSH}	6.0/8.0*2	—	10.6	—	ns	**Figure 3.32**
CS high to DS Tri-state		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low*7		t_{CSLDSL}	0.0	12.5*8	0.0	17.4*8	ns	
DS Tri-state to CS low		t_{DSTCSL}	0.0	—	0.0	—	ns	

Remarks: CK: XSPI_SPCLK
DS: XSPI_DS
CS: XSPI_CS0#, XSPI_CS1#

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 0_1000b for xSPI200.

Note 2. Specification at 133 MHz / Specification at 100 MHz

Note 3. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1b).

Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1b) and the CS negation is extended in CS negating extension bit.

Note 5. The standard value for xSPI266 is 0.8 ns.

Note 6. When IOLH_xx[1:0] is 11b.

Note 7. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 8. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

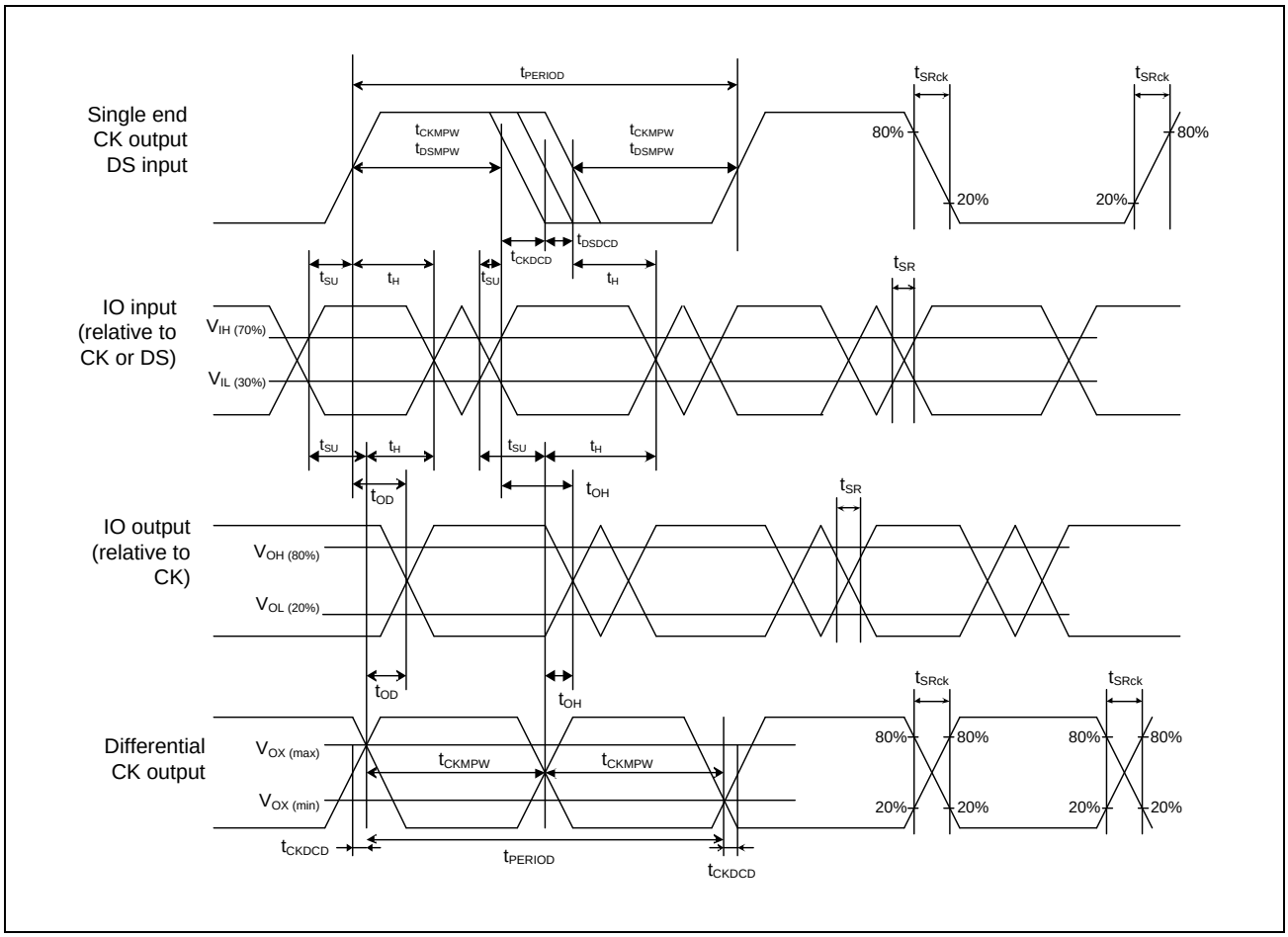


Figure 3.29 xSPI Clock / DS Timing

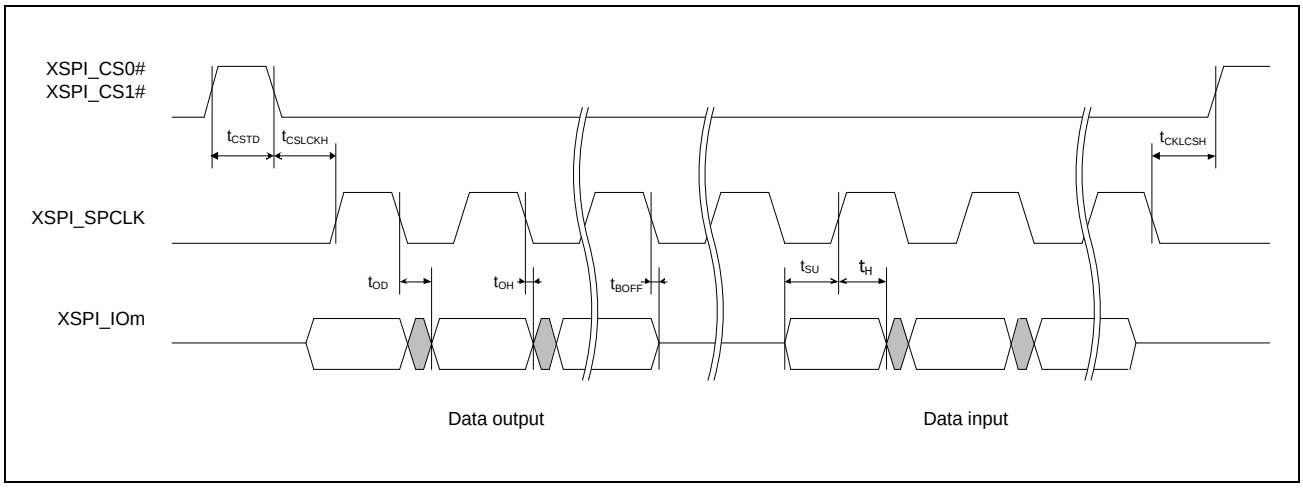


Figure 3.30 SDR Transmit/Receive Timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

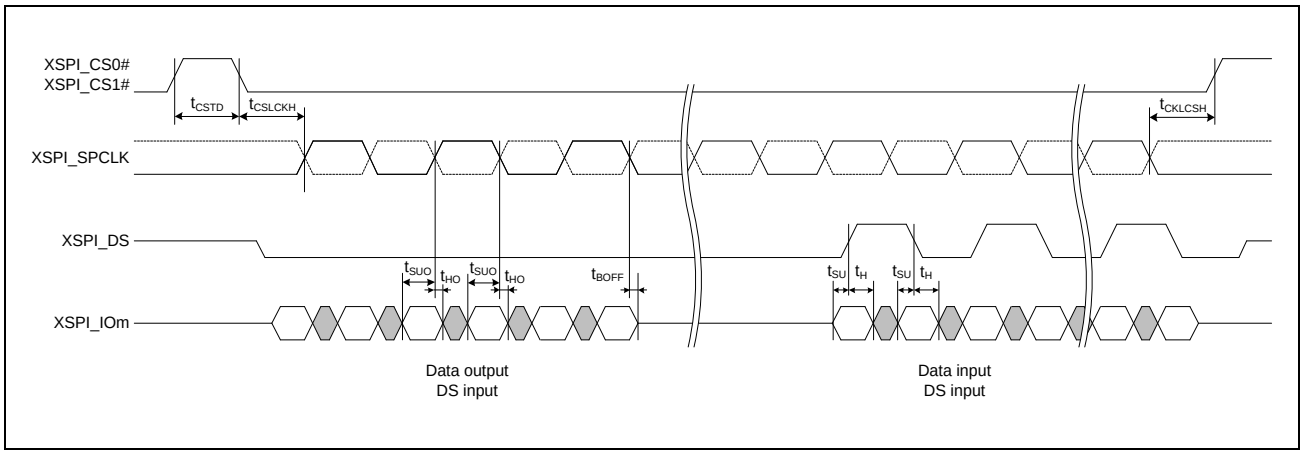


Figure 3.31 DDR Transmit/Receive Timing (8D-8D-8D)

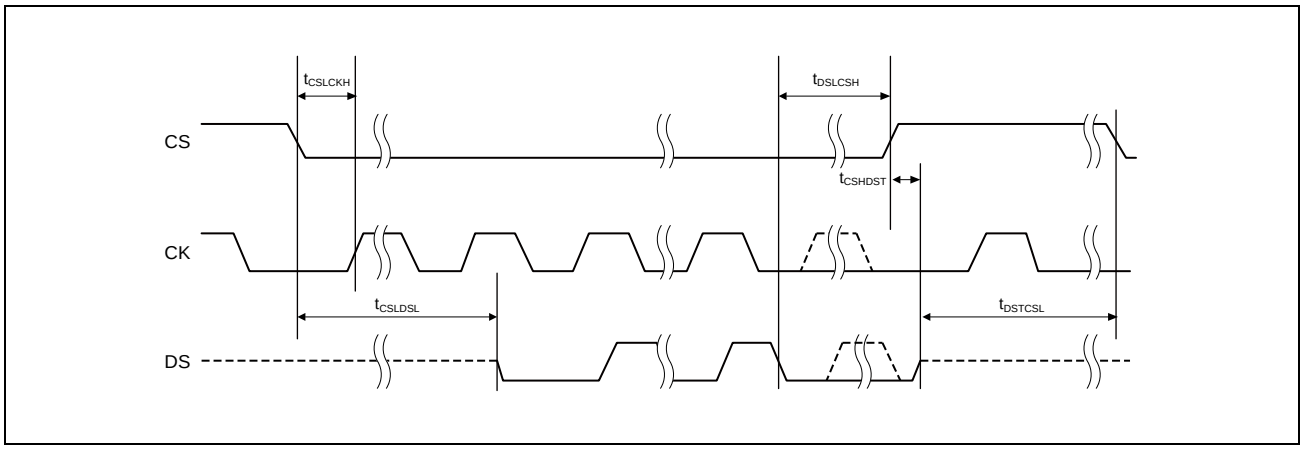


Figure 3.32 DS to CS Signal Timing

3.5.9 Serial Sound Interface (SSIF-2) Access Timing

Table 3.30 SSIF-2 Timing

Item	I/O	Symbol	Min.	Max.	Unit	Figures
Output clock cycle	Output	t_O	80	64000	ns	**Figure 3.33**
Input clock cycle	Input	t_I	80	—	ns	
Clock high	Bidirectional	t_{HC}	32	—	ns	
Clock low		t_{LC}	32	—	ns	
Clock rise time/clock fall time	Output	t_{RC}/t_{FC}	—	25	ns	
Setup time	Input	t_{SR}	25	—	ns	**Figure 3.34**, **Figure 3.35**, **Figure 3.36**
Hold time		t_{HR}	5	—	ns	
SILRCK output delay time	Output	t_{DTR}	−5	25	ns	
Data output delay time (Noise canceler not in use)		t_{DTR}	−5	25	ns	
Data output delay time (Noise canceler in use)		t_{DTR}	10	50	ns	

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

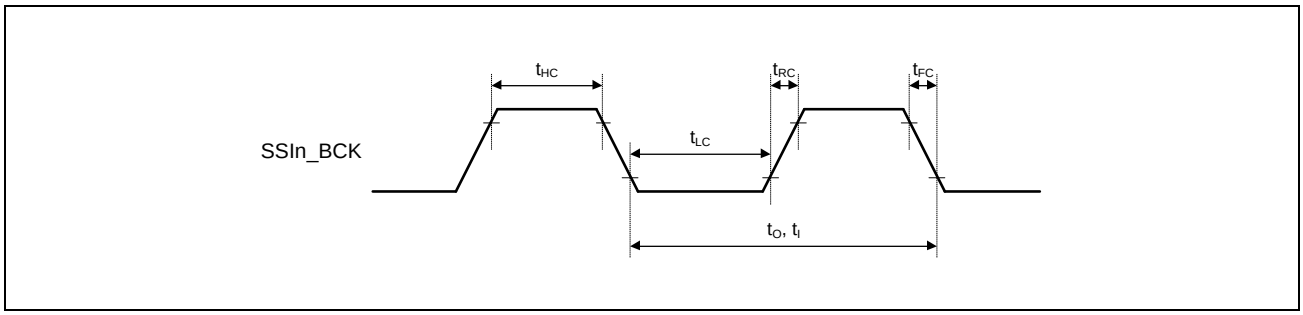


Figure 3.33 Bit Clock Input/Output Timing

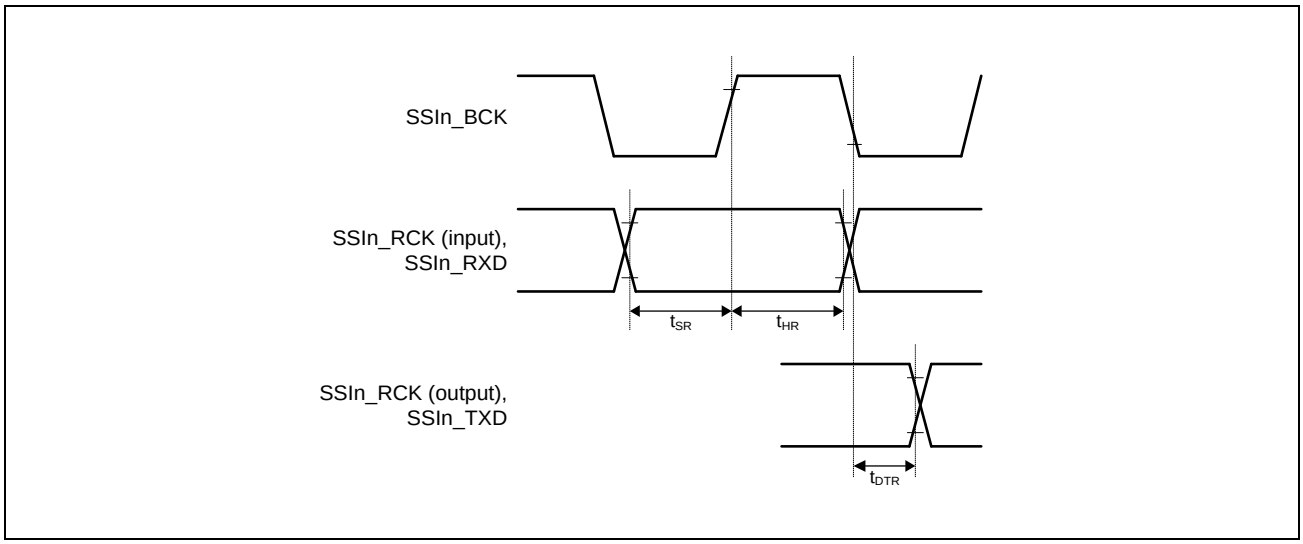


Figure 3.34 Transmission and Reception Timing (SSIBCK Falling Output)

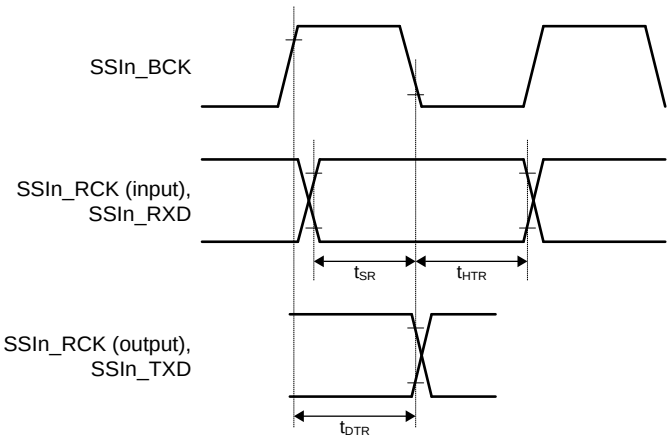
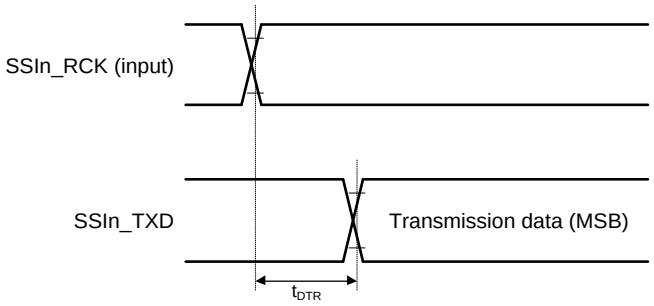


Figure 3.35 Transmission and Reception Timing (SSIBCK Rising Output)



Note: Output timing of the MSB when slave transmission satisfies the following condition a) or b)
a) SSICR.DEL = 1, SSICR.SDTA = 0
b) SSICR.DEL = 1, SSICR.SDTA = 1, without padding

Figure 3.36 Transmission Timing (Slave, in Synchronization with SSILRCK)

3.5.10 CAN-FD Interface Access Timing

Table 3.31 CAN-FD Interface Timing

Item	Symbol	CAN		CAN-FD		Unit	Figures
		Min.	Max.	Min.	Max.		
Internal delay time	t_{node}*1	—	100	—	50	ns	**Figure 3.37**
Transmission rate	—	—	1	—	8	Mbps	

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

Note 1. Internal delay time (t_{node}) = Internal transfer delay time (t_{output}) + Internal receive delay time (t_{input})

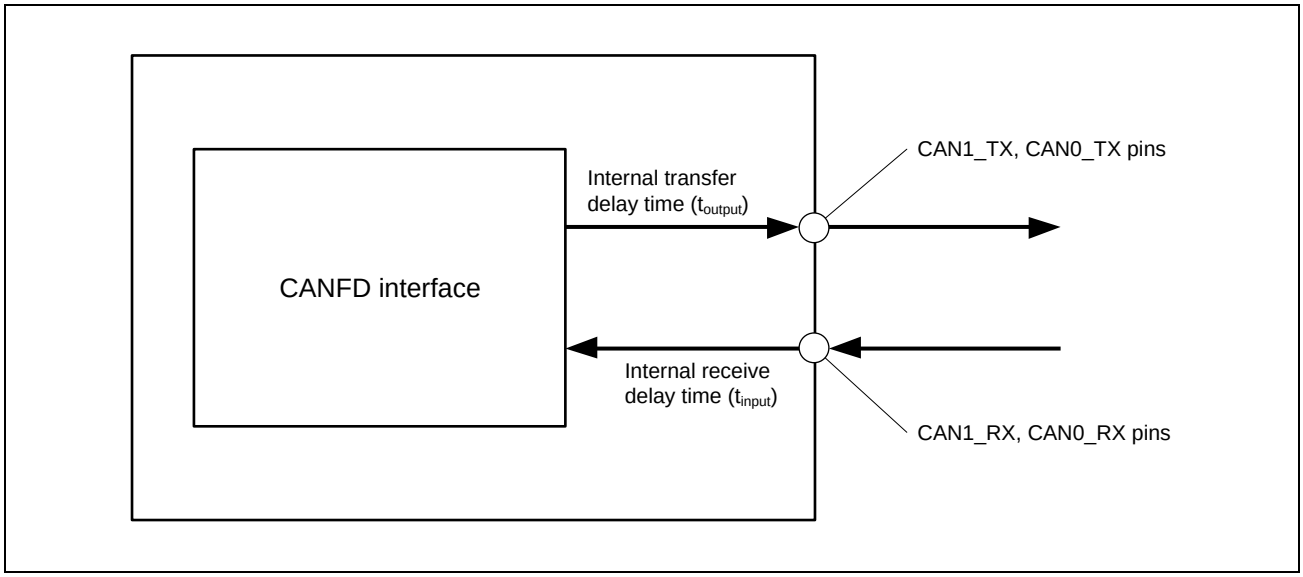


Figure 3.37 CAN-FD Interface Condition

3.5.11 Multi-Function Timer Pulse Unit 3 (MTU3a) Access Timing

Table 3.32 MTU3a Timing

Item			Symbol	Min.	Max.	Unit*1	Figures
MTU3a	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{p1cyc}*1	**Figure 3.38**
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{p1cyc}*1	**Figure 3.39**
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means MTU_X_MCLK_MTU3 (P0ϕ).

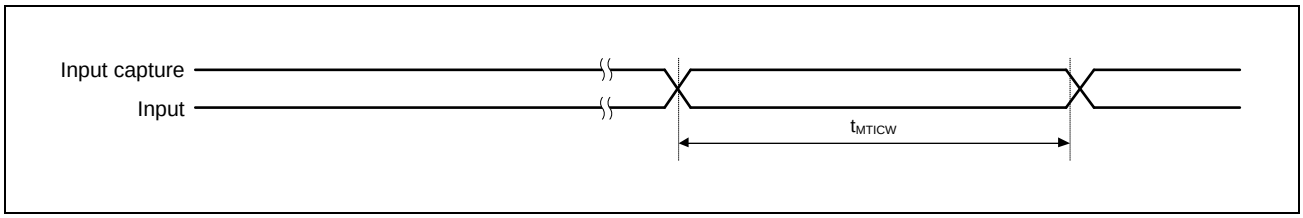


Figure 3.38 MTU3a Input Capture Input Timing

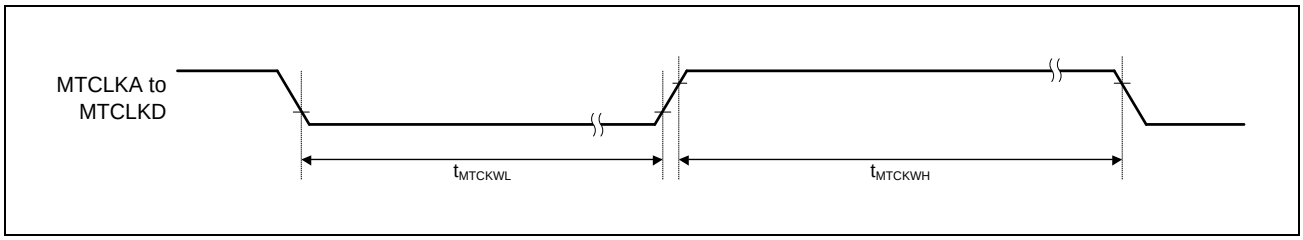


Figure 3.39 MTU3a Clock Input Timing

3.5.12 Port Output Enable 3 (POE3) Access Timing

Table 3.33 POE3 Timing

Item		Symbol	Min.	Max.	Unit	Figures
POE3	POEn# input pulse width	t_{POE3W}	1.5	—	t_{p1cy}*1	**Figure 3.40**

Note 1. t_{p1cyc} indicates peripheral clock means POE3_CLKM_POE (P0ϕ).

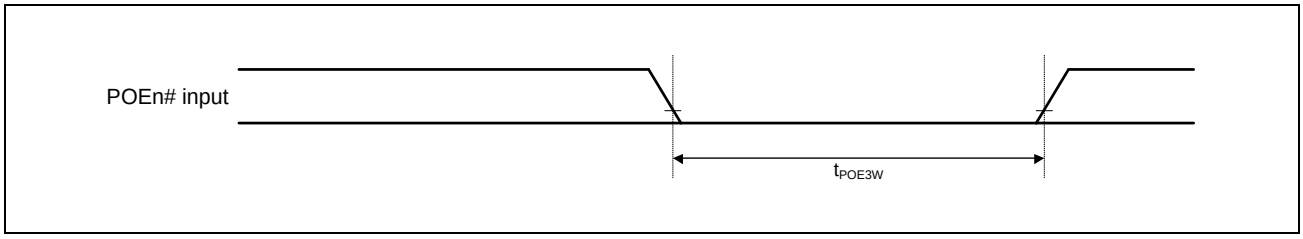


Figure 3.40 POEn# Input Pulse Timing

3.5.13 General PWM Timer (GPT) Access Timing

Table 3.34 GPT Timing

Item			Symbol	Min.	Max.	Unit	Figures
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{p1cyc}*1	**Figure 3.41**
		Both-edge setting		2.5	—		

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means GPT_PCLK (P0ϕ).

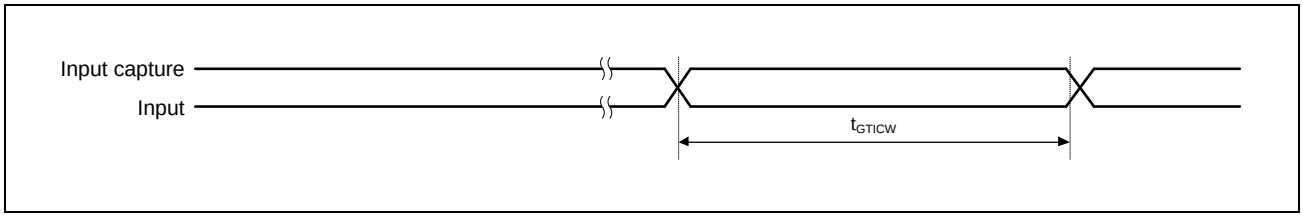


Figure 3.41 GPT Input Capture Input Timing

3.5.14 Port Output Enable for GPT (POEG) Access Timing

Table 3.35 POEG Timing

Item		Symbol	Min.	Max.	Unit	Figures
POEG	POEG input pulse width	t_{POEGW}	3	—	t_{p1cyc}*1	**Figure 3.42**

Note 1. t_{p1cyc} indicates peripheral clock means POEG_x_CLKP (P0ϕ) (x = A, B, C, D).

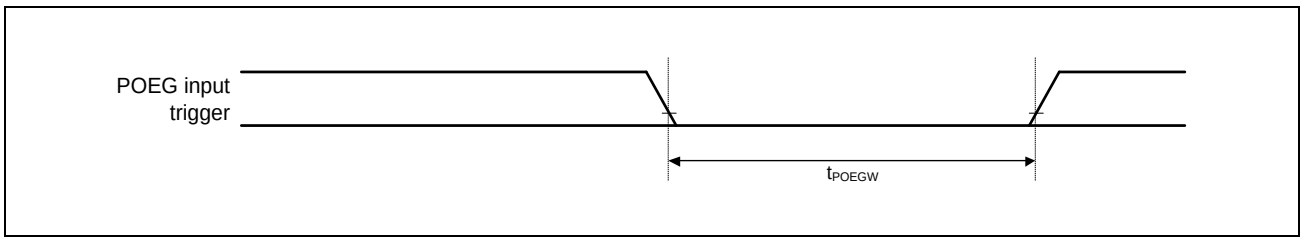


Figure 3.42 POEG Input Trigger Timing

3.5.15 I²C Bus Interface Access Timing

Table 3.36 I²C Bus Interface Timing

Item	Symbol	I/O	Standard Mode (Sm)		Fast Mode (Fm)		Fast Mode Plus (Fm+)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{CLK}	I/O	0	100	0	400	0	1000	kHz
Bus free time (between stop and start condition)	t_{BUF}	I/O	4.7	—	1.3	—	0.5	—	µs
Hold time*1	$t_{HD:STA}$	I/O	4.0	—	0.6	—	0.26	—	µs
Low period of SCL clock	t_{LOW}	I/O	4.7	—	1.3	—	0.5	—	µs
High period of SCL clock	t_{HIGH}	I/O	4.0	—	0.6	—	0.26	—	µs
Setup time for start / restart condition	$t_{SU:STA}$	I/O	4.7	—	0.6	—	0.26	—	µs
Data hold time (I²C bus device)	$t_{HD:DAT}$	I/O	0*2	—	0*2	—	0	—	µs
Data setup time	$t_{SU:DAT}$	I/O	250	—	100*3	—	50	—	ns
SDA and SCL signal rise time	t_R	Input	—	1000	20	300	—	120	ns
SDA and SCL signal fall time*3	t_F	Input	—	300	20 × (PV_{DD18}/ 5.5 V)	300	20 × (PV_{DD18}/ 5.5 V)	120	ns
		Output	—	300	20 × (PV_{DD18}/ 5.5 V)*6	300*6	20 × (PV_{DD18}/ 5.5 V)*7	120*7	ns
Setup time for STOP condition	$t_{SU:STO}$	I/O	4.0	—	0.6	—	0.26	—	µs
Capacitive load for each bus line	C_b	—	—	400*4	—	400*4	—	550*4	pF
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	Input	—	—	0	50*5	0	50*5	ns

Note: In the above table and subsequently, SCL and SDA refer to the RIICnSCL and RIICnSDA signals, respectively.

Note: AC access timing condition: drive ability 4 mA, output load 400 pF

Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.

Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the CnSCL signal reaches V_{IL} (max.) from V_{IH} (min.)).

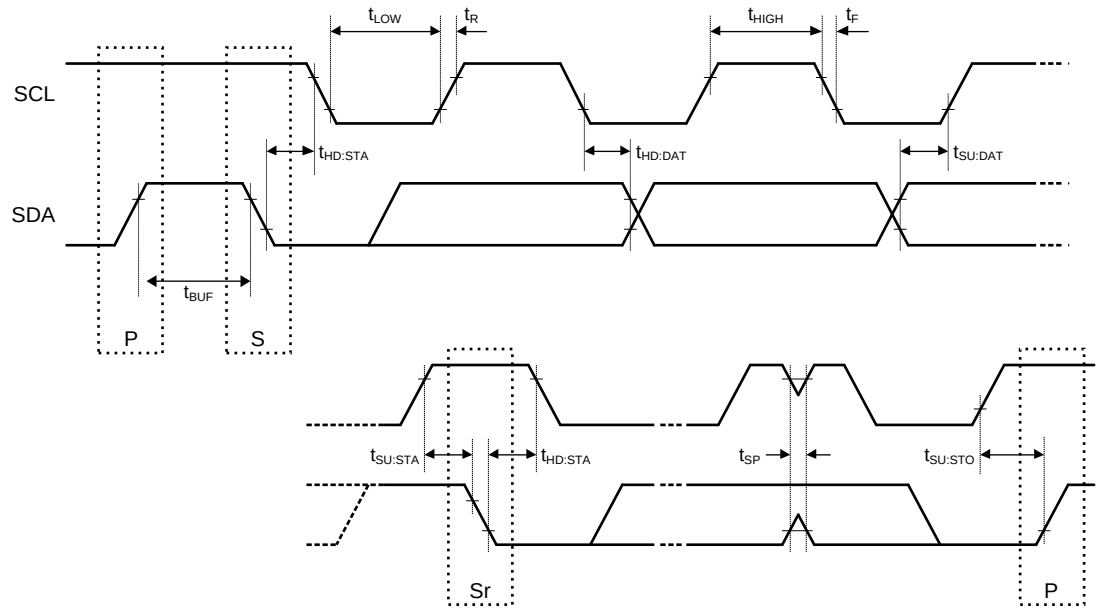
Note 3. The fast-mode I²C bus device can be used in the standard mode I²C bus system. In this case, the minimum value of the data setup time ($t_{SU:DAT}$ (min.) 250 [ns]) must be satisfied.
If the system does not extend the low period of SCL clock (t_{LOW}), this condition is automatically satisfied. If the system extends the low period of SCL clock (t_{LOW}), transmit the subsequent data bit to the SDA line before the SCL line is released (t_R (max.) + $t_{SU:DAT}$ (min.) = 1000 + 250 = 1250 [ns]: (standard mode I²C bus specification)).

Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I²C bus specification provided by NXP Semiconductors.

Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICϕ) and the NF[1:0] bits in RIICnMR3. For details, refer to *Section 25, I²C Bus Interface*, in the *User's Manual: Hardware*.

Note 6. When using RIIC ch2 or RIIC ch3, the following limitations exists.
- Driving ability: IOLH_xx[1:0] = 01b
- Tfmin cannot meet the specification when the load of bus line is less than 200 pF.
- The range of pull-up resistance (Rp) (in the case of 200/300/400 pF)
  Cb is 200 pF: 1076.7 to 1770Ω, Cb is 300 pF: 966.7 to 1180Ω, Cb is 400 pF: 856.7 to 885Ω

Note 7. When using RIIC ch2 or RIIC ch3, the following limitations exists.
- Driving ability: IOLH_xx[1:0] = 11b
- The range of pull-up resistance (Rp) (in the case of 10/150/275/400/550 pF)
  Cb is 10 pF: 300 to 14163Ω, Cb is 150 pF: 300 to 944Ω, Cb is 275 pF: 300 to 515Ω, Cb is 400 pF: 300 to 354Ω, Cb is 550 pF: 300Ω (fixed)
- Tfmin cannot meet the specification in fast-mode plus.



Note: P: Stop condition
S: Start condition
Sr: Start condition for retransmission

Figure 3.43 Input/Output Timing

3.5.16 I3C Bus Interface Access Timing

Table 3.37 Characteristics of the SDA and SCL Bus Lines for Standard, Fast, and Fast-Mode Plus I²C-Bus Devices*1

Item	Symbol	Conditions	Standard-Mode		Fast-Mode		Fast-Mode Plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		0	100	0	400	0	1000	kHz
Hold time (repeated) START condition	$t_{HD:STA}$	After this period,the first clock pulse is generated	4.0	—	0.6	—	0.26	—	µs
LOW period of the SCL clock	t_{LOW}		4.7	—	1.3	—	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	0.26	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	0.26	—	µs
Data hold time*2	$t_{HD:DAT}$	I²C-bus device	0 *3	—*4	0*3	—*4	0	—	µs
Data setup time	$t_{SU:DAT}$		250	—	100	—	50	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	—	120	ns
Fall time of both SDA and SCL signals*3,*6,*7	t_f		—	300	20 × (I3C_PV_{DD}/ 5.5 V)	300	20 × (I3C_PV_{DD}/ 5.5 V)*8	120*7	ns
Setup time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	0.26	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	0.5	—	µs

Note 1. All values referred to V_{IH}(min) (0.3 × I3C_PV_{DD}) and V_{IL}(max) (0.7 × I3C_PV_{DD}) levels, refer to **Table 3.6**

Note 2. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.

Note 3. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 4. The maximum $V_{HD:DAT}$ could be 3.45 µs and 0.9 µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period () of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.

Note 5. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU:DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Note 6. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

Note 7. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

Note 8. Necessary to be backwards compatible to Fast-mode.

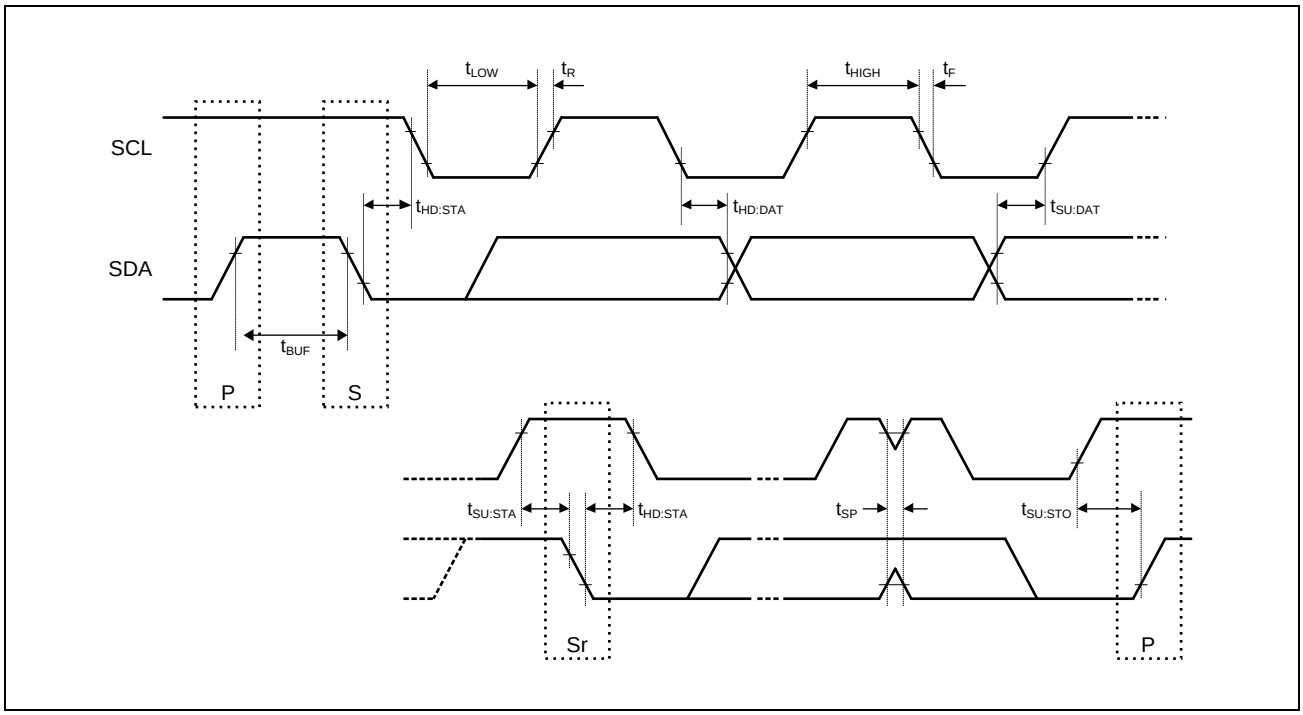


Figure 3.44 Input/Output Timing

Table 3.38 I3C Open Drain Timing Parameters

Item	Symbol	I3C Open Drain Mode			Figures	Notes
		Min.	Max.	Unit		
Low Period of SCL Clock	t_{LOW_OD}	200	—	ns	**Figure 3.48**	*1, *2
	$t_{DIG\_OD\_L}$	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	**Figure 3.48**	
High Period of SCL Clock	t_{HIGH}	—	41	ns	**Figure 3.46**	*3, *4
	t_{DIG_H}	—	t_{HIGH} + t_{CF}	ns	**Figure 3.46**, **Figure 3.55**	
Fall Time of SDA Signal	t_{fDA_OD}	t_{CF}	12	ns	**Figure 3.48**	
SDA Data Setup Time During Open Drain Mode	t_{SU_OD}	3	—	ns	**Figure 3.47**, **Figure 3.48**	*1
Clock After START(S) Condition	t_{CAS}	38.4 nano	For ENTAS0: 1 µ For ENTAS1: 100 µ For ENTAS2: 2 milli For ENTAS3: 50 milli	seconds	**Figure 3.48**	*5, *6
Clock Before STOP(P) Condition	t_{CBP}	t_{CASmin}/2	—	seconds	**Figure 3.49**	
Current Master to secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	**Figure 3.54**	
Bus Available Condition	t_{AVAL}	1	—	µs	—	*7
Bus Idle Condition	t_{IDLE}	200	—	µs	—	
Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	**Figure 3.54**	

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{fDA_ODtyp} + t_{SU_ODmin}.

Note 2. The Master may use a shorter low period if it knows that this is safe, i.e., that SDA is already above V_{IH}.

Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect.

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short bus).

Note 5. On a Legacy Bus where I^2C Devices need to see Start, the t_{CAS}(min) value is further constrained.

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS}(max) value shown for ENTAS3.

Note 7. On a Mixed Bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF}).

Table 3.39 I3C Push-Pull Timing Parameters for SDR Mode

Item		Symbol	Min.	Typ.	Max.	Unit	Figures	Notes
SCL Clock Frequency		f_{SCL}	0.01	12.5	12.9	MHz	—	*1
SCL Clock Low Period		t_{LOW}	24	—	—	ns	**Figure 3.45**	—
		t_{DIG_L}	32	—	—	ns	**Figure 3.46**	*2, *4
SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24	—	—	ns	**Figure 3.46**	—
		$t_{DIG\_H\_MIXED}$	32	—	45	ns	**Figure 3.46**	*2, *3
SCL Clock High Period		t_{HIGH}	24	—	—	ns	**Figure 3.45**	—
		t_{DIG_H}	32	—	—	ns	**Figure 3.46** **Figure 3.45**	*2
Clock in to Data Out for Slave		t_{SCO}	—	—	12	ns	**Figure 3.51**	*7, *8
SCL Clock Rise Time		t_{CR}	—	—	150e06 × 1 / f_{SCL} (capped at 60)	ns	**Figure 3.45**	*5
SCL Clock Fall Time		t_{CF}	—	—	150e06 × 1 / f_{SCL} (capped at 60)	ns	**Figure 3.45**	*5
SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP}	t_{CR} + 3 and t_{CF} +3	—	—	—	**Figure 3.50**	*4, *6
	Slave	t_{HD_PP}	0	—	—	—	**Figure 3.52**	*6
SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	3	—	N/A	ns	**Figure 3.50**, **Figure 3.51**	—
Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	—	N/A	ns	**Figure 3.53**	—
Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	—	N/A	ns	**Figure 3.53**	—
Capacitive Load per Bus Line (SDA/SDL)		C_b	—	—	50	pF	—	—

Note 1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})

Note 2. t_{DIG_L} and t_{DIG_H} are the clock low and high periods as seen at the receiver end of the I3C bus using V_{IL} and V_{IH} (see **Figure 3.45**).

Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.

Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

Note 5. The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.

Note 6. t_{HD_PP} is a Hold time parameter for Push-Pull Mode that has a different value for Master mode vs. Slave mode. In SDR Mode the Hold time parameter is referred to as t_{HD_SDR}.

Note 7. Devices with more than 12 ns of t_{SCO} delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Master to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.

Note 8. Pad delay based on 90Ω/4 mA driver and 50 pF load. Note that Master may be a Slave in a multi-Master system, and thus shall also adhere to this requirement.

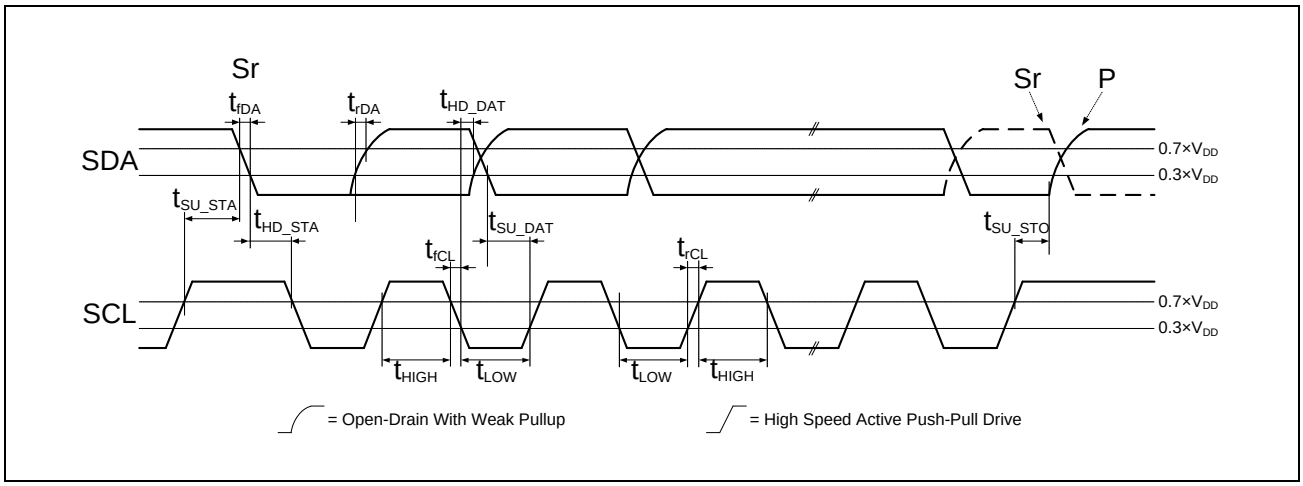


Figure 3.45 I3C Legacy Mode Timing

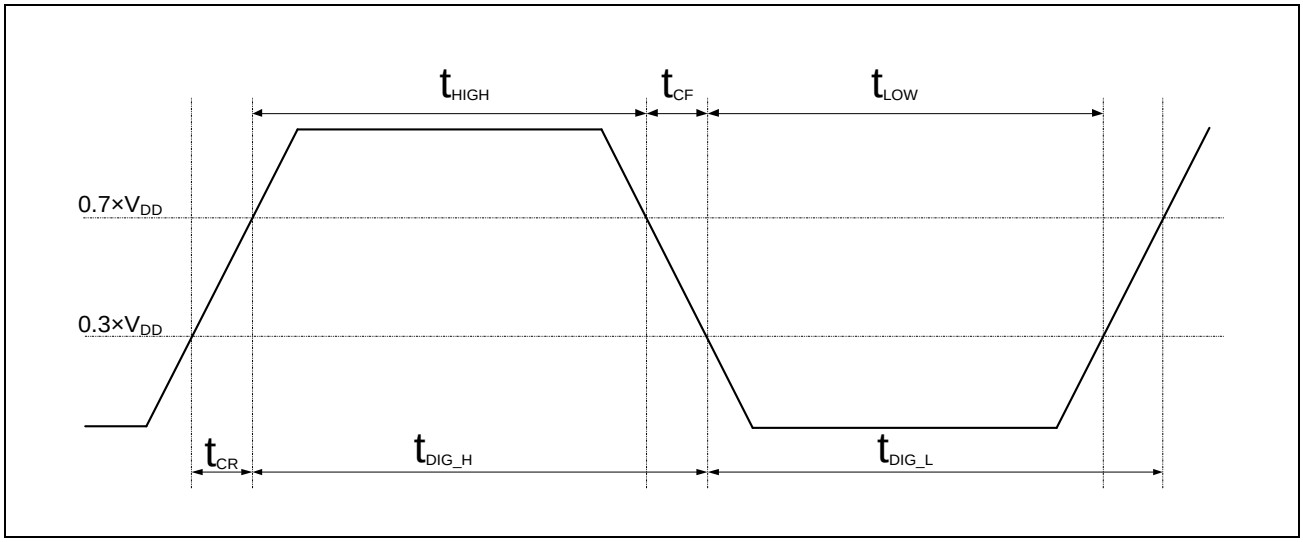


Figure 3.46 t_{DIG_H} and t_{DIG_L}

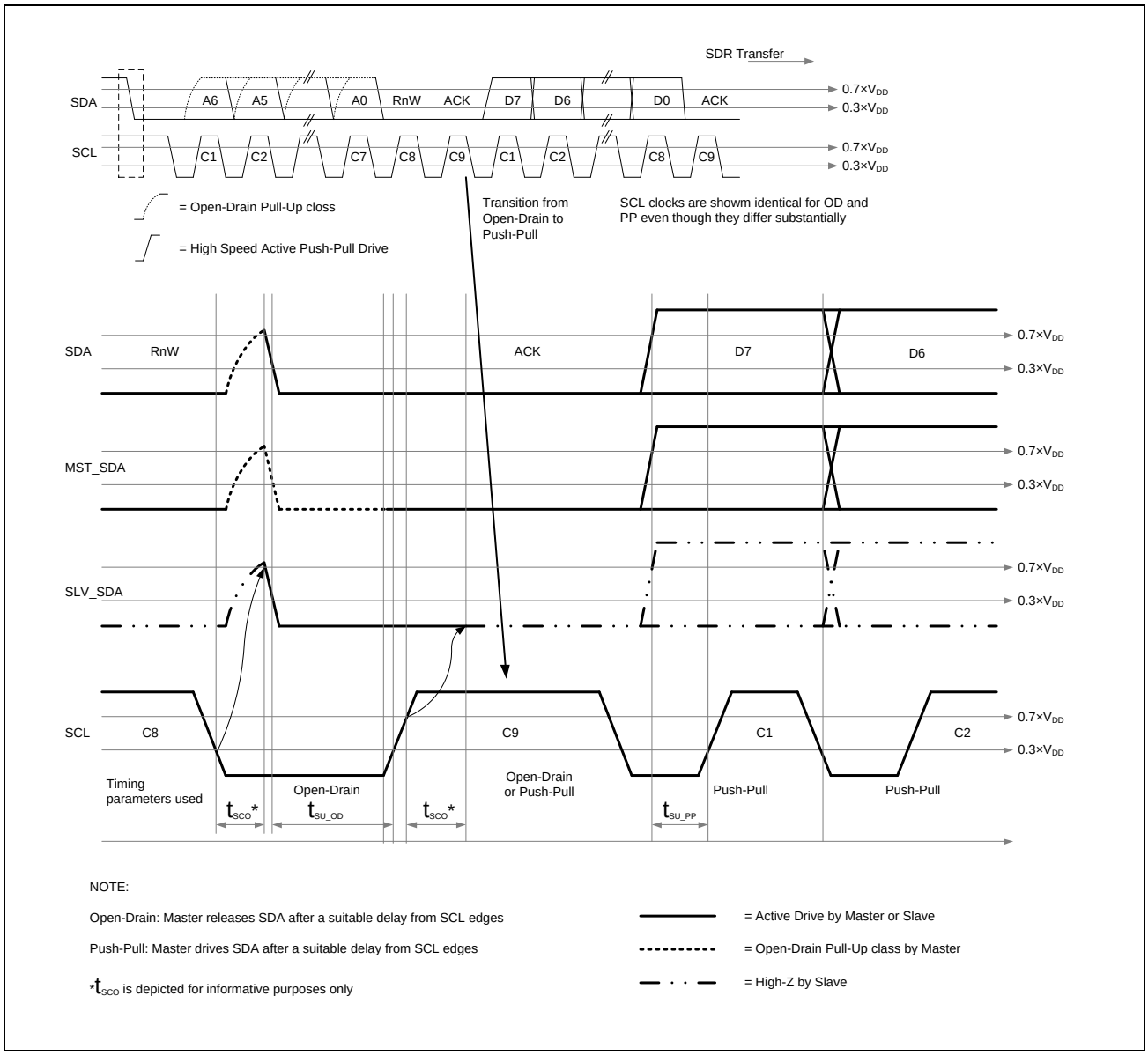


Figure 3.47 I3C Data Transfer – ACK by Slave

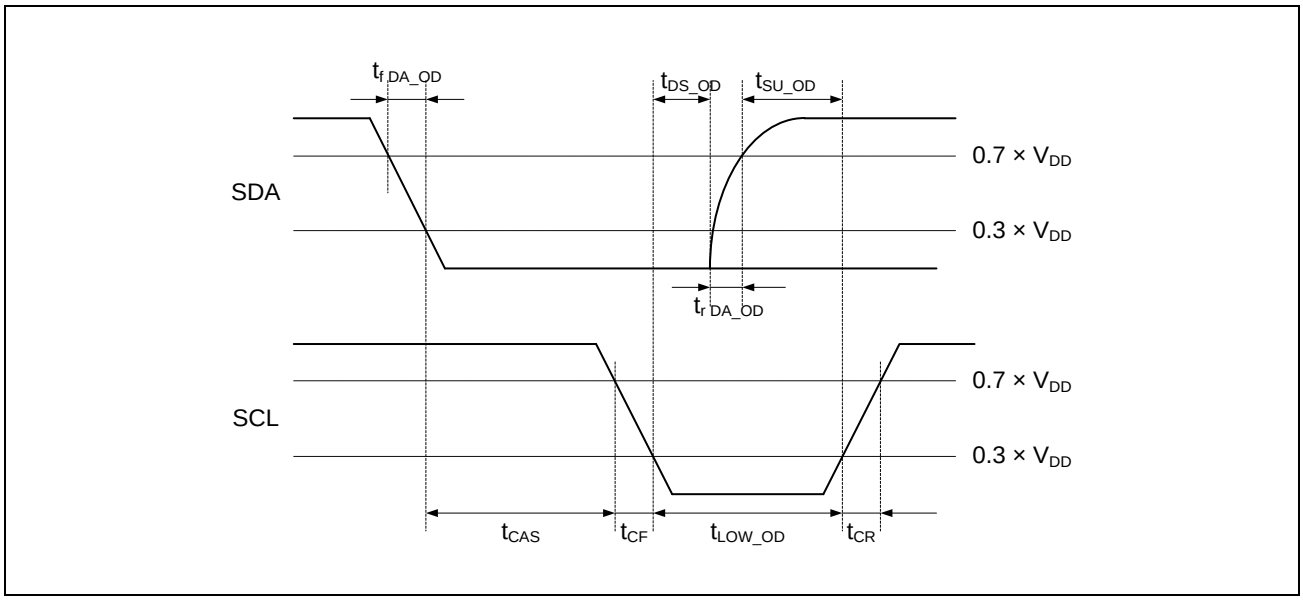


Figure 3.48 I3C START Condition Timing

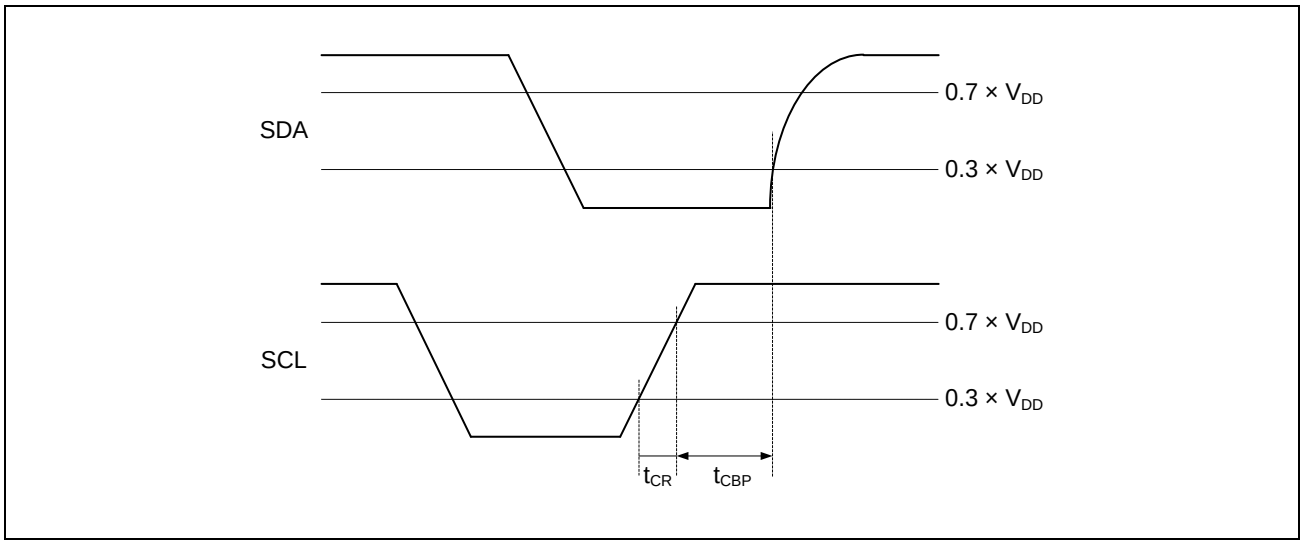


Figure 3.49 I3C STOP Condition Timing

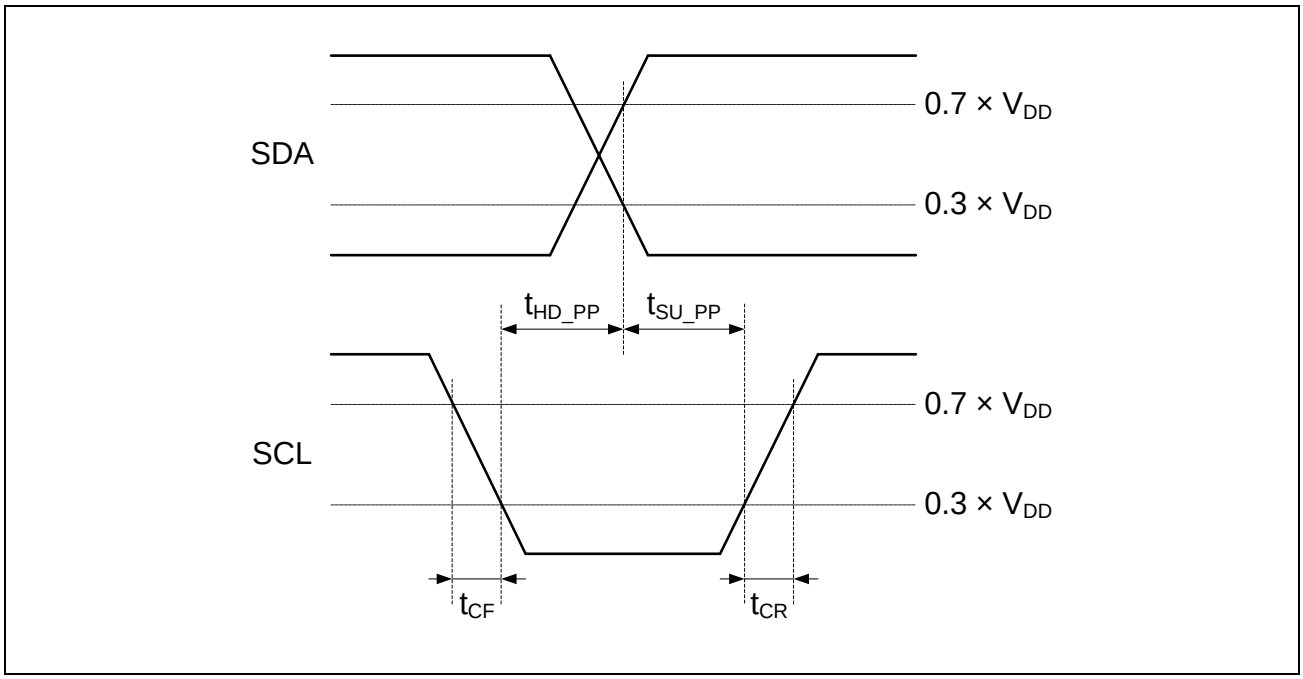


Figure 3.50 I3C Master Out Timing

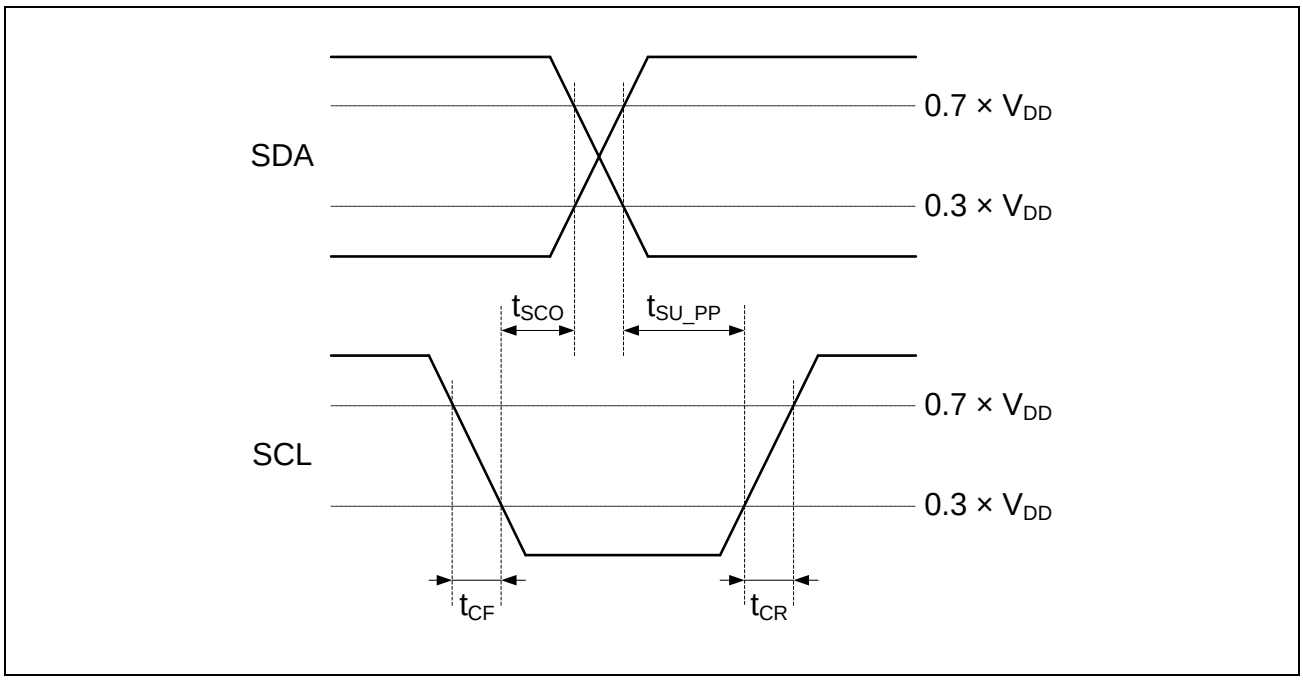


Figure 3.51 I3C Slave Out Timing

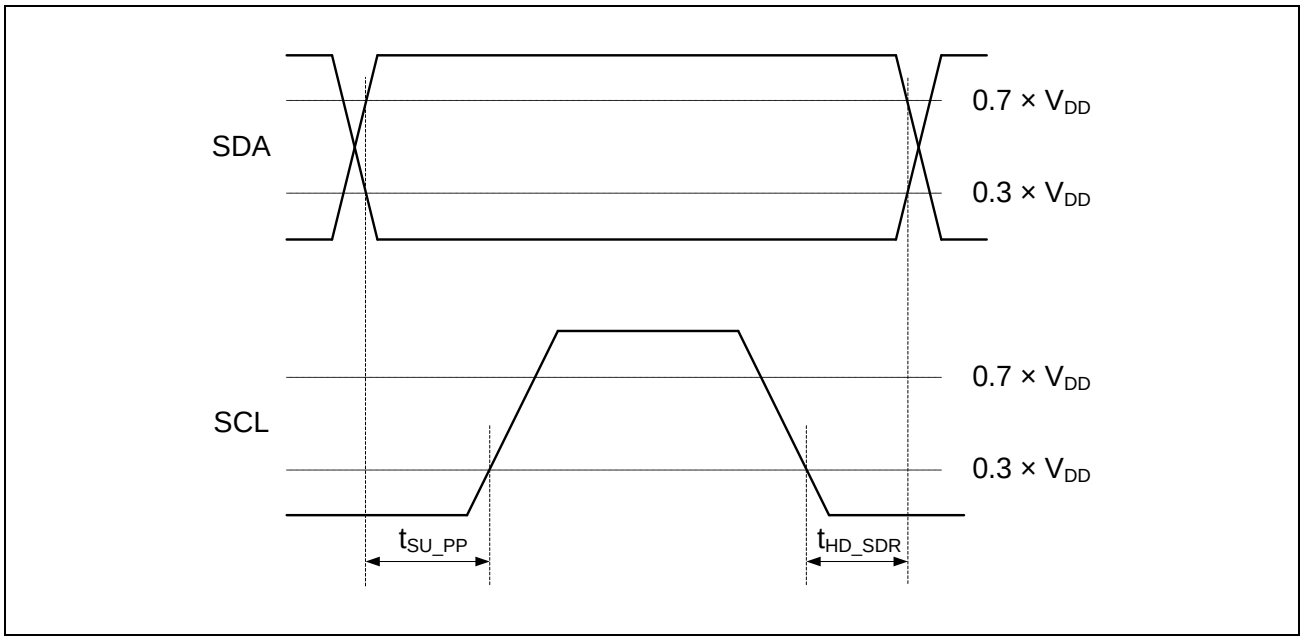


Figure 3.52 Master SDR Timing

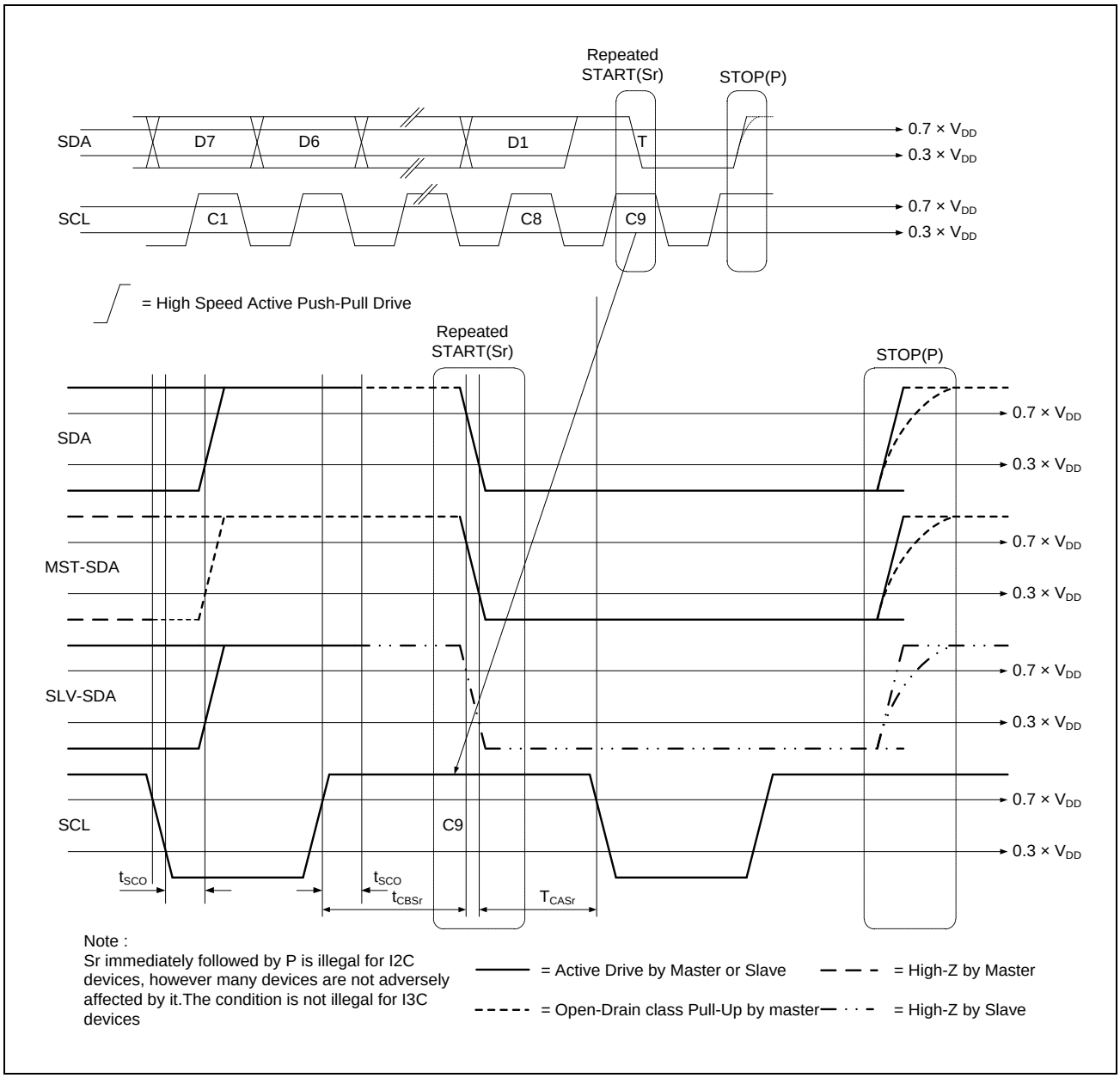


Figure 3.53 T-Bit When Master Ends Read with Repeated START and STOP

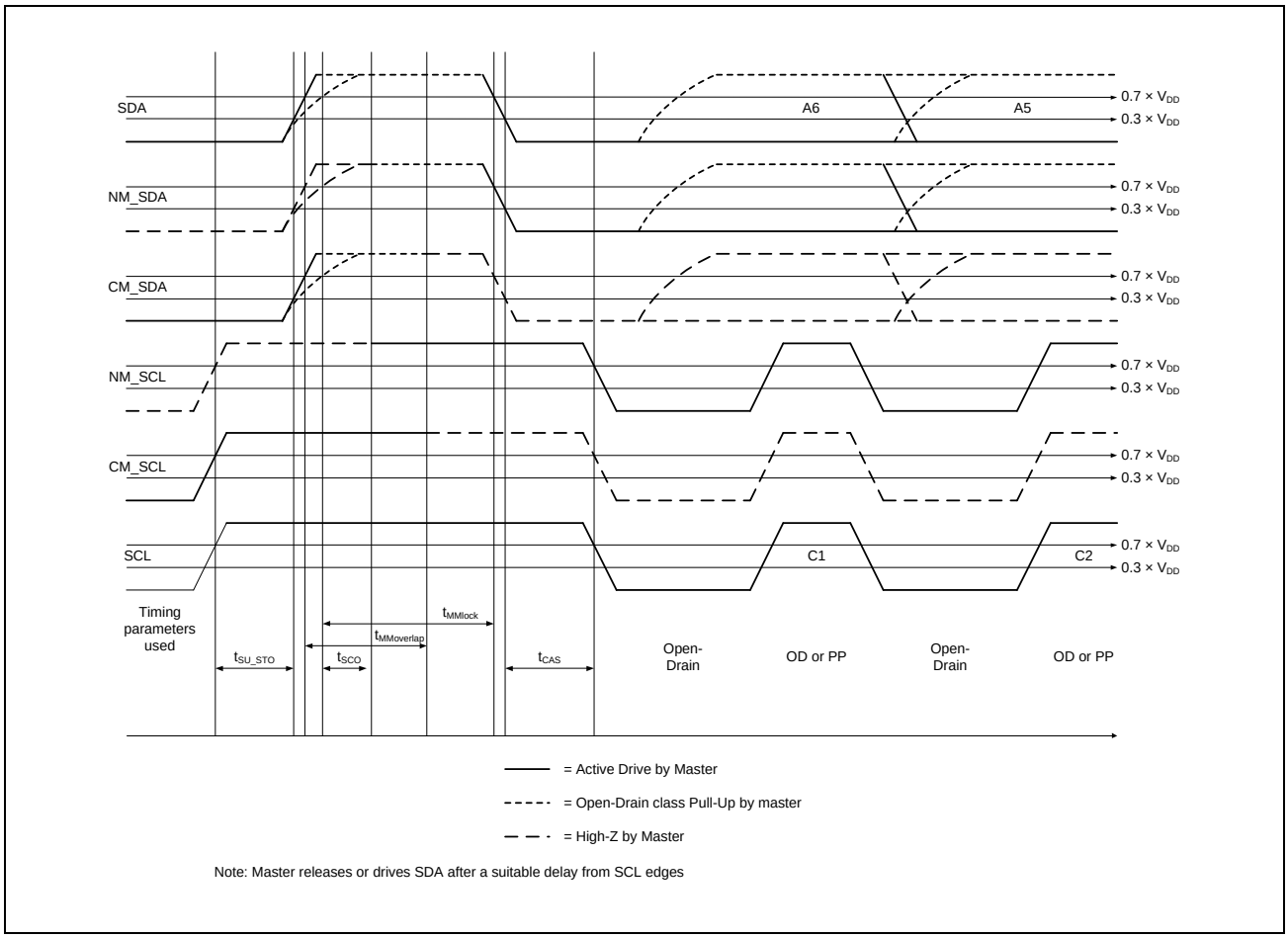


Figure 3.54 I3C Timing

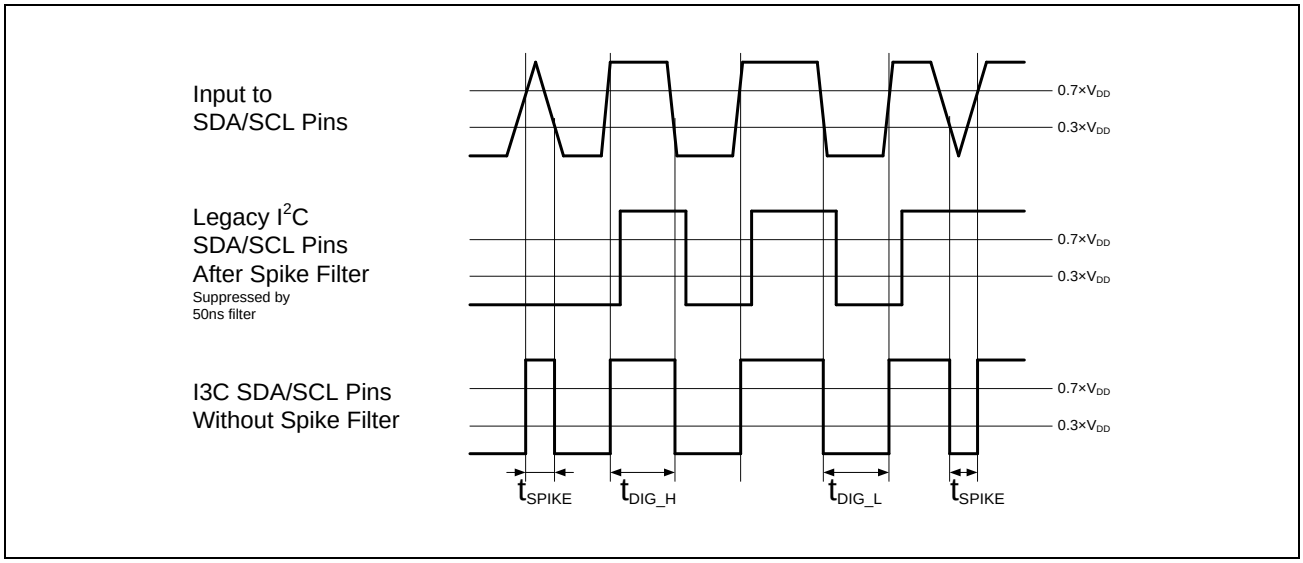


Figure 3.55 I2C Spike Filter Behavior

3.5.17 Serial Communications Interface with FIFO (SCIFA) Access Timing

Table 3.40 SCIFA Timing

Item			Symbol	Min.	Max.	Unit	Figures
SCIFA	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{p1cyc}*1	**Figure 3.56**
		Clocked synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{p1cyc}*1	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{p1cyc}*1	
		Clocked synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{p1cyc}*1	
	Output clock rise time		t_{SCKr}	—	9	ns	
	Output clock fall time		t_{SCKf}	—	9	ns	
	Transmit data delay time	Internal clock	t_{TXD}	−10	10	ns	**Figure 3.57**
		External clock		3 × t_{p1cyc}*1	4 × t_{p1cyc}*1 + 20		
	Receive data setup time	Internal clock	t_{RXS}	3 × t_{p1cyc}*1 + 20	—	ns	
		External clock		t_{p1cyc}*1 + 10	—		
	Receive data hold time	Internal clock	t_{RXH}	−3 × t_{p1cyc}*1	—	ns	
		External clock		2 × t_{p1cyc}*1 + 10	—		

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 11b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means SCIFn_CLK_PCK (P0ϕ) (n = 0 to 5).

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.

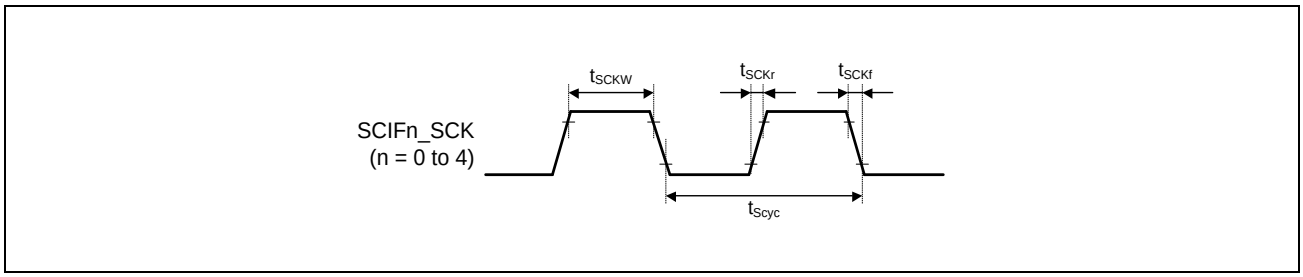
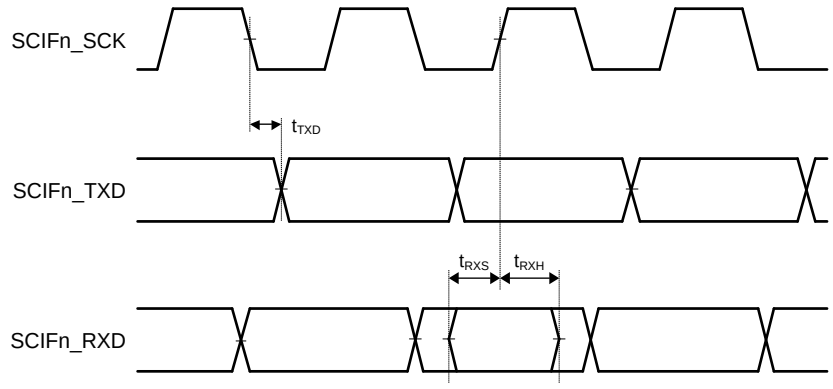


Figure 3.56 SCK Input Clock Timing



Note: n = 0 to 4

Figure 3.57 SCIFA Input/Output Timing in Clocked Synchronous Mode

3.5.18 Serial Communications Interface (SCIg) Access Timing

Table 3.41 SCIg Timing

Item			Symbol	Min.	Max.	Unit	Figures
SCIg	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{p1cyc}*1	**Figure 3.58**
		Clocked synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{p1cyc}*1	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{p1cyc}*1	
		Clocked synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{p1cyc}*1	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Clocked synchronous	t_{TXD}	—	28	ns	**Figure 3.59**
	Receive data setup time	Clocked synchronous	t_{RXS}	15	—	ns	
	Receive data hold time	Clocked synchronous	t_{RXH}	5	—	ns	

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 11b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means SCIn_CLKP (P0ϕ) (n = 0 to 1).

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.

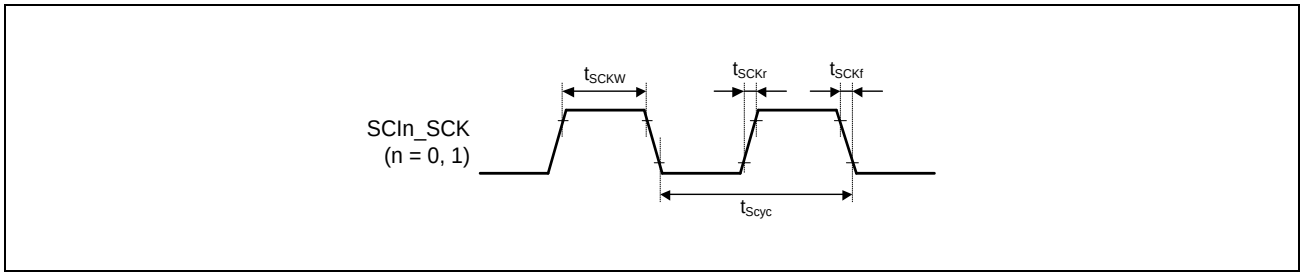
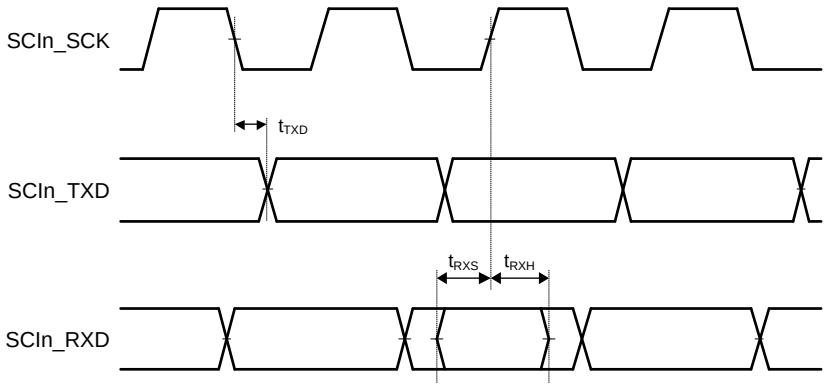


Figure 3.58 SCK Input Clock Timing



Note: n = 0, 1

Figure 3.59 SCIFA Input/Output Timing in Clocked Synchronous Mode

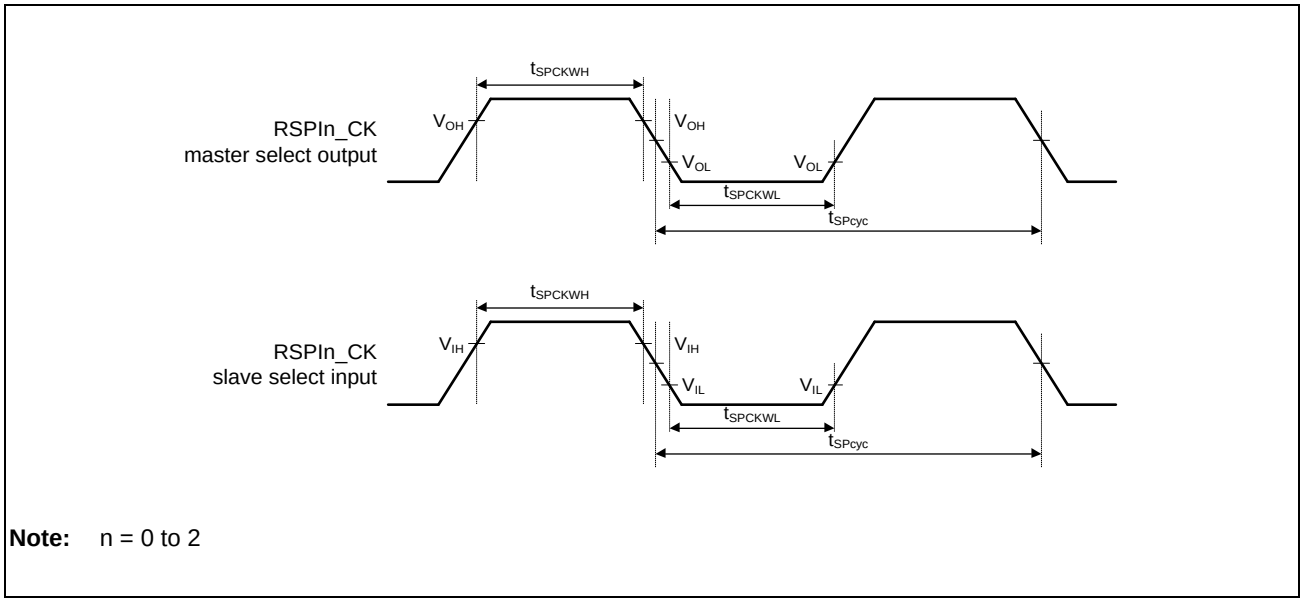
3.5.19 Renesas Serial Peripheral Interface (RSPI) Access Timing

Table 3.42 Renesas Serial Peripheral Interface Timing

Item		Symbol	Min.	Max.	Unit	Figure
RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{p1cyc}*1	**Figure 3.60**
	Slave		8	4096		
RSPCK clock high pulse width	Master	t_{SPCKWH}	0.4	—	t_{SPcyc}*1	
	Slave		0.4	—		
RSPCK clock low pulse width	Master	t_{SPCKWL}	0.4	—	t_{SPcyc}*1	
	Slave		0.4	—		
Data input setup time	Master	t_{SU}	10	—	ns	**Figure 3.61** to **Figure 3.64**
	Slave		0	—	t_{p1cyc}*1	
Data input hold time	Master	t_H	0	—	ns	
	Slave		4	—	t_{p1cyc}*1	
SSL setup time	Master	t_{LEAD}	1 × t_{SPcyc} − 20	8 × t_{SPcyc}	ns	
	Slave		4	—	t_{p1cyc}*1	
SSL hold time	Master	t_{LAG}	1 × t_{SPcyc}	8 × t_{SPcyc} + 20	ns	
	Slave		4	—	t_{p1cyc}*1	
Data output delay time	Master	t_{OD}	—	19	ns	
	Slave		—	4	t_{p1cyc}*1	
Data output hold time	Master	t_{OH}	5	—	ns	
	Slave		2	—	t_{p1cyc}*1	
Continuous transmission delay time	Master	t_{TD}	1 × t_{SPcyc} + 2 × t_{cyc}	8 × t_{SPcyc} + 2 × t_{cyc}	ns	
	Slave		4 × t_{cyc}	—		
Slave access time		t_{SA}	—	4	t_{p1cyc}*1	**Figure 3.63**, **Figure 3.64**
Slave out release time		t_{REL}	—	3	t_{p1cyc}*1	

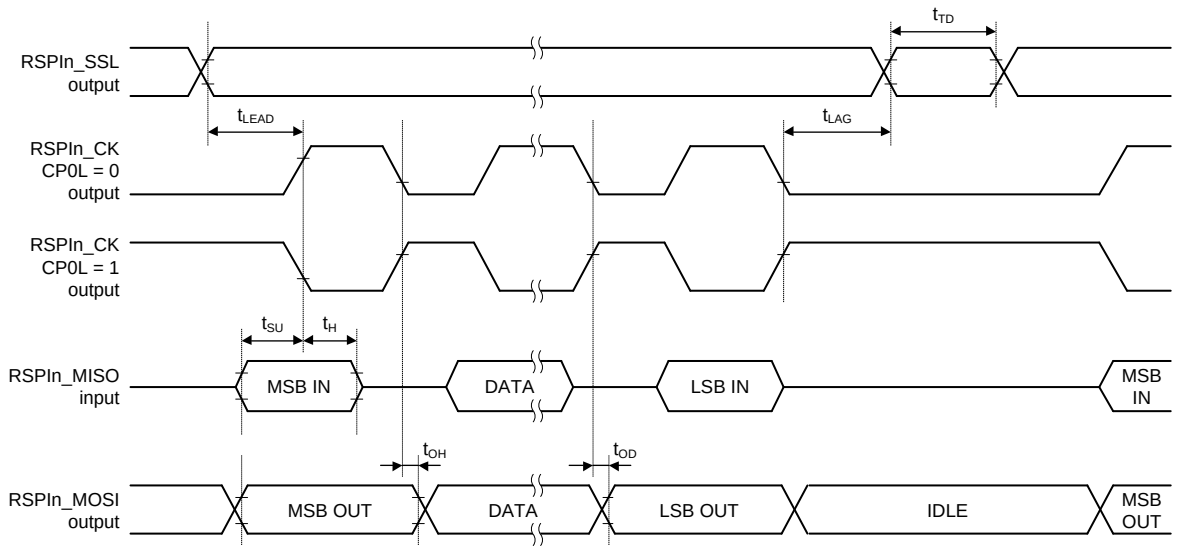
Note: AC access timing condition: drive ability IOLH_xx[1:0] = 11b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means RSPIn_CLKB (P0ϕ) (0 to 4).



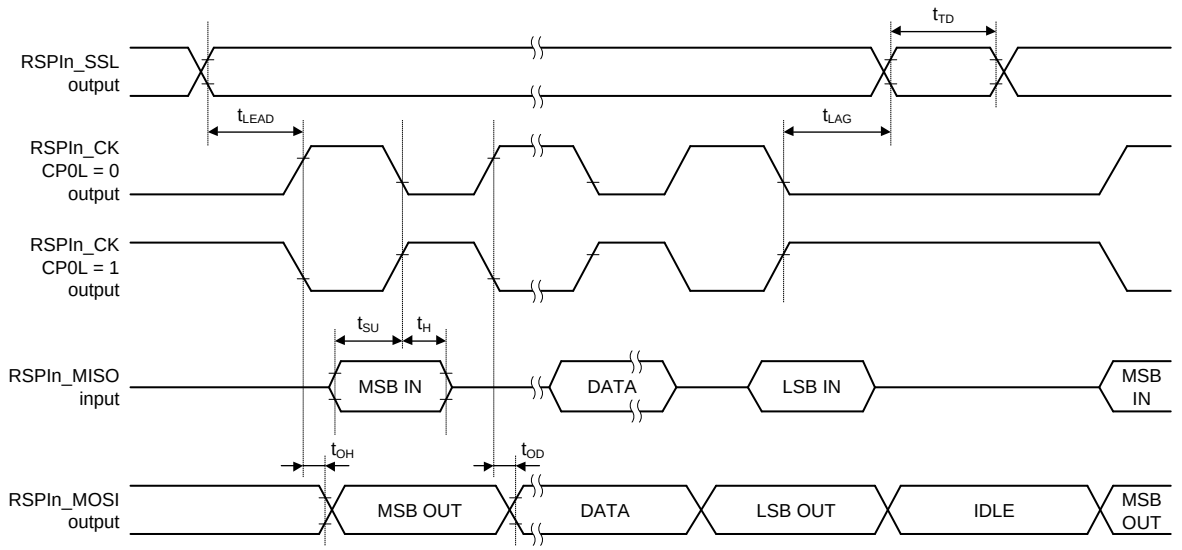
Note: n = 0 to 2

Figure 3.60 Clock Timing



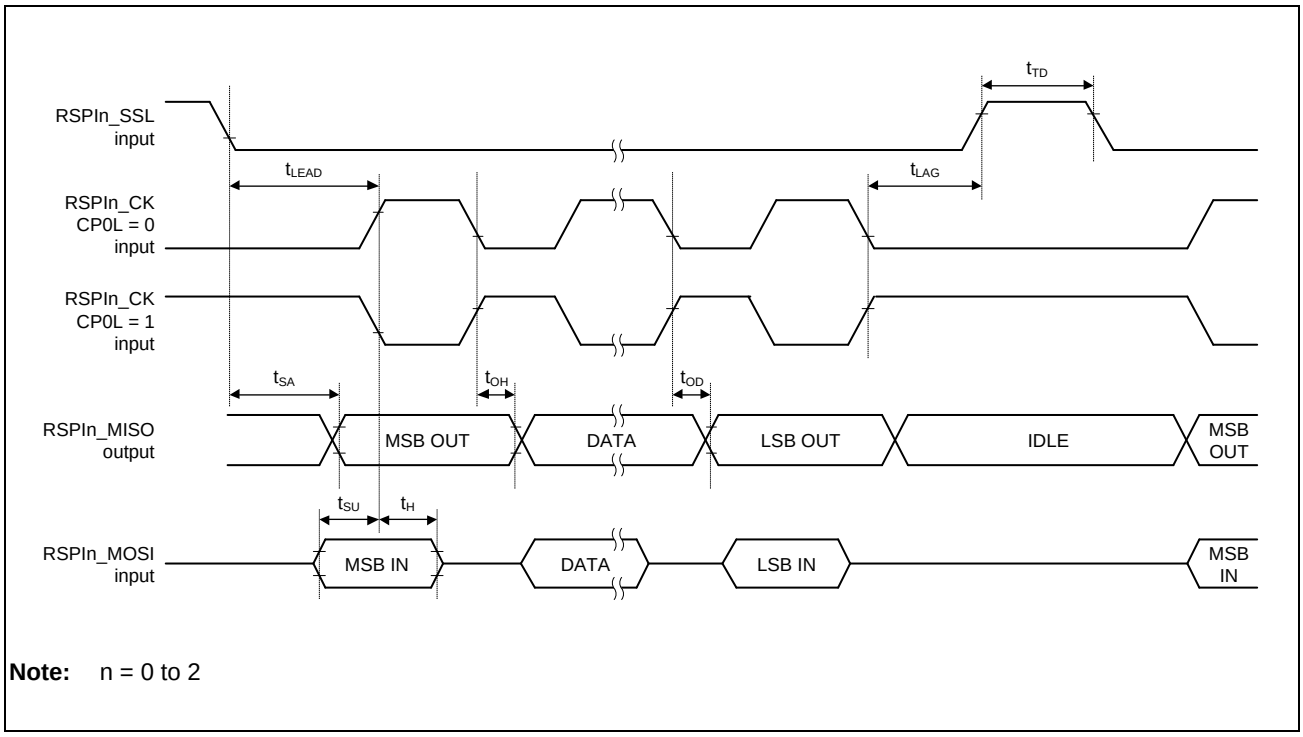
Note: n = 0 to 2

Figure 3.61 Transmission and Reception Timing (Master, CPHA = 0)



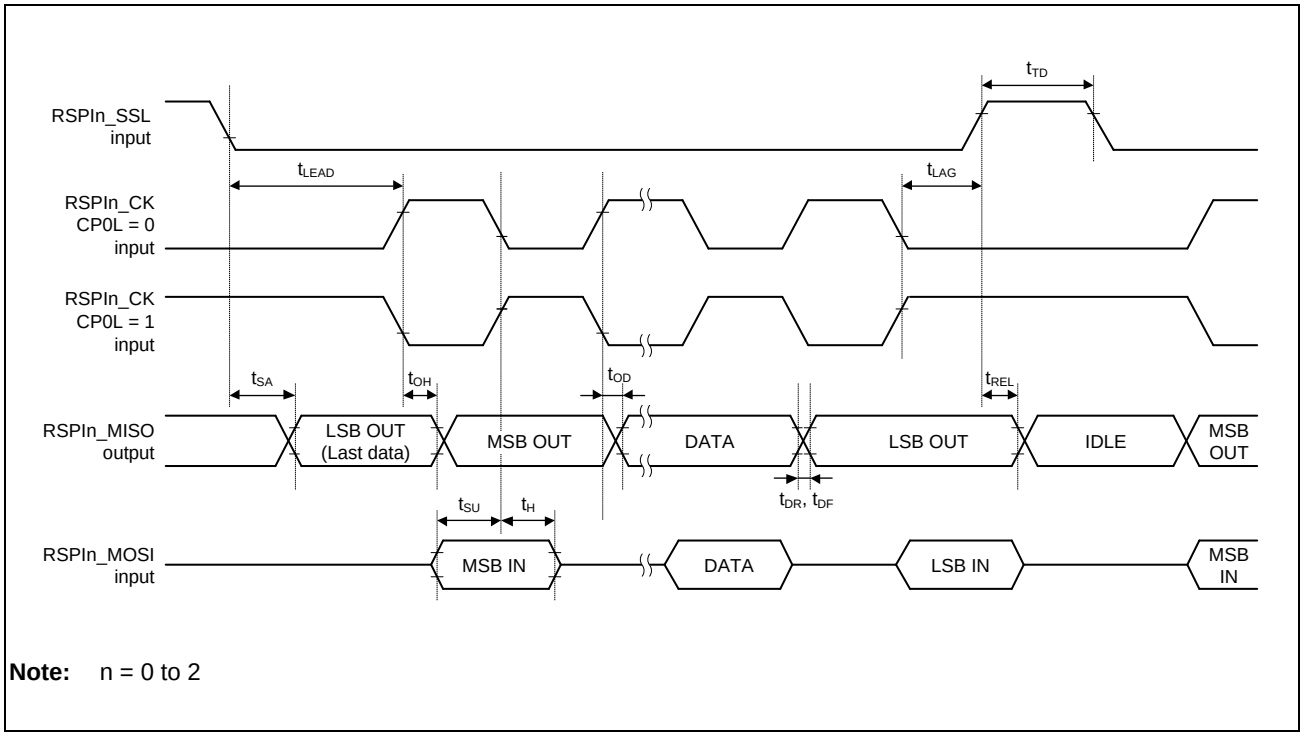
Note: n = 0 to 2

Figure 3.62 Transmission and Reception Timing (Master, CPHA = 1)



Note: n = 0 to 2

Figure 3.63 Transmission and Reception Timing (Slave, CPHA = 0)



Note: n = 0 to 2

Figure 3.64 Transmission and Reception Timing (Slave, CPHA = 1)

3.5.20 A/D Converter Access Timing

Table 3.43 A/D Converter Timing

Item	Symbol	Min.	Max.	Unit	Figures
ADC Trigger Input Pulse Width	t_{TRGW}	1.5*2		t_{P1cyc}*1	**Figure 3.65**

Note 1. t_{p1cyc} indicates peripheral clock means ADC_ADCLK (TSUϕ).

Note 2. When a noise filter in ADC is off.

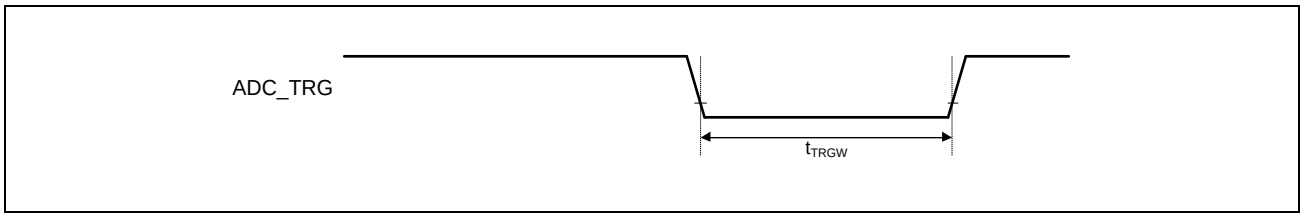


Figure 3.65 ADC Trigger Input Timing

3.5.21 Watchdog Timer Access Timing

Table 3.44 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figures
WDTOVF_PERROUT# Output Time	t_L	64	64	t_{P1cyc}*1	**Figure 3.66**

Note 1. t_{P1cyc} indicates peripheral clock means WDTn_CLK (OSCCLK) (n = 0 to 2).

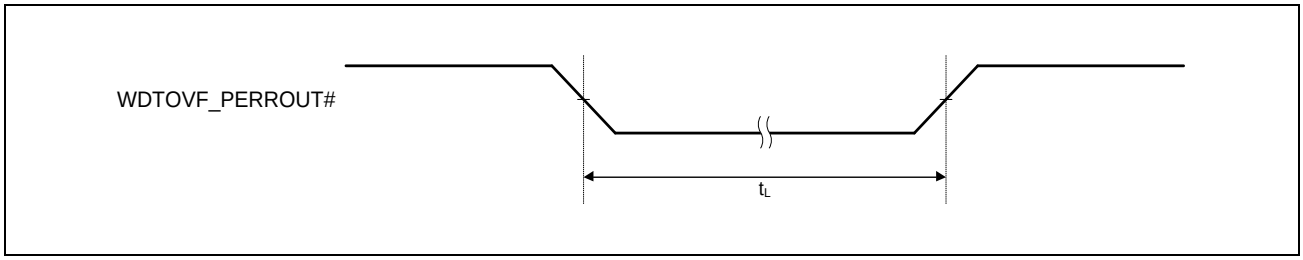


Figure 3.66 Watchdog Timer Output Timing

3.5.22 PDM Interface Access Timing

Table 3.45 PDM Interface Timing

Item	Symbol	Min.	Max.	Unit	Remarks
Clock period	t_{PSYNC}	2	32	t_{CCcyc} = 125 ns (8 MHz)	
Clock High level period	t_{PDCKWH}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	
Clock Low level period	t_{PDCKWL}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	

Note: I/O driving ability: IOLH_xx[1:0] = 01b, CL = 30 pF

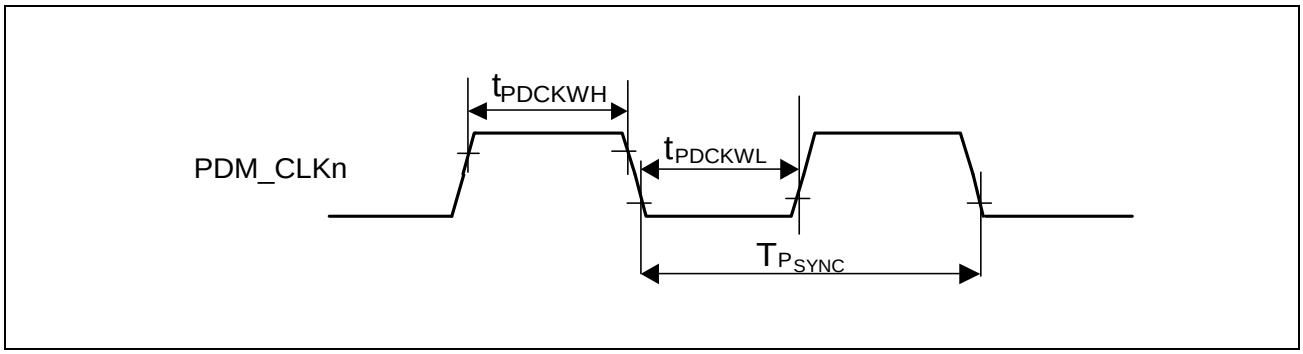


Figure 3.67 Timing of Clock Output (PDMn_CLK)

Table 3.46 PDM Interface Timing

Item	Symbol	Min.	Max.	Unit	Remarks
PDMn_DAT input setup time	t_{SU}	12.5	—	ns	
PDMn_DAT input hold time	t_H	0.0	—	ns	

Note: I/O driving ability: IOLH_xx[1:0] = 01b, CL = 30 pF

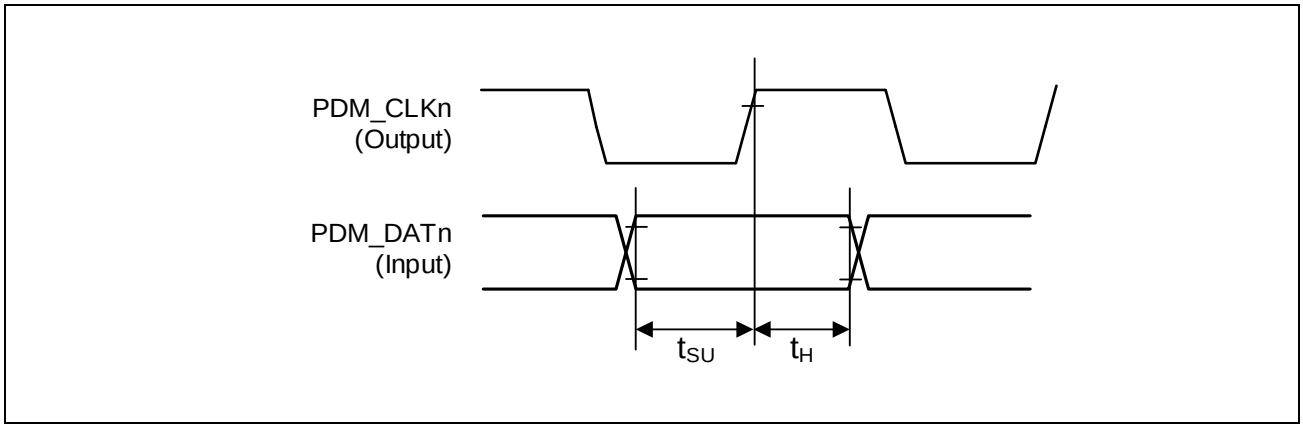


Figure 3.68 Receive Timing (Synchronized with the Rise of PDMn_CLK)

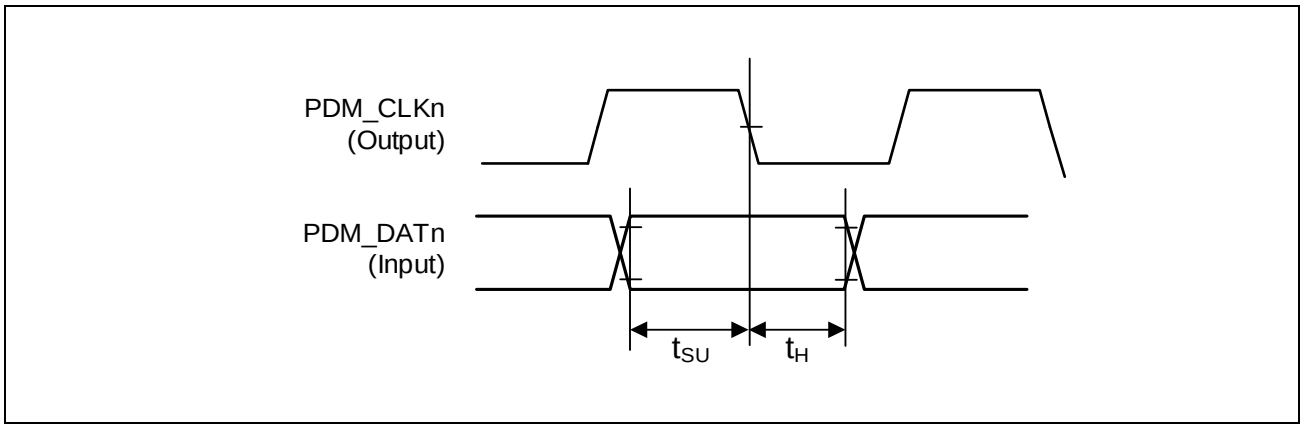


Figure 3.69 Receive Timing (Synchronized with the Fall of PDMn_CLK)

3.5.23 Octa Memory Controller Timing

Table 3.47 Octa Memory Controller Timing*1,*2

Item		Symbol	Min.	Max.	Unit	Figures
QSPI0_SPCLK clock frequency		f_{OCcyc}	—	100	MHz	**Figure 3.70**
QSPI0_SPCLK high pulse width		t_{OCwh}	0.45	0.55	t_{OCcyc}	
QSPI0_SPCLK low pulse width		t_{OCwl}	0.45	0.55	t_{OCcyc}	
QSPI0_SPCLK rise time		t_{OCr}	—	1	ns	
QSPI0_SPCLK fall time		t_{OCf}	—	1	ns	
OM_CS1#, QSPI0_SSL setup time	SPI/SOPI	t_{OCLEAD}	$1 \times t_{OCcyc} - 3$ (Minimum register settings)	$2.5 \times t_{OCcyc} + 3$ (Maximum register settings)	ns	**Figure 3.71**, **Figure 3.72**
	DOPI	t_{OCLEAD}	$0.75 \times t_{OCcyc} - 3$ (Minimum register settings)	$2.25 \times t_{OCcyc} + 3$ (Maximum register settings)	ns	**Figure 3.73**
OM_CS1#, QSPI0_SSL hold time	SPI/SOPI	t_{OCLAG}	$1 \times t_{OCcyc} - 3$ (Minimum register settings)	$4.5 \times t_{OCcyc} + 3$ (Maximum register settings)	ns	**Figure 3.71**, **Figure 3.72**
	DOPI read	t_{OCLAG}	$3.25 \times t_{OCcyc} - 3$ (Minimum register settings)	$4.25 \times t_{OCcyc} + 3$ (Maximum register settings)	ns	**Figure 3.73**
	DOPI write	t_{OCLAG}	$0.75 \times t_{OCcyc} - 3$ (Minimum register settings)	$4.25 \times t_{OCcyc} + 3$ (Maximum register settings)	ns	
Continuous transfer delay time		t_{OCTD}	$1 \times t_{OCcyc} - 3$ (Minimum register settings)	$8.5 \times t_{OCcyc} + 3$ (Maximum register settings)	ns	**Figure 3.71**, **Figure 3.72**, **Figure 3.73**
Data input setup time	QSPI0_SPCLK base point	t_{SU}	8.5	—	ns	**Figure 3.71**
Data input hold time		t_H	0.5	—	ns	
Data input setup time	SOPI/DOPI DQS base point*3	t_{SU}	−0.7	—	ns	**Figure 3.72**, **Figure 3.73**
Data input hold time		t_H	2.775	—	ns	
Skew of Clock to Data Strobe		t_{CKDS}	—	20	ns	
Data output delay time	SPI/SOPI	t_{OD}	—	1.4	ns	**Figure 3.71**, **Figure 3.72**
Data output hold time		t_{OH}	−1.4	—	ns	
Data output buffer off time	SOPI	t_{BOFF}	2	—	ns	**Figure 3.72**
Data output delay time	DOPI*3	t_{OD}	2.775	—	ns	**Figure 3.73**, **Figure 3.74**
Data output hold time		t_{OH}	0.975	—	ns	
Data output buffer off time	DOPI	t_{BOFF}	0.9	—	ns	**Figure 3.73**
DQS refresh input setup time		t_{DQSS}	12	—	ns	**Figure 3.75**
DQS refresh input hold time		t_{DQSH}	$0.5 \times t_{OCcyc}$	—	ns	

Note 1. t_{OCcyc} indicates the QSPI0_SPCLK cycle.

Note 2. Maximum load capacitance: 15 pF

Note 3. QSPI0_SPCLK frequency: 100 MHz

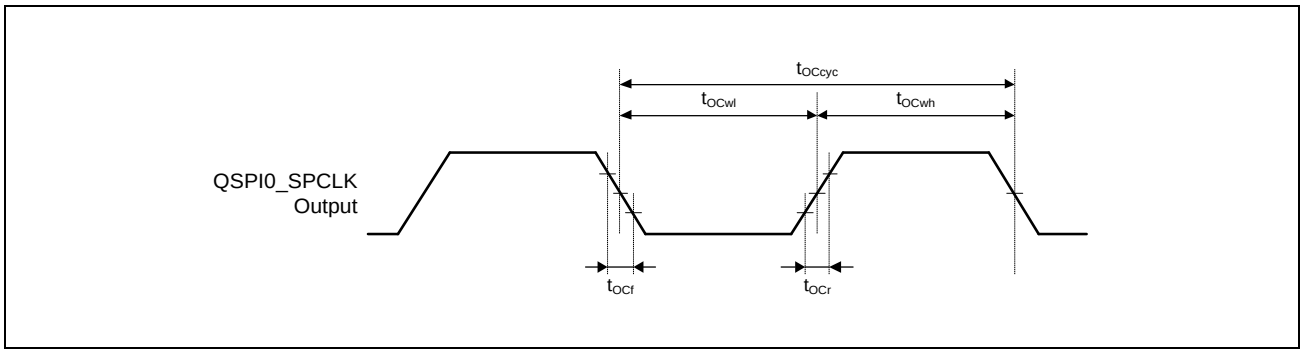


Figure 3.70 Clock Timing

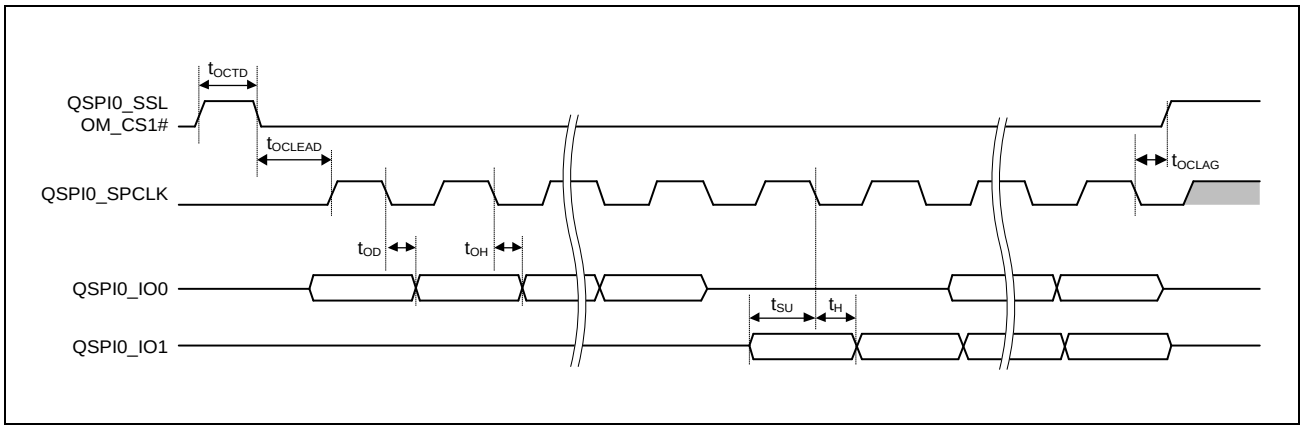


Figure 3.71 SPI Transferring Format Transmission and Receiving Timing

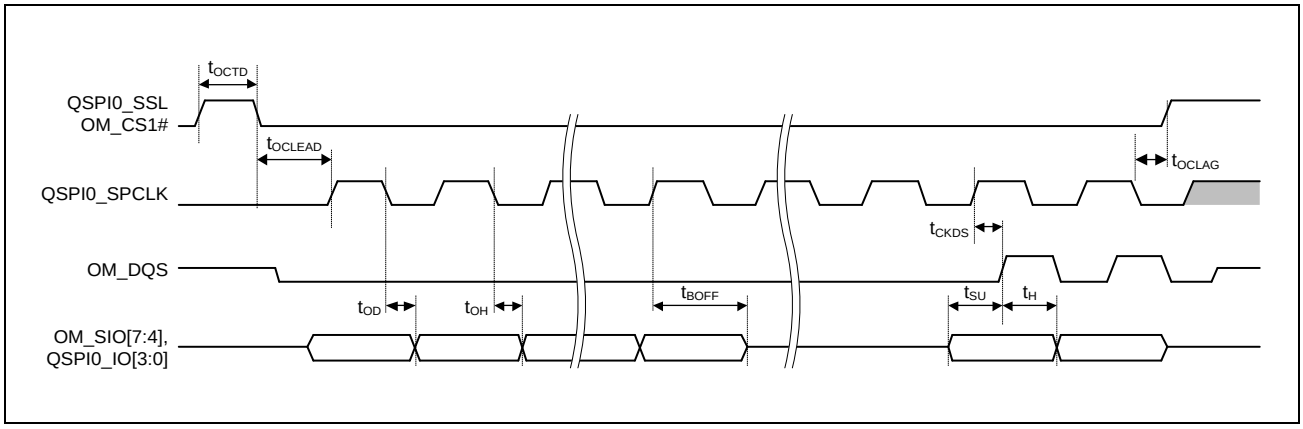


Figure 3.72 SOPI Transferring Format Transmission and Receiving Timing

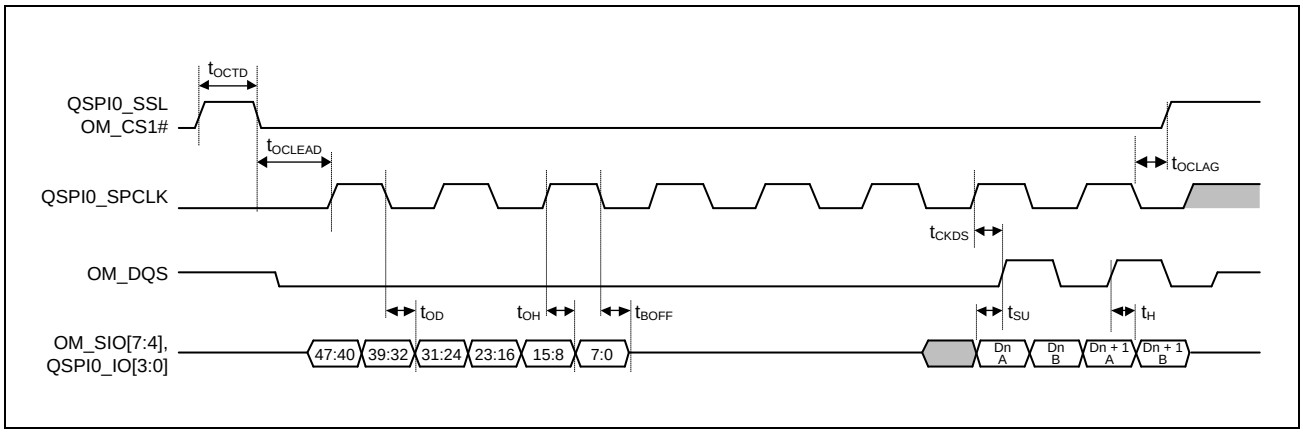


Figure 3.73 DOPI Transferring Format Transmission and Receiving Timing

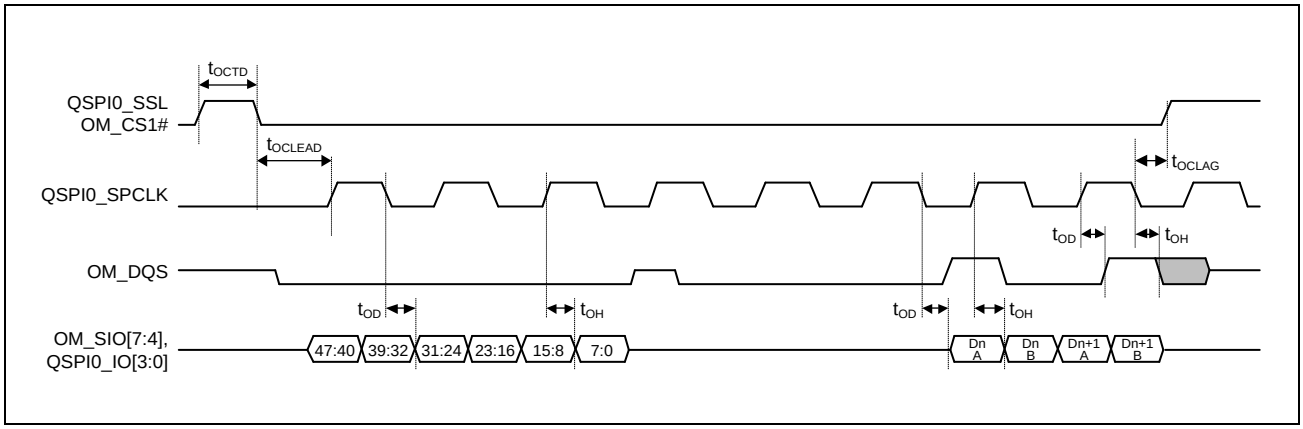


Figure 3.74 DOPI Transferring Format Transmission Timing

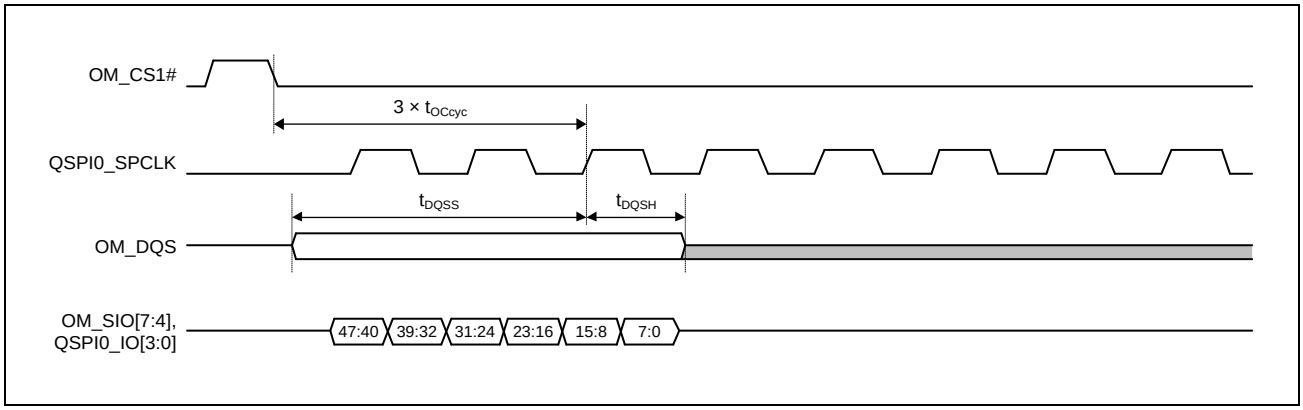


Figure 3.75 DQS Refresh Input Timing (OctaRAM Read and Write)

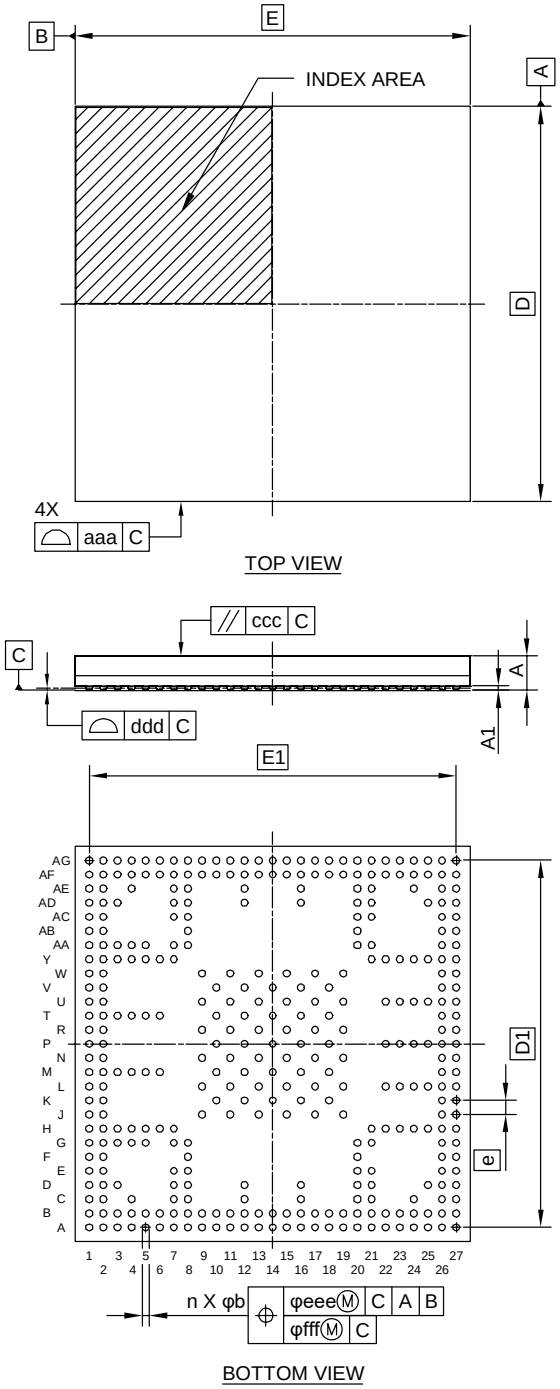
3.5.24 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of the PCI Express® Base Specification for Gen1/Gen 2/ Gen 3

4. Package Dimensions

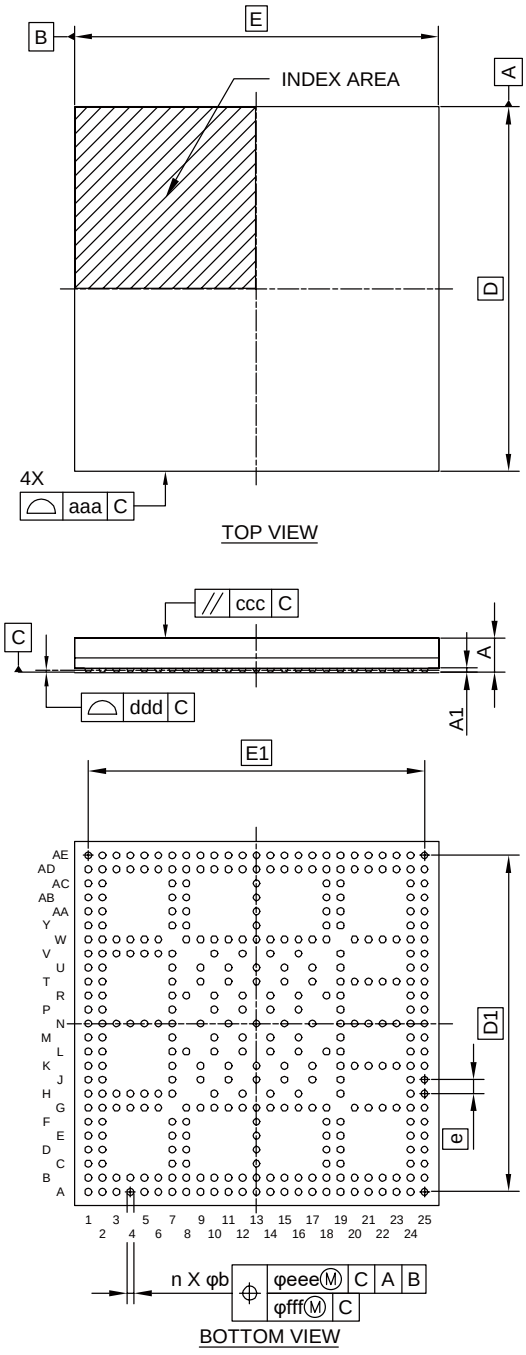
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA359-14x14-0.50	PLBG0359KA-A	0.45



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	–	14.00	–
E	–	14.00	–
D1	–	13.00	–
E1	–	13.00	–
A	–	–	1.40
A1	0.11	–	–
b	0.20	0.25	0.30
e	–	0.50	–
aaa	–	–	0.15
ccc	–	–	0.20
ddd	–	–	0.08
eee	–	–	0.15
fff	–	–	0.08
n	–	359	–

Figure 4.1 Package Dimensions (359Pin BGA)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA361-13x13-0.50	PLBG0361KD-A	0.40



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	13.00	—
E	—	13.00	—
D1	—	12.00	—
E1	—	12.00	—
A	—	—	1.40
A1	0.11	—	—
b	0.20	0.25	0.30
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.08
n	—	361	—

Figure 4.2 Package Dimensions (361Pin BGA)

REVISION HISTORY	RZ/G3S Group DATASHEET

Rev.	Date	Description	
		Page	Summary
1.00	Dec 25, 2024	—	First edition issued
1.10	Jul 31, 2025	1. Overview	
		11	1.1.15 Package: Package: The description, modified
		13	Figure 1.1 Configuration of LSI Internal Bus: Text, modified (MPU Bus → MCPU Bus) SRC, deleted
		2. Pin	
		15	2.1 Pin Assignment: The main text, modified
		15	2.2 External Pins and Multiplexed Functional Pins: The section title, modified. The main text, modified.
		3. Electrical Characteristics	
		18	Figure 3.1 Power-On/Power-Off Sequence 1 (All_OFF to ALL_ON, ALL_ON to ALL_OFF), modified (VBATTRESETN → VBATTRESET#). Note 7, added.
		19	Figure 3.2 Power-On/Power-Off Sequence 2 (ALL_ON to AWO_DDR_RETENTION, AWO_DDR_RETENTION to ALL_ON): The figure title, modified. The figure, modified (VBATTRESETN → VBATTRESET#) (AWO (+ DDR Retention) → AWO_DDR_RETENTION).
		—	Figure 3.3 Power-On/Power-Off Sequence 3 (ALL_ON to AWO, AWO to ALL_ON), deleted
		20	Figure 3.3 Power-On/Power-Off Sequence 3 (ALL_ON to VBATT_DDR_RETENTION, VBATT_DDR_RETENTION to ALL_ON): The figure title, modified. The figure, modified (VBATTRESETN → VBATTRESET#) (VBATT + DDR Retention → VBATT_DDR_RETENTION).
		21	Figure 3.4 Power-On/Power-Off Sequence 4 (ALL_ON to VBATT, VBATT to ALL_ON), added
		22	Table 3.3 DC Characteristics (1) [GP I/O (3.3 V)]: Input leakage current, added
		25	Table 3.11 DC Characteristics (9) [ADC]: Full-scale error, Offset error, Analog input capacitance, Analog input resistance, External capacitance, and External resistance, added. Note 1, added.
		26	Figure 3.5 Analog Input Equivalent Circuit, added
		27	Table 3.12 DC Characteristics (10) [Current Consumption] The Max current of Power Supply Voltage (I/O) and Power Supply Voltage (PCIe), modified. The Max current and Remarks of Power Supply Voltage (XSPI) (1.8 V), Power Supply Voltage (XSPI) (3.3 V), Power Supply Voltage (SD) (1.8 V), Power Supply Voltage (SD) (3.3 V), Power Supply Voltage (Ether) (1.8 V), Power Supply Voltage (Ether) (2.5 V), and Power Supply Voltage (Ether) (3.3 V), modified.
		33	Table 3.16 SDHC AC Access Timing (SDR at 3.3-V Operation) SD_CLK clock high level width, SD_CLK clock low level width, SD_CMD, and SD_DATA output delay: The Min values, modified
		34	Table 3.17 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply) SD0_CLK clock cycle, SD0_CLK clock high level width, SD0_CLK clock low level width, and SD0_CMD/SDDAT output delay: The Min values, modified
		34	Table 3.18 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply) SD0_CLK clock cycle, SD0_CLK clock high level width, and SD0_CLK clock low level width: The Min values, modified. SD0_CMD/SDDAT output delay: The Min and Max values, modified.
		35	3.5.4.2 eMMC Host Interface Timing (HS-SDR), modified
		36	Table 3.21 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF) SD0_CLK clock high level width, and SD0_CLK clock low level width: The Min values, modified. SD0_CMD/SDDAT output delay: The Min and Max values, modified.

Rev.	Date	Description	
		Page	Summary
1.10	Jul 31, 2025	41	Table 3.26 Ethernet-IF Access Timing (Ether MII): Note, modified
		42	Table 3.27 Ethernet-IF Access Timing (Ether RGMII): The Min and Max values of Duty_G, modified. Note 1, deleted. The Note number, modified (Note 2 → Note 1).
		46	Table 3.29 xSPI Timing: The Max value of “CS low to DS low”, modified. Note 6, modified. Notes 7 and 8, added.
		49	Table 3.30 SSIF-2 Timing: Note, modified
		51	Table 3.31 CAN-FD Interface Timing: Note, modified
		52	Table 3.32 MTU3a Timing: Note, modified
		54	Table 3.34 GPT Timing: Note, modified
		68	Table 3.40 SCIFA Timing: Note, modified
		70	Table 3.41 SCIg Timing: Note, modified
		72	Table 3.42 Renesas Serial Peripheral Interface Timing: Note, modified
		76	Table 3.45 PDM Interface Timing, Table 3.46 PDM Interface Timing: Note, modified
1.20	May 29, 2026	2. Pin	
		15	2.2 External Pins and Multiplexed Functional Pins: pin condition and Handling when the pin is not in use, modified
		3. Electrical Characteristics	
		76	Table 3.45 PDM Interface Timing: Clock High level period, and Clock Low level period: The Min and Max values, modified.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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