RZ/T2H and RZ/N2H Groups
RZ Arm-based High-end 32 & 64-bit MPUs

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600/1200 MHz, Cortex-A55 Quad/Dual/Single MPCore, 500/1000 MHz, Dual Arm® Cortex®-R52 on-chip FPU and NEON™, 2.0 MB of on-chip SRAM, LPDDR4-3200 with 32-bit, Ethernet MAC, EtherCAT, USB 2.0 high-speed, PCI Express Gen3, SD card host interface, CAN/CANFD, various communications interfaces such as an xSPI and ΔΣ interface, encoder interfaces, and security functions

Features

On-chip 64-bit Arm Cortex-A55 processor

- Quad/Dual/Single MPCore cores
- Maximum operating frequency:
  - Core: 600/1200 MHz
  - DSU: 500/1000 MHz
- 64-bit Arm Cortex-A55 Quad/Dual/Single MPCore cores (revision r2p0)
- Address space: 32 Gbytes
- L1 cache:
  - I-cache: 32 Kbytes (with parity)
  - D-cache: 32 Kbytes (with ECC)
- L2 cache: 0 bytes
- L3 cache: 1024 Kbytes (with ECC)
- NEON/FPU supported
- Cryptographic extension supported (Security product only)
- Arm V8.2-A architecture

On-chip 32-bit Arm Cortex-R52 processor

- High-speed realtime control with operating frequency of 500/1000 MHz
- On-chip Dual 32-bit Arm Cortex-R52 (revision r1p4)
- Tightly coupled memory (TCM) with ECC
  - CPU0, CPU1: 512 KB/64 KB
- Instruction cache/data cache with ECC
  - CPU0, CPU1: 16 KB per cache
- High-speed interrupt
- NEON/FPU supported
- Harvard architecture with 8-stage pipeline
- Supports the memory protection unit (MPU)
- Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces.
- No DCLS (Dual Core Lock Step) support

Low power consumption

- Standby mode and module stop function

On-chip SRAM

- 2.0 MB of the on-chip SRAM with ECC
- 250 MHz

LPDDR4 SDRAM Memory Interface

- Data transfer: 3.2 Gbps
- Bus width: 32-bit
- Rank: 1, 2
- Size: up to 64 Gb

Data transfer

- DMAC: 16 channels × 3 units

Event link controller

- Module operations can be started by event signals rather than by interrupt handlers.
- Linked operation of modules is available even while the CPU is in the standby state.

Reset and power supply voltage control

- Ten reset sources including a pin reset

Clock functions

- External clock/oscillator input frequency: 25 MHz
- CPU clock frequency: 600/1200 MHz (Cortex-A55), 500/1000 MHz (Cortex-R52)
- System clock frequency: 400 MHz (A-Bus), 250 MHz (R-Bus)
- Low-speed on-chip oscillator (LOCO): 1 MHz

Safety functions

- Register write protection, input clock oscillation stop detection and CRC
- Master Memory Protection Unit (MPU)

Security functions (optional)

- Boot mode with security through encryption
- JTAG authentication
- Cryptologic accelerator
- TRNG
- Cortex-A55 Crypto Extension
- Arm® TrustZone® technology

Encoder interfaces

- 16 channels
- EnDat 2.2, BiSS-C, A-format, and HIPERFACE DSL-compliant interfaces
- Frequency-divided output from an encoder

Various communications interfaces

- Ethernet
  - EtherCAT slave Controller: 3 ports
  - Ethernet switch: 3 ports
  - Ethernet MAC: 1 port × 3 units
- USB 2.0 high-speed host/functions: 1 channel
- CAN/CANFD (compliant with ISO11898-1): 2 channels
- SCI with 16-byte transmission and reception FIFOs: 6 channels + 12 channels (for encoder)
- I2C bus interface: 3 channel for transfer at up to 400 kbps
- SPI: 4 channels
- xSPI: 2 channels
- PCI Express Gen3: 2 lane × 1 port or 1 lane × 2 ports
- SD card host interface: 2 channels

External host interface

- Serial host interface

External address space

- Buses for high-speed data transfer at up to 125 MHz
- Support for up to 4 CS areas
- 8-, 16- or 32-bit bus space is selectable per area

Up to 73 extended-function timers

- 16-bit × 8 + 32-bit MTU3 (9 channels), 32-bit GPT (56 channels)
- 16-bit CMT (6 channels), 32-bit CMTW (2 channels)

ΔΣ interface

- Up to 30 ΔΣ modulators are connectable externally.

Trigonometric function unit

- 2 units
- Simultaneous calculation of sine and cosine
- Simultaneous calculation of arctangent and hypot_k

12-bit A/D converter

- 12 bits × 3 unit (4 channels for unit 0, 1, 15 channels for unit 2)

Temperature sensor for measuring temperature within the chip

LCD Controller

- Support Image Processing (Dither, Clipping, Gamma Correction)
- Parallel output interface
- Output Data Format: RGB666 / RGB888
- Support WXGA (1280 × 800), 60 fps

General-purpose I/O ports

- Input pull-up/pull-down
- The locations of input/output functions for peripheral modules are selectable from among multiple pins.

Operating temperature range

- Tj = -40 to +125°C

1. Overview

1.1 Outline of Specifications

The MPU is a high-performance ASSP that has Cortex-A55 quad MPCore and dual Arm Cortex®-R52 processor with Floating-Point Unit (FPU) and NEON™. It incorporates integrated peripheral functions necessary for system configuration.

Table 1.1 CPU

Feature	Functional description
Arm® Cortex®-A55	• One Processor which consist of Quad/Dual/Single MPCore cores • Operating frequency – Core: 600 MHz/1200 MHz – DSU: 500 MHz/1000 MHz • 64-bit CPU Cortex-A55 designed by Arm (core revision r2p0) • Address space: 32 GB • L1 cache – I-cache: 32 KB (with parity) each core – D-cache: 32 KB (with ECC) each core • L2 cache: 0 bytes • L3 cache: 1024 KB (with ECC) • Arm V8.2-A architecture • NEON/FPU supported • Cryptographic extension supported (Security product only)
Arm® Cortex®-R52	• Two processors which consist of single core • Operating frequency – Each CPU0 and CPU1: 500 MHz/1000 MHz • 32-bit CPU Cortex-R52 designed by Arm (core revision r1p4) • Address space: 4 GB • Instruction cache – Each CPU0 and CPU1: 16 KB (with ECC) • Data cache – Each CPU0 and CPU1: 16 KB (with ECC) • Tightly coupled memory (TCM) – Each CPU0 and CPU1 ATCM: 512 KB (with ECC) 0 wait (500 MHz) / 1 wait (1000 MHz) BTCM: 64 KB (with ECC) 0 wait CTCM: 0 KB • Instruction set: ARMv8-R architecture, so support includes Thumb® and Thumb-2 • Two stage Memory protection unit (MPU) • NEON/FPU supported

Table 1.2 Memory

Feature	Functional description
On-chip system SRAM with ECC	• Capacity: 2.0 MB (512 KB × 4 units) (with ECC) • Operating frequency: 250 MHz • SEC-DED (single error correction/double error detection) Error injection supported
One-time programmable memory	• Overwrite protection • Redundancy support • Available information – Unique ID – Authentication settings – Trimming data – Boot mode setting – User area
LPDDR4 SDRAM memory interface	• Data transfer: 3.2 Gbps • Bus width: 32 bits • Rank: 1, 2 • Size: up to 64 Gb • Inline ECC • No support of LPDDR4X

Table 1.3 System

Feature	Functional description
Operating modes	The operating mode can be selected from the following seven boot modes: ● xSPI0 boot mode (CS0 × 1 boot Serial Flash) ● xSPI0 boot mode (CS0 × 8 boot Serial Flash) ● eMMC boot mode ● SD boot mode ● xSPI1 boot mode (CS0 × 1 boot Serial Flash) ● SCI boot mode ● USB boot mode
Clock generation circuit	● The input clock can be selected from an external clock or external resonator. ● Detection of input clock oscillation stopping ● The following clocks are generated: – Cortex-A55 clock: 600 or 1200 MHz (selectable each core) – Cortex-R52 clock: 500 or 1000 MHz (selectable each unit) – A-Bus clock: 400 MHz – R-Bus clock: 250 MHz – High-speed peripheral module clock A (PCLKAH): 400 MHz – Middle-speed peripheral module clock A (PCLKAM): 200 MHz – Low-speed peripheral module clock A (PCLKAL): 100 MHz – High-speed peripheral module clock R (PCLKH): 250 MHz – Middle-speed peripheral module clock R (PCLKM): 125 MHz – Low-speed peripheral module clock R (PCLKL): 62.5 MHz – ADC clock in the 12-bit A/D converter: 62.5 MHz – External bus clock 125 MHz – Low-speed on-chip oscillator: 1 MHz
Reset	RES# pin reset, software reset, error reset, Cortex-A55 cluster software reset, Cortex-A55 core0 software reset, Cortex-A55 core1 software reset, Cortex-A55 core2 software reset, Cortex-A55 core3 software reset, Cortex-R52 CPU0 software reset, Cortex-R52 CPU1 software reset
Low-power consumption function	● Standby mode (Cortex-A55, Cortex-R52) ● Module stop function
Interrupt controller (ICU)	● Connect an interrupt to the GIC600 for Cortex-A55 ● Connect an interrupt to the GIC (Generic Interrupt Controller) for Cortex-R52 CPU0 and CPU1 ● Connect an activating trigger to the DMAC and ELC ● Peripheral function interrupts: 394 sources ● External interrupts: 16 sources (IRQ0 to IRQ15 pins) ● Software interrupts: 16 sources ● System error interrupts: 1 source ● 32 levels specifiable for the order of priority in the GIC
Bus state controller (BSC)	● The external address space is divided into four areas (CS0, CS2, CS3, and CS5) for management. ● The following features are configurable for each area independently: Bus size (8, 16, or 32 bits): Available sizes depend on the area. Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas). Idle wait cycle insertion (between same area access cycles or different area access cycles). Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. ● Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software).

Table 1.4 Direct memory access

Feature	Functional description
Direct memory access controller (DMAC)	● 3 units (16 channels each unit) ● Transfer modes: Single transfer mode and block transfer mode ● Transfer size – Unit 0: 1/2/4/8/16/32/64 bytes – Unit 1, 2: 1/2/4/8/16/32 bytes ● Activation sources: Software trigger, external DMA requests (DREQ), external interrupts, and interrupt requests from peripheral functions

Table 1.5 I/O Ports

Feature	Functional description
General-purpose I/O ports	● 729-pin FCBGA – I/O pins: 287 – Input pins: 0 – Pull-up/pull-down resistors: 287 ● 576-pin FCBGA – I/O pins: 189 – Input pins: 0 – Pull-up/pull-down resistors: 189 ● The locations of input/output functions are selectable from among multiple pins.

Table 1.6 Event link

Feature	Functional description
Event link controller (ELC)	● Up to 648 event signals can be interlinked with the operation of modules. ● In particular, the operation of timer modules can be started by input event signals. ● Event-linked operation of signals of ports 14 and port 30 is to be possible.

Table 1.7 Timers (1 of 2)

Feature	Functional description
Multi-function timer pulse unit 3 (MTU3)	● 9 channels (16 bits × 8 channels, 32 bits × 1 channel) ● Maximum of 28 pulse-input/output and 3 pulse-input possible ● Select from among 10, 11, 12, or 14 counter-input clock signals for each channel (with maximum operating frequency of 250 MHz) ● Input capture function ● 39 output compare/input capture registers ● Counter clear operation (synchronous clearing by compare match/input capture) ● Simultaneous writing to multiple timer counters (TCNT) ● Simultaneous register input/output by synchronous counter operation ● Buffered operation ● Support for cascade-connected operation ● Automatic transfer of register data ● Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM ● Complementary PWM output mode – Outputs non-overlapping waveforms for controlling 3-phase inverters – Automatic specification of dead times – PWM duty cycle: Selectable as any value from 0% to 100% – Delay can be applied to requests for A/D conversion. – Non-generation of interrupt requests at peak or trough values of counters can be selected. – Double buffer configuration ● Reset synchronous PWM mode Six phases of positive and negative PWM waveforms can be output with desired duty cycles. ● Phase-counting mode: 16-bit mode (channels 1 and 2), 32-bit mode (channels 1 and 2 in cascade connection) ● Counter functionality for dead-time compensation ● Generation of triggers for A/D converter conversion ● A/D converter start triggers can be skipped ● Digital noise filter function for signals on the input capture and external counter clock pins ● Event linking by the ELC

Table 1.7 Timers (2 of 2)

Feature	Functional description
General PWM timer (GPT)	• 32 bits × 56 channels (5 channels × 9 units + 7 channels × 1 unit + 4 channels × 1 unit) • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 500 MHz for LLPP) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of 3 counters, generation of automatic 3-phase PWM waveforms incorporating dead times • Starting, clearing, stopping, switching, up/down counters, and input capture in response to external or internal triggers • Starting, clearing, stopping, switching, up/down counters, and input capture in response to input level comparison • Internal trigger sources: software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter function for signals on the input capture and external trigger pins • Event linking by the ELC • Function of output duty 0% and 100% is selectable from troughs or crests/troughs.
Compare match timer (CMT)	• (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel
Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.
Watchdog timer (WDT)	• 14 bits × 6 channels • Select from among six counter-input clock signals for each channel
Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by input clock oscillation-stoppage detection, PLL oscillation anomaly detection, two types of DSMIF error detection, or software • Additional programming of output control target pins is enabled
Port output enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPT • Initiation by detection of oscillation stop, two types of DSMIF error detection, or by software
Real time clock (RTC)	• A 100 year calendar from 2000 to 2099 • BCD code display • Clock source is division of main oscillator. • Automatic adjustment function for leap years

Table 1.8 Communication interfaces (1 of 3)

Feature	Functional description
Ethernet MAC (GMAC)	• 1 port × 3 units • IEEE802.3 • IEEE1588-2008 • IEEE802.3-az-2010 for EEE • Support for 10/100/1000 Mbps data transfer • Full duplex and half duplex are supported • Programmable frame length to support both standard and jumbo frames up to 16 KB • 32 MAC address registers for the address filter block • Variety of flexible addresses filtering modes are supported • Advanced IEEE 1588-2002 & 2008 Ethernet frame time-stamping supported • MII/RMII/RGMII interface is supported by RMII/RGMII converter • TSN features (IEEE802.1Qbv, IEEE802.1Qbu/802.3br) • Multi queues support up to 8 RX and 8 TX queues • DMA channels: 8 RX and 8 TX channels • VLAN Filtering, L3 and L4 Filtering
Ethernet switch (ETHSW)	• 3-port PHY interfaces • IEEE802.3 • Support for 10/100/1000 Mbps data transfer • Full and half duplex (1000 Mbps supports full-duplex only) • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with eight priority levels • Multicasting and broadcasting • VLAN frame • IEEE 1588-2008 compatible • Programmable addition, removal and manipulation of ingress and egress VLAN tags, supporting single and double-tagged VLAN frames on each port • Cut-through and hub features • Device level ring (DLR) • Programmable egress rate limit per port • Ingress Configurable Broadcast/multicast storm protection per port • IEEE802.1X source address authentication supported • IEEE802.1X guest VLAN supported • PRP functionality (IEC 62439-3 edition 2.0- 2012) • Configurable Time Multiplexed (TDMA) output queue scheduler supporting real-time network infrastructures using time slots for bandwidth reservation enabling deterministic delays • Frame preemption • Cyclic queuing and forwarding • Forwarding rule for the TSN-IA profile • A MAC source address filtering • Pattern matchers 12 channels • Independent two timer module are available for timestamping and time for TDMA. • Remote monitoring through SNMP • Powerlink capable hub • Ingress filtering and frame header manipulation (active stream identification, flow metering) with Enhanced Frame Parser • 4 additional PTP timer pulse generators • MII/RMII/RGMII interface is supported by RMII/RGMII converter
EtherCAT slave controller (ESC)*1	• 1 channel (3 ports) • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented • MII interface is supported. RMII/RGMII interface is supported by RGMII converter in Ethernet Subsystem.
USB 2.0 HS host/function module	• 1 port • Compliance with the USB 2.0 specification • OTG support • Transfer rate High speed (480 Mbps), full speed (12 Mbps), low speed (1.5 Mbps, host only) • Communications buffer – Incorporates 1 KB of RAM for host mode – Incorporates 8 KB of RAM for function mode • DMAC (2 channels) incorporated

Table 1.8 Communication interfaces (2 of 3)

Feature	Functional description
Serial communication interface (SCI)	• 6 channels + 12 channels (for encoder) • 6 communication mode – Asynchronous interfaces – 8-bit clock synchronous interface – Simple I^2C (master-only) – Simple SPI – Smart card interface – Manchester mode (For channel for encoder, Simple I^2C, Simple SPI, and Smart card interface mode are not supported.) • Clock source is select from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and half-duplex communication • Data length: 7 to 9 bits (Asynchronous mode) • Bit rate modulation • Double speed mode (Asynchronous, Clock Synchronous, Simple SPI mode, Manchester mode) • RS-485 driver control function (Asynchronous mode) • Loopback function to enable self-diagnosis (Asynchronous, Clock synchronous mode)
I^2C bus interface (IIC)	• 3 channels • Communication formats: I^2C bus format or SMBus format • Master or slave mode selectable • Supports the multi-master • Maximum transfer rate: 400 kbps (Standard mode and Fast mode)
CAN-FD module (CANFD)	• 2 channels • Comply with CAN-FD ISO 11898-1 (2015) • Communication speed – Classical CAN mode: 1 Mbps – CAN FD mode: Nominal bit rate: max. 1 Mbps Data bit rate: max. 8 Mbps • Total 192 message buffers (in case frame size is 76 bytes) – Individual buffers: 64 for TX – Shared buffers: 128 for TX and RX including FIFO • Selectable ID type with 11-bit Standard and 18-bit Extended • Selectable Frame type: Data Frame and Remote Frame • Up to 256 receive rules
Serial peripheral interface (SPI)	• 4 channels • SPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (SPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) capable of handling serial transfer as a master or slave • Data formats – Switching between MSB first and LSB first – Transfer bit length selectable to 4 - 32 bits – 32 bits × 4-stage FIFO transmit and receive buffers – Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • RSPCK can be stopped automatically with the reception buffer full for master reception

Table 1.8 Communication interfaces (3 of 3)

Feature	Functional description
Expanded serial peripheral interface (xSPI)	• 2 channels • Comply with JESD251 • Multiple slave up to 2 slaves • Protocol mode: 1/4/8pin with SDR/DDR 1S-1S-1S, 4S-4D-4D, 8D-8D-8D • Support OctaFlash, OctaRAM, HyperFlash and HyperRAM • Protocol mode: 2/4pin with SDR compatible with QSPI 1S-2S-2S, 2S-2S-2S 1S-4S-4S, 4S-4S-4S • Configurable address length • Configurable initial access latency cycle • Support XiP mode • Support up to 256 MB address space • Prefetch function for burst-read with low latency • Outstanding buffer for burst-write with high throughput • Manual command configurable up to 4 commands • Output clock/input strobe port timing shift • Automatic command after released reset: up to 4 commands
SD/eMMC Host Interface (SDHI)	• SD memory/IO card interface (1-bit/4-bit SD bus) • SD, SDHC, and SDXC SD memory card access supported • Default, high-speed, UHS-I/SDR12, SDR25, SDR50, SDR104, and DDR50 transfer modes supported • Error check function: CRC7 (for command/response), CRC16 (for data) • Card detect function • Write protect supported • MMC interface (1-/4-/8-bit MMC bus) • e-MMC device access supported • Backward-compatible, high-speed (SDR/DDR), and HS200 transfer modes supported • High-priority interrupt (HPI) supported
PCI Express Gen3 (PCIE)	• PCI Express Gen1 (2.5 [GT/s]) / Gen2 (5.0 [GT/s]) / Gen3 (8.0 [GT/s]) • Root Complex / Endpoint Applications, Type 0/1 Configuration Register • Lane/Port: 1 lane × 2 ports or 2 lanes × 1 port selectable • Support Polarity inversion • Maximum data payload of 256 bytes, Maximum read request size 512 bytes • Number of outstanding 1-8 • Dynamic control of speed/width up/down configuration • Power Management (not support ASPM L1-Substate) • Error handling/logging (AER Support) • Replay FIFO with ECC • Number of Support Functions 2

Note 1. EtherCAT is a registered trademark of Beckhoff Automation GmbH, Germany.

Table 1.9 Analog

Feature	Functional description
12-bit A/D converter (ADC12)	• 12 bits × 3 units (unit 0, 1: 4 channels, unit 2: 15 channels) • 12-bit resolution • Conversion time 0.32 µs per channel • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in all units) included • Sampling variable Sampling time can be set up for each channel • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, timer (MTU3, ELC) trigger, external trigger • Event linking by the ELC
Temperature sensor unit (TSU)	• 1 channel • Relative precision: ±2°C (typ)

Table 1.10 Hardware accelerator for industrial interfaces

Feature	Functional description
ΔΣ interface (DSMIF)	• 3 channels × 10 units • Selectable 2 inputs (U/V) or 3 inputs (U/V/W) • Up to 6 ΔΣ modulators are externally connectable • Sinc filter can be selected as first, second or third order • Direct error connection to POE3 and POEG • Enhancement of current error detection • Core clock: 250 MHz/400 MHz selectable
Trigonometric function unit (TFU)	• 2 units • Calculation of sine, cosine, arctangent, hypot_k ($\sqrt{x^2+y^2}/k$) • Simultaneous calculation of sine and cosine • Simultaneous calculation of arctangent and hypot_k
Encoder interfaces	• EnDat 2.2 (16 units) • BiSS-C (16 units) • A-format (16 units) • HIPERFACE DSL (16 units) • ENCOUT (1 unit)

Table 1.11 Safety

Feature	Functional description
Memory protection unit (MPU)	• Cortex-R52 MPU Two stages MPUs (EL2 and EL1) 24 regions each MPU • Master MPU Memory protection for masters except Cortex-A55 and Cortex-R52 (DMAC, USB, Ethernet MAC, CoreSight, SHOSTIF, LCDC, SDHI, PCIE)
Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
CRC calculator (CRC)	• 2 channels • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of five generating polynomials: – $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet) – $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) – $X^{16} + X^{15} + X^2 + 1$ (CRC-16) – $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) – $X^8 + X^2 + X + 1$ (CRC-8)
Clock monitor circuit (CLMA)	• Monitors the abnormal output clock frequency from the input clock (main clock oscillator), PLL circuit, or low-speed on-chip oscillator. • Input clock oscillation stop detection: Available
Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Isolated peripherals	• Safety dedicated peripherals are available: – GPT: 4 ch – SCI: 1 ch – IIC: 1 ch – SPI: 1 ch – CRC: 1 unit – RTC: 1 unit – GPIO: Sharable with normal GPIO – On-chip system SRAM with ECC • They are mapped independently from normal peripherals so that access protection can be done by EL2 MPU.

Table 1.12 Security

Feature	Functional description
Security*1	• Secure boot • JTAG authentication • SCI/USB boot authentication • Cryptographic accelerators – Symmetric Cipher: AES 128/192/256 bits with CBC/ECB/CTR/GCM/XTS – Asymmetric Cipher: ECC 256 bits, RSA 1024/2048/3072 bits, RSAES-OAEP – Hash: SHA-1, SHA-2 – Message authentication: HMAC, CMAC, GMAC – Signature algorithms: ECDSA with NIST P-256, RSASSA-PSS, RSASSA-PKCS1 • TRNG • Cortex-A55 Crypto Extension • Arm® TrustZone® technology

Note 1. For details, contact our sales representative.

Table 1.13 Debug

Feature	Functional description
Debugging interface	• CoreSight architecture designed by Arm • Debugging function by the JTAG/SWD interface, and trace function by ETF and system bus by ETR

Table 1.14 External host interface

Feature	Functional description
Serial host interface (SHOSTIF)	• Serial communication is possible in slave mode. • Supported interface – Motorola Serial Peripheral Interface (4-wire SPI) – Enhanced SPI Modes with Dual, Quad, or Octal SPI • Serial clock polarity switching • Serial clock phase switching • Single Data Transfer • Data size is up to 32 bits × 64 burst
Mailbox and semaphore (MBXSEM)	• Eight semaphores for external host CPU and Cortex-A55/Cortex-R52 • Four 32-bit mailboxes for both external host CPU to Cortex-A55/Cortex-R52 and Cortex-A55/Cortex-R52 to external host CPU • Interrupts can be generated and cleared from both external host CPU and Cortex-A55/Cortex-R52 • Semaphores and Mailboxes with exclusive access among Cortex-A55, Cortex-R52 CPU0 and CPU1.

Table 1.15 Display interface

Feature	Functional description
LCD Controller (LCDC)	• 2 planes blending (can blend 2 different size images) • Support Image Processing: – Dither processing (RGB666) – Clipping – RGB Gamma Correction LUT • Support Input Data Format: – RGB565 / RGB666 / RGB888 – ARGB1555 / ARGB4444 / ARGB8888 – YcbCr444 8-bit / YcbCr422 8-bit / YcbCr420 8-bit • Support WXGA (1280 × 800), 60 fps • Support Output Data Format: – RGB666 / RGB888 • CLK / HD / VD timing signal supported

Table 1.16 Others

Feature	Functional description
Power supply voltage	0.8 V: Core (Digital and Analog (PLL, TSU, OTP, USB, PCIE, ADC)) 1.1 V: DDR 1.8 V: PLL, OSC, USB, ADC, TSU, OTP, PCIE, DDR, RGMII 3.3 V: GPIO (in 3.3 V fixed domain), USB, OSC, RMII/MII, other peripherals 1.8 V/3.3 V selectable: xSPI, SDHI, GPIO (in 1.8 V/3.3 V selectable domains)
Operating temperature	Tj = −40 to +125°C
Packages	RZ/T2H: 729 pin FCBGA 23 × 23 mm, 0.8-mm pitch RZ/N2H: 576 pin FCBGA 21 × 21 mm, 0.8-mm pitch

1.2 Function Comparison

Table 1.17 Function comparison (1 of 2)

Module/Function		RZ/T2H (729-pin FCBGA)	RZ/N2H (576-pin FCBGA)
CPU	ARM Cortex-A55	Quad/Dual/Single	
	ARM Cortex-R52	Two	
Memory	System SRAM	2.0 MB	
External bus	External bus width	32 bits	
Interrupt	External interrupt	SEI, IRQ0 to IRQ15	
DMA	DMA controller (DMAC)	3 units (16 channels each unit)	
Timer	Multi-function timer pulse unit 3 (MTU3)	1 unit (9 channels)	
	General PWM timer (GPT)	11 units (56 channels)	11 units (56 channels)*1
	Compare match timer (CMT)	3 units (6 channels)	
	Compare match timer W (CMTW)	2 channels	
	Watchdog timer	6 channels	
	Port output enable 3 (POE3)	1 unit	
	Port output enable for GPT (POEG)	3 unit	
	Real time clock (RTC)	1 unit	
Communication function	Ethernet MAC (GMAC)	3 units	3 units*1
	Ethernet switch (ETHSW)	1 unit (3 external ports)	1 unit (3 external ports)*1
	EtherCAT slave controller (ESC)	1 unit (3 external ports)	
	USB 2.0 HS host/function module (USB)	1 unit (1 port)	
	Serial communication interface (SCI, SCIE)	6 channels + 12 channels	
	I2C bus interface (IIC)	3 channels	
	CANFD module (CANFD)	2 channels	
	Serial peripheral interface (SPI)	4 channels	4 channels*1
	Expanded serial peripheral interface (xSPI)	2 channels	2 channels*1
	PCI Express Gen3 (PCIE)	1 unit (1 lane × 2 ports or 2 lanes × 1 port)	
	SD/eMMC Host Interface (SDHI)	2 channels	
12-bit A/D converter (ADC12)		3 units (4 channels for unit 0 and unit 1, 6 channels for unit 2)	3 units (4 channels for unit 0 and unit 1, 15 channels for unit 2)
Temperature sensor unit (TSU)		1 unit	
ΔΣ interface (DSMIF)		10 units (30 channels)	8 units (23 channels)*2
Trigonometric function unit (TFU)		2 units	
Encoder I/F	EnDat 2.2 (ENDAT)	16 units	14 units*3
	BiSS-C (BISS)	16 units	14 units*3
	A-format (AFMT)	16 units	14 units*3
	Hiperface DSL (HDSL)	16 units	14 units*1 *3
	ENCOUT	1 unit	1 unit
CRC calculator (CRC)		2 channels	
Clock monitor circuit (CLMA)		7 units	
Data operation circuit (DOC)		1 unit	
Security*4		Optional	

Table 1.17 Function comparison (2 of 2)

Module/Function	RZ/T2H (729-pin FCBGA)	RZ/N2H (576-pin FCBGA)
One-time programmable memory (OTP)	Available	
Serial host interface	1 unit	
Mailbox and semaphore (MBXSEM)	Available	
Event link controller (ELC)	Available	
LPDDR4 SDRAM Subsystem (DDRSS)	32 bits	
LCD Controller (LCDC)	1 unit	

Note 1. A part of external signals are not available.
Note 2. Unit 6, 9 and ch 2 of unit 8 are not available due to lack of mandatory external signals.
Note 3. Unit 8 and 15 are not available due to lack of mandatory external signals.
Note 4. For details, contact our sales representative.

1.3 Product Lineup

Table 1.18 shows a product lineup.

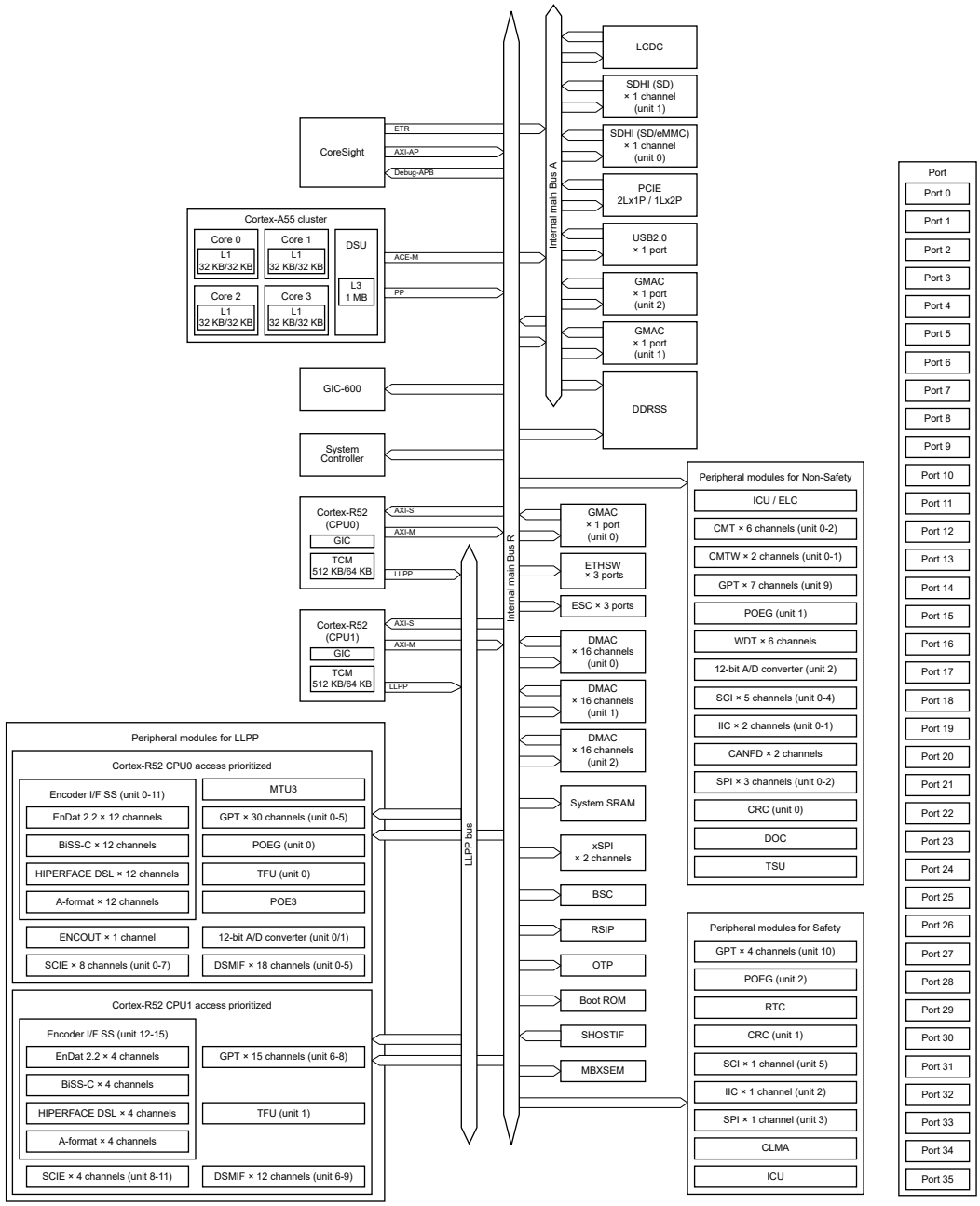
Table 1.18 Product lineup

Product	Part Number	Package	Cortex-A55	Cortex-R52	Security*1
RZ/T2H	R9A09G077M48GBG	729-pin FCBGA	Quad cores	Two CPUs	Available
	R9A09G077M28GBG	729-pin FCBGA	Dual cores	Two CPUs	Available
	R9A09G077M08GBG	729-pin FCBGA	Single core	Two CPUs	Available
	R9A09G077M44GBG	729-pin FCBGA	Quad cores	Two CPUs	Not available
	R9A09G077M24GBG	729-pin FCBGA	Dual cores	Two CPUs	Not available
	R9A09G077M04GBG	729-pin FCBGA	Single core	Two CPUs	Not available
RZ/N2H	R9A09G087M48GBG	576-pin FCBGA	Quad cores	Two CPUs	Available
	R9A09G087M28GBG	576-pin FCBGA	Dual cores	Two CPUs	Available
	R9A09G087M08GBG	576-pin FCBGA	Single core	Two CPUs	Available
	R9A09G087M44GBG	576-pin FCBGA	Quad cores	Two CPUs	Not available
	R9A09G087M24GBG	576-pin FCBGA	Dual cores	Two CPUs	Not available
	R9A09G087M04GBG	576-pin FCBGA	Single core	Two CPUs	Not available

Note 1. Except for TrustZone. TrustZone is available for all part number.

1.4 Block Diagram

Figure 1.1 shows a block diagram.



GMAC	: Ethernet MAC	GPT	: General PWM timer
ETHSW	: Ethernet switch	CMT	: Compare match timer
ESC	: EtherCAT slave controller	CMTW	: Compare match timer W
DMAC	: DMA controller	POE3	: Port output enable 3
BSC	: Bus state controller	POEG	: Port output enable for GPT
xSPI	: Expanded serial peripheral interface	RTC	: Real time clock
WDT	: Watchdog timer	IIC	: I^2C bus interface
SCI	: Serial communication interface	CANFD	: CANFD module
SCIE	: Serial communication interface for encoder	DSMIF	: ΔΣ interface
		TFU	: Arithmetic unit for trigonometric functions
SPI	: Serial peripheral interface	CRC	: CRC (cyclic redundancy check) calculator
USB	: USB 2.0 HS host/function module	CLMA	: Clock monitor circuit
GIC	: Generic interrupt controller	DOC	: Data operation circuit
ELC	: Event link controller	TSU	: Temperature sensor unit
MTU3	: Multi-function timer pulse unit 3	RSIP	: Renesas Security IP
SHOSTIF	: Serial host interface	OTP	: One-time programmable memory
MBXSEM	: Mailbox and Semaphore	LCDC	: LCD Controller
SDHI	: SD/eMMC host interface	DDRSS	: LPDDR4 SDRAM memory interface
PCIE	: PCI Express Gen 3		

Figure 1.1 Block diagram

1.5 Pin Functions

Table 1.19 lists the pin functions.

Table 1.19 Pin functions (1 of 10)

Classification	Pin name	I/O	Description
Power supply	VDD33	Input	3.3 V power supply pin for I/O
	VDD1833_0 to VDD1833_7	Input	Power supply pins for each I/O domains. (1.8 V or 3.3 V) VDD1833_0: ETH0 domain VDD1833_1: ETH1 domain VDD1833_2: ETH2 domain VDD1833_3: ETH3 domain VDD1833_4: xSPI0 domain VDD1833_5: xSPI1 domain VDD1833_6: SDHI0 domain VDD1833_7: SDHI1 domain
	VDDP_18_33, VDDP_18_0 to VDDP18_7	Input	1.8 V power supply pins for I/O
	VDD08	Input	0.8 V power supply pin.
	VDD18_PLL0 to VDD18_PLL4	Input	1.8 V power supply pins for PLL
	VDD08_PLL0 to VDD08_PLL4	Input	0.8 V power supply pins for PLL
	VDD33_X	Input	3.3 V power supply pin for Oscillator
	VDDP_18_X	Input	1.8 V power supply pin for Oscillator
	AVDD18A_TSU	Input	1.8 V power supply pin for Thermal sensor
	DVDD08A_TSU	Input	0.8 V power supply pin for Thermal sensor
	OTPVDD18	Input	1.8 V power supply pin for OTP
	OTPVDD08	Input	0.8 V power supply pin for OTP
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VSS_PLL0 to VSS_PLL4	Input	Ground pin for PLL. Connect to the system power supply (0 V).
Clock	XTAL	Output	Connected to a crystal resonator. When external clock signal is used, EXTAL pin should be driven low. XTAL pin should never be driven or loaded by anything other than crystal oscillator. The voltage level of EXTAL must not exceed VDD18 (1.8 V).
	EXTAL	Input	
	EXTCLKIN	Input	Inputs the external clock. When a crystal resonator is connected, it should be driven low.
	XTALSEL	Input	Main clock source select pin (low: EXTCLKIN, high: XTAL/EXTAL)
	CKIO	Output	Outputs the external bus clock for external devices.
	ETH0_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 0
	ETH1_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 1
	ETH2_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 2
	ETH3_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 3
	RMII0_REFCLK	Output	Outputs 50 MHz clock for RMII0
	RMII1_REFCLK	Output	Outputs 50 MHz clock for RMII1
	RMII2_REFCLK	Output	Outputs 50 MHz clock for RMII2
	RMII3_REFCLK	Output	Outputs 50 MHz clock for RMII3

Table 1.19 Pin functions (2 of 10)

Classification	Pin name	I/O	Description
Operating mode control	MDX	Input	This signal should be driven low.
	MD0 to MD2	Input	Input the operating mode select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDV	Input	Input the operating voltage select signal for boot peripheral. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
	MDW0, MDW1	Input	Input the ATCM wait cycle select signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
	MDD	Input	Input the enabling JTAG authentication by hash signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES#	Input	Inputs the reset signal. This MPU enters the reset state when this signal goes low.
	BSCANP	Input	Inputs the boundary scan enable signal. Boundary scan is enabled when this pin goes high. When boundary scan is not used, this pin should be driven low.
	RSTOUT#	Output	Outputs the reset signal externally
Debugging interface	TRST#	Input	Test reset pin for the on-chip emulator
	TMS	I/O	Test mode select pin for the on-chip emulator Functions as the SWDIO pin in serial wire debug (SWD) mode
	TDI	Input	Test data input pin for the on-chip emulator
	TDO	Output	Test data output pin for the on-chip emulator
	TCK	Input	Test clock pin for the on-chip emulator Functions as the SWCLK pin in serial wire debug (SWD) mode
Bus state controller (BSC)	A25 to A0	Output	Output the address
	D31 to D0	I/O	Input and output the data
	CS0#, CS2#, CS3#, CS5#	Output	Output the chip select signal for the external memory or device.
	RD#	Output	Outputs the strobe signal which indicates a read is in progress.
	RD/WR#	Output	Outputs the strobe signal which indicates a read or write access
	BS#	Output	Outputs the status signal which indicates the start of the bus cycle
	AH#	Output	Outputs the address hold signal for the device that uses the multiplexed I/O interface
	WAIT#	Input	Inputs the external wait control signal which inserts a wait cycle into the bus cycle
	WE0#	Output	Outputs the write strobe signal to D7 to D0
	WE1#	Output	Outputs the write strobe signal to D15 to D8
	WE2#	Output	Outputs the write strobe signal to D23 to D16
	WE3#	Output	Outputs the write strobe signal to D31 to D24

Table 1.19 Pin functions (3 of 10)

Classification	Pin name	I/O	Description
Direct memory access controller (DMAC)	DREQ	Input	Inputs the DMA transfer request signal from the external device
	DACK	Output	Outputs the acknowledge signal which indicates acceptance of the DMA transfer request from the external device
	TEND	Output	Outputs the DMA transfer end signal
Interrupt	SEI	Input	Input the system error interrupt signal
	IRQ0 to IRQ15	Input	Input the external interrupt request signal
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	TGRA0 to TGRD0 input capture input, output compare output, and PWM output pins
	MTIOC1A, MTIOC1B	I/O	TGRA1 and TGRB1 input capture input, output compare output, and PWM output pins
	MTIOC2A, MTIOC2B	I/O	TGRA2 and TGRB2 input capture input, output compare output, and PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	TGRA3 to TGRD3 input capture input, output compare output, and PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	TGRA4 to TGRD4 input capture input, output compare output, and PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	TGRU5, TGRV5, and TGRW5 input capture input and dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	External clock input pins for MTU3
Port output enable 3 (POE3)	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input the request signal to place the MTU3 in the high-impedance state

Table 1.19 Pin functions (4 of 10)

Classification	Pin name	I/O	Description
General PWM timer (GPT)/ Port output enable for GPT (POEG)	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input and output-disable request input pins
	GTETRGSA, GTETRGSB	Input	External trigger input and output-disable request input pins (SAFETY)
	GTIOC00_0A to GTIOC00_4A, GTIOC00_0B to GTIOC00_4B, GTIOC01_0A to GTIOC01_4A, GTIOC01_0B to GTIOC01_4B, GTIOC02_0A to GTIOC02_4A, GTIOC02_0B to GTIOC02_4B, GTIOC03_0A to GTIOC03_4A, GTIOC03_0B to GTIOC03_4B, GTIOC04_0A to GTIOC04_4A, GTIOC04_0B to GTIOC04_4B, GTIOC05_0A to GTIOC05_4A, GTIOC05_0B to GTIOC05_4B, GTIOC06_0A to GTIOC06_4A, GTIOC06_0B to GTIOC06_4B, GTIOC07_0A to GTIOC07_4A, GTIOC07_0B to GTIOC07_4B, GTIOC08_0A to GTIOC08_4A, GTIOC08_0B to GTIOC08_4B, GTIOC09_0A to GTIOC09_6A, GTIOC09_0B to GTIOC09_6B, GTIOC10_0A to GTIOC10_3A, GTIOC10_0B to GTIOC10_3B	I/O	Input capture input/output compare output/PWM output pins
	GTADSM00_0 to GTADSM00_1, GTADSM01_0 to GTADSM01_1, GTADSM02_0 to GTADSM02_1, GTADSM03_0 to GTADSM03_1, GTADSM04_0 to GTADSM04_1, GTADSM05_0 to GTADSM05_1, GTADSM06_0 to GTADSM06_1, GTADSM07_0 to GTADSM07_1, GTADSM08_0 to GTADSM08_1, GTADSM09_0 to GTADSM09_1	Output	Output pins for monitoring A/D conversion start requests
Compare match timer W (CMTW)	CMTW0_TIC0, CMTW0_TIC1, CMTW1_TIC0, CMTW1_TIC1	Input	CMTW input capture input pins
	CMTW0_TOC0, CMTW0_TOC1, CMTW1_TOC0, CMTW1_TOC1	Output	CMTW output compare output pins
Real time clock (RTC)	RTCAT1HZ	Output	RTC 1 Hz output pin

Table 1.19 Pin functions (5 of 10)

Classification	Pin name	I/O	Description
Serial communication interface (SCI)	SCK0 to SCK5	I/O	Clock I/O pins (clock synchronous mode/simple SPI mode/smart card mode)
	RXD0 to RXD5	Input	Input the receive data (asynchronous mode/clock synchronous mode/smart card mode)
	TXD0 to TXD5	Output	Output the transmit data (asynchronous mode/clock synchronous mode/smart card mode)
	CTS0# to CTS5#	Input	Input the start of transmission (asynchronous mode/ clock synchronous mode) active-low
	RTS0# to RTS5#	Output	Output the reception (asynchronous mode/clock synchronous mode) active-low
	SCL0 to SCL5	I/O	Input/output the I2C clocks (simple I2C mode)
	SDA0 to SDA5	I/O	Input/output the I2C data (simple I2C mode)
	MISO0 to MISO5	I/O	Input/output the data for slave transmission (simple SPI mode)
	MOSI0 to MOSI5	I/O	Input/output the data for master transmission (simple SPI mode)
	SS0# to SS5#	Input	Chip-select input pins (simple SPI mode) active-low
	DE0 to DE5	Output	Driver enable output pins (asynchronous mode)
Serial communication interface for Encoder (SCIE)	SCKE00 to SCKE11	Output	Clock I/O pins (clock synchronous mode)
	RXDE00 to RXDE11	Input	Input the receive data (asynchronous mode/clock synchronous mode)
	TXDE00 to TXDE11	Output	Output the transmit data (asynchronous mode/clock synchronous mode)
	DEE00 to DEE11	Output	Driver enable output pins (asynchronous mode)
I^2C bus interface (IIC)	IIC_SCL0 to IIC_SCL2	I/O	Clock I/O pins
	IIC_SDA0 to IIC_SDA2	I/O	Data I/O pins

Table 1.19 Pin functions (6 of 10)

Classification	Pin name	I/O	Description
Ethernet	ETH0_TXCLK to ETH3_TXCLK	I/O	TX clock input pins (MII mode) TX clock output pins (RGMII mode)
	ETH0_TXD0 to ETH3_TXD0	Output	TX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_TXD1 to ETH3_TXD1	Output	TX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_TXD2 to ETH3_TXD2	Output	TX data 2 pins (RGMII and MII modes)
	ETH0_TXD3 to ETH3_TXD3	Output	TX data 3 pins (RGMII and MII modes)
	ETH0_TXEN to ETH3_TXEN	Output	TX data enable pins (RMII and MII modes) TX data enable/TX data error (TX_CTL) pins (RGMII mode)
	ETH0_TXER to ETH3_TXER	Output	TX data error pins (MII mode)
	ETH0_RXCLK to ETH3_RXCLK	Input	RX clock pins (RGMII, RMII, and MII modes)
	ETH0_RXD0 to ETH3_RXD0	Input	RX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_RXD1 to ETH3_RXD1	Input	RX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_RXD2 to ETH3_RXD2	Input	RX data 2 pins (RGMII and MII modes)
	ETH0_RXD3 to ETH3_RXD3	Input	RX data 3 pins (RGMII and MII modes)
	ETH0_RXDV to ETH3_RXDV	Input	RX data valid pins (MII mode) Carrier sense/RX data valid (CRS_DV) pins (RMII mode) RX data valid/RX error (RX_CTL) pins (RGMII mode)
	ETH0_RXER to ETH3_RXER	Input	RX data error pins (RMII and MII modes)
	ETH0_CRS to ETH3_CRS	Input	Carrier sense pins (MII mode)
	ETH0_COL to ETH3_COL	Input	Collision detection pins (MII mode)
Ethernet MAC (GMAC)	GMAC0_PTPTRG0 to GMAC2_PTPTRG0	Input	PTP timer trigger external input 0
	GMAC0_PTPTRG1 to GMAC2_PTPTRG1	Input	PTP timer trigger external input 1
	GMAC0_MDC to GMAC2_MDC	Output	Management data clock output pin
	GMAC0_MDIO to GMAC2_MDIO	I/O	Management data I/O pin
Ethernet switch (ETHSW)	ETHSW_LPI0	Output	Port 0 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_LPI1	Output	Port 1 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_LPI2	Output	Port 2 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_PTPOUT0 to ETHSW_PTPOUT3	Output	Ethernet switch timer pulse output pins
	ETHSW_TDMAOUT0 to ETHSW_TDMAOUT3	Output	Ethernet switch TDMA timer output pins
	ETHSW_PHYLINK0 to ETHSW_PHYLINK2	Input	Ethernet switch PHY link status input pins
	ETHSW_MDC	Output	Management data clock output pin
	ETHSW_MDIO	I/O	Management data I/O pin

Table 1.19 Pin functions (7 of 10)

Classification	Pin name	I/O	Description
EtherCAT slave controller (ESC)	ESC_LEDRUN	Output	Outputs the EtherCAT RUN LED signal
	ESC_IRQ	Output	Outputs the EtherCAT IRQ signal
	ESC_LEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal
	ESC_LEDERR	Output	Outputs the EtherCAT error LED signal
	ESC_LINKACT0 to ESC_LINKACT2	Output	Output the EtherCAT link/activity LED signal
	ESC_SYNC0, ESC_SYNC1	Output	Output the EtherCAT SYNC signal
	ESC_LATCH0, ESC_LATCH1	Input	Input the EtherCAT LATCH signal
	ESC_RESETOUT#	Output	Output the EtherCAT reset signal
	ESC_I2CCLK	Output	Outputs the EtherCAT EEPROM I2C clock signal
	ESC_I2CDATA	I/O	Inputs and outputs the EtherCAT EEPROM I2C data signal
	ESC_PHYLINK0 to ESC_PHYLINK2	Input	Inputs the EtherCAT PHY link status signal.
	ESC_MDC	Output	Management data clock output pin
	ESC_MDIO	I/O	Management data I/O pin
USB 2.0 host/function module	USB_USVDD33	Input	3.3 V power supply input pin for USB
	USB_USVDD18	Input	1.8 V power supply input pin for USB
	USB_USDVDD	Input	0.8 V power supply
	USB_TXRTUNE	Input	USB2 transmitter tune pin. Connect this pin to GND via 200 Ω (±1%).
	USB_QDP	I/O	USB bus D+ data I/O pin
	USB_QDM	I/O	USB bus D- data I/O pin
	USB_VBUSEN	Output	Outputs the VBUS power enable signal for USB
	USB_OVRCUR	Input	Inputs the overcurrent signal for USB
	USB_VUBUSIN	Input	USB cable connection/disconnection detection input pin
	USB_EXICEN	Output	OTG power supply IC control pin
	USB_OTG_ID	Input	OTG ID pin
CANFD module (CANFD)	CANRX0, CANRX1	Input	Receive data input pins
	CANTX0, CANTX1	Output	Transmit data output pins
	CANRXDP0, CANRXDP1	Output	Receive data phase output pins
	CANTXDP0, CANTXDP1	Output	Transmit data phase output pins
Serial peripheral interface (SPI)	SPI_RSPCK0 to SPI_RSPCK3	I/O	Clock I/O pins
	SPI_MOSI0 to SPI_MOSI3	I/O	Master transmit data I/O pins
	SPI_MISO0 to SPI_MISO3	I/O	Slave transmit data I/O pins
	SPI_SSL00 to SPI_SSL30	I/O	Slave select signal I/O pins
	SPI_SSL01 to SPI_SSL31, SPI_SSL02 to SPI_SSL32, SPI_SSL03 to SPI_SSL33	Output	Slave select signal output pins

Table 1.19 Pin functions (8 of 10)

Classification	Pin name	I/O	Description
Expanded serial peripheral interface (xSPI)	XSPI0_CKP, XSPI1_CKP, XSPI0_CKN	Output	Clock output pins
	XSPI0_CS0#, XSPI0_CS1#, XSPI1_CS0#, XSPI1_CS1#	Output	Chip select output pins
	XSPI0_DS, XSPI1_DS	I/O	Read data strobe/write data mask input/output pin
	XSPI0_IO0 to XSPI0_IO7, XSPI1_IO0 to XSPI1_IO7	I/O	Data0 to Data7 input/output pins
	XSPI0_RESET0#, XSPI0_RESET1#	Output	Master reset status output pins
	XSPI0_RSTO0#, XSPI0_RSTO1#	Input	Slave reset status input pins
	XSPI0_INT0#, XSPI0_INT1#	Input	Interrupt input pins
	XSPI0_ECS0#, XSPI0_ECS1#	Input	Error correction status input pins
	XSPI0_WP0#, XSPI0_WP1#	Output	Write protect output pins
ΔΣ interface (DSMIF)	MCLK00 to MCLK90, MCLK01 to MCLK91, MCLK02 to MCLK92	I/O	Clock I/O pins
	MDAT00 to MDAT90, MDAT01 to MDAT91, MDAT02 to MDAT92	Input	Data input pins
12-bit A/D converter (ADC12)	AVDD_ADC0 to AVDD_ADC2	Input	0.8 V power supply pins for ADC
	AVDDIO_ADC0 to AVDDIO_ADC2	Input	1.8 V power supply pins for ADC
	AVSS_ADC0 to AVSS_ADC2	Input	Ground pins for ADC
	AVSSIO_ADC0 to AVSSIO_ADC2	Input	Ground pins for ADC
	AVDDREF_ADC0 to AVDDREF_ADC2	Input	Voltage Reference Analog Supply
	AN000 to AN003, AN100 to AN103, AN200 to AN214	input	Analog input pins for the A/D converter
	ADTRG0# to ADTRG2#	input	External trigger input pins for the start of A/D conversion
Serial host interface (SHOSTIF)	HSPI_CK	Input	Clock input pin
	HSPI_CS#	Input	Chip select input pin
	HSPI_IO0 to HSPI_IO7	I/O	Data0 to Data7 input/output pins
	HSPI_INT#	Output	Interrupt output pin
Mailbox and Semaphore (MBXSEM)	MBX_HINT#	Output	Mailbox (Cortex-A55/Cortex-R52 to Host CPU) interrupt output pin
Encoder I/F common	ENCIFCK00 to ENCIFCK15	Output	Encoder I/F clock output pins
	ENCIFOE00 to ENCIFOE15	Output	Encoder I/F data output enable pins
	ENCIFDO00 to ENCIFDO15	Output	Encoder I/F data output pins
	ENCIFDI00 to ENCIFDI15	Input	Encoder I/F data input pins
EnDat 2.2 (ENDAT)	DUEI00 to DUEI15	Output	EnDat 2.2 Data transfer
	TST_OUT00 to TSTOUT15	Output	EnDat 2.2 Data input after internal synchronization
	SI00# to SI15#	Output	EnDat 2.2 Start pulse

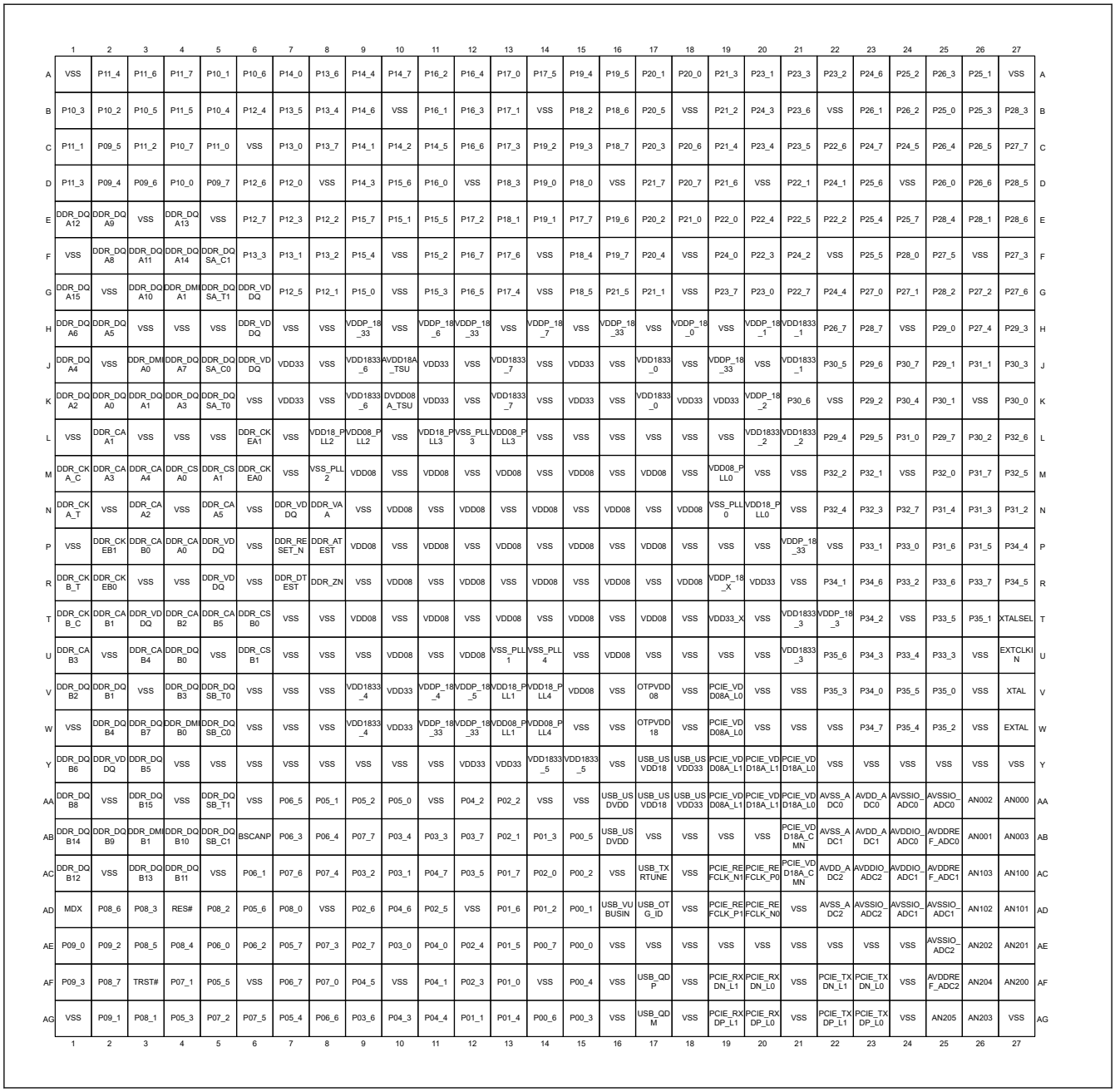
Table 1.19 Pin functions (9 of 10)

Classification	Pin name	I/O	Description
Hiperface DSL (HDSL)	HDSL00_LINK to HDSL15_LINK	Output	HDSL LINK
	HDSL00_SMPL to HDSL15_SMPL	Output	HDSL Test signal line sampler
	HDSL00_CLK1 to HDSL15_CLK1	Input	HDSL SPI clock safe 1
	HDSL00_SEL1 to HDSL15_SEL1	Input	HDSL SPI selection safe 1
	HDSL00_MISO1 to HDSL15_MISO1	Output	HDSL SPI data output safe 1
	HDSL00_MOSI1 to HDSL15_MOSI1	Input	HDSL SPI data input safe 1
	HDSL00_CLK2 to HDSL15_CLK2	Input	HDSL SPI clock safe 2
	HDSL00_SEL2 to HDSL15_SEL2	Input	HDSL SPI selection safe 2
	HDSL00_MISO2 to HDSL15_MISO2	Output	HDSL SPI data output safe 2
	HDSL00_MOSI2 to HDSL15_MOSI2	Input	HDSL SPI data input safe 2
ENCOUT	POUTA	Output	ENCOUT A-phase output pin
	POUTB	Output	ENCOUT B-phase output pin
	POUTZ	Output	ENCOUT Z-phase output pin
LCD Controller (LCDC)	DISP_CLK	Output	Display Parallel Interface pixel clock
	DISP_HSYNC	Output	Display Parallel Interface Horizontal sync pulse
	DISP_VSYNC	Output	Display Parallel Interface Vertical sync pulse
	DISP_DE	Output	Display Parallel Interface data enable
	DISP_DATAR0 to DISP_DATAR7	Output	Display Parallel Interface pixel data output Red
	DISP_DATAG0 to DISP_DATAG7	Output	Display Parallel Interface pixel data output Green
	DISP_DATAB0 to DISP_DATAB7	Output	Display Parallel Interface pixel data output Blue
SD/eMMC Host Interface (SDHI)	SD0_CLK, SD1_CLK	Output	SD/MMC clock output
	SD0_CMD, SD1_CMD	I/O	SD/MMC command output, response input
	SD0_DATA0 to SD0_DATA7, SD1_DATA0 to SD1_DATA3	I/O	SD/MMC Data
	SD0_CD, SD1_CD	Input	SD card detection
	SD0_WP, SD1_WP	Input	SD write protection
	SD0_RST#	Output	MMC reset
	SD0_PWEN, SD1_PWEN	Output	SD power enable
	SD0_IOVS, SD1_IOVS	Output	SD voltage select
PCI Express Gen3 (PCIE)	PCIE_VDD18A_CMN, PCIE_VDD18A_L0, PCIE_VDD18A_L1	Input	1.8 V power supply pins for PCIE
	PCIE_VDD08A_L0, PCIE_VDD08A_L1	Input	0.8 V power supply pins for PCIE
	PCIE_REFCLK_P0, PCIE_REFCLK_N0, PCIE_REFCLK_P1, PCIE_REFCLK_N1	Input	Reference clock input
	PCIE_RXDP_L0, PCIE_RXDN_L0, PCIE_RXDP_L1, PCIE_RXDN_L1	Input	Serial data input
	PCIE_TXDP_L0, PCIE_TXDN_L0, PCIE_TXDP_L1, PCIE_TXDN_L1	Output	Serial data output
	PCIE_RSTOUT0B, PCIE_RSTOUT1B	Output	PCIE Reset output for Root Complex

Table 1.19 Pin functions (10 of 10)

Classification	Pin name	I/O	Description
LPDDR4 SDRAM Subsystem (DDRSS)	DDR_VAA	Input	1.8 V power supply pin for DDRPHY
	DDR_VDDQ	Input	1.1 V power supply pin for DDRPHY
	DDR_ZN	Output	DDRSS calibration external reference resistor
	DDR_DTEST	I/O	DDRSS Digital test point for debug
	DDR_ATEST	I/O	DDRSS Analog test point for debug
	DDR_RESET_N	Output	DDRSS DRAM reset
	DDR_CKA_T, DDR_CKA_C, DDR_CKB_T, DDR_CKB_C	I/O	DDRSS DRAM Ch A/B Clock
	DDR_CKEA[1:0], DDR_CKEB[1:0]	I/O	DDRSS DRAM Ch A/B Clock Enable
	DDR_CSA[1:0], DDR_CSB[1:0]	I/O	DDRSS DRAM Ch A/B Chip Select
	DDR_CAA[5:0], DDR_CAB[5:0]	I/O	DDRSS DRAM Ch A/B Command/Address
	DDR_DQA[15:0], DDR_DQB[15:0]	I/O	DDRSS DRAM Ch A/B Data
	DDR_DMIA[1:0], DDR_DMIB[1:0]	I/O	DDRSS DRAM Ch A/B Data Mask Inversion
	DDR_DQSA_T[1:0], DDR_DQSB_T[1:0]	I/O	DDRSS DRAM Ch A/B Data Strobe (positive)
	DDR_DQSA_C[1:0], DDR_DQSB_C[1:0]	I/O	DDRSS DRAM Ch A/B Data Strobe (negative)
I/O ports	P00_0 to P35_6	I/O	General-purpose input/output pins

1.6 RZ/T2H FCBGA 729 Pin Assignments



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	VSS	P11_4	P11_6	P11_7	P10_1	P10_6	P14_0	P13_6	P14_4	P14_7	P16_2	P16_4	P17_0	P17_5	P19_4	P19_5	P20_1	P20_0	P21_3	P23_1	P23_3	P23_2	P24_6	P25_2	P26_3	P25_1	VSS	A
B	P10_3	P10_2	P10_5	P11_5	P10_4	P12_4	P13_5	P13_4	P14_6	VSS	P16_1	P16_3	P17_1	VSS	P18_2	P18_6	P20_5	VSS	P21_2	P24_3	P23_6	VSS	P26_1	P26_2	P25_0	P25_3	P28_3	B
C	P11_1	P09_5	P11_2	P10_7	P11_0	VSS	P13_0	P13_7	P14_1	P14_2	P14_5	P16_6	P17_3	P19_2	P19_3	P18_7	P20_3	P20_6	P21_4	P23_4	P23_5	P22_6	P24_7	P24_5	P26_4	P26_5	P27_7	C
D	P11_3	P09_4	P09_6	P10_0	P09_7	P12_6	P12_0	VSS	P14_3	P15_6	P16_0	VSS	P18_3	P19_0	P18_0	VSS	P21_7	P20_7	P21_6	VSS	P22_1	P24_1	P25_6	VSS	P26_0	P26_6	P28_5	D
E	DDR_DQA12	DDR_DQA9	VSS	DDR_DQA13	VSS	P12_7	P12_3	P12_2	P15_7	P15_1	P15_5	P17_2	P18_1	P19_1	P17_7	P19_6	P20_2	P21_0	P22_0	P22_4	P22_5	P22_2	P25_4	P25_7	P28_4	P28_1	P28_6	E
F	VSS	DDR_DQA8	DDR_DQA11	DDR_DQA14	DDR_DQSA_C1	P13_3	P13_1	P13_2	P15_4	VSS	P15_2	P16_7	P17_6	VSS	P18_4	P19_7	P20_4	VSS	P24_0	P22_3	P24_2	VSS	P25_5	P28_0	P27_5	VSS	P27_3	F
G	DDR_DQA15	VSS	DDR_DQA10	DDR_DMA1	DDR_DQSA_T1	DDR_VDDQ	P12_5	P12_1	P15_0	VSS	P15_3	P16_5	P17_4	VSS	P18_5	P21_5	P21_1	VSS	P23_7	P23_0	P22_7	P24_4	P27_0	P27_1	P28_2	P27_2	P27_6	G
H	DDR_DQA6	DDR_DQA5	VSS	VSS	VSS	DDR_VDDQ	VSS	VSS	VDDP_18_33	VSS	VDDP_18_6	VDDP_18_33	VSS	VDDP_18_7	VSS	VDDP_18_33	VSS	VDDP_18_0	VSS	VDDP_18_1	VDD1833_1	P26_7	P28_7	VSS	P29_0	P27_4	P29_3	H
J	DDR_DQA4	VSS	DDR_DMA0	DDR_DQA7	DDR_DQSA_C0	DDR_VDDQ	VDD33	VSS	VDD1833_6	AVDD18A_TSU	VDD33	VSS	VDD1833_7	VSS	VDD33	VSS	VDD1833_0	VSS	VDDP_18_33	VSS	VDD1833_1	P30_5	P29_6	P30_7	P29_1	P31_1	P30_3	J
K	DDR_DQA2	DDR_DQA0	DDR_DQA1	DDR_DQA3	DDR_DQSA_T0	VSS	VDD33	VSS	VDD1833_6	DVDD08A_TSU	VDD33	VSS	VDD1833_7	VSS	VDD33	VSS	VDD1833_0	VDD33	VDD33	VDDP_18_2	P30_6	VSS	P29_2	P30_4	P30_1	VSS	P30_0	K
L	VSS	DDR_CAA1	VSS	VSS	VSS	DDR_CKEA1	VSS	VDD18_PLL2	VDD08_PLL2	VSS	VDD18_PLL3	VSS_PLL3	VDD08_PLL3	VSS	VSS	VSS	VSS	VSS	VSS	VDD1833_2	VDD1833_2	P29_4	P29_5	P31_0	P29_7	P30_2	P32_6	L
M	DDR_CKA_C	DDR_CAA3	DDR_CAA4	DDR_CSA0	DDR_CSA1	DDR_CKEA0	VSS	VSS_PLL2	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08_PLL0	VSS	VSS	P32_2	P32_1	VSS	P32_0	P31_7	P32_5	M
N	DDR_CKA_T	VSS	DDR_CAA2	VSS	DDR_CAA5	VSS	DDR_VDDQ	DDR_VAA	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS_PLL0	VDD18_PLL0	VSS	P32_4	P32_3	P32_7	P31_4	P31_3	P31_2	N
P	VSS	DDR_CKEB1	DDR_CAB0	DDR_CAA0	DDR_VDDQ	VSS	DDR_RESET_N	DDR_ATEST	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VSS	VSS	VDDP_18_33	VSS	P33_1	P33_0	P31_6	P31_5	P34_4	P
R	DDR_CKB_T	DDR_CKEB0	VSS	VSS	DDR_VDDQ	VSS	DDR_DTEST	DDR_ZN	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VDDP_18_X	VDD33	VSS	P34_1	P34_6	P33_2	P33_6	P33_7	P34_5	R
T	DDR_CKB_C	DDR_CAB1	DDR_VDDQ	DDR_CAB2	DDR_CAB5	DDR_CSB0	VSS	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD33_X	VSS	VDD1833_3	VDDP_18_3	P34_2	VSS	P33_5	P35_1	XTALSEL	T
U	DDR_CAB3	VSS	DDR_CAB4	DDR_DQB0	VSS	DDR_CSB1	VSS	VSS	VSS	VDD08	VSS	VDD08	VSS_PLL1	VSS_PLL4	VSS	VDD08	VSS	VSS	VSS	VSS	VDD1833_3	P35_6	P34_3	P33_4	P33_3	VSS	EXTCLKIN	U
V	DDR_DQB2	DDR_DQB1	VSS	DDR_DQB3	DDR_DQSB_T0	VSS	VSS	VSS	VDD1833_4	VDD33	VDDP_18_4	VDDP_18_5	VDD18_PLL1	VDD18_PLL4	VDD08	VSS	OTPVDD08	VSS	PCIE_VDD08A_L0	VSS	VSS	P35_3	P34_0	P35_5	P35_0	VSS	XTAL	V
W	VSS	DDR_DQB4	DDR_DQB7	DDR_DMB0	DDR_DQSB_C0	VSS	VSS	VSS	VDD1833_4	VDD33	VDDP_18_33	VDDP_18_33	VDD08_PLL1	VDD08_PLL4	VSS	VSS	OTPVDD18	VSS	PCIE_VDD08A_L0	VSS	VSS	VSS	P34_7	P35_4	P35_2	VSS	EXTAL	W
Y	DDR_DQB6	DDR_VDDQ	DDR_DQB5	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33	VDD33	VDD1833_5	VDD1833_5	VSS	USB_USVDD18	USB_USVDD33	PCIE_VDD08A_L1	PCIE_VDD18A_L1	PCIE_VDD18A_L0	VSS	VSS	VSS	VSS	VSS	VSS	Y
AA	DDR_DQB8	VSS	DDR_DQB15	VSS	DDR_DQSB_T1	VSS	P06_5	P05_1	P05_2	P05_0	VSS	P04_2	P02_2	VSS	VSS	USB_USDVDD	USB_USVDD18	USB_USVDD33	PCIE_VDD08A_L1	PCIE_VDD18A_L1	PCIE_VDD18A_L0	AVSS_ADC0	AVDD_ADC0	AVSSIO_ADC0	AVSSIO_ADC0	AN002	AN000	AA
AB	DDR_DQB14	DDR_DQB9	DDR_DMB1	DDR_DQB10	DDR_DQSB_C1	BSCANP	P06_3	P06_4	P07_7	P03_4	P03_3	P03_7	P02_1	P01_3	P00_5	USB_USDVDD	VSS	VSS	VSS	VSS	PCIE_VDD18A_CMN	AVSS_ADC1	AVDD_ADC1	AVDDIO_ADC0	AVDDREF_ADC0	AN001	AN003	AB
AC	DDR_DQB12	VSS	DDR_DQB13	DDR_DQB11	VSS	P06_1	P07_6	P07_4	P03_2	P03_1	P04_7	P03_5	P01_7	P02_0	P00_2	VSS	USB_TXRTUNE	VSS	PCIE_REFCLK_N1	PCIE_REFCLK_P0	PCIE_VDD18A_CMN	AVDD_ADC2	AVDDIO_ADC2	AVDDIO_ADC1	AVDDREF_ADC1	AN103	AN100	AC
AD	MDX	P08_6	P08_3	RES#	P08_2	P05_6	P08_0	VSS	P02_6	P04_6	P02_5	VSS	P01_6	P01_2	P00_1	USB_VUBUSIN	USB_OTG_ID	VSS	PCIE_REFCLK_P1	PCIE_REFCLK_N0	VSS	AVSS_ADC2	AVSSIO_ADC2	AVSSIO_ADC1	AVSSIO_ADC1	AN102	AN101	AD
AE	P09_0	P09_2	P08_5	P08_4	P06_0	P06_2	P05_7	P07_3	P02_7	P03_0	P04_0	P02_4	P01_5	P00_7	P00_0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVSSIO_ADC2	AN202	AN201	AE
AF	P09_3	P08_7	TRST#	P07_1	P05_5	VSS	P06_7	P07_0	P04_5	VSS	P04_1	P02_3	P01_0	VSS	P00_4	VSS	USB_QDP	VSS	PCIE_RXDN_L1	PCIE_RXDN_L0	VSS	PCIE_TXDN_L1	PCIE_TXDN_L0	VSS	AVDDREF_ADC2	AN204	AN200	AF
AG	VSS	P09_1	P08_1	P05_3	P07_2	P07_5	P05_4	P06_6	P03_6	P04_3	P04_4	P01_1	P01_4	P00_6	P00_3	VSS	USB_QDM	VSS	PCIE_RXDP_L1	PCIE_RXDP_L0	VSS	PCIE_TXDP_L1	PCIE_TXDP_L0	VSS	AN205	AN203	VSS	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 1.2 Pin arrangement (RZ/T2H 729-pin FCBGA) (top view)

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (1 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
A1	—	VSS	—	—	—	—	—	—	—	—	—
A2	VDD33	IRQ7	P11_4	—	—	DE1	MCLK31	—	—	—	HDSL09_SMPL
A3	VDD33	—	P11_6	—	GTIOC05_0A	—	—	—	—	—	TST_OUT00 / HDSL09_SEL1
A4	VDD33	—	P11_7	—	GTIOC05_0B	—	—	—	—	—	SI00# / HDSL09_MISO1
A5	VDD33	IRQ7	P10_1	WAIT#	MTIOC7D / GTIOC04_2B / GTIOC10_2B	SCK0	MDAT72	DISP_DATAR1	—	—	SI14# / HDSL08_LINK

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (2 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
A6	VDD33	IRQ0	P10_6	A3	MTIOC0B / GTIOC05_0A	DE0	MCLK21	DISP_DATAR6	—	—	HDSL08_MOSI1 / POUTA
A7	VDD1833_6	IRQ5	P14_0	A0	GTIOC06_4B	ETHSW_PTPOUT2 / ESC_SYNC0 / DE3	MCLK42	—	—	—	HDSL11_SMPL
A8	VDD1833_6	—	P13_6	D30	GTIOC06_3B / GTIOC04_3A	SS3#/CTS3#/ RTS3# / SPI_SSL23	MCLK41	—	—	—	ENCIFDO13 / TXDE09 / HDSL10_MOSI2
A9	VDD33	—	P14_4	DACK	POE4# / GTIOC06_1B / GTIOC09_1B / GTIOC06_3A / CMTW0_TIC0	ESC_IRQ / SS4#/ CTS4#/RTS4# / SD1_WP	—	DISP_DATAG4	—	MBX_HINT#	ENCIFDO00 / TXDE00 / HDSL11_MOSI1
A10	VDD33	IRQ9	P14_7	—	POE11# / GTIOC09_3A / CMTW0_TOC 1	ESC_I2CDATA / IIC_SDA0 / SD0_IOVS	MCLK32	—	—	—	SI02# / HDSL11_MISO2
A11	VDD33	—	P16_2	—	—	SCK5	MDAT51	—	—	—	SI03# / HDSL12_MOSI2
A12	VDD33	IRQ11	P16_4	—	GTETRGSB	ESC_LINKACT1 / TXD5/SDA5/MOSI5	—	—	—	—	TST_OUT04 / HDSL13_SMPL
A13	VDD1833_7	IRQ12	P17_0	—	GTIOC03_1B	SD1_DATA1	—	—	—	—	SI05# / HDSL13_MOSI1
A14	VDD33	—	P17_5	A7 / DACK	GTADSM00_1 / GTETRGC / CMTW1_TOC 0	SCK0 / CANTX0 / SD1_WP	—	—	—	—	TST_OUT07 / HDSL14_LINK
A15	VDD33	—	P19_4	—	GTIOC07_2A	—	—	—	—	—	TST_OUT10 / HDSL15_MOSI1
A16	VDD33	—	P19_5	—	GTIOC07_2B	—	—	—	—	—	SI10# / HDSL15_CLK2
A17	VDD1833_0	MDV	P20_1	—	—	ETH0_TXD0	—	—	—	—	—
A18	VDD1833_0	—	P20_0	—	—	ETH0_TXCLK	—	—	—	—	HDSL15_MOSI2
A19	VDD1833_0	—	P21_3	—	—	ETH0_RXDV	—	—	—	—	DUEI13 / HDSL00_CLK2
A20	VDD33	—	P23_1	—	GTIOC06_1A	ESC_IRQ	—	—	—	—	DUEI00 / HDSL02_LINK
A21	VDD33	—	P23_3	—	GTIOC06_2A	ESC_I2CCLK / IIC_SCL0	—	—	—	—	SI00# / HDSL02_CLK1
A22	VDD33	—	P23_2	—	GTIOC06_1B	ESC_RESETOUT#	—	—	—	—	TST_OUT00 / HDSL02_SMPL
A23	VDD1833_1	MD0	P24_6	—	—	ETH1_TXD0	—	—	—	—	—
A24	VDD1833_1	MDW1	P25_2	—	—	ETH1_TXEN	—	—	—	—	—
A25	VDD1833_1	—	P26_3	—	—	ETHSW_PHYLINK1 / ESC_PHYLINK1	—	—	—	—	HDSL04_SMPL
A26	VDD1833_1	MDW0	P25_1	—	—	ETH1_TXD3 / CANTXDP0	—	—	—	—	—
A27	—	VSS	—	—	—	—	—	—	—	—	—
B1	VDD33	IRQ2	P10_3	RD#	MTCLKD / MTIOC2B / GTIOC04_3B / GTIOC10_3B	TXD0/SDA0/MOSI0	MDAT10 / MDAT00	DISP_DATAR3	—	—	ENCIFOE04 / DEE04 / HDSL08_CLK1
B2	VDD33	IRQ1	P10_2	CS0#	MTCLKC / MTIOC2A / GTIOC04_3A / GTIOC10_3A	RXD0/SCL0/MISO0	MCLK10 / MCLK00	DISP_DATAR2	—	—	ENCIFCK04 / SCKE04 / HDSL08_SMPL
B3	VDD33	—	P10_5	A2	MTIOC1B / MTIOC0A / GTIOC04_4B	CTS0#	MDAT11 / MDAT01	DISP_DATAR5	—	—	ENCIFDI04 / RXDE04 / HDSL08_MISO1
B4	VDD33	—	P11_5	—	—	—	MDAT31	—	—	—	DUEI00 / HDSL09_CLK1
B5	VDD33	IRQ3	P10_4	A1	MTIOC1A / GTIOC04_4A	SS0#/CTS0#/RTS0#	MCLK11 / MCLK01	DISP_DATAR4	—	—	ENCIFDO04 / TXDE04 / HDSL08_SEL1

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (3 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
B6	VDD1833_6	IRQ1	P12_4	D20	GTIOC05_3A / CMTW1_TIC0	RXD2/SCL2/MISO2 / SD0_DATA2	MCLK02	—	—	—	ENCIFCK05 / SCKE05 / HDSL09_MOSI2
B7	VDD1833_6	IRQ4	P13_5	D29	GTIOC06_3A	TXD3/SDA3/MOSI3 / SPI_SSL32	MDAT40	—	—	—	ENCIFOE13 / DEE09 / HDSL10_MISO2
B8	VDD1833_6	—	P13_4	D28	GTIOC03_3B	RXD3/SCL3/MISO3 / SPI_SSL31	MCLK40	—	—	—	ENCIFCK13 / SCKE09 / HDSL10_SEL2
B9	VDD33	IRQ8	P14_6	—	POE10# / GTIOC06_2B / GTIOC09_2B / CMTW0_TIC1	ESC_I2CCLK / DE4 / IIC_SCL0 / SD0_PWEN	—	DISP_DATAG6	—	—	TST_OUT02 / HDSL11_SEL2
B10	—	VSS	—	—	—	—	—	—	—	—	—
B11	VDD33	—	P16_1	—	—	DE5	MCLK51	—	—	—	TST_OUT03 / HDSL12_MISO2
B12	VDD33	IRQ10	P16_3	—	GTETRGSA	ESC_LINKACT0 / RXD5/SCL5/MISO5	—	—	—	—	DUEI04 / HDSL13_LINK
B13	VDD1833_7	IRQ13	P17_1	—	GTIOC03_2A	SD1_DATA2	—	—	—	—	DUEI06 / HDSL13_CLK2
B14	—	VSS	—	—	—	—	—	—	—	—	—
B15	VDD33	SEI	P18_2	A10	GTADSM03_0 / GTIOC07_3B	ETH1_CRS / GMAC1_MDC / SCK1 / CANRX0 / SD1_PWEN	MCLK10	DISP_DATAB3	—	—	HDSL14_MOSI1
B16	VDD33	IRQ3	P18_6	A14	GTIOC07_4A / GTADSM05_0	CTS1# / CANRXDP1	MCLK12	DISP_DATAB7	—	—	ENCIFDO13 / ENCIFDO14 / TXDE09 / TXDE10 / HDSL14_MOSI2
B17	VDD1833_0	—	P20_5	—	—	ETH0_TXEN	—	—	—	—	DUEI11 / HDSL00_LINK
B18	—	VSS	—	—	—	—	—	—	—	—	—
B19	VDD1833_0	—	P21_2	—	—	ETH0_RXD3 / CANTXDP0	—	—	—	—	SI12# / HDSL00_MOSI1
B20	VDD33	IRQ14	P24_3	—	—	ESC_I2CCLK / IIC_SCL1 / CANRX0	MCLK70	—	—	—	HDSL03_LINK
B21	VDD33	—	P23_6	—	—	ETHSW_LPI0	MDAT60	—	—	—	SI01# / HDSL02_MOSI1
B22	—	VSS	—	—	—	—	—	—	—	—	—
B23	VDD1833_1	—	P26_1	—	—	GMAC1_MDC / ETHSW_MDC / ESC_MDC / CANRXDP1	—	—	—	—	HDSL03_MOSI2
B24	VDD1833_1	—	P26_2	—	—	GMAC1_MDIO / ETHSW_MDIO / ESC_MDIO / CANTXDP1	—	—	—	—	HDSL04_LINK
B25	VDD1833_1	MD2	P25_0	—	—	ETH1_TXD2 / CANRXDP0	—	—	—	—	—
B26	VDD1833_1	—	P25_3	—	—	ETH1_RXCLK	—	—	—	—	DUEI03 / HDSL03_SEL1
B27	VDD33	—	P28_3	—	GTIOC08_2A	SPI_SSL11	—	—	—	—	TST_OUT06 / HDSL05_CLK2
C1	VDD33	IRQ4	P11_1	—	—	ESC_LEDRUN / TXD1/SDA1/MOSI1	MDAT22	—	—	—	DUEI15 / HDSL08_MISO2
C2	VDD33	—	P09_5	D14	MTIOC6D / GTIOC04_0B / GTIOC10_0B	—	MDAT70	DISP_HSYNC	—	—	TST_OUT13 / HDSL07_CLK2
C3	VDD33	IRQ5	P11_2	—	—	SS1#/CTS1#/RTS1#	MCLK30	—	—	—	TST_OUT15 / HDSL08_MOSI2
C4	VDD33	IRQ9	P10_7	A4	MTIC5U / GTIOC05_0B / GTIOC00_3A	SCK1	MDAT21	DISP_DATAR7	—	—	HDSL08_CLK2 / POUTB

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (4 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
C5	VDD33	IRQ13	P11_0	A5	GTIOC00_3B	ESC_RESETOUT# / RXD1 / SCL1 / MISO1	MCLK22	DISP_DATAG0	—	—	HDSL08_SEL2 / POUTZ
C6	—	VSS	—	—	—	—	—	—	—	—	—
C7	VDD1833_6	—	P13_0	D24	GTIOC02_3A	DE2 / SPI_RSPCK3 / SD0_DATA6	MCLK00	—	—	—	ENCIFCK12 / ENCIFCK03 / SCKE08 / SCKE03 / HDSL10_SEL1
C8	VDD1833_6	IRQ14	P13_7	D31	GTIOC06_4A / GTIOC04_3B	CTS3#	MDAT41	—	—	—	ENCIFDI13 / RXDE09 / HDSL11_LINK
C9	VDD33	—	P14_1	RD/WR#	GTIOC06_0A / GTIOC09_0A / GTIOC05_3A / RTCAT1HZ	SCK4 / SD0_CD	MDAT42	DISP_DATAG1	—	—	DUEI02 / HDSL11_CLK1
C10	VDD33	—	P14_2	BS#	GTIOC06_0B / GTIOC09_0B / GTIOC05_3B	RXD4/SCL4/MISO4 / SD0_WP	—	DISP_DATAG2	—	—	ENCIFCK00 / SCKE00 / HDSL11_SEL1
C11	VDD33	—	P14_5	TEND	POE8# / GTIOC06_2A / GTIOC09_2A / GTIOC06_3B / CMTW0_TOC0	ESC_RESETOUT# / CTS4#	—	DISP_DATAG5	—	—	ENCIFDI00 / RXDE00 / HDSL11_CLK2
C12	VDD1833_7	—	P16_6	—	GTIOC03_0B	SD1_CMD	—	—	—	—	DUEI05 / HDSL13_SEL1
C13	VDD1833_7	IRQ15	P17_3	—	GTETRGA	—	—	—	—	—	SI06# / HDSL13_MISO2
C14	VDD33	—	P19_2	—	GTIOC07_1A	—	—	—	—	—	SI09# / HDSL15_SEL1
C15	VDD33	—	P19_3	—	GTIOC07_1B	—	—	—	—	—	DUEI10 / HDSL15_MISO1
C16	VDD33	IRQ4	P18_7	A15	GTIOC07_4B / GTADSM05_1	ETHSW_PTPOUT3 / ESC_SYNC1 / DE1 / CANTXDP1	MDAT12	—	—	—	ENCIFDI13 / ENCIFDI14 / RXDE09 / RXDE10 / HDSL15_LINK
C17	VDD1833_0	—	P20_3	—	—	ETH0_TXD2 / CANRX0	—	—	—	—	—
C18	VDD1833_0	—	P20_6	—	—	ETH0_RXCLK	—	—	—	—	TST_OUT11 / HDSL00_SMPL
C19	VDD1833_0	—	P21_4	—	—	GMAC0_MDC / ETHSW_MDC / ESC_MDC / CANRX1	—	—	—	—	TST_OUT13 / HDSL00_SEL2
C20	VDD33	—	P23_4	—	GTIOC06_2B	ESC_I2CDATA / IIC_SDA0	—	—	—	—	DUEI01 / HDSL02_SEL1
C21	VDD33	—	P23_5	—	—	ESC_LINKACT2	MCLK60	—	—	—	TST_OUT01 / HDSL02_MISO1
C22	VDD33	IRQ8	P22_6	A19	GTETRGSB	GMAC0_PTPTRG1 / ESC_LATCH1 / DE5 / CANTX1 / SD0_WP	—	—	—	—	DUEI15 / HDSL01_SEL2
C23	VDD1833_1	MD1	P24_7	—	—	ETH1_TXD1	—	—	—	—	—
C24	VDD1833_1	—	P24_5	—	—	ETH1_TXCLK	—	—	—	—	HDSL03_CLK1
C25	VDD1833_1	ETH1_REFCLK / RMII1_REFCLK	P26_4	—	—	—	—	—	—	—	—
C26	VDD1833_1	IRQ12	P26_5	—	—	CANTX0	—	—	—	—	ENCIFCK01 / SCKE01 / HDSL04_CLK1
C27	VDD33	IRQ4	P27_7	—	GTIOC08_0A	ETHSW_TDMAOUT0 / SPI_RSPCK1	—	—	—	—	DUEI05 / HDSL05_CLK1
D1	VDD33	IRQ6	P11_3	—	—	CTS1#	MDAT30	—	—	—	SI15# / HDSL09_LINK

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (5 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
D2	VDD33	—	P09_4	D13	MTIOC6B / GTIOC04_0A / GTIOC10_0A	—	MCLK70	DISP_CLK	—	—	DUEI13 / HDSL07_MOSI1
D3	VDD33	—	P09_6	D15	MTIOC7A / GTIOC04_1A / GTIOC10_1A	—	MCLK71	DISP_VSYNC	—	—	SI13# / HDSL07_SEL2
D4	VDD33	IRQ4	P10_0	WE1#	MTIOC7B / GTIOC04_2A / GTIOC10_2A	—	MCLK72	DISP_DATAR0	—	—	TST_OUT14 / HDSL07_MOSI2
D5	VDD33	—	P09_7	WE0#	MTIOC7C / GTIOC04_1B / GTIOC10_1B	—	MDAT71	DISP_DE	—	—	DUEI14 / HDSL07_MISO2
D6	VDD1833_6	—	P12_6	D22	GTIOC05_4A / GTIOC01_3B / CMTW1_TIC1	SS2#/CTS2#/ RTS2# / SD0_DATA4	MCLK10	—	—	—	ENCIFDO05 / TXDE05 / HDSL10_SMPL
D7	VDD1833_6	—	P12_0	D16	MTIC5V / GTIOC05_1A / CMTW0_TIC0	CANRX1 / SD0_CLK	—	—	—	—	DUEI01 / HDSL09_MOSI1
D8	—	VSS	—	—	—	—	—	—	—	—	—
D9	VDD33	IRQ6	P14_3	DREQ	POE0# / GTIOC06_1A / GTIOC09_1A	ESC_LINKACT2 / TXD4/SDA4/MOSI4 / SD1_CD	—	DISP_DATAG3	—	—	ENCIFOE00 / DEE00 / HDSL11_MISO1
D10	VDD33	IRQ1	P15_6	—	GTIOC09_6B	—	MDAT42	—	—	—	ENCIFDO07 / TXDE07 / HDSL12_MOSI1
D11	VDD33	IRQ2	P16_0	—	—	CTS5#	MDAT50	—	—	—	TXDE07 / DUEI03 / HDSL12_SEL2
D12	—	VSS	—	—	—	—	—	—	—	—	—
D13	VDD33	IRQ0	P18_3	A11	GTADSM03_1 / RTCAT1HZ	ETH1_COL / GMAC1_MDIO / RXD1/SCL1/MISO1 / CANTX0 / SD1_IOVS	MDAT10	DISP_DATAB4	—	—	HDSL14_CLK2
D14	VDD33	—	P19_0	—	GTIOC07_0A	—	—	—	—	—	DUEI09 / HDSL15_SMPL
D15	VDD33	IRQ7	P18_0	A8 / TEND	GTADSM02_0	ESC_LEDRUN / SS0#/CTS0#/ RTS0# / CANRXDP0 / SD1_PWEN	—	DISP_DATAB1	—	—	TST_OUT08 / HDSL14_SEL1
D16	—	VSS	—	—	—	—	—	—	—	—	—
D17	VDD1833_0	ETH0_REFCLK / RMII0_REFCLK	P21_7	—	—	CANTXDP1	—	—	—	—	HDSL01_LINK
D18	VDD1833_0	—	P20_7	—	—	ETH0_RXD0	—	—	—	—	SI11# / HDSL00_CLK1
D19	VDD1833_0	—	P21_6	—	—	ETHSW_PHYLINK0 / ESC_PHYLINK0 / CANRXDP1	—	—	—	—	HDSL00_MOSI2
D20	—	VSS	—	—	—	—	—	—	—	—	—
D21	VDD33	—	P22_1	—	GTETRGA	ETH0_TXER / TXD5/ SDA5/MOSI5 / CANTX0	—	—	—	—	HDSL01_CLK1
D22	VDD33	IRQ12	P24_1	—	—	—	MCLK62	—	—	—	SI02# / HDSL02_MISO2
D23	VDD1833_1	—	P25_6	—	—	ETH1_RXD2 / CANRX1	—	—	—	—	DUEI04 / HDSL03_CLK2
D24	—	VSS	—	—	—	—	—	—	—	—	—
D25	VDD1833_1	—	P26_0	—	—	ETH1_RXDV	—	—	—	—	SI04# / HDSL03_MISO2
D26	VDD33	SEI	P26_6	CS2#	—	ETH1_TXER / ESC_RESETOUT# / CANRX0	—	—	—	—	ENCIFOE01 / DEE01 / HDSL04_SEL1

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (6 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
D27	VDD33	—	P28_5	—	—	CANRX0 / SPI_SSL13	MCLK71	—	—	—	ENCIFCK08 / ENCIFCK00 / SCKE08 / SCKE00 / HDSL05_MISO2
E1	—	—	—	—	—	—	—	—	DDR_DQA12	—	—
E2	—	—	—	—	—	—	—	—	DDR_DQA9	—	—
E3	—	VSS	—	—	—	—	—	—	—	—	—
E4	—	—	—	—	—	—	—	—	DDR_DQA13	—	—
E5	—	VSS	—	—	—	—	—	—	—	—	—
E6	VDD1833_6	IRQ2	P12_7	D23	GTIOC05_4B / CMTW1_TOC1	CTS2# / SD0_DATA5	MDAT10	—	—	—	ENCIFDI05 / RXDE05 / HDSL10_CLK1
E7	VDD1833_6	—	P12_3	D19	GTIOC05_2B / CMTW0_TOC1	SCK2 / CANTXDP1 / SD0_DATA1	—	—	—	—	HDSL09_MISO2
E8	VDD1833_6	—	P12_2	D18	GTIOC05_2A / CMTW0_TIC1	CANRXDP1 / SD0_DATA0	—	—	—	—	SI01# / HDSL09_SEL2
E9	VDD33	—	P15_7	—	—	SS5#/CTS5#/RTS5#	MCLK50	—	—	—	ENCIFDI07 / RXDE07 / HDSL12_CLK2
E10	VDD33	—	P15_1	—	GTIOC09_4A	—	MCLK40	—	—	—	ENCIFOE06 / DEE06 / HDSL12_LINK
E11	VDD33	IRQ0	P15_5	—	GTIOC09_6A	—	MCLK42	—	—	—	ENCIFOE07 / DEE07 / HDSL12_MISO1
E12	VDD1833_7	IRQ14	P17_2	—	GTIOC03_2B	SD1_DATA3	—	—	—	—	TST_OUT06 / HDSL13_SEL2
E13	VDD33	IRQ15	P18_1	A9	GTADSM02_1 / GTIOC07_3A	ESC_LEDERR / CTS0# / CANTXDP0 / SD1_IOVS	—	DISP_DATAB2	—	—	SI08# / HDSL14_MISO1
E14	VDD33	—	P19_1	—	GTIOC07_0B	—	—	—	—	—	TST_OUT09 / HDSL15_CLK1
E15	VDD33	—	P17_7	WE3#/AH#	GTADSM01_1 / CMTW1_TOC1	ETHSW_PTPOUT1 / ESC_SYNC1 / TXD0/SDA0/MOSI0 / SD1_IOVS	—	DISP_DATAB0	—	—	DUEI08 / HDSL14_CLK1
E16	VDD33	—	P19_6	—	—	—	MCLK52	—	—	—	HDSL15_SEL2
E17	VDD1833_0	—	P20_2	—	—	ETH0_TXD1	—	—	—	—	—
E18	VDD1833_0	—	P21_0	—	—	ETH0_RXD1	—	—	—	—	DUEI12 / HDSL00_SEL1
E19	VDD1833_0	IRQ11	P22_0	—	—	—	—	—	—	—	HDSL01_SMPL
E20	VDD33	IRQ6	P22_4	A21	GTETRGD	ETH0_COL / SS5#/ CTS5#/RTS5# / CANTXDP0	—	—	—	—	TST_OUT14 / HDSL01_MOSI1
E21	VDD33	IRQ7	P22_5	A20	GTETRGSA	GMAC0_PTPTRG0 / ESC_LATCH0 / CTS5# / CANRX1 / SD0_CD	—	—	—	—	SI14# / HDSL01_CLK2
E22	VDD33	—	P22_2	A23	GTETRGB	ETH0_RXER / RXD5/SCL5/MISO5 / CANRX0	—	—	—	—	HDSL01_SEL1
E23	VDD1833_1	—	P25_4	—	—	ETH1_RXD0	—	—	—	—	TST_OUT03 / HDSL03_MISO1
E24	VDD1833_1	—	P25_7	—	—	ETH1_RXD3 / CANTX1	—	—	—	—	TST_OUT04 / HDSL03_SEL2
E25	VDD33	—	P28_4	—	GTIOC08_2B	SPI_SSL12	—	—	—	—	SI06# / HDSL05_SEL2
E26	VDD33	IRQ6	P28_1	—	GTIOC08_1A	ETHSW_TDMAOUT2 / SPI_MISO1	—	—	—	—	SI05# / HDSL05_MISO1

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (7 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
E27	VDD33	—	P28_6	—	—	CANTX0	MDAT71	—	—	—	ENCIFOE08 / ENCIFOE00 / DEE08 / DEE00 / HDSL05_MOSI2
F1	—	VSS	—	—	—	—	—	—	—	—	—
F2	—	—	—	—	—	—	—	—	DDR_DQA8	—	—
F3	—	—	—	—	—	—	—	—	DDR_DQA11	—	—
F4	—	—	—	—	—	—	—	—	DDR_DQA14	—	—
F5	—	—	—	—	—	—	—	—	DDR_DQSA_C1	—	—
F6	VDD1833_6	—	P13_3	D27	GTIOC03_3A	SCK3 / SPI_SSL30	MDAT01	—	—	—	ENCIFDI12 / ENCIFDI03 / RXDE08 / RXDE03 / HDSL10_CLK2
F7	VDD1833_6	—	P13_1	D25	GTIOC02_3B	SPI_MOSI3 / SD0_DATA7	MDAT00	—	—	—	ENCIFOE12 / ENCIFOE03 / DEE08 / DEE03 / HDSL10_MISO1
F8	VDD1833_6	IRQ3	P13_2	D26	—	SPI_MISO3 / SD0_RST#	MCLK01	—	—	—	ENCIFDO12 / ENCIFDO03 / TXDE08 / TXDE03 / HDSL10_MOSI1
F9	VDD33	—	P15_4	—	GTIOC09_5B	—	MDAT41	—	—	—	ENCIFCK07 / SCKE07 / HDSL12_SEL1
F10	—	VSS	—	—	—	—	—	—	—	—	—
F11	VDD33	—	P15_2	—	GTIOC09_4B	—	MDAT40	—	—	—	ENCIFDO06 / TXDE06 / HDSL12_SMPL
F12	VDD1833_7	—	P16_7	—	GTIOC03_1A	SD1_DATA0	—	—	—	—	TST_OUT05 / HDSL13_MISO1
F13	VDD33	—	P17_6	WE2#	GTADSM01_0 / GTETRGD / CMTW1_TIC1	ETHSW_PTPOUT0 / ESC_SYNC0 / RXD0/SCL0/MISO0 / SD1_PWEN	—	DISP_DATAG7	—	—	SI07# / HDSL14_SMPL
F14	—	VSS	—	—	—	—	—	—	—	—	—
F15	VDD33	IRQ1	P18_4	A12	GTIOC07_3A / GTADSM04_0	ESC_LEDSTER / TXD1/SDA1/MOSI1 / CANRX1	MCLK11	DISP_DATAB5	—	—	ENCIFCK13 / ENCIFCK14 / SCKE09 / SCKE10 / HDSL14_SEL2
F16	VDD33	—	P19_7	—	—	—	MDAT52	—	—	—	HDSL15_MISO2
F17	VDD1833_0	—	P20_4	—	—	ETH0_TXD3 / CANTX0	—	—	—	—	—
F18	—	VSS	—	—	—	—	—	—	—	—	—
F19	VDD33	IRQ11	P24_0	—	—	ETHSW_LPI2	MDAT61	—	—	—	TST_OUT02 / HDSL02_SEL2
F20	VDD33	IRQ5	P22_3	A22	GTETRGC	ETH0_CRS / SCK5 / CANRXDP0	—	—	—	—	DUEI14 / HDSL01_MISO1
F21	VDD33	IRQ13	P24_2	—	—	—	MDAT62	—	—	—	HDSL02_MOSI2
F22	—	VSS	—	—	—	—	—	—	—	—	—
F23	VDD1833_1	—	P25_5	—	—	ETH1_RXD1	—	—	—	—	SI03# / HDSL03_MOSI1
F24	VDD33	IRQ5	P28_0	—	GTIOC08_0B	ETHSW_TDMAOUT1 / SPI_MOSI1	—	—	—	—	TST_OUT05 / HDSL05_SEL1
F25	VDD33	—	P27_5	—	MTIOC1A / GTIOC08_4A / GTIOC02_2A	TXD0/SDA0/MOSI0 / SPI_SSL00	—	—	—	HSPI_IO3	ENCIFDO14 / TXDE10 / HDSL05_LINK
F26	—	VSS	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (8 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
F27	VDD33	—	P27_3	—	MTIOC2A / GTIOC08_3A / GTIOC02_1A	GMAC1_PTPTRG1 / SCK0 / CANRXDP1 / SPI_MOSI0	—	—	—	HSPI_IO1	ENCIFCK14 / SCKE10 / HDSL04_MISO2
G1	—	—	—	—	—	—	—	—	DDR_DQA15	—	—
G2	—	VSS	—	—	—	—	—	—	—	—	—
G3	—	—	—	—	—	—	—	—	DDR_DQA10	—	—
G4	—	—	—	—	—	—	—	—	DDR_DMIA1	—	—
G5	—	—	—	—	—	—	—	—	DDR_DQSA_T 1	—	—
G6	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
G7	VDD1833_6	—	P12_5	D21	GTIOC05_3B / GTIOC01_3A / CMTW1_TOC 0	TXD2/SDA2/MOSI2 / SD0_DATA3	MDAT02	—	—	—	ENCIFOE05 / DEE05 / HDSL10_LINK
G8	VDD1833_6	—	P12_1	D17	MTIC5W / GTIOC05_1B / CMTW0_TOC 0	CANTX1 / SD0_CMD	—	—	—	—	TST_OUT01 / HDSL09_CLK2
G9	VDD33	—	P15_0	—	GTIOC09_3B	—	MDAT32	—	—	—	ENCIFCK06 / SCKE06 / HDSL11_MOSI2
G10	—	VSS	—	—	—	—	—	—	—	—	—
G11	VDD33	—	P15_3	—	GTIOC09_5A	—	MCLK41	—	—	—	ENCIFDI06 / RXDE06 / HDSL12_CLK1
G12	VDD1833_7	—	P16_5	—	GTIOC03_0A	SD1_CLK	—	—	—	—	SI04# / HDSL13_CLK1
G13	VDD33	—	P17_4	A6 / DREQ	GTADSM00_0 / GTETRGB / CMTW1_TIC0	DE0 / CANRX0 / SD1_CD	—	—	—	—	DUEI07 / HDSL13_MOSI2
G14	—	VSS	—	—	—	—	—	—	—	—	—
G15	VDD33	IRQ2	P18_5	A13	GTIOC07_3B / GTADSM04_1	SS1#/CTS1#/ RTS1# / CANTX1	MDAT11	DISP_DATAB6	—	—	ENCIFOE13 / ENCIFOE14 / DEE09 / DEE10 / HDSL14_MISO2
G16	VDD1833_0	—	P21_5	—	—	GMAC0_MDIO / ETHSW_MDIO / ESC_MDIO / CANTX1	—	—	—	—	SI13# / HDSL00_MISO2
G17	VDD1833_0	—	P21_1	—	—	ETH0_RXD2 / CANRXDP0	—	—	—	—	TST_OUT12 / HDSL00_MISO1
G18	—	VSS	—	—	—	—	—	—	—	—	—
G19	VDD33	—	P23_7	—	—	ETHSW_LPI1	MCLK61	—	—	—	DUEI02 / HDSL02_CLK2
G20	VDD33	IRQ10	P23_0	A17	GTIOC06_0B	ETH1_COL / ETHSW_TDMAOUT 3 / ESC_LINKACT1 / CANTXDP1	—	—	—	—	SI15# / HDSL01_MOSI2
G21	VDD33	IRQ9	P22_7	A18	GTIOC06_0A	ETH1_CRS / ETHSW_TDMAOUT 2 / ESC_LINKACT0 / CANRXDP1	—	—	—	—	TST_OUT15 / HDSL01_MISO2
G22	VDD33	IRQ15	P24_4	—	—	ESC_I2CDATA / IIC_SDA1 / CANTX0	MDAT70	—	—	—	HDSL03_SMPL
G23	VDD33	IRQ1	P27_0	CS5#	—	ETH1_CRS / CANTXDP0 / SPI_SSL02	—	—	—	HSPI_INT#	ENCIFDI01 / RXDE01 / HDSL04_MOSI1
G24	VDD33	IRQ2	P27_1	—	GTIOC02_0A	ETH1_COL / CANRX1 / SPI_SSL03	—	—	—	HSPI_CS#	HDSL04_CLK2
G25	VDD33	IRQ7	P28_2	—	GTIOC08_1B	ETHSW_TDMAOUT 3 / SPI_SSL10	—	—	—	—	DUEI06 / HDSL05_MOSI1

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (9 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
G26	VDD33	IRQ3	P27_2	—	GTIOC02_0B	GMAC1_PTPTRG0 / ESC_LEDERR / CANTX1 / SPI_RSPCK0	—	—	—	HSPI_IO0	HDSL04_SEL2
G27	VDD33	—	P27_6	—	MTIOC1B / GTIOC08_4B / GTIOC02_2B	—	—	—	—	HSPI_CK	ENCIFDI14 / RXDE10 / HDSL05_SMPL
H1	—	—	—	—	—	—	—	—	DDR_DQA6	—	—
H2	—	—	—	—	—	—	—	—	DDR_DQA5	—	—
H3	—	VSS	—	—	—	—	—	—	—	—	—
H4	—	VSS	—	—	—	—	—	—	—	—	—
H5	—	VSS	—	—	—	—	—	—	—	—	—
H6	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
H7	—	VSS	—	—	—	—	—	—	—	—	—
H8	—	VSS	—	—	—	—	—	—	—	—	—
H9	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
H10	—	VSS	—	—	—	—	—	—	—	—	—
H11	—	VDDP_18_6	—	—	—	—	—	—	—	—	—
H12	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
H13	—	VSS	—	—	—	—	—	—	—	—	—
H14	—	VDDP_18_7	—	—	—	—	—	—	—	—	—
H15	—	VSS	—	—	—	—	—	—	—	—	—
H16	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
H17	—	VSS	—	—	—	—	—	—	—	—	—
H18	—	VDDP_18_0	—	—	—	—	—	—	—	—	—
H19	—	VSS	—	—	—	—	—	—	—	—	—
H20	—	VDDP_18_1	—	—	—	—	—	—	—	—	—
H21	—	VDD1833_1	—	—	—	—	—	—	—	—	—
H22	VDD33	IRQ0	P26_7	CS3#	—	ETH1_RXER / ESC_LEDSTER / CANRXDP0 / SPI_SSL01	—	—	—	—	ENCIFDO01 / TXDE01 / HDSL04_MISO1
H23	VDD33	—	P28_7	—	—	CANRXDP0	MCLK72	—	—	—	ENCIFDO08 / ENCIFDO00 / TXDE08 / TXDE00 / HDSL06_LINK
H24	—	VSS	—	—	—	—	—	—	—	—	—
H25	VDD33	—	P29_0	—	—	CANTXDP0	MDAT72	—	—	—	ENCIFDI08 / ENCIFDI00 / RXDE08 / RXDE00 / HDSL06_SMPL
H26	VDD33	—	P27_4	—	MTIOC2B / GTIOC08_3B / GTIOC02_1B	RXD0/SCL0/MISO0 / CANTXDP1 / SPI_MISO0	—	—	—	HSPI_IO2	ENCIFOE14 / DEE10 / HDSL04_MOSI2
H27	VDD1833_2	—	P29_3	—	GTIOC09_1A	ETH2_TXD1	—	—	—	—	ENCIFDO09 / TXDE09 / HDSL06_MISO1
J1	—	—	—	—	—	—	—	—	DDR_DQA4	—	—
J2	—	VSS	—	—	—	—	—	—	—	—	—
J3	—	—	—	—	—	—	—	—	DDR_DMIA0	—	—
J4	—	—	—	—	—	—	—	—	DDR_DQA7	—	—
J5	—	—	—	—	—	—	—	—	DDR_DQSA_C 0	—	—
J6	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
J7	—	VDD33	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (10 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
J8	—	VSS	—	—	—	—	—	—	—	—	—
J9	—	VDD1833_6	—	—	—	—	—	—	—	—	—
J10	—	AVDD18A_TSU	—	—	—	—	—	—	—	—	—
J11	—	VDD33	—	—	—	—	—	—	—	—	—
J12	—	VSS	—	—	—	—	—	—	—	—	—
J13	—	VDD1833_7	—	—	—	—	—	—	—	—	—
J14	—	VSS	—	—	—	—	—	—	—	—	—
J15	—	VDD33	—	—	—	—	—	—	—	—	—
J16	—	VSS	—	—	—	—	—	—	—	—	—
J17	—	VDD1833_0	—	—	—	—	—	—	—	—	—
J18	—	VSS	—	—	—	—	—	—	—	—	—
J19	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
J20	—	VSS	—	—	—	—	—	—	—	—	—
J21	—	VDD1833_1	—	—	—	—	—	—	—	—	—
J22	VDD1833_2	—	P30_5	—	GTIOC09_6A	GMAC2_MDC / ETHSW_MDC / ESC_MDC / SPI_RSPCK3	—	—	—	—	DUEI07 / HDSL07_MISO1
J23	VDD1833_2	—	P29_6	—	GTIOC09_2B	ETH2_TXEN / SPI_SSL22	—	—	—	—	ENCIFOE10 / DEE10 / HDSL06_SEL2
J24	VDD1833_2	IRQ14	P30_7	—	—	ETHSW_PHYLINK2 / ESC_PHYLINK2 / SPI_MISO3 / SD1_IOVS	MCLK30	—	—	—	SI07# / HDSL07_CLK2
J25	VDD1833_2	—	P29_1	—	GTIOC09_0A	ETH2_TXCLK	—	—	—	—	ENCIFCK09 / SCKE09 / HDSL06_CLK1
J26	VDD1833_2	IRQ13	P31_1	—	GTETRGSB	ETH2_RXER / SPI_SSL31	—	—	—	—	HDSL07_MISO2
J27	VDD1833_2	IRQ11	P30_3	—	GTIOC09_5A	ETH2_RXD3 / SPI_MISO2	—	—	—	—	ENCIFDO11 / TXDE11 / HDSL07_CLK1
K1	—	—	—	—	—	—	—	—	DDR_DQA2	—	—
K2	—	—	—	—	—	—	—	—	DDR_DQA0	—	—
K3	—	—	—	—	—	—	—	—	DDR_DQA1	—	—
K4	—	—	—	—	—	—	—	—	DDR_DQA3	—	—
K5	—	—	—	—	—	—	—	—	DDR_DQSA_T0	—	—
K6	—	VSS	—	—	—	—	—	—	—	—	—
K7	—	VDD33	—	—	—	—	—	—	—	—	—
K8	—	VSS	—	—	—	—	—	—	—	—	—
K9	—	VDD1833_6	—	—	—	—	—	—	—	—	—
K10	—	DVDD08A_TSU	—	—	—	—	—	—	—	—	—
K11	—	VDD33	—	—	—	—	—	—	—	—	—
K12	—	VSS	—	—	—	—	—	—	—	—	—
K13	—	VDD1833_7	—	—	—	—	—	—	—	—	—
K14	—	VSS	—	—	—	—	—	—	—	—	—
K15	—	VDD33	—	—	—	—	—	—	—	—	—
K16	—	VSS	—	—	—	—	—	—	—	—	—
K17	—	VDD1833_0	—	—	—	—	—	—	—	—	—
K18	—	VDD33	—	—	—	—	—	—	—	—	—
K19	—	VDD33	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (11 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
K20	—	VDDP_18_2	—	—	—	—	—	—	—	—	—
K21	VDD1833_2	—	P30_6	—	GTIOC09_6B	GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / SPI_MOSI3	—	—	—	—	TST_OUT07 / HDSL07_MOSI1
K22	—	VSS	—	—	—	—	—	—	—	—	—
K23	VDD1833_2	—	P29_2	—	GTIOC09_0B	ETH2_TXD0	—	—	—	—	ENCIFOE09 / DEE09 / HDSL06_SEL1
K24	VDD1833_2	—	P30_4	—	GTIOC09_5B	ETH2_RXDV	—	—	—	—	ENCIFDI11 / RXDE11 / HDSL07_SEL1
K25	VDD1833_2	—	P30_1	—	GTIOC09_4A	ETH2_RXD1	—	—	—	—	ENCIFCK11 / SCKE11 / HDSL07_LINK
K26	—	VSS	—	—	—	—	—	—	—	—	—
K27	VDD1833_2	—	P30_0	—	GTIOC09_3B	ETH2_RXD0	—	—	—	—	ENCIFDI10 / RXDE10 / HDSL06_MOSI2
L1	—	VSS	—	—	—	—	—	—	—	—	—
L2	—	—	—	—	—	—	—	—	DDR_CAA1	—	—
L3	—	VSS	—	—	—	—	—	—	—	—	—
L4	—	VSS	—	—	—	—	—	—	—	—	—
L5	—	VSS	—	—	—	—	—	—	—	—	—
L6	—	—	—	—	—	—	—	—	DDR_CKEA1	—	—
L7	—	VSS	—	—	—	—	—	—	—	—	—
L8	—	VDD18_PLL2	—	—	—	—	—	—	—	—	—
L9	—	VDD08_PLL2	—	—	—	—	—	—	—	—	—
L10	—	VSS	—	—	—	—	—	—	—	—	—
L11	—	VDD18_PLL3	—	—	—	—	—	—	—	—	—
L12	—	VSS_PLL3	—	—	—	—	—	—	—	—	—
L13	—	VDD08_PLL3	—	—	—	—	—	—	—	—	—
L14	—	VSS	—	—	—	—	—	—	—	—	—
L15	—	VSS	—	—	—	—	—	—	—	—	—
L16	—	VSS	—	—	—	—	—	—	—	—	—
L17	—	VSS	—	—	—	—	—	—	—	—	—
L18	—	VSS	—	—	—	—	—	—	—	—	—
L19	—	VSS	—	—	—	—	—	—	—	—	—
L20	—	VDD1833_2	—	—	—	—	—	—	—	—	—
L21	—	VDD1833_2	—	—	—	—	—	—	—	—	—
L22	VDD1833_2	IRQ8	P29_4	—	GTIOC09_1B	ETH2_TXD2 / SPI_SSL20	—	—	—	—	ENCIFDI09 / RXDE09 / HDSL06_MOSI1
L23	VDD1833_2	IRQ9	P29_5	—	GTIOC09_2A	ETH2_TXD3 / SPI_SSL21	—	—	—	—	ENCIFCK10 / SCKE10 / HDSL06_CLK2
L24	VDD1833_2	ETH2_REFCLK / RMII2_REFCLK	P31_0	—	GTETRGSA	SPI_SSL30	—	—	—	—	HDSL07_SEL2
L25	VDD1833_2	—	P29_7	—	GTIOC09_3A	ETH2_RXCLK / SPI_SSL23	—	—	—	—	ENCIFDO10 / TXDE10 / HDSL06_MISO2
L26	VDD1833_2	IRQ10	P30_2	—	GTIOC09_4B	ETH2_RXD2 / SPI_MOSI2	—	—	—	—	ENCIFOE11 / DEE11 / HDSL07_SMPL

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (12 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
L27	VDD33	—	P32_6	—	GTIOC10_2A / GTIOC01_2A	SPI_SSL10	—	—	—	—	ENCIFCK11 / SCKE11 / HDSL09_SMPL
M1	—	—	—	—	—	—	—	—	DDR_CKA_C	—	—
M2	—	—	—	—	—	—	—	—	DDR_CAA3	—	—
M3	—	—	—	—	—	—	—	—	DDR_CAA4	—	—
M4	—	—	—	—	—	—	—	—	DDR_CSA0	—	—
M5	—	—	—	—	—	—	—	—	DDR_CSA1	—	—
M6	—	—	—	—	—	—	—	—	DDR_CKEA0	—	—
M7	—	VSS	—	—	—	—	—	—	—	—	—
M8	—	VSS_PLL2	—	—	—	—	—	—	—	—	—
M9	—	VDD08	—	—	—	—	—	—	—	—	—
M10	—	VSS	—	—	—	—	—	—	—	—	—
M11	—	VDD08	—	—	—	—	—	—	—	—	—
M12	—	VSS	—	—	—	—	—	—	—	—	—
M13	—	VDD08	—	—	—	—	—	—	—	—	—
M14	—	VSS	—	—	—	—	—	—	—	—	—
M15	—	VDD08	—	—	—	—	—	—	—	—	—
M16	—	VSS	—	—	—	—	—	—	—	—	—
M17	—	VDD08	—	—	—	—	—	—	—	—	—
M18	—	VSS	—	—	—	—	—	—	—	—	—
M19	—	VDD08_PLL0	—	—	—	—	—	—	—	—	—
M20	—	VSS	—	—	—	—	—	—	—	—	—
M21	—	VSS	—	—	—	—	—	—	—	—	—
M22	VDD33	—	P32_2	—	GTIOC10_0A / GTIOC01_0A	SPI_SSL03	—	—	—	—	ENCIFCK10 / SCKE10 / HDSL08_SEL2
M23	VDD33	—	P32_1	—	—	SPI_SSL02	—	—	—	—	ENCIFDI15 / ENCIFDI01 / RXDE11 / RXDE01 / HDSL08_CLK2
M24	—	VSS	—	—	—	—	—	—	—	—	—
M25	VDD33	—	P32_0	—	—	SPI_SSL01	—	—	—	—	ENCIFDO15 / ENCIFDO01 / TXDE11 / TXDE01 / HDSL08_MOSI1
M26	VDD33	—	P31_7	—	—	GMAC2_PTPTRG1 / SPI_SSL00	—	—	—	—	ENCIFOE15 / ENCIFOE01 / DEE11 / DEE01 / HDSL08_MISO1
M27	VDD33	—	P32_5	—	GTIOC10_1B / GTIOC01_1B	SPI_MISO1	—	—	—	—	ENCIFDI10 / RXDE10 / HDSL09_LINK
N1	—	—	—	—	—	—	—	—	DDR_CKA_T	—	—
N2	—	VSS	—	—	—	—	—	—	—	—	—
N3	—	—	—	—	—	—	—	—	DDR_CAA2	—	—
N4	—	VSS	—	—	—	—	—	—	—	—	—
N5	—	—	—	—	—	—	—	—	DDR_CAA5	—	—
N6	—	VSS	—	—	—	—	—	—	—	—	—
N7	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
N8	—	DDR_VAA	—	—	—	—	—	—	—	—	—
N9	—	VSS	—	—	—	—	—	—	—	—	—
N10	—	VDD08	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (13 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
N11	—	VSS	—	—	—	—	—	—	—	—	—
N12	—	VDD08	—	—	—	—	—	—	—	—	—
N13	—	VSS	—	—	—	—	—	—	—	—	—
N14	—	VDD08	—	—	—	—	—	—	—	—	—
N15	—	VSS	—	—	—	—	—	—	—	—	—
N16	—	VDD08	—	—	—	—	—	—	—	—	—
N17	—	VSS	—	—	—	—	—	—	—	—	—
N18	—	VDD08	—	—	—	—	—	—	—	—	—
N19	—	VSS_PLL0	—	—	—	—	—	—	—	—	—
N20	—	VDD18_PLL0	—	—	—	—	—	—	—	—	—
N21	—	VSS	—	—	—	—	—	—	—	—	—
N22	VDD33	—	P32_4	—	GTIOC10_1A / GTIOC01_1A	SPI_MOSI1	—	—	—	—	ENCIFDO10 / TXDE10 / HDSL08_MOSI2
N23	VDD33	—	P32_3	—	GTIOC10_0B / GTIOC01_0B	SPI_RSPCK1	—	—	—	—	ENCIFOE10 / DEE10 / HDSL08_MISO2
N24	VDD33	—	P32_7	—	GTIOC10_2B / GTIOC01_2B	SPI_SSL11	—	—	—	—	ENCIFOE11 / DEE11 / HDSL09_CLK1
N25	VDD33	—	P31_4	DREQ	POE8#	ETH2_CRS / ETHSW_PTPOUT2 / ESC_SYNC0 / SPI_RSPCK0 / SPI_SSL30	MCLK81 / MDAT31	—	—	HSPI_IO6	ENCIFDO09 / TXDE09 / HDSL08_SMPL / POUTB
N26	VDD33	—	P31_3	—	POE4#	ETH2_RXER / ETHSW_TDMAOUT 1 / ESC_LEDERR / SPI_SSL33	MDAT80 / MCLK31	—	—	HSPI_IO5	ENCIFOE09 / DEE09 / HDSL08_LINK
N27	VDD33	—	P31_2	—	POE0#	ETH2_TXER / SPI_SSL32	MCLK80 / MDAT30	—	—	HSPI_IO4	ENCIFCK09 / SCKE09 / HDSL07_MOSI2 / POUTA
P1	—	VSS	—	—	—	—	—	—	—	—	—
P2	—	—	—	—	—	—	—	—	DDR_CKEB1	—	—
P3	—	—	—	—	—	—	—	—	DDR_CAB0	—	—
P4	—	—	—	—	—	—	—	—	DDR_CAA0	—	—
P5	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
P6	—	VSS	—	—	—	—	—	—	—	—	—
P7	—	—	—	—	—	—	—	—	DDR_RESET_N	—	—
P8	—	—	—	—	—	—	—	—	DDR_ATEST	—	—
P9	—	VDD08	—	—	—	—	—	—	—	—	—
P10	—	VSS	—	—	—	—	—	—	—	—	—
P11	—	VDD08	—	—	—	—	—	—	—	—	—
P12	—	VSS	—	—	—	—	—	—	—	—	—
P13	—	VDD08	—	—	—	—	—	—	—	—	—
P14	—	VSS	—	—	—	—	—	—	—	—	—
P15	—	VDD08	—	—	—	—	—	—	—	—	—
P16	—	VSS	—	—	—	—	—	—	—	—	—
P17	—	VDD08	—	—	—	—	—	—	—	—	—
P18	—	VSS	—	—	—	—	—	—	—	—	—
P19	—	VSS	—	—	—	—	—	—	—	—	—
P20	—	VSS	—	—	—	—	—	—	—	—	—
P21	—	VDDP_18_33	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (14 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
P22	—	VSS	—	—	—	—	—	—	—	—	—
P23	VDD33	—	P33_1	—	GTIOC10_3B	SPI_SSL13	MDAT82	—	—	—	ENCIFDI11 / RXDE11 / HDSL09_MISO1
P24	VDD33	—	P33_0	—	GTIOC10_3A	SPI_SSL12	MCLK82	—	—	—	ENCIFDO11 / TXDE11 / HDSL09_SEL1
P25	VDD33	—	P31_6	A16 / TEND	POE11#	GMAC2_PTPTRG0 / ETHSW_TDMAOUT 0 / ESC_LEDRUN / SPI_MISO0	MDAT32	—	—	—	ENCIFCK15 / ENCIFCK01 / SCKE11 / SCKE01 / HDSL08_SEL1
P26	VDD33	—	P31_5	DACK	POE10#	ETH2_COL / ETHSW_PTPOUT3 / ESC_SYNC1 / SPI_MOSI0 / SPI_SSL31	MDAT81 / MCLK32	—	—	HSPI_IO7	ENCIFDI09 / RXDE09 / HDSL08_CLK1 / POUTZ
P27	VDD1833_3	—	P34_4	CS2#	GTADSM05_0 / GTIOC03_2A	ETH3_RXD3 / RXD3/ SCL3/MISO3 / SPI_SSL22 / SD1_IOVS	—	—	ADTRG0#	—	ENCIFDO07 / TXDE07 / HDSL10_MOSI1
R1	—	—	—	—	—	—	—	—	DDR_CKB_T	—	—
R2	—	—	—	—	—	—	—	—	DDR_CKEB0	—	—
R3	—	VSS	—	—	—	—	—	—	—	—	—
R4	—	VSS	—	—	—	—	—	—	—	—	—
R5	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
R6	—	VSS	—	—	—	—	—	—	—	—	—
R7	—	—	—	—	—	—	—	—	DDR_DTEST	—	—
R8	—	—	—	—	—	—	—	—	DDR_ZN	—	—
R9	—	VSS	—	—	—	—	—	—	—	—	—
R10	—	VDD08	—	—	—	—	—	—	—	—	—
R11	—	VSS	—	—	—	—	—	—	—	—	—
R12	—	VDD08	—	—	—	—	—	—	—	—	—
R13	—	VSS	—	—	—	—	—	—	—	—	—
R14	—	VDD08	—	—	—	—	—	—	—	—	—
R15	—	VSS	—	—	—	—	—	—	—	—	—
R16	—	VDD08	—	—	—	—	—	—	—	—	—
R17	—	VSS	—	—	—	—	—	—	—	—	—
R18	—	VDD08	—	—	—	—	—	—	—	—	—
R19	—	VDDP_18_X	—	—	—	—	—	—	—	—	—
R20	—	VDD33	—	—	—	—	—	—	—	—	—
R21	—	VSS	—	—	—	—	—	—	—	—	—
R22	VDD1833_3	—	P34_1	A23	GTADSM03_1 / GTIOC03_0B	ETH3_RXD0 / SPI_MISO2	—	—	—	—	ENCIFDI06 / RXDE06 / HDSL10_CLK1
R23	VDD1833_3	ETH3_REFCLK / RMII3_REFCLK	P34_6	CS5#	—	ETH1_RXER / ESC_I2CDATA / IIC_SDA1 / SPI_RSPCK3	—	—	ADTRG2#	—	DUEI08 / HDSL10_SEL2
R24	VDD1833_3	—	P33_2	A16	GTADSM00_0	ETH3_TXCLK / SCK1 / SPI_RSPCK1 / SPI_SSL30	MCLK50	—	—	—	ENCIFCK01 / SCKE01 / HDSL09_MOSI1
R25	VDD1833_3	IRQ15	P33_6	A20	GTADSM02_0	ETH3_TXD3 / TXD2/ SDA2/MOSI2 / SPI_SSL11 / SPI_SSL00	MCLK52	—	—	—	ENCIFCK06 / SCKE06 / HDSL09_MOSI2
R26	VDD1833_3	—	P33_7	A21	GTADSM02_1	ETH3_TXEN / SPI_RSPCK2	MDAT52	—	—	—	ENCIFOE06 / DEE06 / HDSL10_LINK

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (15 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
R27	VDD1833_3	—	P34_5	CS3#	GTADSM05_1 / GTIOC03_2B	ETH3_RXDV / ESC_I2CCLK / TXD3/SDA3/MOSI3 / IIC_SCL1 / SPI_SSL23	—	—	ADTRG1#	—	ENCIFDI07 / RXDE07 / HDSL10_CLK2
T1	—	—	—	—	—	—	—	—	DDR_CKB_C	—	—
T2	—	—	—	—	—	—	—	—	DDR_CAB1	—	—
T3	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
T4	—	—	—	—	—	—	—	—	DDR_CAB2	—	—
T5	—	—	—	—	—	—	—	—	DDR_CAB5	—	—
T6	—	—	—	—	—	—	—	—	DDR_CSB0	—	—
T7	—	VSS	—	—	—	—	—	—	—	—	—
T8	—	VSS	—	—	—	—	—	—	—	—	—
T9	—	VDD08	—	—	—	—	—	—	—	—	—
T10	—	VSS	—	—	—	—	—	—	—	—	—
T11	—	VDD08	—	—	—	—	—	—	—	—	—
T12	—	VSS	—	—	—	—	—	—	—	—	—
T13	—	VDD08	—	—	—	—	—	—	—	—	—
T14	—	VSS	—	—	—	—	—	—	—	—	—
T15	—	VDD08	—	—	—	—	—	—	—	—	—
T16	—	VSS	—	—	—	—	—	—	—	—	—
T17	—	VDD08	—	—	—	—	—	—	—	—	—
T18	—	VSS	—	—	—	—	—	—	—	—	—
T19	—	VDD33_X	—	—	—	—	—	—	—	—	—
T20	—	VSS	—	—	—	—	—	—	—	—	—
T21	—	VDD1833_3	—	—	—	—	—	—	—	—	—
T22	—	VDDP_18_3	—	—	—	—	—	—	—	—	—
T23	VDD1833_3	—	P34_2	A24	GTADSM04_0 / GTIOC03_1A	ETH3_RXD1 / SPI_SSL20	—	—	—	—	ENCIFCK07 / SCKE07 / HDSL10_SEL1
T24	—	VSS	—	—	—	—	—	—	—	—	—
T25	VDD1833_3	IRQ14	P33_5	A19	GTADSM01_1	ETH3_TXD2 / RXD2/ SCL2/MISO2 / SPI_SSL10 / SPI_MISO0	MDAT51	—	—	—	ENCIFDI01 / RXDE01 / HDSL09_MISO2
T26	VDD33	—	P35_1	TEND	GTADSM07_0	ETH3_CRS / SPI_SSL30 / SPI_MISO1	MCLK90	—	—	—	DUEI09 / HDSL11_LINK
T27	VDD33_X	XTALSEL	—	—	—	—	—	—	—	—	—
U1	—	—	—	—	—	—	—	—	DDR_CAB3	—	—
U2	—	VSS	—	—	—	—	—	—	—	—	—
U3	—	—	—	—	—	—	—	—	DDR_CAB4	—	—
U4	—	—	—	—	—	—	—	—	DDR_DQB0	—	—
U5	—	VSS	—	—	—	—	—	—	—	—	—
U6	—	—	—	—	—	—	—	—	DDR_CSB1	—	—
U7	—	VSS	—	—	—	—	—	—	—	—	—
U8	—	VSS	—	—	—	—	—	—	—	—	—
U9	—	VSS	—	—	—	—	—	—	—	—	—
U10	—	VDD08	—	—	—	—	—	—	—	—	—
U11	—	VSS	—	—	—	—	—	—	—	—	—
U12	—	VDD08	—	—	—	—	—	—	—	—	—
U13	—	VSS_PLL1	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (16 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
U14	—	VSS_PLL4	—	—	—	—	—	—	—	—	—
U15	—	VSS	—	—	—	—	—	—	—	—	—
U16	—	VDD08	—	—	—	—	—	—	—	—	—
U17	—	VSS	—	—	—	—	—	—	—	—	—
U18	—	VSS	—	—	—	—	—	—	—	—	—
U19	—	VSS	—	—	—	—	—	—	—	—	—
U20	—	VSS	—	—	—	—	—	—	—	—	—
U21	—	VDD1833_3	—	—	—	—	—	—	—	—	—
U22	VDD33	—	P35_6	—	GTADSM09_1	TXD4/SDA4/MOSI4 / SPI_SSL12	MDAT92	—	—	—	SI10# / HDSL11_MOSI1
U23	VDD1833_3	—	P34_3	A25	GTADSM04_1 / GTIOC03_1B	ETH3_RXD2 / SPI_SSL21 / SD1_PWEN	—	—	—	—	ENCIFOE07 / DEE07 / HDSL10_MISO1
U24	VDD1833_3	IRQ13	P33_4	A18	GTADSM01_0	ETH3_TXD1 / TXD1/ SDA1/MOSI1 / SPI_MISO1 / SPI_MOSI0	MCLK51	—	PCIE_RSTOUT1B	—	ENCIFDO01 / TXDE01 / HDSL09_SEL2
U25	VDD1833_3	IRQ12	P33_3	A17	GTADSM00_1	ETH3_TXD0 / RXD1/ SCL1/MISO1 / SPI_MOSI1 / SPI_RSPCK0	MDAT50	—	PCIE_RSTOUT0B	—	ENCIFOE01 / DEE01 / HDSL09_CLK2
U26	—	VSS	—	—	—	—	—	—	—	—	—
U27	VDD33_X	EXTCLKIN	—	—	—	—	—	—	—	—	—
V1	—	—	—	—	—	—	—	—	DDR_DQB2	—	—
V2	—	—	—	—	—	—	—	—	DDR_DQB1	—	—
V3	—	VSS	—	—	—	—	—	—	—	—	—
V4	—	—	—	—	—	—	—	—	DDR_DQB3	—	—
V5	—	—	—	—	—	—	—	—	DDR_DQSB_T0	—	—
V6	—	VSS	—	—	—	—	—	—	—	—	—
V7	—	VSS	—	—	—	—	—	—	—	—	—
V8	—	VSS	—	—	—	—	—	—	—	—	—
V9	—	VDD1833_4	—	—	—	—	—	—	—	—	—
V10	—	VDD33	—	—	—	—	—	—	—	—	—
V11	—	VDDP_18_4	—	—	—	—	—	—	—	—	—
V12	—	VDDP_18_5	—	—	—	—	—	—	—	—	—
V13	—	VDD18_PLL1	—	—	—	—	—	—	—	—	—
V14	—	VDD18_PLL4	—	—	—	—	—	—	—	—	—
V15	—	VDD08	—	—	—	—	—	—	—	—	—
V16	—	VSS	—	—	—	—	—	—	—	—	—
V17	—	OTPVDD08	—	—	—	—	—	—	—	—	—
V18	—	VSS	—	—	—	—	—	—	—	—	—
V19	—	PCIE_VDD08A_L0	—	—	—	—	—	—	—	—	—
V20	—	VSS	—	—	—	—	—	—	—	—	—
V21	—	VSS	—	—	—	—	—	—	—	—	—
V22	VDD33	—	P35_3	—	GTADSM08_0	SPI_SSL32 / SPI_MOSI1	MCLK91	—	ADTRG0#	—	SI09# / HDSL11_CLK1
V23	VDD1833_3	—	P34_0	A22	GTADSM03_0 / GTIOC03_0A	ETH3_RXCLK / SPI_MOSI2	—	—	—	—	ENCIFDO06 / TXDE06 / HDSL10_SMPL
V24	VDD33	—	P35_5	—	GTADSM09_0	RXD4/SCL4/MISO4 / SPI_RSPCK1	MCLK92	—	—	—	TST_OUT10 / HDSL11_MISO1
V25	VDD33	—	P35_0	DACK	GTADSM06_1	ETH3_RXER / SPI_MISO3	—	—	—	—	SI08# / HDSL10_MOSI2

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (17 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
V26	—	VSS	—	—	—	—	—	—	—	—	—
V27	—	XTAL	—	—	—	—	—	—	—	—	—
W1	—	VSS	—	—	—	—	—	—	—	—	—
W2	—	—	—	—	—	—	—	—	DDR_DQB4	—	—
W3	—	—	—	—	—	—	—	—	DDR_DQB7	—	—
W4	—	—	—	—	—	—	—	—	DDR_DMIB0	—	—
W5	—	—	—	—	—	—	—	—	DDR_DQSB_C 0	—	—
W6	—	VSS	—	—	—	—	—	—	—	—	—
W7	—	VSS	—	—	—	—	—	—	—	—	—
W8	—	VSS	—	—	—	—	—	—	—	—	—
W9	—	VDD1833_4	—	—	—	—	—	—	—	—	—
W10	—	VDD33	—	—	—	—	—	—	—	—	—
W11	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
W12	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
W13	—	VDD08_PLL1	—	—	—	—	—	—	—	—	—
W14	—	VDD08_PLL4	—	—	—	—	—	—	—	—	—
W15	—	VSS	—	—	—	—	—	—	—	—	—
W16	—	VSS	—	—	—	—	—	—	—	—	—
W17	—	OTPVDD18	—	—	—	—	—	—	—	—	—
W18	—	VSS	—	—	—	—	—	—	—	—	—
W19	—	PCIE_VDD08A _L0	—	—	—	—	—	—	—	—	—
W20	—	VSS	—	—	—	—	—	—	—	—	—
W21	—	VSS	—	—	—	—	—	—	—	—	—
W22	—	VSS	—	—	—	—	—	—	—	—	—
W23	VDD33	IRQ14	P34_7	DREQ	GTADSM06_0	ETH3_TXER / ESC_RESETOUT# / SPI_MOSI3	—	—	—	—	TST_OUT08 / HDSL10_MISO2
W24	VDD33	—	P35_4	—	GTADSM08_1	SPI_SSL33 / SPI_SSL11	MDAT91	—	ADTRG1#	—	DUEI10 / HDSL11_SEL1
W25	VDD33	—	P35_2	—	GTADSM07_1	ETH3_COL / SPI_SSL31 / SPI_SSL10	MDAT90	—	ADTRG2#	—	TST_OUT09 / HDSL11_SMPL
W26	—	VSS	—	—	—	—	—	—	—	—	—
W27	—	EXTAL	—	—	—	—	—	—	—	—	—
Y1	—	—	—	—	—	—	—	—	DDR_DQB6	—	—
Y2	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
Y3	—	—	—	—	—	—	—	—	DDR_DQB5	—	—
Y4	—	VSS	—	—	—	—	—	—	—	—	—
Y5	—	VSS	—	—	—	—	—	—	—	—	—
Y6	—	VSS	—	—	—	—	—	—	—	—	—
Y7	—	VSS	—	—	—	—	—	—	—	—	—
Y8	—	VSS	—	—	—	—	—	—	—	—	—
Y9	—	VSS	—	—	—	—	—	—	—	—	—
Y10	—	VSS	—	—	—	—	—	—	—	—	—
Y11	—	VSS	—	—	—	—	—	—	—	—	—
Y12	—	VDD33	—	—	—	—	—	—	—	—	—
Y13	—	VDD33	—	—	—	—	—	—	—	—	—
Y14	—	VDD1833_5	—	—	—	—	—	—	—	—	—
Y15	—	VDD1833_5	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (18 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
Y16	—	VSS	—	—	—	—	—	—	—	—	—
Y17	—	USB_USVDD18	—	—	—	—	—	—	—	—	—
Y18	—	USB_USVDD33	—	—	—	—	—	—	—	—	—
Y19	—	PCIE_VDD08A_L1	—	—	—	—	—	—	—	—	—
Y20	—	PCIE_VDD18A_L1	—	—	—	—	—	—	—	—	—
Y21	—	PCIE_VDD18A_L0	—	—	—	—	—	—	—	—	—
Y22	—	VSS	—	—	—	—	—	—	—	—	—
Y23	—	VSS	—	—	—	—	—	—	—	—	—
Y24	—	VSS	—	—	—	—	—	—	—	—	—
Y25	—	VSS	—	—	—	—	—	—	—	—	—
Y26	—	VSS	—	—	—	—	—	—	—	—	—
Y27	—	VSS	—	—	—	—	—	—	—	—	—
AA1	—	—	—	—	—	—	—	—	DDR_DQB8	—	—
AA2	—	VSS	—	—	—	—	—	—	—	—	—
AA3	—	—	—	—	—	—	—	—	DDR_DQB15	—	—
AA4	—	VSS	—	—	—	—	—	—	—	—	—
AA5	—	—	—	—	—	—	—	—	DDR_DQSB_T1	—	—
AA6	—	VSS	—	—	—	—	—	—	—	—	—
AA7	VDD1833_4	IRQ11	P06_5	—	GTETRGC	IIC_SDA1 / XSPI0_IO7	—	—	—	—	HDSL05_SEL1
AA8	VDD1833_4	IRQ3	P05_1	—	—	XSPI0_CKP	—	—	—	—	DUEI06 / HDSL04_SMPL
AA9	VDD1833_4	IRQ4	P05_2	—	—	IIC_SCL2 / XSPI0_CKN	—	—	—	—	TST_OUT06 / HDSL04_CLK1
AA10	VDD33	IRQ2	P05_0	—	MTIOC6C / MTIOC0B / GTIOC03_4B	IIC_SDA1	—	—	—	—	ENCIFDI03 / RXDE03 / HDSL04_LINK
AA11	—	VSS	—	—	—	—	—	—	—	—	—
AA12	VDD33	—	P04_2	—	MTIOC7C / GTIOC03_1B / CMTW0_TOC1	—	—	—	—	—	DUEI05 / HDSL03_MISO1
AA13	VDD1833_5	IRQ9	P02_2	—	MTIOC6A / MTIOC1A / GTIOC01_4A	ETH3_CRS / IIC_SDA2 / XSPI1_IO6	MCLK22	—	USB_VBUSEN	—	ENCIFDO01 / TXDE01 / HDSL01_MISO2
AA14	—	VSS	—	—	—	—	—	—	—	—	—
AA15	—	VSS	—	—	—	—	—	—	—	—	—
AA16	—	USB_USDVDD	—	—	—	—	—	—	—	—	—
AA17	—	USB_USVDD18	—	—	—	—	—	—	—	—	—
AA18	—	USB_USVDD33	—	—	—	—	—	—	—	—	—
AA19	—	PCIE_VDD08A_L1	—	—	—	—	—	—	—	—	—
AA20	—	PCIE_VDD18A_L1	—	—	—	—	—	—	—	—	—
AA21	—	PCIE_VDD18A_L0	—	—	—	—	—	—	—	—	—
AA22	—	AVSS_ADC0	—	—	—	—	—	—	—	—	—
AA23	—	AVDD_ADC0	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (19 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AA24	—	AVSSIO_ADC0	—	—	—	—	—	—	—	—	—
AA25	—	AVSSIO_ADC0	—	—	—	—	—	—	—	—	—
AA26	—	—	—	—	—	—	—	—	AN002	—	—
AA27	—	—	—	—	—	—	—	—	AN000	—	—
AB1	—	—	—	—	—	—	—	—	DDR_DQB14	—	—
AB2	—	—	—	—	—	—	—	—	DDR_DQB9	—	—
AB3	—	—	—	—	—	—	—	—	DDR_DMIB1	—	—
AB4	—	—	—	—	—	—	—	—	DDR_DQB10	—	—
AB5	—	—	—	—	—	—	—	—	DDR_DQSB_C1	—	—
AB6	VDD33	BSCANP	—	—	—	—	—	—	—	—	—
AB7	VDD1833_4	IRQ9	P06_3	—	GTETRGA	IIC_SDA0 / XSPI0_IO5	—	—	—	—	TST_OUT09 / HDSL05_SMPL
AB8	VDD1833_4	IRQ10	P06_4	—	GTETRGB	IIC_SCL1 / XSPI0_IO6	—	—	—	—	SI09# / HDSL05_CLK1
AB9	VDD1833_4	—	P07_7	—	—	IIC_SCL0 / XSPI0_WP0#	MCLK10	—	—	—	ENCIFDO05 / TXDE05 / HDSL06_CLK1
AB10	VDD33	IRQ14	P03_4	D12	MTCLKB / MTIOC8D / GTIOC02_3B / GTADSM09_1 / CMTW1_TOC1 / RTCAT1HZ	IIC_SDA1	—	—	—	—	ENCIFOE02 / DEE02 / HDSL02_MISO2
AB11	VDD33	IRQ13	P03_3	D11	MTCLKA / MTIOC8C / GTIOC02_3A / GTADSM09_0 / CMTW1_TIC1	IIC_SCL1	—	—	—	—	ENCIFCK02 / SCKE02 / HDSL02_SEL2
AB12	VDD33	—	P03_7	—	MTIOC6B / MTIOC1B / GTIOC03_0A / CMTW0_TIC0	—	—	—	—	—	DUEI04 / HDSL03_SMPL
AB13	VDD1833_5	IRQ8	P02_1	—	MTCLKD / MTIOC0D / GTIOC01_3B	ETH3_RXER / IIC_SCL2 / XSPI1_IO5	MDAT21	—	—	—	ENCIFOE01 / DEE01 / HDSL01_SEL2
AB14	VDD1833_5	—	P01_3	—	MTIOC6D / MTIC5U / GTIOC01_0B / GTIOC04_0B	XSPI1_DS	—	—	—	—	TST_OUT02 / HDSL01_SMPL
AB15	VDD33	—	P00_5	—	MTIOC4D / MTIOC8C / GTIOC00_2B	—	—	—	USB_VBUSEN	—	SI01# / HDSL00_MOSI1
AB16	—	USB_USDVDD	—	—	—	—	—	—	—	—	—
AB17	—	VSS	—	—	—	—	—	—	—	—	—
AB18	—	VSS	—	—	—	—	—	—	—	—	—
AB19	—	VSS	—	—	—	—	—	—	—	—	—
AB20	—	VSS	—	—	—	—	—	—	—	—	—
AB21	—	PCIE_VDD18A_CMN	—	—	—	—	—	—	—	—	—
AB22	—	AVSS_ADC1	—	—	—	—	—	—	—	—	—
AB23	—	AVDD_ADC1	—	—	—	—	—	—	—	—	—
AB24	—	AVDDIO_ADC0	—	—	—	—	—	—	—	—	—
AB25	—	AVDDREF_ADC0	—	—	—	—	—	—	—	—	—
AB26	—	—	—	—	—	—	—	—	AN001	—	—
AB27	—	—	—	—	—	—	—	—	AN003	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (20 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AC1	—	—	—	—	—	—	—	—	DDR_DQB12	—	—
AC2	—	VSS	—	—	—	—	—	—	—	—	—
AC3	—	—	—	—	—	—	—	—	DDR_DQB13	—	—
AC4	—	—	—	—	—	—	—	—	DDR_DQB11	—	—
AC5	—	VSS	—	—	—	—	—	—	—	—	—
AC6	VDD1833_4	—	P06_1	—	—	XSPI0_IO3	—	—	—	—	SI08# / HDSL04_MOSI2
AC7	VDD1833_4	—	P07_6	—	—	IIC_SDA2 / XSPI0_ECS1#	MDAT02	—	—	—	ENCIFOE05 / DEE05 / HDSL06_SMPL
AC8	VDD1833_4	—	P07_4	—	—	IIC_SDA1 / XSPI0_INT1#	MDAT01	—	—	—	ENCIFDI04 / ENCIFDI12 / RXDE04 / RXDE08 / HDSL05_MOSI2
AC9	VDD33	IRQ12	P03_2	D10	MTIOC4D / MTIOC1A / GTIOC02_2B / GTADSM08_1 / CMTW1_TOC0	—	—	—	—	—	ENCIFDI02 / RXDE02 / HDSL02_CLK2
AC10	VDD33	—	P03_1	D9	MTIOC4B / MTIOC1B / GTIOC02_2A / GTADSM08_0 / CMTW1_TIC0	—	—	—	—	—	ENCIFDO02 / TXDE02 / HDSL02_MOSI1
AC11	VDD33	IRQ1	P04_7	—	MTIOC6A / MTIOC0A / GTIOC03_4A	IIC_SCL1	—	—	—	—	ENCIFDO03 / TXDE03 / HDSL03_MOSI2
AC12	VDD33	IRQ15	P03_5	—	MTIOC3A / MTIC5W / GTIOC02_4A	IIC_SCL2	—	—	—	—	ENCIFDO02 / TXDE02 / HDSL02_MOSI2
AC13	VDD1833_5	—	P01_7	—	MTIOC7D / MTIOC0B / GTIOC01_2B / GTIOC04_2B	XSPI1_IO3	—	—	—	—	SI03# / HDSL01_MOSI1
AC14	VDD1833_5	IRQ7	P02_0	—	MTCLKC / MTIOC0C / GTIOC01_3A	ETH3_TXER / IIC_SDA1 / XSPI1_IO4	MCLK21	—	—	—	ENCIFCK01 / SCKE01 / HDSL01_CLK2
AC15	VDD33	IRQ1	P00_2	D2	MTIOC4A / GTIOC00_1A	ETH3_CRS	—	—	ADTRG0# / USB_EXICEN	—	SI00# / HDSL00_CLK1
AC16	—	VSS	—	—	—	—	—	—	—	—	—
AC17	—	—	—	—	—	—	—	—	USB_TXRTUNE	—	—
AC18	—	VSS	—	—	—	—	—	—	—	—	—
AC19	—	—	—	—	—	—	—	—	PCIE_REFCLK_N1	—	—
AC20	—	—	—	—	—	—	—	—	PCIE_REFCLK_P0	—	—
AC21	—	PCIE_VDD18A_CMN	—	—	—	—	—	—	—	—	—
AC22	—	AVDD_ADC2	—	—	—	—	—	—	—	—	—
AC23	—	AVDDIO_ADC2	—	—	—	—	—	—	—	—	—
AC24	—	AVDDIO_ADC1	—	—	—	—	—	—	—	—	—
AC25	—	AVDDREF_ADC1	—	—	—	—	—	—	—	—	—
AC26	—	—	—	—	—	—	—	—	AN103	—	—
AC27	—	—	—	—	—	—	—	—	AN100	—	—
AD1	VDD33	MDX	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (21 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AD2	VDD33	SEI / CKIO	P08_6	—	GTIOC08_3A / GTETRGSB	IIC_SDA1 / SD1_IOVS	MDAT02 / MCLK11	—	—	—	DUEI11 / HDSL06_MOSI2
AD3	VDD33	TCK	P08_3	—	—	—	—	—	—	—	SI10# / HDSL06_CLK2
AD4	VDD33	RES#	—	—	—	—	—	—	—	—	—
AD5	VDD33	TDI	P08_2	—	—	—	—	—	—	—	TST_OUT10 / HDSL06_MOSI1
AD6	VDD1833_4	—	P05_6	—	—	XSPI0_IO0	—	—	—	—	SI07# / HDSL04_CLK2
AD7	VDD1833_4	—	P08_0	—	RTCAT1HZ	IIC_SDA0 / XSPI0_WP1#	MDAT10	—	—	MBX_HINT#	ENCIFDI05 / RXDE05 / HDSL06_SEL1
AD8	—	VSS	—	—	—	—	—	—	—	—	—
AD9	VDD33	—	P02_6	D6	MTIOC3D / MTIOC8B / GTIOC02_0B / GTADSM06_1 / CMTW0_TOC0	SD0_IOVS	MDAT00	—	—	—	HDSL02_CLK1 / POUTB
AD10	VDD33	IRQ0	P04_6	—	MTCLKD / MTIOC0D / GTIOC03_3B / CMTW1_TOC1	IIC_SDA0	—	—	ADTRG2#	MBX_HINT#	ENCIFOE03 / DEE03 / HDSL03_MISO2
AD11	VDD33	—	P02_5	D5	MTIOC3B / MTIOC8A / GTIOC02_0A / GTADSM06_0 / CMTW0_TIC0	IIC_SCL0 / SD0_PWEN	MCLK00	—	—	—	HDSL02_SMPL / POUTA
AD12	—	VSS	—	—	—	—	—	—	—	—	—
AD13	VDD1833_5	—	P01_6	—	MTIOC7B / MTIOC0A / GTIOC01_2A / GTIOC04_2A	XSPI1_IO2	—	—	—	—	TST_OUT03 / HDSL01_MISO1
AD14	VDD1833_5	—	P01_2	—	MTIOC6B / MTIOC8B / GTIOC01_0A / GTIOC04_0A	XSPI1_CS1#	—	—	—	—	DUEI02 / HDSL01_LINK
AD15	VDD33	IRQ0	P00_1	D1	MTIOC3D / GTIOC00_0B	ETH3_RXER	—	—	USB_OVRCUR	—	TST_OUT00 / HDSL00_SMPL
AD16	—	—	—	—	—	—	—	—	USB_VUBUSIN	—	—
AD17	—	—	—	—	—	—	—	—	USB_OTG_ID	—	—
AD18	—	VSS	—	—	—	—	—	—	—	—	—
AD19	—	—	—	—	—	—	—	—	PCIE_REFCLK_P1	—	—
AD20	—	—	—	—	—	—	—	—	PCIE_REFCLK_N0	—	—
AD21	—	VSS	—	—	—	—	—	—	—	—	—
AD22	—	AVSS_ADC2	—	—	—	—	—	—	—	—	—
AD23	—	AVSSIO_ADC2	—	—	—	—	—	—	—	—	—
AD24	—	AVSSIO_ADC1	—	—	—	—	—	—	—	—	—
AD25	—	AVSSIO_ADC1	—	—	—	—	—	—	—	—	—
AD26	—	—	—	—	—	—	—	—	AN102	—	—
AD27	—	—	—	—	—	—	—	—	AN101	—	—
AE1	VDD33	—	P09_0	—	—	IIC_SDA2	MCLK12	—	—	—	SI11# / HDSL07_SMPL
AE2	VDD33	—	P09_2	—	—	—	MCLK20	—	—	—	TST_OUT12 / HDSL07_SEL1

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (22 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AE3	VDD33	IRQ8 / RSTOUT#	P08_5	—	GTETRGSA	IIC_SCL1 / SD1_PWEN	MCLK02	—	—	—	HDSL06_MISO2
AE4	VDD33	TDO	P08_4	—	—	—	—	—	—	—	HDSL06_SEL2
AE5	VDD1833_4	—	P06_0	—	—	XSPI0_IO2	—	—	—	—	TST_OUT08 / HDSL04_MISO2
AE6	VDD1833_4	IRQ8	P06_2	—	—	IIC_SCL0 / XSPI0_IO4	—	—	—	—	DUEI09 / HDSL05_LINK
AE7	VDD1833_4	—	P05_7	—	—	XSPI0_IO1	—	—	—	—	DUEI08 / HDSL04_SEL2
AE8	VDD1833_4	—	P07_3	—	POE11#	IIC_SCL1 / XSPI0_INT0#	MCLK01	—	—	—	ENCIFDO04 / ENCIFDO12 / TXDE04 / TXDE08 / HDSL05_MISO2
AE9	VDD33	—	P02_7	D7	MTIOC4A / MTIC5U / GTIOC02_1A / GTADSM07_0 / CMTW0_TIC1	—	MCLK01	—	—	—	HDSL02_SEL1 / POUTZ
AE10	VDD33	—	P03_0	D8	MTIOC4C / MTIC5V / GTIOC02_1B / GTADSM07_1 / CMTW0_TOC1	—	MDAT01	—	—	—	HDSL02_MISO1
AE11	VDD33	—	P04_0	—	MTIOC6D / GTIOC03_0B / CMTW0_TOC0	—	—	—	—	—	TST_OUT04 / HDSL03_CLK1
AE12	VDD1833_5	IRQ11	P02_4	—	POE0#	IIC_SDA0	MDAT20	—	USB_EXICEN	MBX_HINT#	HDSL02_LINK
AE13	VDD1833_5	—	P01_5	—	MTIOC7C / MTIC5W / GTIOC01_1B / GTIOC04_1B	XSPI1_IO1	—	—	—	—	DUEI03 / HDSL01_SEL1
AE14	VDD33	IRQ5	P00_7	—	MTCLKB / MTIOC1B / GTIOC00_3B	IIC_SDA0	—	—	USB_EXICEN	—	ENCIFOE00 / ENCIFOE04 / DEE00 / DEE04 / HDSL00_SEL2
AE15	VDD33	SEI	P00_0	D0	MTIOC3B / GTIOC00_0A	ETH3_TXER	—	—	USB_VBUSEN	—	DUEI00 / HDSL00_LINK
AE16	—	VSS	—	—	—	—	—	—	—	—	—
AE17	—	VSS	—	—	—	—	—	—	—	—	—
AE18	—	VSS	—	—	—	—	—	—	—	—	—
AE19	—	VSS	—	—	—	—	—	—	—	—	—
AE20	—	VSS	—	—	—	—	—	—	—	—	—
AE21	—	VSS	—	—	—	—	—	—	—	—	—
AE22	—	VSS	—	—	—	—	—	—	—	—	—
AE23	—	VSS	—	—	—	—	—	—	—	—	—
AE24	—	VSS	—	—	—	—	—	—	—	—	—
AE25	—	AVSSIO_ADC2	—	—	—	—	—	—	—	—	—
AE26	—	—	—	—	—	—	—	—	AN202	—	—
AE27	—	—	—	—	—	—	—	—	AN201	—	—
AF1	VDD33	—	P09_3	—	—	—	MDAT20	—	—	—	SI12# / HDSL07_MISO1
AF2	VDD33	IRQ0	P08_7	A0	GTIOC08_3B	IIC_SCL2 / IIC_SCL1	MDAT11	—	—	—	TST_OUT11 / HDSL07_LINK
AF3	VDD33	TRST#	—	—	—	—	—	—	—	—	—

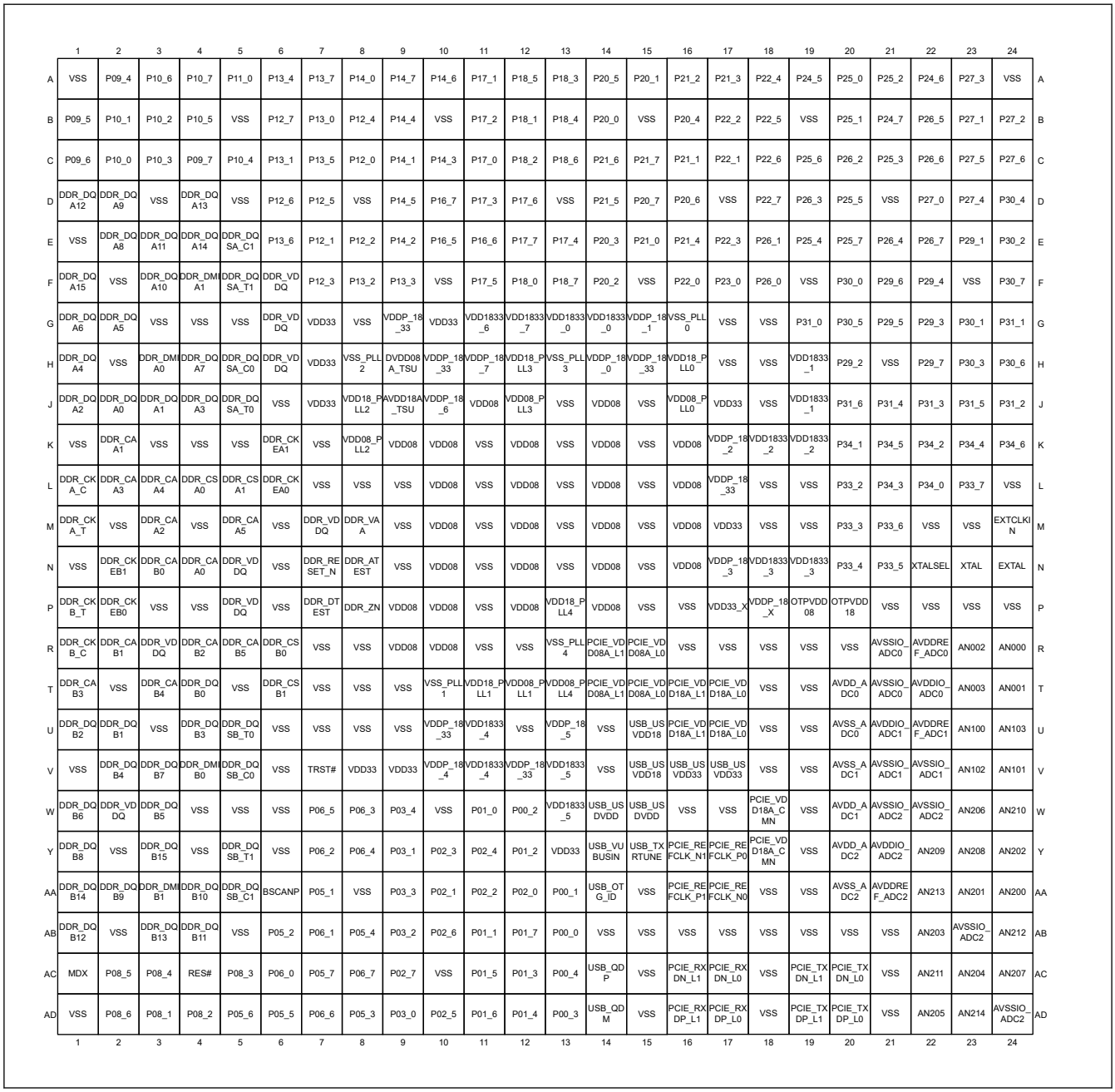
Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (23 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AF4	VDD1833_4	IRQ14	P07_1	—	POE8#	IIC_SCL0 / XSPI0_RSTO0#	MCLK00	—	—	—	ENCIFCK04 / ENCIFCK12 / SCKE04 / SCKE08 / HDSL05_CLK2
AF5	VDD1833_4	—	P05_5	—	—	XSPI0_DS	—	—	—	—	TST_OUT07 / HDSL04_MOSI1
AF6	—	VSS	—	—	—	—	—	—	—	—	—
AF7	VDD1833_4	IRQ12	P06_7	—	POE4# / GTETRGD	GMAC1_MDC / IIC_SCL2	—	—	—	—	HDSL05_MISO1
AF8	VDD1833_4	IRQ13	P07_0	—	—	GMAC1_MDIO / IIC_SDA2 / XSPI0_RESET1#	—	—	—	—	HDSL05_MOSI1
AF9	VDD33	SEI	P04_5	—	MTCLKC / MTIOC0C / GTIOC03_3A / CMTW1_TIC1	IIC_SCL0	—	—	ADTRG1#	—	ENCIFCK03 / SCKE03 / HDSL03_SEL2
AF10	—	VSS	—	—	—	—	—	—	—	—	—
AF11	VDD33	—	P04_1	—	MTIOC7A / GTIOC03_1A / CMTW0_TIC1	—	—	—	—	—	SI04# / HDSL03_SEL1
AF12	VDD1833_5	IRQ10	P02_3	—	MTIOC6C / MTIOC1B / GTIOC01_4B	ETH3_COL / IIC_SCL0 / IIC_SCL2 / XSPI1_IO7	MDAT22	—	USB_OVRCUR	—	ENCIFDI01 / RXDE01 / HDSL01_MOSI2
AF13	VDD1833_5	IRQ6	P01_0	—	MTIOC3A / MTIOC1A / GTIOC00_4A / GTIOC00_2B	IIC_SCL1 / XSPI1_CKP	—	—	—	—	ENCIFDO00 / ENCIFDO04 / TXDE00 / TXDE04 / HDSL00_MISO2
AF14	—	VSS	—	—	—	—	—	—	—	—	—
AF15	VDD33	IRQ3	P00_4	D4	MTIOC4B / GTIOC00_2A	—	—	—	ADTRG2#	—	TST_OUT01 / HDSL00_MISO1
AF16	—	VSS	—	—	—	—	—	—	—	—	—
AF17	—	—	—	—	—	—	—	—	USB_QDP	—	—
AF18	—	VSS	—	—	—	—	—	—	—	—	—
AF19	—	—	—	—	—	—	—	—	PCIE_RXDN_L1	—	—
AF20	—	—	—	—	—	—	—	—	PCIE_RXDN_L0	—	—
AF21	—	VSS	—	—	—	—	—	—	—	—	—
AF22	—	—	—	—	—	—	—	—	PCIE_TXDN_L1	—	—
AF23	—	—	—	—	—	—	—	—	PCIE_TXDN_L0	—	—
AF24	—	VSS	—	—	—	—	—	—	—	—	—
AF25	—	AVDDREF_ADC2	—	—	—	—	—	—	—	—	—
AF26	—	—	—	—	—	—	—	—	AN204	—	—
AF27	—	—	—	—	—	—	—	—	AN200	—	—
AG1	—	VSS	—	—	—	—	—	—	—	—	—
AG2	VDD33	—	P09_1	—	—	—	MDAT12	—	—	—	DUEI12 / HDSL07_CLK1
AG3	VDD33	TMS	P08_1	—	—	—	—	—	—	—	DUEI10 / HDSL06_MISO1
AG4	VDD1833_4	IRQ5	P05_3	—	—	XSPI0_CS0#	—	—	—	—	SI06# / HDSL04_SEL1
AG5	VDD1833_4	IRQ15	P07_2	—	POE10#	IIC_SDA0 / XSPI0_RSTO1#	MDAT00	—	—	—	ENCIFOE04 / ENCIFOE12 / DEE04 / DEE08 / HDSL05_SEL2

Table 1.20 List of pins and pin functions (RZ/T2H 729-pin FCBGA) (24 of 24)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AG6	VDD1833_4	—	P07_5	—	—	IIC_SCL2 / XSPI0_ECS0#	MCLK02	—	—	—	ENCIFCK05 / SCKE05 / HDSL06_LINK
AG7	VDD1833_4	IRQ6	P05_4	—	—	IIC_SDA2 / XSPI0_CS1#	—	—	—	—	DUEI07 / HDSL04_MISO1
AG8	VDD1833_4	MDD	P06_6	—	—	XSPI0_RESET0#	—	—	—	—	—
AG9	VDD33	—	P03_6	—	MTIOC3C / MTIOC1A / GTIOC02_4B	IIC_SDA2	—	—	—	—	ENCIFDI02 / RXDE02 / HDSL03_LINK
AG10	VDD33	—	P04_3	—	MTIOC7B / GTIOC03_2A / CMTW1_TIC0	—	—	—	—	—	TST_OUT05 / HDSL03_MOSI1
AG11	VDD33	—	P04_4	—	MTIOC7D / GTIOC03_2B / CMTW1_TOC 0	—	—	—	ADTRG0#	—	SI05# / HDSL03_CLK2
AG12	VDD1833_5	—	P01_1	—	MTIOC3C / MTIOC8A / GTIOC00_4B	XSPI1_CS0#	MCLK20	—	—	—	ENCIFDI00 / ENCIFDI04 / RXDE00 / RXDE04 / HDSL00_MOSI2
AG13	VDD1833_5	—	P01_4	—	MTIOC7A / MTIC5V / GTIOC01_1A / GTIOC04_1A	XSPI1_IO0	—	—	—	—	SI02# / HDSL01_CLK1
AG14	VDD33	IRQ4	P00_6	—	MTCLKA / MTIOC8D / GTIOC00_3A	IIC_SCL0	—	—	USB_OVRCU R	—	ENCIFCK00 / ENCIFCK04 / SCKE00 / SCKE04 / HDSL00_CLK2
AG15	VDD33	IRQ2	P00_3	D3	MTIOC4C / GTIOC00_1B	ETH3_COL	—	—	ADTRG1#	—	DUEI01 / HDSL00_SEL1
AG16	—	VSS	—	—	—	—	—	—	—	—	—
AG17	—	—	—	—	—	—	—	—	USB_QDM	—	—
AG18	—	VSS	—	—	—	—	—	—	—	—	—
AG19	—	—	—	—	—	—	—	—	PCIE_RXDP_L 1	—	—
AG20	—	—	—	—	—	—	—	—	PCIE_RXDP_L 0	—	—
AG21	—	VSS	—	—	—	—	—	—	—	—	—
AG22	—	—	—	—	—	—	—	—	PCIE_TXDP_L 1	—	—
AG23	—	—	—	—	—	—	—	—	PCIE_TXDP_L 0	—	—
AG24	—	VSS	—	—	—	—	—	—	—	—	—
AG25	—	—	—	—	—	—	—	—	AN205	—	—
AG26	—	—	—	—	—	—	—	—	AN203	—	—
AG27	—	VSS	—	—	—	—	—	—	—	—	—

1.7 RZ/N2H FCBGA 576 Pin Assignments



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	VSS	P09_4	P10_6	P10_7	P11_0	P13_4	P13_7	P14_0	P14_7	P14_6	P17_1	P18_5	P18_3	P20_5	P20_1	P21_2	P21_3	P22_4	P24_5	P25_0	P25_2	P24_6	P27_3	VSS	A
B	P09_5	P10_1	P10_2	P10_5	VSS	P12_7	P13_0	P12_4	P14_4	VSS	P17_2	P18_1	P18_4	P20_0	VSS	P20_4	P22_2	P22_5	VSS	P25_1	P24_7	P26_5	P27_1	P27_2	B
C	P09_6	P10_0	P10_3	P09_7	P10_4	P13_1	P13_5	P12_0	P14_1	P14_3	P17_0	P18_2	P18_6	P21_6	P21_7	P21_1	P22_1	P22_6	P25_6	P26_2	P25_3	P26_6	P27_5	P27_6	C
D	DDR_DQA12	DDR_DQA9	VSS	DDR_DQA13	VSS	P12_6	P12_5	VSS	P14_5	P16_7	P17_3	P17_6	VSS	P21_5	P20_7	P20_6	VSS	P22_7	P26_3	P25_5	VSS	P27_0	P27_4	P30_4	D
E	VSS	DDR_DQA8	DDR_DQA11	DDR_DQA14	DDR_DQSA_C1	P13_6	P12_1	P12_2	P14_2	P16_5	P16_6	P17_7	P17_4	P20_3	P21_0	P21_4	P22_3	P26_1	P25_4	P25_7	P26_4	P26_7	P29_1	P30_2	E
F	DDR_DQA15	VSS	DDR_DQA10	DDR_DMIA1	DDR_DQSA_T1	DDR_VDDQ	P12_3	P13_2	P13_3	VSS	P17_5	P18_0	P18_7	P20_2	VSS	P22_0	P23_0	P26_0	VSS	P30_0	P29_6	P29_4	VSS	P30_7	F
G	DDR_DQA6	DDR_DQA5	VSS	VSS	VSS	DDR_VDDQ	VDD33	VSS	VDDP_18_33	VDD33	VDD1833_6	VDD1833_7	VDD1833_0	VDD1833_0	VDDP_18_1	VSS_PLL0	VSS	VSS	P31_0	P30_5	P29_5	P29_3	P30_1	P31_1	G
H	DDR_DQA4	VSS	DDR_DMIA0	DDR_DQA7	DDR_DQSA_C0	DDR_VDDQ	VDD33	VSS_PLL2	DVDD08A_TSU	VDDP_18_33	VDDP_18_7	VDD18_PLL3	VSS_PLL3	VDDP_18_0	VDDP_18_33	VDD18_PLL0	VSS	VSS	VDD1833_1	P29_2	VSS	P29_7	P30_3	P30_6	H
J	DDR_DQA2	DDR_DQA0	DDR_DQA1	DDR_DQA3	DDR_DQSA_T0	VSS	VDD33	VDD18_PLL2	AVDD18A_TSU	VDDP_18_6	VDD08	VDD08_PLL3	VSS	VDD08	VSS	VDD08_PLL0	VDD33	VSS	VDD1833_1	P31_6	P31_4	P31_3	P31_5	P31_2	J
K	VSS	DDR_CAA1	VSS	VSS	VSS	DDR_CKEA1	VSS	VDD08_PLL2	VDD08	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VDDP_18_2	VDD1833_2	VDD1833_2	P34_1	P34_5	P34_2	P34_4	P34_6	K
L	DDR_CKA_C	DDR_CAA3	DDR_CAA4	DDR_CSA0	DDR_CSA1	DDR_CKEA0	VSS	VSS	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VDDP_18_33	VSS	VSS	P33_2	P34_3	P34_0	P33_7	VSS	L
M	DDR_CKA_T	VSS	DDR_CAA2	VSS	DDR_CAA5	VSS	DDR_VDDQ	DDR_VAA	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VDD33	VSS	VSS	P33_3	P33_6	VSS	VSS	EXTCLKIN	M
N	VSS	DDR_CKEB1	DDR_CAB0	DDR_CAA0	DDR_VDDQ	VSS	DDR_RESET_N	DDR_ATEST	VSS	VDD08	VSS	VDD08	VSS	VDD08	VSS	VDD08	VDDP_18_3	VDD1833_3	VDD1833_3	P33_4	P33_5	XTALSEL	XTAL	EXTAL	N
P	DDR_CKB_T	DDR_CKEB0	VSS	VSS	DDR_VDDQ	VSS	DDR_DTEST	DDR_ZN	VDD08	VDD08	VSS	VDD08	VDD18_PLL4	VDD08	VSS	VSS	VDD33_X	VDDP_18_X	OTPVDD08	OTPVDD18	VSS	VSS	VSS	VSS	P
R	DDR_CKB_C	DDR_CAB1	DDR_VDDQ	DDR_CAB2	DDR_CAB5	DDR_CSB0	VSS	VSS	VDD08	VDD08	VSS	VSS	VSS_PLL4	PCIE_VDD08A_L1	PCIE_VDD08A_L0	VSS	VSS	VSS	VSS	VSS	AVSSIO_ADC0	AVDDREF_ADC0	AN002	AN000	R
T	DDR_CAB3	VSS	DDR_CAB4	DDR_DQB0	VSS	DDR_CSB1	VSS	VSS	VSS	VSS_PLL1	VDD18_PLL1	VDD08_PLL1	VDD08_PLL4	PCIE_VDD08A_L1	PCIE_VDD08A_L0	PCIE_VDD18A_L1	PCIE_VDD18A_L0	VSS	VSS	AVDD_ADC0	AVSSIO_ADC0	AVDDIO_ADC0	AN003	AN001	T
U	DDR_DQB2	DDR_DQB1	VSS	DDR_DQB3	DDR_DQSB_T0	VSS	VSS	VSS	VSS	VDDP_18_33	VDD1833_4	VSS	VDDP_18_5	VSS	USB_USVDD18	PCIE_VDD18A_L1	PCIE_VDD18A_L0	VSS	VSS	AVSS_ADC0	AVDDIO_ADC1	AVDDREF_ADC1	AN100	AN103	U
V	VSS	DDR_DQB4	DDR_DQB7	DDR_DMIB0	DDR_DQSB_C0	VSS	TRST#	VDD33	VDD33	VDDP_18_4	VDD1833_4	VDDP_18_33	VDD1833_5	VSS	USB_USVDD18	USB_USVDD33	USB_USVDD33	VSS	VSS	AVSS_ADC1	AVSSIO_ADC1	AVSSIO_ADC1	AN102	AN101	V
W	DDR_DQB6	DDR_VDDQ	DDR_DQB5	VSS	VSS	VSS	P06_5	P06_3	P03_4	VSS	P01_0	P00_2	VDD1833_5	USB_USDVDD	USB_USDVDD	VSS	VSS	PCIE_VDD18A_CMN	VSS	AVDD_ADC1	AVSSIO_ADC2	AVSSIO_ADC2	AN206	AN210	W
Y	DDR_DQB8	VSS	DDR_DQB15	VSS	DDR_DQSB_T1	VSS	P06_2	P06_4	P03_1	P02_3	P02_4	P01_2	VDD33	USB_VUBUSIN	USB_TXRTUNE	PCIE_REFCLK_N1	PCIE_REFCLK_P0	PCIE_VDD18A_CMN	VSS	AVDD_ADC2	AVDDIO_ADC2	AN209	AN208	AN202	Y
AA	DDR_DQB14	DDR_DQB9	DDR_DMIB1	DDR_DQB10	DDR_DQSB_C1	BSCANP	P05_1	VSS	P03_3	P02_1	P02_2	P02_0	P00_1	USB_OTG_ID	VSS	PCIE_REFCLK_P1	PCIE_REFCLK_N0	VSS	VSS	AVSS_ADC2	AVDDREF_ADC2	AN213	AN201	AN200	AA
AB	DDR_DQB12	VSS	DDR_DQB13	DDR_DQB11	VSS	P05_2	P06_1	P05_4	P03_2	P02_6	P01_1	P01_7	P00_0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AN203	AVSSIO_ADC2	AN212	AB
AC	MDX	P08_5	P08_4	RES#	P08_3	P06_0	P05_7	P06_7	P02_7	VSS	P01_5	P01_3	P00_4	USB_QDP	VSS	PCIE_RXDN_L1	PCIE_RXDN_L0	VSS	PCIE_TXDN_L1	PCIE_TXDN_L0	VSS	AN211	AN204	AN207	AC
AD	VSS	P08_6	P08_1	P08_2	P05_6	P05_5	P06_6	P05_3	P03_0	P02_5	P01_6	P01_4	P00_3	USB_QDM	VSS	PCIE_RXDP_L1	PCIE_RXDP_L0	VSS	PCIE_TXDP_L1	PCIE_TXDP_L0	VSS	AN205	AN214	AVSSIO_ADC2	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

Figure 1.3 Pin arrangement (RZ/N2H 576-pin FCBGA) (top view)

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (1 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
A1	—	VSS	—	—	—	—	—	—	—	—	—
A2	VDD33	—	P09_4	D13	MTIOC6B / GTIOC04_0A / GTIOC10_0A	—	MCLK70	DISP_CLK	—	—	DUEI13 / HDSL07_MOSI1
A3	VDD33	IRQ0	P10_6	A3	MTIOC0B / GTIOC05_0A	DE0	MCLK21	DISP_DATAR6	—	—	HDSL08_MOSI1 / POUTA
A4	VDD33	IRQ9	P10_7	A4	MTIC5U / GTIOC05_0B / GTIOC00_3A	SCK1	MDAT21	DISP_DATAR7	—	—	HDSL08_CLK2 / POUTB

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (2 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
A5	VDD33	IRQ13	P11_0	A5	GTIOC00_3B	ESC_RESETOUT# / RXD1/SCL1/MISO1	MCLK22	DISP_DATAG0	—	—	HDSL08_SEL2 / POUTZ
A6	VDD1833_6	—	P13_4	D28	GTIOC03_3B	RXD3/SCL3/MISO3 / SPI_SSL31	MCLK40	—	—	—	ENCIFCK13 / SCKE09 / HDSL10_SEL2
A7	VDD1833_6	IRQ14	P13_7	D31	GTIOC06_4A / GTIOC04_3B	CTS3#	MDAT41	—	—	—	ENCIFDI13 / RXDE09 / HDSL11_LINK
A8	VDD1833_6	IRQ5	P14_0	A0	GTIOC06_4B	ETHSW_PTPOUT2 / ESC_SYNC0 / DE3	MCLK42	—	—	—	HDSL11_SMPL
A9	VDD33	IRQ9	P14_7	—	POE11# / GTIOC09_3A / CMTW0_TOC1	ESC_I2CDATA / IIC_SDA0 / SD0_IOVS	MCLK32	—	—	—	SI02# / HDSL11_MISO2
A10	VDD33	IRQ8	P14_6	—	POE10# / GTIOC06_2B / GTIOC09_2B / CMTW0_TIC1	ESC_I2CCLK / DE4 / IIC_SCL0 / SD0_PWEN	—	DISP_DATAG6	—	—	TST_OUT02 / HDSL11_SEL2
A11	VDD1833_7	IRQ13	P17_1	—	GTIOC03_2A	SD1_DATA2	—	—	—	—	DUEI06 / HDSL13_CLK2
A12	VDD33	IRQ2	P18_5	A13	GTIOC07_3B / GTADSM04_1	SS1#/CTS1#/ RTS1# / CANTX1	MDAT11	DISP_DATAB6	—	—	ENCIFOE13 / ENCIFOE14 / DEE09 / DEE10 / HDSL14_MISO2
A13	VDD33	IRQ0	P18_3	A11	GTADSM03_1 / RTCAT1HZ	ETH1_COL / GMAC1_MDIO / RXD1/SCL1/MISO1 / CANTX0 / SD1_IOVS	MDAT10	DISP_DATAB4	—	—	HDSL14_CLK2
A14	VDD1833_0	—	P20_5	—	—	ETH0_TXEN	—	—	—	—	DUEI11 / HDSL00_LINK
A15	VDD1833_0	MDV	P20_1	—	—	ETH0_TXD0	—	—	—	—	—
A16	VDD1833_0	—	P21_2	—	—	ETH0_RXD3 / CANTXDP0	—	—	—	—	SI12# / HDSL00_MOSI1
A17	VDD1833_0	—	P21_3	—	—	ETH0_RXDV	—	—	—	—	DUEI13 / HDSL00_CLK2
A18	VDD33	IRQ6	P22_4	A21	GTETRGD	ETH0_COL / SS5#/ CTS5#/RTS5# / CANTXDP0	—	—	—	—	TST_OUT14 / HDSL01_MOSI1
A19	VDD1833_1	—	P24_5	—	—	ETH1_TXCLK	—	—	—	—	HDSL03_CLK1
A20	VDD1833_1	MD2	P25_0	—	—	ETH1_TXD2 / CANRXDP0	—	—	—	—	—
A21	VDD1833_1	MDW1	P25_2	—	—	ETH1_TXEN	—	—	—	—	—
A22	VDD1833_1	MD0	P24_6	—	—	ETH1_TXD0	—	—	—	—	—
A23	VDD33	—	P27_3	—	MTIOC2A / GTIOC08_3A / GTIOC02_1A	GMAC1_PTPTRG1 / SCK0 / CANRXDP1 / SPI_MOSI0	—	—	—	HSPI_IO1	ENCIFCK14 / SCKE10 / HDSL04_MISO2
A24	—	VSS	—	—	—	—	—	—	—	—	—
B1	VDD33	—	P09_5	D14	MTIOC6D / GTIOC04_0B / GTIOC10_0B	—	MDAT70	DISP_HSYNC	—	—	TST_OUT13 / HDSL07_CLK2
B2	VDD33	IRQ7	P10_1	WAIT#	MTIOC7D / GTIOC04_2B / GTIOC10_2B	SCK0	MDAT72	DISP_DATAR1	—	—	SI14# / HDSL08_LINK
B3	VDD33	IRQ1	P10_2	CS0#	MTCLKC / MTIOC2A / GTIOC04_3A / GTIOC10_3A	RXD0/SCL0/MISO0	MCLK10 / MCLK00	DISP_DATAR2	—	—	ENCIFCK04 / SCKE04 / HDSL08_SMPL
B4	VDD33	—	P10_5	A2	MTIOC1B / MTIOC0A / GTIOC04_4B	CTS0#	MDAT11 / MDAT01	DISP_DATAR5	—	—	ENCIFDI04 / RXDE04 / HDSL08_MISO1
B5	—	VSS	—	—	—	—	—	—	—	—	—
B6	VDD1833_6	IRQ2	P12_7	D23	GTIOC05_4B / CMTW1_TOC1	CTS2# / SD0_DATA5	MDAT10	—	—	—	ENCIFDI05 / RXDE05 / HDSL10_CLK1

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (3 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
B7	VDD1833_6	—	P13_0	D24	GTIOC02_3A	DE2 / SPI_RSPCK3 / SD0_DATA6	MCLK00	—	—	—	ENCIFCK12 / ENCIFCK03 / SCKE08 / SCKE03 / HDSL10_SEL1
B8	VDD1833_6	IRQ1	P12_4	D20	GTIOC05_3A / CMTW1_TIC0	RXD2/SCL2/MISO2 / SD0_DATA2	MCLK02	—	—	—	ENCIFCK05 / SCKE05 / HDSL09_MOSI2
B9	VDD33	—	P14_4	DACK	POE4# / GTIOC06_1B / GTIOC09_1B / GTIOC06_3A / CMTW0_TIC0	ESC_IRQ / SS4#/ CTS4#/RTS4# / SD1_WP	—	DISP_DATAG4	—	MBX_HINT#	ENCIFDO00 / TXDE00 / HDSL11_MOSI1
B10	—	VSS	—	—	—	—	—	—	—	—	—
B11	VDD1833_7	IRQ14	P17_2	—	GTIOC03_2B	SD1_DATA3	—	—	—	—	TST_OUT06 / HDSL13_SEL2
B12	VDD33	IRQ15	P18_1	A9	GTADSM02_1 / GTIOC07_3A	ESC_LEDERR / CTS0# / CANTXDP0 / SD1_IOVS	—	DISP_DATAB2	—	—	SI08# / HDSL14_MISO1
B13	VDD33	IRQ1	P18_4	A12	GTIOC07_3A / GTADSM04_0	ESC_LEDSTER / TXD1/SDA1/MOSI1 / CANRX1	MCLK11	DISP_DATAB5	—	—	ENCIFCK13 / ENCIFCK14 / SCKE09 / SCKE10 / HDSL14_SEL2
B14	VDD1833_0	—	P20_0	—	—	ETH0_TXCLK	—	—	—	—	HDSL15_MOSI2
B15	—	VSS	—	—	—	—	—	—	—	—	—
B16	VDD1833_0	—	P20_4	—	—	ETH0_TXD3 / CANTX0	—	—	—	—	—
B17	VDD33	—	P22_2	A23	GTETRGB	ETH0_RXER / RXD5/SCL5/MISO5 / CANRX0	—	—	—	—	HDSL01_SEL1
B18	VDD33	IRQ7	P22_5	A20	GTETRGSA	GMAC0_PTPTRG0 / ESC_LATCH0 / CTS5# / CANRX1 / SD0_CD	—	—	—	—	SI14# / HDSL01_CLK2
B19	—	VSS	—	—	—	—	—	—	—	—	—
B20	VDD1833_1	MDW0	P25_1	—	—	ETH1_TXD3 / CANTXDP0	—	—	—	—	—
B21	VDD1833_1	MD1	P24_7	—	—	ETH1_TXD1	—	—	—	—	—
B22	VDD1833_1	IRQ12	P26_5	—	—	CANTX0	—	—	—	—	ENCIFCK01 / SCKE01 / HDSL04_CLK1
B23	VDD33	IRQ2	P27_1	—	GTIOC02_0A	ETH1_COL / CANRX1 / SPI_SSL03	—	—	—	HSPI_CS#	HDSL04_CLK2
B24	VDD33	IRQ3	P27_2	—	GTIOC02_0B	GMAC1_PTPTRG0 / ESC_LEDERR / CANTX1 / SPI_RSPCK0	—	—	—	HSPI_IO0	HDSL04_SEL2
C1	VDD33	—	P09_6	D15	MTIOC7A / GTIOC04_1A / GTIOC10_1A	—	MCLK71	DISP_VSYNC	—	—	SI13# / HDSL07_SEL2
C2	VDD33	IRQ4	P10_0	WE1#	MTIOC7B / GTIOC04_2A / GTIOC10_2A	—	MCLK72	DISP_DATAR0	—	—	TST_OUT14 / HDSL07_MOSI2
C3	VDD33	IRQ2	P10_3	RD#	MTCLKD / MTIOC2B / GTIOC04_3B / GTIOC10_3B	TXD0/SDA0/MOSI0	MDAT10 / MDAT00	DISP_DATAR3	—	—	ENCIFOE04 / DEE04 / HDSL08_CLK1
C4	VDD33	—	P09_7	WE0#	MTIOC7C / GTIOC04_1B / GTIOC10_1B	—	MDAT71	DISP_DE	—	—	DUEI14 / HDSL07_MISO2
C5	VDD33	IRQ3	P10_4	A1	MTIOC1A / GTIOC04_4A	SS0#/CTS0#/RTS0#	MCLK11 / MCLK01	DISP_DATAR4	—	—	ENCIFDO04 / TXDE04 / HDSL08_SEL1

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (4 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
C6	VDD1833_6	—	P13_1	D25	GTIOC02_3B	SPI_MOSI3 / SD0_DATA7	MDAT00	—	—	—	ENCIFOE12 / ENCIFOE03 / DEE08 / DEE03 / HDSL10_MISO1
C7	VDD1833_6	IRQ4	P13_5	D29	GTIOC06_3A	TXD3/SDA3/MOSI3 / SPI_SSL32	MDAT40	—	—	—	ENCIFOE13 / DEE09 / HDSL10_MISO2
C8	VDD1833_6	—	P12_0	D16	MTIC5V / GTIOC05_1A / CMTW0_TIC0	CANRX1 / SD0_CLK	—	—	—	—	DUEI01 / HDSL09_MOSI1
C9	VDD33	—	P14_1	RD/WR #	GTIOC06_0A / GTIOC09_0A / GTIOC05_3A / RTCAT1HZ	SCK4 / SD0_CD	MDAT42	DISP_DATAG1	—	—	DUEI02 / HDSL11_CLK1
C10	VDD33	IRQ6	P14_3	DREQ	POE0# / GTIOC06_1A / GTIOC09_1A	ESC_LINKACT2 / TXD4/SDA4/MOSI4 / SD1_CD	—	DISP_DATAG3	—	—	ENCIFOE00 / DEE00 / HDSL11_MISO1
C11	VDD1833_7	IRQ12	P17_0	—	GTIOC03_1B	SD1_DATA1	—	—	—	—	SI05# / HDSL13_MOSI1
C12	VDD33	SEI	P18_2	A10	GTADSM03_0 / GTIOC07_3B	ETH1_CRS / GMAC1_MDC / SCK1 / CANRX0 / SD1_PWEN	MCLK10	DISP_DATAB3	—	—	HDSL14_MOSI1
C13	VDD33	IRQ3	P18_6	A14	GTIOC07_4A / GTADSM05_0	CTS1# / CANRXDP1	MCLK12	DISP_DATAB7	—	—	ENCIFDO13 / ENCIFDO14 / TXDE09 / TXDE10 / HDSL14_MOSI2
C14	VDD1833_0	—	P21_6	—	—	ETHSW_PHYLINK0 / ESC_PHYLINK0 / CANRXDP1	—	—	—	—	HDSL00_MOSI2
C15	VDD1833_0	ETH0_REFCLK / RMII0_REFCLK	P21_7	—	—	CANTXDP1	—	—	—	—	HDSL01_LINK
C16	VDD1833_0	—	P21_1	—	—	ETH0_RXD2 / CANRXDP0	—	—	—	—	TST_OUT12 / HDSL00_MISO1
C17	VDD33	—	P22_1	—	GTETRGA	ETH0_TXER / TXD5/ SDA5/MOSI5 / CANTX0	—	—	—	—	HDSL01_CLK1
C18	VDD33	IRQ8	P22_6	A19	GTETRGSB	GMAC0_PTPTRG1 / ESC_LATCH1 / DE5 / CANTX1 / SD0_WP	—	—	—	—	DUEI15 / HDSL01_SEL2
C19	VDD1833_1	—	P25_6	—	—	ETH1_RXD2 / CANRX1	—	—	—	—	DUEI04 / HDSL03_CLK2
C20	VDD1833_1	—	P26_2	—	—	GMAC1_MDIO / ETHSW_MDIO / ESC_MDIO / CANTXDP1	—	—	—	—	HDSL04_LINK
C21	VDD1833_1	—	P25_3	—	—	ETH1_RXCLK	—	—	—	—	DUEI03 / HDSL03_SEL1
C22	VDD33	SEI	P26_6	CS2#	—	ETH1_TXER / ESC_RESETOUT# / CANRX0	—	—	—	—	ENCIFOE01 / DEE01 / HDSL04_SEL1
C23	VDD33	—	P27_5	—	MTIOC1A / GTIOC08_4A / GTIOC02_2A	TXD0/SDA0/MOSI0 / SPI_SSL00	—	—	—	HSPI_IO3	ENCIFDO14 / TXDE10 / HDSL05_LINK
C24	VDD33	—	P27_6	—	MTIOC1B / GTIOC08_4B / GTIOC02_2B	—	—	—	—	HSPI_CK	ENCIFDI14 / RXDE10 / HDSL05_SMPL
D1	—	—	—	—	—	—	—	—	DDR_DQA12	—	—
D2	—	—	—	—	—	—	—	—	DDR_DQA9	—	—
D3	—	VSS	—	—	—	—	—	—	—	—	—
D4	—	—	—	—	—	—	—	—	DDR_DQA13	—	—
D5	—	VSS	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (5 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
D6	VDD1833_6	—	P12_6	D22	GTIOC05_4A / GTIOC01_3B / CMTW1_TIC1	SS2#/CTS2#/ RTS2# / SD0_DATA4	MCLK10	—	—	—	ENCIFDO05 / TXDE05 / HDSL10_SMPL
D7	VDD1833_6	—	P12_5	D21	GTIOC05_3B / GTIOC01_3A / CMTW1_TOC 0	TXD2/SDA2/MOSI2 / SD0_DATA3	MDAT02	—	—	—	ENCIFOE05 / DEE05 / HDSL10_LINK
D8	—	VSS	—	—	—	—	—	—	—	—	—
D9	VDD33	—	P14_5	TEND	POE8# / GTIOC06_2A / GTIOC09_2A / GTIOC06_3B / CMTW0_TOC 0	ESC_RESETOUT# / CTS4#	—	DISP_DATAG5	—	—	ENCIFDI00 / RXDE00 / HDSL11_CLK2
D10	VDD1833_7	—	P16_7	—	GTIOC03_1A	SD1_DATA0	—	—	—	—	TST_OUT05 / HDSL13_MISO1
D11	VDD1833_7	IRQ15	P17_3	—	GTETRGA	—	—	—	—	—	SI06# / HDSL13_MISO2
D12	VDD33	—	P17_6	WE2#	GTADSM01_0 / GTETRGD / CMTW1_TIC1	ETHSW_PTPOUT0 / ESC_SYNC0 / RXD0/SCL0/MISO0 / SD1_PWEN	—	DISP_DATAG7	—	—	SI07# / HDSL14_SMPL
D13	—	VSS	—	—	—	—	—	—	—	—	—
D14	VDD1833_0	—	P21_5	—	—	GMAC0_MDIO / ETHSW_MDIO / ESC_MDIO / CANTX1	—	—	—	—	SI13# / HDSL00_MISO2
D15	VDD1833_0	—	P20_7	—	—	ETH0_RXD0	—	—	—	—	SI11# / HDSL00_CLK1
D16	VDD1833_0	—	P20_6	—	—	ETH0_RXCLK	—	—	—	—	TST_OUT11 / HDSL00_SMPL
D17	—	VSS	—	—	—	—	—	—	—	—	—
D18	VDD33	IRQ9	P22_7	A18	GTIOC06_0A	ETH1_CRS / ETHSW_TDMAOUT 2 / ESC_LINKACT0 / CANRXDP1	—	—	—	—	TST_OUT15 / HDSL01_MISO2
D19	VDD1833_1	—	P26_3	—	—	ETHSW_PHYLINK1 / ESC_PHYLINK1	—	—	—	—	HDSL04_SMPL
D20	VDD1833_1	—	P25_5	—	—	ETH1_RXD1	—	—	—	—	SI03# / HDSL03_MOSI1
D21	—	VSS	—	—	—	—	—	—	—	—	—
D22	VDD33	IRQ1	P27_0	CS5#	—	ETH1_CRS / CANTXDP0 / SPI_SSL02	—	—	—	HSPI_INT#	ENCIFDI01 / RXDE01 / HDSL04_MOSI1
D23	VDD33	—	P27_4	—	MTIOC2B / GTIOC08_3B / GTIOC02_1B	RXD0/SCL0/MISO0 / CANTXDP1 / SPI_MISO0	—	—	—	HSPI_IO2	ENCIFOE14 / DEE10 / HDSL04_MOSI2
D24	VDD1833_2	—	P30_4	—	GTIOC09_5B	ETH2_RXDV	—	—	—	—	ENCIFDI11 / RXDE11 / HDSL07_SEL1
E1	—	VSS	—	—	—	—	—	—	—	—	—
E2	—	—	—	—	—	—	—	—	DDR_DQA8	—	—
E3	—	—	—	—	—	—	—	—	DDR_DQA11	—	—
E4	—	—	—	—	—	—	—	—	DDR_DQA14	—	—
E5	—	—	—	—	—	—	—	—	DDR_DQSA_C 1	—	—
E6	VDD1833_6	—	P13_6	D30	GTIOC06_3B / GTIOC04_3A	SS3#/CTS3#/ RTS3# / SPI_SSL23	MCLK41	—	—	—	ENCIFDO13 / TXDE09 / HDSL10_MOSI2
E7	VDD1833_6	—	P12_1	D17	MTIC5W / GTIOC05_1B / CMTW0_TOC 0	CANTX1 / SD0_CMD	—	—	—	—	TST_OUT01 / HDSL09_CLK2
E8	VDD1833_6	—	P12_2	D18	GTIOC05_2A / CMTW0_TIC1	CANRXDP1 / SD0_DATA0	—	—	—	—	SI01# / HDSL09_SEL2

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (6 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
E9	VDD33	—	P14_2	BS#	GTIOC06_0B / GTIOC09_0B / GTIOC05_3B	RXD4/SCL4/MISO4 / SD0_WP	—	DISP_DATAG2	—	—	ENCIFCK00 / SCKE00 / HDSL11_SEL1
E10	VDD1833_7	—	P16_5	—	GTIOC03_0A	SD1_CLK	—	—	—	—	SI04# / HDSL13_CLK1
E11	VDD1833_7	—	P16_6	—	GTIOC03_0B	SD1_CMD	—	—	—	—	DUEI05 / HDSL13_SEL1
E12	VDD33	—	P17_7	WE3#/AH#	GTADSM01_1 / CMTW1_TOC1	ETHSW_PTPOUT1 / ESC_SYNC1 / TXD0/SDA0/MOSI0 / SD1_IOVS	—	DISP_DATAB0	—	—	DUEI08 / HDSL14_CLK1
E13	VDD33	—	P17_4	A6 / DREQ	GTADSM00_0 / GTETRGB / CMTW1_TIC0	DE0 / CANRX0 / SD1_CD	—	—	—	—	DUEI07 / HDSL13_MOSI2
E14	VDD1833_0	—	P20_3	—	—	ETH0_TXD2 / CANRX0	—	—	—	—	—
E15	VDD1833_0	—	P21_0	—	—	ETH0_RXD1	—	—	—	—	DUEI12 / HDSL00_SEL1
E16	VDD1833_0	—	P21_4	—	—	GMAC0_MDC / ETHSW_MDC / ESC_MDC / CANRX1	—	—	—	—	TST_OUT13 / HDSL00_SEL2
E17	VDD33	IRQ5	P22_3	A22	GTETRGC	ETH0_CRS / SCK5 / CANRXDP0	—	—	—	—	DUEI14 / HDSL01_MISO1
E18	VDD1833_1	—	P26_1	—	—	GMAC1_MDC / ETHSW_MDC / ESC_MDC / CANRXDP1	—	—	—	—	HDSL03_MOSI2
E19	VDD1833_1	—	P25_4	—	—	ETH1_RXD0	—	—	—	—	TST_OUT03 / HDSL03_MISO1
E20	VDD1833_1	—	P25_7	—	—	ETH1_RXD3 / CANTX1	—	—	—	—	TST_OUT04 / HDSL03_SEL2
E21	VDD1833_1	ETH1_REFCLK / RMII1_REFCLK	P26_4	—	—	—	—	—	—	—	—
E22	VDD33	IRQ0	P26_7	CS3#	—	ETH1_RXER / ESC_LEDSTER / CANRXDP0 / SPI_SSL01	—	—	—	—	ENCIFDO01 / TXDE01 / HDSL04_MISO1
E23	VDD1833_2	—	P29_1	—	GTIOC09_0A	ETH2_TXCLK	—	—	—	—	ENCIFCK09 / SCKE09 / HDSL06_CLK1
E24	VDD1833_2	IRQ10	P30_2	—	GTIOC09_4B	ETH2_RXD2 / SPI_MOSI2	—	—	—	—	ENCIFOE11 / DEE11 / HDSL07_SMPL
F1	—	—	—	—	—	—	—	—	DDR_DQA15	—	—
F2	—	VSS	—	—	—	—	—	—	—	—	—
F3	—	—	—	—	—	—	—	—	DDR_DQA10	—	—
F4	—	—	—	—	—	—	—	—	DDR_DMIA1	—	—
F5	—	—	—	—	—	—	—	—	DDR_DQSA_T1	—	—
F6	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
F7	VDD1833_6	—	P12_3	D19	GTIOC05_2B / CMTW0_TOC1	SCK2 / CANTXDP1 / SD0_DATA1	—	—	—	—	HDSL09_MISO2
F8	VDD1833_6	IRQ3	P13_2	D26	—	SPI_MISO3 / SD0_RST#	MCLK01	—	—	—	ENCIFDO12 / ENCIFDO03 / TXDE08 / TXDE03 / HDSL10_MOSI1
F9	VDD1833_6	—	P13_3	D27	GTIOC03_3A	SCK3 / SPI_SSL30	MDAT01	—	—	—	ENCIFDI12 / ENCIFDI03 / RXDE08 / RXDE03 / HDSL10_CLK2

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (7 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
F10	—	VSS	—	—	—	—	—	—	—	—	—
F11	VDD33	—	P17_5	A7 / DACK	GTADSM00_1 / GTETRGC / CMTW1_TOC0	SCK0 / CANTX0 / SD1_WP	—	—	—	—	TST_OUT07 / HDSL14_LINK
F12	VDD33	IRQ7	P18_0	A8 / TEND	GTADSM02_0	ESC_LEDRUN / SS0#/CTS0#/ RTS0# / CANRXDP0 / SD1_PWEN	—	DISP_DATAB1	—	—	TST_OUT08 / HDSL14_SEL1
F13	VDD33	IRQ4	P18_7	A15	GTIOC07_4B / GTADSM05_1	ETHSW_PTPOUT3 / ESC_SYNC1 / DE1 / CANTXDP1	MDAT12	—	—	—	ENCIFDI13 / ENCIFDI14 / RXDE09 / RXDE10 / HDSL15_LINK
F14	VDD1833_0	—	P20_2	—	—	ETH0_TXD1	—	—	—	—	—
F15	—	VSS	—	—	—	—	—	—	—	—	—
F16	VDD1833_0	IRQ11	P22_0	—	—	—	—	—	—	—	HDSL01_SMPL
F17	VDD33	IRQ10	P23_0	A17	GTIOC06_0B	ETH1_COL / ETHSW_TDMAOUT3 / ESC_LINKACT1 / CANTXDP1	—	—	—	—	SI15# / HDSL01_MOSI2
F18	VDD1833_1	—	P26_0	—	—	ETH1_RXDV	—	—	—	—	SI04# / HDSL03_MISO2
F19	—	VSS	—	—	—	—	—	—	—	—	—
F20	VDD1833_2	—	P30_0	—	GTIOC09_3B	ETH2_RXD0	—	—	—	—	ENCIFDI10 / RXDE10 / HDSL06_MOSI2
F21	VDD1833_2	—	P29_6	—	GTIOC09_2B	ETH2_TXEN / SPI_SSL22	—	—	—	—	ENCIFOE10 / DEE10 / HDSL06_SEL2
F22	VDD1833_2	IRQ8	P29_4	—	GTIOC09_1B	ETH2_TXD2 / SPI_SSL20	—	—	—	—	ENCIFDI09 / RXDE09 / HDSL06_MOSI1
F23	—	VSS	—	—	—	—	—	—	—	—	—
F24	VDD1833_2	IRQ14	P30_7	—	—	ETHSW_PHYLINK2 / ESC_PHYLINK2 / SPI_MISO3 / SD1_IOVS	MCLK30	—	—	—	SI07# / HDSL07_CLK2
G1	—	—	—	—	—	—	—	—	DDR_DQA6	—	—
G2	—	—	—	—	—	—	—	—	DDR_DQA5	—	—
G3	—	VSS	—	—	—	—	—	—	—	—	—
G4	—	VSS	—	—	—	—	—	—	—	—	—
G5	—	VSS	—	—	—	—	—	—	—	—	—
G6	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
G7	—	VDD33	—	—	—	—	—	—	—	—	—
G8	—	VSS	—	—	—	—	—	—	—	—	—
G9	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
G10	—	VDD33	—	—	—	—	—	—	—	—	—
G11	—	VDD1833_6	—	—	—	—	—	—	—	—	—
G12	—	VDD1833_7	—	—	—	—	—	—	—	—	—
G13	—	VDD1833_0	—	—	—	—	—	—	—	—	—
G14	—	VDD1833_0	—	—	—	—	—	—	—	—	—
G15	—	VDDP_18_1	—	—	—	—	—	—	—	—	—
G16	—	VSS_PLL0	—	—	—	—	—	—	—	—	—
G17	—	VSS	—	—	—	—	—	—	—	—	—
G18	—	VSS	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (8 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
G19	VDD1833_2	ETH2_REFCLK / RMII2_REFCLK	P31_0	—	GTETRGSA	SPI_SSL30	—	—	—	—	HDSL07_SEL2
G20	VDD1833_2	—	P30_5	—	GTIOC09_6A	GMAC2_MDC / ETHSW_MDC / ESC_MDC / SPI_RSPCK3	—	—	—	—	DUEI07 / HDSL07_MISO1
G21	VDD1833_2	IRQ9	P29_5	—	GTIOC09_2A	ETH2_TXD3 / SPI_SSL21	—	—	—	—	ENCIFCK10 / SCKE10 / HDSL06_CLK2
G22	VDD1833_2	—	P29_3	—	GTIOC09_1A	ETH2_TXD1	—	—	—	—	ENCIFDO09 / TXDE09 / HDSL06_MISO1
G23	VDD1833_2	—	P30_1	—	GTIOC09_4A	ETH2_RXD1	—	—	—	—	ENCIFCK11 / SCKE11 / HDSL07_LINK
G24	VDD1833_2	IRQ13	P31_1	—	GTETRGSB	ETH2_RXER / SPI_SSL31	—	—	—	—	HDSL07_MISO2
H1	—	—	—	—	—	—	—	—	DDR_DQA4	—	—
H2	—	VSS	—	—	—	—	—	—	—	—	—
H3	—	—	—	—	—	—	—	—	DDR_DMIA0	—	—
H4	—	—	—	—	—	—	—	—	DDR_DQA7	—	—
H5	—	—	—	—	—	—	—	—	DDR_DQSA_C0	—	—
H6	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
H7	—	VDD33	—	—	—	—	—	—	—	—	—
H8	—	VSS_PLL2	—	—	—	—	—	—	—	—	—
H9	—	DVDD08A_TSU	—	—	—	—	—	—	—	—	—
H10	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
H11	—	VDDP_18_7	—	—	—	—	—	—	—	—	—
H12	—	VDD18_PLL3	—	—	—	—	—	—	—	—	—
H13	—	VSS_PLL3	—	—	—	—	—	—	—	—	—
H14	—	VDDP_18_0	—	—	—	—	—	—	—	—	—
H15	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
H16	—	VDD18_PLL0	—	—	—	—	—	—	—	—	—
H17	—	VSS	—	—	—	—	—	—	—	—	—
H18	—	VSS	—	—	—	—	—	—	—	—	—
H19	—	VDD1833_1	—	—	—	—	—	—	—	—	—
H20	VDD1833_2	—	P29_2	—	GTIOC09_0B	ETH2_TXD0	—	—	—	—	ENCIFOE09 / DEE09 / HDSL06_SEL1
H21	—	VSS	—	—	—	—	—	—	—	—	—
H22	VDD1833_2	—	P29_7	—	GTIOC09_3A	ETH2_RXCLK / SPI_SSL23	—	—	—	—	ENCIFDO10 / TXDE10 / HDSL06_MISO2
H23	VDD1833_2	IRQ11	P30_3	—	GTIOC09_5A	ETH2_RXD3 / SPI_MISO2	—	—	—	—	ENCIFDO11 / TXDE11 / HDSL07_CLK1
H24	VDD1833_2	—	P30_6	—	GTIOC09_6B	GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / SPI_MOSI3	—	—	—	—	TST_OUT07 / HDSL07_MOSI1
J1	—	—	—	—	—	—	—	—	DDR_DQA2	—	—
J2	—	—	—	—	—	—	—	—	DDR_DQA0	—	—
J3	—	—	—	—	—	—	—	—	DDR_DQA1	—	—
J4	—	—	—	—	—	—	—	—	DDR_DQA3	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (9 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
J5	—	—	—	—	—	—	—	—	DDR_DQSA_T0	—	—
J6	—	VSS	—	—	—	—	—	—	—	—	—
J7	—	VDD33	—	—	—	—	—	—	—	—	—
J8	—	VDD18_PLL2	—	—	—	—	—	—	—	—	—
J9	—	AVDD18A_TSU	—	—	—	—	—	—	—	—	—
J10	—	VDDP_18_6	—	—	—	—	—	—	—	—	—
J11	—	VDD08	—	—	—	—	—	—	—	—	—
J12	—	VDD08_PLL3	—	—	—	—	—	—	—	—	—
J13	—	VSS	—	—	—	—	—	—	—	—	—
J14	—	VDD08	—	—	—	—	—	—	—	—	—
J15	—	VSS	—	—	—	—	—	—	—	—	—
J16	—	VDD08_PLL0	—	—	—	—	—	—	—	—	—
J17	—	VDD33	—	—	—	—	—	—	—	—	—
J18	—	VSS	—	—	—	—	—	—	—	—	—
J19	—	VDD1833_1	—	—	—	—	—	—	—	—	—
J20	VDD33	—	P31_6	A16 / TEND	POE11#	GMAC2_PTPTRG0 / ETHSW_TDMAOUT0 / ESC_LEDRUN / SPI_MISO0	MDAT32	—	—	—	ENCIFCK15 / ENCIFCK01 / SCKE11 / SCKE01 / HDSL08_SEL1
J21	VDD33	—	P31_4	DREQ	POE8#	ETH2_CRS / ETHSW_PTPOUT2 / ESC_SYNC0 / SPI_RSPCK0 / SPI_SSL30	MCLK81 / MDAT31	—	—	HSPI_IO6	ENCIFDO09 / TXDE09 / HDSL08_SMPL / POUTB
J22	VDD33	—	P31_3	—	POE4#	ETH2_RXER / ETHSW_TDMAOUT1 / ESC_LEDERR / SPI_SSL33	MDAT80 / MCLK31	—	—	HSPI_IO5	ENCIFOE09 / DEE09 / HDSL08_LINK
J23	VDD33	—	P31_5	DACK	POE10#	ETH2_COL / ETHSW_PTPOUT3 / ESC_SYNC1 / SPI_MOSI0 / SPI_SSL31	MDAT81 / MCLK32	—	—	HSPI_IO7	ENCIFDI09 / RXDE09 / HDSL08_CLK1 / POUTZ
J24	VDD33	—	P31_2	—	POE0#	ETH2_TXER / SPI_SSL32	MCLK80 / MDAT30	—	—	HSPI_IO4	ENCIFCK09 / SCKE09 / HDSL07_MOSI2 / POUTA
K1	—	VSS	—	—	—	—	—	—	—	—	—
K2	—	—	—	—	—	—	—	—	DDR_CAA1	—	—
K3	—	VSS	—	—	—	—	—	—	—	—	—
K4	—	VSS	—	—	—	—	—	—	—	—	—
K5	—	VSS	—	—	—	—	—	—	—	—	—
K6	—	—	—	—	—	—	—	—	DDR_CKEA1	—	—
K7	—	VSS	—	—	—	—	—	—	—	—	—
K8	—	VDD08_PLL2	—	—	—	—	—	—	—	—	—
K9	—	VDD08	—	—	—	—	—	—	—	—	—
K10	—	VDD08	—	—	—	—	—	—	—	—	—
K11	—	VSS	—	—	—	—	—	—	—	—	—
K12	—	VDD08	—	—	—	—	—	—	—	—	—
K13	—	VSS	—	—	—	—	—	—	—	—	—
K14	—	VDD08	—	—	—	—	—	—	—	—	—
K15	—	VSS	—	—	—	—	—	—	—	—	—
K16	—	VDD08	—	—	—	—	—	—	—	—	—
K17	—	VDDP_18_2	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (10 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
K18	—	VDD1833_2	—	—	—	—	—	—	—	—	—
K19	—	VDD1833_2	—	—	—	—	—	—	—	—	—
K20	VDD1833_3	—	P34_1	A23	GTADSM03_1 / GTIOC03_0B	ETH3_RXD0 / SPI_MISO2	—	—	—	—	ENCIFDI06 / RXDE06 / HDSL10_CLK1
K21	VDD1833_3	—	P34_5	CS3#	GTADSM05_1 / GTIOC03_2B	ETH3_RXDV / ESC_I2CCLK / TXD3/SDA3/MOSI3 / IIC_SCL1 / SPI_SSL23	—	—	ADTRG1#	—	ENCIFDI07 / RXDE07 / HDSL10_CLK2
K22	VDD1833_3	—	P34_2	A24	GTADSM04_0 / GTIOC03_1A	ETH3_RXD1 / SPI_SSL20	—	—	—	—	ENCIFCK07 / SCKE07 / HDSL10_SEL1
K23	VDD1833_3	—	P34_4	CS2#	GTADSM05_0 / GTIOC03_2A	ETH3_RXD3 / RXD3/ SCL3/MISO3 / SPI_SSL22 / SD1_IOVS	—	—	ADTRG0#	—	ENCIFDO07 / TXDE07 / HDSL10_MOSI1
K24	VDD1833_3	ETH3_REFCLK / RMII3_REFCLK	P34_6	CS5#	—	ETH1_RXER / ESC_I2CDATA / IIC_SDA1 / SPI_RSPCK3	—	—	ADTRG2#	—	DUEI08 / HDSL10_SEL2
L1	—	—	—	—	—	—	—	—	DDR_CKA_C	—	—
L2	—	—	—	—	—	—	—	—	DDR_CAA3	—	—
L3	—	—	—	—	—	—	—	—	DDR_CAA4	—	—
L4	—	—	—	—	—	—	—	—	DDR_CSA0	—	—
L5	—	—	—	—	—	—	—	—	DDR_CSA1	—	—
L6	—	—	—	—	—	—	—	—	DDR_CKEA0	—	—
L7	—	VSS	—	—	—	—	—	—	—	—	—
L8	—	VSS	—	—	—	—	—	—	—	—	—
L9	—	VSS	—	—	—	—	—	—	—	—	—
L10	—	VDD08	—	—	—	—	—	—	—	—	—
L11	—	VSS	—	—	—	—	—	—	—	—	—
L12	—	VDD08	—	—	—	—	—	—	—	—	—
L13	—	VSS	—	—	—	—	—	—	—	—	—
L14	—	VDD08	—	—	—	—	—	—	—	—	—
L15	—	VSS	—	—	—	—	—	—	—	—	—
L16	—	VDD08	—	—	—	—	—	—	—	—	—
L17	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
L18	—	VSS	—	—	—	—	—	—	—	—	—
L19	—	VSS	—	—	—	—	—	—	—	—	—
L20	VDD1833_3	—	P33_2	A16	GTADSM00_0	ETH3_TXCLK / SCK1 / SPI_RSPCK1 / SPI_SSL30	MCLK50	—	—	—	ENCIFCK01 / SCKE01 / HDSL09_MOSI1
L21	VDD1833_3	—	P34_3	A25	GTADSM04_1 / GTIOC03_1B	ETH3_RXD2 / SPI_SSL21 / SD1_PWEN	—	—	—	—	ENCIFOE07 / DEE07 / HDSL10_MISO1
L22	VDD1833_3	—	P34_0	A22	GTADSM03_0 / GTIOC03_0A	ETH3_RXCLK / SPI_MOSI2	—	—	—	—	ENCIFDO06 / TXDE06 / HDSL10_SMPL
L23	VDD1833_3	—	P33_7	A21	GTADSM02_1	ETH3_TXEN / SPI_RSPCK2	MDAT52	—	—	—	ENCIFOE06 / DEE06 / HDSL10_LINK
L24	—	VSS	—	—	—	—	—	—	—	—	—
M1	—	—	—	—	—	—	—	—	DDR_CKA_T	—	—
M2	—	VSS	—	—	—	—	—	—	—	—	—
M3	—	—	—	—	—	—	—	—	DDR_CAA2	—	—
M4	—	VSS	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (11 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
M5	—	—	—	—	—	—	—	—	DDR_CAA5	—	—
M6	—	VSS	—	—	—	—	—	—	—	—	—
M7	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
M8	—	DDR_VAA	—	—	—	—	—	—	—	—	—
M9	—	VSS	—	—	—	—	—	—	—	—	—
M10	—	VDD08	—	—	—	—	—	—	—	—	—
M11	—	VSS	—	—	—	—	—	—	—	—	—
M12	—	VDD08	—	—	—	—	—	—	—	—	—
M13	—	VSS	—	—	—	—	—	—	—	—	—
M14	—	VDD08	—	—	—	—	—	—	—	—	—
M15	—	VSS	—	—	—	—	—	—	—	—	—
M16	—	VDD08	—	—	—	—	—	—	—	—	—
M17	—	VDD33	—	—	—	—	—	—	—	—	—
M18	—	VSS	—	—	—	—	—	—	—	—	—
M19	—	VSS	—	—	—	—	—	—	—	—	—
M20	VDD1833_3	IRQ12	P33_3	A17	GTADSM00_1	ETH3_TXD0 / RXD1/ SCL1/MISO1 / SPI_MOSI1 / SPI_RSPCK0	MDAT50	—	PCIE_RSTOUT0B	—	ENCIFOE01 / DEE01 / HDSL09_CLK2
M21	VDD1833_3	IRQ15	P33_6	A20	GTADSM02_0	ETH3_TXD3 / TXD2/ SDA2/MOSI2 / SPI_SSL11 / SPI_SSL00	MCLK52	—	—	—	ENCIFCK06 / SCKE06 / HDSL09_MOSI2
M22	—	VSS	—	—	—	—	—	—	—	—	—
M23	—	VSS	—	—	—	—	—	—	—	—	—
M24	VDD33_X	EXTCLKIN	—	—	—	—	—	—	—	—	—
N1	—	VSS	—	—	—	—	—	—	—	—	—
N2	—	—	—	—	—	—	—	—	DDR_CKEB1	—	—
N3	—	—	—	—	—	—	—	—	DDR_CAB0	—	—
N4	—	—	—	—	—	—	—	—	DDR_CAA0	—	—
N5	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
N6	—	VSS	—	—	—	—	—	—	—	—	—
N7	—	—	—	—	—	—	—	—	DDR_RESET_N	—	—
N8	—	—	—	—	—	—	—	—	DDR_ATEST	—	—
N9	—	VSS	—	—	—	—	—	—	—	—	—
N10	—	VDD08	—	—	—	—	—	—	—	—	—
N11	—	VSS	—	—	—	—	—	—	—	—	—
N12	—	VDD08	—	—	—	—	—	—	—	—	—
N13	—	VSS	—	—	—	—	—	—	—	—	—
N14	—	VDD08	—	—	—	—	—	—	—	—	—
N15	—	VSS	—	—	—	—	—	—	—	—	—
N16	—	VDD08	—	—	—	—	—	—	—	—	—
N17	—	VDDP_18_3	—	—	—	—	—	—	—	—	—
N18	—	VDD1833_3	—	—	—	—	—	—	—	—	—
N19	—	VDD1833_3	—	—	—	—	—	—	—	—	—
N20	VDD1833_3	IRQ13	P33_4	A18	GTADSM01_0	ETH3_TXD1 / TXD1/ SDA1/MOSI1 / SPI_MISO1 / SPI_MOSI0	MCLK51	—	PCIE_RSTOUT1B	—	ENCIFDO01 / TXDE01 / HDSL09_SEL2

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (12 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
N21	VDD1833_3	IRQ14	P33_5	A19	GTADSM01_1	ETH3_TXD2 / RXD2/ SCL2/MISO2 / SPI_SSL10 / SPI_MISO0	MDAT51	—	—	—	ENCIFDI01 / RXDE01 / HDSL09_MISO2
N22	VDD33_X	XTALSEL	—	—	—	—	—	—	—	—	—
N23	—	XTAL	—	—	—	—	—	—	—	—	—
N24	—	EXTAL	—	—	—	—	—	—	—	—	—
P1	—	—	—	—	—	—	—	—	DDR_CKB_T	—	—
P2	—	—	—	—	—	—	—	—	DDR_CKEB0	—	—
P3	—	VSS	—	—	—	—	—	—	—	—	—
P4	—	VSS	—	—	—	—	—	—	—	—	—
P5	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
P6	—	VSS	—	—	—	—	—	—	—	—	—
P7	—	—	—	—	—	—	—	—	DDR_DTEST	—	—
P8	—	—	—	—	—	—	—	—	DDR_ZN	—	—
P9	—	VDD08	—	—	—	—	—	—	—	—	—
P10	—	VDD08	—	—	—	—	—	—	—	—	—
P11	—	VSS	—	—	—	—	—	—	—	—	—
P12	—	VDD08	—	—	—	—	—	—	—	—	—
P13	—	VDD18_PLL4	—	—	—	—	—	—	—	—	—
P14	—	VDD08	—	—	—	—	—	—	—	—	—
P15	—	VSS	—	—	—	—	—	—	—	—	—
P16	—	VSS	—	—	—	—	—	—	—	—	—
P17	—	VDD33_X	—	—	—	—	—	—	—	—	—
P18	—	VDDP_18_X	—	—	—	—	—	—	—	—	—
P19	—	OTPVDD08	—	—	—	—	—	—	—	—	—
P20	—	OTPVDD18	—	—	—	—	—	—	—	—	—
P21	—	VSS	—	—	—	—	—	—	—	—	—
P22	—	VSS	—	—	—	—	—	—	—	—	—
P23	—	VSS	—	—	—	—	—	—	—	—	—
P24	—	VSS	—	—	—	—	—	—	—	—	—
R1	—	—	—	—	—	—	—	—	DDR_CKB_C	—	—
R2	—	—	—	—	—	—	—	—	DDR_CAB1	—	—
R3	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
R4	—	—	—	—	—	—	—	—	DDR_CAB2	—	—
R5	—	—	—	—	—	—	—	—	DDR_CAB5	—	—
R6	—	—	—	—	—	—	—	—	DDR_CSB0	—	—
R7	—	VSS	—	—	—	—	—	—	—	—	—
R8	—	VSS	—	—	—	—	—	—	—	—	—
R9	—	VDD08	—	—	—	—	—	—	—	—	—
R10	—	VDD08	—	—	—	—	—	—	—	—	—
R11	—	VSS	—	—	—	—	—	—	—	—	—
R12	—	VSS	—	—	—	—	—	—	—	—	—
R13	—	VSS_PLL4	—	—	—	—	—	—	—	—	—
R14	—	PCIE_VDD08A_L1	—	—	—	—	—	—	—	—	—
R15	—	PCIE_VDD08A_L0	—	—	—	—	—	—	—	—	—
R16	—	VSS	—	—	—	—	—	—	—	—	—
R17	—	VSS	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (13 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
R18	—	VSS	—	—	—	—	—	—	—	—	—
R19	—	VSS	—	—	—	—	—	—	—	—	—
R20	—	VSS	—	—	—	—	—	—	—	—	—
R21	—	AVSSIO_ADC0	—	—	—	—	—	—	—	—	—
R22	—	AVDDREF_ADC0	—	—	—	—	—	—	—	—	—
R23	—	—	—	—	—	—	—	—	AN002	—	—
R24	—	—	—	—	—	—	—	—	AN000	—	—
T1	—	—	—	—	—	—	—	—	DDR_CAB3	—	—
T2	—	VSS	—	—	—	—	—	—	—	—	—
T3	—	—	—	—	—	—	—	—	DDR_CAB4	—	—
T4	—	—	—	—	—	—	—	—	DDR_DQB0	—	—
T5	—	VSS	—	—	—	—	—	—	—	—	—
T6	—	—	—	—	—	—	—	—	DDR_CSB1	—	—
T7	—	VSS	—	—	—	—	—	—	—	—	—
T8	—	VSS	—	—	—	—	—	—	—	—	—
T9	—	VSS	—	—	—	—	—	—	—	—	—
T10	—	VSS_PLL1	—	—	—	—	—	—	—	—	—
T11	—	VDD18_PLL1	—	—	—	—	—	—	—	—	—
T12	—	VDD08_PLL1	—	—	—	—	—	—	—	—	—
T13	—	VDD08_PLL4	—	—	—	—	—	—	—	—	—
T14	—	PCIE_VDD08A_L1	—	—	—	—	—	—	—	—	—
T15	—	PCIE_VDD08A_L0	—	—	—	—	—	—	—	—	—
T16	—	PCIE_VDD18A_L1	—	—	—	—	—	—	—	—	—
T17	—	PCIE_VDD18A_L0	—	—	—	—	—	—	—	—	—
T18	—	VSS	—	—	—	—	—	—	—	—	—
T19	—	VSS	—	—	—	—	—	—	—	—	—
T20	—	AVDD_ADC0	—	—	—	—	—	—	—	—	—
T21	—	AVSSIO_ADC0	—	—	—	—	—	—	—	—	—
T22	—	AVDDIO_ADC0	—	—	—	—	—	—	—	—	—
T23	—	—	—	—	—	—	—	—	AN003	—	—
T24	—	—	—	—	—	—	—	—	AN001	—	—
U1	—	—	—	—	—	—	—	—	DDR_DQB2	—	—
U2	—	—	—	—	—	—	—	—	DDR_DQB1	—	—
U3	—	VSS	—	—	—	—	—	—	—	—	—
U4	—	—	—	—	—	—	—	—	DDR_DQB3	—	—
U5	—	—	—	—	—	—	—	—	DDR_DQSB_T0	—	—
U6	—	VSS	—	—	—	—	—	—	—	—	—
U7	—	VSS	—	—	—	—	—	—	—	—	—
U8	—	VSS	—	—	—	—	—	—	—	—	—
U9	—	VSS	—	—	—	—	—	—	—	—	—
U10	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
U11	—	VDD1833_4	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (14 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
U12	—	VSS	—	—	—	—	—	—	—	—	—
U13	—	VDDP_18_5	—	—	—	—	—	—	—	—	—
U14	—	VSS	—	—	—	—	—	—	—	—	—
U15	—	USB_USVDD18	—	—	—	—	—	—	—	—	—
U16	—	PCIE_VDD18A_L1	—	—	—	—	—	—	—	—	—
U17	—	PCIE_VDD18A_L0	—	—	—	—	—	—	—	—	—
U18	—	VSS	—	—	—	—	—	—	—	—	—
U19	—	VSS	—	—	—	—	—	—	—	—	—
U20	—	AVSS_ADC0	—	—	—	—	—	—	—	—	—
U21	—	AVDDIO_ADC1	—	—	—	—	—	—	—	—	—
U22	—	AVDDREF_ADC1	—	—	—	—	—	—	—	—	—
U23	—	—	—	—	—	—	—	—	AN100	—	—
U24	—	—	—	—	—	—	—	—	AN103	—	—
V1	—	VSS	—	—	—	—	—	—	—	—	—
V2	—	—	—	—	—	—	—	—	DDR_DQB4	—	—
V3	—	—	—	—	—	—	—	—	DDR_DQB7	—	—
V4	—	—	—	—	—	—	—	—	DDR_DMIB0	—	—
V5	—	—	—	—	—	—	—	—	DDR_DQSB_C0	—	—
V6	—	VSS	—	—	—	—	—	—	—	—	—
V7	VDD33	TRST#	—	—	—	—	—	—	—	—	—
V8	—	VDD33	—	—	—	—	—	—	—	—	—
V9	—	VDD33	—	—	—	—	—	—	—	—	—
V10	—	VDDP_18_4	—	—	—	—	—	—	—	—	—
V11	—	VDD1833_4	—	—	—	—	—	—	—	—	—
V12	—	VDDP_18_33	—	—	—	—	—	—	—	—	—
V13	—	VDD1833_5	—	—	—	—	—	—	—	—	—
V14	—	VSS	—	—	—	—	—	—	—	—	—
V15	—	USB_USVDD18	—	—	—	—	—	—	—	—	—
V16	—	USB_USVDD33	—	—	—	—	—	—	—	—	—
V17	—	USB_USVDD33	—	—	—	—	—	—	—	—	—
V18	—	VSS	—	—	—	—	—	—	—	—	—
V19	—	VSS	—	—	—	—	—	—	—	—	—
V20	—	AVSS_ADC1	—	—	—	—	—	—	—	—	—
V21	—	AVSSIO_ADC1	—	—	—	—	—	—	—	—	—
V22	—	AVSSIO_ADC1	—	—	—	—	—	—	—	—	—
V23	—	—	—	—	—	—	—	—	AN102	—	—
V24	—	—	—	—	—	—	—	—	AN101	—	—
W1	—	—	—	—	—	—	—	—	DDR_DQB6	—	—
W2	—	DDR_VDDQ	—	—	—	—	—	—	—	—	—
W3	—	—	—	—	—	—	—	—	DDR_DQB5	—	—
W4	—	VSS	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (15 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
W5	—	VSS	—	—	—	—	—	—	—	—	—
W6	—	VSS	—	—	—	—	—	—	—	—	—
W7	VDD1833_4	IRQ11	P06_5	—	GTETRGC	IIC_SDA1 / XSPI0_IO7	—	—	—	—	HDSL05_SEL1
W8	VDD1833_4	IRQ9	P06_3	—	GTETRGA	IIC_SDA0 / XSPI0_IO5	—	—	—	—	TST_OUT09 / HDSL05_SMPL
W9	VDD33	IRQ14	P03_4	D12	MTCLKB / MTIOC8D / GTIOC02_3B / GTADSM09_1 / CMTW1_TOC1 / RTCAT1HZ	IIC_SDA1	—	—	—	—	ENCIFOE02 / DEE02 / HDSL02_MISO2
W10	—	VSS	—	—	—	—	—	—	—	—	—
W11	VDD1833_5	IRQ6	P01_0	—	MTIOC3A / MTIOC1A / GTIOC00_4A / GTIOC00_2B	IIC_SCL1 / XSPI1_CKP	—	—	—	—	ENCIFDO00 / ENCIFDO04 / TXDE00 / TXDE04 / HDSL00_MISO2
W12	VDD33	IRQ1	P00_2	D2	MTIOC4A / GTIOC00_1A	ETH3_CRS	—	—	ADTRG0# / USB_EXICEN	—	SI00# / HDSL00_CLK1
W13	—	VDD1833_5	—	—	—	—	—	—	—	—	—
W14	—	USB_USDVDD	—	—	—	—	—	—	—	—	—
W15	—	USB_USDVDD	—	—	—	—	—	—	—	—	—
W16	—	VSS	—	—	—	—	—	—	—	—	—
W17	—	VSS	—	—	—	—	—	—	—	—	—
W18	—	PCIE_VDD18A_CMN	—	—	—	—	—	—	—	—	—
W19	—	VSS	—	—	—	—	—	—	—	—	—
W20	—	AVDD_ADC1	—	—	—	—	—	—	—	—	—
W21	—	AVSSIO_ADC2	—	—	—	—	—	—	—	—	—
W22	—	AVSSIO_ADC2	—	—	—	—	—	—	—	—	—
W23	—	—	—	—	—	—	—	—	AN206	—	—
W24	—	—	—	—	—	—	—	—	AN210	—	—
Y1	—	—	—	—	—	—	—	—	DDR_DQB8	—	—
Y2	—	VSS	—	—	—	—	—	—	—	—	—
Y3	—	—	—	—	—	—	—	—	DDR_DQB15	—	—
Y4	—	VSS	—	—	—	—	—	—	—	—	—
Y5	—	—	—	—	—	—	—	—	DDR_DQSB_T1	—	—
Y6	—	VSS	—	—	—	—	—	—	—	—	—
Y7	VDD1833_4	IRQ8	P06_2	—	—	IIC_SCL0 / XSPI0_IO4	—	—	—	—	DUEI09 / HDSL05_LINK
Y8	VDD1833_4	IRQ10	P06_4	—	GTETRGB	IIC_SCL1 / XSPI0_IO6	—	—	—	—	SI09# / HDSL05_CLK1
Y9	VDD33	—	P03_1	D9	MTIOC4B / MTIOC1B / GTIOC02_2A / GTADSM08_0 / CMTW1_TIC0	—	—	—	—	—	ENCIFDO02 / TXDE02 / HDSL02_MOSI1
Y10	VDD1833_5	IRQ10	P02_3	—	MTIOC6C / MTIOC1B / GTIOC01_4B	ETH3_COL / IIC_SCL0 / IIC_SCL2 / XSPI1_IO7	MDAT22	—	USB_OVRCUR	—	ENCIFDI01 / RXDE01 / HDSL01_MOSI2
Y11	VDD1833_5	IRQ11	P02_4	—	POE0#	IIC_SDA0	MDAT20	—	USB_EXICEN	MBX_HINT#	HDSL02_LINK

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (16 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
Y12	VDD1833_5	—	P01_2	—	MTIOC6B / MTIOC8B / GTIOC01_0A / GTIOC04_0A	XSPI1_CS1#	—	—	—	—	DUEI02 / HDSL01_LINK
Y13	—	VDD33	—	—	—	—	—	—	—	—	—
Y14	—	—	—	—	—	—	—	—	USB_VUBUSIN	—	—
Y15	—	—	—	—	—	—	—	—	USB_TXRTUNE	—	—
Y16	—	—	—	—	—	—	—	—	PCIE_REFCLK_N1	—	—
Y17	—	—	—	—	—	—	—	—	PCIE_REFCLK_P0	—	—
Y18	—	PCIE_VDD18A_CMN	—	—	—	—	—	—	—	—	—
Y19	—	VSS	—	—	—	—	—	—	—	—	—
Y20	—	AVDD_ADC2	—	—	—	—	—	—	—	—	—
Y21	—	AVDDIO_ADC2	—	—	—	—	—	—	—	—	—
Y22	—	—	—	—	—	—	—	—	AN209	—	—
Y23	—	—	—	—	—	—	—	—	AN208	—	—
Y24	—	—	—	—	—	—	—	—	AN202	—	—
AA1	—	—	—	—	—	—	—	—	DDR_DQB14	—	—
AA2	—	—	—	—	—	—	—	—	DDR_DQB9	—	—
AA3	—	—	—	—	—	—	—	—	DDR_DMIB1	—	—
AA4	—	—	—	—	—	—	—	—	DDR_DQB10	—	—
AA5	—	—	—	—	—	—	—	—	DDR_DQSB_C1	—	—
AA6	VDD33	BSCANP	—	—	—	—	—	—	—	—	—
AA7	VDD1833_4	IRQ3	P05_1	—	—	XSPI0_CKP	—	—	—	—	DUEI06 / HDSL04_SMPL
AA8	—	VSS	—	—	—	—	—	—	—	—	—
AA9	VDD33	IRQ13	P03_3	D11	MTCLKA / MTIOC8C / GTIOC02_3A / GTADSM09_0 / CMTW1_TIC1	IIC_SCL1	—	—	—	—	ENCIFCK02 / SCKE02 / HDSL02_SEL2
AA10	VDD1833_5	IRQ8	P02_1	—	MTCLKD / MTIOC0D / GTIOC01_3B	ETH3_RXER / IIC_SCL2 / XSPI1_IO5	MDAT21	—	—	—	ENCIFOE01 / DEE01 / HDSL01_SEL2
AA11	VDD1833_5	IRQ9	P02_2	—	MTIOC6A / MTIOC1A / GTIOC01_4A	ETH3_CRS / IIC_SDA2 / XSPI1_IO6	MCLK22	—	USB_VBUSEN	—	ENCIFDO01 / TXDE01 / HDSL01_MISO2
AA12	VDD1833_5	IRQ7	P02_0	—	MTCLKC / MTIOC0C / GTIOC01_3A	ETH3_TXER / IIC_SDA1 / XSPI1_IO4	MCLK21	—	—	—	ENCIFCK01 / SCKE01 / HDSL01_CLK2
AA13	VDD33	IRQ0	P00_1	D1	MTIOC3D / GTIOC00_0B	ETH3_RXER	—	—	USB_OVRCUR	—	TST_OUT00 / HDSL00_SMPL
AA14	—	—	—	—	—	—	—	—	USB_OTG_ID	—	—
AA15	—	VSS	—	—	—	—	—	—	—	—	—
AA16	—	—	—	—	—	—	—	—	PCIE_REFCLK_P1	—	—
AA17	—	—	—	—	—	—	—	—	PCIE_REFCLK_N0	—	—
AA18	—	VSS	—	—	—	—	—	—	—	—	—
AA19	—	VSS	—	—	—	—	—	—	—	—	—
AA20	—	AVSS_ADC2	—	—	—	—	—	—	—	—	—

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (17 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AA21	—	AVDDREF_ADC2	—	—	—	—	—	—	—	—	—
AA22	—	—	—	—	—	—	—	—	AN213	—	—
AA23	—	—	—	—	—	—	—	—	AN201	—	—
AA24	—	—	—	—	—	—	—	—	AN200	—	—
AB1	—	—	—	—	—	—	—	—	DDR_DQB12	—	—
AB2	—	VSS	—	—	—	—	—	—	—	—	—
AB3	—	—	—	—	—	—	—	—	DDR_DQB13	—	—
AB4	—	—	—	—	—	—	—	—	DDR_DQB11	—	—
AB5	—	VSS	—	—	—	—	—	—	—	—	—
AB6	VDD1833_4	IRQ4	P05_2	—	—	IIC_SCL2 / XSPI0_CKN	—	—	—	—	TST_OUT06 / HDSL04_CLK1
AB7	VDD1833_4	—	P06_1	—	—	XSPI0_IO3	—	—	—	—	SI08# / HDSL04_MOSI2
AB8	VDD1833_4	IRQ6	P05_4	—	—	IIC_SDA2 / XSPI0_CS1#	—	—	—	—	DUEI07 / HDSL04_MISO1
AB9	VDD33	IRQ12	P03_2	D10	MTIOC4D / MTIOC1A / GTIOC02_2B / GTADSM08_1 / CMTW1_TOC0	—	—	—	—	—	ENCIFDI02 / RXDE02 / HDSL02_CLK2
AB10	VDD33	—	P02_6	D6	MTIOC3D / MTIOC8B / GTIOC02_0B / GTADSM06_1 / CMTW0_TOC0	SD0_IOVS	MDAT00	—	—	—	HDSL02_CLK1 / POUTB
AB11	VDD1833_5	—	P01_1	—	MTIOC3C / MTIOC8A / GTIOC00_4B	XSPI1_CS0#	MCLK20	—	—	—	ENCIFDI00 / ENCIFDI04 / RXDE00 / RXDE04 / HDSL00_MOSI2
AB12	VDD1833_5	—	P01_7	—	MTIOC7D / MTIOC0B / GTIOC01_2B / GTIOC04_2B	XSPI1_IO3	—	—	—	—	SI03# / HDSL01_MOSI1
AB13	VDD33	SEI	P00_0	D0	MTIOC3B / GTIOC00_0A	ETH3_TXER	—	—	USB_VBUSEN	—	DUEI00 / HDSL00_LINK
AB14	—	VSS	—	—	—	—	—	—	—	—	—
AB15	—	VSS	—	—	—	—	—	—	—	—	—
AB16	—	VSS	—	—	—	—	—	—	—	—	—
AB17	—	VSS	—	—	—	—	—	—	—	—	—
AB18	—	VSS	—	—	—	—	—	—	—	—	—
AB19	—	VSS	—	—	—	—	—	—	—	—	—
AB20	—	VSS	—	—	—	—	—	—	—	—	—
AB21	—	VSS	—	—	—	—	—	—	—	—	—
AB22	—	—	—	—	—	—	—	—	AN203	—	—
AB23	—	AVSSIO_ADC2	—	—	—	—	—	—	—	—	—
AB24	—	—	—	—	—	—	—	—	AN212	—	—
AC1	VDD33	MDX	—	—	—	—	—	—	—	—	—
AC2	VDD33	IRQ8 / RSTOUT#	P08_5	—	GTETRGSA	IIC_SCL1 / SD1_PWEN	MCLK02	—	—	—	HDSL06_MISO2
AC3	VDD33	TDO	P08_4	—	—	—	—	—	—	—	HDSL06_SEL2
AC4	VDD33	RES#	—	—	—	—	—	—	—	—	—
AC5	VDD33	TCK	P08_3	—	—	—	—	—	—	—	SI10# / HDSL06_CLK2

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (18 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AC6	VDD1833_4	—	P06_0	—	—	XSPI0_IO2	—	—	—	—	TST_OUT08 / HDSL04_MISO2
AC7	VDD1833_4	—	P05_7	—	—	XSPI0_IO1	—	—	—	—	DUEI08 / HDSL04_SEL2
AC8	VDD1833_4	IRQ12	P06_7	—	POE4# / GTETRGD	GMAC1_MDC / IIC_SCL2	—	—	—	—	HDSL05_MISO1
AC9	VDD33	—	P02_7	D7	MTIOC4A / MTIC5U / GTIOC02_1A / GTADSM07_0 / CMTW0_TIC1	—	MCLK01	—	—	—	HDSL02_SEL1 / POUTZ
AC10	—	VSS	—	—	—	—	—	—	—	—	—
AC11	VDD1833_5	—	P01_5	—	MTIOC7C / MTIC5W / GTIOC01_1B / GTIOC04_1B	XSPI1_IO1	—	—	—	—	DUEI03 / HDSL01_SEL1
AC12	VDD1833_5	—	P01_3	—	MTIOC6D / MTIC5U / GTIOC01_0B / GTIOC04_0B	XSPI1_DS	—	—	—	—	TST_OUT02 / HDSL01_SMPL
AC13	VDD33	IRQ3	P00_4	D4	MTIOC4B / GTIOC00_2A	—	—	—	ADTRG2#	—	TST_OUT01 / HDSL00_MISO1
AC14	—	—	—	—	—	—	—	—	USB_QDP	—	—
AC15	—	VSS	—	—	—	—	—	—	—	—	—
AC16	—	—	—	—	—	—	—	—	PCIE_RXDN_L1	—	—
AC17	—	—	—	—	—	—	—	—	PCIE_RXDN_L0	—	—
AC18	—	VSS	—	—	—	—	—	—	—	—	—
AC19	—	—	—	—	—	—	—	—	PCIE_TXDN_L1	—	—
AC20	—	—	—	—	—	—	—	—	PCIE_TXDN_L0	—	—
AC21	—	VSS	—	—	—	—	—	—	—	—	—
AC22	—	—	—	—	—	—	—	—	AN211	—	—
AC23	—	—	—	—	—	—	—	—	AN204	—	—
AC24	—	—	—	—	—	—	—	—	AN207	—	—
AD1	—	VSS	—	—	—	—	—	—	—	—	—
AD2	VDD33	SEI / CKIO	P08_6	—	GTIOC08_3A / GTETRGSB	IIC_SDA1 / SD1_IOVS	MDAT02 / MCLK11	—	—	—	DUEI11 / HDSL06_MOSI2
AD3	VDD33	TMS	P08_1	—	—	—	—	—	—	—	DUEI10 / HDSL06_MISO1
AD4	VDD33	TDI	P08_2	—	—	—	—	—	—	—	TST_OUT10 / HDSL06_MOSI1
AD5	VDD1833_4	—	P05_6	—	—	XSPI0_IO0	—	—	—	—	SI07# / HDSL04_CLK2
AD6	VDD1833_4	—	P05_5	—	—	XSPI0_DS	—	—	—	—	TST_OUT07 / HDSL04_MOSI1
AD7	VDD1833_4	MDD	P06_6	—	—	XSPI0_RESET0#	—	—	—	—	—
AD8	VDD1833_4	IRQ5	P05_3	—	—	XSPI0_CS0#	—	—	—	—	SI06# / HDSL04_SEL1
AD9	VDD33	—	P03_0	D8	MTIOC4C / MTIC5V / GTIOC02_1B / GTADSM07_1 / CMTW0_TOC1	—	MDAT01	—	—	—	HDSL02_MISO1

Table 1.21 List of pins and pin functions (RZ/N2H 576-pin FCBGA) (19 of 19)

Pin number	IO Port power domain	Power supply clock, system control, Interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI, SDHI)	DSMIF	LCDC	Analog / High speed (DDRSS, ADC, USB, PCIE)	Host Interface (SHOST, MBXSEM)	Encoder I/F (ENCIF, SCIE, ENDAT, HDSL, ENCOUT)
AD10	VDD33	—	P02_5	D5	MTIOC3B / MTIOC8A / GTIOC02_0A / GTADSM06_0 / CMTW0_TIC0	IIC_SCL0 / SD0_PWEN	MCLK00	—	—	—	HDSL02_SMPL / POUTA
AD11	VDD1833_5	—	P01_6	—	MTIOC7B / MTIOC0A / GTIOC01_2A / GTIOC04_2A	XSPI1_IO2	—	—	—	—	TST_OUT03 / HDSL01_MISO1
AD12	VDD1833_5	—	P01_4	—	MTIOC7A / MTIC5V / GTIOC01_1A / GTIOC04_1A	XSPI1_IO0	—	—	—	—	SI02# / HDSL01_CLK1
AD13	VDD33	IRQ2	P00_3	D3	MTIOC4C / GTIOC00_1B	ETH3_COL	—	—	ADTRG1#	—	DUEI01 / HDSL00_SEL1
AD14	—	—	—	—	—	—	—	—	USB_QDM	—	—
AD15	—	VSS	—	—	—	—	—	—	—	—	—
AD16	—	—	—	—	—	—	—	—	PCIE_RXDP_L1	—	—
AD17	—	—	—	—	—	—	—	—	PCIE_RXDP_L0	—	—
AD18	—	VSS	—	—	—	—	—	—	—	—	—
AD19	—	—	—	—	—	—	—	—	PCIE_TXDP_L1	—	—
AD20	—	—	—	—	—	—	—	—	PCIE_TXDP_L0	—	—
AD21	—	VSS	—	—	—	—	—	—	—	—	—
AD22	—	—	—	—	—	—	—	—	AN205	—	—
AD23	—	—	—	—	—	—	—	—	AN214	—	—
AD24	—	AVSSIO_ADC2	—	—	—	—	—	—	—	—	—

2. Electrical Characteristics

Electrical characteristics of this LSI is defined with the following conditions unless otherwise described.

Conditions:

- Core voltage
  VDD08 = VDD08_PLLn (n = 0 to 4) = DVDD08A_TSU = OTPVDD08 = USB_USDVDD = PCIE_VDD08A_Ln (n = 0, 1) = AVDD_ADCn (n = 0 to 2) = 0.76 to 0.84 V
- LPDDR4 I/O voltage
  DDR_VDDQ = 1.06 to 1.17 V
- 1.8V I/O and analog voltage
  VDD1833_n (n = 0 to 7, 1.8 V mode) = VDDP_18_n (n = 0 to 7, 33, X) = VDD18_PLLn (n = 0 to 4) = AVDD18A_TSU = OTPVDD18 = USB_USVDD18 = PCIE_VDD18A_CMN = PCIE_VDD18A_L0 = PCIE_VDD18A_L1 = DDR_VAA = AVDDIO_ADCn (n = 0 to 2) = AVDDREF_ADCn (n = 0 to 2) = 1.71 to 1.89 V
- 3.3V I/O and analog voltage
  VDD33 = VDD1833_n (n = 0 to 7, 3.3 V mode) = VDD33_X = USB_USVDD33 = 3.135 to 3.465 V
- Ground
  VSS = VSS_PLLn (n = 0 to 4) = AVSS_ADCn (n = 0 to 2) = AVSSIO_ADCn (n = 0 to 2) = 0 V
- Operating Temperature
  Tj = −40 to 125ºC

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter	Symbol	Value	Unit
Power supply voltage (3.3-V I/O)	VDD33, VDD1833_0 to VDD1833_7 (3.3-V mode)	−0.3 to +3.8	V
Power supply voltage (1.8-V I/O)	VDD1833_0 to VDD1833_7 (1.8-V mode), VDDP_18_33, VDDP_18_0 to VDDP_18_7	−0.3 to +2.5	V
Power supply voltage (Core)	VDD08	−0.3 to +1.2	V
Input voltage	Vin (3.3-V logic)	−0.3 to smaller value of VDD33/ VDD1833_n (3.3-V mode) + 0.3 or 3.8	V
Input voltage	Vin (1.8-V logic)	−0.3 to smaller value of VDD1833_n (1.8-V mode) + 0.3 or 2.5	V
Oscillator power supply voltage	VDD33_X	−0.3 to +3.8	V
	VDDP_18_X	−0.3 to +2.5	V
PLL power supply voltage	VDD18_PLL0 to VDD18_PLL4	−0.3 to +2.5	V
	VDD08_PLL0 to VDD08_PLL4	−0.3 to +1.2	V
TSU power supply voltage	AVDD18A_TSU	−0.3 to +2.5	V
	DVDD08A_TSU	−0.3 to +1.2	V
OTP power supply voltage	OTPVDD18	−0.3 to +2.5	V
	OTPVDD08	−0.3 to +1.2	V
USB power supply voltage	USB_USVDD33	−0.3 to +3.8	V
	USB_USVDD18	−0.3 to +2.5	V
	USB_USDVDD	−0.3 to +1.2	V
PCI Express power supply voltage	PCIE_VDD18A_CMN, PCIE_VDD18A_L0, PCIE_VDD18A_L1	−0.3 to +2.5	V
	PCIE_VDD08A_L0, PCIE_VDD08A_L1	−0.3 to +1.2	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
LPDDR4 power supply voltage	DDR_VAA	−0.3 to +2.5	V
	DDR_VDDQ	−0.3 to +1.5	V
ADC12 power supply voltage	AVDDIO_ADC0 to AVDDIO_ADC2	−0.3 to +2.5	V
	AVDD_ADC0 to AVDD_ADC2	−0.3 to +1.2	V
ADC12 analog input voltage	VAN	−0.3 to smaller value of AVDDIO_ADCn + 0.3 or 2.5	V
ADC12 reference voltage	AVDDREF_ADC0 to AVDDREF_ADC2	−0.3 to smaller value of AVDDIO_ADCn + 0.3 or 2.5	V
Crystal oscillator pins input voltage	XTAL, EXTAL	−0.3 to + 2.5	V
Operating temperature (Junction temperature)	T_j	−40 to +125	°C
Storage temperature	T_{stg}	−40 to +125	°C

Caution: Permanent damage to the LSI might result if absolute maximum ratings are exceeded.

2.2 Power Supply

Table 2.2 Power supply (1 of 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (3.3-V I/O)	VDD33, VDD1833_0 to VDD1833_7 (3.3-V mode)	3.135	3.3	3.465	V
Power supply voltage (1.8-V I/O)	VDD1833_0 to VDD1833_7 (1.8-V mode), VDDP_18_33, VDDP_18_0 to VDDP_18_7	1.71	1.8	1.89	V
Power supply voltage (Core)	VDD08	0.76	0.8	0.84	V
Ground	VSS	—	0	—	V
Oscillator power supply voltage	VDD33_X	3.135	3.3	3.465	V
	VDDP_18_X	1.71	1.8	1.89	V
PLL power supply voltage	VDD18_PLL0 to VDD18_PLL4	1.71	1.8	1.89	V
	VDD08_PLL0 to VDD08_PLL4	0.76	0.8	0.84	V
	VSS_PLL0 to VSS_PLL4	—	0	—	V
TSU power supply voltage	AVDD18A_TSU	1.71	1.8	1.89	V
	DVDD08A_TSU	0.76	0.8	0.84	V
OTP power supply voltage	OTPVDD18	1.71	1.8	1.89	V
	OTPVDD08	0.76	0.8	0.84	V
USB power supply voltage	USB_USVDD33	3.135	3.3	3.465	V
	USB_USVDD18	1.71	1.8	1.89	V
	USB_USDVDD	0.76	0.8	0.84	V
PCI Express power supply voltage	PCIE_VDD18A_CMN, PCIE_VDD18A_L0, PCIE_VDD18A_L1	1.71	1.8	1.89	V
	PCIE_VDD08A_L0, PCIE_VDD08A_L1	0.76	0.8	0.84	V
LPDDR4 power supply voltage	DDR_VAA	1.71	1.8	1.89	V
	DDR_VDDQ	1.06	1.1	1.17	V

Table 2.2 Power supply (2 of 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
ADC12 power supply voltage	AVDDIO_ADC0 to AVDDIO_ADC2	1.71	1.8	1.89	V
	AVDD_ADC0 to AVDD_ADC2	0.76	0.8	0.84	V
	AVSSIO_ADC0 to AVSSIO_ADC2	—	0	—	V
	AVSS_ADC0 to AVSS_ADC2	—	0	—	V

2.3 Power On/Off Sequence

Power on/off sequence and timing are shown in the figure and table below.

For power-up, 0.8-V (i.e. VDD08) must be supplied first, 1.8-V power (i.e. VDD18 and AVDD) must be supplied second, 1.1-V power must be supplied third, then 3.3-V power (i.e. DDR_VDDQ and VDD33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e. RES#) must be held to Low level during the power-up.

For Power-down, 1.1-V and 3.3-V power (i.e. DDR_VDDQ and VDD33) must go down first and then 0.8-V and 1.8-V power (i.e. VDD08, VDD18, and AVDD). The power-down sequence must be completed within 100 ms.

Rise time of each power supply for the power-up must be larger than 40 µs and fall time of each power supply for the power-down must be larger than 10 µs.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

Stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when reset signal (i.e. RES#) is driven high.

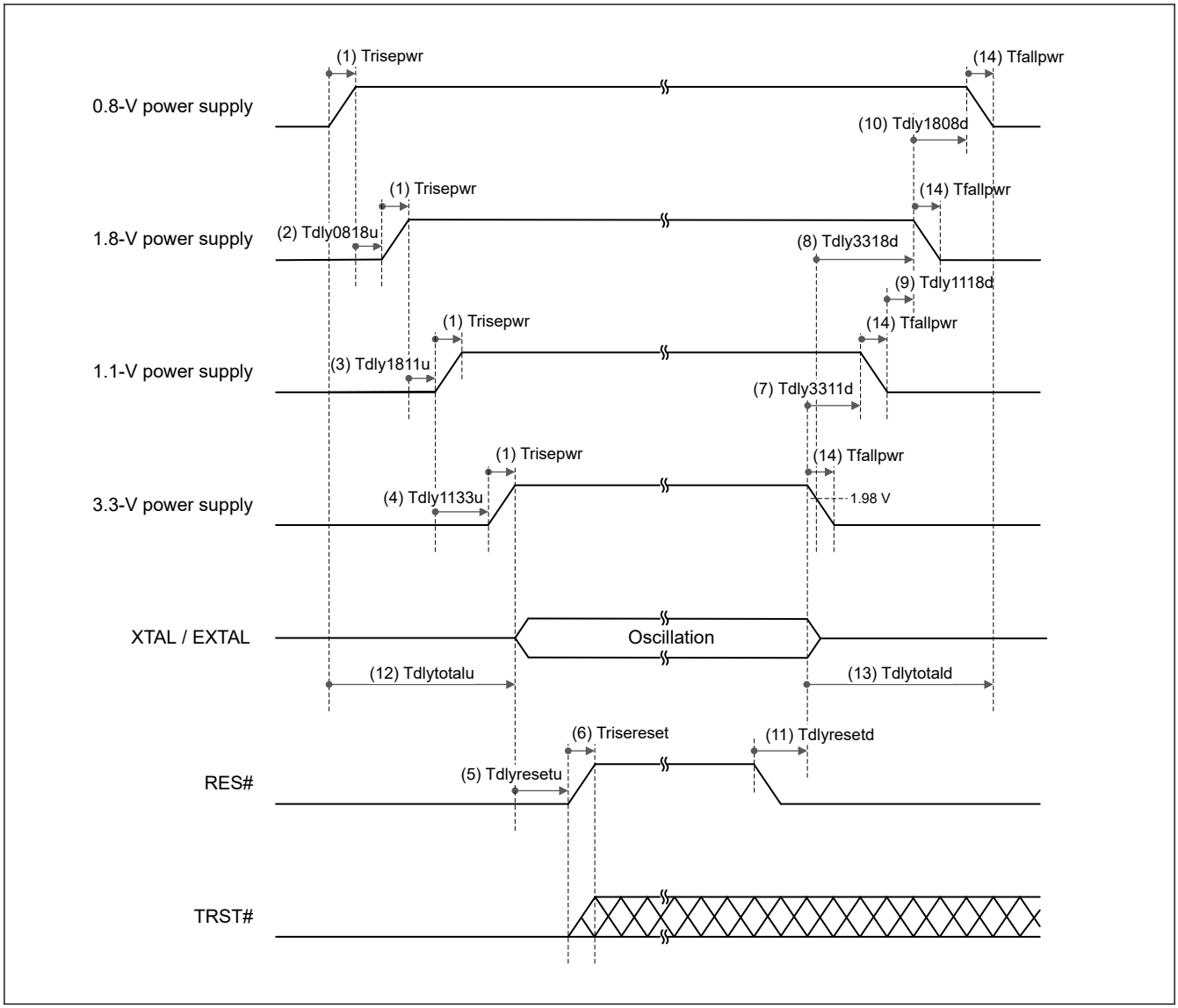


Figure 2.1 Power on/off sequence

Table 2.3 Power on/off sequence timing (1 of 2)

No	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepwr	Rising time of the power supply voltage	40 µs	—	30 ms
(2)	Tdly0818u	Delay time from completion of rising of the 0.8-V power supply voltage to start of rising of the 1.8-V power supply voltage	1 µs	—	100 ms
(3)	Tdly1811u	Delay time from completion of rising of the 1.8-V power supply voltage to start of rising of the 1.1-V power supply voltage	0	—	100 ms
(4)	Tdly1133u	Delay time from start of rising of the 1.1-V power supply voltage to start of rising of the 3.3-V power supply voltage	0	—	100 ms
(5)	Tdlyresetu	Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of RES#	10 ms	—	—
(6)	Triserese t	Rising time of RES#	—	—	150 µs
(7)	Tdly3311d	Delay time from start of falling of the 3.3-V power supply voltage to start of falling of the 1.1-V power supply voltage	0	—	100 ms
(8)	Tdly3318d	Delay time from the time when 3.3-V power supply voltage drops below 1.98-V to start of falling of the 1.8-V power supply voltage	0	—	100 ms

Table 2.3 Power on/off sequence timing (2 of 2)

No	Symbol	Description	Value		
			Min.	Typ.	Max.
(9)	Tdly1118d	Delay time from completion of falling of the 1.1-V power supply voltage to start of falling of the 1.8-V power supply voltage	0	—	100 ms
(10)	Tdly1808d	Delay time from start of falling of the 1.8-V power supply voltage to start of falling of 0.8-V power supply voltage	0	—	100 ms
(11)	Tdlyresetd	Delay time from start of falling of RES# to start of falling of the 3.3-V power supply voltage	10 µs	—	—
(12)	Tdlytotalu	Startup time of all power supply voltage	0	—	100 ms
(13)	Tdlytotald	Shut down time of all power supply voltage	0	—	100 ms
(14)	Tfallpwr	Falling time of the power supply voltage	10 µs	—	30 ms

2.4 DC Characteristics

Table 2.4 DC Characteristics for Type A I/O buffer (VDD33 domain)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH33}	—	VDD33 × 0.7	—	VDD33 + 0.3	V
Input Low-level voltage	V_{IL33}	—	−0.3	—	VDD33 × 0.3	V
Hysteresis voltage	ΔV_{T33}	—	VDD33 × 0.08	—	—	V
Output High-level voltage	V_{OH33}	Low, IOH = −2 mA	VDD33 × 0.8	—	VDD33	V
		Middle, IOH = −4 mA	VDD33 × 0.8	—	VDD33	V
		High, IOH = −8 mA	VDD33 × 0.8	—	VDD33	V
		Ultra High, IOH = −12 mA	VDD33 × 0.8	—	VDD33	V
Output Low-level voltage	V_{OL33}	Low, IOL = 2 mA	0	—	VDD33 × 0.2	V
		Middle, IOL = 4 mA	0	—	VDD33 × 0.2	V
		High, IOL = 8 mA	0	—	VDD33 × 0.2	V
		Ultra High, IOL = 12 mA	0	—	VDD33 × 0.2	V
Input leakage current	$\lvert I_{in} \rvert$	Vin = 0 V, Vin = VDD33	—	—	12	µA
Three-State leakage current (off state)	$\lvert I_{TSI} \rvert$	Vin = 0 V, Vin = VDD33	—	—	12	µA
Input Pull-up resistors resistance	Rpu	Vin = 0 V	10	—	100	kΩ
Input Pull-down resistors resistance	Rpd	Vin = VDD33	10	—	100	kΩ
Input Capacitance	Cin	All input/output and input pins	—	—	10	pF

Table 2.5 DC Characteristics for Type B I/O buffer (VDD1833_n domain) (3.3-V mode) (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH33}	—	VDD1833 × 0.7	—	VDD1833 + 0.3	V
Input Low-level voltage	V_{IL33}	—	−0.3	—	VDD1833 × 0.3	V
Hysteresis voltage	ΔV_{T33}	—	0.1	—	—	V
Output High-level voltage	V_{OH33}	Low, IOH = −8 mA	VDD1833 × 0.8	—	VDD1833	V
		Middle, IOH = −11 mA	VDD1833 × 0.8	—	VDD1833	V
		High, IOH = −14 mA	VDD1833 × 0.8	—	VDD1833	V
		Ultra High, IOH = −17 mA	VDD1833 × 0.8	—	VDD1833	V

Table 2.5 DC Characteristics for Type B I/O buffer (VDD1833_n domain) (3.3-V mode) (2 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Low-level voltage	V_{OL33}	Low, IOL = 8 mA	0	—	VDD1833 × 0.2	V
		Middle, IOL = 11 mA	0	—	VDD1833 × 0.2	V
		High, IOL = 14 mA	0	—	VDD1833 × 0.2	V
		Ultra High, IOL = 17 mA	0	—	VDD1833 × 0.2	V
Input leakage current	$\|I_{in}\|$	Vin = 0 V, Vin = VDD1833	—	—	12	µA
Three-State leakage current (off state)	$\|I_{TSI}\|$	Vin = 0 V, Vin = VDD1833	—	—	12	µA
Input Pull-up resistors resistance	Rpu	Vin = 0 V	18	—	72	kΩ
Input Pull-down resistors resistance	Rpd	Vin = VDD1833	24	—	87	kΩ
Input Capacitance	Cin	All input/output and input pins	—	—	10	pF

Table 2.6 DC Characteristics for Type B I/O buffer (VDD1833_n domain) (1.8-V mode)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH18}	—	VDD1833 × 0.7	—	VDD1833 + 0.3	V
Input Low-level voltage	V_{IL18}	—	−0.3	—	VDD1833 × 0.3	V
Hysteresis voltage	ΔV_{T18}	—	0.1	—	—	V
Output High-level voltage	V_{OH18}	Low, IOH = −4 mA	VDD1833 × 0.8	—	VDD1833	V
		Middle, IOH = −5 mA	VDD1833 × 0.8	—	VDD1833	V
		High, IOH = −6 mA	VDD1833 × 0.8	—	VDD1833	V
		Ultra High, IOH = −7 mA	VDD1833 × 0.8	—	VDD1833	V
Output Low-level voltage	V_{OL18}	Low, IOL = 4 mA	0	—	VDD1833 × 0.2	V
		Middle, IOL = 5 mA	0	—	VDD1833 × 0.2	V
		High, IOL = 6 mA	0	—	VDD1833 × 0.2	V
		Ultra High, IOL = 7 mA	0	—	VDD1833 × 0.2	V
Input leakage current	|Iin|	Vin = 0 V, Vin = VDD1833	—	—	12	µA
Three-State leakage current (off state)	$\|I_{TSI}\|$	Vin = 0 V, Vin = VDD1833	—	—	12	µA
Input Pull-up resistors resistance	Rpu	Vin = 0 V	12	—	92	kΩ
Input Pull-down resistors resistance	Rpd	Vin = VDD1833	13	—	92	kΩ
Input Capacitance	Cin	All input/output and input pins	—	—	10	pF

Table 2.7 Supply Current (1 of 3)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Normal operation	I_{VDD08}	Cortex-A55 Clock = 1.2 GHz, Cortex-R52 Clock = 1.0 GHz, Tj ≤ 110 °C	—	—	4600	mA
	I_{VDD33}	*1	—	50	—	mA
	$I_{VDD1833\_0}$	*1	—	9	—	mA
	$I_{VDD1833\_1}$	*1	—	9	—	mA
	$I_{VDD1833\_2}$	*1	—	9	—	mA
	$I_{VDD1833\_3}$	*1	—	9	—	mA
	$I_{VDD1833\_4}$	*1	—	9	—	mA
	$I_{VDD1833\_5}$	*1	—	9	—	mA
	$I_{VDD1833\_6}$	*1	—	14	—	mA
	$I_{VDD1833\_7}$	*1	—	9	—	mA
	$I_{VDDP\_18\_33}$	—	—	12	—	mA
	$I_{VDDP\_18\_0}$	—	—	2	—	mA
	$I_{VDDP\_18\_1}$	—	—	2	—	mA
	$I_{VDDP\_18\_2}$	—	—	2	—	mA
	$I_{VDDP\_18\_3}$	—	—	2	—	mA
	$I_{VDDP\_18\_4}$	—	—	2	—	mA
	$I_{VDDP\_18\_5}$	—	—	2	—	mA
	$I_{VDDP\_18\_6}$	—	—	2	—	mA
	$I_{VDDP\_18\_7}$	—	—	2	—	mA
	I_{VDD33_X}	—	—	1	—	mA
	$I_{VDDP\_18\_X}$	—	—	10	—	mA
	I_{VDD18_PLL0}	—	—	—	2.2	mA
	I_{VDD18_PLL1}	—	—	—	2.2	mA
	I_{VDD18_PLL2}	—	—	—	2.2	mA
	I_{VDD18_PLL3}	—	—	—	2.2	mA
	I_{VDD18_PLL4}	—	—	—	2.2	mA
	I_{VDD08_PLL0}	—	—	—	2.6	mA
	I_{VDD08_PLL1}	—	—	—	2.6	mA
	I_{VDD08_PLL2}	—	—	—	2.6	mA
	I_{VDD08_PLL3}	—	—	—	2.6	mA
	I_{VDD08_PLL4}	—	—	—	2.6	mA
	$I_{AVDD18A\_TSU}$	—	—	—	1	mA
	$I_{DVDD08A\_TSU}$	—	—	—	0.07	mA
	$I_{OTPVD18}$	—	—	—	18	mA
	$I_{OTPVDD08}$	—	—	—	1.4	mA
	$I_{USB\_USVDD33}$	—	—	—	4.7	mA
	$I_{USB\_USVDD18}$	—	—	—	23	mA
	I_{USB_USDVDD}	—	—	—	8.4	mA

Table 2.7 Supply Current (2 of 3)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Normal operation	$I_{PCIE\_VDD18A\_CMN}$	—	—	—	19	mA
	$I_{PCIE\_VDD18A\_L0}$	—	—	—	27	mA
	$I_{PCIE\_VDD18A\_L1}$	—	—	—	27	mA
	$I_{PCIE\_VDD08A\_L0}$	—	—	—	42	mA
	$I_{PCIE\_VDD08A\_L1}$	—	—	—	42	mA
	I_{DDR_VAA}	—	—	—	5	mA
	I_{DDR_VDDQ}	—	—	—	300	mA
	I_{AVDDIO_ADC0}	—	—	—	0.06	mA
	I_{AVDDIO_ADC1}	—	—	—	0.06	mA
	I_{AVDDIO_ADC2}	—	—	—	0.06	mA
	I_{AVDD_ADC0}	—	—	—	0.7	mA
	I_{AVDD_ADC1}	—	—	—	0.7	mA
	I_{AVDD_ADC2}	—	—	—	0.7	mA
Low power consumption mode*2	I_{VDD08}	All modules inactive	—	105	—	mA
	I_{VDD33}	*1	—	5	—	mA
	$I_{VDD1833\_0}$	*1	—	1	—	mA
	$I_{VDD1833\_1}$	*1	—	1	—	mA
	$I_{VDD1833\_2}$	*1	—	1	—	mA
	$I_{VDD1833\_3}$	*1	—	1	—	mA
	$I_{VDD1833\_4}$	*1	—	1	—	mA
	$I_{VDD1833\_5}$	*1	—	1	—	mA
	$I_{VDD1833\_6}$	*1	—	1	—	mA
	$I_{VDD1833\_7}$	*1	—	1	—	mA
	$I_{VDDP\_18\_33}$	—	—	8	—	mA
	$I_{VDDP\_18\_0}$	—	—	1	—	mA
	$I_{VDDP\_18\_1}$	—	—	1	—	mA
	$I_{VDDP\_18\_2}$	—	—	1	—	mA
	$I_{VDDP\_18\_3}$	—	—	1	—	mA
	$I_{VDDP\_18\_4}$	—	—	1	—	mA
	$I_{VDDP\_18\_5}$	—	—	1	—	mA
	$I_{VDDP\_18\_6}$	—	—	1	—	mA
	$I_{VDDP\_18\_7}$	—	—	1	—	mA
	I_{VDD33_X}	—	—	1	—	mA
	$I_{VDDP\_18\_X}$	—	—	10	—	mA
	I_{VDD18_PLL0}	—	—	2	—	µA
	I_{VDD18_PLL1}	—	—	2.2	—	mA
	I_{VDD18_PLL2}	—	—	2	—	µA
	I_{VDD18_PLL3}	—	—	2	—	µA

Table 2.7 Supply Current (3 of 3)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low power consumption mode*2	I_{VDD18_PLL4}	—	—	2.2	—	mA
	I_{VDD08_PLL0}	—	—	9	—	µA
	I_{VDD08_PLL1}	—	—	1.6	—	mA
	I_{VDD08_PLL2}	—	—	9	—	µA
	I_{VDD08_PLL3}	—	—	9	—	µA
	I_{VDD08_PLL4}	—	—	1.6	—	mA
	$I_{AVDD18A\_TSU}$	—	—	11	—	µA
	$I_{DVDD08A\_TSU}$	—	—	13	—	µA
	$I_{OTPVD18}$	—	—	28	—	µA
	$I_{OTPVDD08}$	—	—	63	—	µA
	$I_{USB\_USVDD33}$	—	—	54	—	µA
	$I_{USB\_USVDD18}$	—	—	18	—	µA
	I_{USB_USDVDD}	—	—	1	—	µA
	$I_{PCIE\_VDD18A\_CMN}$	—	—	0.9	—	mA
	$I_{PCIE\_VDD18A\_L0}$	—	—	0.05	—	mA
	$I_{PCIE\_VDD18A\_L1}$	—	—	0.05	—	mA
	$I_{PCIE\_VDD08A\_L0}$	—	—	1.3	—	mA
	$I_{PCIE\_VDD08A\_L1}$	—	—	1.3	—	mA
	I_{DDR_VAA}	—	—	0.2	—	mA
	I_{DDR_VDDQ}	—	—	0.2	—	mA
	I_{AVDDIO_ADC0}	—	—	0.3	—	µA
	I_{AVDDIO_ADC1}	—	—	0.3	—	µA
	I_{AVDDIO_ADC2}	—	—	0.3	—	µA
	I_{AVDD_ADC0}	—	—	3	—	µA
	I_{AVDD_ADC1}	—	—	3	—	µA
	I_{AVDD_ADC2}	—	—	3	—	µA

Note: These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.

Note 1. IO supply current (I_{VDD33}, $I_{VDD1833\_n\ (n = 0\ to\ 7)}$) should be 50 mA or less. (ΣIOH in Table 2.8)

Note 2. All applicable modules are stopped or standby mode with the lowest clock frequency setting, no pull-up/down or operation for all I/O ports, and room temperature.

Table 2.8 Permissible Output Currents (1 of 2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Permissible output low current (max. value per pin)	IOL	All output pins	Low	—	—	2.5	mA
			Middle	—	—	5.0	
			High	—	—	9.0	
			Ultra High	—	—	11.8	
Permissible output low current (total)	ΣIOL	Sum of all output pins		—	—	50	mA

Table 2.8 Permissible Output Currents (2 of 2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Permissible output high current (max. value per pin)	IOH	All output pins	Low	—	—	2.5	mA
			Middle	—	—	5.0	
			High	—	—	9.0	
			Ultra High	—	—	11.8	
Permissible output high current (total)	ΣIOH	Sum of all output pins		—	—	50	mA

Table 2.9 Thermal Resistance value (Reference)

Item	Symbol	Package	Max.	Unit
Thermal Resistance	Θja	729 pin FCBGA 23 × 23 mm, 0.8-mm pitch	10.9	°C/W
		576 pin FCBGA 21 × 21 mm, 0.8-mm pitch	11.2	°C/W
	Ψjt	729 pin FCBGA 23 × 23 mm, 0.8-mm pitch	0.02	°C/W
		576 pin FCBGA 21 × 21 mm, 0.8-mm pitch	0.02	°C/W

2.5 AC Characteristics

Table 2.10 Operating frequency

Parameter		Symbol	Min.	Max.	Unit
Operating frequency	Cortex-A55 Core clock (CA55CnCLK, n = 0 to 3)	f	600	1200	MHz
	Cortex-A55 SCU clock (CA55SCLK)		500	1000	
	Cortex-R52 Core clock (CR52CnCLK, n = 0, 1)		500	1000	
	Peripheral module clock AH (PCLKAH)		400		
	Peripheral module clock AM (PCLKAM)		200		
	Peripheral module clock AL (PCLKAL)		100		
	Peripheral module clock H (PCLKH)		250		
	Peripheral module clock M (PCLKM)		125		
	Peripheral module clock L (PCLKL)		62.5		
	Peripheral module clock for SCIn (PCLKSCIn, n = 0 to 5)		75	125	
	Peripheral module clock for SCIEn (PCLKSCIEn, n = 0 to 11)		75	125	
	Peripheral module clock for SPIn (PCLKSPIn, n = 0 to 3)		75	125	
	xSPI serial clock (XSPI_CLKn) (n = 0, 1)		12.5	133	
	LCDC clock		5	100	
	DDR controller DFI clock (DFICLK)		800		
	External bus clock output (CKIO)		31.25	125	
	Ethernet PHY reference clock (ETHn_REFCLK, n = 0 to 3)		25		
	Ethernet PHY reference clock (RMIIn_REFCLK, n = 0 to 3)		50		

AC Characteristics are defined in condition of the IO setting (DRCTLm register setting) show in Table 2.11.

Table 2.11 IO setting (DRCTLm register setting) condition (1 of 2)

Module	Signal	IO type	Voltage	DRCTLm register		
				DRVn	SRn	SMTn
Bus, DMAC	CKIO	—	3.3 V	High	Fast	—
	Other than the above	Type A	3.3 V	Middle	Fast	Disable
		Type B	3.3 V	Low	Fast	Disable

Table 2.11 IO setting (DRCTLm register setting) condition (2 of 2)

Module		Signal	IO type	Voltage	DRCTLm register		
					DRVn	SRn	SMTn
MTU3, GPT, IIC, CANFD, DSMIF, ENCIF, ENDAT, HDSL		All signals	Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
SCI, SCIE, SPI		All signals	—	3.3 V	High	Fast	Disable
xSPI (n = 0, 1; m = 0, 1)		XSPIn_CKP, XSPIn_CKN, XSPIn_IO[7:0], XSPIn_CSm#, XSPIn_DS	—	1.8 V	High	Fast	Disable
			—	3.3 V	High	Fast	Enable
		Other than the above	—	—	Low	Slow	Disable
Ethernet Interface (n = 0 to 3, m = 0 to 2)		ETHn_TXCLK	—	1.8 V/3.3 V	Ultra-high	Fast	Disable
		ETHn_TXD[3:0], ETHn_TXEN	—	1.8 V (RGMII)	Ultra-high	Fast	—
			—	3.3 V (RMII)	High	Fast	—
			—	3.3 V (MII)	Middle	Fast	—
		ETHn_TXER	—	3.3 V (MII)	Middle	Fast	—
		ETHn_RXCLK, ETHn_RXD[3:0], ETHn_RXDV	—	1.8 V/3.3 V	—	—	Disable
		ETHn_RXER, ETHn_COL, ETHn_CRS	—	3.3 V	—	—	Disable
		ETHn_REFCLK	—	1.8 V/3.3 V	Middle	Fast	—
		RMIIn_REFCLK	—	1.8 V/3.3 V	High	Fast	—
		GMACm_MDC, GMACm_MDIO, ETHSW_MDC, ETHSW_MDIO, ESC_MDC, ESC_MDIO	—	1.8 V/3.3 V	Middle	Slow	Disable
		Other than the above	—	3.3 V	Middle	Slow	Disable
SHOSTIF, MBXSEM		HSPI_CK, HSPI_CS#, HSPI_IO[7:0]	—	3.3 V	High	Fast	Disable
		HSPI_INT#, MBX_HINT#	Type A	3.3 V	Middle	Slow	—
			Type B	3.3 V	Low	Slow	—
LCDC		All signals	—	3.3 V	Ultra-high	Fast	—
SDHI (n = 0, 1)	SDR104, SDR50, HS200	SDn_CLK	—	1.8 V	Ultra-high	Fast	—
		Other than the above	—	1.8 V	High	Fast	Disable
	DDR50, High Speed DDR	All signals	—	1.8 V/3 .3 V	High	Fast	Disable
	Other than the above	SDn_CLK	—	1.8 V/3 .3 V	High	Fast	—
		Other than the above	—	1.8 V/3 .3 V	Middle	Fast	Disable
Debug Interface		TDO, TMS	—	3.3 V	High	Fast	Disable
		TCK, TDI	—	3.3 V	—	—	Enable
GPIO		All signals in 1.8 V or 3.3 V selectable domain (VDD1833_n (n = 0 to 7))	—	1.8 V/3.3 V	Any	Any	Any
		All signals in 3.3 V fixed domain (VDD33)	—	3.3 V	Any	Any	Any
Other than the above		All signals	—	3.3 V	Low	Slow	Disable

2.5.1 Clock Timing

2.5.1.1 CKIO Pin Output Timing

Table 2.12 CKIO pin output timing

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CKIO pin output cycle time	t_{CKcyc}	Figure 2.2		8*1	—	32	ns
CKIO pin output high level pulse width	t_{CKH}			t_{CKcyc} / 2 - t_{CKr}	—	—	ns
CKIO pin output low level pulse width	t_{CKL}			t_{CKcyc} / 2 - t_{CKf}	—	—	ns
CKIO pin output rising time 1	t_{CKr}	V_{OH33} = VDD33 – 0.5 V, V_{OL33} = 0.4 V	C = 30 pF	—	—	4.0	ns
			C = 15 pF	—	—	3.5	ns
CKIO pin output falling time 1	t_{CKf}	V_{OH33} = VDD33 – 0.5 V, V_{OL33} = 0.4 V	C = 30 pF	—	—	4.0	ns
			C = 15 pF	—	—	3.5	ns
CKIO pin output rising time 2	t_{CKr}	V_{OH33} = 2.0 V, V_{OL33} = 0.8 V	C = 30 pF	—	—	2.3	ns
			C = 15 pF	—	—	1.5	ns
CKIO pin output falling time 2	t_{CKf}	V_{OH33} = 2.0 V, V_{OL33} = 0.8 V	C = 30 pF	—	—	2.3	ns
			C = 15 pF	—	—	1.5	ns

Note 1. Condition is C=15 pF. In case of C = 30 pF, Min. is 12.

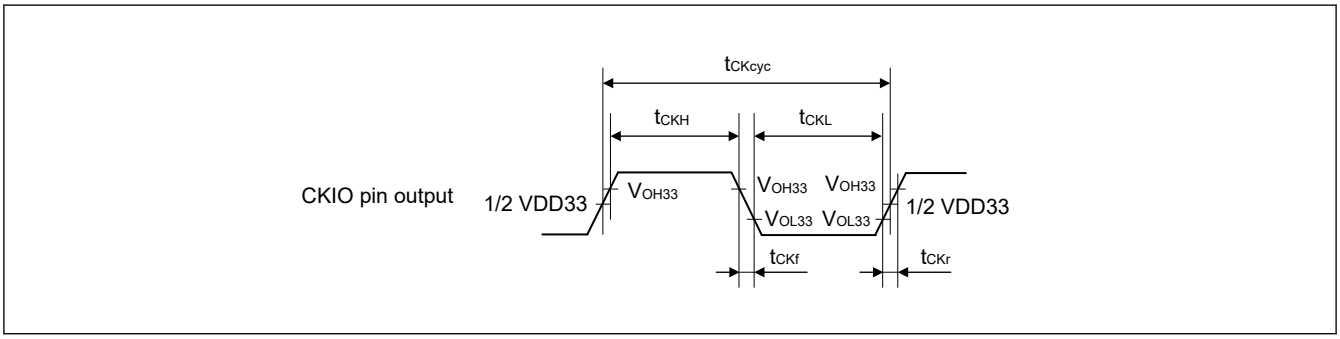


Figure 2.2 CKIO pin output timing

2.5.1.2 Ethernet PHY Reference Clock Output Timing

Conditions:

C = 30 pF (ETHn_REFCLK)

C = 20 pF (RMIIn_REFCLK)

Table 2.13 Ethernet PHY reference clock output timing (1 of 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ETHn_REFCLK cycle time	t_{CK}	—	40	—	—	ns
ETHn_REFCLK frequency	—	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
ETHn_REFCLK duty	—	—	45	—	55	%
		*1	35	—	65	%
ETHn_REFCLK rising/falling time	t_{CKr} / t_{CKf}	—	0.5	—	4.0	ns
RMIIn_REFCLK cycle time	t_{CK}	—	20	—	—	ns
RMIIn_REFCLK frequency	—	—	50.00 ± 50 ppm			MHz
RMIIn_REFCLK duty	—	—	45	—	55	%

Table 2.13 Ethernet PHY reference clock output timing (2 of 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RMIIn_REFCLK rising/falling time	t_{CKr} / t_{CKf}	—	0.5	—	3.5	ns

Note 1. When main clock oscillator is used as reference clock input (by connecting a resonator) and SCKCR.PHYSEL is set to 1 (main clock oscillator is selected as reference clock output).

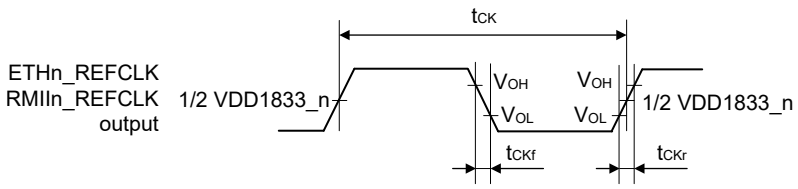


Figure 2.3 Ethernet PHY reference clock output timing

2.5.1.3 EXTCLKIN External Clock Input

Table 2.14 EXTCLKIN clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTCLKIN external clock frequency	$f_{EXTCLKIN}$	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
EXTCLKIN duty	$r_{EXTCLKIN}$	—	±5%			—
EXTCLKIN rising time	$t_{rEXTCLKIN}$	—	0	—	5	ns
EXTCLKIN falling time	$t_{fEXTCLKIN}$	—	0	—	5	ns

Note: XTALSEL and EXTAL should be driven low. Leave XTAL open-circuit.
Note: When using crystal resonator (i.e. EXTA/XTAL clock is used), EXTCLKIN should be driven low and XTALSEL should be driven high.

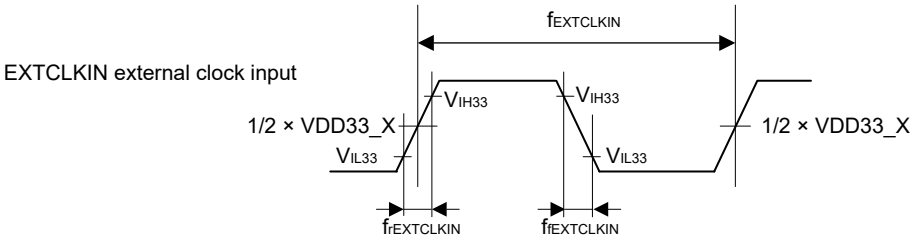


Figure 2.4 EXTCLKIN external clock input timing

2.5.1.4 EXTAL/XTAL Clock Timing

Table 2.15 EXTAL/XTAL clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTAL/XTAL clock frequency*1	f_{XTAL}	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz

Note: XTALSEL should be driven high and EXTCLKIN should be driven low.
Note: When using an external oscillator, be sure to leave XTAL open-circuit and make sure that XTALSEL and EXTAL are driven low.
Note 1. When using the EXTAL/XTAL clock (i.e. crystal resonator), ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.

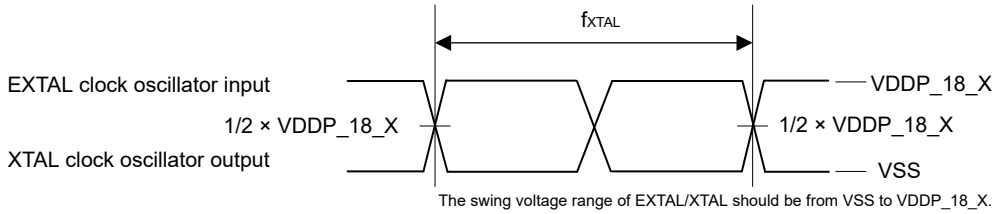


Figure 2.5 EXTAL clock oscillator input and XTAL clock oscillator output timing

2.5.1.5 LOCO Clock Timing

Table 2.16 LOCO clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOCO clock cycle time	t_{Lcyc}	—	0.83	1	1.25	µs
LOCO clock oscillation frequency	t_{LOCO}	—	0.8	1	1.2	MHz
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	—	5	µs

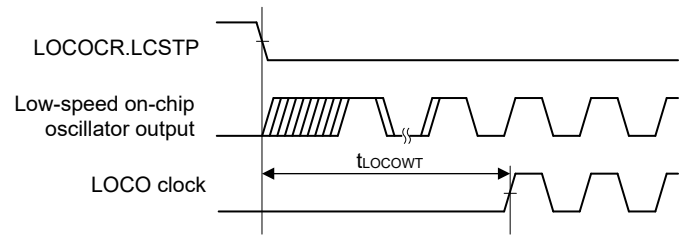


Figure 2.6 LOCO clock oscillation start timing

2.5.2 Reset, Interrupt, and Mode Timing

Table 2.17 Reset, interrupt, and mode timing

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
RES# pulse width	At power on	$t_{dlyreset}$	Figure 2.7	10	—	—	ms
	Other than above	$t_{dlyreset2}$		1	—	—	ms
RES# rising time		$t_{risereset}$		—	—	150	µs
TRST# pulse width	At power on	$t_{dlyreset}$		10	—	—	ms
	Other than above	$t_{dlyreset2}$		1	—	—	ms
TRST# rising time		$t_{risereset}$		—	—	150	µs
SEI pulse width	Level detection	t_{SEIW}	Figure 2.8	t_{PHcyc} × 2 *1	—	—	ns
	Edge detection			t_{PMcyc} × 3.5 *2 *3	—	—	ns
IRQ pulse width	Level detection	t_{IRQW}	Figure 2.9	t_{PHcyc} × 2 *1	—	—	ns
	Edge detection			t_{PMcyc} × 3.5 *2 *3	—	—	ns
Mode hold time (to RES#)	At power on	t_{MDH}	Figure 2.10	250	—	—	ns

Note 1. t_{PHcyc}: PCLKH cycle
Note 2. t_{PMcyc}: PCLKM cycle

Note 3. This value is when noise filter sampling frequency divided rate is 1. In other cases, it is [clock division rate] × t_{PMcyc} × 3.5.

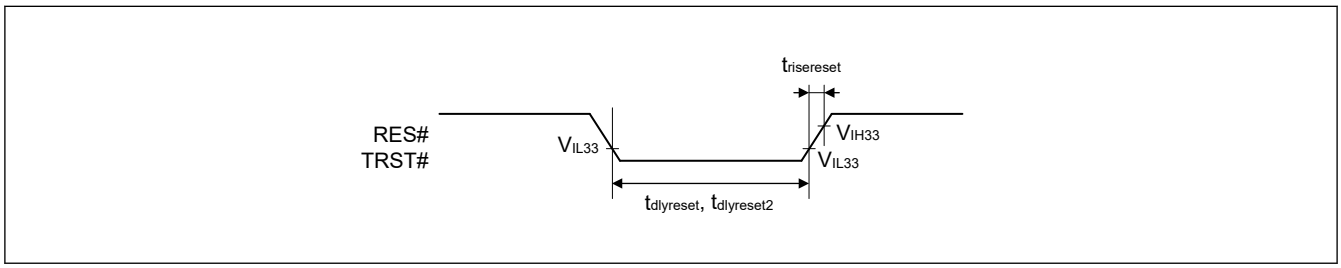


Figure 2.7 Reset input timing

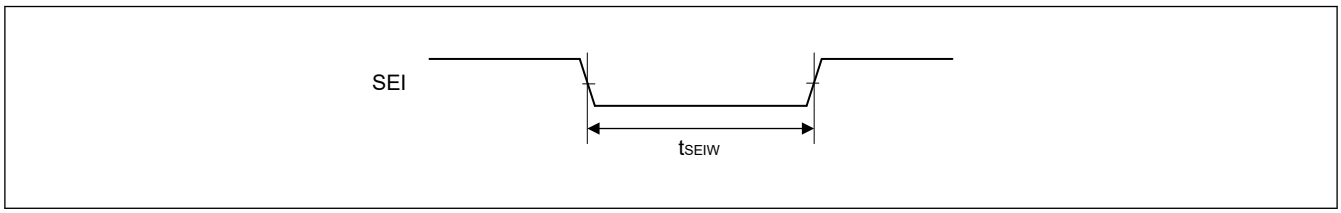


Figure 2.8 SEI interrupt input timing

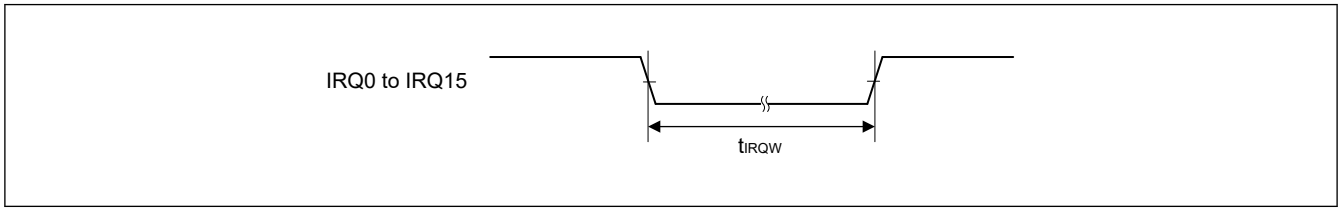


Figure 2.9 IRQ interrupt input timing

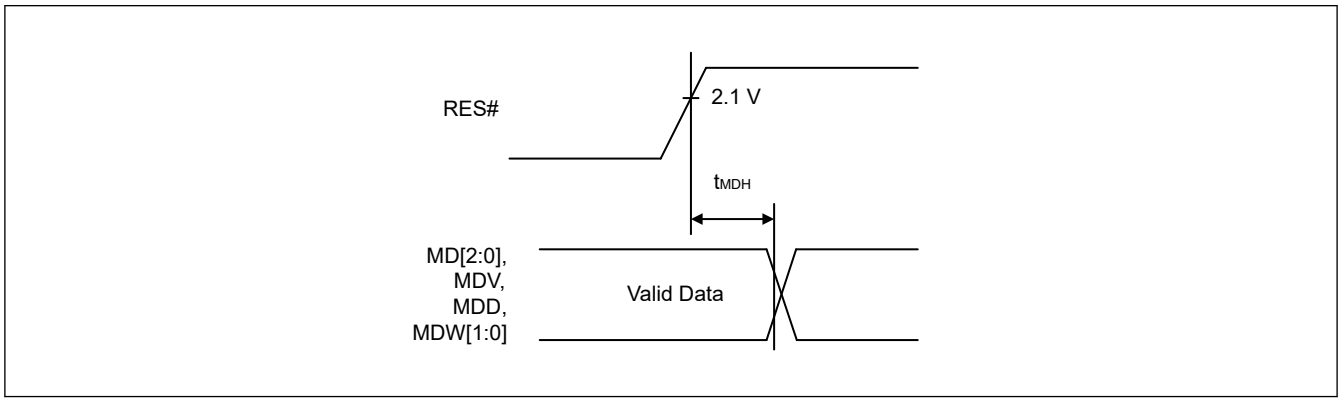


Figure 2.10 Mode input timing

2.5.3 Bus Timing

Table 2.18 Bus timing (1 of 2)

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter	Symbol	CKIO = 1/tCKcyc (Max 83.3 MHz)		Unit	Reference Figure
		Min.	Max.		
Address delay time 1	t_{AD1}	0	8	ns	Figure 2.11 to Figure 2.18
Address delay time 2	t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.18
Address setup time	t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Chip enable setup time	t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18

Table 2.18 Bus timing (2 of 2)

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter	Symbol	CKIO = 1/tCKcyc (Max 83.3 MHz)		Unit	Reference Figure
		Min.	Max.		
Address hold time	t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time	t_{BSD}	—	8	ns	Figure 2.11 to Figure 2.18
CSn# delay time 1	t_{CSD1}	0	8	ns	Figure 2.11 to Figure 2.18
Read/write delay time 1	t_{RWD1}	0	8	ns	Figure 2.11 to Figure 2.18
Read strobe delay time	t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.11 to Figure 2.18
Read data setup time 1	t_{RDS1}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.11 to Figure 2.17
Read data setup time 3	t_{RDS3}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.18
Read data hold time 1	t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1	t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2	t_{WED2}	—	8	ns	Figure 2.17
Write data delay time 1	t_{WDD1}	—	8	ns	Figure 2.11 to Figure 2.17
Write data hold time 1	t_{WDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 4	t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time	t_{WTS}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.12 to Figure 2.18
WAIT# hold time	t_{WTH}	$1/2t_{CKcyc}$	—	ns	Figure 2.12 to Figure 2.18
AH# delay time	t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.15
Multiplex address delay time	t_{MAD}	—	8	ns	Figure 2.15
Multiplex address hold time	t_{MAH}	0	—	ns	Figure 2.15
Address setup time to AH#	t_{AVVH}	$1/2t_{CKcyc}$ − 2	—	ns	Figure 2.15
DACK/TEND delay time	t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.18

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

Table 2.19 Bus timing (1 of 2)

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

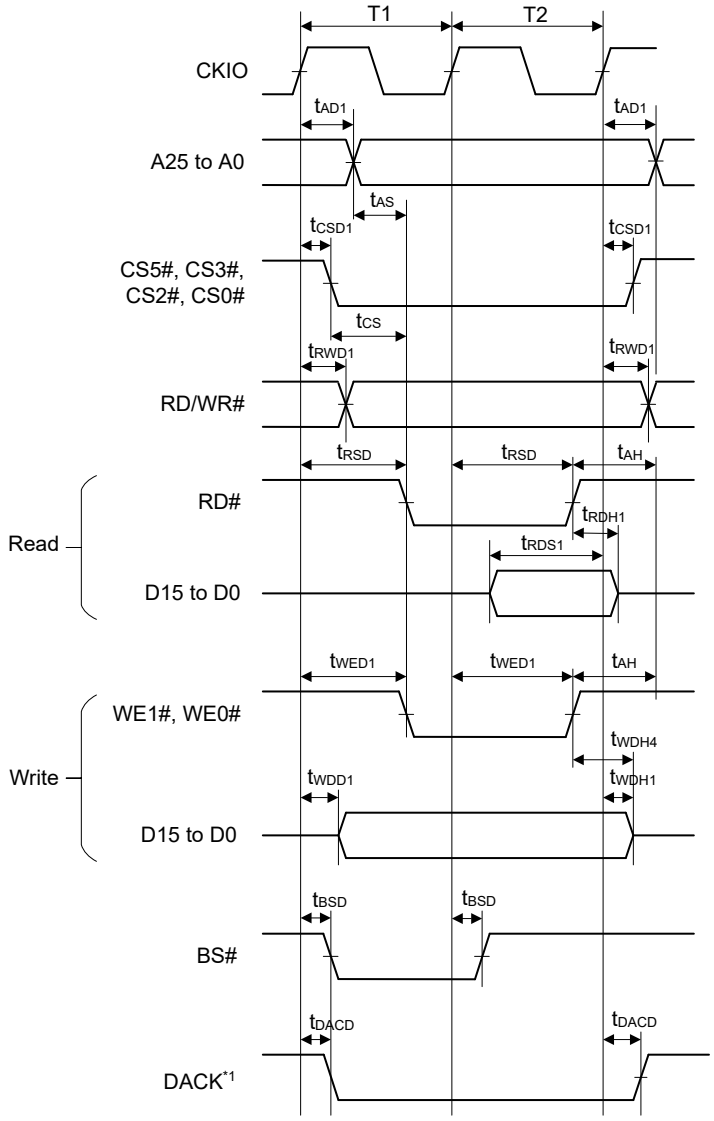
Parameter	Symbol	CKIO = 1/tCKcyc (Max 125 MHz)		Unit	Reference Figure
		Min.	Max.		
Address delay time 1	t_{AD1}	0	6	ns	Figure 2.11 to Figure 2.18
Address delay time 2	t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 6	ns	Figure 2.18
Address setup time	t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Chip enable setup time	t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Address hold time	t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time	t_{BSD}	—	6	ns	Figure 2.11 to Figure 2.18
CSn# delay time 1	t_{CSD1}	0	6	ns	Figure 2.11 to Figure 2.18
Read/write delay time 1	t_{RWD1}	0	6	ns	Figure 2.11 to Figure 2.18
Read strobe delay time	t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 6	ns	Figure 2.11 to Figure 2.18
Read data setup time 1	t_{RDS1}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.11 to Figure 2.17

Table 2.19 Bus timing (2 of 2)

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

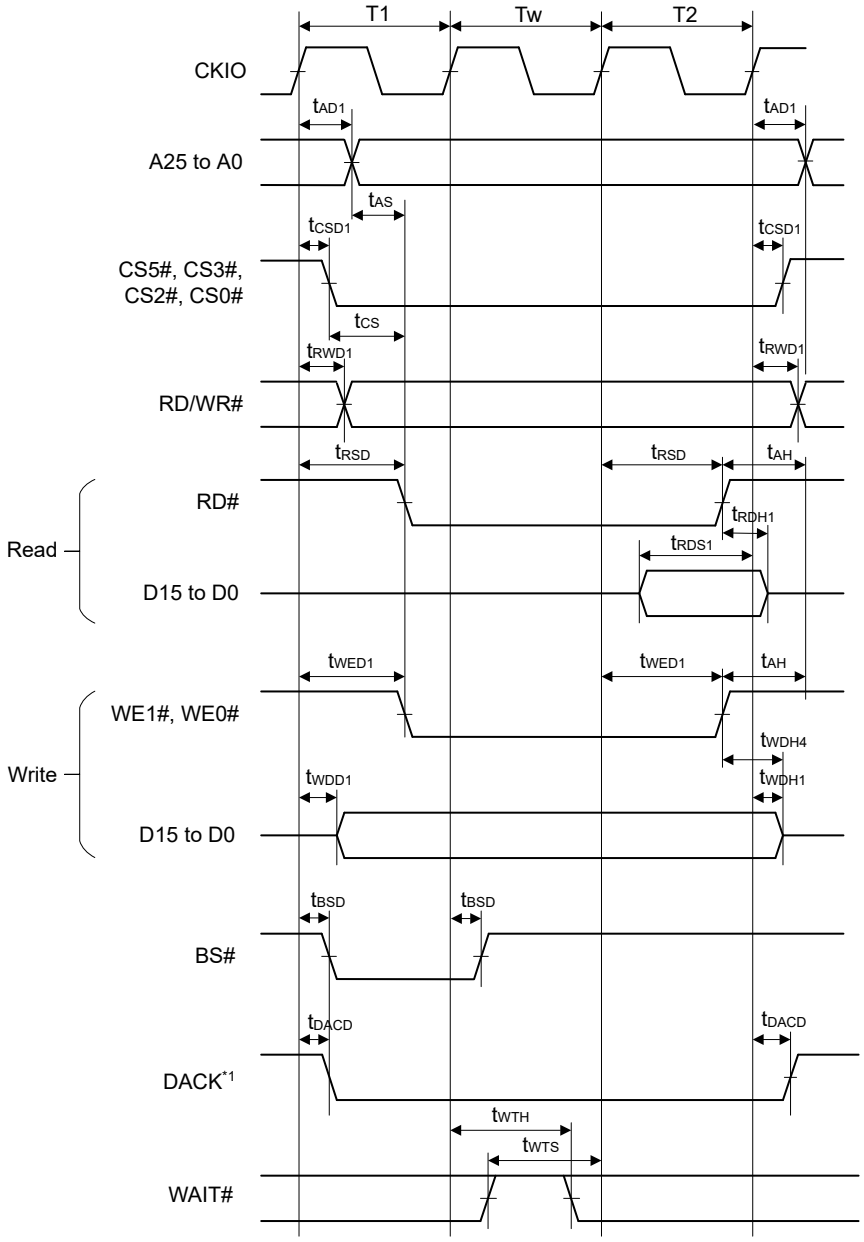
Parameter	Symbol	CKIO = 1/tCKcyc (Max 125 MHz)		Unit	Reference Figure
		Min.	Max.		
Read data setup time 3	t_{RDS3}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.18
Read data hold time 1	t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1	t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 6	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2	t_{WED2}	—	6	ns	Figure 2.17
Write data delay time 1	t_{WDD1}	—	6	ns	Figure 2.11 to Figure 2.17
Write data hold time 1	t_{WDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 4	t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time	t_{WTS}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.12 to Figure 2.18
WAIT# hold time	t_{WTH}	$1/2t_{CKcyc}$	—	ns	Figure 2.12 to Figure 2.18
AH# delay time	t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 6	ns	Figure 2.15
Multiplex address delay time	t_{MAD}	—	6	ns	Figure 2.15
Multiplex address hold time	t_{MAH}	0	—	ns	Figure 2.15
Address setup time to AH#	t_{AVVH}	$1/2t_{CKcyc}$ − 2	—	ns	Figure 2.15
DACK/TEND delay time	t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.18

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.



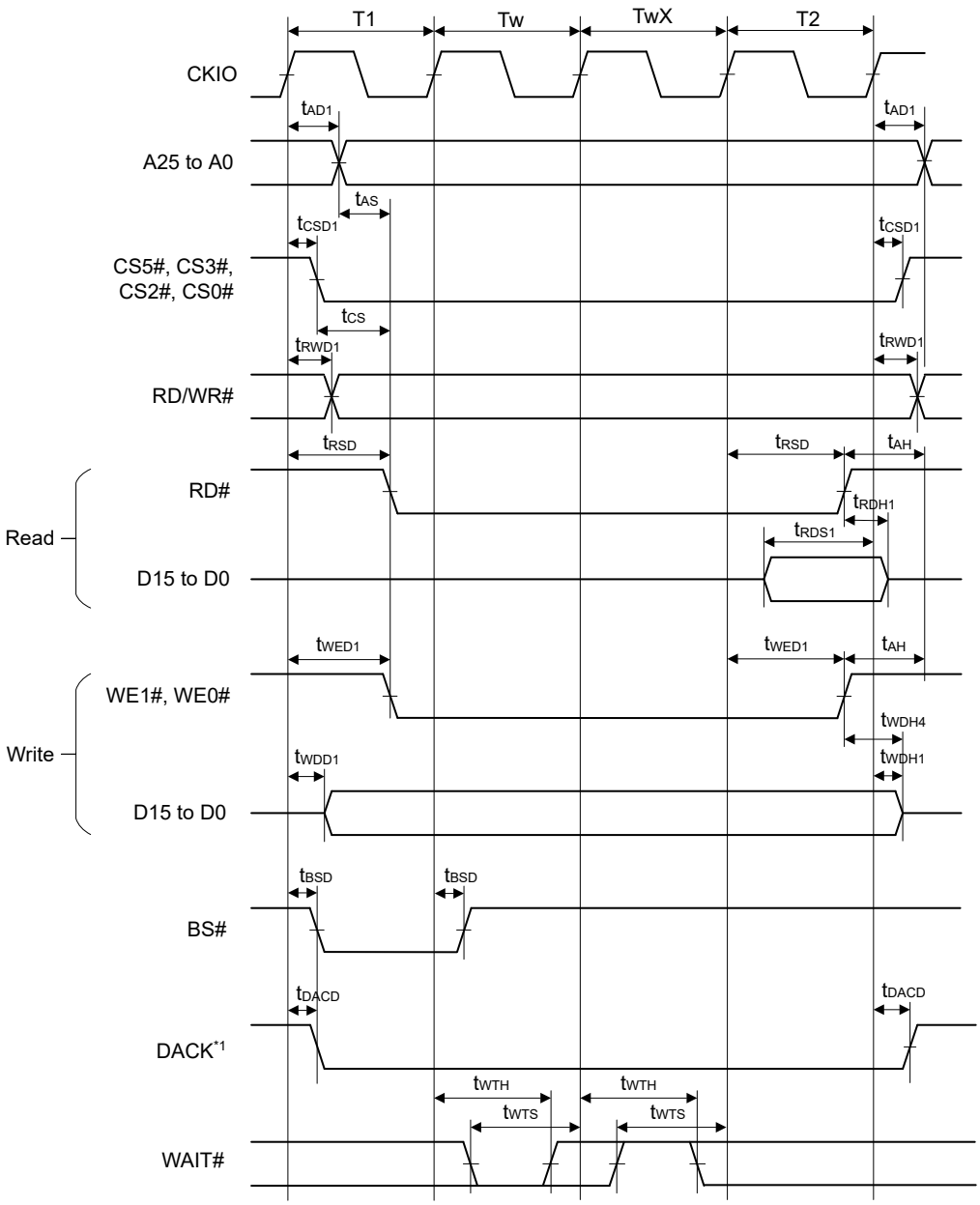
Note 1. DACK is waveform when active-low is specified.

Figure 2.11 SRAM interface basic bus cycle (no wait)



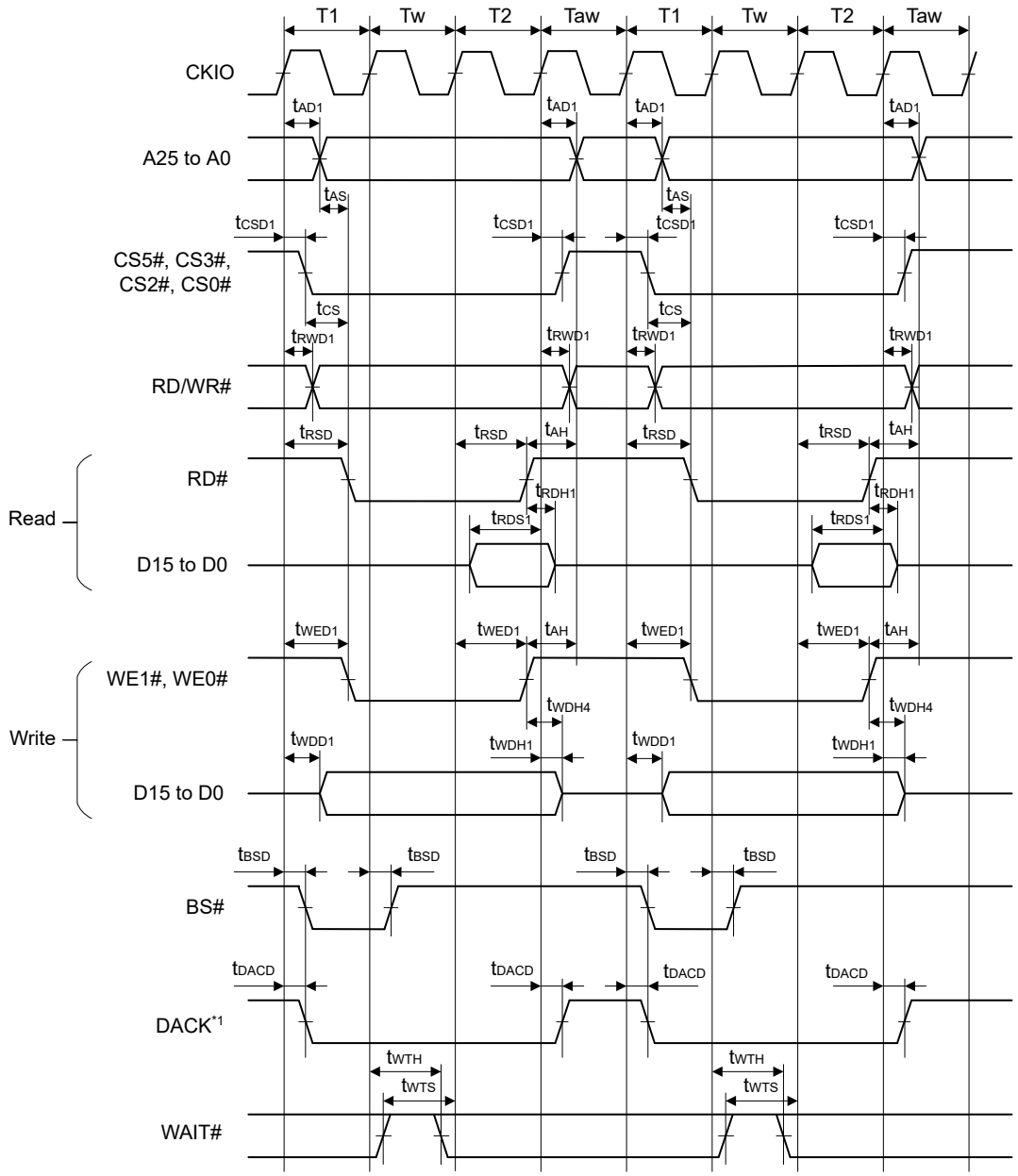
Note 1. DACK is waveform when active-low is specified.

Figure 2.12 SRAM interface basic bus cycle (software wait 1)



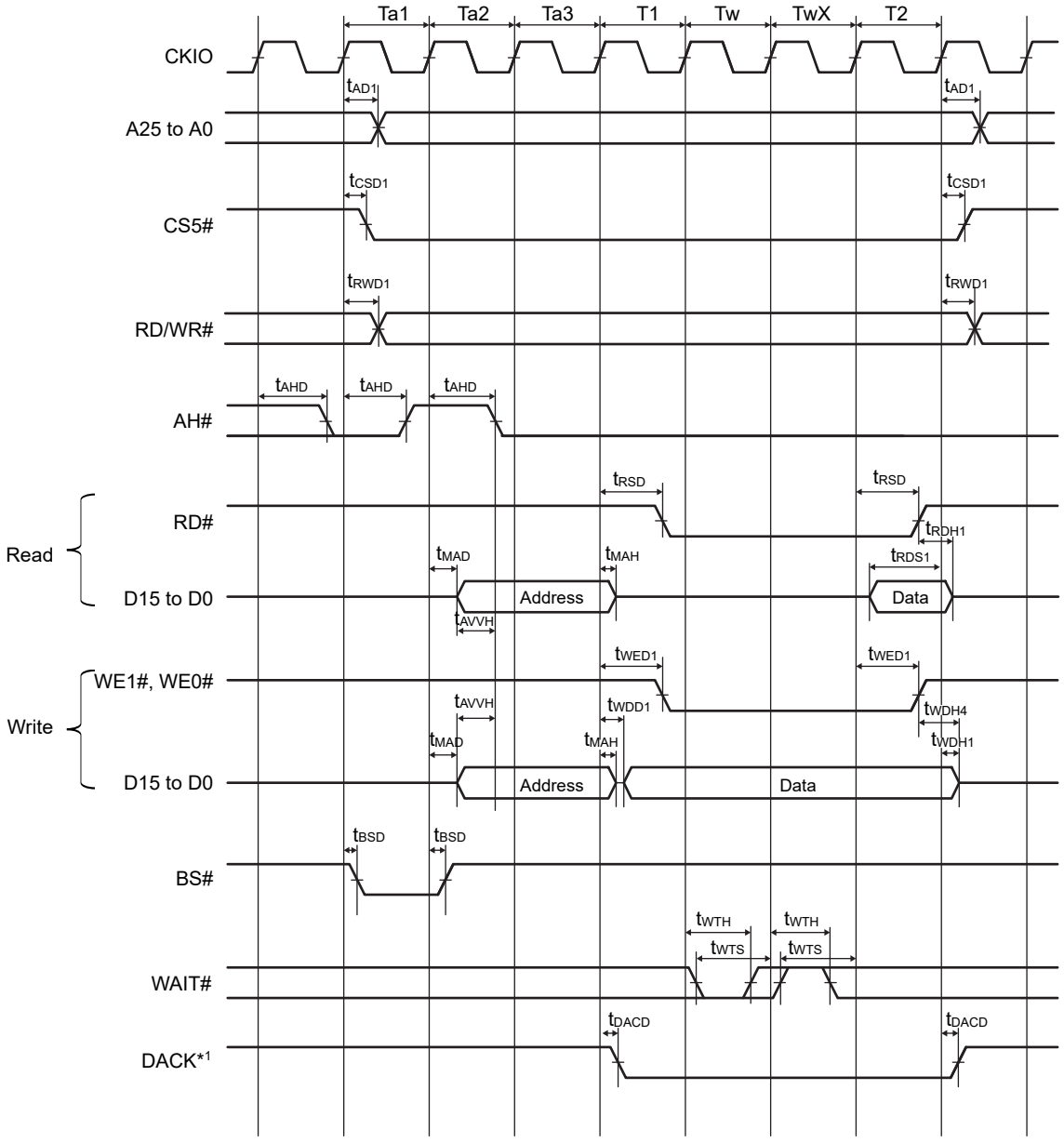
Note 1. DACK is waveform when active-low is specified.

Figure 2.13 SRAM interface basic bus cycle (software wait 1, external wait 1 inserted)



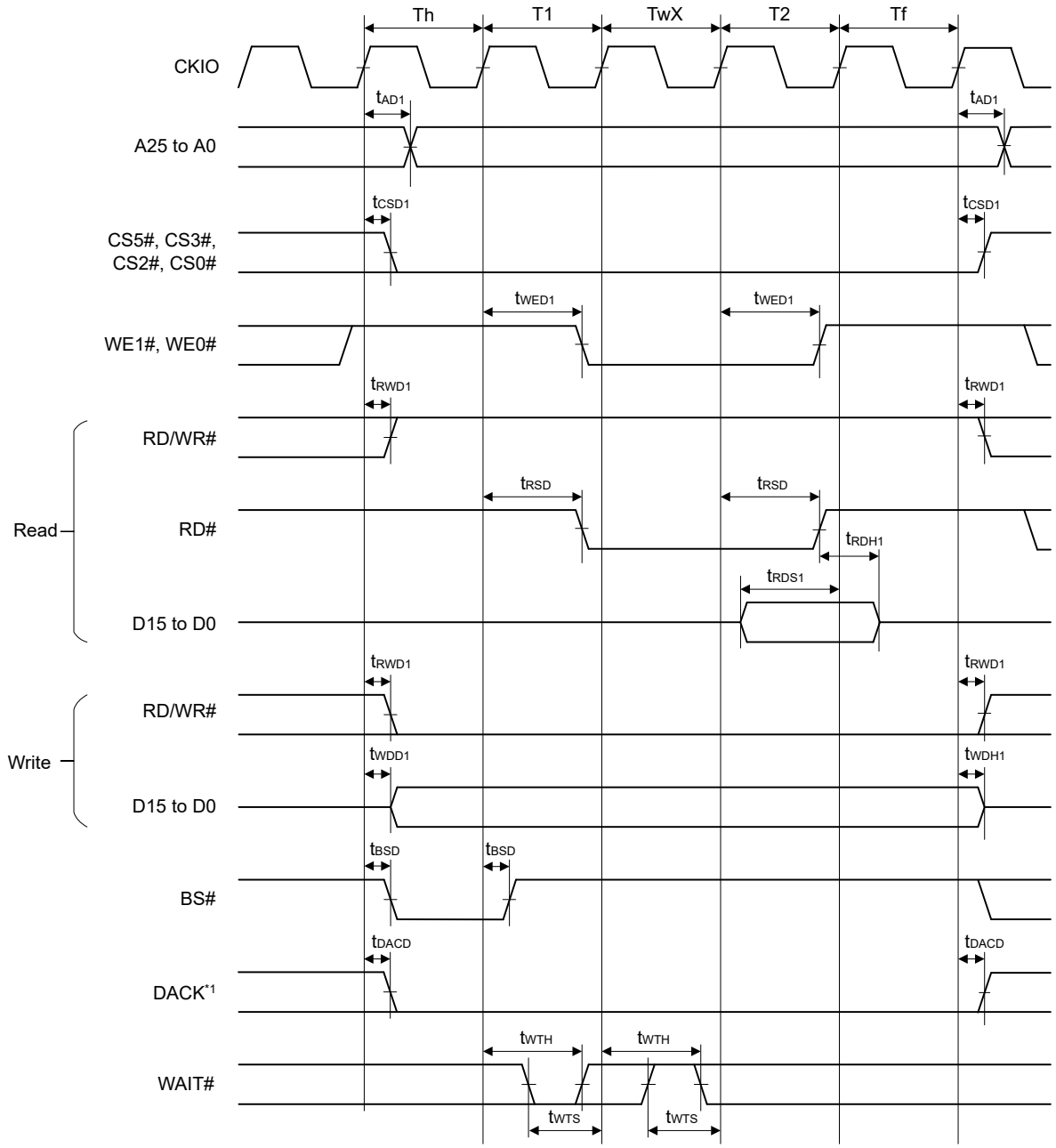
Note 1. DACK is waveform when active-low is specified.

Figure 2.14 SRAM interface basic bus cycle (software wait 1, external wait enabled (WM = 0), no idle cycle)



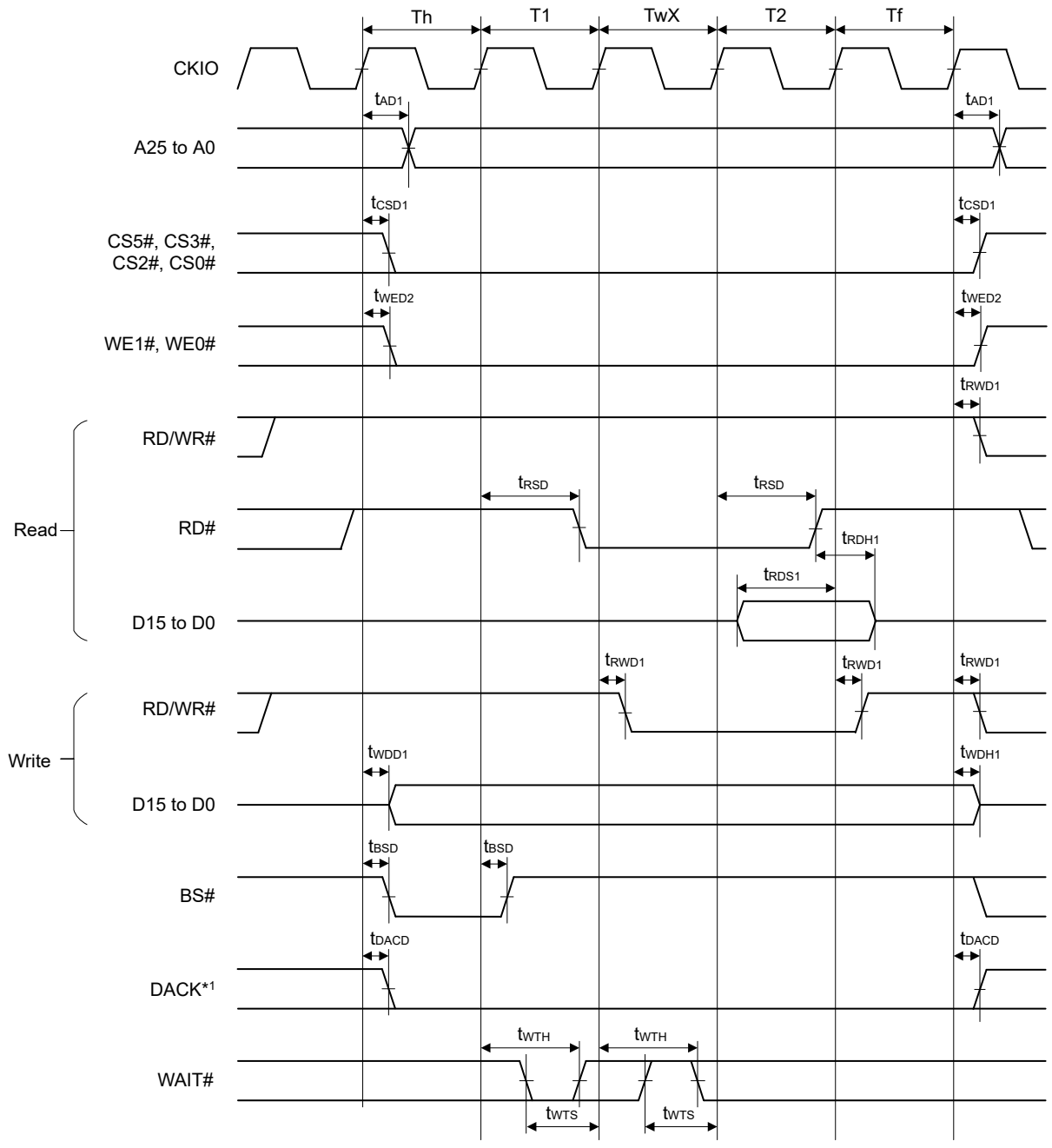
Note 1. DACK is waveform when active-low is specified.

Figure 2.15 MPX-I/O interface bus cycle (address cycle 3, software wait 1, external wait 1 inserted)



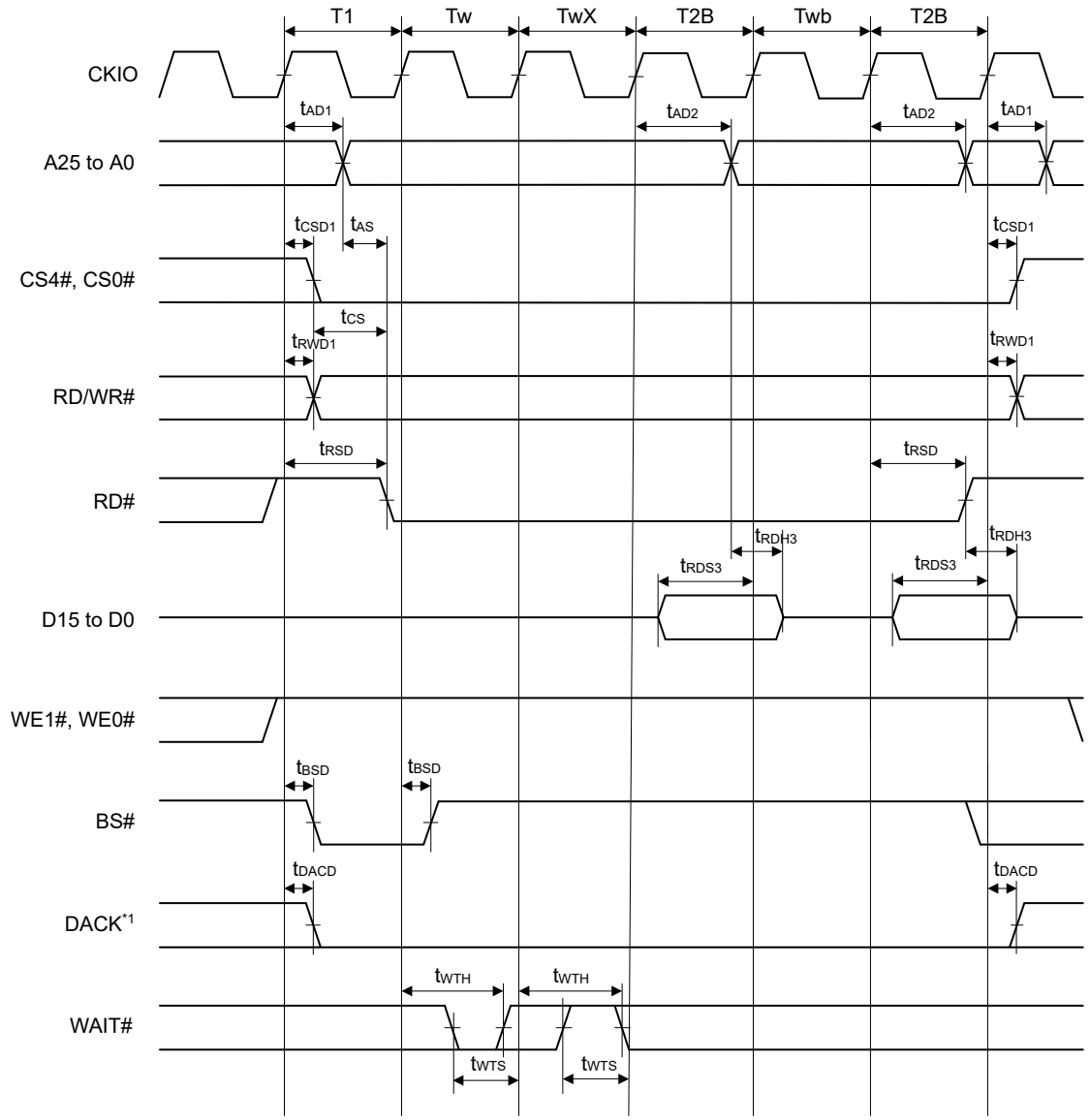
Note 1. DACK is waveform when active-low is specified.

Figure 2.16 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 0 (write cycle UB/LB control))



Note 1. DACK is waveform when active-low is specified.

Figure 2.17 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 1 (write cycle WE control))



Note 1. DACK is waveform when active-low is specified.

Figure 2.18 Burst ROM read cycle (software wait 1, asynchronous external wait 1 inserted, burst wait 1, 2)

2.5.4 DMAC Timing

Table 2.20 DMAC timing

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	t_{PHcyc} × 2	—	ns	Figure 2.19
	DACK and TEND delay time	t_{DACD}	0	8	ns	Figure 2.20

Note 1. t_{PHcyc}: PCLKH cycle

Table 2.21 DMAC timing

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	t_{PHcyc} × 2	—	ns	Figure 2.19
	DACK and TEND delay time	t_{DACD}	0	6	ns	Figure 2.20

Note 1. t_{PHcyc}: PCLKH cycle

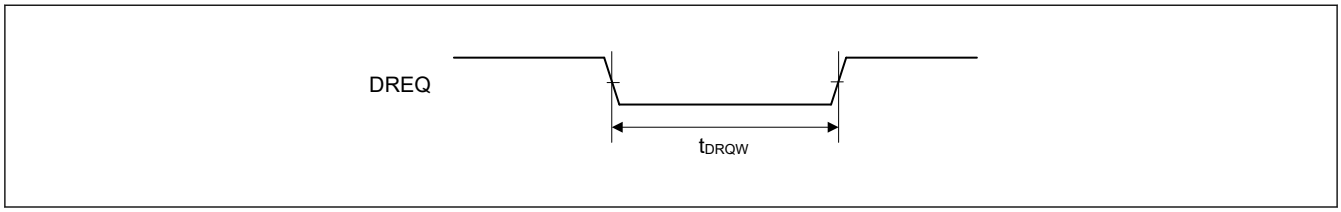


Figure 2.19 DREQ input timing

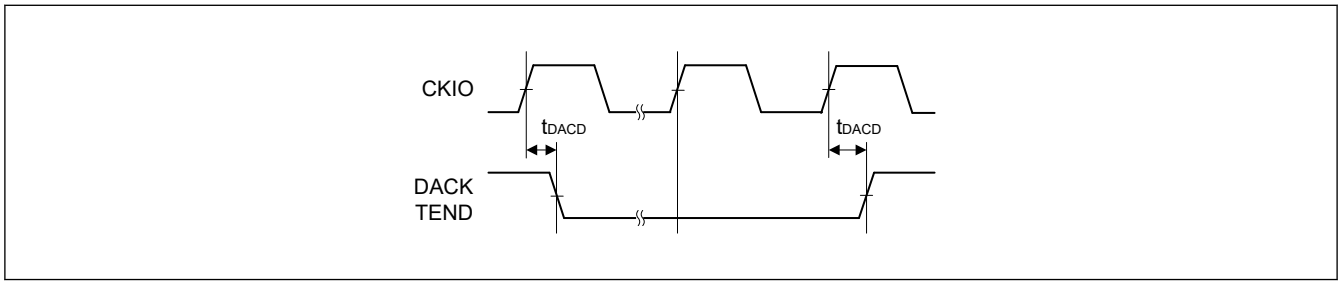


Figure 2.20 DACK and TEND output timing

2.5.5 On-Chip Peripheral Module Timing

2.5.5.1 I/O Port Timing

Table 2.22 I/O port timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PLcyc}	Figure 2.21

Note 1. t_{PLcyc}: PCLKL cycle

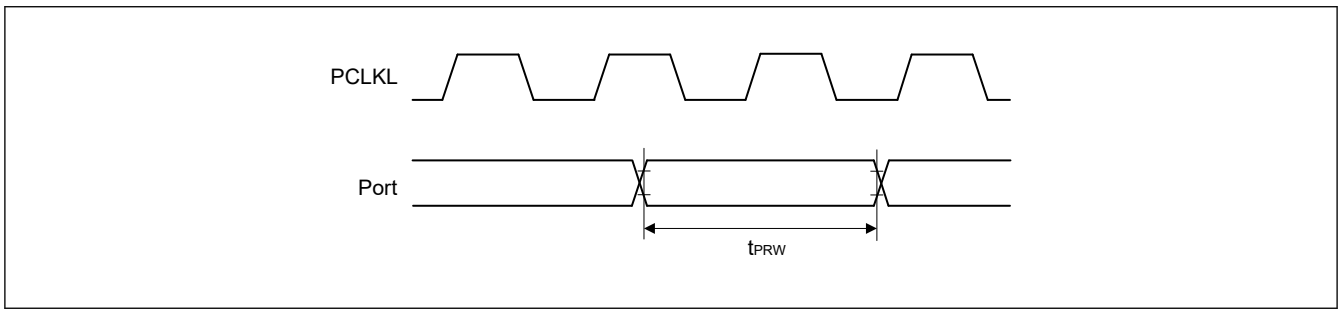


Figure 2.21 I/O port input timing

2.5.5.2 CMTW Timing

Table 2.23 CMTW timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PLcyc}	Figure 2.22
		Both-edge setting		2.5	—		

Note 1. t_{PLcyc}: PCLKL cycle

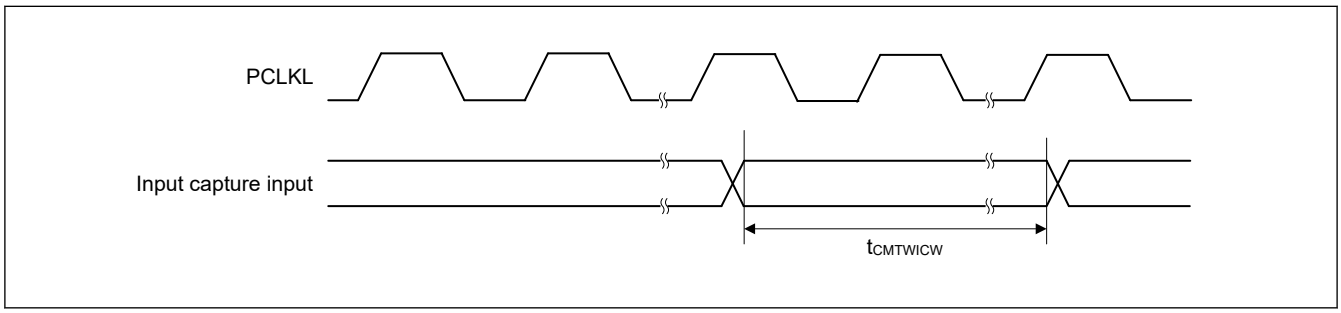


Figure 2.22 CMTW input capture input timing

2.5.5.3 MTU3 Timing

Table 2.24 MTU3 timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	2.5	—	t_{PHcyc}	Figure 2.23
		Both-edge setting		3.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	2.5	—	t_{PHcyc}	Figure 2.24
		Both-edge setting		3.5	—		
		Phase counting mode		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle

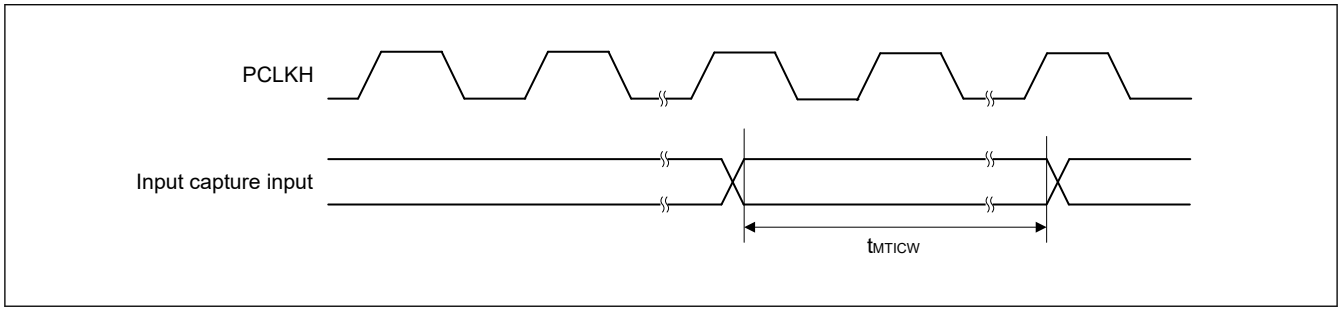


Figure 2.23 MTU3 input capture input timing

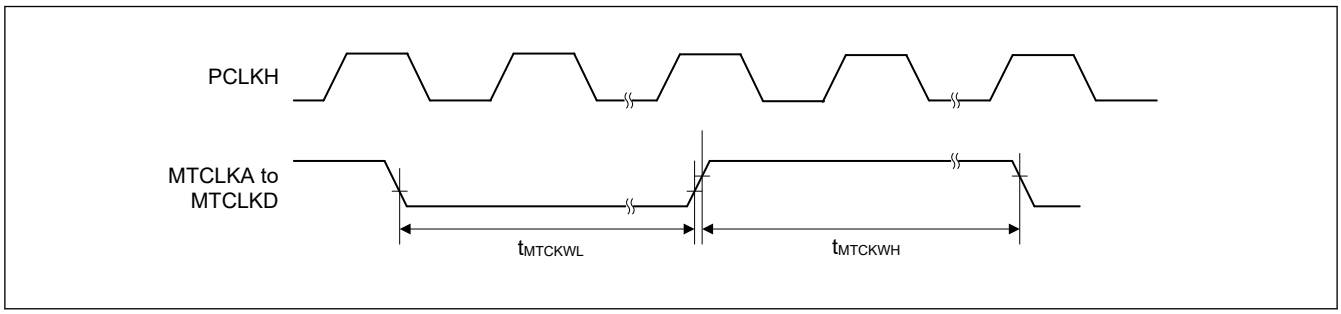


Figure 2.24 MTU3 clock input timing

2.5.5.4 POE3 Timing

Table 2.25 POE3 timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
POE3	POEn# input pulse width		t_{POEW}	2.5	—	t_{PHcyc}	Figure 2.25
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	5 × PCLKH + 0.1	µs	Figure 2.26
		Simultaneous conduction of output pins	t_{POEDO}	—	3 × PCLKH + 0.1	µs	Figure 2.27
		Register setting	t_{POEDS}	—	PCLKH + 0.1	µs	Figure 2.28
		Oscillation stop detection	t_{POEDOS}	—	74	µs	Figure 2.29

Note 1. t_{PHcyc}: PCLKH cycle

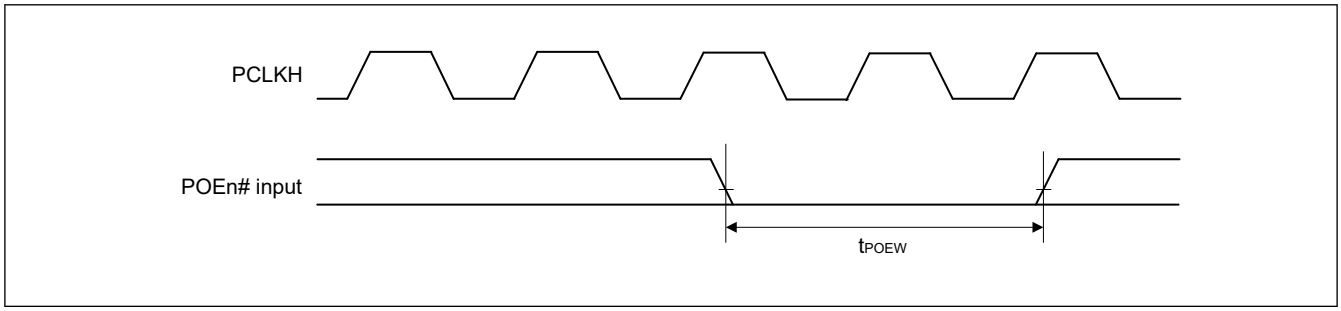


Figure 2.25 POEn# input pulse timing

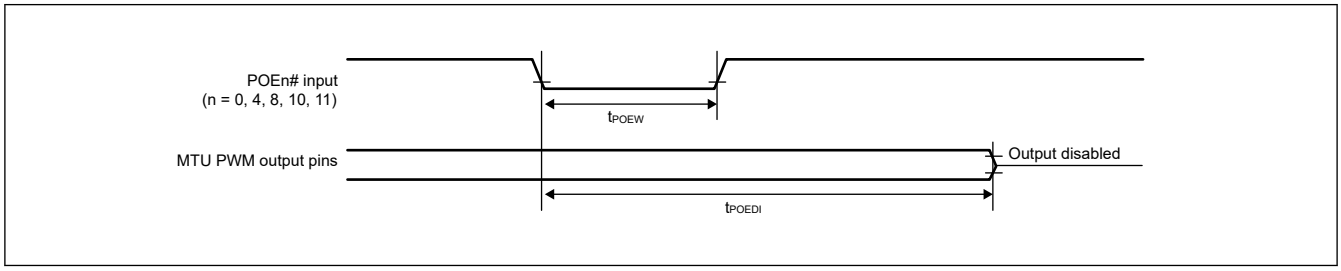
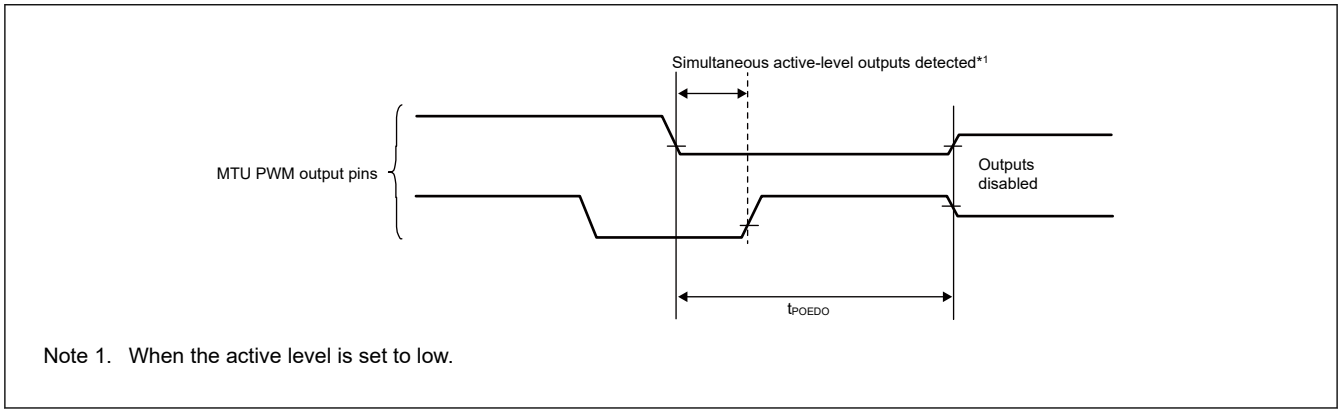


Figure 2.26 Output disable time for POE in response to transition of the POEn# signal level



Note 1. When the active level is set to low.

Figure 2.27 Output disable time for POE in response to the simultaneous conduction of output pins

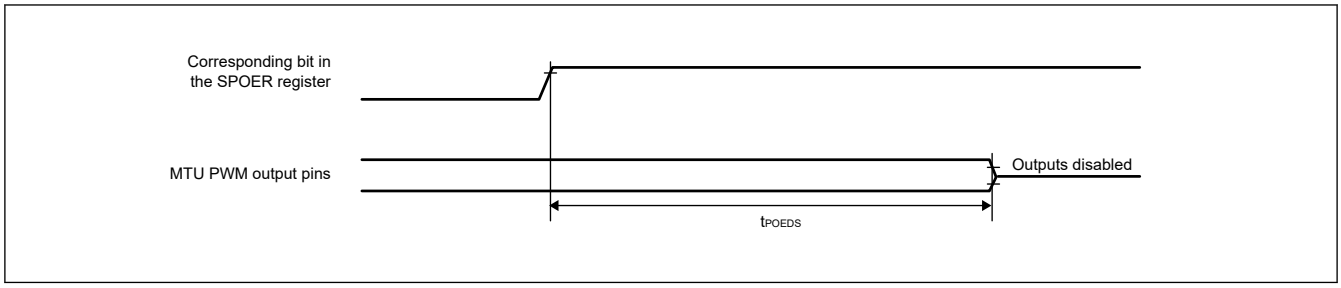


Figure 2.28 Output disable time for POE in response to the register setting

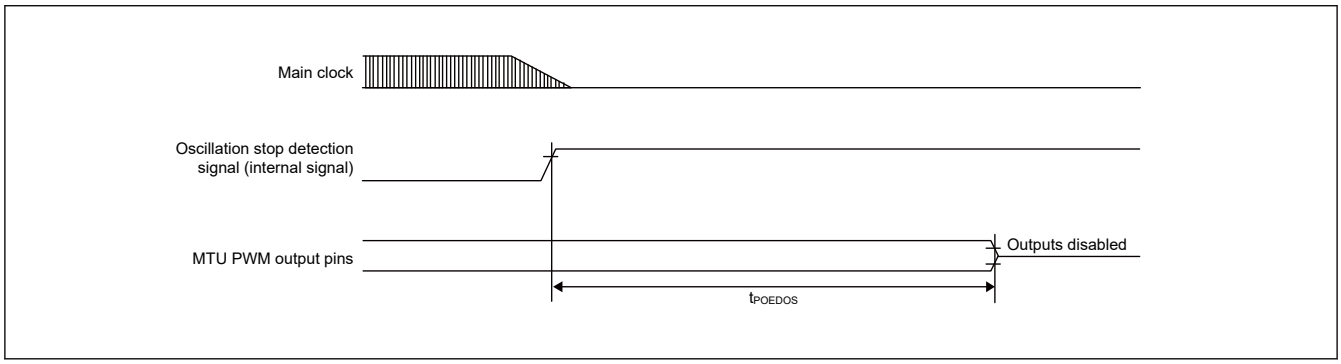


Figure 2.29 Output disable time for POE in response to the oscillation stop detection

2.5.5.5 GPT Timing

Table 2.26 GPT timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	2.5	—	t_{PHcyc}	Figure 2.30
		Both-edge setting		3.5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	2.5	—	t_{PHcyc}	Figure 2.31
		Both-edge setting		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKM cycle (Other channels)

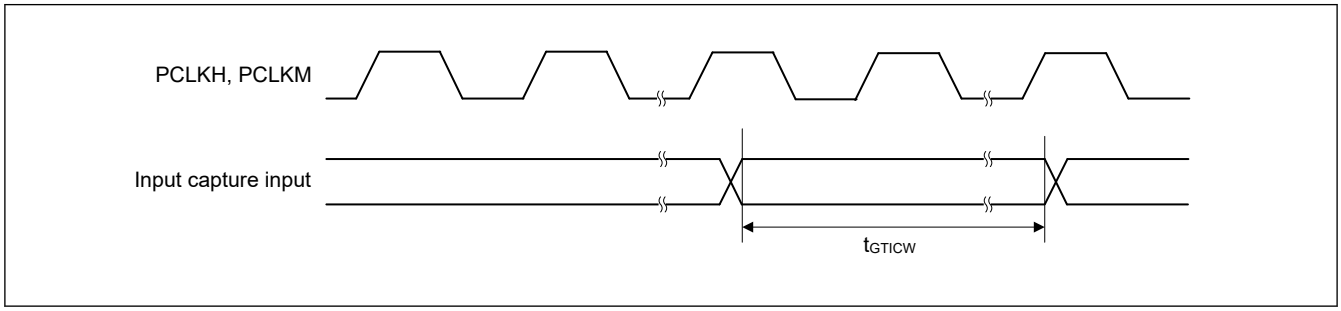


Figure 2.30 GPT input capture input timing

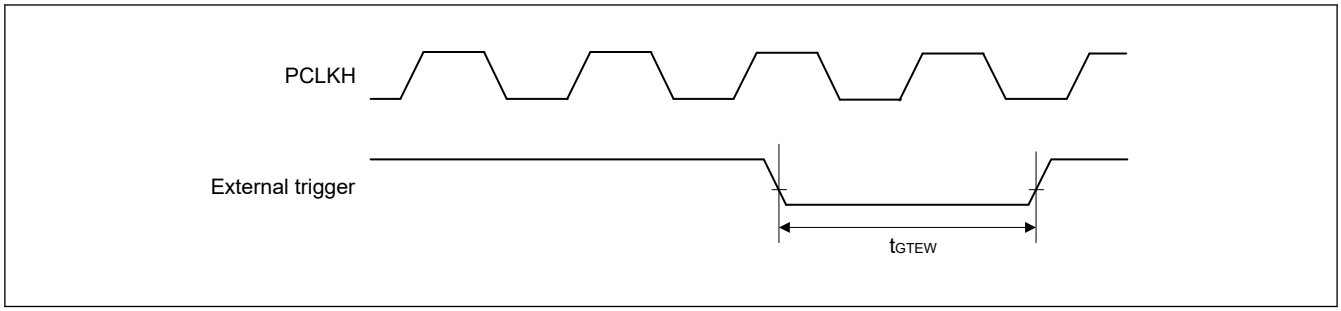


Figure 2.31 GPT external trigger input timing

2.5.5.6 POEG Timing

Table 2.27 POEG timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	2.5	—	t_{PHcyc}	Figure 2.32
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	3 × PCLKH + 0.1	µs	Figure 2.33
		Detection of the output stopping signal from GPT (dead time error, simultaneous high output, or simultaneous low output)	t_{POEGDO}	—	0.1	µs	Figure 2.34
		Register setting	t_{POEGDS}	—	PCLKH + 0.1	µs	Figure 2.35
		Oscillation stop detection	$t_{POEGDOS}$	—	74	µs	Figure 2.36

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKL cycle (Other channels)

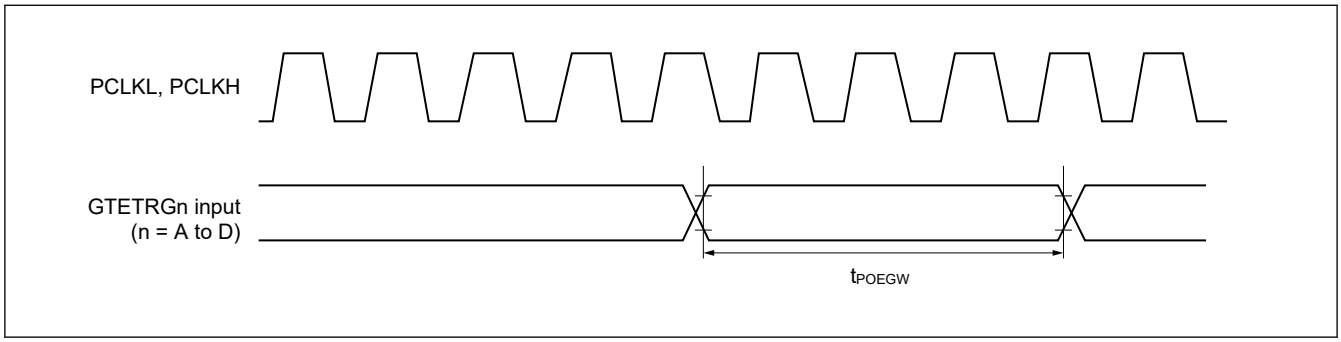


Figure 2.32 POEG input timing

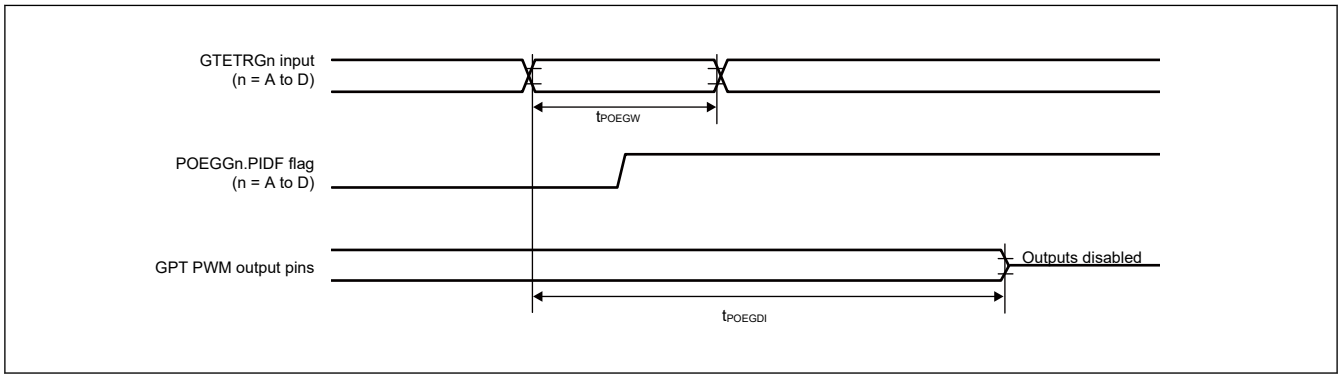
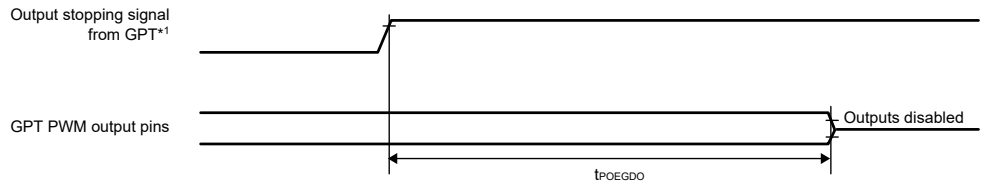


Figure 2.33 Output disable time for POEG via detection flag in response to the input level detection of the GTETRGn pin



Note 1. GPTn.GTST.DTEF (dead time error flag), GPTn.GTST.OABLF (simultaneous low out flag), or GPTn.GTST.OABHF (simultaneous high output flag)

Figure 2.34 Output disable time for POEG in response to detection of the output stopping signal from GPT

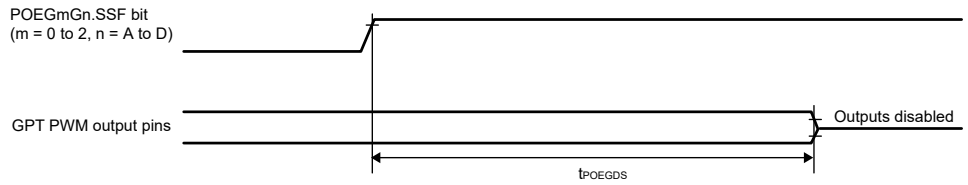


Figure 2.35 Output disable time for POEG in response to the register setting

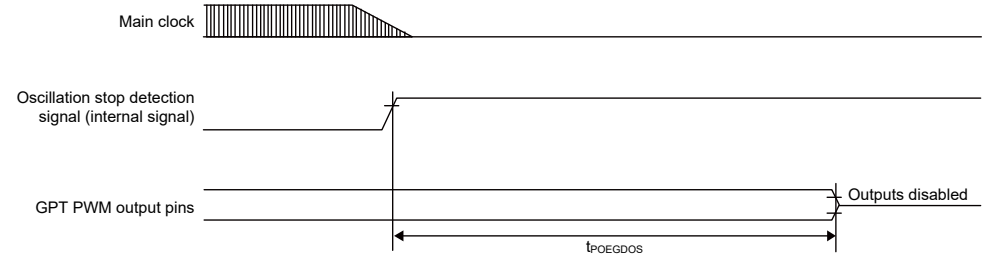


Figure 2.36 Output disable time for POEG in response to the oscillation stop detection

2.5.5.7 A/D Converter Trigger Timing

Table 2.28 A/D converter trigger timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
A/D converter	A/D converter trigger input pulse width	ADTRG0#, ADTRG1#, ADTRG2#	t_{TRGW}	1.5	—	$t_{PCLKLcyc}$	Figure 2.37

Note 1. $t_{PCLKLcyc}$: PCLKL cycle

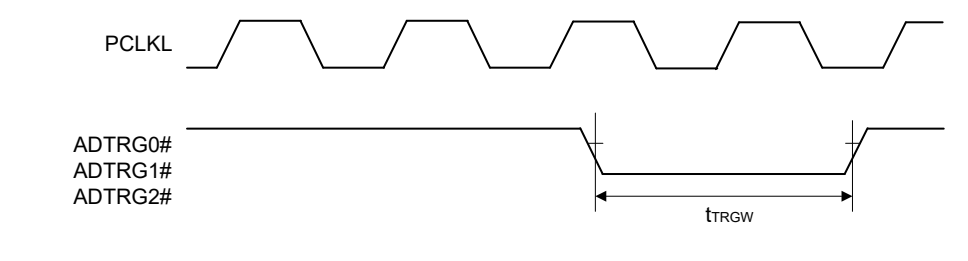


Figure 2.37 A/D converter trigger input timing (ADTRG0#, ADTRG1#, ADTRG2#)

2.5.5.8 SCI, SCIE Timing

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (except Simple I2C)

Table 2.29 SCI, SCIE timing (1 of 2)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
SCI, SCIE (Asynchronous)	Input clock cycle	t_{Scyc}	4	—	$t_{PSCIcyc}$	Figure 2.38
	Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time	t_{SCKr}	—	3	ns	
	Input clock fall time	t_{SCKf}	—	3	ns	
	Output clock cycle	t_{Scyc}	6	—	$t_{PSCIcyc}$	
	Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	t_{SCKr}	—	4	ns	
	Output clock fall time	t_{SCKf}	—	4	ns	
SCI (Simple I2C, Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.39
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	2 × NF_{cyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
SCI (Simple I2C, Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.39
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	2 × NF_{cyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 2.29 SCI, SCIE timing (2 of 2)

Parameter			Symbol	Min.	Max.	Unit	Reference figure
SCI (Clock sync, Simple SPI) SCIE (Clock sync)	SCK output clock cycle (master)		t_{SPcyc}	2*2	65536	$t_{PSCIcyc}$	Figure 2.40 to Figure 2.45
	SCK input clock cycle (slave)			2*2	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKR}, t_{SPCKF}	—	4	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		3	—		
	Data input hold time	Internal clock	t_H	3	—	ns	
		External clock		3	—		
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	12		
	Data output hold time	Internal clock	t_{OH}	-3	—	ns	
		External clock		0	—		
	Data rise/fall time		t_{DR}, t_{DF}	—	4	ns	
	Slave access time	Internal clock	t_{SA}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12		
	Slave output release time	Internal clock	t_{REL}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12		
SCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}, t_{SSF}	—	3	ns	

Note: $t_{PSCIcyc}$: PCLKSCIn cycle

Note 1. $N_{Fcyc} = 4^n \times 2^{m-1} \times t_{PSCIcyc}$
n: CCR2.CKS[1:0] (n = 0, 1, 2, 3)
m: CCR1.NFCS[2:0] (m = 1, 2, 3, 4)

Note 2. In case of PCLKSCIn = 125 MHz, Min. is 4.

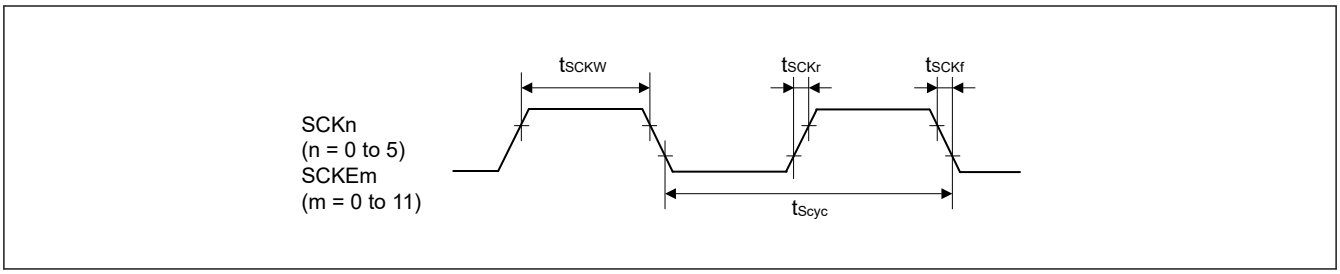
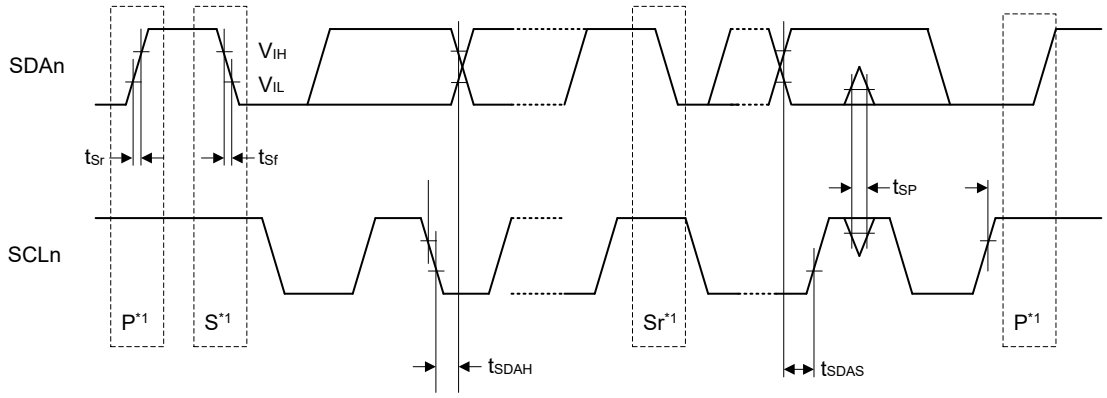


Figure 2.38 SCK clock input/output timing



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.39 SCI simple I2C mode timing

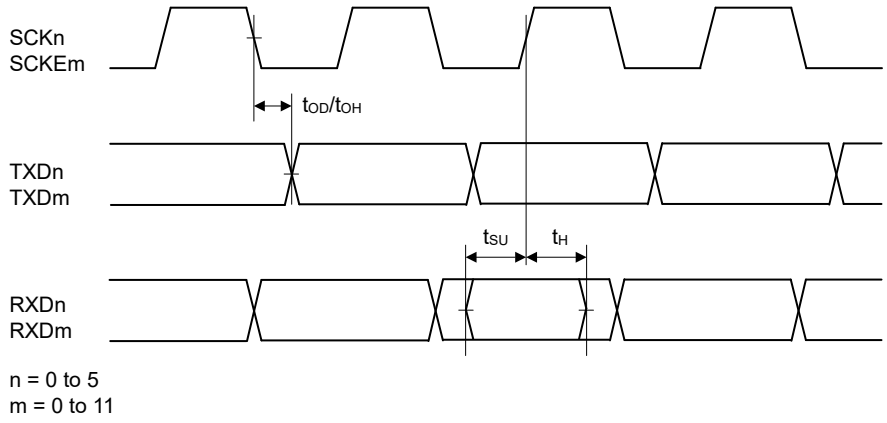
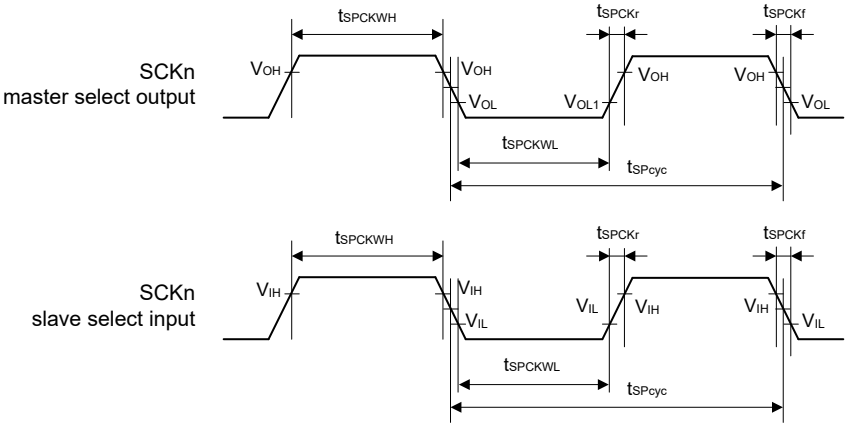


Figure 2.40 SCI input/output timing in clock synchronous mode



V_{OH} = 0.7 × VCC33, V_{OL} = 0.3 × VCC33, V_{IH} = 0.7 × VCC33, V_{IL} = 0.3 × VCC33

Figure 2.41 SCI simple SPI mode clock timing

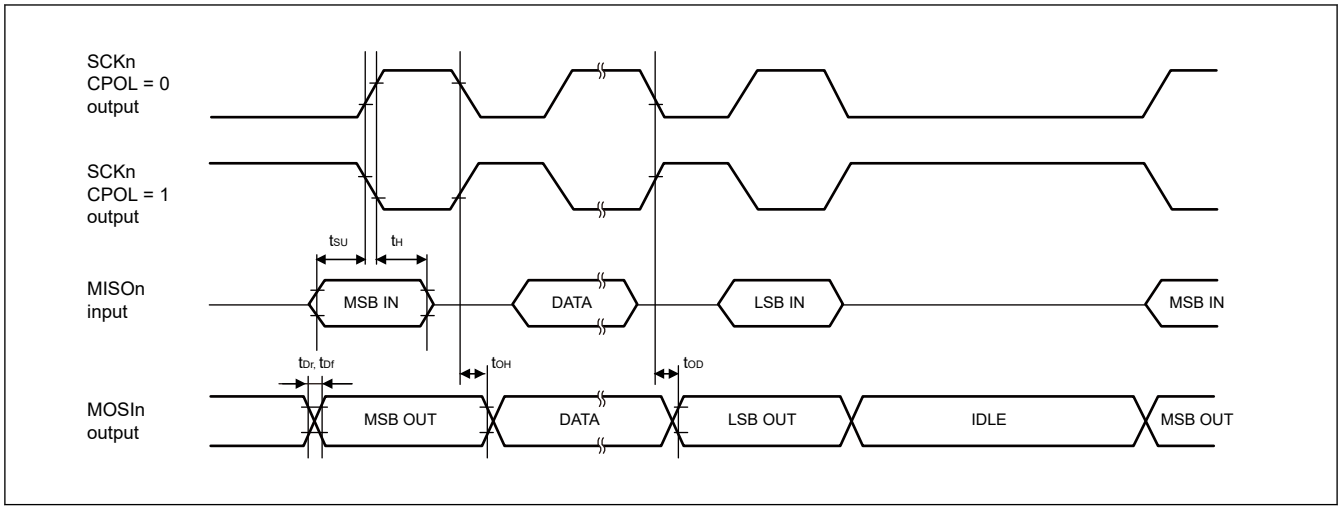


Figure 2.42 SCI simple SPI mode timing for master when CPHA = 0

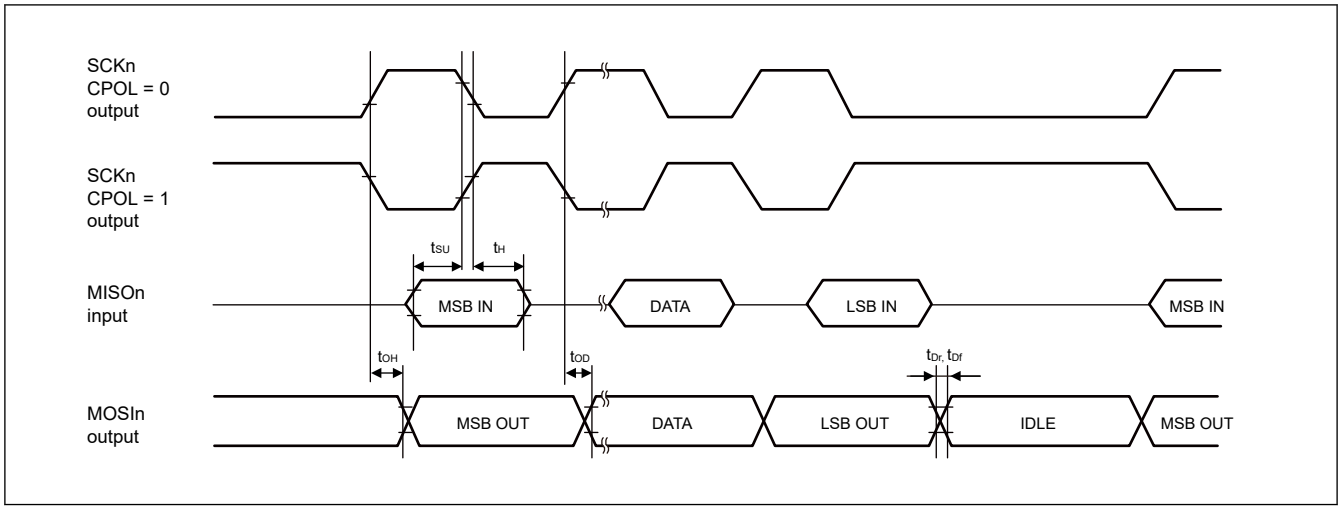


Figure 2.43 SCI simple SPI mode timing for master when CPHA = 1

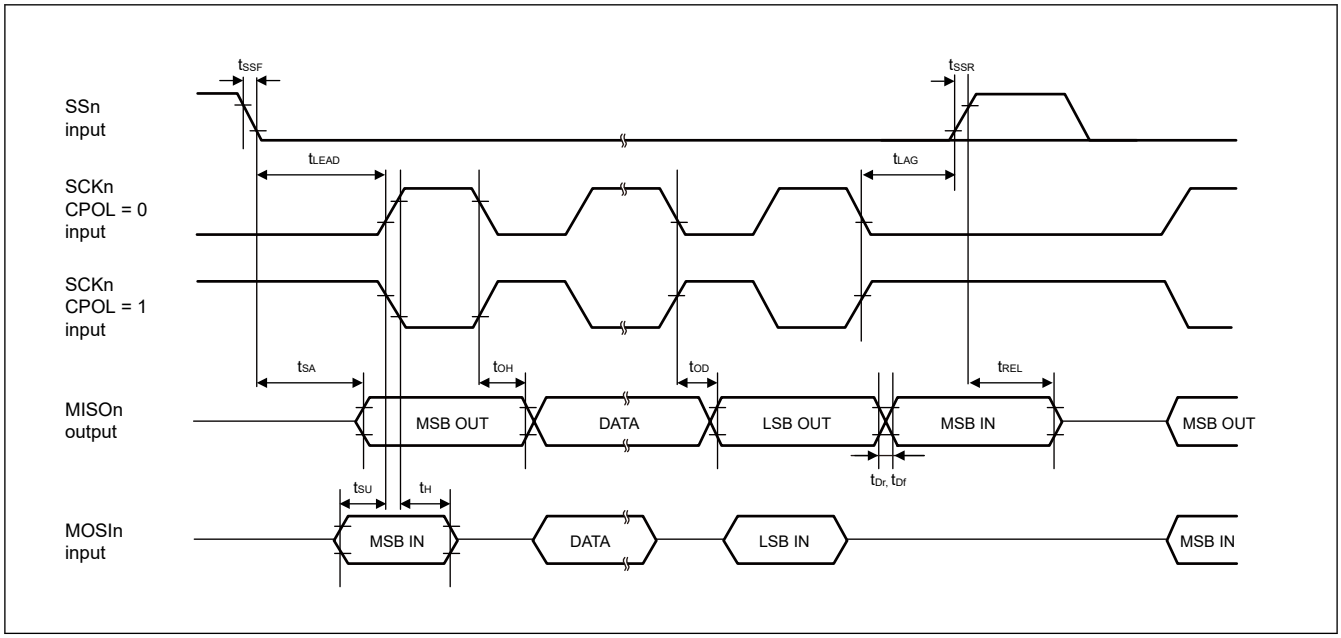


Figure 2.44 SCI simple SPI mode timing for slave when CPHA = 0

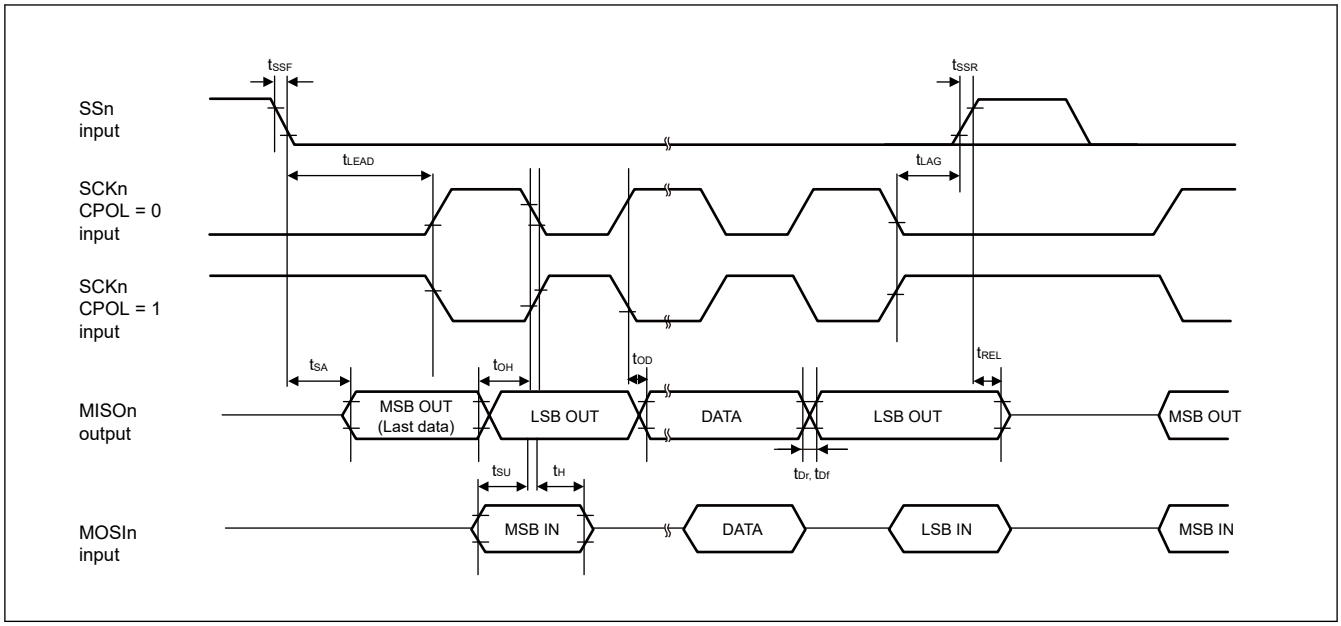


Figure 2.45 SCI simple SPI mode timing for slave when CPHA = 1

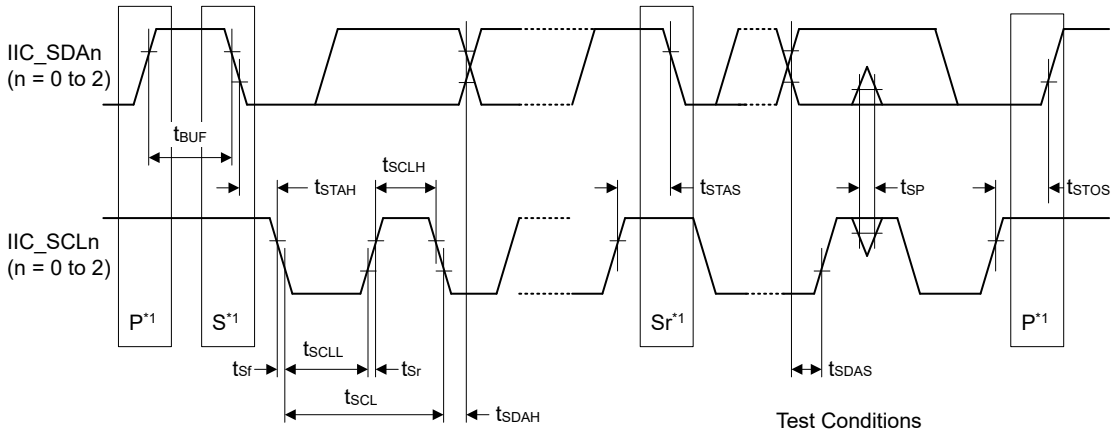
2.5.5.9 IIC Timing

Conditions: V_{OL} = 0.4 V, I_{OL} = 4 mA

Table 2.30 IIC timing

Parameter		Symbol	Min.*1 *2	Max.*1 *2	Unit	Reference figure
IIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.46
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc}: IIC internal reference clock (IICΦ) cycle
Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.
Note 4. The minimum values are not specified for t_{sr} and t_{sf} in Fast-mode.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.46 IIC bus interface input/output timing

2.5.5.10 CANFD Timing

Table 2.31 CANFD timing

Parameter		Symbol	CAN		CANFD		Unit	Reference figure
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}	—	100	—	50	ns	Figure 2.47
	Transmission rate	—	—	1	—	8	Mbps	

Note: Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

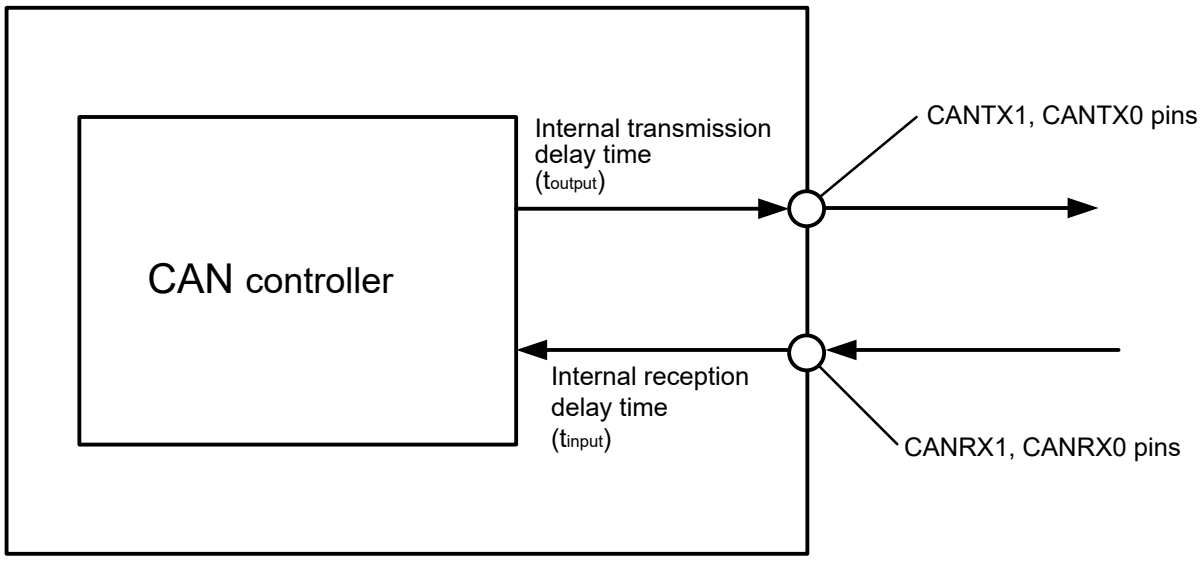


Figure 2.47 CAN interface condition

2.5.5.11 SPI Timing

Table 2.32 SPI timing (1 of 2)

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF

Parameter		Symbol	Min.*1	Max.*1	Unit*1	Reference figure
RSPCK clock cycle	Master	t_{SPcyc}	2^{*5}	4096	t_{SPIcyc}	Figure 2.48
	Slave		2^{*5}	4096		
RSPCK clock high level pulse width	Master	t_{SPCKWH}	(t_{SPcyc} − t_{SPCKr} − t_{SPCKf}) / 2 − 2.5	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock low level pulse width	Master	t_{SPCKWL}	(t_{SPcyc} − t_{SPCKr} − t_{SPCKf}) / 2 − 2.5	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock rising/falling time	Output	t_{SPCKr}, t_{SPCKf}	—	4	ns	
	Input		—	1	ns	
Data input setup time	Master	t_{SU}	5	—	ns	Figure 2.49 to Figure 2.55
	Slave		3	—		
Data input hold time	Master	t_H	3	—	ns	
	Slave		3	—		
SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} − 3^{*2}	N × t_{SPcyc} + 3^{*2}	ns	Figure 2.49 to Figure 2.52
	Slave		4	—	t_{SPIcyc}	
SSL hold time	Master	t_{LAG}	N × t_{SPcyc} − 3^{*3}	N × t_{SPcyc} + 3^{*3}	ns	
	Slave		4	—	t_{SPIcyc}	
Continuous transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{SPIcyc}	8 × t_{SPcyc} + 2 × t_{SPIcyc}	ns	
	Slave		t_{SPcyc} + 5 × t_{SPIcyc}	—		
TI-SSP SS input setup time		t_{TISS}	3	—	ns	Figure 2.53 to Figure 2.55
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M^{*4}	—	t_{SPIcyc}	
TI-SSP Master SS output delay		t_{TISSOD}	-3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	12	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	8	ns	
Data output delay time	Master	t_{OD}	—	3	ns	Figure 2.49 to Figure 2.55
	Slave		—	12	ns	
Data output hold time	Master	t_{OH}	-3	—	ns	
	Slave		3	—		
MOSI, MISO rising/falling time	Output	t_{Dr}, t_{Df}	—	4	ns	
	Input		—	1	µs	
SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	4	ns	Figure 2.49, Figure 2.50
	Input		—	1	µs	

Table 2.32 SPI timing (2 of 2)

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF

Parameter	Symbol	Min.*1	Max.*1	Unit*1	Reference figure
Slave access time	t_{SA}	—	12	ns	Figure 2.51, Figure 2.52
Slave output release time	t_{REL}	—	12	ns	

Note 1. t_{SPIcyc}: PCLKSPIn cycle
Note 2. SPCKD set value + 1 (1 to 8)
Note 3. SSLND set value + 1 (1 to 8)
Note 4. SSLND set value + 2 (2 to 9)
Note 5. In case of PCLKSPIn = 125 MHz, Min. is 4.

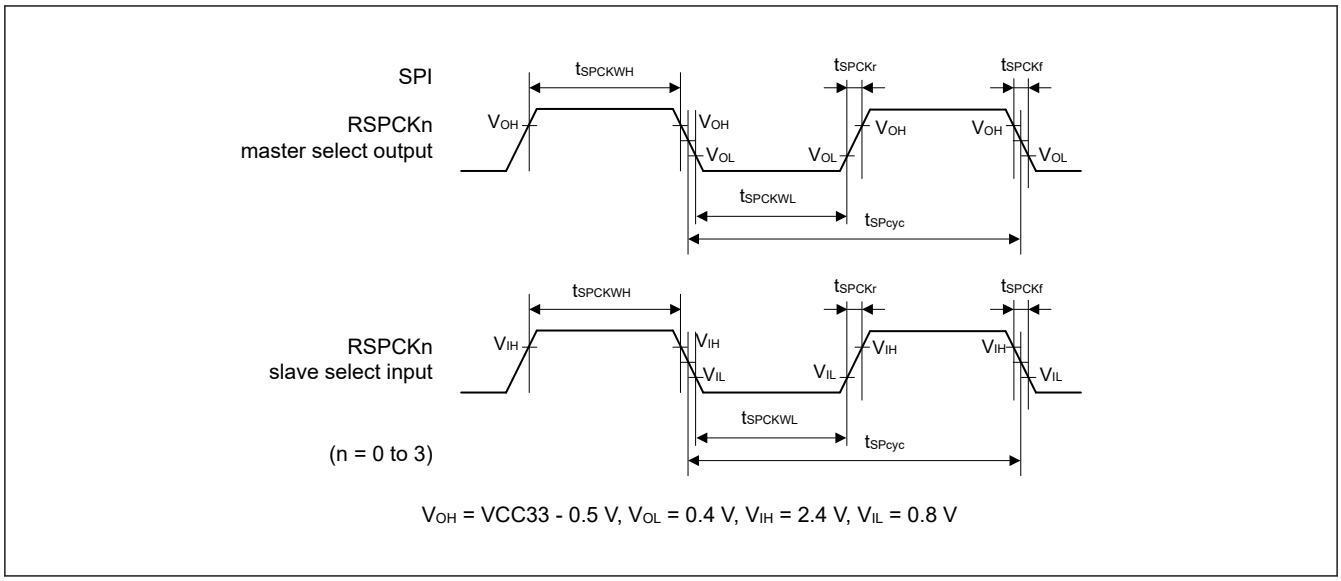


Figure 2.48 SPI clock timing

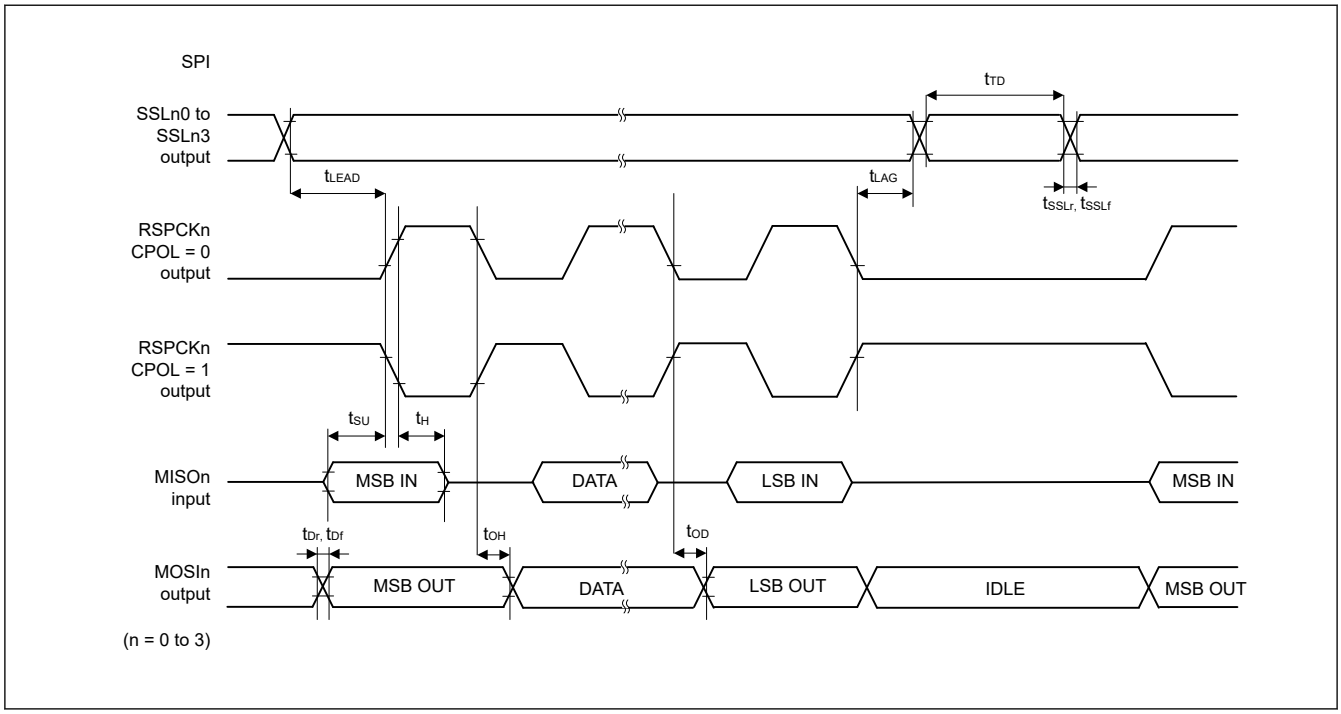


Figure 2.49 SPI timing (Master, Motorola SPI, CPHA = 0)

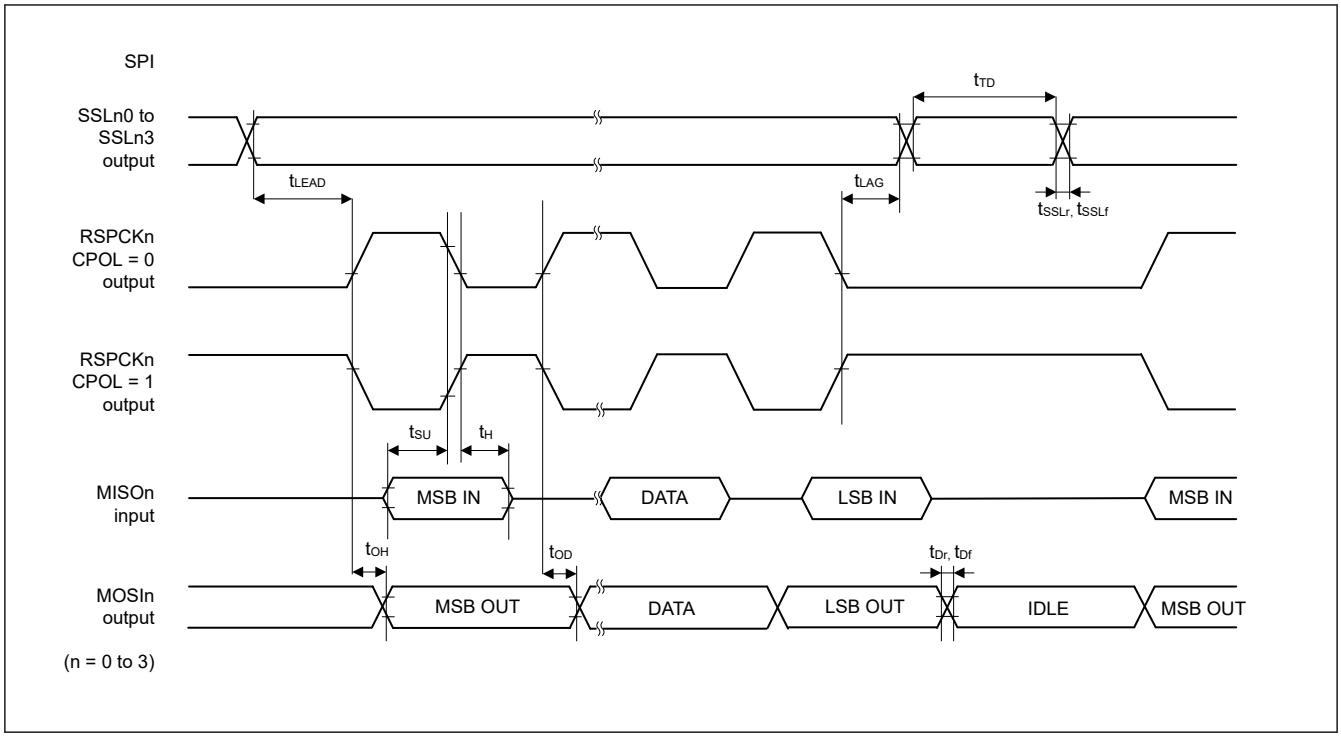


Figure 2.50 SPI timing (Master, Motorola SPI, CPHA = 1)

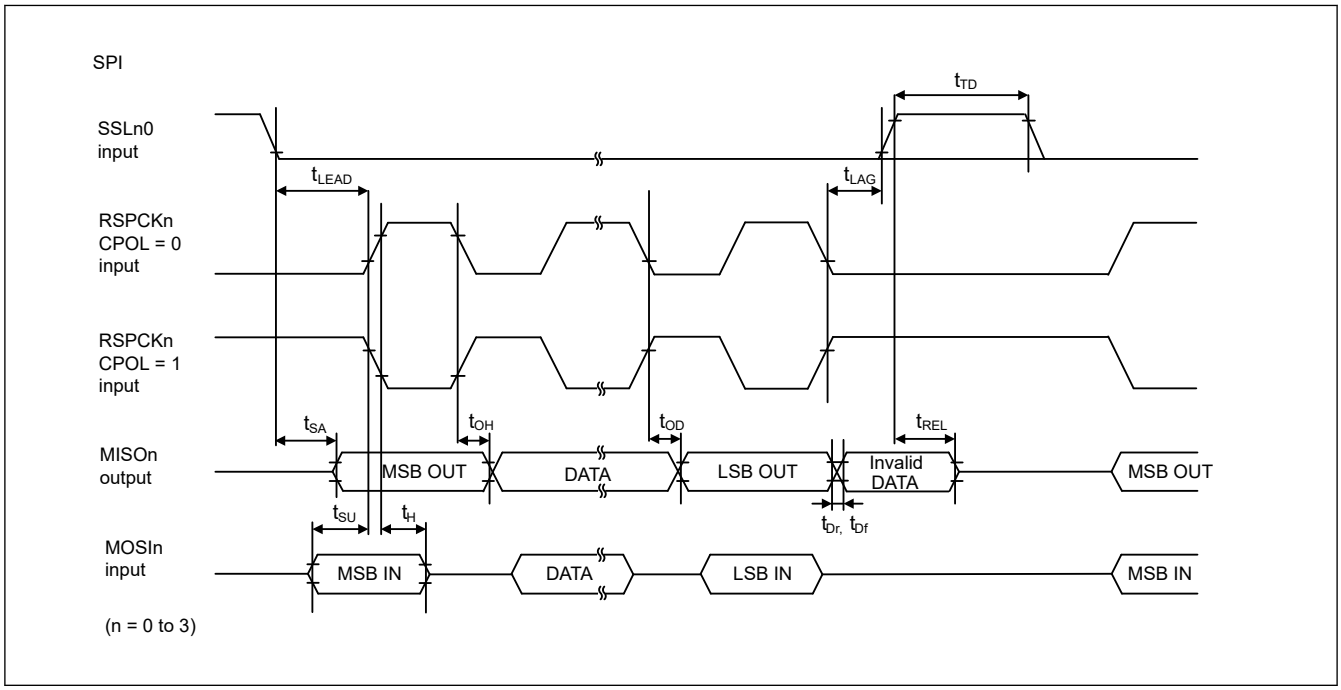


Figure 2.51 SPI timing (Slave, Motorola SPI, CPHA = 0)

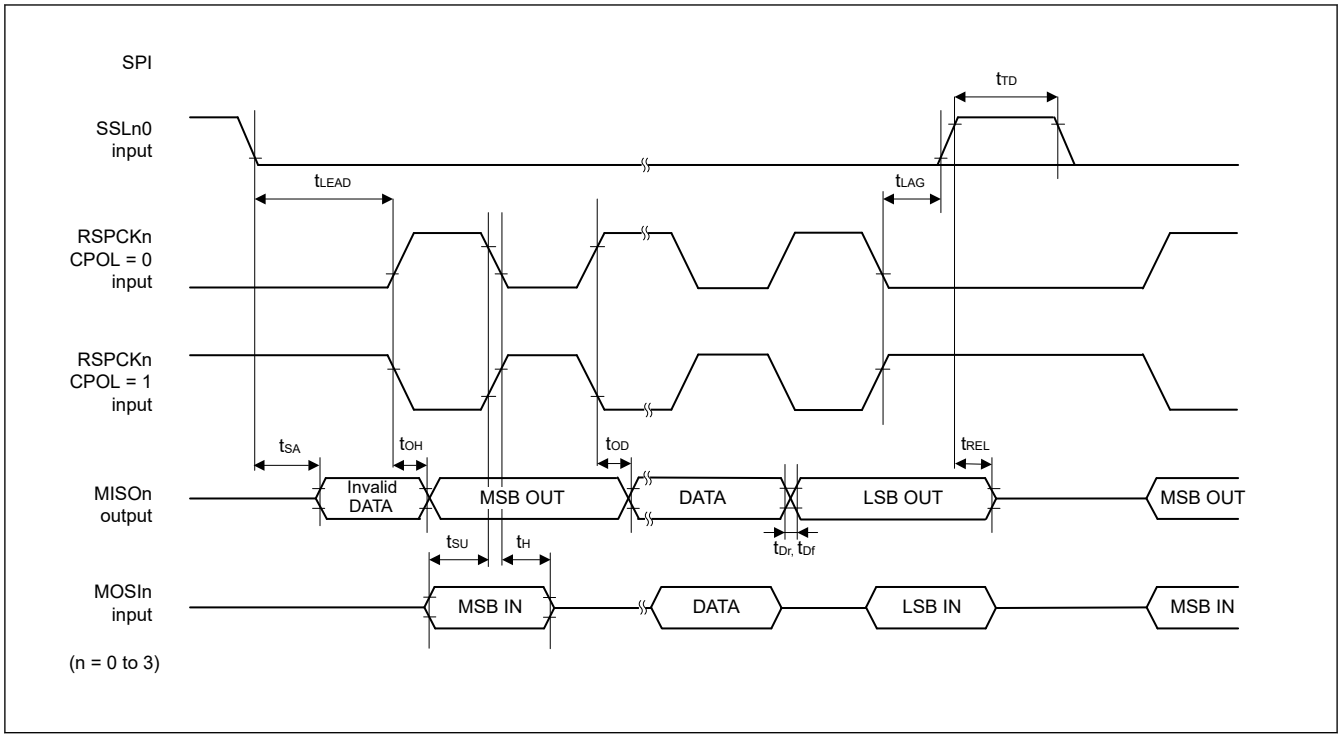


Figure 2.52 SPI timing (Slave, Motorola SPI, CPHA = 1)

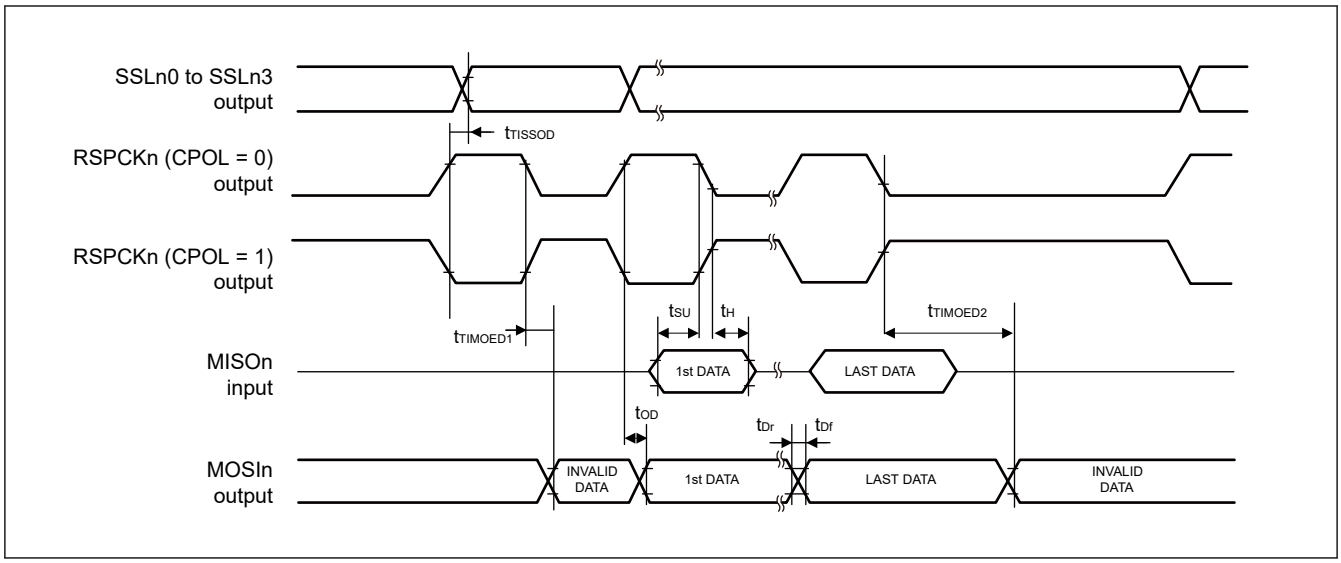


Figure 2.53 SPI timing (Master, TI SSP)

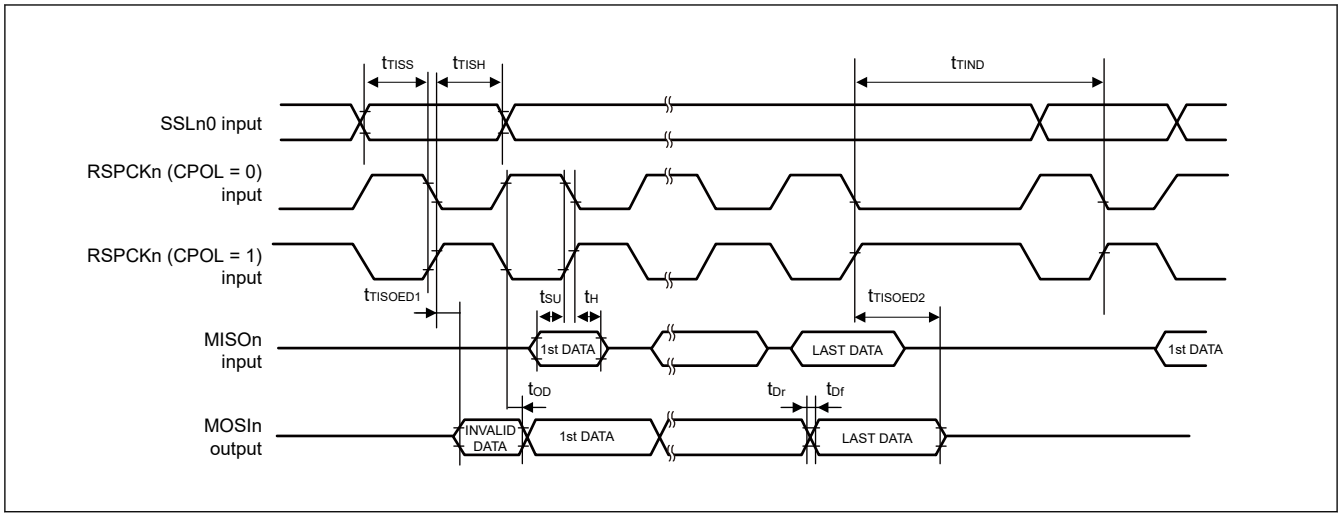


Figure 2.54 SPI timing (Slave, TI-SSP, with delay in burst transfer)

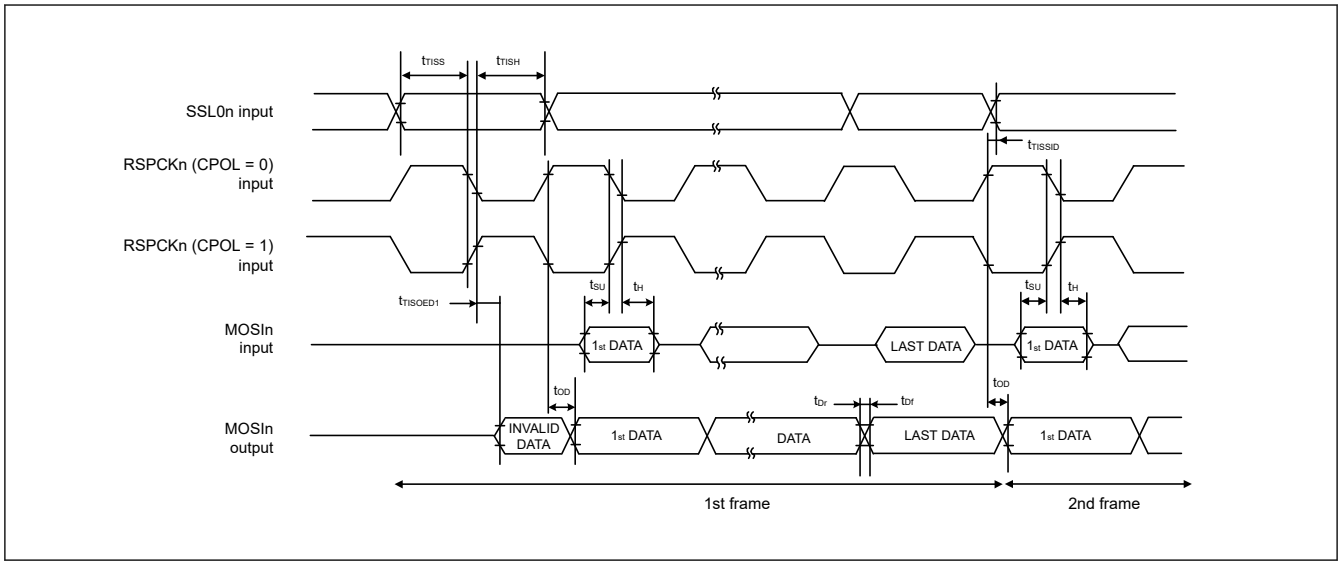


Figure 2.55 SPI timing (Slave, TI-SSP, without delay in burst transfer)

2.5.5.12 xSPI Timing

Table 2.33 xSPI timing

Conditions:
V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5, C = 15 pF (VDD1833 = 1.8 V or 3.3 V)

Parameter		Symbol	1.8 V		3.3 V		Unit	Reference figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t_{PERIOD}	7.5	—	10.0	—	ns	Figure 2.56
	DDR		7.5	—	10.0	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*2	—	0.56	—	V/ns	
Clock duty cycle distortion		t_{CKDCD}	0.0	t_{PERIOD} × 0.05	0.0	t_{PERIOD} × 0.05	ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	0.4 × VCC18	0.6 × VCC18	—	—	V	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	0.56	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.0	—	ns	Figure 2.57
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.0*3	—	2.0*3	ns	
Data output hold time		t_{OH}	-1.0	—	-2.0	—	ns	
Data output buffer off time		t_{BOFF}	-1.0	—	-2.0	—	ns	
Data input setup time (to DS)	DDR*1 *3	t_{SU}	-0.4/-0.6*2	—	-0.3	—	ns	Figure 2.58, Figure 2.59
Data input hold time (to DS)		t_{H}	t_{PERIOD} × 0.41 - 0.4/0.6*2	—	t_{PERIOD} × 0.41 - 0.3	—	ns	
Data output setup time (to CK)		t_{SUO}	0.8/1.0*2	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	0.8/1.0*2	—	1.0	—	ns	
CS low to clock high		t_{CSLCKH}	6.0/8.0*2 *4	—	8.0*4	—	ns	Figure 2.57 to Figure 2.59
Clock low to CS high		t_{CKLCSH}	6.0/8.0*2	—	8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS low to CS high		t_{DSLCSH}	6.0/8.0*2 *5	—	10.6*5	—	ns	Figure 2.60
CS high to DS tri-state		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low*8		t_{CSLDSL}	0.0	16.0*9	0.0	20.0*9	ns	
DS tri-state to CS low		t_{DSTCSL}	0.0	—	0.0	—	ns	
CK low to DS low*6		t_{CKLDSL}	—	(0.45 + e) × t_{PERIOD} − 2 *7	—	(0.45 + e) × t_{PERIOD} − 2 *7	ns	

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 01001b for 133 MHz and 01100b for 100 MHz.
Note 2. Specification at 133 MHz / Specification at 100 MHz
Note 3. These are the values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1).
Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1).
Note 5. These are the values when the t_{CKLDSL} constraint is satisfied.
Note 6. This constraint is necessary only to satisfy the t_{DSLCSH} requirement in JESD251, which specifies that t_{DSLCSH} must be at least 80% of t_{PERIOD}. Set LIOCFGCSn.CSNEGEX to the appropriate value to ensure the memory specification complies with this constraint.

Note 7. e = LIOCFGCSn.CSNEGEX
Note 8. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.
Note 9. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

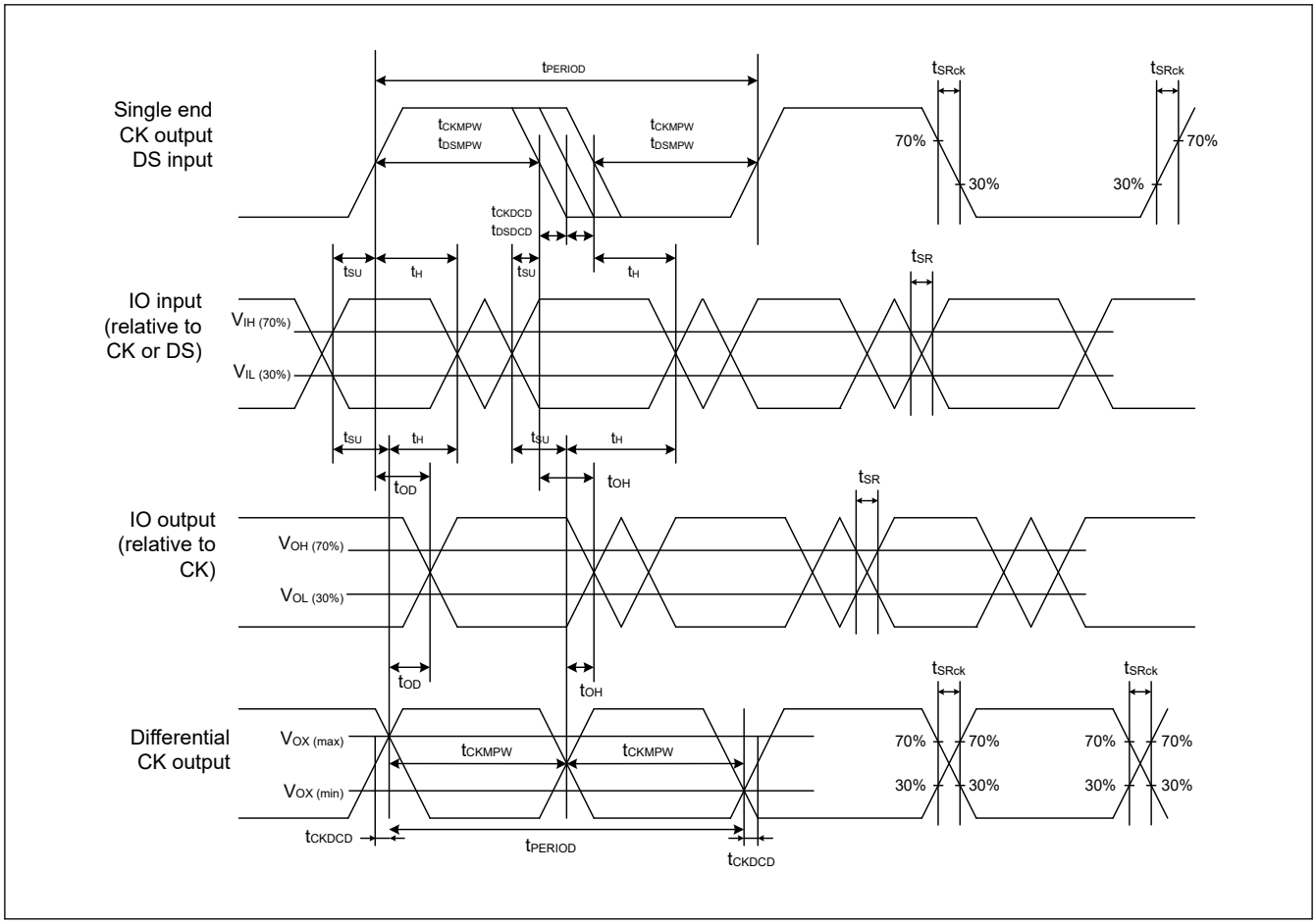


Figure 2.56 xSPI clock / DS timing

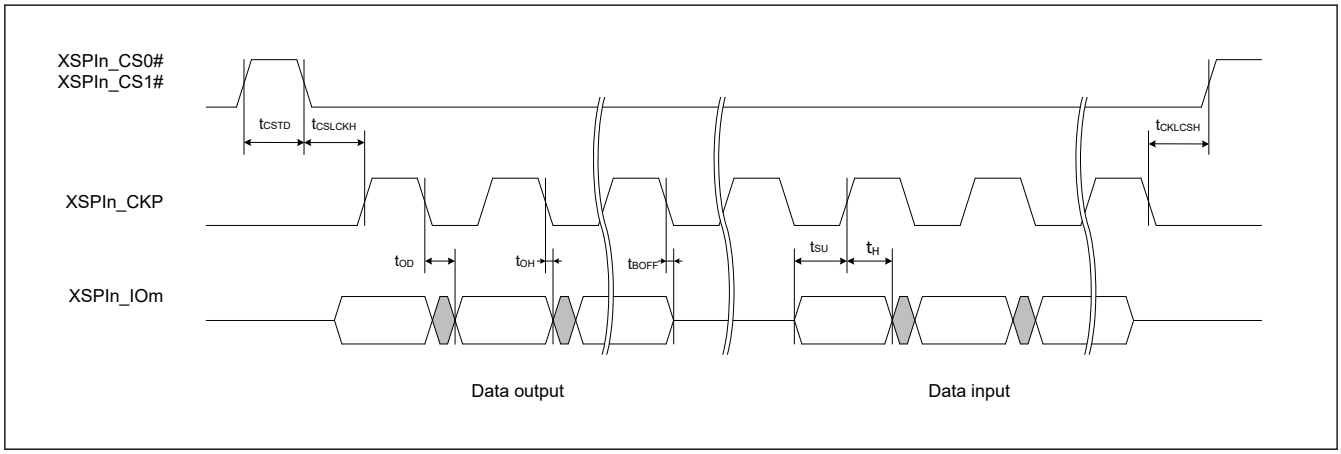


Figure 2.57 SDR transmit/receive timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

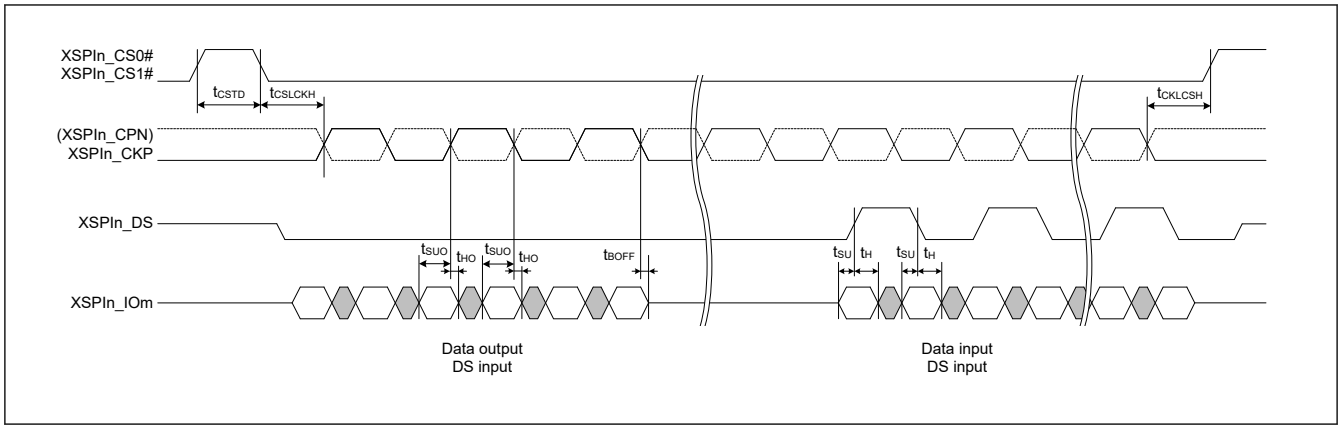


Figure 2.58 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

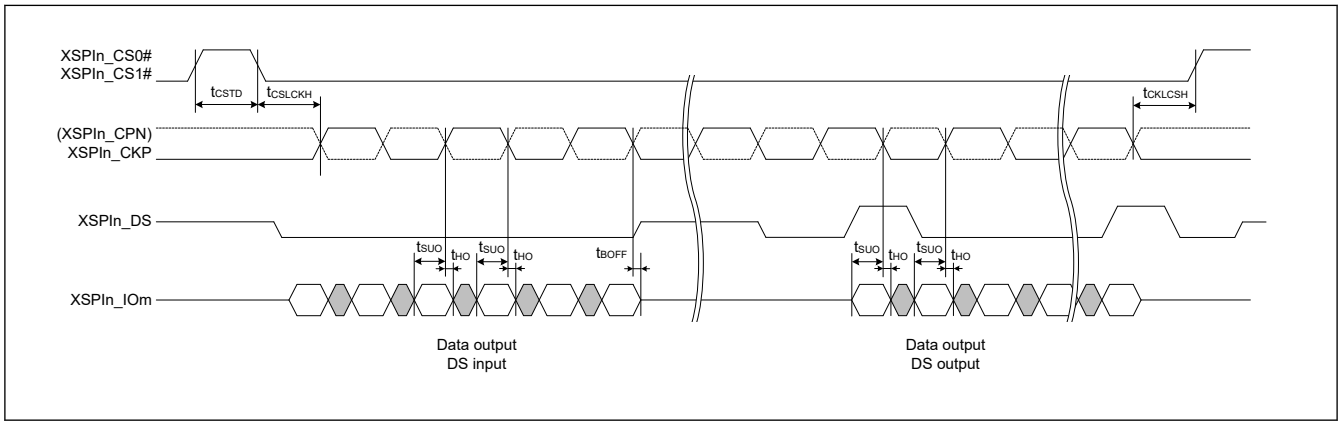


Figure 2.59 DDR transmit/receive timing (HyperRAM write)

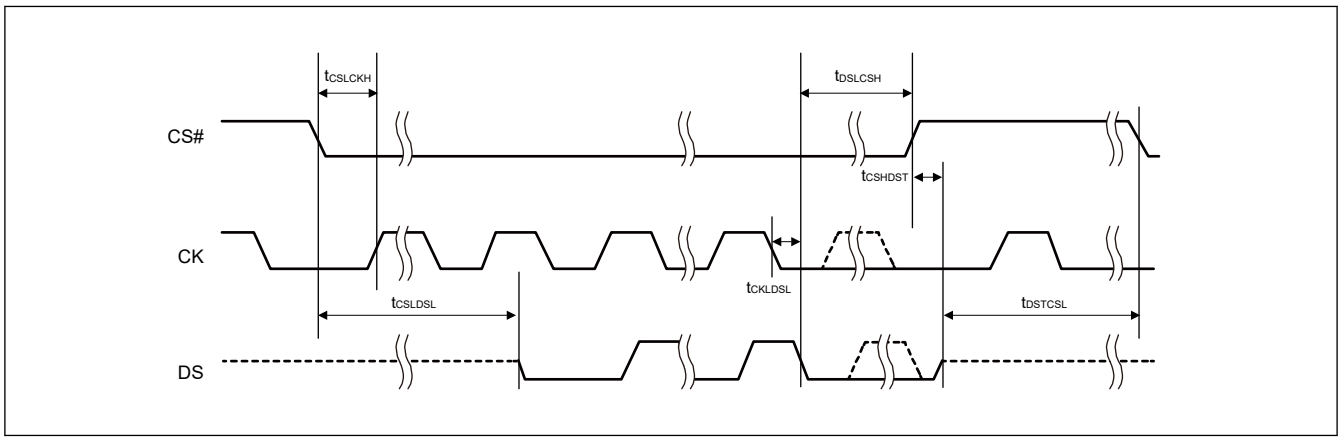


Figure 2.60 DS to CS signal timing

2.5.5.13 Delta-Sigma Interface Timing

Conditions: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF

Table 2.34 ΔΣ interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
DSMIF	Clock cycle	Master	t_{DScyc}	40	200	ns	Figure 2.61
		Slave		40	200		
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—		
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—		
	Setup time	Master	t_{SU}	15	—	ns	Figure 2.62, Figure 2.63
		Slave		5	—		
	Hold time	Master	t_H	0	—	ns	
		Slave		5	—		

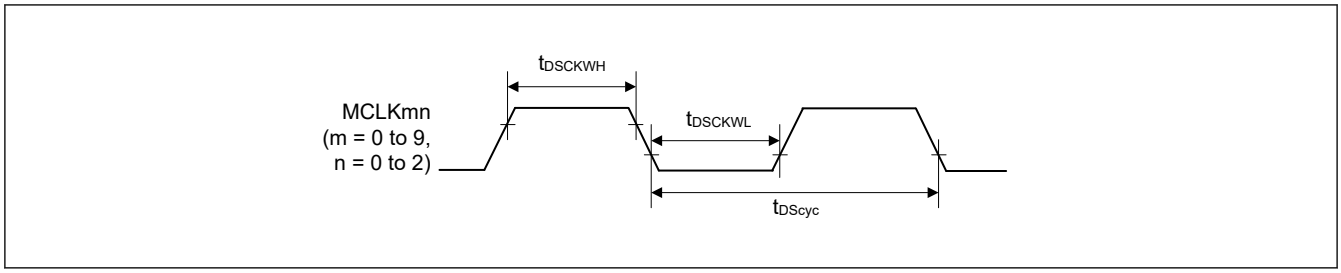


Figure 2.61 Clock input/output timing

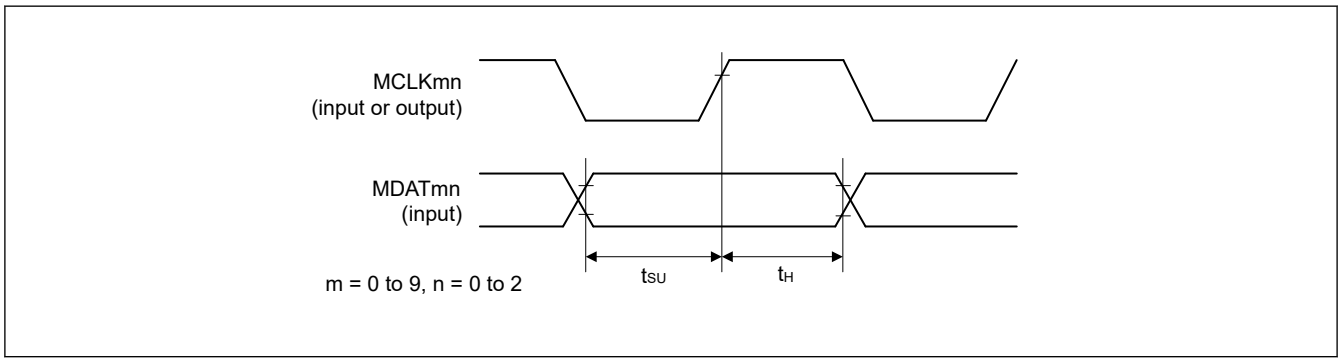


Figure 2.62 Reception timing (MCLKn rising synchronous)

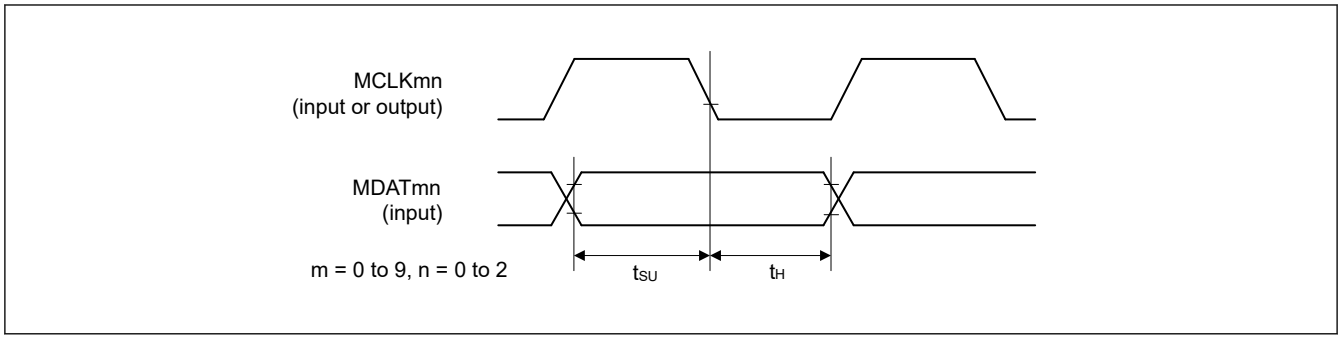


Figure 2.63 Reception timing (MCLKn falling synchronous)

2.5.5.14 Ethernet Interface Timing

Conditions:

V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5, C = 15 pF (RGMII, VDD1833 = 1.8 V)*1

V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5, C = 25 pF (RMII, VDD1833 = 3.3 V)

V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5, C = 30 pF (MII, VDD1833 = 3.3 V)

Table 2.35 Ethernet interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
Ethernet (RGMII)	ETHn_TXCLK, ETHn_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	Figure 2.64
		100 Mbps		36	44		
		10 Mbps		360	440		
	ETHn_TXCLK, ETHn_RXCLK frequency	1 Gbps	—	125 − 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 − 50 ppm	25 + 50 ppm		
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm		
	ETHn_TXCLK, ETHn_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps		40	60		
	ETHn_TXCLK, ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL), ETHn_RXCLK, ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) rise/fall time		t_{RGMIIr}, t_{RGMIIf} *1	—	0.75	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) to ETHn_TXCLK output skew		$t_{RGMIIos}$	−0.5	0.5	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) setup time		t_{RGMIIs}	1	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) hold time		t_{RGMIIh}	1	—	ns	
Ethernet (RMII)	ETHn_RXCLK cycle time		t_{RMIIck}	20	—	ns	Figure 2.65
	ETHn_RXCLK frequency Typ. 50 MHz		—	50 − 50 ppm	50 + 50 ppm	MHz	
	ETHn_RXCLK duty		—	35	65	%	
	ETHn_RXCLK rise/fall time		$t_{RMIIckr}$, $t_{RMIIckf}$	0.5	3.5	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN output delay time		t_{RMIId}	2.5	12	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time		t_{RMIIs}	4	—	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) hold time		t_{RMIIh}	2	—	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN, ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) rise/fall time		t_{RMIIr}, t_{RMIIf}	0.5	4	ns	
Ethernet (MII)	ETHn_TXCLK, ETHn_RXCLK cycle time	100 Mbps	t_{MIIck}	40	—	ns	Figure 2.66
		10 Mbps		400	—		
	ETHn_TXCLK, ETHn_RXCLK frequency	100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm		
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN, ETHn_TXER output delay time		t_{MIId}	1	20	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER setup time		t_{MIIs}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER hold time		t_{MIIh}	10	—	ns	

Note 1. Measurement condition of tRGMIIr and tRGMIIf is FIGURE 3 in Reduced Gigabit Media Independent Interface (RGMII) 12/10/2000 Version 1.3.

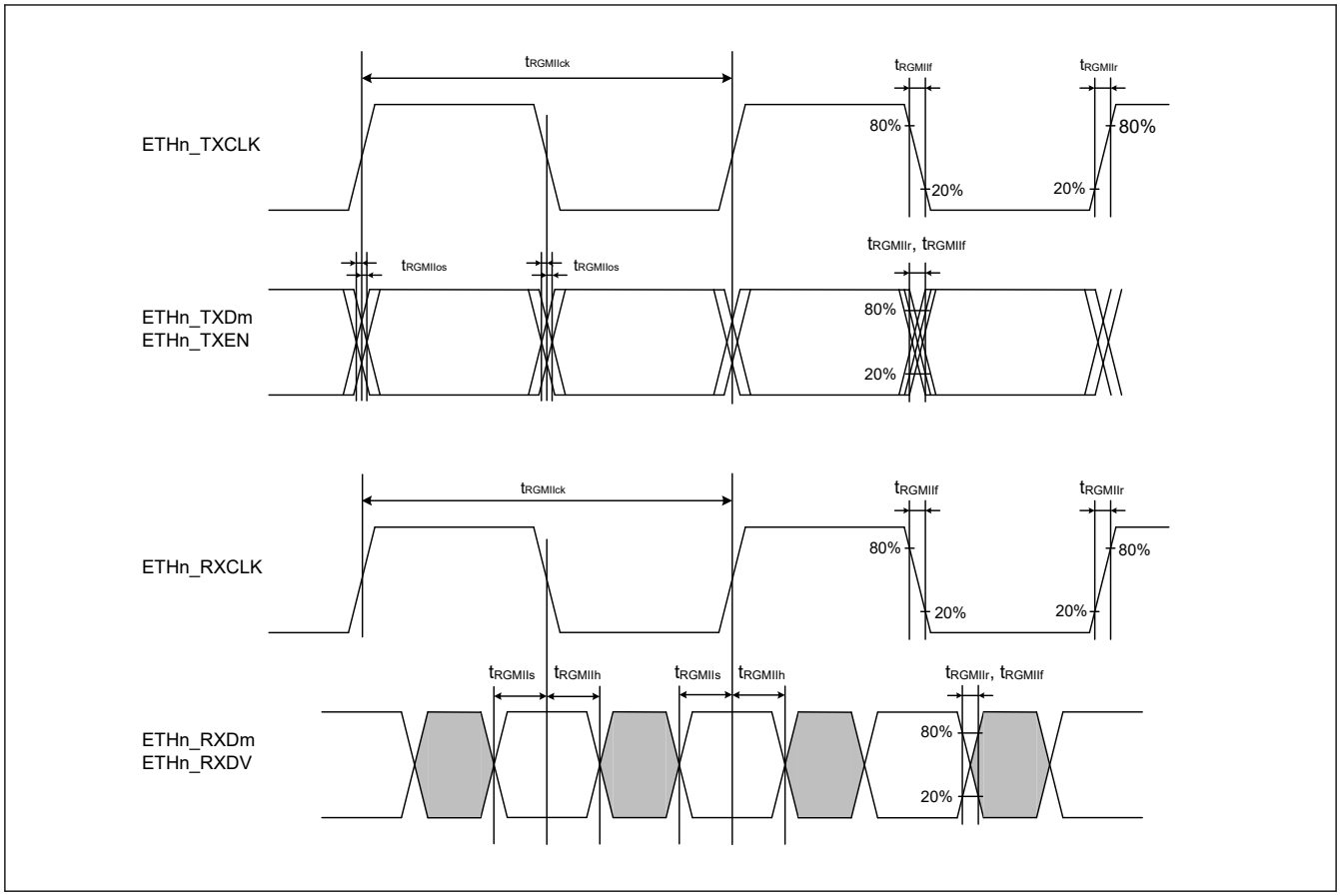


Figure 2.64 RGMII transmission and reception timing (n = 0 to 3, m = 0 to 3)

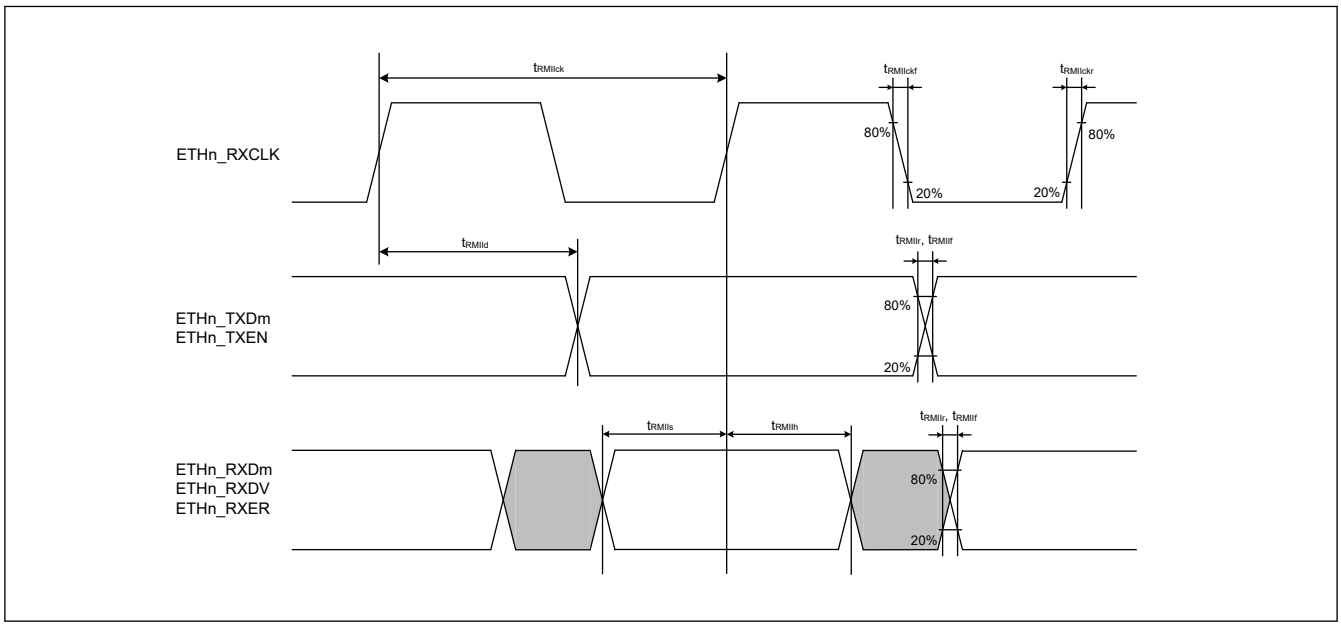


Figure 2.65 RMII transmission and reception timing (n = 0 to 3, m = 0 to 1)

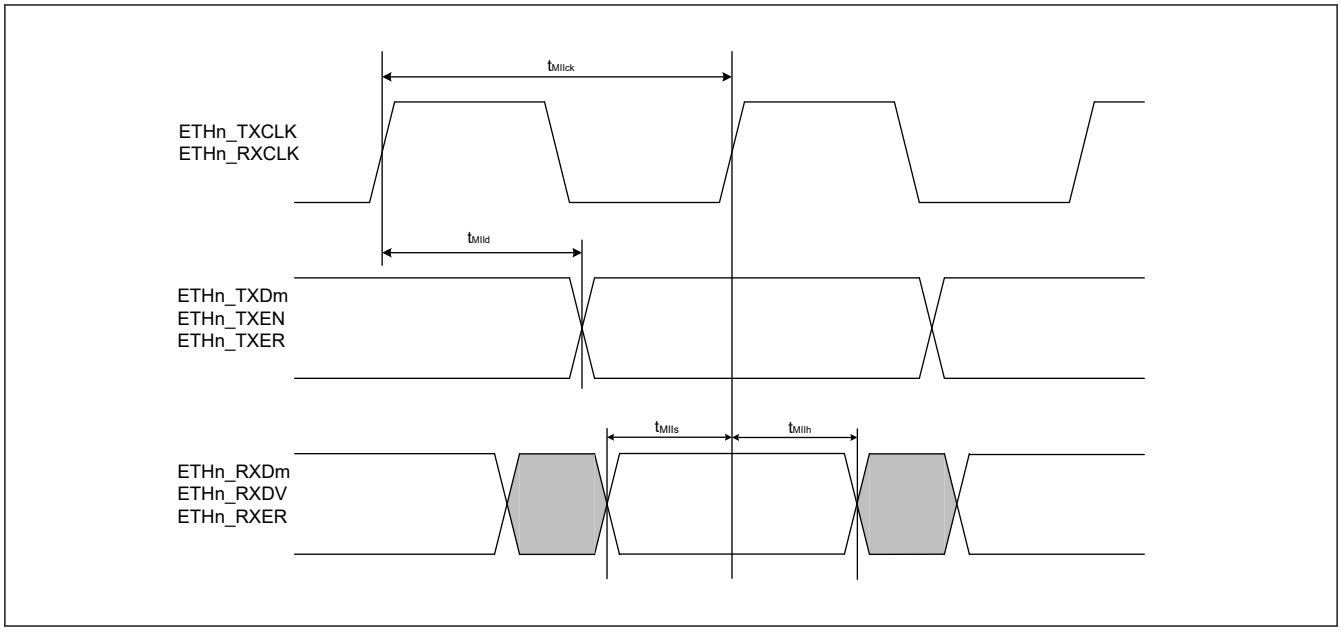


Figure 2.66 MII transmission and reception timing (n = 0 to 3, m = 0 to 3)

2.5.5.15 Serial Management Interface Timing

Conditions:

V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5, C = 30 pF (VDD1833 = 1.8 V or 3.3 V)

Table 2.36 Serial management interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
MDIO	MDC output cycle time	GMACn_MDC, ETHSW_MDC	T_{MDCck}	80	—	ns	Figure 2.67
		ESC_MDC		400	—	ns	
	MDIO output delay time (for MDC fall)*1		T_{MDIOd}	—	20	ns	
	MDIO input setup time (for MDC rise)	GMACn_MDC, ETHSW_MDC	T_{MDIOs}	18	—	ns	
		ESC_MDC		70	—	ns	
	MDIO input hold time (for MDC rise)		T_{MDIOh}	0	—	ns	

Note 1. The output timing from ETHSW is based on the rising edge of MDC, and the output delay can be set in the register.

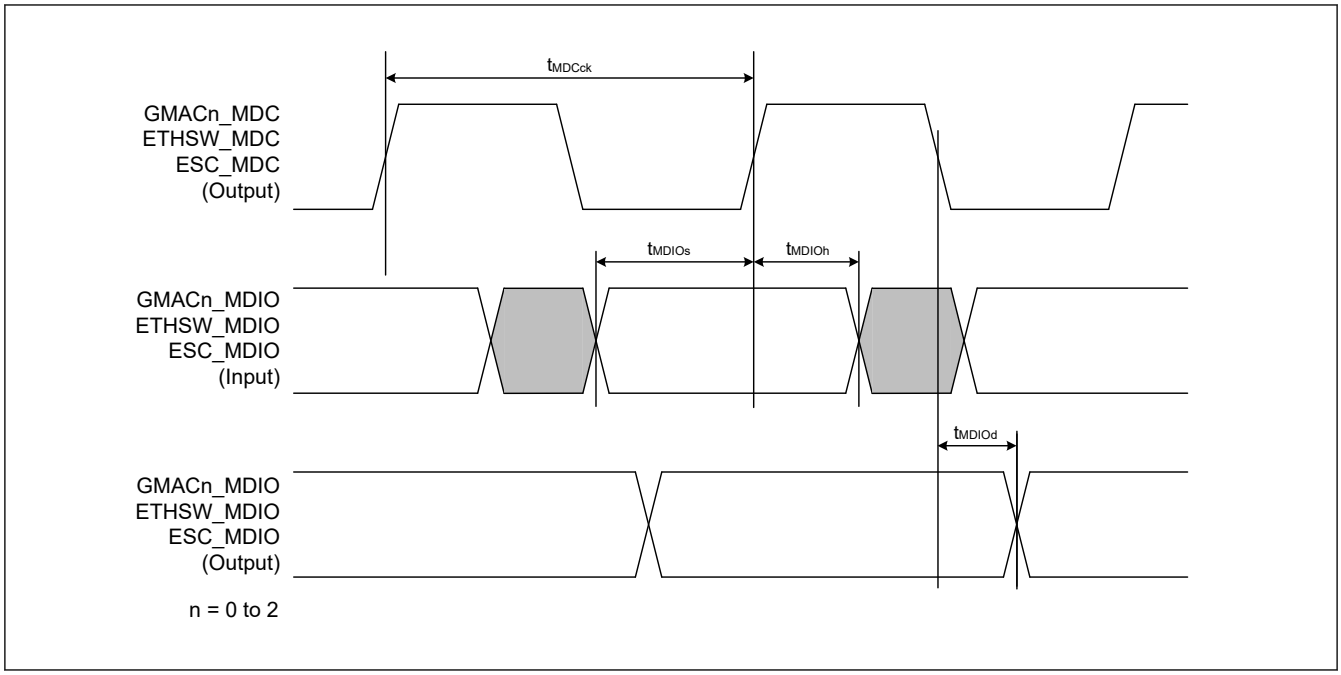


Figure 2.67 Serial management interface timing

2.5.5.16 SHOSTIF Timing

Conditions:

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF

Table 2.37 SHOSTIF timing

Parameter		Symbol	Min.	Max.	Unit	Reference figure
SHOSTIF	Clock cycle time	t_{SHck}	25	—	ns	Figure 2.68
	Clock high time	t_{CH}	0.45	0.55	t_{SHck}	
	Clock low time	t_{CL}	0.45	0.55	t_{SHck}	
	Clock rise slew rate	t_{CRT}	0.1	—	V/ns	
	Clock fall slew rate	t_{CFT}	0.1	—	V/ns	
	CS# high time	t_{CS}	2	—	t_{SHck}	Figure 2.69, Figure 2.70
	CS# active setup time	t_{CSS}	15	—	ns	
	CS# active hold time	t_{CSH}	15	—	ns	
	Data input setup time	t_{SU}	3	—	ns	
	Data input hold time	t_{HD}	10.5	—	ns	
	Clock low to output valid	t_{V}	—	15.5	ns	
	Data output hold time	t_{HO}	6	—	ns	
	Data output disable time	t_{DIS}	—	18	ns	

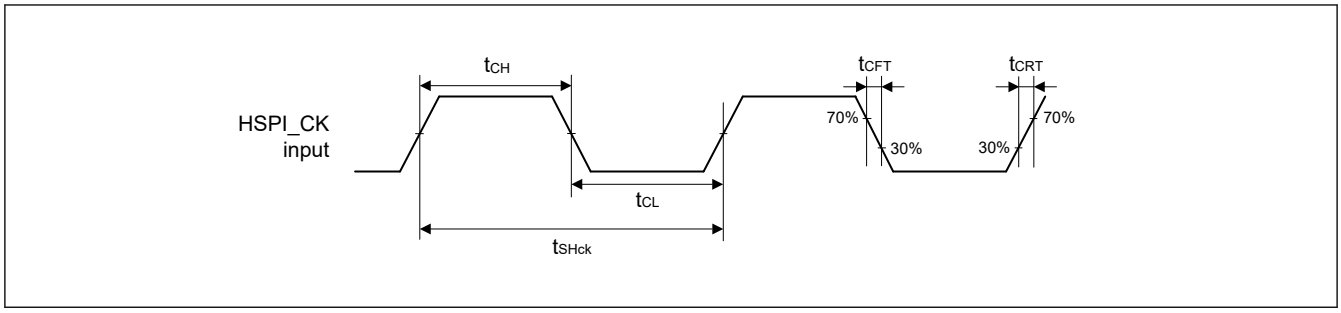


Figure 2.68 SHOSTIF clock timing

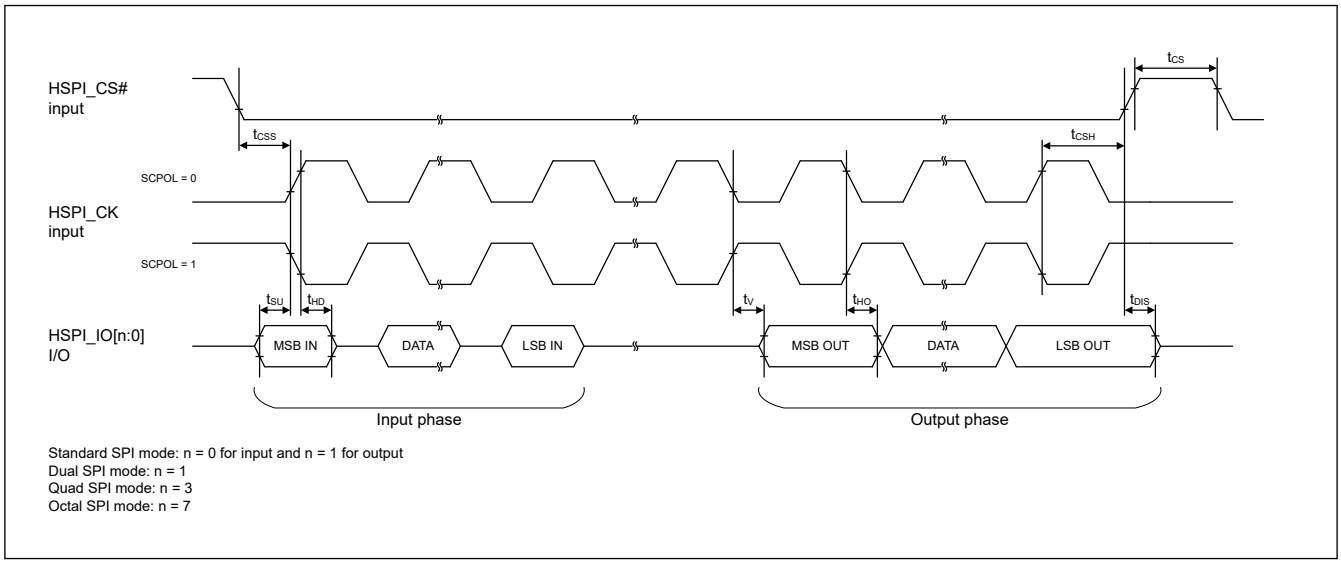


Figure 2.69 SHOSTIF timing (SCPH = 0)

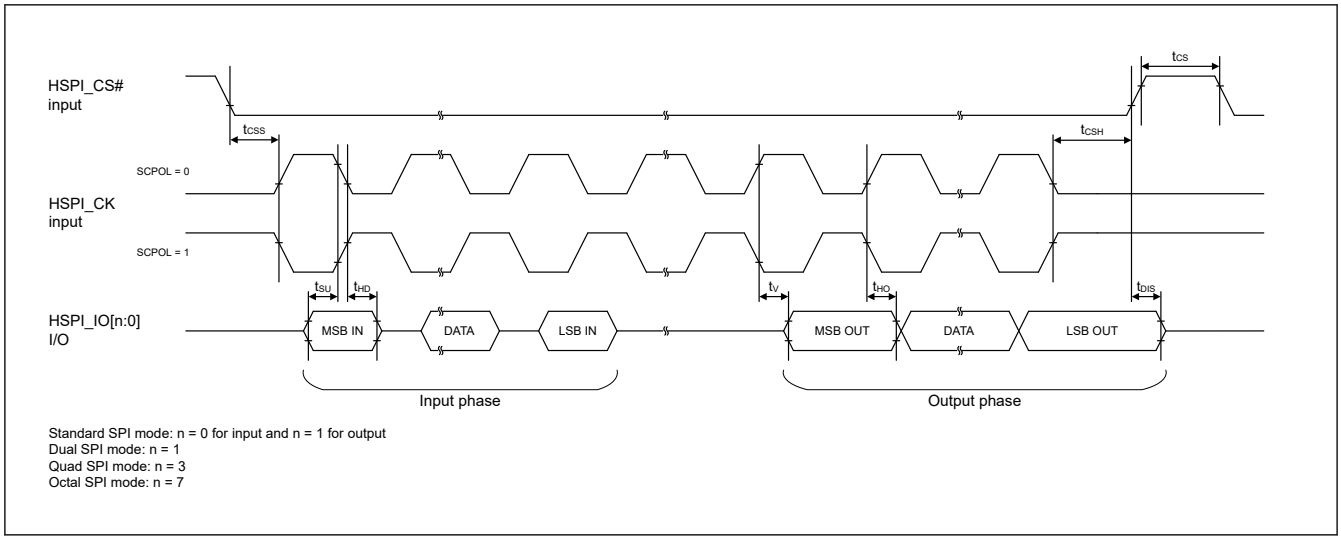


Figure 2.70 SHOSTIF timing (SCPH = 1)

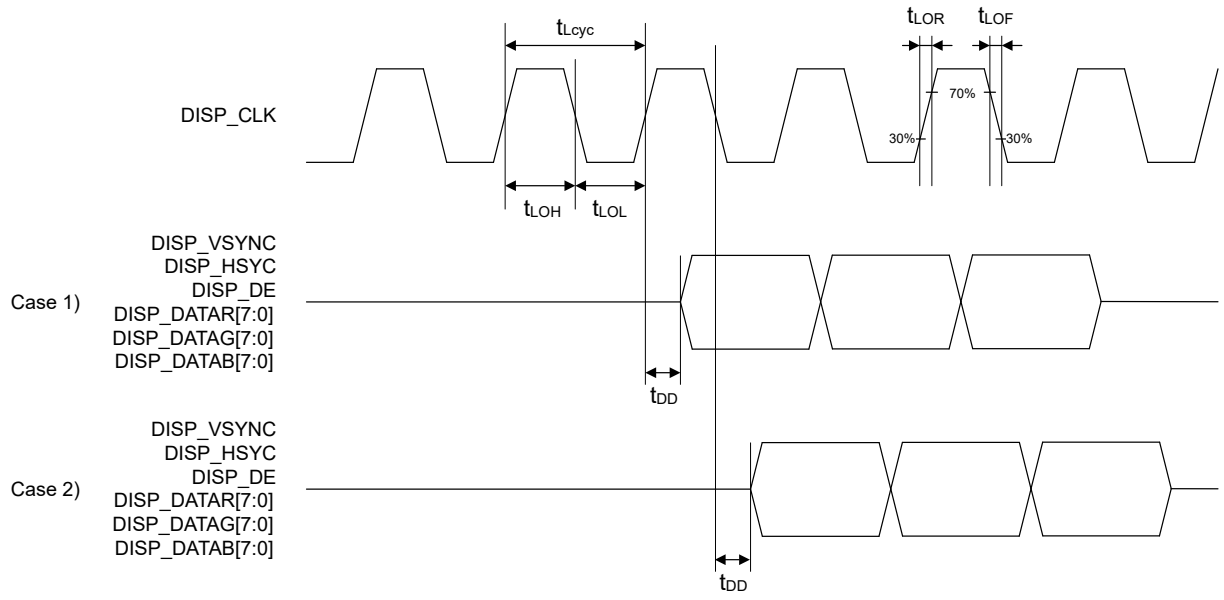
2.5.5.17 LCDC Timing

Conditions:

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF

Table 2.38 LCDC timing

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference figure
LCDC	DCLK output period	t_{Lcyc}	10	—	200	ns	Figure 2.71
	DCLK output low pulse width	t_{LOL}	$t_{Lcyc}/2 - 1$	—	$t_{Lcyc}/2 + 1$	ns	
	DCLK output high pulse width	t_{LOH}	$t_{Lcyc}/2 - 1$	—	$t_{Lcyc}/2 + 1$	ns	
	DCLK output rise time	t_{LOR}	—	—	3	ns	
	DCLK output fall time	t_{LOF}	—	—	3	ns	
	Data output delay	t_{DD}	−1.5	—	1.5	ns	



Note:
Case 1) DISP_CLK forward rotation output mode when DPI_CLKMD bit in DU_DITR0 register is 0.
Case 2) DISP_CLK inverted output mode when DPI_CLKMD bit in DU_DITR0 register is 1.

Figure 2.71 LCDC timing

2.5.5.18 SDHI Timing

Table 2.39 1.8 V SDHI timing (1 of 2)

Conditions: V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5 (VDD1833 = 1.8 V)

Parameter		Symbol	Conditions	Min.	Max.	Unit	Reference figure
(SD) SDR104 (eMMC) HS200	SD_CLK clock cycle	T_{SDCYC}	C = 15 pF Drive Strength CLK: Ultra-high Others: High	5		ns	Figure 2.72
	SD_CLK clock high level width	T_{SDWH}		1.5	—	ns	
	SD_CLK clock low level width	T_{SDWL}		1.5	—	ns	
	SD_CLK clock rise time	T_{SDLH}		—	1	ns	
	SD_CLK clock fall time	T_{SDHL}		—	1	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		−1.7	0.9	ns	
	SD_CMD, SD_DATA input set up time	T_{SDIS}		—	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		—	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		2.88	—	ns	

Table 2.39 1.8 V SDHI timing (2 of 2)

Conditions: V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5 (VDD1833 = 1.8 V)

Parameter		Symbol	Conditions	Min.	Max.	Unit	Reference figure
(SD) SDR50, SDR25, SDR12 (eMMC) High Speed SDR, Backwards Compatibility	SD_CLK clock cycle	T_{SDCYC}	C = 20 pF Drive Strength CLK: Ultra-high Others: High	10	—	ns	Figure 2.72
	SD_CLK clock high level width	T_{SDWH}		3	—	ns	
	SD_CLK clock low level width	T_{SDWL}		3	—	ns	
	SD_CLK clock rise time	T_{SDLH}		—	2	ns	
	SD_CLK clock fall time	T_{SDHL}		—	2	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		−4.2	1.6	ns	
	SD_CMD, SD_DATA input set up time	T_{SDIS}		1.1	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		1.8	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		—	—	ns	
(SD) DDR50 (eMMC) High Speed DDR	SD_CLK clock cycle	T_{SDCYC}	C = 25 pF Drive Strength CLK: High Others: High	20	—	ns	Figure 2.73
	SD_CLK clock high level width	T_{SDWH}		9	11	ns	
	SD_CLK clock low level width	T_{SDWL}		9	11	ns	
	SD_CLK clock rise time	T_{SDLH}		—	3	ns	
	SD_CLK clock fall time	T_{SDHL}		—	3	ns	
	SD_CMD output delay (SDR)	T_{SDODLY}		−6	3	ns	
	SD_CMD input set up time (SDR)	T_{SDIS}		4.8	—	ns	
	SD_CMD input hold time (SDR)	T_{SDIH}		2.5	—	ns	
	SD_DATA output delay (DDR)	T_{SDODLY_DDR}		2.5	6	ns	
	SD_DATA input set up time (DDR)	T_{SDIS_DDR}		1.5	—	ns	
	SD_DATA input hold time (DDR)	T_{SDIH_DDR}		1.5	—	ns	

Table 2.40 3.3 V SDHI timing (1 of 2)

Conditions: V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5 (VDD1833 = 3.3 V)

Parameter		Symbol	Conditions	Min.	Max.	Unit	Reference figure
(SD) High Speed (eMMC) High Speed SDR,	SD_CLK clock cycle	T_{SDCYC}	C = 40 pF Drive Strength CLK: High Others: Middle	20	—	ns	Figure 2.72
	SD_CLK clock high level width	T_{SDWH}		7	—	ns	
	SD_CLK clock low level width	T_{SDWL}		7	—	ns	
	SD_CLK clock rise time	T_{SDLH}		—	3	ns	
	SD_CLK clock fall time	T_{SDHL}		—	3	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		−6.2	2.5	ns	
	SD_CMD, SD_DATA input set up time	T_{SDIS}		4	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		2	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		—	—	ns	

Table 2.40 3.3 V SDHI timing (2 of 2)

Conditions: V_{OH} = VDD1833 × 0.5, V_{OL} = VDD1833 × 0.5 (VDD1833 = 3.3 V)

Parameter		Symbol	Conditions	Min.	Max.	Unit	Reference figure
(SD) Default Speed (eMMC) Backwards Compatibility	SD_CLK clock cycle	T_{SDCYC}	C = 40 pF Drive Strength CLK: High Others: Middle	40	—	ns	Figure 2.72
	SD_CLK clock high level width	T_{SDWH}		10	—	ns	
	SD_CLK clock low level width	T_{SDWL}		10	—	ns	
	SD_CLK clock rise time	T_{SDLH}		—	10	ns	
	SD_CLK clock fall time	T_{SDHL}		—	10	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		−7.5	2.5	ns	
	SD_CMD, SD_DATA input set up time	T_{SDIS}		4	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		2	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		—	—	ns	
(eMMC) High Speed DDR	SD_CLK clock cycle	T_{SDCYC}	C = 30 pF Drive Strength CLK: High Others: High	20	—	ns	Figure 2.73
	SD_CLK clock high level width	T_{SDWH}		9	11	ns	
	SD_CLK clock low level width	T_{SDWL}		9	11	ns	
	SD_CLK clock rise time	T_{SDLH}		—	3	ns	
	SD_CLK clock fall time	T_{SDHL}		—	3	ns	
	SD_CMD output delay (SDR)	T_{SDODLY}		−6	6	ns	
	SD_CMD input set up time (SDR)	T_{SDIS}		4.8	—	ns	
	SD_CMD input hold time (SDR)	T_{SDIH}		2.5	—	ns	
	SD_DATA output delay (DDR)	T_{SDODLY_DDR}		2.5	6.5	ns	
	SD_DATA input set up time (DDR)	T_{SDIS_DDR}		1.7	—	ns	
	SD_DATA input hold time (DDR)	T_{SDIH_DDR}		1.5	—	ns	

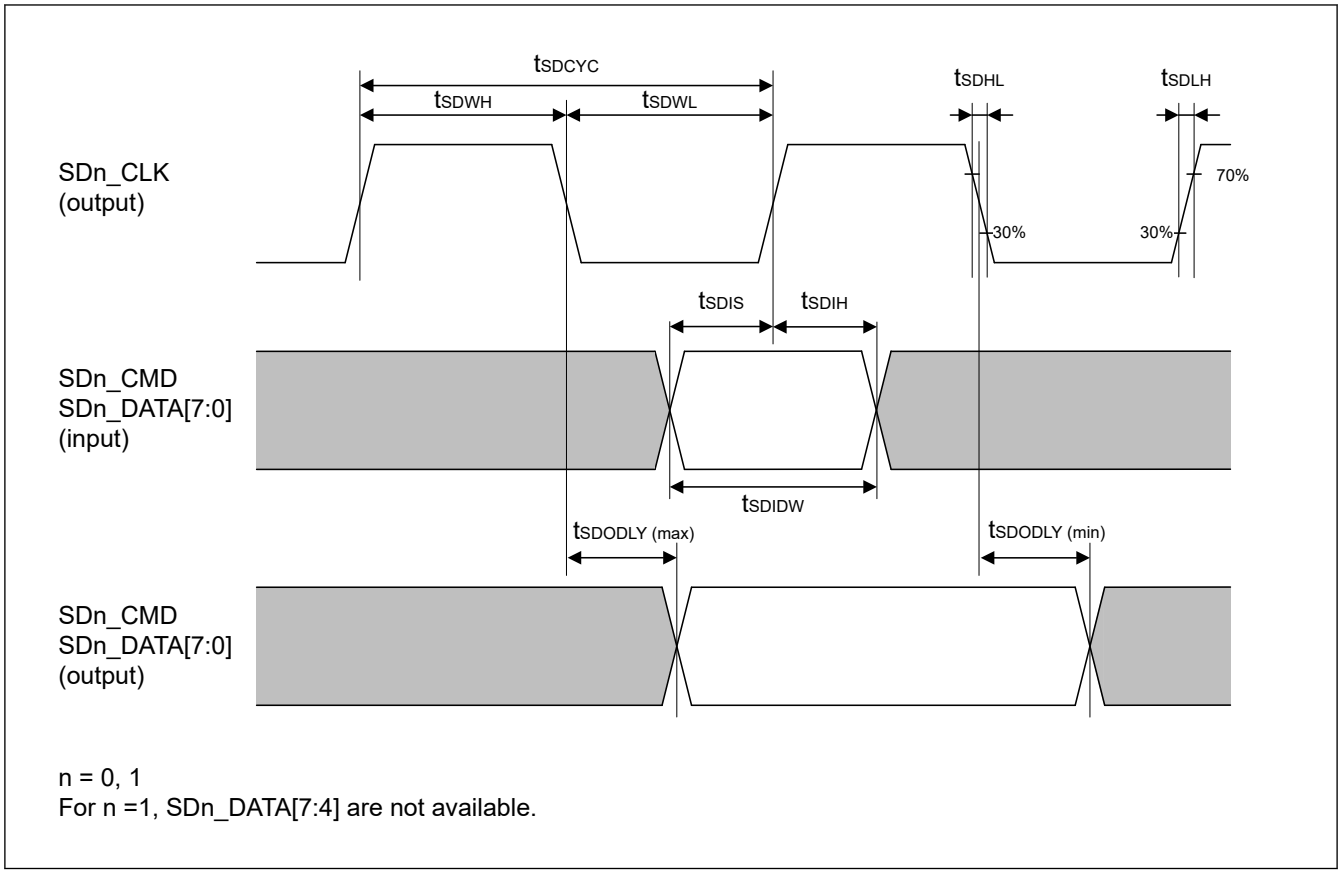


Figure 2.72 SDHI timing (SDR)

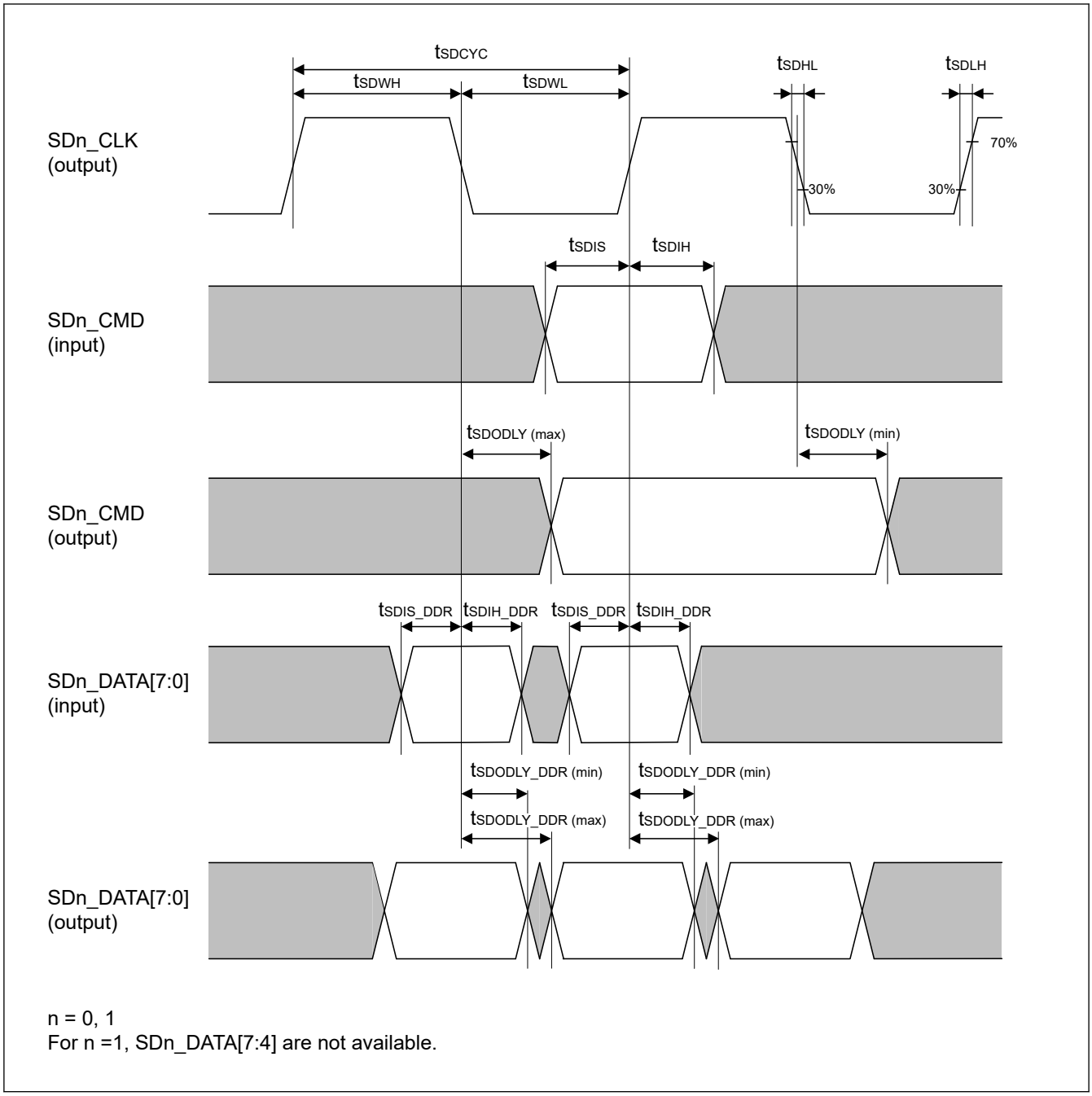


Figure 2.73 SDHI timing (DDR)

2.6 USB Characteristics

The USB PHY of this LSI is compliant with the Universal Serial Bus Specification, Revision 2.0.

Note: 30 (±1%) kΩ external resistor must be connected between USB_VUBUSIN pin and VBUS voltage supply.
200 (±1%) Ω external resistor must be connected between USB_TXRTUNE pin and VSS.

2.7 A/D Conversion Characteristics

Table 2.41 12-Bit A/D conversion characteristics (1 of 2)

Parameter	Min.	Typ.	Max.	Unit	Reference figure
Resolution			12	bits	—

Table 2.41 12-Bit A/D conversion characteristics (2 of 2)

Parameter		Min.	Typ.	Max.	Unit	Reference figure
Analog input capacitance		—	—	15	pF	—
Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ	Channel-dedicated sample-and-hold circuits in use	0.64	—	—	μs	—
	Channel-dedicated sample-and-hold circuits not in use	0.32	—	—		—
Offset error		—	—	±50	LSB	—
Full-scale error		—	—	±50	LSB	—
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	—	±55	LSB	—
DNL differential non-linearity error		—	—	±2	LSB	—
INL integral non-linearity error		—	—	±3.5	LSB	—
Dynamic range		0.02	—	AVDDREF_ADCn - 0.02	V	—

Note: The specified values in the table apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the specified ranges.
Note 1. The conversion time is the total of the sampling time and the comparison time.

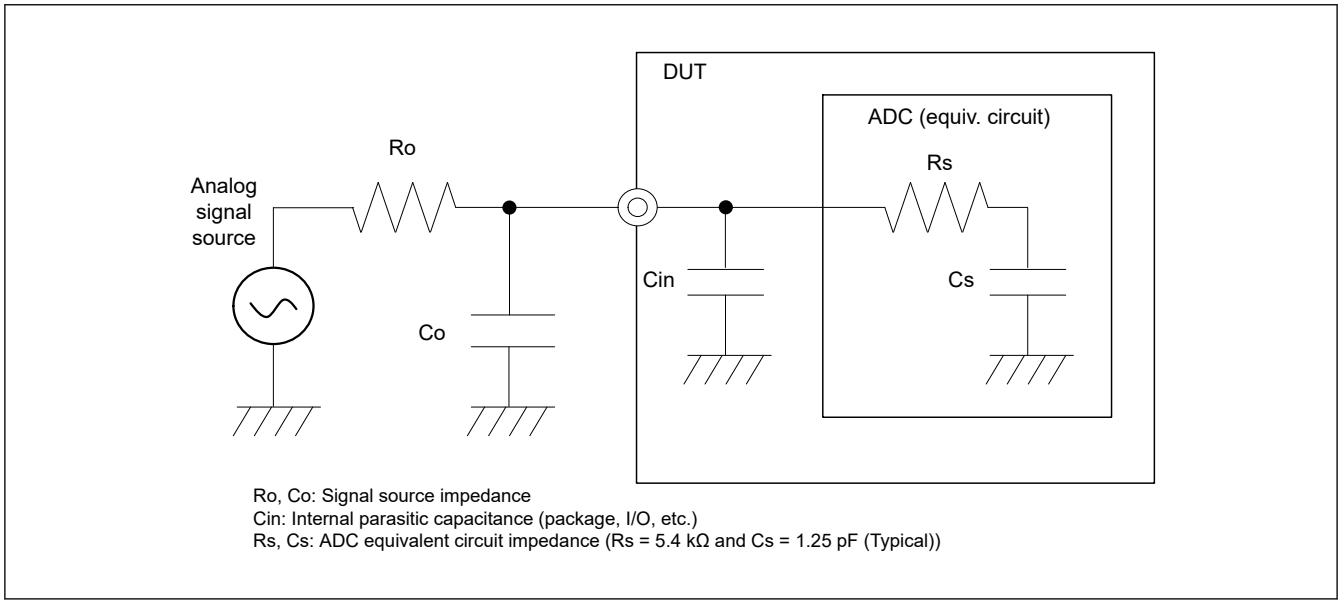


Figure 2.74 A/D converter equivalent circuit and peripheral configuration diagram

2.8 Temperature Sensor Characteristics

Table 2.42 Temperature sensor characteristics

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±2	—	°C	*1
Temperature slope	—	0.0625	—	°C/LSB	—
Output code (at 25°C)	—	1751 (decimal)	—	—	SCRR register

Note 1. 2-point calibration (Tj = −40°C and Tj = 125°C) and 8 times averaging.

2.9 PCI-Express Characteristics

The PCI Express PHY of this LSI is compliant with the PCI Express® Base Specification 3.1 (Gen1/Gen2/Gen3).

Table 2.43 PCI Express REFCLK input characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Input single-end termination impedance	$Z_{RX-SINGLEEND}$	—	10	—	—	kΩ
Differential input peak-to-peak voltage	$V_{RXCLK-DPP}$	—	120	—	—	mV
Input common mode voltage	$V_{RXCLK-DC-CM}$	—	0.25	0.6	0.95	V
Absolute single-end input voltage	$V_{RXCLK-SE}$	—	−0.3	—	1.1	V

2.10 DDRSS (LPDDR4) Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4D standard.

Note: 120 (±1%) Ω external resistor must be connected between DDR_ZN and VSS.

2.11 Debug Interface Timing

Condition: V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5

Table 2.44 Debug interface timing

Parameter		Symbol	Min.	Max.	Unit	Reference figure
TCK cycle time	With an ICE connected	t_{TCKcyc}	30*1	—	ns	Figure 2.75
	For use in BSCAN		80	—		
TCK high pulse width		t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width		t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time		t_{TDIS}	5	—	ns	Figure 2.76 Output load: 30 pF
TDI hold time		t_{TDIH}	5	—	ns	
TMS/SWDIO setup time		t_{TMSS}	5	—	ns	
TMS/SWDIO hold time		t_{TMSH}	5	—	ns	
SWDIO delay time		t_{SWDO}	—	15	ns	
TDO delay time	With an ICE connected	t_{TDOD}	—	15	ns	
	For use in BSCAN		—	22		
Capture register setup time		t_{CAPTS}	5	—	ns	Figure 2.77
Capture register hold time		t_{CAPTH}	5	—	ns	
Update register delay time		$t_{UPDATED}$	—	15	ns	

Note 1. This value is the minimum cycle time for the normal operation of internal circuits.
The actual cycle time should be determined in consideration of the TCK capture edge timing and cable length of the connected ICE.

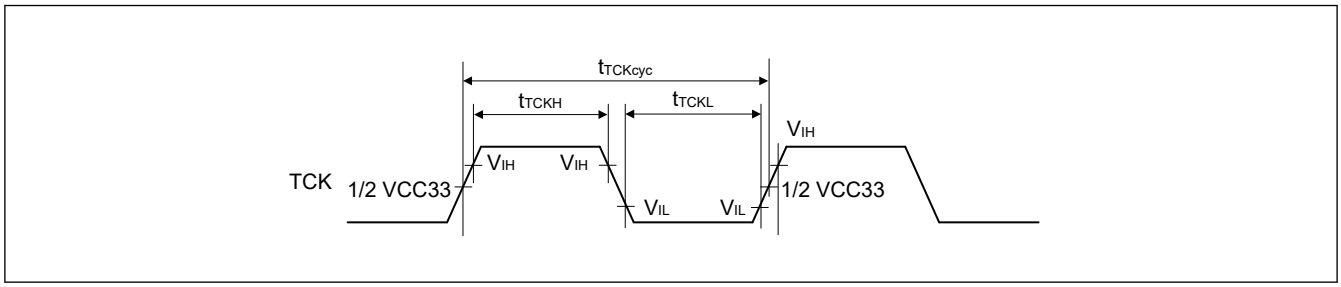


Figure 2.75 TCK input timing

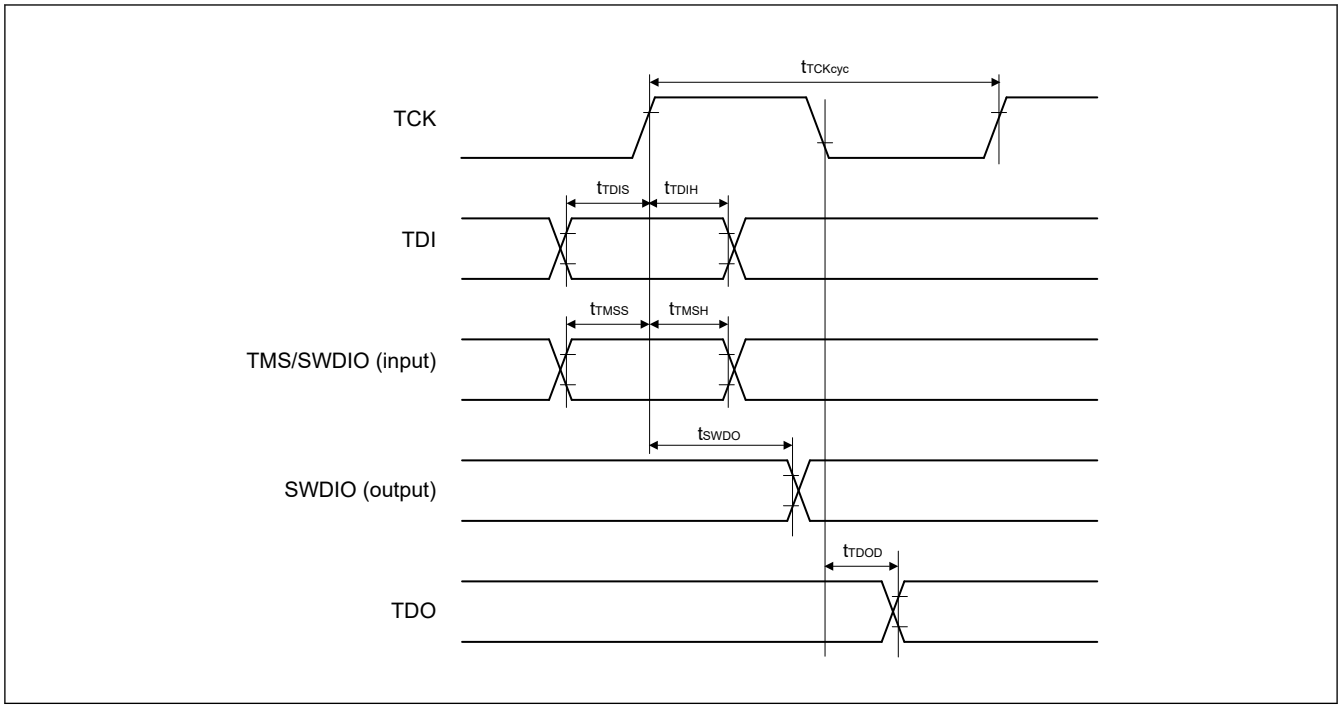


Figure 2.76 Data transfer timing

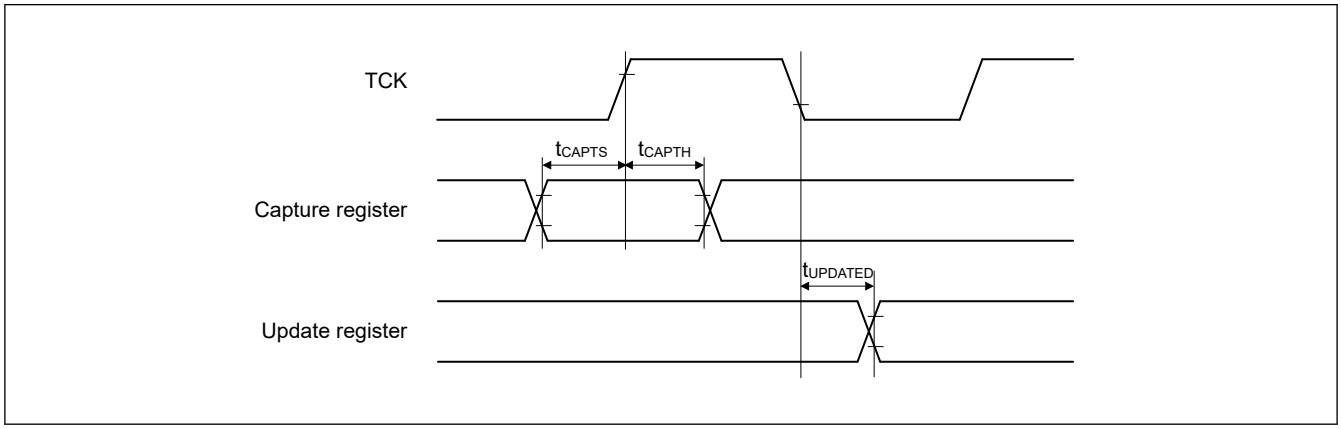
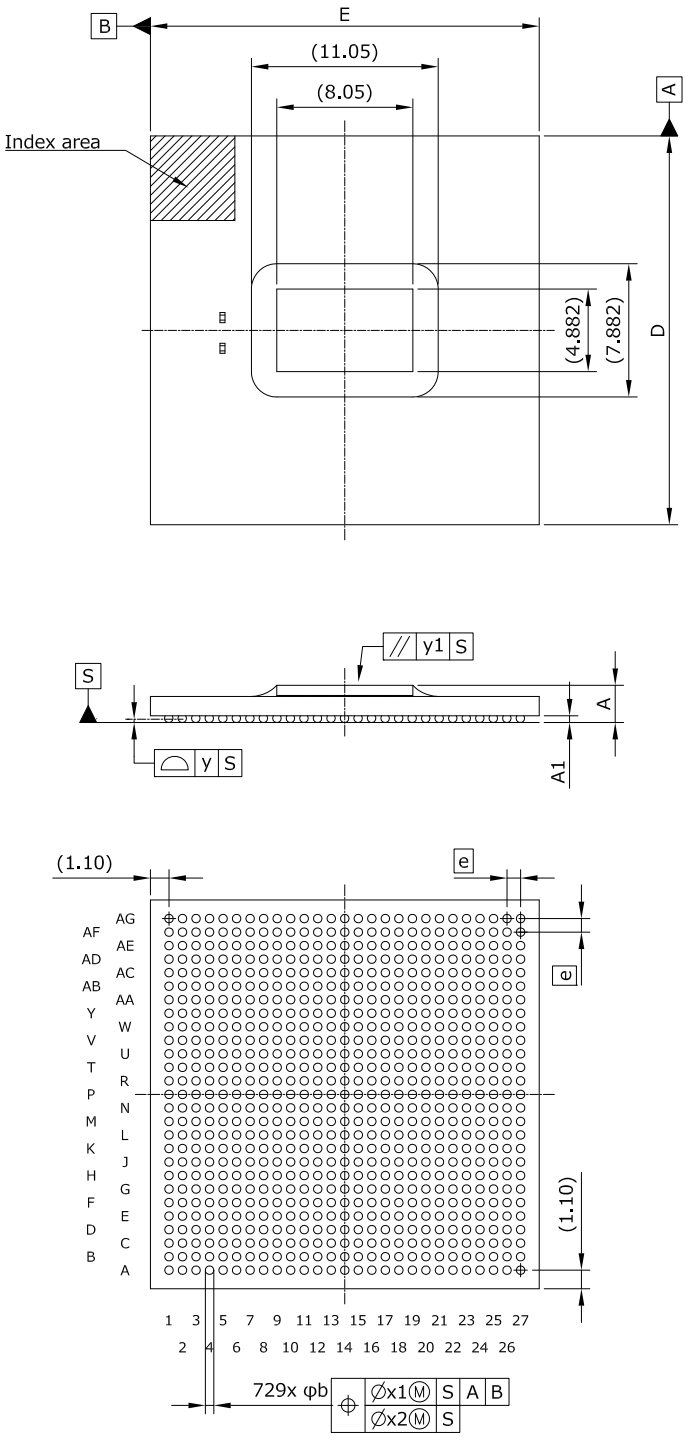


Figure 2.77 Boundary scan input/output timing

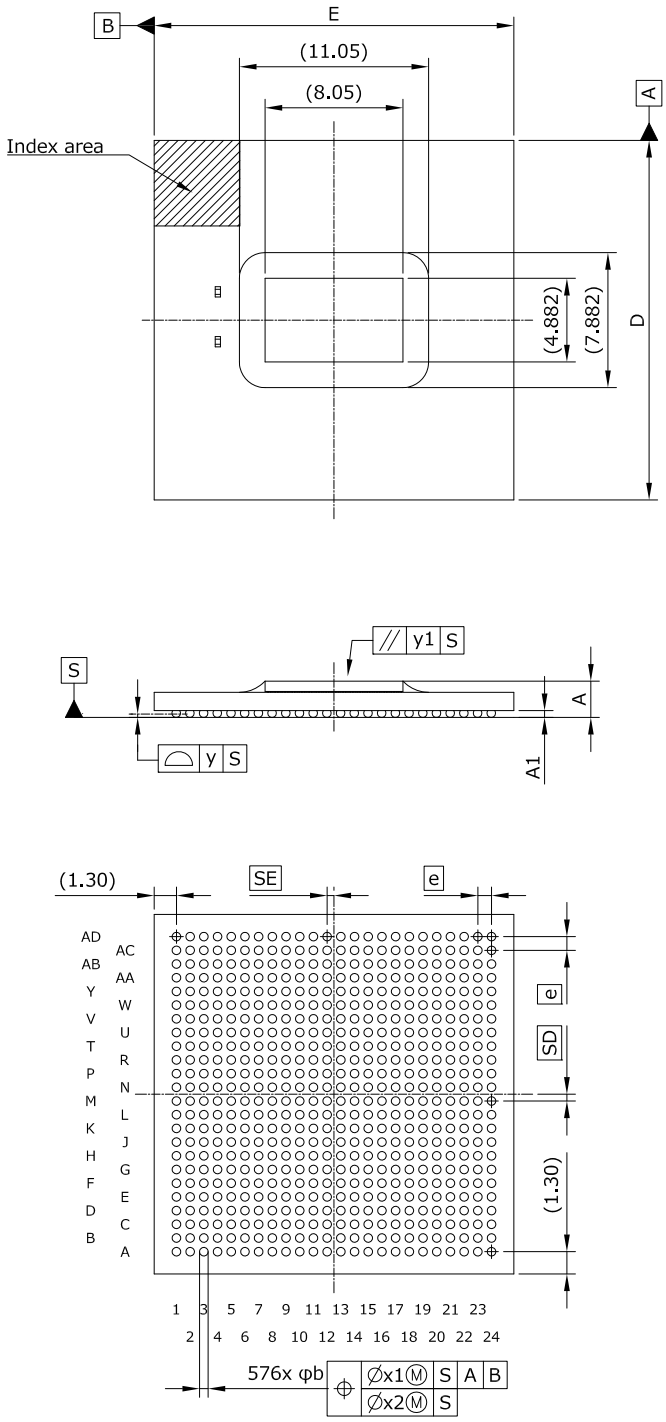
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.



Reference Symbol	Dimension in Milimeters		
	Min	Nom	Max
D	22.8	23.0	23.2
E	22.8	23.0	23.2
A	—	—	2.40
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x1	—	—	0.20
x2	—	—	0.08
y	—	—	0.15
y1	—	—	0.2

Figure A1.1 729-pin FCBGA



Reference Symbol	Dimension in Milimeters		
	Min	Nom	Max
D	20.85	21.0	21.15
E	20.85	21.0	21.15
A	—	—	2.30
A1	0.35	0.40	0.45
e	—	0.80	—
SD	—	0.4	—
SE	—	0.4	—
b	0.45	0.50	0.55
x1	—	—	0.20
x2	—	—	0.08
y	—	—	0.15
y1	—	—	0.2

Figure A1.2 576-pin FCBGA

Revision History

Revision 1.00 — June 28, 2024

Initial release

Revision 1.10 — October 11, 2024

2. Electrical Characteristics:
- Updated Table 2.29 SCI, SCIE timing.

Revision 1.20 — February 13, 2026

2. Electrical Characteristics:
- Updated Table 2.13 Ethernet PHY reference clock output timing
- Updated Table 2.17 Reset, interrupt, and mode timing
- Updated Table 2.20 DMAC timing
- Updated Table 2.21 DMAC timing
- Updated Table 2.33 xSPI timing
- Updated Table 2.39 1.8 V SDHI timing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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