RZ/T2ME Group
RZ Arm-based High-end 32 & 64-bit MPUs

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200/400/800 MHz, Dual Arm® Cortex®-R52 on-chip FPU and NEON™, 2.0 MB of on-chip SRAM, Ethernet MAC, EtherCAT, USB 2.0 high-speed, CAN/CANFD, various communications interfaces such as an xSPI and ΔΣ interface, encoder interfaces, and security functions

Features

On-chip 32-bit Arm Cortex-R52 processor

- High-speed realtime control with operating frequency of 200/400/800 MHz
- On-chip Dual 32-bit Arm Cortex-R52 (revision r1p2)
- Tightly coupled memory (TCM) with ECC
  - CPU0: 512 KB/64 KB
  - CPU1: No support
- Instruction cache/data cache with ECC
  - CPU0: 16 KB per cache
  - CPU1: 32 KB per cache
- High-speed interrupt
- The FPU supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single-precision and double-precision.
- The NEON, Advanced SIMD, supports integer or single precision results.
- Harvard architecture with 8-stage pipeline
- Supports the memory protection unit (MPU)
- Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces.
- No DCLS (Dual Core Lock Step) support

Low power consumption

- Standby mode and module stop function

On-chip SRAM

- 2.0 MB of the on-chip SRAM with ECC
- 150/200 MHz

Data transfer

- DMAC: 16 channels × 2 units

Event link controller

- Module operations can be started by event signals rather than by interrupt handlers.
- Linked operation of modules is available even while the CPU is in the standby state.

Reset and power supply voltage control

- Five reset sources including a pin reset

Clock functions

- External clock/oscillator input frequency: 25 MHz
- CPU clock frequency: 200/400/800 MHz or 150/300/600 MHz
- System clock frequency: 200 MHz or 150 MHz
- Low-speed on-chip oscillator (LOCO): 240 kHz

Safety functions

- Register write protection, input clock oscillation stop detection and CRC
- Master Memory Protection Unit (MPU)

Security functions

- Boot mode with security through encryption
- JTAG authentication
- Cryptologic accelerator
- TRNG

Encoder interfaces

- 2 channels
- EnDat 2.2, BiSS-C, FA-CODER, A-format, and HIPERFACE DSL-compliant interfaces
- Frequency-divided output from an encoder

Various communications interfaces

- Ethernet
  - EtherCAT slave Controller: 3 ports
  - Ethernet switch: 3 ports
  - Ethernet MAC: 1 port
- USB 2.0 high-speed host/functions: 1 channel
- CAN/CANFD (compliant with ISO11898-1): 2 channels
- SCI with 16-byte transmission and reception FIFOs: 6 channels
- I2C bus interface: 3 channel for transfer at up to 400 kbps
- SPI: 4 channels
- xSPI: 2 channels

External address space

- Buses for high-speed data transfer at up to 100 MHz
- Support for up to 4 CS areas
- 8-, 16- or 32-bit bus space is selectable per area

Up to 35 extended-function timers

- 16-bit × 8 + 32-bit MTU3 (9 channels), 32-bit GPT (18 channels): Input capture, output compare, PWM waveform output
- 16-bit CMT (6 channels), 32-bit CMTW (2 channels)

ΔΣ interface

- Up to 6 ΔΣ modulators are connectable externally.

Trigonometric function unit

- Simultaneous calculation of sine and cosine
- Simultaneous calculation of arctangent and hypot_k

12-bit A/D converter

- 12 bits × 2 unit (8 channels for unit 0, 16 channels for unit 1)

Temperature sensor for measuring temperature within the chip

General-purpose I/O ports

- Input pull-up/pull-down
- The locations of input/output functions for peripheral modules are selectable from among multiple pins.

Operating temperature range

- Tj = -40 to +125°C

1. Overview

1.1 Outline of Specifications

The MPU is a high-performance ASSP that has dual Arm Cortex®-R52 processor with Floating-Point Unit (FPU) and NEON™. It incorporates integrated peripheral functions necessary for system configuration.

Table 1.1 CPU

Feature	Functional description
Arm® Cortex®-R52	● Two processors consist of single core ● Operating frequency – 200 MHz/400 MHz/800 MHz (in case of 200 MHz system clock) – 150 MHz/300 MHz/600 MHz (in case of 150 MHz system clock) ● 32-bit CPU Cortex-R52 designed by Arm (core revision r1p2) ● Address space: 4 GB ● Instruction cache – CPU0: 16 KB (with ECC) – CPU1: 32 KB (with ECC) ● Data cache – CPU0: 16 KB (with ECC) – CPU1: 32 KB (with ECC) ● Tightly coupled memory (TCM) – CPU0 ATCM: 512 KB (with ECC) 1 wait (0 wait selectable if less than 400 MHz) BTCM: 64 KB (with ECC) 0 wait CTCM: 0 KB (with ECC) – CPU1 ATCM: 0 KB BTCM: 0 KB CTCM: 0 KB ● Instruction set: Arm v8-R architecture, so support includes Thumb® and Thumb-2 ● Data arrangement – Instructions: Little endian – Data: Little endian ● 2-stage memory protection unit (MPU) ● No DCLS (Dual Core Lock Step) support
FPU	● Supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single- and double-precision. ● Registers 64-bit single-word registers: 64 bits × 32 (can be used as 16 double-word registers: 128 bits × 16)
NEON	The Advanced SIMD supporting integer or single precision results

Table 1.2 Memory

Feature	Functional description
On-chip system SRAM with ECC	● Capacity: Up to 2.0 MB (512 KB × 4 units) (with ECC) ● Operating frequency: 150 MHz/200 MHz ● SEC-DED (single error correction/double error detection) Error injection supported
One-time programmable memory	● Overwrite protection ● Redundancy support ● ECC support ● Available information – Unique ID – Authentication settings – Trimming data – Boot mode setting – User area

Table 1.3 System

Feature	Functional description
Operating modes	The operating mode can be selected from the following seven boot modes: ● xSPI0 boot mode (CS0 × 1 boot Serial Flash) ● xSPI0 boot mode (CS0 × 8 boot Serial Flash) ● 16-bit bus boot mode (CS0 NOR Flash) ● 32-bit bus boot mode (CS0 NOR Flash) ● xSPI1 boot mode (CS0 × 1 boot Serial Flash) ● SCI boot mode ● USB boot mode
Clock generation circuit	● The input clock can be selected from an external clock or external resonator. ● Detection of input clock oscillation stopping ● The following clocks are generated: – CPU0 clock: System clock x1, x2 or x4 – CPU1 clock: System clock x1, x2 or x4 – System clock: 150 or 200 MHz – High-speed peripheral module clock: 150 or 200 MHz – Middle-speed peripheral module clock: 75 or 100 MHz – Low-speed peripheral module clock: 37.5 or 50 MHz – ADC clock in the 12-bit A/D converter: 18.75 or 25 MHz – External bus clock: 100 MHz (max.) – Low-speed on-chip oscillator: 240 kHz (fixed)
Reset	RES# pin reset, software reset, error reset, CPU0 software reset, CPU1 software reset
Low-power consumption function	● Standby mode (Cortex-R52) ● Module stop function
Interrupt controller (ICU)	● Connect an interrupt to the GIC (Generic Interrupt Controller) for Cortex-R52 CPU0 and CPU1 ● Connect an activating trigger to the DMAC and ELC ● Peripheral function interrupts: 394 sources ● External interrupts: 16 sources (IRQ0 to IRQ15 pins) ● Software interrupts: 8 sources ● Non-maskable interrupts: 1 sources ● 32 levels specifiable for the order of priority in the GIC
Bus state controller (BSC)	● The external address space is divided into four areas (CS0, CS2, CS3, and CS5) for management. ● The following features are configurable for each area independently: Bus size (8, 16, or 32 bits): Available sizes depend on the area. Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas). Idle wait cycle insertion (between same area access cycles or different area access cycles). Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. ● Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software). ● Connectable memory type for each area CS0: SRAM, burst ROM CS2: SRAM CS2 + CS3: SRAM, SDRAM (CS2 only for SDRAM is not supported) CS3: SRAM, SDRAM CS5: SRAM, MPX-IO ● SDRAM refresh Auto refresh or self-refresh mode selectable ● SDRAM burst access

Table 1.4 Direct memory access

Feature	Functional description
Direct memory access controller (DMAC)	● 2 units (16 channels each unit) ● Transfer modes: Single transfer mode and block transfer mode ● Transfer size - Unit 0: 1/2/4/8/16/32/64 bytes - Unit 1: 1/2/4/8/16/32 bytes ● Activation sources: Software trigger, external DMA requests (DREQ), external interrupts, and interrupt requests from peripheral functions

Table 1.5 I/O Ports

Feature	Functional description
General-purpose I/O ports	• 320-pin FBGA – I/O pins: 193 – Input pins: 1 – Pull-up/pull-down resistors: 194 • 225-pin FBGA – I/O pins: 134 – Input pins: 1 – Pull-up/pull-down resistors: 135 • The locations of input/output functions are selectable from among multiple pins.

Table 1.6 Event link

Feature	Functional description
Event link controller (ELC)	• Up to 213 event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of ports 16 and port 18 is to be possible.

Table 1.7 Timers (1 of 2)

Feature	Functional description
Multi-function timer pulse unit 3 (MTU3)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 10, 11, 12, or 14 counter-input clock signals for each channel (with maximum operating frequency of 200 MHz) • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode - Outputs non-overlapping waveforms for controlling 3-phase inverters - Automatic specification of dead times - PWM duty cycle: Selectable as any value from 0% to 100% - Delay can be applied to requests for A/D conversion. - Non-generation of interrupt requests at peak or trough values of counters can be selected. - Double buffer configuration • Reset synchronous PWM mode Six phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2), 32-bit mode (channels 1 and 2 in cascade connection) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital noise filter function for signals on the input capture and external counter clock pins • Event linking by the ELC

Table 1.7 Timers (2 of 2)

Feature	Functional description
General PWM timer (GPT)	• 32 bits × 18 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 400 MHz for LLPP) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of 3 counters, generation of automatic 3-phase PWM waveforms incorporating dead times • Starting, clearing, stopping, switching, up/down counters, and input capture in response to external or internal triggers • Starting, clearing, stopping, switching, up/down counters, and input capture in response to input level comparison • Internal trigger sources: software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter function for signals on the input capture and external trigger pins • Event linking by the ELC • Function of output duty 0% and 100% is selectable from troughs or crests/troughs. (all units)
Compare match timer (CMT)	• (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel
Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.
Watchdog timer (WDT)	• 14 bits × 2 channels • Select from among six counter-input clock signals for each channel
Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by input clock oscillation-stoppage detection, PLL oscillation anomaly detection, DSMIF error detection, or software • Additional programming of output control target pins is enabled
Port output enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPT • Initiation by detection of oscillation stop, DSMIF error detection, or by software
Real time clock (RTC)	• A 100 year calendar from 2000 to 2099 • BCD code display • Clock source is division of main oscillator. • Automatic adjustment function for leap years

Table 1.8 Communication interfaces (1 of 3)

Feature	Functional description
Ethernet MAC (GMAC)	• 1 port • IEEE802.3 • IEEE1588-2008 • IEEE802.3-az-2010 for EEE • Support for 10/100/1000 Mbps data transfer • Full duplex and half duplex are supported • Programmable frame length to support both standard and jumbo frames up to 16 KB • 17 MAC address registers for the address filter block • Variety of flexible addresses filtering modes are supported • Advanced IEEE 1588-2002 & 2008 Ethernet frame time-stamping supported • MII/RMII/RGMII interface is supported by RMII/RGMII converter
Ethernet switch (ETHSW)	• 3-port PHY interfaces • IEEE802.3 • Support for 10/100/1000 Mbps data transfer • Full and half duplex (1000 Mbps supports full-duplex only) • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with eight priority levels • Multicasting and broadcasting • VLAN frame • IEEE 1588-2008 compatible • Programmable addition, removal and manipulation of ingress and egress VLAN tags, supporting single and double-tagged VLAN frames on each port • Cut-through and hub features • Device level ring (DLR) • Programmable egress rate limit per port • Ingress Configurable Broadcast/multicast storm protection per port • IEEE802.1X source address authentication supported • IEEE802.1X guest VLAN supported • PRP functionality (IEC 62439-3 edition 2.0- 2012) • Configurable Time Multiplexed (TDMA) output queue scheduler supporting real-time network infrastructures using time slots for bandwidth reservation enabling deterministic delays • Frame preemption • Cyclic queuing and forwarding • Forwarding rule for the TSN-IA profile • A MAC source address filtering • Pattern matchers 12 channels • Independent two timer module are available for timestamping and time for TDMA. • Remote monitoring through SNMP • Powerlink capable hub • 4 additional PTP timer pulse generators • MAC to MAC connection • MII/RMII/RGMII interface is supported by RMII/RGMII converter • 802.1CB, Clause 6.6 (Active Stream Identification) • 802.1, Clause 8.5 and 6.9: TCI.PCP remapping / TCI.VID assignment • 802.1Q, Cluase 12.20.3: Priority Regeneration Override • 802.1Q, Clause 8.6.5 and MEF 10.3: Flow clasification and metering • IEEE1588 UDP/IPv4 1step E2E TC
EtherCAT slave controller (ESC)*1	• 1 channel (3 ports) • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented • MII interface is supported. RMII/RGMII interface is supported by RGMII converter in Ethernet Subsystem.
USB 2.0 HS host/function module	• 1 port • Compliance with the USB 2.0 specification • OTG support • Transfer rate High speed (480 Mbps), full speed (12 Mbps), low speed (1.5 Mbps, host only) • Communications buffer – Incorporates 1 KB of RAM for host mode – Incorporates 8 KB of RAM for function mode • DMAC (2 channels) incorporated

Table 1.8 Communication interfaces (2 of 3)

Feature	Functional description
Serial communication interface (SCI)	• 6 channels • 5 communication mode – Asynchronous interfaces – 8-bit clock synchronous interface – Simple I2C (master-only) – Simple SPI – Smart card interface • Clock source is select from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and half-duplex communication • Data length: 7 to 9 bits (Asynchronous mode) • Bit rate modulation • Double speed mode (Asynchronous, Clock Synchronous, Simple SPI mode) • RS-485 driver control function (Asynchronous mode) • Loopback function to enable self-diagnosis (Asynchronous, Clock synchronous mode)
I^2C bus interface (IIC)	• 3 channels • Communication formats: I2C bus format or SMBus format • Master or slave mode selectable • Supports the multi-master • Maximum transfer rate: 400 kbps (Standard mode and Fast mode)
CAN-FD module (CANFD)	• 2 channels • Comply with CAN-FD ISO 11898-1 (2015) • Communication speed – Classical CAN mode: 1 Mbps – CAN FD mode: Nominal bit rate: max. 1 Mbps Data bit rate: max. 8 Mbps • Total 192 message buffers (in case frame size is 76 bytes) – Individual buffers: 64 for TX – Shared buffers: 128 for TX and RX including FIFO • Selectable ID type with 11-bit Standard and 18-bit Extended • Selectable Frame type: Data Frame and Remote Frame • Up to 256 receive rules
Serial peripheral interface (SPI)	• 4 channels • SPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (SPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) capable of handling serial transfer as a master or slave • Data formats – Switching between MSB first and LSB first – Transfer bit length selectable to 4 - 32 bits – 32 bits × 4-stage FIFO transmit and receive buffers – Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • RSPCK can be stopped automatically with the reception buffer full for master reception

Table 1.8 Communication interfaces (3 of 3)

Feature	Functional description
Expanded serial peripheral interface (xSPI)	• 2 channels • Comply with JESD251 • Multiple slave up to 2 slaves • Protocol mode: 1/4/8pin with SDR/DDR 1S-1S-1S, 4S-4D-4D, 8D-8D-8D • Support OctaFlash, OctaRAM, HyperFlash and HyperRAM • Protocol mode: 2/4pin with SDR compatible with QSPI 1S-2S-2S, 2S-2S-2S 1S-4S-4S, 4S-4S-4S • Configurable address length • Configurable initial access latency cycle • Support XiP mode • Support up to 128 MB address space each CS • Prefetch function for burst-read with low latency • Outstanding buffer for burst-write with high throughput • Manual command configurable up to 4 commands • Output clock/input strobe port timing shift • Automatic command after released reset: up to 4 commands • CS size can be changed • Support on-the-fly decription – Outstanding: 2 – Bypass area /decryption area selectable – AES CTR mode decryption – Support only decription read (No support encryption write)

Note 1. EtherCAT is a registered trademark of Beckhoff Automation GmbH, Germany.

Table 1.9 Analog

Feature	Functional description
12-bit A/D converter (ADC12)	• 12 bits × 2 units (unit 0: 8 channels, unit 1: 16 channels) • 12-bit resolution • Conversion time 0.84 µs per channel • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, timer (MTU3, ELC) trigger, external trigger • Event linking by the ELC
Temperature sensor unit (TSU)	• 1 channel • Relative precision: ±1°C (typ)

Table 1.10 Hardware accelerator for industrial interfaces

Feature	Functional description
ΔΣ interface (DSMIF)	• 3 channels × 2 units • Selectable 2 inputs (U/V) or 3 inputs (U/V/W) • Up to 6 ΔΣ modulators are externally connectable • Sinc filter can be selected as first, second or third order • Direct error connection to POE3 and POEG
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, hypot_k ($\sqrt{x^2+y^2}/k$) • Simultaneous calculation of sine and cosine • Simultaneous calculation of arctangent and hypot_k
Encoder interfaces*1	• EnDat 2.2, BiSS, FA-CODER, A-format, and HIPERFACE DSL-compliant interfaces

Note 1. This applies to the devices with the encoder interfaces.

Table 1.11 Safety

Feature	Functional description
Memory protection unit (MPU)	• Cortex-R52 MPU Two stages MPUs (EL2 and EL1) 24 regions each MPU • Master MPU Memory protection for masters except Cortex-R52 (DMAC, USB, Ethernet MAC, CoreSight)
Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
CRC calculator (CRC)	• 2 channels • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: – $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet) – $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) – $X^{16} + X^{15} + X^2 + 1$ (CRC-16) – $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) – $X^8 + X^2 + X + 1$ (CRC-8)
Clock monitor circuit (CLMA)	• Monitors the abnormal output clock frequency from the input clock (main clock oscillator), PLL circuit, or low-speed on-chip oscillator. • Input clock oscillation stop detection: Available
Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Isolated peripherals	• Safety dedicated peripherals are available: – GPT: 4 ch – SCI: 1 ch – IIC: 1 ch – SPI: 1 ch – CRC: 1 unit – RTC: 1 unit – GPIO: Sharable with normal GPIO – On-chip system SRAM with ECC • They are mapped independently from normal peripherals so that access protection can be done by EL2 MPU.

Table 1.12 Security

Feature	Functional description
Security	• Secure boot • JTAG authentication • SCI/USB boot disable • Cryptographic accelerators – Symmetric Cipher: AES 128/192/256 bits with CBC/ECB/CTR/GCM/XTS – Asymmetric Cipher: ECC 256 bits, RSA 1024/2048/3072 bits, RSAES-OAEP – Hash: SHA-1, SHA-2 – Message authentication: HMAC, CMAC, GMAC – Signature algorithms: ECDSA with NIST P-256, RSASSA-PSS, RSASSA-PKCS1 • TRNG

Table 1.13 Debug

Feature	Functional description
Debugging interface	• CoreSight architecture designed by Arm • Debugging function by the JTAG/SWD interface, and trace function by the trace port interface

Table 1.14 Others (1 of 2)

Feature	Functional description
Power supply voltage	VDD = 1.1 V (Core) VCC18 = 1.8 V (PLL, USB, ADC, TSU) VCC33 = 3.3 V (I/O, USB) VCC1833 = 1.8 V (RGMII, xSPI) or 3.3 V (RMII/MII, xSPI[*1])
Operating temperature	Tj = −40 to +125°C

Table 1.14 Others (2 of 2)

Feature	Functional description
Packages	320 pin FBGA 17 × 17 mm, 0.8-mm pitch 225 pin FBGA 13 × 13 mm, 0.8-mm pitch

Note 1. Maximum xSPI clock frequency is 75 MHz at 3.3 V.

1.2 Function Comparison

Table 1.15 Comparison of Functions for Different Packages

Module/Function		320 pins	225 pins
CPU	ARM Cortex-R52	Dual	Dual
Memory	System SRAM	2.0 MB	2.0 MB
External bus	External bus width	32 bits	
Interrupt	External interrupt	NMI, IRQ0 to IRQ15	
DMA	DMA controller (DMAC)	2 units (DMAC0: 16 channels, DMAC1: 16 channels)	
Timer	Multi-function timer pulse unit 3 (MTU3)	9 channels	
	General PWM timer (GPT)	18 channels	
	Compare match timer (CMT)	6 channels	
	Compare match timer W (CMTW)	2 channels	
	Watchdog timer	2 channels	
	Port output enable 3 (POE3)	Available	
	Port output enable for GPT (POEG)	Available	
	Real time clock (RTC)	Available	
Communication function	Ethernet MAC (GMAC)	1 port	
	Ethernet switch (ETHSW)	3 ports (PHY interface)	
	EtherCAT slave controller (ESC)	3 ports	
	USB 2.0 HS host/function module (USB)	1 port	
	Serial communication interface (SCI)	6 channels	
	I2C bus interface (IIC)	3 channels	
	CANFD module (CANFD)	2 channels	
	Serial peripheral interface (SPI)	4 channels	
	Expanded serial peripheral interface (xSPI)	2 channels (1.8 V or 3.3 V)	1 channel (1.8 V or 3.3 V)
ΔΣ interface (DSMIF)		2 units (DSMIF0: 3 channels, DSMIF1: 3 channels)	
Trigonometric function unit (TFU)		Available	
12-bit A/D converter (ADC12)		2 units (ADC120: 8 channels, ADC121: 16 channels)	2 units (ADC120: 4 channels, ADC121: 8 channels)
Temperature sensor unit (TSU)		Available	
CRC calculator (CRC)		2 channels	
Clock monitor circuit (CLMA)		Available	
Data operation circuit (DOC)		Available	
Security		Available	
Event link controller (ELC)		Available	
Encoder interfaces		Available	

1.3 Product Lineup

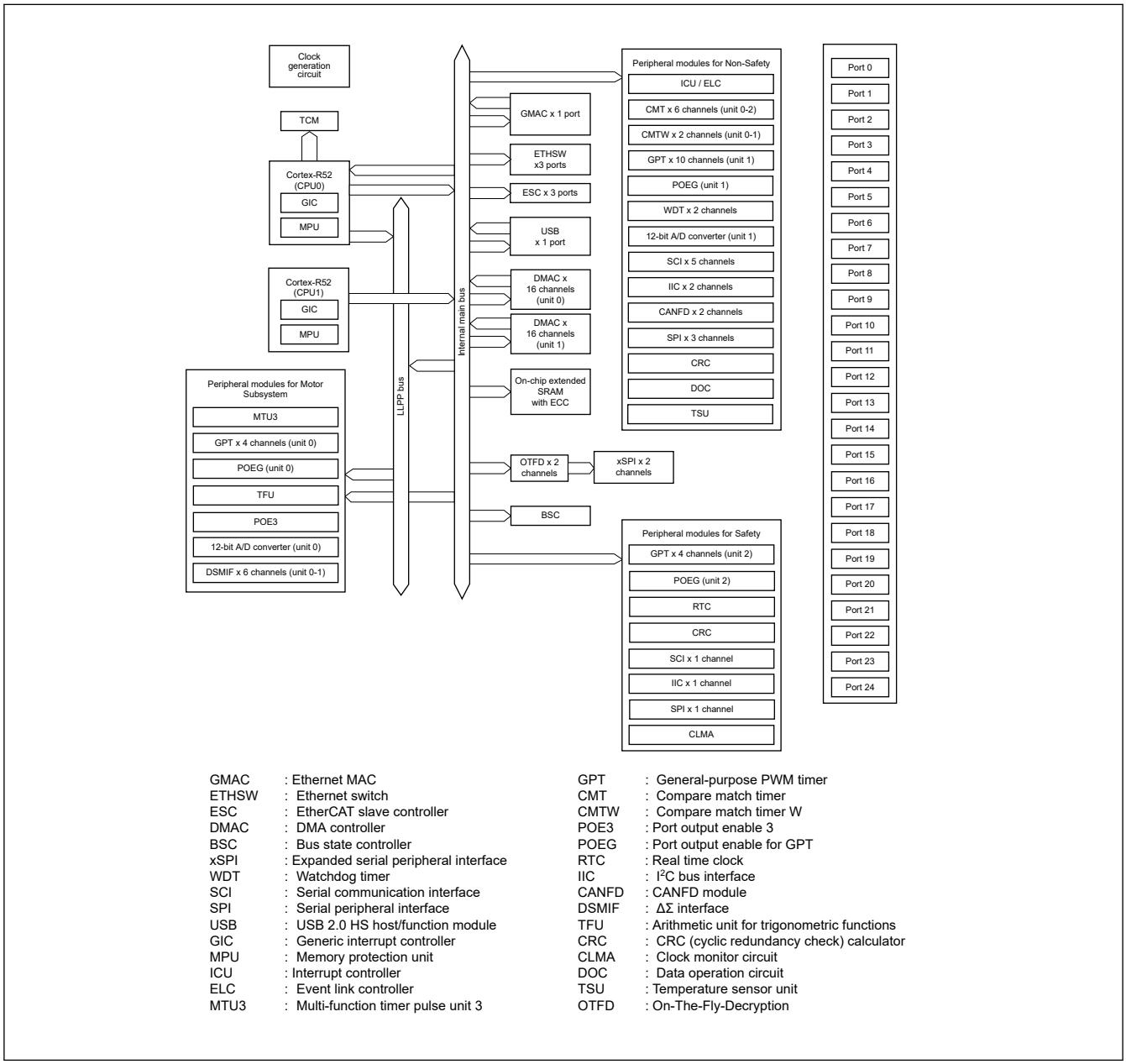
Table 1.16 shows a product lineup.

Table 1.16 Product lineup

Part Number	Package	CPU	System SRAM Capacity	CAN	Ethernet	Security
R9A07G075M29GBG	PLBG0320GA-A	Dual Cortex-R52	2.0 MB	CAN-FD	Available	Available
R9A07G075M29GBA	PLBG0225GB-A	Dual Cortex-R52	2.0 MB	CAN-FD	Available	Available

1.4 Block Diagram

Figure 1.1 shows a block diagram of a 320-pin device.



GMAC : Ethernet MAC
ETHSW : Ethernet switch
ESC : EtherCAT slave controller
DMAC : DMA controller
BSC : Bus state controller
xSPI : Expanded serial peripheral interface
WDT : Watchdog timer
SCI : Serial communication interface
SPI : Serial peripheral interface
USB : USB 2.0 HS host/function module
GIC : Generic interrupt controller
MPU : Memory protection unit
ICU : Interrupt controller
ELC : Event link controller
MTU3 : Multi-function timer pulse unit 3

GPT : General-purpose PWM timer
CMT : Compare match timer
CMTW : Compare match timer W
POE3 : Port output enable 3
POEG : Port output enable for GPT
RTC : Real time clock
IIC : I^2C bus interface
CANFD : CANFD module
DSMIF : ΔΣ interface
TFU : Arithmetic unit for trigonometric functions
CRC : CRC (cyclic redundancy check) calculator
CLMA : Clock monitor circuit
DOC : Data operation circuit
TSU : Temperature sensor unit
OTFD : On-The-Fly-Decryption

Figure 1.1 Block diagram of a 320-pin device

1.5 Pin Functions

Table 1.17 lists the pin functions.

Table 1.17 Pin functions (1 of 6)

Classification	Pin name	I/O	Description
Power supply	VDD	Input	Power supply pin. Connect this pin to the system power supply.
	VSS	Input	Ground pin. Connect this pin to the system power supply (0 V).
	VCC1833_0 VCC1833_1 VCC1833_2 VCC1833_3 VCC1833_4	Input	Power supply pin for each I/O domains. (1.8 V or 3.3 V) This pin is available for BGA package product only.
	VCC33	Input	Power supply pin for I/O pins.
	VCC18_PLL0, VCC18_PLL1	Input	Power supply pins for the on-chip PLL oscillator
	AVCC18_TSU	Input	Power supply pin for the temperature sensor unit
Clock	XTAL	Output	Connected to a crystal resonator. When external clock signal is used, EXTAL pin should be driven low. XTAL pin should never be driven or loaded by anything other than crystal oscillator. The voltage level of EXTAL must not exceed core VDD (1.16 V).
	EXTAL	Input	
	EXTCLKIN	Input	Inputs the external clock. When a crystal resonator is connected, it should be driven low.
	CKIO	Output	Outputs the external bus clock for external devices.
	ETH0_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 0
	ETH1_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 1
	ETH2_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 2
	RMII0_REFCLK	Output	Outputs 50 MHz clock for RMII0
	RMII1_REFCLK	Output	Outputs 50 MHz clock for RMII1
	RMII2_REFCLK	Output	Outputs 50 MHz clock for RMII2
Operating mode control	MDX	Input	This signal should be driven low.
	MD0 to MD2	Input	Input the operating mode select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDV0 to MDV4	Input	Input the operating voltage select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDW	Input	Input the ATCM wait cycle select signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
	MDD	Input	Input the enabling JTAG authentication by hash signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES#	Input	Inputs the reset signal. This MPU enters the reset state when this signal goes low.
	BSCANP	Input	Inputs the boundary scan enable signal. Boundary scan is enabled when this pin goes high. When boundary scan is not used, this pin should be driven low.
	RSTOUT#	Output	Outputs the reset signal externally

Table 1.17 Pin functions (2 of 6)

Classification	Pin name	I/O	Description
Debugging interface	TRST#	Input	Test reset pin for the on-chip emulator
	TMS	I/O	Test mode select pin for the on-chip emulator Functions as the SWDIO pin in serial wire debug (SWD) mode
	TDI	Input	Test data input pin for the on-chip emulator
	TDO	Output	Test data output pin for the on-chip emulator
	TCK	Input	Test clock pin for the on-chip emulator Functions as the SWCLK pin in serial wire debug (SWD) mode
	TRACECLK	Output	Outputs the clock for synchronization with trace data
	TRACECTL	Output	Outputs the enable signal for trace control
	TRACEDATA0 to TRACEDATA7	Output	Output trace data
Bus state controller (BSC)	A25 to A0	Output	Output the address
	D31 to D0	I/O	Input and output the data
	CS0#, CS2#, CS3#, CS5#	Output	Output the chip select signal for the external memory or device.
	RD#	Output	Outputs the strobe signal which indicates a read is in progress.
	RD/WR#	Output	Outputs the strobe signal which indicates a read or write access
	BS#	Output	Outputs the status signal which indicates the start of the bus cycle
	AH#	Output	Outputs the address hold signal for the device that uses the multiplexed I/O interface
	WAIT#	Input	Inputs the external wait control signal which inserts a wait cycle into the bus cycle
	WE0#	Output	Outputs the write strobe signal to D7 to D0
	WE1#	Output	Outputs the write strobe signal to D15 to D8
	WE2#	Output	Outputs the write strobe signal to D23 to D16
	WE3#	Output	Outputs the write strobe signal to D31 to D24
	DQMLL	Output	Outputs the data mask enable signal to D7 to D0 when SDRAM is connected
	DQMLU	Output	Outputs the data mask enable signal to D15 to D8 when SDRAM is connected
	DQMUL	Output	Outputs the data mask enable signal to D23 to D16 when SDRAM is connected
	DQMUU	Output	Outputs the data mask enable signal to D31 to D24 when SDRAM is connected
	RAS#	Output	Outputs the row-address strobe signal to the SDRAM. This pin should be connected to the RAS# pin on the SDRAM.
	CAS#	Output	Outputs the column-address strobe signal to the SDRAM. This pin should be connected to the CAS# pin on the SDRAM.
	CKE	Output	Outputs the clock enable signal to the SDRAM. This pin should be connected to the CKE pin on the SDRAM.

Table 1.17 Pin functions (3 of 6)

Classification	Pin name	I/O	Description
Direct memory access controller (DMAC)	DREQ	Input	Inputs the DMA transfer request signal from the external device
	DACK	Output	Outputs the acknowledge signal which indicates acceptance of the DMA transfer request from the external device
	TEND	Output	Outputs the DMA transfer end signal
Interrupt	NMI	Input	Inputs the non-maskable interrupt request signal
	IRQ0 to IRQ15	Input	Input the external interrupt request signal
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	TGRA0 to TGRD0 input capture input, output compare output, and PWM output pins
	MTIOC1A, MTIOC1B	I/O	TGRA1 and TGRB1 input capture input, output compare output, and PWM output pins
	MTIOC2A, MTIOC2B	I/O	TGRA2 and TGRB2 input capture input, output compare output, and PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	TGRA3 to TGRD3 input capture input, output compare output, and PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	TGRA4 to TGRD4 input capture input, output compare output, and PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	TGRU5, TGRV5, and TGRW5 input capture input and dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	External clock input pins for MTU3
Port output enable 3 (POE3)	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input the request signal to place the MTU3 in the high-impedance state
General PWM timer (GPT)/ Port output enable for GPT (POEG)	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input and output-disable request input pins
	GTETRGSA, GTETRGSB	Input	External trigger input and output-disable request input pins (SAFETY)
	GTIOC0A to GTIOC17A, GTIOC0B to GTIOC17B	I/O	Input capture input/output compare output/PWM output pins
	GTADSML0, GTADSML1, GTADSMP0, GTADSMP1	Output	Output pins for monitoring A/D conversion start requests
Compare match timer W (CMTW)	CMTW0_TIC0, CMTW0_TIC1, CMTW1_TIC0, CMTW1_TIC1	Input	CMTW input capture input pins
	CMTW0_TOC0, CMTW0_TOC1, CMTW1_TOC0, CMTW1_TOC1	Output	CMTW output compare output pins
Real time clock (RTC)	RTCAT1HZ	Output	RTC 1 Hz output pin

Table 1.17 Pin functions (4 of 6)

Classification	Pin name	I/O	Description
Serial communication interface (SCI)	SCK0 to SCK5	I/O	Clock I/O pins (clock synchronous mode/simple SPI mode/smart card mode)
	RXD0 to RXD5	Input	Input the receive data (asynchronous mode/clock synchronous mode/smart card mode)
	TXD0 to TXD5	Output	Output the transmit data (asynchronous mode/clock synchronous mode/smart card mode)
	CTS0# to CTS5#	Input	Input the start of transmission (asynchronous mode/ clock synchronous mode) active-low
	RTS0# to RTS5#	Output	Output the reception (asynchronous mode/clock synchronous mode) active-low
	SCL0 to SCL5	I/O	Input/output the I2C clocks (simple I2C mode)
	SDA0 to SDA5	I/O	Input/output the I2C data (simple I2C mode)
	MISO0 to MISO5	I/O	Input/output the data for slave transmission (simple SPI mode)
	MOSI0 to MOSI5	I/O	Input/output the data for master transmission (simple SPI mode)
	SS0# to SS5#	Input	Chip-select input pins (simple SPI mode) active-low
	DE0 to DE5	Output	Driver enable output pins (asynchronous mode)
I2C bus interface (IIC)	IIC_SCL0 to IIC_SCL2	I/O	Clock I/O pins
	IIC_SDA0 to IIC_SDA2	I/O	Data I/O pins
Ethernet	ETH0_TXCLK to ETH2_TXCLK	I/O	TX clock input pins (MII mode) TX clock output pins (RGMII mode)
	ETH0_TXD0 to ETH2_TXD0	Output	TX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_TXD1 to ETH2_TXD1	Output	TX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_TXD2 to ETH2_TXD2	Output	TX data 2 pins (RGMII and MII modes)
	ETH0_TXD3 to ETH2_TXD3	Output	TX data 3 pins (RGMII and MII modes)
	ETH0_TXEN to ETH2_TXEN	Output	TX data enable pins (RMII and MII modes) TX data enable/TX data error (TX_CTL) pins (RGMII mode)
	ETH0_TXER to ETH2_TXER	Output	TX data error pins (MII mode)
	ETH0_RXCLK to ETH2_RXCLK	Input	RX clock pins (RGMII, RMII, and MII modes)
	ETH0_RXD0 to ETH2_RXD0	Input	RX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_RXD1 to ETH2_RXD1	Input	RX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_RXD2 to ETH2_RXD2	Input	RX data 2 pins (RGMII and MII modes)
	ETH0_RXD3 to ETH2_RXD3	Input	RX data 3 pins (RGMII and MII modes)
	ETH0_RXDV to ETH2_RXDV	Input	RX data valid pins (MII mode) Carrier sense/RX data valid (CRS_DV) pins (RMII mode) RX data valid/RX error (RX_CTL) pins (RGMII mode)
	ETH0_RXER to ETH2_RXER	Input	RX data error pins (RMII and MII modes)
	ETH0_CRS to ETH2_CRS	Input	Carrier sense pins (MII mode)
	ETH0_COL to ETH2_COL	Input	Collision detection pins (MII mode)
Ethernet MAC (GMAC)	GMAC_PTPTRG0	Input	PTP timer trigger external input 0
	GMAC_PTPTRG1	Input	PTP timer trigger external input 1
	GMAC_MDC	Output	Management data clock output pin
	GMAC_MDIO	I/O	Management data I/O pin

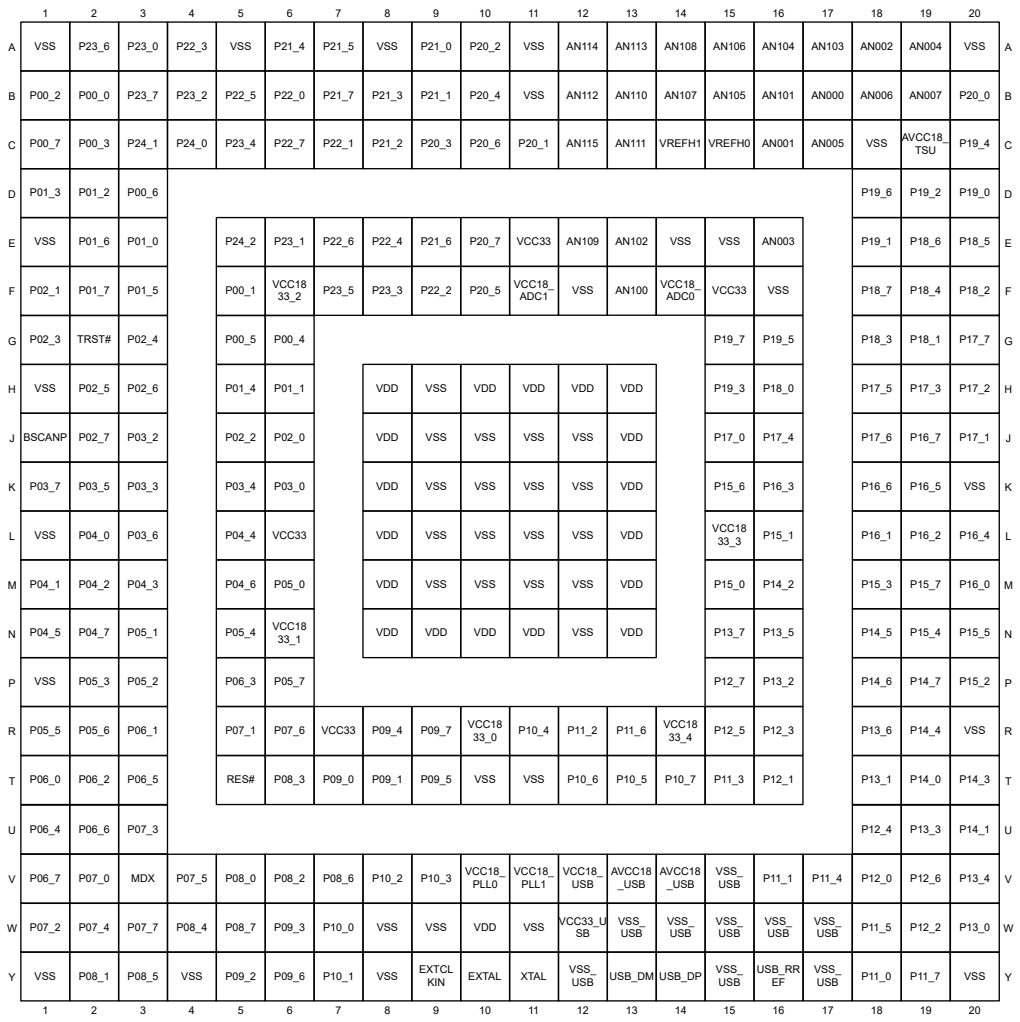
Table 1.17 Pin functions (5 of 6)

Classification	Pin name	I/O	Description
Ethernet switch (ETHSW)	ETHSW_LPI0	Output	Port 0 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_LPI1	Output	Port 1 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_LPI2	Output	Port 2 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_PTPOUT0 to ETHSW_PTPOUT3	Output	Ethernet switch timer pulse output pins
	ETHSW_TDMAOUT0 to ETHSW_TDMAOUT3	Output	Ethernet switch TDMA timer output pins
	ETHSW_PHYLINK0 to ETHSW_PHYLINK2	Input	Ethernet switch PHY link status input pins
	ETHSW_MDC	Output	Management data clock output pin
	ETHSW_MDIO	I/O	Management data I/O pin
EtherCAT slave controller (ESC)	ESC_LEDRUN	Output	Outputs the EtherCAT RUN LED signal
	ESC_IRQ	Output	Outputs the EtherCAT IRQ signal
	ESC_LEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal
	ESC_LEDERR	Output	Outputs the EtherCAT error LED signal
	ESC_LINKACT0 to ESC_LINKACT2	Output	Output the EtherCAT link/activity LED signal
	ESC_SYNC0, ESC_SYNC1	Output	Output the EtherCAT SYNC signal
	ESC_LATCH0, ESC_LATCH1	Input	Input the EtherCAT LATCH signal
	ESC_RESETOUT#	Output	Output the EtherCAT reset signal
	ESC_I2CCLK	Output	Outputs the EtherCAT EEPROM I2C clock signal
	ESC_I2CDATA	I/O	Inputs and outputs the EtherCAT EEPROM I2C data signal
	ESC_PHYLINK0 to ESC_PHYLINK2	Input	Inputs the EtherCAT PHY link status signal.
	ESC_MDC	Output	Management data clock output pin
	ESC_MDIO	I/O	Management data I/O pin
USB 2.0 host/function module	VCC33_USB	Input	Power supply input pin for USB
	VCC18_USB	Input	Power supply input pin for USB
	VSS_USB	Input	Ground input pins for USB
	AVCC18_USB	Input	Analog power supply input pin for USB
	USB_RREF	Input	Reference current input pin for USB. Connect this pin to the VSS_USB pin with 1.8 kΩ (±1%).
	USB_DP	I/O	USB bus D+ data I/O pin
	USB_DM	I/O	USB bus D- data I/O pin
	USB_VBUSEN	Output	Outputs the VBUS power enable signal for USB
	USB_OVRCUR	Input	Inputs the overcurrent signal for USB
	USB_VBUSIN	Input	USB cable connection/disconnection detection input pin
	USB_EXICEN	Output	OTG power supply IC control pin
	USB_OTGID	Input	OTG ID pin

Table 1.17 Pin functions (6 of 6)

Classification	Pin name	I/O	Description
CANFD module (CANFD)	CANRX0, CANRX1	Input	Receive data input pins
	CANTX0, CANTX1	Output	Transmit data output pins
	CANRXDP0, CANRXDP1	Output	Receive data phase output pins
	CANTXDP0, CANTXDP1	Output	Transmit data phase output pins
Serial peripheral interface (SPI)	SPI_RSPCK0 to SPI_RSPCK3	I/O	Clock I/O pins
	SPI_MOSI0 to SPI_MOSI3	I/O	Master transmit data I/O pins
	SPI_MISO0 to SPI_MISO3	I/O	Slave transmit data I/O pins
	SPI_SSL00 to SPI_SSL30	I/O	Slave select signal I/O pins
	SPI_SSL01 to SPI_SSL31, SPI_SSL02 to SPI_SSL32, SPI_SSL03 to SPI_SSL33	Output	Slave select signal output pins
Expanded serial peripheral interface (xSPI)	XSPI0_CKP, XSPI1_CKP, XSPI0_CKN, XSPI1_CKN	Output	Clock output pins
	XSPI0_CS0#, XSPI0_CS1#, XSPI1_CS0#, XSPI1_CS1#	Output	Chip select output pins
	XSPI0_DS, XSPI1_DS	I/O	Read data strobe/write data mask input/output pin
	XSPI0_IO0 to XSPI0_IO7, XSPI1_IO0 to XSPI1_IO7	I/O	Data0 to Data7 input/output pins
	XSPI0_RESET0#, XSPI0_RESET1#, XSPI1_RESET0#, XSPI1_RESET1#	Output	Master reset status output pins
	XSPI0_RSTO0#, XSPI0_RSTO1#, XSPI1_RSTO0#, XSPI1_RSTO1#	Input	Slave reset status input pins
	XSPI0_INT0#, XSPI0_INT1#, XSPI1_INT0#, XSPI1_INT1#	Input	Interrupt input pins
	XSPI0_ECS0#, XSPI0_ECS1#, XSPI1_ECS0#, XSPI1_ECS1#	Input	Error correction status input pins
	XSPI0_WP0#, XSPI0_WP1#, XSPI1_WP0#, XSPI1_WP1#	Output	Write protect output pins
ΔΣ interface (DSMIF)	MCLK0 to MCLK5	I/O	Clock I/O pins
	MDAT0 to MDAT5	Input	Data input pins
12-bit A/D converter (ADC12)	AN000 to AN007, AN100 to AN115	Input	Analog input pins for the A/D converter
	ADTRG0#, ADTRG1#	Input	External trigger input pins for the start of A/D conversion
Analog power supply	VCC18_ADC0, VCC18_ADC1	Input	Analog power supply input pin for the 12-bit A/D converter. Connect this pin to the 1.8 V power supply if the 12-bit A/D converter is not to be used.
	VREFH0, VREFH1	Input	Reference voltage input pin for the 12-bit A/D converter. Connect this pin to the 1.8 V power supply if the 12-bit A/D converter is not to be used.
I/O ports	P00_0 to P24_2	I/O	General-purpose input/output pins
Encoder I/F	ENCIF0 to ENCIF15	I/O	I/O pins for multi-protocol encoder interface

1.6 FBGA 320 Pin Assignments



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	P23_6	P23_0	P22_3	VSS	P21_4	P21_5	VSS	P21_0	P20_2	VSS	AN114	AN113	AN108	AN106	AN104	AN103	AN002	AN004	VSS	A
B	P00_2	P00_0	P23_7	P23_2	P22_5	P22_0	P21_7	P21_3	P21_1	P20_4	VSS	AN112	AN110	AN107	AN105	AN101	AN000	AN006	AN007	P20_0	B
C	P00_7	P00_3	P24_1	P24_0	P23_4	P22_7	P22_1	P21_2	P20_3	P20_6	P20_1	AN115	AN111	VREFH1	VREFH0	AN001	AN005	VSS	AVCC18_TSU	P19_4	C
D	P01_3	P01_2	P00_6															P19_6	P19_2	P19_0	D
E	VSS	P01_6	P01_0		P24_2	P23_1	P22_6	P22_4	P21_6	P20_7	VCC33	AN109	AN102	VSS	VSS	AN003		P19_1	P18_6	P18_5	E
F	P02_1	P01_7	P01_5		P00_1	VCC18 33_2	P23_5	P23_3	P22_2	P20_5	VCC18_ADC1	VSS	AN100	VCC18_ADC0	VCC33	VSS		P18_7	P18_4	P18_2	F
G	P02_3	TRST#	P02_4		P00_5	P00_4									P19_7	P19_5		P18_3	P18_1	P17_7	G
H	VSS	P02_5	P02_6		P01_4	P01_1		VDD	VSS	VDD	VDD	VDD	VDD		P19_3	P18_0		P17_5	P17_3	P17_2	H
J	BSCANP	P02_7	P03_2		P02_2	P02_0		VDD	VSS	VSS	VSS	VSS	VDD		P17_0	P17_4		P17_6	P16_7	P17_1	J
K	P03_7	P03_5	P03_3		P03_4	P03_0		VDD	VSS	VSS	VSS	VSS	VDD		P15_6	P16_3		P16_6	P16_5	VSS	K
L	VSS	P04_0	P03_6		P04_4	VCC33		VDD	VSS	VSS	VSS	VSS	VDD		VCC18 33_3	P15_1		P16_1	P16_2	P16_4	L
M	P04_1	P04_2	P04_3		P04_6	P05_0		VDD	VSS	VSS	VSS	VSS	VDD		P15_0	P14_2		P15_3	P15_7	P16_0	M
N	P04_5	P04_7	P05_1		P05_4	VCC18 33_1		VDD	VDD	VDD	VDD	VSS	VDD		P13_7	P13_5		P14_5	P15_4	P15_5	N
P	VSS	P05_3	P05_2		P06_3	P05_7									P12_7	P13_2		P14_6	P14_7	P15_2	P
R	P05_5	P05_6	P06_1		P07_1	P07_6	VCC33	P09_4	P09_7	VCC18 33_0	P10_4	P11_2	P11_6	VCC18 33_4	P12_5	P12_3		P13_6	P14_4	VSS	R
T	P06_0	P06_2	P06_5		RES#	P08_3	P09_0	P09_1	P09_5	VSS	VSS	P10_6	P10_5	P10_7	P11_3	P12_1		P13_1	P14_0	P14_3	T
U	P06_4	P06_6	P07_3															P12_4	P13_3	P14_1	U
V	P06_7	P07_0	MDX	P07_5	P08_0	P08_2	P08_6	P10_2	P10_3	VCC18_PLL0	VCC18_PLL1	VCC18_USB	AVCC18_USB	AVCC18_USB	VSS_USB	P11_1	P11_4	P12_0	P12_6	P13_4	V
W	P07_2	P07_4	P07_7	P08_4	P08_7	P09_3	P10_0	VSS	VSS	VDD	VSS	VCC33_USB	VSS_USB	VSS_USB	VSS_USB	VSS_USB	VSS_USB	P11_5	P12_2	P13_0	W
Y	VSS	P08_1	P08_5	VSS	P09_2	P09_6	P10_1	VSS	EXTCLKIN	EXTAL	XTAL	VSS_USB	USB_DM	USB_DP	VSS_USB	USB_RREF	VSS_USB	P11_0	P11_7	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.2 Pin arrangement (320-pin FBGA) (top view)

Table 1.18 List of pins and pin functions (320-pin FBGA) (1 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
A1	—	VSS	—	—	—	—	—	—	—	—
A2	—	—	P23_6	D21	MTIOC8B	SS0# / CTS0# / RTS0#	—	—	—	—
A3	—	—	P23_0	D15	—	SPI_MOSI2	—	IRQ5	—	—
A4	—	—	P22_3	D10	MTIOC8D / GTETRGSB	—	—	—	—	ENCIF11
A5	—	VSS	—	—	—	—	—	—	—	—
A6	—	TRACEDATA3	P21_4	D3	MTIOC6D / GTIOC15B	SS5# / CTS5# / RTS5# / SPI_SSL02	MDAT1	—	—	ENCIF8
A7	—	TRACEDATA4	P21_5	D4	MTIOC7A / GTIOC16A / CMTW1_TOC1	CTS5# / SPI_MISO0	MCLK2	IRQ6	ADTRG1#	ENCIF9
A8	—	VSS	—	—	—	—	—	—	—	—
A9	—	—	P21_0	WE2# / DQMUL	MTIOC2B / GTIOC13B	ETHSW_PTPOUT3 / ESC_LINKACT2	MDAT5	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (2 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
A10	—	MDV1	P20_2	—	—	DE3 / ETHSW_TDMAOUT1 / ESC_LEDRUN / ESC_LEDSTER	—	—	—	—
A11	—	VSS	—	—	—	—	—	—	—	—
A12	—	—	—	—	—	—	—	—	AN114	—
A13	—	—	—	—	—	—	—	—	AN113	—
A14	—	—	—	—	—	—	—	—	AN108	—
A15	—	—	—	—	—	—	—	—	AN106	—
A16	—	—	—	—	—	—	—	—	AN104	—
A17	—	—	—	—	—	—	—	—	AN103	—
A18	—	—	—	—	—	—	—	—	AN002	—
A19	—	—	—	—	—	—	—	—	AN004	—
A20	—	VSS	—	—	—	—	—	—	—	—
B1	VCC1833_2	—	P00_2	D28 / RD#	MTIC5V	TXD2 / SDA2 / MOSI2 / ETH2_TXEN / USB_OVRCUR	—	—	—	—
B2	VCC1833_2	—	P00_0	D26 / D15	—	SCK2 / ETH2_RXD3	—	—	—	—
B3	VCC1833_2	—	P23_7	D22 / D11 / BS	MTIOC0A / GTETRGA	SCK1 / ETH2_RXD0	MCLK 4	—	—	ENCIF12
B4	—	—	P23_2	D17 / WE1# / DQMLU	MTCLKB	—	—	IRQ8	—	—
B5	—	—	P22_5	D12	—	CTS4#	—	—	—	—
B6	—	TRACEDATA7	P22_0	D7	MTIOC7D / GTIOC17B	DE5	MDAT 3	IRQ15	—	—
B7	—	TRACEDATA6	P21_7	D6 / DREQ	MTIOC7C / GTIOC17A	DE0	MCLK 3	IRQ10	—	—
B8	—	TRACEDATA2	P21_3	D2	MTIOC6C / GTIOC15A	TXD5 / SDA5 / MOSI5 / SPI_SSL33	MCLK 1	—	—	ENCIF7
B9	—	TRACEDATA0	P21_1	D0	MTIOC6A / GTIOC14A / CMTW0_TIC0	SCK5 / IIC_SCL1 / SPI_SSL20	MCLK 0	—	—	ENCIF5
B10	—	MDV3	P20_4	—	—	ETHSW_TDMAOUT3 / ESC_LINKACT1	—	—	—	—
B11	—	VSS	—	—	—	—	—	—	—	—
B12	—	—	—	—	—	—	—	—	AN112	—
B13	—	—	—	—	—	—	—	—	AN110	—
B14	—	—	—	—	—	—	—	—	AN107	—
B15	—	—	—	—	—	—	—	—	AN105	—
B16	—	—	—	—	—	—	—	—	AN101	—
B17	—	—	—	—	—	—	—	—	AN000	—
B18	—	—	—	—	—	—	—	—	AN006	—
B19	—	—	—	—	—	—	—	—	AN007	—
B20	—	—	P20_0	—	MTIOC7D / GTIOC7B	—	—	—	—	—
C1	VCC1833_2	—	P00_7	RAS#	MTIOC4A / GTIOC2A	—	—	IRQ13	—	—
C2	VCC1833_2	—	P00_3	D29 / RD/WR#	MTIC5W	SS2# / CTS2# / RTS2# / ETH2_REFCLK / RMII2_REFCLK	—	IRQ1	—	—
C3	VCC1833_2	—	P24_1	D24 / D13 / CAS#	MTIOC0C / POE8# / GTETRGC	ETH2_RXCLK	MCLK 5	—	—	ENCIF14
C4	VCC1833_2	—	P24_0	D23 / D12 / CKE / DREQ	MTIOC0B / GTETRGB	RXD1 / SCL1 / MISO1 / ETH2_RXD1	MDAT 4	—	—	ENCIF13
C5	—	—	P23_4	D19 / CS5#	MTCLKD	—	—	—	—	—
C6	—	—	P22_7	D14	—	SCK0 / IIC_SDA1	—	—	—	—
C7	—	TRACECTL	P22_1	D8	POE4#	SS4# / CTS4# / RTS4# / ESC_LINKACT2	—	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (3 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
C8	—	TRACEDATA1	P21_2	D1	MTIOC6B / GTIOC14B / CMTW0_TIC1	RXD5 / SCL5 / MISO5 / IIC_SDA1 / SPI_MISO2	MDAT 0	—	—	ENCIF6
C9	—	MDV2	P20_3	—	—	ETHSW_TDMAOUT2 / ESC_LEDERR	—	—	—	—
C10	—	—	P20_6	—	MTIOC1B	IIC_SDA0 / ESC_I2CDATA	MDAT 4	—	—	—
C11	—	MDV0	P20_1	—	—	ETHSW_TDMAOUT0 / ESC_LINKACT0	—	—	—	—
C12	—	—	—	—	—	—	—	—	AN115	—
C13	—	—	—	—	—	—	—	—	AN111	—
C14	—	VREFH1	—	—	—	—	—	—	—	—
C15	—	VREFH0	—	—	—	—	—	—	—	—
C16	—	—	—	—	—	—	—	—	AN001	—
C17	—	—	—	—	—	—	—	—	AN005	—
C18	—	VSS	—	—	—	—	—	—	—	—
C19	—	AVCC18_TSU	—	—	—	—	—	—	—	—
C20	—	—	P19_4	—	MTIOC7A / GTIOC6A	—	—	—	—	—
D1	VCC1833_2	—	P01_3	WE3# / DQMUU / AH#	MTIOC4D / GTIOC3B	ETH2_TXD2	—	—	—	—
D2	VCC1833_2	—	P01_2	CS2#	MTIOC4B / GTIOC2B	ETH2_TXD3	—	IRQ2	—	—
D3	VCC1833_2	—	P00_6	CS5#	MTIOC3B / GTIOC1A	ETH2_TXCLK	—	—	—	—
D18	—	—	P19_6	—	MTIOC6D / GTIOC5B	—	—	—	—	—
D19	—	—	P19_2	—	MTIOC6C / GTIOC4B	—	—	IRQ3	—	—
D20	—	MDV4	P19_0	—	—	USB_VBUSEN	—	—	—	—
E1	—	VSS	—	—	—	—	—	—	—	—
E2	—	TRACEDATA0	P01_6	A20	MTIOC1A / GTIOC9A	CTS1# / GMAC_PTPTRG1 / ESC_LATCH1 / ESC_LATCH0 / CANTXDP1	—	—	—	ENCIF0
E3	VCC1833_2	—	P01_0	CAS#	MTIOC4C / GTIOC3A	CTS2# / GMAC_MDIO / ETHSW_MDIO / ESC_MDIO	MCLK 1	—	—	—
E5	VCC1833_2	—	P24_2	D25 / D14 / RAS#	MTIOC0D / GTETRGD	TXD1 / SDA1 / MOSI1 / ETH2_RXD2	MDAT 5	—	—	ENCIF15
E6	—	—	P23_1	D16 / WE0# / DQMLL	MTCLKA	—	—	NMI	—	—
E7	—	—	P22_6	D13	—	DE4 / IIC_SCL1	—	—	—	—
E8	—	—	P22_4	D11	—	—	—	—	—	—
E9	—	TRACEDATA5	P21_6	D5 / TEND	MTIOC7B / GTIOC16B	CTS0#	MDAT 2	IRQ9	—	—
E10	—	—	P20_7	—	MTIOC2A / GTIOC13A	ETHSW_PTPOUT2 / ESC_RESETOUT#	MCLK 5	—	—	—
E11	—	VCC33	—	—	—	—	—	—	—	—
E12	—	—	—	—	—	—	—	—	AN109	—
E13	—	—	—	—	—	—	—	—	AN102	—
E14	—	VSS	—	—	—	—	—	—	—	—
E15	—	VSS	—	—	—	—	—	—	—	—
E16	—	—	—	—	—	—	—	—	AN003	—
E18	—	—	P19_1	—	MTIOC6A / GTIOC4A	—	—	—	—	—
E19	—	TRACECLK	P18_6	—	MTIC5W	SCK4 / IIC_SCL2 / SPI_MISO2	—	IRQ11	ADTRG0#	ENCIF15
E20	—	TRACECTL	P18_5	—	MTIC5V	RXD4 / SCL4 / MISO4 / SPI_MOSI2	—	—	—	ENCIF14
F1	—	MDW	P02_1	A17	—	ETHSW_PTPOUT1 / ESC_SYNC1 / ESC_SYNC0	—	—	—	—
F2	—	TRACEDATA1	P01_7	A19	MTIOC1B / GTIOC9B	SCK1 / ETHSW_LPI1 / CANRX0 / SPI_RSPCK3	—	—	ADTRG0#	ENCIF1

Table 1.18 List of pins and pin functions (320-pin FBGA) (4 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
F3	VCC1833_2	—	P01_5	WE0# / DQMLL	—	ETH2_TXD0	—	—	—	—
F5	VCC1833_2	—	P00_1	D27 / A13	MTIC5U	RXD2 / SCL2 / MISO2 / ETH2_RXDV	—	IRQ0	—	—
F6	—	VCC1833_2	—	—	—	—	—	—	—	—
F7	—	—	P23_5	D20 / CS2#	MTIOC8A	TXD0 / SDA0 / MOSI0	—	—	—	—
F8	—	—	P23_3	D18 / WE3# / DQMUU / AH#	MTCLKC	RXD0 / SCL0 / MISO0	—	—	—	—
F9	—	TRACECLK	P22_2	D9	MTIOC8C / GTETRGSA	SPI_SSL12	—	IRQ4	—	ENCIF10
F10	—	—	P20_5	—	MTIOC1A	IIC_SCL0 / ESC_I2CCLK	MCLK 4	—	—	—
F11	—	VCC18_ADC1	—	—	—	—	—	—	—	—
F12	—	VSS	—	—	—	—	—	—	—	—
F13	—	—	—	—	—	—	—	—	AN100	—
F14	—	VCC18_ADC0	—	—	—	—	—	—	—	—
F15	—	VCC33	—	—	—	—	—	—	—	—
F16	—	VSS	—	—	—	—	—	—	—	—
F18	—	—	P18_7	—	POE4# / GTETRGD	IIC_SDA2 / USB_VBUSEN / SPI_SSL20	—	IRQ2	—	—
F19	—	—	P18_4	—	MTIC5U	TXD4 / SDA4 / MOSI4 / SPI_RSPCK2	—	IRQ1	—	ENCIF13
F20	—	—	P18_2	—	MTIOC4B / MTIOC4D / GTIOC2B / GTIOC3B	—	—	—	—	ENCIF11
G1	—	—	P02_3	A15 / WE3# / DQMUU / AH#	MTIOC2B / POE11# / GTIOC10B	SS1# / CTS1# / RTS1# / ETHSW_TDMAOUT1 / CANRX1 / SPI_SSL30	—	IRQ15	—	ENCIF4
G2	—	TRST#	—	—	—	—	—	—	—	—
G3	—	TDO	P02_4	WE0# / DQMLL	—	DE1 / SPI_SSL33	—	—	—	—
G5	VCC1833_2	—	P00_5	D31 / CS0#	MTIOC3C / GTIOC0B	ETHSW_PHYLINK2 / ESC_PHYLINK2	MDAT 0	—	—	—
G6	VCC1833_2	—	P00_4	D30 / WAIT#	MTIOC3A / GTIOC0A	ETH2_RXER	MCLK 0	IRQ13	—	—
G15	—	—	P19_7	—	MTIOC7B / GTIOC6B	—	—	—	—	—
G16	—	—	P19_5	—	MTIOC7C / GTIOC7A	—	—	—	—	—
G18	—	—	P18_3	—	MTIOC4D / MTIOC4B / GTIOC3B / GTIOC2B / CMTW1_TIC1	CANRXDP1	—	IRQ0	—	ENCIF12
G19	—	—	P18_1	—	MTIOC3D / GTIOC1B	SS3# / CTS3# / RTS3#	—	IRQ10	ADTRG1#	ENCIF10
G20	—	—	P17_7	DACK	MTIOC4A / MTIOC4C / GTIOC2A / GTIOC3A	RXD3 / SCL3 / MISO3	—	—	—	ENCIF9
H1	—	VSS	—	—	—	—	—	—	—	—
H2	—	TDI	P02_5	WE1# / DQMLU	—	SCK5 / ETHSW_TDMAOUT3 / SPI_SSL31	—	—	—	ENCIF5
H3	—	TMS	P02_6	—	—	RXD5 / SCL5 / MISO5	—	—	—	ENCIF6
H5	VCC1833_2	—	P01_4	WE1# / DQMLU	POE0#	ETH2_TXD1	—	IRQ3	—	—
H6	VCC1833_2	—	P01_1	CKE	MTIOC3D / GTIOC1B	DE2 / GMAC_MDC / ETHSW_MDC / ESC_MDC	MDAT 1	—	—	—
H8	—	VDD	—	—	—	—	—	—	—	—
H9	—	VSS	—	—	—	—	—	—	—	—
H10	—	VDD	—	—	—	—	—	—	—	—
H11	—	VDD	—	—	—	—	—	—	—	—
H12	—	VDD	—	—	—	—	—	—	—	—
H13	—	VDD	—	—	—	—	—	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (5 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
H15	—	—	P19_3	—	MTIOC6B / GTIOC5A	—	—	—	—	—
H16	—	—	P18_0	—	MTIOC4C / MTIOC4A / GTIOC3A / GTIOC2A	TXD3 / SDA3 / MOSI3	—	—	—	—
H18	—	RSTOUT#	P17_5	TEND	MTIOC3A / GTETRGC / GTIOC0B	USB_OVRCUR	—	—	—	ENCIF7
H19	—	TRACECTL	P17_3	DREQ	POE0# / GTETRGA	SPI_SSL31	—	—	ADTRG1#	ENCIF5
H20	—	—	P17_2	—	CMTW1_TIC0	—	—	IRQ9	—	—
J1	—	BSCANP	—	—	—	—	—	—	—	—
J2	—	TCK	P02_7	—	—	TXD5 / SDA5 / MOSI5	—	—	—	ENCIF7
J3	—	—	P03_2	A13	—	CTS2# / ETHSW_TDMAOUT2 / CANRXDP0	—	NMI	—	—
J5	—	—	P02_2	A16	MTIOC2A / POE10# / GTIOC10A / RTCAT1HZ	TXD1 / SDA1 / MOSI1 / ETHSW_TDMAOUT0 / CANTX0 / SPI_MOSI3	—	IRQ14	—	ENCIF3
J6	—	TRACEDATA2	P02_0	A18	GTADSML0	RXD1 / SCL1 / MISO1 / ETHSW_LPI2 / USB_OTGID / CANTX1 / SPI_MISO3	—	IRQ4	—	ENCIF2
J8	—	VDD	—	—	—	—	—	—	—	—
J9	—	VSS	—	—	—	—	—	—	—	—
J10	—	VSS	—	—	—	—	—	—	—	—
J11	—	VSS	—	—	—	—	—	—	—	—
J12	—	VSS	—	—	—	—	—	—	—	—
J13	—	VDD	—	—	—	—	—	—	—	—
J15	—	MDD	P17_0	—	—	SS0# / CTS0# / RTS0# / ESC_IRQ	—	—	—	—
J16	—	TRACECLK	P17_4	—	MTIOC3C / GTETRGB / GTIOC0A	CTS3# / SPI_SSL32	—	—	—	ENCIF6
J18	—	—	P17_6	—	MTIOC3B / GTIOC1A	SCK3	—	—	—	ENCIF8
J19	—	—	P16_7	—	MTIC5W	SCK0	—	—	—	—
J20	—	—	P17_1	—	—	DE0	—	—	—	—
K1	—	TRACEDATA5	P03_7	A10	MTIOC3C / GTIOC5A	SCK3 / ETH2_TXER	—	IRQ9	—	—
K2	—	—	P03_5	A12	MTIOC3A / GTIOC4A	RXD2 / SCL2 / MISO2 / ETH2_CRS	MCLK2	IRQ5	—	—
K3	—	—	P03_3	WAIT# / TEND	—	DE2 / USB_OTGID	—	IRQ11	—	ENCIF9
K5	—	—	P03_4	RD/WR#	—	SS2# / CTS2# / RTS2# / SPI_SSL03	—	IRQ7	—	—
K6	—	TRACEDATA3	P03_0	A14 / CS5#	GTADSML1	SCK2 / CANTXDP1 / SPI_SSL32	—	IRQ14	—	ENCIF8
K8	—	VDD	—	—	—	—	—	—	—	—
K9	—	VSS	—	—	—	—	—	—	—	—
K10	—	VSS	—	—	—	—	—	—	—	—
K11	—	VSS	—	—	—	—	—	—	—	—
K12	—	VSS	—	—	—	—	—	—	—	—
K13	—	VDD	—	—	—	—	—	—	—	—
K15	VCC1833_3	—	P15_6	—	—	SPI_SSL12 / XSPI0_IO7	MDAT2	—	—	—
K16	VCC1833_3	—	P16_3	—	GTADSMP1	SCK0 / ETH1_TXER / SPI_SSL30 / XSPI0_RSTO#	—	IRQ7	—	ENCIF4
K18	—	—	P16_6	—	MTIC5V	RXD0 / SCL0 / MISO0	—	IRQ8	—	—
K19	—	—	P16_5	—	MTIC5U	TXD0 / SDA0 / MOSI0	—	—	—	—
K20	—	VSS	—	—	—	—	—	—	—	—
L1	—	VSS	—	—	—	—	—	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (6 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
L2	—	TRACEDATA6	P04_0	A9	MTIOC3D / GTIOC5B	RXD3 / SCL3 / MISO3	—	—	—	—
L3	—	TRACEDATA4	P03_6	A11	MTIOC3B / GTIOC4B	TXD2 / SDA2 / MOSI2 / ETH2_COL / SPI_SSL13	MDAT2	IRQ8	—	—
L5	—	TRACEDATA7	P04_4	A8	POE10# / GTADSMP0	CTS3# / SPI_RSPCK1	—	IRQ10	—	ENCIF10
L6	—	VCC33	—	—	—	—	—	—	—	—
L8	—	VDD	—	—	—	—	—	—	—	—
L9	—	VSS	—	—	—	—	—	—	—	—
L10	—	VSS	—	—	—	—	—	—	—	—
L11	—	VSS	—	—	—	—	—	—	—	—
L12	—	VSS	—	—	—	—	—	—	—	—
L13	—	VDD	—	—	—	—	—	—	—	—
L15	—	VCC1833_3	—	—	—	—	—	—	—	—
L16	VCC1833_3	—	P15_1	A24	MTIOC0C	TXD5 / SDA5 / MOSI5 / SPI_SSL10 / XSPI0_IO2	—	—	—	—
L18	VCC1833_3	—	P16_1	—	CMTW0_TOC1	RXD0 / SCL0 / MISO0 / SPI_MISO3 / XSPI0_RESET0#	MDAT3	—	ADTRG0#	ENCIF2
L19	VCC1833_3	—	P16_2	—	—	CTS0# / USB_EXICEN / SPI_RSPCK3 / XSPI0_RESET1#	—	NMI	—	ENCIF3
L20	VCC1833_3	—	P16_4	—	—	—	—	—	—	—
M1	—	—	P04_1	CKIO	—	TXD3 / SDA3 / MOSI3 / IIC_SDA2 / SPI_MOSI0	—	—	—	—
M2	—	—	P04_2	CS0#	—	—	—	—	—	—
M3	—	—	P04_3	RD#	—	SS3# / CTS3# / RTS3# / IIC_SCL2 / USB_OVRCUR / SPI_RSPCK0	—	—	—	—
M5	—	MD1	P04_6	A6 / DACK	RTCAT1HZ	ETH1_TXER	—	—	—	—
M6	—	—	P05_0	A4	MTIOC4A / GTIOC6A / CMTW0_TOC0	SS5# / CTS5# / RTS5# / ETH1_CRS / USB_VBUSEN / CANTXDP0	MCLK3	IRQ12	—	ENCIF11
M8	—	VDD	—	—	—	—	—	—	—	—
M9	—	VSS	—	—	—	—	—	—	—	—
M10	—	VSS	—	—	—	—	—	—	—	—
M11	—	VSS	—	—	—	—	—	—	—	—
M12	—	VSS	—	—	—	—	—	—	—	—
M13	—	VDD	—	—	—	—	—	—	—	—
M15	VCC1833_3	—	P15_0	A23	—	RXD5 / SCL5 / MISO5 / SPI_MOSI1 / XSPI0_IO1	—	—	—	—
M16	VCC1833_3	—	P14_2	—	MTIOC8B / GTIOC8B	ETH0_CRS / XSPI0_ECS0#	—	IRQ6	—	ENCIF12
M18	VCC1833_3	—	P15_3	—	MTIOC8C	XSPI0_IO4	MCLK1	—	—	—
M19	VCC1833_3	—	P15_7	TEND	—	CTS5# / SPI_SSL13 / XSPI0_CS0#	—	—	—	ENCIF1
M20	VCC1833_3	—	P16_0	—	—	TXD0 / SDA0 / MOSI0 / ETH0_TXER / SPI_MOSI3 / XSPI0_CS1#	MCLK3	—	—	ENCIF0
N1	—	MD0	P04_5	A7	—	DE3	—	—	—	—
N2	—	MD2	P04_7	A5	—	ETH0_TXER / SPI_SSL21	—	—	—	—
N3	—	—	P05_1	A3	MTIOC4B / GTIOC6B / CMTW0_TIC1	CTS5# / ETH1_COL / USB_EXICEN / CANRXDP0	MDAT3	IRQ13	—	ENCIF12
N5	VCC1833_1	—	P05_4	A0 / DACK	GTIOC14A	RXD4 / SCL4 / MISO4 / ETHSW_LPI0 / USB_OVRCUR / CANTXDP0 / SPI_SSL00	—	IRQ12	—	ENCIF15
N6	—	VCC1833_1	—	—	—	—	—	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (7 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
N8	—	VDD	—	—	—	—	—	—	—	—
N9	—	VDD	—	—	—	—	—	—	—	—
N10	—	VDD	—	—	—	—	—	—	—	—
N11	—	VDD	—	—	—	—	—	—	—	—
N12	—	VSS	—	—	—	—	—	—	—	—
N13	—	VDD	—	—	—	—	—	—	—	—
N15	VCC1833_3	—	P13_7	—	MTCLKC	GMAC_PTPTRG1 / ESC_LATCH1 / ESC_LATCH0 / XSPI0_ECS1#	—	—	—	—
N16	VCC1833_3	—	P13_5	—	MTCLKA	GMAC_PTPTRG0 / ESC_LATCH0 / ESC_LATCH1 / SPI_RSPCK1 / XSPI0_WP1#	—	—	—	—
N18	VCC1833_3	—	P14_5	CS3#	POE8#	XSPI0_CKN	—	—	—	—
N19	VCC1833_3	—	P15_4	—	MTIOC8D	XSPI0_IO5	MDAT 1	—	—	—
N20	VCC1833_3	—	P15_5	—	—	XSPI0_IO6	MCLK 2	—	—	—
P1	—	VSS	—	—	—	—	—	—	—	—
P2	—	—	P05_3	A1	MTIOC4D / POE11# / GTETRGSB / GTIOC7B / CMTW0_TIC0	SCK4 / IIC_SDA1 / ETH0_COL / USB_EXICEN / CANTX0	—	IRQ15	—	ENCIF14
P3	—	—	P05_2	A2 / DREQ	MTIOC4C / GTETRGSA / GTIOC7A / CMTW0_TOC0	DE5 / IIC_SCL1 / ETH0_CRS / USB_VBUSEN / CANRX0	—	IRQ14	—	ENCIF13
P5	VCC1833_1	—	P06_3	D23	GTIOC17B / CMTW1_TIC1	DE4 / ETH1_TXD0 / CANTXDP1 / SPI_MISO1	—	—	—	—
P6	VCC1833_1	—	P05_7	D18	GTIOC15B / CMTW1_TOC1	TXD4 / SDA4 / MOSI4 / ETH1_TXD2 / SPI_SSL23	—	—	—	—
P15	VCC1833_4	TRACEDATA3	P12_7	D12	MTCLKB / MTCLKC	SCK1 / SPI_SSL01 / XSPI1_IO1	MDAT 5	IRQ4	—	ENCIF2
P16	VCC1833_4	TRACEDATA6	P13_2	D9	MTIOC0A / POE8# / GTIOC10A	SS1# / CTS1# / RTS1# / IIC_SCL0 / ETHSW_PTPOUT2 / ESC_I2CCLK / SPI_MISO0 / XSPI1_CS1#	MCLK 4	IRQ5	—	ENCIF8
P18	VCC1833_3	—	P14_6	A21	—	XSPI0_CKP	—	—	—	—
P19	VCC1833_3	—	P14_7	A22	—	SCK5 / SPI_MISO1 / XSPI0_IO0	—	—	—	—
P20	VCC1833_3	—	P15_2	A25	MTIOC0D	SS5# / CTS5# / RTS5# / SPI_SSL11 / XSPI0_IO3	—	—	—	—
R1	VCC1833_1	—	P05_5	D16	GTIOC14B / CMTW0_TOC1	ETHSW_PHYLINK1 / ESC_PHYLINK1 / SPI_RSPCK2	—	—	—	—
R2	VCC1833_1	—	P05_6	D17	GTIOC15A / CMTW1_TIC0	ETH1_RXER / SPI_SSL22	—	IRQ12	—	—
R3	VCC1833_1	—	P06_1	D22	GTIOC16B	CTS4# / ETH1_REFCLK / RMII1_REFCLK / CANTX1 / SPI_SSL22	—	—	—	—
R5	VCC1833_1	—	P07_1	D28	GTIOC13B	ETH1_RXD3	—	—	—	—
R6	—	—	P07_6	A22 / D23	—	SPI_SSL21	—	—	—	—
R7	—	VCC33	—	—	—	—	—	—	—	—
R8	VCC1833_0	—	P09_4	—	—	ETH0_TXD2	—	—	—	—
R9	VCC1833_0	—	P09_7	—	—	ETH0_TXCLK	—	—	—	—
R10	—	VCC1833_0	—	—	—	—	—	—	—	—
R11	VCC1833_0	—	P10_4	WE2# / DQMUL	—	ETHSW_PHYLINK0 / ESC_PHYLINK0	—	IRQ11	—	—
R12	VCC1833_4	—	P11_2	—	MTIOC1B / GTIOC11B	ETH1_TXER / XSPI1_WP0#	—	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (8 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
R13	VCC1833_4	—	P11_6	—	MTIOC8C	ETH0_COL / XSPI1_RESET1#	—	—	—	ENCIF1
R14	—	VCC1833_4	—	—	—	—	—	—	—	—
R15	VCC1833_4	TRACEDATA1	P12_5	D14 / DACK	MTIOC8A / GTIOC8A	SPI_SSL03 / XSPI1_IO3	—	—	—	ENCIF0
R16	VCC1833_4	—	P12_3	—	GTADSMP0	XSPI1_IO4	—	—	—	ENCIF6
R18	VCC1833_3	—	P13_6	—	MTCLKB	ETHSW_PTPOUT0 / ESC_SYNC0 / ESC_SYNC1 / XSPI0_WP0#	—	—	—	—
R19	VCC1833_3	—	P14_4	BS	MTIOC0B	ESC_IRQ / XSPI0_DS	—	—	—	—
R20	—	VSS	—	—	—	—	—	—	—	—
T1	VCC1833_1	—	P06_0	D19	GTIOC16A / CMTW1_TOC0	SS4# / CTS4# / RTS4# / ETH1_TXD3 / CANRX1 / SPI_SSL23	—	—	—	—
T2	VCC1833_1	—	P06_2	D20	GTIOC17A	ETH1_TXD1 / CANRXDP1	—	—	—	—
T3	VCC1833_1	—	P06_5	D25	GTIOC11B	ETH1_TXEN	—	—	—	—
T5	—	RES#	—	—	—	—	—	—	—	—
T6	—	—	P08_3	D28	—	ETHSW_PTPOUT0 / ESC_SYNC0 / ESC_SYNC1	—	—	—	—
T7	VCC1833_0	—	P09_0	D30	MTIOC7A	GMAC_MDIO / ETHSW_MDIO / ESC_MDIO	—	—	—	—
T8	VCC1833_0	—	P09_1	—	MTIOC7B	ETH0_REFCLK / RMII0_REFCLK	—	—	—	—
T9	VCC1833_0	—	P09_5	—	—	ETH0_TXD1	—	—	—	—
T10	—	VSS	—	—	—	—	—	—	—	—
T11	—	VSS	—	—	—	—	—	—	—	—
T12	VCC1833_4	—	P10_6	—	—	ETH2_COL / XSPI1_INT1#	—	—	—	—
T13	VCC1833_4	—	P10_5	—	—	ETH2_CRS	—	IRQ2	—	—
T14	VCC1833_4	—	P10_7	—	—	ETH2_TXER / XSPI1_INT0#	—	—	—	—
T15	VCC1833_4	—	P11_3	—	MTIOC2A / GTIOC12A	ETH0_TXER / XSPI1_ECS0#	—	—	—	—
T16	VCC1833_4	—	P12_1	—	GTADSML0	XSPI1_IO6	—	—	—	ENCIF4
T18	VCC1833_4	TRACEDATA5	P13_1	D10	MTCLKD / GTIOC9B	TXD1 / SDA1 / MOSI1 / SPI_MOSI0 / XSPI1_CS0#	MDAT 0	—	—	ENCIF4
T19	VCC1833_3	—	P14_0	—	MTCLKD	ETHSW_PTPOUT1 / ESC_SYNC1 / ESC_SYNC0 / XSPI0_INT0#	—	—	—	—
T20	VCC1833_3	—	P14_3	—	MTIOC0A	ETH0_COL / XSPI0_RSTO1#	—	—	—	ENCIF13
U1	VCC1833_1	—	P06_4	D24	GTIOC11A	ETH1_TXCLK / SPI_MOSI1	—	—	—	—
U2	VCC1833_1	—	P06_6	D21	GTIOC12A	ETH1_RXD0 / SPI_SSL10	—	—	—	—
U3	VCC1833_1	—	P07_3	D30	—	ETH1_RXCLK	—	—	—	—
U18	VCC1833_4	TRACEDATA0	P12_4	D15	MTIOC8B / GTIOC8B	ETH1_CRS / SPI_SSL01 / XSPI1_RESET0#	—	—	—	ENCIF7
U19	VCC1833_4	TRACEDATA7	P13_3	D8	MTIOC0C / MTIOC0B / GTIOC10B / CMTW1_TOC0	CTS1# / IIC_SDA0 / ETHSW_PTPOUT3 / ESC_I2CDATA / SPI_RSPCK0 / XSPI1_CKP	MDAT 4	—	—	ENCIF9
U20	VCC1833_3	—	P14_1	—	MTIOC8A / GTIOC8A	ETH1_COL / XSPI0_INT1#	—	—	—	ENCIF11
V1	VCC1833_1	—	P06_7	D26	GTIOC12B	ETH1_RXD1 / SPI_SSL11	—	—	—	—
V2	VCC1833_1	—	P07_0	D27	GTIOC13A	ETH1_RXD2	—	—	—	—
V3	—	MDX	—	—	—	—	—	—	—	—
V4	—	—	P07_5	A21 / D22	—	—	—	—	—	—
V5	—	—	P08_0	A24 / D25	—	ETHSW_LPI0	—	—	—	—
V6	—	—	P08_2	D27	—	GMAC_PTPTRG0 / ESC_LATCH0 / ESC_LATCH1	—	—	—	—
V7	VCC1833_0	—	P08_6	—	MTIOC6C	ETH0_RXCLK	—	—	—	—
V8	VCC1833_0	—	P10_2	—	—	ETH0_RXD1	—	—	—	—

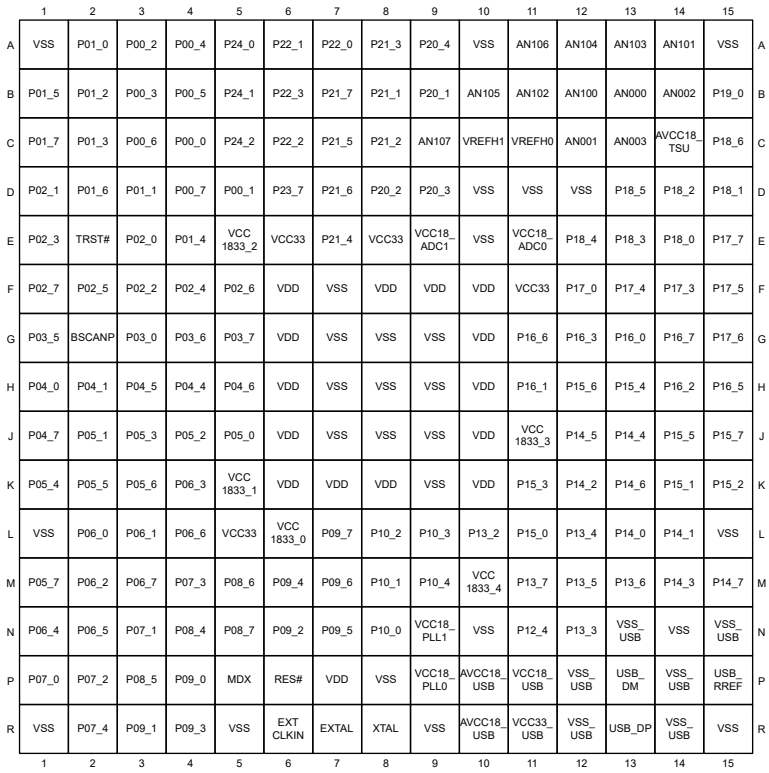
Table 1.18 List of pins and pin functions (320-pin FBGA) (9 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
V9	VCC1833_0	—	P10_3	—	RTCAT1HZ	ETH0_RXD2	—	—	—	—
V10	—	VCC18_PLL0	—	—	—	—	—	—	—	—
V11	—	VCC18_PLL1	—	—	—	—	—	—	—	—
V12	—	VCC18_USB	—	—	—	—	—	—	—	—
V13	—	AVCC18_USB	—	—	—	—	—	—	—	—
V14	—	AVCC18_USB	—	—	—	—	—	—	—	—
V15	—	VSS_USB	—	—	—	—	—	—	—	—
V16	VCC1833_4	—	P11_1	—	MTIOC1A / GTIOC11A	ETH1_COL / XSPI1_WP1#	—	—	—	—
V17	VCC1833_4	—	P11_4	—	MTIOC2B / GTIOC12B	ETH0_CRS / XSPI1_RSTO1#	—	—	—	—
V18	VCC1833_4	—	P12_0	—	GTADSMP1	XSPI1_IO7	—	—	—	ENCIF3
V19	VCC1833_4	TRACEDATA2	P12_6	D13	MTCLKA	DE1 / SPI_SSL02 / XSPI1_IO2	MCLK 5	IRQ3	—	ENCIF1
V20	VCC1833_4	—	P13_4	—	MTIOC0D / GTIOC8B	ESC_RESETOUT# / XSPI1_CKN	—	—	—	ENCIF10
W1	VCC1833_1	—	P07_2	D29	—	ETH1_RXDV	—	—	—	—
W2	—	—	P07_4	—	—	USB_VBUSIN	—	IRQ1	ADTRG0#	—
W3	—	—	P07_7	A23 / D24	—	ETHSW_LPI1	—	—	—	—
W4	VCC1833_0	—	P08_4	D31	MTIOC6A	ETH0_RXD3	—	—	—	—
W5	VCC1833_0	—	P08_7	D29	MTIOC6D	GMAC_MDC / ETHSW_MDC / ESC_MDC	—	—	—	—
W6	VCC1833_0	—	P09_3	—	MTIOC7D	ETH0_TXD3	—	—	—	—
W7	VCC1833_0	—	P10_0	—	—	ETH0_TXEN	—	—	—	—
W8	—	VSS	—	—	—	—	—	—	—	—
W9	—	VSS	—	—	—	—	—	—	—	—
W10	—	VDD	—	—	—	—	—	—	—	—
W11	—	VSS	—	—	—	—	—	—	—	—
W12	—	VCC33_USB	—	—	—	—	—	—	—	—
W13	—	VSS_USB	—	—	—	—	—	—	—	—
W14	—	VSS_USB	—	—	—	—	—	—	—	—
W15	—	VSS_USB	—	—	—	—	—	—	—	—
W16	—	VSS_USB	—	—	—	—	—	—	—	—
W17	—	VSS_USB	—	—	—	—	—	—	—	—
W18	VCC1833_4	—	P11_5	—	MTIOC0B	XSPI1_RSTO0#	—	—	—	ENCIF0
W19	VCC1833_4	—	P12_2	—	GTADSML1	XSPI1_IO5	—	—	—	ENCIF5
W20	VCC1833_4	TRACEDATA4	P13_0	D11	MTCLKC / MTCLKB / GTIOC9A	RXD1 / SCL1 / MISO1 / SPI_SSL00 / XSPI1_IO0	MCLK 0	—	—	ENCIF3
Y1	—	VSS	—	—	—	—	—	—	—	—
Y2	—	—	P08_1	A25 / D26	—	ETHSW_LPI2 / USB_VBUSEN	—	—	—	—
Y3	VCC1833_0	—	P08_5	—	MTIOC6B	ETH0_RXDV	—	—	—	—
Y4	—	VSS	—	—	—	—	—	—	—	—
Y5	VCC1833_0	—	P09_2	D31	MTIOC7C	ETH0_RXER	—	IRQ0	—	—
Y6	VCC1833_0	—	P09_6	—	—	ETH0_TXD0	—	—	—	—
Y7	VCC1833_0	—	P10_1	—	—	ETH0_RXD0	—	—	—	—
Y8	—	VSS	—	—	—	—	—	—	—	—
Y9	—	EXTCLKIN	—	—	—	—	—	—	—	—
Y10	—	EXTAL	—	—	—	—	—	—	—	—
Y11	—	XTAL	—	—	—	—	—	—	—	—
Y12	—	VSS_USB	—	—	—	—	—	—	—	—
Y13	—	USB_DM	—	—	—	—	—	—	—	—

Table 1.18 List of pins and pin functions (320-pin FBGA) (10 of 10)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
Y14	—	USB_DP	—	—	—	—	—	—	—	—
Y15	—	VSS_USB	—	—	—	—	—	—	—	—
Y16	—	USB_RREF	—	—	—	—	—	—	—	—
Y17	—	VSS_USB	—	—	—	—	—	—	—	—
Y18	VCC1833_4	—	P11_0	—	—	ETH1_CRS / XSPI1_ECS1#	—	—	—	—
Y19	VCC1833_4	—	P11_7	—	MTIOC8D	USB_OVRCUR / XSPI1_DS	—	—	—	ENCIF2
Y20	—	VSS	—	—	—	—	—	—	—	—

1.7 FBGA 225 Pin Assignments



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	VSS	P01_0	P00_2	P00_4	P24_0	P22_1	P22_0	P21_3	P20_4	VSS	AN106	AN104	AN103	AN101	VSS	A
B	P01_5	P01_2	P00_3	P00_5	P24_1	P22_3	P21_7	P21_1	P20_1	AN105	AN102	AN100	AN000	AN002	P19_0	B
C	P01_7	P01_3	P00_6	P00_0	P24_2	P22_2	P21_5	P21_2	AN107	VREFH1	VREFH0	AN001	AN003	AVCC18_ TSU	P18_6	C
D	P02_1	P01_6	P01_1	P00_7	P00_1	P23_7	P21_6	P20_2	P20_3	VSS	VSS	VSS	P18_5	P18_2	P18_1	D
E	P02_3	TRST#	P02_0	P01_4	VCC 1833_2	VCC33	P21_4	VCC33	VCC18_ ADC1	VSS	VCC18_ ADC0	P18_4	P18_3	P18_0	P17_7	E
F	P02_7	P02_5	P02_2	P02_4	P02_6	VDD	VSS	VDD	VDD	VDD	VCC33	P17_0	P17_4	P17_3	P17_5	F
G	P03_5	BSCANP	P03_0	P03_6	P03_7	VDD	VSS	VSS	VSS	VDD	P16_6	P16_3	P16_0	P16_7	P17_6	G
H	P04_0	P04_1	P04_5	P04_4	P04_6	VDD	VSS	VSS	VSS	VDD	P16_1	P15_6	P15_4	P16_2	P16_5	H
J	P04_7	P05_1	P05_3	P05_2	P05_0	VDD	VSS	VSS	VSS	VDD	VCC 1833_3	P14_5	P14_4	P15_5	P15_7	J
K	P05_4	P05_5	P05_6	P06_3	VCC 1833_1	VDD	VDD	VDD	VSS	VDD	P15_3	P14_2	P14_6	P15_1	P15_2	K
L	VSS	P06_0	P06_1	P06_6	VCC33	VCC 1833_0	P09_7	P10_2	P10_3	P13_2	P15_0	P13_4	P14_0	P14_1	VSS	L
M	P05_7	P06_2	P06_7	P07_3	P08_6	P09_4	P09_6	P10_1	P10_4	VCC 1833_4	P13_7	P13_5	P13_6	P14_3	P14_7	M
N	P06_4	P06_5	P07_1	P08_4	P08_7	P09_2	P09_5	P10_0	VCC18_ PLL1	VSS	P12_4	P13_3	VSS_ USB	VSS	VSS_ USB	N
P	P07_0	P07_2	P08_5	P09_0	MDX	RES#	VDD	VSS	VCC18_ PLL0	AVCC18_ USB	VCC18_ USB	VSS_ USB	USB_ DM	VSS_ USB	USB_ RREF	P
R	VSS	P07_4	P09_1	P09_3	VSS	EXT CLKIN	EXTAL	XTAL	VSS	AVCC18_ USB	VCC33_ USB	VSS_ USB	USB_DP	VSS_ USB	VSS	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.3 Pin arrangement (225-pin FBGA) (top view)

Table 1.19 List of pins and pin functions (225-pin FBGA) (1 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
A1	—	VSS	—	—	—	—	—	—	—	—
A2	VCC1833_2	—	P01_0	CAS#	MTIOC4C / GTIOC3A	CTS2# / GMAC_MDIO / ETHSW_MDIO / ESC_MDIO	MCLK 1	—	—	—
A3	VCC1833_2	—	P00_2	D28 / RD#	MTIC5V	TXD2 / SDA2 / MOSI2 / ETH2_TXEN / USB_OVRCUR	—	—	—	—
A4	VCC1833_2	—	P00_4	D30 / WAIT#	MTIOC3A / GTIOC0A	ETH2_RXER	MCLK 0	IRQ13	—	—
A5	VCC1833_2	—	P24_0	D23 / D12 / CKE / DREQ	MTIOC0B / GTETRGB	RXD1 / SCL1 / MISO1 / ETH2_RXD1	MDAT 4	—	—	ENCIF13
A6	—	TRACECTL	P22_1	D8	POE4#	SS4# / CTS4# / RTS4# / ESC_LINKACT2	—	—	—	—
A7	—	TRACEDATA7	P22_0	D7	MTIOC7D / GTIOC17B	DE5	MDAT 3	IRQ15	—	—
A8	—	TRACEDATA2	P21_3	D2	MTIOC6C / GTIOC15A	TXD5 / SDA5 / MOSI5 / SPI_SSL33	MCLK 1	—	—	ENCIF7
A9	—	MDV3	P20_4	—	—	ETHSW_TDMAOUT3 / ESC_LINKACT1	—	—	—	—
A10	—	VSS	—	—	—	—	—	—	—	—
A11	—	—	—	—	—	—	—	—	AN106	—
A12	—	—	—	—	—	—	—	—	AN104	—
A13	—	—	—	—	—	—	—	—	AN103	—
A14	—	—	—	—	—	—	—	—	AN101	—
A15	—	VSS	—	—	—	—	—	—	—	—
B1	VCC1833_2	—	P01_5	WE0# / DQMLL	—	ETH2_TXD0	—	—	—	—

Table 1.19 List of pins and pin functions (225-pin FBGA) (2 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
B2	VCC1833_2	—	P01_2	CS2#	MTIOC4B / GTIOC2B	ETH2_TXD3	—	IRQ2	—	—
B3	VCC1833_2	—	P00_3	D29 / RD/WR#	MTIC5W	SS2# / CTS2# / RTS2# / ETH2_REFCLK / RMII2_REFCLK	—	IRQ1	—	—
B4	VCC1833_2	—	P00_5	D31 / CS0#	MTIOC3C / GTIOC0B	ETHSW_PHYLINK2 / ESC_PHYLINK2	MDAT 0	—	—	—
B5	VCC1833_2	—	P24_1	D24 / D13 / CAS#	MTIOC0C / POE8# / GTETRGC	ETH2_RXCLK	MCLK 5	—	—	ENCIF14
B6	—	—	P22_3	D10	MTIOC8D / GTETRGSB	—	—	—	—	ENCIF11
B7	—	TRACEDATA6	P21_7	D6 / DREQ	MTIOC7C / GTIOC17A	DE0	MCLK 3	IRQ10	—	—
B8	—	TRACEDATA0	P21_1	D0	MTIOC6A / GTIOC14A / CMTW0_TIC0	SCK5 / IIC_SCL1 / SPI_SSL20	MCLK 0	—	—	ENCIF5
B9	—	MDV0	P20_1	—	—	ETHSW_TDMAOUT0 / ESC_LINKACT0	—	—	—	—
B10	—	—	—	—	—	—	—	—	AN105	—
B11	—	—	—	—	—	—	—	—	AN102	—
B12	—	—	—	—	—	—	—	—	AN100	—
B13	—	—	—	—	—	—	—	—	AN000	—
B14	—	—	—	—	—	—	—	—	AN002	—
B15	—	MDV4	P19_0	—	—	USB_VBUSEN	—	—	—	—
C1	—	TRACEDATA1	P01_7	A19	MTIOC1B / GTIOC9B	SCK1 / ETHSW_LPI1 / CANRX0 / SPI_RSPCK3	—	—	ADTRG0#	ENCIF1
C2	VCC1833_2	—	P01_3	WE3# / DQMUU / AH#	MTIOC4D / GTIOC3B	ETH2_TXD2	—	—	—	—
C3	VCC1833_2	—	P00_6	CS5#	MTIOC3B / GTIOC1A	ETH2_TXCLK	—	—	—	—
C4	VCC1833_2	—	P00_0	D26 / D15	—	SCK2 / ETH2_RXD3	—	—	—	—
C5	VCC1833_2	—	P24_2	D25 / D14 / RAS#	MTIOC0D / GTETRGD	TXD1 / SDA1 / MOSI1 / ETH2_RXD2	MDAT 5	—	—	ENCIF15
C6	—	TRACECLK	P22_2	D9	MTIOC8C / GTETRGSA	SPI_SSL12	—	IRQ4	—	ENCIF10
C7	—	TRACEDATA4	P21_5	D4	MTIOC7A / GTIOC16A / CMTW1_TOC1	CTS5# / SPI_MISO0	MCLK 2	IRQ6	ADTRG1#	ENCIF9
C8	—	TRACEDATA1	P21_2	D1	MTIOC6B / GTIOC14B / CMTW0_TIC1	RXD5 / SCL5 / MISO5 / IIC_SDA1 / SPI_MISO2	MDAT 0	—	—	ENCIF6
C9	—	—	—	—	—	—	—	—	AN107	—
C10	—	VREFH1	—	—	—	—	—	—	—	—
C11	—	VREFH0	—	—	—	—	—	—	—	—
C12	—	—	—	—	—	—	—	—	AN001	—
C13	—	—	—	—	—	—	—	—	AN003	—
C14	—	AVCC18_TSU	—	—	—	—	—	—	—	—
C15	—	TRACECLK	P18_6	—	MTIC5W	SCK4 / IIC_SCL2 / SPI_MISO2	—	IRQ11	ADTRG0#	ENCIF15
D1	—	MDW	P02_1	A17	—	ETHSW_PTPOUT1 / ESC_SYNC1 / ESC_SYNC0	—	—	—	—
D2	—	TRACEDATA0	P01_6	A20	MTIOC1A / GTIOC9A	CTS1# / GMAC_PTPTRG1 / ESC_LATCH1 / ESC_LATCH0 / CANTXDP1	—	—	—	ENCIF0
D3	VCC1833_2	—	P01_1	CKE	MTIOC3D / GTIOC1B	DE2 / GMAC_MDC / ETHSW_MDC / ESC_MDC	MDAT 1	—	—	—
D4	VCC1833_2	—	P00_7	RAS#	MTIOC4A / GTIOC2A	—	—	IRQ13	—	—
D5	VCC1833_2	—	P00_1	D27 / A13	MTIC5U	RXD2 / SCL2 / MISO2 / ETH2_RXDV	—	IRQ0	—	—
D6	VCC1833_2	—	P23_7	D22 / D11 / BS	MTIOC0A / GTETRGA	SCK1 / ETH2_RXD0	MCLK 4	—	—	ENCIF12

Table 1.19 List of pins and pin functions (225-pin FBGA) (3 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
D7	—	TRACEDATA5	P21_6	D5 / TEND	MTIOC7B / GTIOC16B	CTS0#	MDAT 2	IRQ9	—	—
D8	—	MDV1	P20_2	—	—	DE3 / ETHSW_TDMAOUT1 / ESC_LEDRUN / ESC_LEDSTER	—	—	—	—
D9	—	MDV2	P20_3	—	—	ETHSW_TDMAOUT2 / ESC_LEDERR	—	—	—	—
D10	—	VSS	—	—	—	—	—	—	—	—
D11	—	VSS	—	—	—	—	—	—	—	—
D12	—	VSS	—	—	—	—	—	—	—	—
D13	—	TRACECTL	P18_5	—	MTIC5V	RXD4 / SCL4 / MISO4 / SPI_MOSI2	—	—	—	ENCIF14
D14	—	—	P18_2	—	MTIOC4B / MTIOC4D / GTIOC2B / GTIOC3B	—	—	—	—	ENCIF11
D15	—	—	P18_1	—	MTIOC3D / GTIOC1B	SS3# / CTS3# / RTS3#	—	IRQ10	ADTRG1#	ENCIF10
E1	—	—	P02_3	A15 / WE3# / DQMUU / AH#	MTIOC2B / POE11# / GTIOC10B	SS1# / CTS1# / RTS1# / ETHSW_TDMAOUT1 / CANRX1 / SPI_SSL30	—	IRQ15	—	ENCIF4
E2	—	TRST#	—	—	—	—	—	—	—	—
E3	—	TRACEDATA2	P02_0	A18	GTADSML0	RXD1 / SCL1 / MISO1 / ETHSW_LPI2 / USB_OTGID / CANTX1 / SPI_MISO3	—	IRQ4	—	ENCIF2
E4	VCC1833_2	—	P01_4	WE1# / DQMLU	POE0#	ETH2_TXD1	—	IRQ3	—	—
E5	—	VCC1833_2	—	—	—	—	—	—	—	—
E6	—	VCC33	—	—	—	—	—	—	—	—
E7	—	TRACEDATA3	P21_4	D3	MTIOC6D / GTIOC15B	SS5# / CTS5# / RTS5# / SPI_SSL02	MDAT 1	—	—	ENCIF8
E8	—	VCC33	—	—	—	—	—	—	—	—
E9	—	VCC18_ADC1	—	—	—	—	—	—	—	—
E10	—	VSS	—	—	—	—	—	—	—	—
E11	—	VCC18_ADC0	—	—	—	—	—	—	—	—
E12	—	—	P18_4	—	MTIC5U	TXD4 / SDA4 / MOSI4 / SPI_RSPCK2	—	IRQ1	—	ENCIF13
E13	—	—	P18_3	—	MTIOC4D / MTIOC4B / GTIOC3B / GTIOC2B / CMTW1_TIC1	CANRXDP1	—	IRQ0	—	ENCIF12
E14	—	—	P18_0	—	MTIOC4C / MTIOC4A / GTIOC3A / GTIOC2A	TXD3 / SDA3 / MOSI3	—	—	—	—
E15	—	—	P17_7	DACK	MTIOC4A / MTIOC4C / GTIOC2A / GTIOC3A	RXD3 / SCL3 / MISO3	—	—	—	ENCIF9
F1	—	TCK	P02_7	—	—	TXD5 / SDA5 / MOSI5	—	—	—	ENCIF7
F2	—	TDI	P02_5	WE1# / DQMLU	—	SCK5 / ETHSW_TDMAOUT3 / SPI_SSL31	—	—	—	ENCIF5
F3	—	—	P02_2	A16	MTIOC2A / POE10# / GTIOC10A / RTCAT1HZ	TXD1 / SDA1 / MOSI1 / ETHSW_TDMAOUT0 / CANTX0 / SPI_MOSI3	—	IRQ14	—	ENCIF3
F4	—	TDO	P02_4	WE0# / DQMLL	—	DE1 / SPI_SSL33	—	—	—	—
F5	—	TMS	P02_6	—	—	RXD5 / SCL5 / MISO5	—	—	—	ENCIF6
F6	—	VDD	—	—	—	—	—	—	—	—
F7	—	VSS	—	—	—	—	—	—	—	—
F8	—	VDD	—	—	—	—	—	—	—	—
F9	—	VDD	—	—	—	—	—	—	—	—
F10	—	VDD	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (225-pin FBGA) (4 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
F11	—	VCC33	—	—	—	—	—	—	—	—
F12	—	MDD	P17_0	—	—	SS0# / CTS0# / RTS0# / ESC_IRQ	—	—	—	—
F13	—	TRACECLK	P17_4	—	MTIOC3C / GTETRGB / GTIOC0A	CTS3# / SPI_SSL32	—	—	—	ENCIF6
F14	—	TRACECTL	P17_3	DREQ	POE0# / GTETRGA	SPI_SSL31	—	—	ADTRG1#	ENCIF5
F15	—	RSTOUT#	P17_5	TEND	MTIOC3A / GTETRGC / GTIOC0B	USB_OVRCUR	—	—	—	ENCIF7
G1	—	—	P03_5	A12	MTIOC3A / GTIOC4A	RXD2 / SCL2 / MISO2 / ETH2_CRS	MCLK 2	IRQ5	—	—
G2	—	BSCANP	—	—	—	—	—	—	—	—
G3	—	TRACEDATA3	P03_0	A14 / CS5#	GTADSML1	SCK2 / CANTXDP1 / SPI_SSL32	—	IRQ14	—	ENCIF8
G4	—	TRACEDATA4	P03_6	A11	MTIOC3B / GTIOC4B	TXD2 / SDA2 / MOSI2 / ETH2_COL / SPI_SSL13	MDAT 2	IRQ8	—	—
G5	—	TRACEDATA5	P03_7	A10	MTIOC3C / GTIOC5A	SCK3 / ETH2_TXER	—	IRQ9	—	—
G6	—	VDD	—	—	—	—	—	—	—	—
G7	—	VSS	—	—	—	—	—	—	—	—
G8	—	VSS	—	—	—	—	—	—	—	—
G9	—	VSS	—	—	—	—	—	—	—	—
G10	—	VDD	—	—	—	—	—	—	—	—
G11	—	—	P16_6	—	MTIC5V	RXD0 / SCL0 / MISO0	—	IRQ8	—	—
G12	VCC1833_3	—	P16_3	—	GTADSMP1	SCK0 / ETH1_TXER / SPI_SSL30 / XSPI0_RSTO0#	—	IRQ7	—	ENCIF4
G13	VCC1833_3	—	P16_0	—	—	TXD0 / SDA0 / MOSI0 / ETH0_TXER / SPI_MOSI3 / XSPI0_CS1#	MCLK 3	—	—	ENCIF0
G14	—	—	P16_7	—	MTIC5W	SCK0	—	—	—	—
G15	—	—	P17_6	—	MTIOC3B / GTIOC1A	SCK3	—	—	—	ENCIF8
H1	—	TRACEDATA6	P04_0	A9	MTIOC3D / GTIOC5B	RXD3 / SCL3 / MISO3	—	—	—	—
H2	—	—	P04_1	CKIO	—	TXD3 / SDA3 / MOSI3 / IIC_SDA2 / SPI_MOSI0	—	—	—	—
H3	—	MD0	P04_5	A7	—	DE3	—	—	—	—
H4	—	TRACEDATA7	P04_4	A8	POE10# / GTADSMP0	CTS3# / SPI_RSPCK1	—	IRQ10	—	ENCIF10
H5	—	MD1	P04_6	A6 / DACK	RTCAT1HZ	ETH1_TXER	—	—	—	—
H6	—	VDD	—	—	—	—	—	—	—	—
H7	—	VSS	—	—	—	—	—	—	—	—
H8	—	VSS	—	—	—	—	—	—	—	—
H9	—	VSS	—	—	—	—	—	—	—	—
H10	—	VDD	—	—	—	—	—	—	—	—
H11	VCC1833_3	—	P16_1	—	CMTW0_TOC1	RXD0 / SCL0 / MISO0 / SPI_MISO3 / XSPI0_RESET0#	MDAT 3	—	ADTRG0#	ENCIF2
H12	VCC1833_3	—	P15_6	—	—	SPI_SSL12 / XSPI0_IO7	MDAT 2	—	—	—
H13	VCC1833_3	—	P15_4	—	MTIOC8D	XSPI0_IO5	MDAT 1	—	—	—
H14	VCC1833_3	—	P16_2	—	—	CTS0# / USB_EXICEN / SPI_RSPCK3 / XSPI0_RESET1#	—	NMI	—	ENCIF3
H15	—	—	P16_5	—	MTIC5U	TXD0 / SDA0 / MOSI0	—	—	—	—
J1	—	MD2	P04_7	A5	—	ETH0_TXER / SPI_SSL21	—	—	—	—
J2	—	—	P05_1	A3	MTIOC4B / GTIOC6B / CMTW0_TIC1	CTS5# / ETH1_COL / USB_EXICEN / CANRXDP0	MDAT 3	IRQ13	—	ENCIF12

Table 1.19 List of pins and pin functions (225-pin FBGA) (5 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
J3	—	—	P05_3	A1	MTIOC4D / POE11# / GTETRGSB / GTIOC7B / CMTW0_TIC0	SCK4 / IIC_SDA1 / ETH0_COL / USB_EXICEN / CANTX0	—	IRQ15	—	ENCIF14
J4	—	—	P05_2	A2 / DREQ	MTIOC4C / GTETRGSA / GTIOC7A / CMTW0_TOC0	DE5 / IIC_SCL1 / ETH0_CRS / USB_VBUSEN / CANRX0	—	IRQ14	—	ENCIF13
J5	—	—	P05_0	A4	MTIOC4A / GTIOC6A / CMTW0_TOC0	SS5# / CTS5# / RTS5# / ETH1_CRS / USB_VBUSEN / CANTXDP0	MCLK 3	IRQ12	—	ENCIF11
J6	—	VDD	—	—	—	—	—	—	—	—
J7	—	VSS	—	—	—	—	—	—	—	—
J8	—	VSS	—	—	—	—	—	—	—	—
J9	—	VSS	—	—	—	—	—	—	—	—
J10	—	VDD	—	—	—	—	—	—	—	—
J11	—	VCC1833_3	—	—	—	—	—	—	—	—
J12	VCC1833_3	—	P14_5	CS3#	POE8#	XSPI0_CKN	—	—	—	—
J13	VCC1833_3	—	P14_4	BS	MTIOC0B	ESC_IRQ / XSPI0_DS	—	—	—	—
J14	VCC1833_3	—	P15_5	—	—	XSPI0_IO6	MCLK 2	—	—	—
J15	VCC1833_3	—	P15_7	TEND	—	CTS5# / SPI_SSL13 / XSPI0_CS0#	—	—	—	ENCIF1
K1	VCC1833_1	—	P05_4	A0 / DACK	GTIOC14A	RXD4 / SCL4 / MISO4 / ETHSW_LPI0 / USB_OVRCUR / CANTXDP0 / SPI_SSL00	—	IRQ12	—	ENCIF15
K2	VCC1833_1	—	P05_5	D16	GTIOC14B / CMTW0_TOC1	ETHSW_PHYLINK1 / ESC_PHYLINK1 / SPI_RSPCK2	—	—	—	—
K3	VCC1833_1	—	P05_6	D17	GTIOC15A / CMTW1_TIC0	ETH1_RXER / SPI_SSL22	—	IRQ12	—	—
K4	VCC1833_1	—	P06_3	D23	GTIOC17B / CMTW1_TIC1	DE4 / ETH1_TXD0 / CANTXDP1 / SPI_MISO1	—	—	—	—
K5	—	VCC1833_1	—	—	—	—	—	—	—	—
K6	—	VDD	—	—	—	—	—	—	—	—
K7	—	VDD	—	—	—	—	—	—	—	—
K8	—	VDD	—	—	—	—	—	—	—	—
K9	—	VSS	—	—	—	—	—	—	—	—
K10	—	VDD	—	—	—	—	—	—	—	—
K11	VCC1833_3	—	P15_3	—	MTIOC8C	XSPI0_IO4	MCLK 1	—	—	—
K12	VCC1833_3	—	P14_2	—	MTIOC8B / GTIOC8B	ETH0_CRS / XSPI0_ECS0#	—	IRQ6	—	ENCIF12
K13	VCC1833_3	—	P14_6	A21	—	XSPI0_CKP	—	—	—	—
K14	VCC1833_3	—	P15_1	A24	MTIOC0C	TXD5 / SDA5 / MOSI5 / SPI_SSL10 / XSPI0_IO2	—	—	—	—
K15	VCC1833_3	—	P15_2	A25	MTIOC0D	SS5# / CTS5# / RTS5# / SPI_SSL11 / XSPI0_IO3	—	—	—	—
L1	—	VSS	—	—	—	—	—	—	—	—
L2	VCC1833_1	—	P06_0	D19	GTIOC16A / CMTW1_TOC0	SS4# / CTS4# / RTS4# / ETH1_TXD3 / CANRX1 / SPI_SSL23	—	—	—	—
L3	VCC1833_1	—	P06_1	D22	GTIOC16B	CTS4# / ETH1_REFCLK / RMII1_REFCLK / CANTX1 / SPI_SSL22	—	—	—	—
L4	VCC1833_1	—	P06_6	D21	GTIOC12A	ETH1_RXD0 / SPI_SSL10	—	—	—	—
L5	—	VCC33	—	—	—	—	—	—	—	—
L6	—	VCC1833_0	—	—	—	—	—	—	—	—
L7	VCC1833_0	—	P09_7	—	—	ETH0_TXCLK	—	—	—	—

Table 1.19 List of pins and pin functions (225-pin FBGA) (6 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
L8	VCC1833_0	—	P10_2	—	—	ETH0_RXD1	—	—	—	—
L9	VCC1833_0	—	P10_3	—	RTCAT1HZ	ETH0_RXD2	—	—	—	—
L10	VCC1833_4	TRACEDATA6	P13_2	D9	MTIOC0A / POE8# / GTIOC10A	SS1# / CTS1# / RTS1# / IIC_SCL0 / ETHSW_PTPOUT2 / ESC_I2CCLK / SPI_MISO0	MCLK 4	IRQ5	—	ENCIF8
L11	VCC1833_3	—	P15_0	A23	—	RXD5 / SCL5 / MISO5 / SPI_MOSI1 / XSPI0_IO1	—	—	—	—
L12	VCC1833_4	—	P13_4	—	MTIOC0D / GTIOC8B	ESC_RESETOUT#	—	—	—	ENCIF10
L13	VCC1833_3	—	P14_0	—	MTCLKD	ETHSW_PTPOUT1 / ESC_SYNC1 / ESC_SYNC0 / XSPI0_INT0#	—	—	—	—
L14	VCC1833_3	—	P14_1	—	MTIOC8A / GTIOC8A	ETH1_COL / XSPI0_INT1#	—	—	—	ENCIF11
L15	—	VSS	—	—	—	—	—	—	—	—
M1	VCC1833_1	—	P05_7	D18	GTIOC15B / CMTW1_TOC1	TXD4 / SDA4 / MOSI4 / ETH1_TXD2 / SPI_SSL23	—	—	—	—
M2	VCC1833_1	—	P06_2	D20	GTIOC17A	ETH1_TXD1 / CANRXDP1	—	—	—	—
M3	VCC1833_1	—	P06_7	D26	GTIOC12B	ETH1_RXD1 / SPI_SSL11	—	—	—	—
M4	VCC1833_1	—	P07_3	D30	—	ETH1_RXCLK	—	—	—	—
M5	VCC1833_0	—	P08_6	—	MTIOC6C	ETH0_RXCLK	—	—	—	—
M6	VCC1833_0	—	P09_4	—	—	ETH0_TXD2	—	—	—	—
M7	VCC1833_0	—	P09_6	—	—	ETH0_TXD0	—	—	—	—
M8	VCC1833_0	—	P10_1	—	—	ETH0_RXD0	—	—	—	—
M9	VCC1833_0	—	P10_4	WE2# / DQMUL	—	ETHSW_PHYLINK0 / ESC_PHYLINK0	—	IRQ11	—	—
M10	—	VCC1833_4	—	—	—	—	—	—	—	—
M11	VCC1833_3	—	P13_7	—	MTCLKC	GMAC_PTPTRG1 / ESC_LATCH1 / ESC_LATCH0 / XSPI0_ECS1#	—	—	—	—
M12	VCC1833_3	—	P13_5	—	MTCLKA	GMAC_PTPTRG0 / ESC_LATCH0 / ESC_LATCH1 / SPI_RSPCK1 / XSPI0_WP1#	—	—	—	—
M13	VCC1833_3	—	P13_6	—	MTCLKB	ETHSW_PTPOUT0 / ESC_SYNC0 / ESC_SYNC1 / XSPI0_WP0#	—	—	—	—
M14	VCC1833_3	—	P14_3	—	MTIOC0A	ETH0_COL / XSPI0_RSTO1#	—	—	—	ENCIF13
M15	VCC1833_3	—	P14_7	A22	—	SCK5 / SPI_MISO1 / XSPI0_IO0	—	—	—	—
N1	VCC1833_1	—	P06_4	D24	GTIOC11A	ETH1_TXCLK / SPI_MOSI1	—	—	—	—
N2	VCC1833_1	—	P06_5	D25	GTIOC11B	ETH1_TXEN	—	—	—	—
N3	VCC1833_1	—	P07_1	D28	GTIOC13B	ETH1_RXD3	—	—	—	—
N4	VCC1833_0	—	P08_4	D31	MTIOC6A	ETH0_RXD3	—	—	—	—
N5	VCC1833_0	—	P08_7	D29	MTIOC6D	GMAC_MDC / ETHSW_MDC / ESC_MDC	—	—	—	—
N6	VCC1833_0	—	P09_2	D31	MTIOC7C	ETH0_RXER	—	IRQ0	—	—
N7	VCC1833_0	—	P09_5	—	—	ETH0_TXD1	—	—	—	—
N8	VCC1833_0	—	P10_0	—	—	ETH0_TXEN	—	—	—	—
N9	—	VCC18_PLL1	—	—	—	—	—	—	—	—
N10	—	VSS	—	—	—	—	—	—	—	—
N11	VCC1833_4	TRACEDATA0	P12_4	D15	MTIOC8B / GTIOC8B	ETH1_CRS / SPI_SSL01	—	—	—	ENCIF7
N12	VCC1833_4	TRACEDATA7	P13_3	D8	MTIOC0C / MTIOC0B / GTIOC10B / CMTW1_TOC0	CTS1# / IIC_SDA0 / ETHSW_PTPOUT3 / ESC_I2CDATA / SPI_RSPCK0	MDAT 4	—	—	ENCIF9
N13	—	VSS_USB	—	—	—	—	—	—	—	—
N14	—	VSS	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (225-pin FBGA) (7 of 7)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, USB, CANFD, SPI, xSPI)	DSMIF	Interrupt	ADC12	Encoder I/F
N15	—	VSS_USB	—	—	—	—	—	—	—	—
P1	VCC1833_1	—	P07_0	D27	GTIOC13A	ETH1_RXD2	—	—	—	—
P2	VCC1833_1	—	P07_2	D29	—	ETH1_RXDV	—	—	—	—
P3	VCC1833_0	—	P08_5	—	MTIOC6B	ETH0_RXDV	—	—	—	—
P4	VCC1833_0	—	P09_0	D30	MTIOC7A	GMAC_MDIO / ETHSW_MDIO / ESC_MDIO	—	—	—	—
P5	—	MDX	—	—	—	—	—	—	—	—
P6	—	RES#	—	—	—	—	—	—	—	—
P7	—	VDD	—	—	—	—	—	—	—	—
P8	—	VSS	—	—	—	—	—	—	—	—
P9	—	VCC18_PLL0	—	—	—	—	—	—	—	—
P10	—	AVCC18_USB	—	—	—	—	—	—	—	—
P11	—	VCC18_USB	—	—	—	—	—	—	—	—
P12	—	VSS_USB	—	—	—	—	—	—	—	—
P13	—	USB_DM	—	—	—	—	—	—	—	—
P14	—	VSS_USB	—	—	—	—	—	—	—	—
P15	—	USB_RREF	—	—	—	—	—	—	—	—
R1	—	VSS	—	—	—	—	—	—	—	—
R2	—	—	P07_4	—	—	USB_VBUSIN	—	IRQ1	ADTRG0#	—
R3	VCC1833_0	—	P09_1	—	MTIOC7B	ETH0_REFCLK / RMII0_REFCLK	—	—	—	—
R4	VCC1833_0	—	P09_3	—	MTIOC7D	ETH0_TXD3	—	—	—	—
R5	—	VSS	—	—	—	—	—	—	—	—
R6	—	EXTCLKIN	—	—	—	—	—	—	—	—
R7	—	EXTAL	—	—	—	—	—	—	—	—
R8	—	XTAL	—	—	—	—	—	—	—	—
R9	—	VSS	—	—	—	—	—	—	—	—
R10	—	AVCC18_USB	—	—	—	—	—	—	—	—
R11	—	VCC33_USB	—	—	—	—	—	—	—	—
R12	—	VSS_USB	—	—	—	—	—	—	—	—
R13	—	USB_DP	—	—	—	—	—	—	—	—
R14	—	VSS_USB	—	—	—	—	—	—	—	—
R15	—	VSS	—	—	—	—	—	—	—	—

2. Electrical Characteristics

Electrical characteristics of this LSI is defined with the following conditions unless otherwise described.

Conditions:

VDD = 1.05 to 1.15 V

VCC18 = VCC1833_n (1.8-V mode) = VCC18_PLL0 = VCC18_PLL1 = VCC18_USB = AVCC18_USB = VCC18_ADC0 = VCC18_ADC1 = AVCC18_TSU = VREFH0 = VREFH1= 1.70 to 1.95 V

VCC33 = VCC1833_n (3.3-V mode) = VCC33_USB = 3.135 to 3.465 V

VSS = VSS_USB = 0 V

Tj = −40 to 125ºC

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage (3.3-V mode)	VCC33, VCC1833_0, VCC1833_1, VCC1833_2, VCC1833_3, VCC1833_4	−0.3 to +3.8	V
Power supply voltage (1.8-V mode)	(VCC18) VCC1833_0 VCC1833_1, VCC1833_2, VCC1833_3, VCC1833_4	−0.3 to +2.5	V
Power supply voltage	VDD	−0.3 to +1.5	V
Input voltage	Vin (3.3-V logic)	−0.3 to VCC33 + 0.3	V
Input voltage	Vin (1.8-V logic)	−0.3 to VCC18 + 0.3	V
Analog power supply voltage	VCC18_PLL0, VCC18_PLL1, VCC18_USB, AVCC18_USB, VCC18_ADC0, VCC18_ADC1, AVCC18_TSU*1	−0.3 to smaller value of VCC18*2 + 0.3 or 2.5	V
	VCC33_USB	−0.3 to smaller value of VCC33 + 0.3 or 3.8	V
Voltage difference between power supply pins	VCC33-VCC18	-2.5 to + 2.1	V
Analog input voltage	VAN	−0.3 to smaller value of VCC18_ADC0/1 + 0.3 or 2.5	V
Reference voltage	VREFH0, VREFH1	−0.3 to smaller value of VCC18_ADC0/1 + 0.3 or 2.5	V
Crystal oscillator pins input voltage	XTAL, EXTAL	−0.3 to +1.5	V
Operating temperature (Junction temperature)	T_j	−40 to +125	ºC
Storage temperature	T_{stg}	−55 to +125	ºC

Note 1. Connect Analog power supply pins to VCC18 when Analog block(s) are not used. Do not leave these pins open.
Note 2. For convention, "VCC18" virtually represents any 1.8-V power supplies of the chip such as VCC1833_n in 1.8-V mode.

Caution: Permanent damage to the LSI might result if absolute maximum ratings are exceeded.

2.2 Power Supply

Table 2.2 Power supply

Parameter	Symbol	Value	Min.	Typ.	Max.	Unit
Power supply voltages	VCC33		3.135	—	3.465	V
	VDD		1.05	1.1	1.15	V
	VSS		—	0	—	V
Power supply voltages supporting multi voltage mode	VCC1833_0, VCC1833_1, VCC1833_2, VCC1833_3, VCC1833_4	3.3-V mode	3.135	3.3	3.465	V
		1.8-V mode (VCC18)	1.70	1.8	1.95	V
Analog power supply voltages	VCC18_PLL0		—	VCC18	—	V
	VCC18_PLL1		—	VCC18	—	V
	VCC33_USB		—	VCC33	—	V
	VCC18_USB		—	VCC18	—	V
	AVCC18_USB		—	VCC18	—	V
	VCC18_ADC0		—	VCC18	—	V
	VCC18_ADC1		—	VCC18	—	V
	AVCC18_TSU		—	VCC18	—	V
	VREFH0		VSS	—	VCC18_ADC0	V
	VREFH1		VSS	—	VCC18_ADC1	V
	VSS_USB		—	0	—	V

Note: The condition of A/D conversion characteristics is VREFHn = VCC18_ADCn (n = 0, 1). And power-up/down sequence should follow VCC18_ADCn.

2.3 Power On/Off Sequence

Power on/off sequence and timing are shown in the figure and table below.

For power-up, 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC) must be supplied first, then 3.3-V power (i.e. VCC33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e. RES#) must be held to Low level during the power-up.

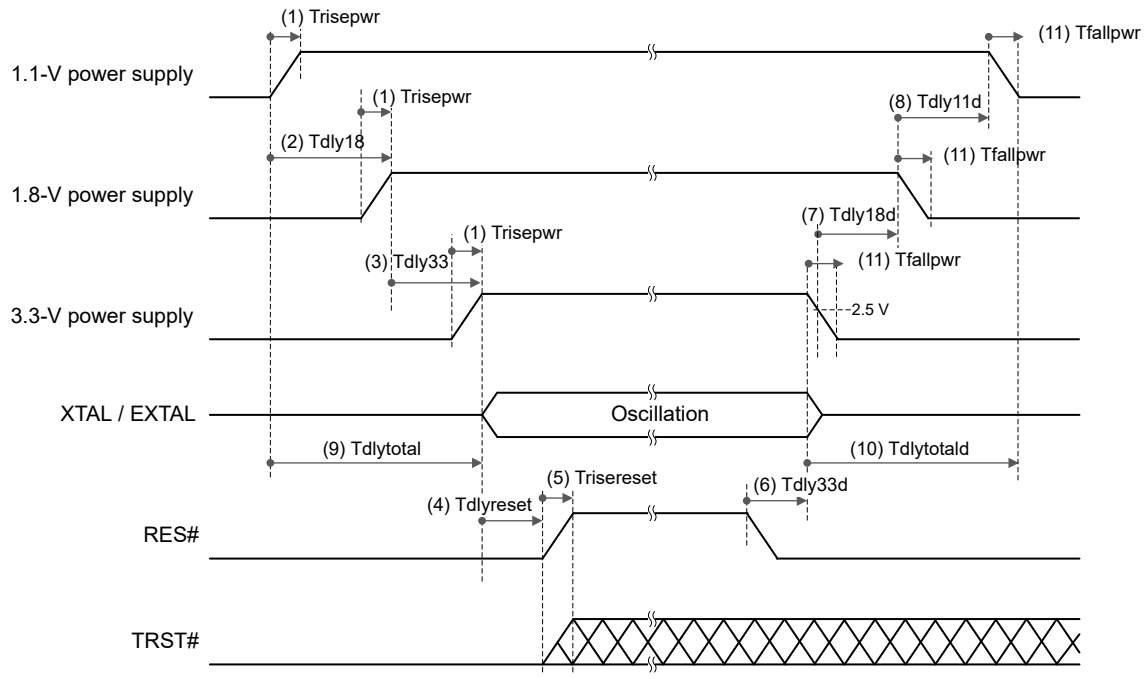
For Power-down, 3.3-V power (i.e. VCC33) must go down first and then 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC). The power-down sequence must be completed within 100 ms.

Rise and fall time of each power supply for the power-up and the power-down must be larger than 10 µs.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

Stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when reset signal (i.e. RES#) is driven high.



Note:
- When 1.8-V is supplied to VCC1833_n, should follow the 1.8-V power supply sequence. When 3.3-V is supplied to VCC1833_n, should follow the 3.3-V power supply sequence.
- All 3.3-V power supplies must start up the same time.

Figure 2.1 Power on/off sequence

Table 2.3 Power on/off sequence timing

No.	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepwr	Rising time of the power supply voltage	10 µs	—	30 ms
(2)	Tdly18	Delay time from start of rising of the 1.1-V power supply voltage to completion of rising of the 1.8-V power supply voltage	0	—	100 ms
(3)	Tdly33	Delay time from completion of rising of the 1.8-V power supply voltage to completion of rising of the 3.3-V power supply voltage	0	—	100 ms
(4)	Tdlyreset	Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of RES# when XTAL/EXTAL is used.	10 ms	—	—
		Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of RES# when EXTCLKIN is used.	1 ms	—	—
(5)	Trisereset	Rising time of RES#	—	—	150 µs
(6)	Tdly33d	Delay time from start of falling of RES# to start of falling of the 3.3-V power supply voltage	10 µs	—	—
(7)	Tdly18d	Delay time from start of falling time of the 3.3-V power supply voltage to start of falling of the 1.8-V power supply voltage	0	—	100 ms
(8)	Tdly11d	Delay time from start of falling of the 1.8-V power supply voltage to start of falling of the 1.1-V power supply voltage	0	—	100 ms
(9)	Tdlytotal	Startup time of all power supply voltage	—	—	100 ms
(10)	Tdlytotald	Shut down time of all power supply voltage	—	—	100 ms
(11)	Tfallpwr	Falling time of the power supply voltage	10 µs	—	30 ms

2.4 DC Characteristics

Table 2.4 DC Characteristics (3.3-V mode)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH33}	3.3-V mode, Schmitt Trigger Control Disabled, Except P07_4 pin	2.0	—	VCC33 + 0.3	V
Input Low-level voltage	V_{IL33}		−0.3	—	0.8	V
Positive trigger voltage	V_{T33+}	3.3-V mode, Schmitt Trigger Control Enabled, Except P07_4 pin	0.9	—	2.1	V
Negative trigger voltage	V_{T33-}		0.7	—	1.9	V
Hysteresis voltage	ΔV_{T33}		0.2	—	—	V
Input High-level voltage 2	V_{IH33_2}	3.3-V mode, Schmitt Trigger Control Disabled, P07_4 pin ONLY	VCC33 × 0.7	—	VCC33 + 0.3	V
Input Low-level voltage 2	V_{IL33_2}		-0.3	—	VCC33 × 0.3	V
Positive trigger voltage 2	V_{T33+_2}	3.3-V mode, Schmitt Trigger Control Enabled, P07_4 pin ONLY	—	—	VCC33 × 0.72	V
Negative trigger voltage 2	V_{T33-_2}		VCC33 × 0.3	—	—	V
Hysteresis voltage 2	ΔV_{T33_2}		VCC33 × 0.1	—	—	V
Output High-level voltage	V_{OH33}	Low, IOH = −2 mA	VCC33 − 0.4	—	—	V
	V_{OH33}	Middle, IOH = −4 mA	VCC33 − 0.4	—	—	V
	V_{OH33}	High, IOH = −8 mA	VCC33 − 0.4	—	—	V
	V_{OH33}	Ultra High, IOH = −12 mA	VCC33 − 0.4	—	—	V
Output Low-level voltage	V_{OL33}	Low, IOL = 2 mA	—	—	0.4	V
	V_{OL33}	Middle, IOL = 4 mA	—	—	0.4	V
	V_{OL33}	High, IOL = 8 mA	—	—	0.4	V
	V_{OL33}	Ultra High, IOL = 12 mA	—	—	0.4	V
Input leakage current	|Iin|	Vin = 0 V, Vin = VCC33	—	—	10	µA
Three-State leakage current (off state)	$\|I_{TSI}\|$	Vin = 0 V, Vin = VCC33	—	—	10	µA
Input Pull-up resistors resistance	Rpu	Vin = 0 V	15	—	300	kΩ
Input Pull-up resistors current	Ipu	Vin = 0 V	-220	—	-11	µA
Input Pull-down resistors resistance	Rpd	Vin = VCC33	15	—	300	kΩ
Input Pull-down resistors current	Ipd	Vin = VCC33	11	—	220	µA
Input Capacitance BGA package	Cin	All input/output and input pins	—	—	10	pF

Table 2.5 DC Characteristics (1.8-V mode) (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH18}	1.8-V mode, Schmitt Trigger Control Disabled	VCC18 × 0.65	—	VCC18 + 0.3	V
Input Low-level voltage	V_{IL18}		−0.3	—	VCC18 × 0.35	V
Positive trigger voltage	V_{T18+}	1.8-V mode, Schmitt Trigger Control Enabled	VCC18 × 0.4	—	VCC18 × 0.7	V
Negative trigger voltage	V_{T18-}		VCC18 × 0.3	—	VCC18 × 0.6	V
Hysteresis voltage	ΔV_{T18}		VCC18 × 0.1	—	—	V
Output High-level voltage	V_{OH18}	Low, IOH = −2 mA	VCC18 − 0.45	—	—	V
	V_{OH18}	Middle, IOH = −4 mA	VCC18 − 0.45	—	—	V
	V_{OH18}	High, IOH = −8 mA	VCC18 − 0.45	—	—	V
	V_{OH18}	Ultra High, IOH = −12 mA	VCC18 − 0.45	—	—	V

Table 2.5 DC Characteristics (1.8-V mode) (2 of 2)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Low-level voltage		V_{OL18}	Low, IOL = 2 mA	—	—	0.45	V
		V_{OL18}	Middle, IOL = 4 mA	—	—	0.45	V
		V_{OL18}	High, IOL = 8 mA	—	—	0.45	V
		V_{OL18}	Ultra High, IOL = 12 mA	—	—	0.45	V
Input leakage current		|Iin|	Vin = 0 V, Vin = VCC18	—	—	10	µA
Three-State leakage current (off state)		$\|I_{TSI}\|$	Vin = 0 V, Vin = VCC18	—	—	10	µA
Input Pull-up resistors resistance		Rpu	Vin = 0 V	15	—	300	kΩ
Input Pull-up resistors current		Ipu	Vin = 0 V	-120	—	-6	µA
Input Pull-down resistors resistance		Rpd	Vin = VCC18	15	—	300	kΩ
Input Pull-down resistors current		Ipd	Vin = VCC18	6	—	120	µA
Input Capacitance	BGA package	Cin	All input/output and input pins	—	—	10	pF

Table 2.6 USB2.0 USB_RREF Pin

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference resistor*1	R_{REF}	—		1.8 (±1%)		kΩ

Note 1. The reference resistor connected to the USB_RREF pin is for external connection to this LSI.

Table 2.7 USB2.0 Pull-Up/Pull-Down Resistors

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
USB_DP pull-up resistor (when the function controller is selected)	R_{PU}	Idle	0.900	—	1.575	kΩ
		Transmission/reception	1.425	—	3.090	kΩ
USB_DP/USB_DM pull-down resistors (when the host controller is selected)	R_{PD}	—	14.25	—	24.80	kΩ

Table 2.8 USB2.0 Host/Function-Related Pins (Low/Full Speed)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high level voltage	V_{FSIH}	—	2.0	—	—	V
Input low level voltage	V_{FSIL}	—	—	—	0.8	V
Differential input sensitivity	V_{FSDI}	|(USB_DP) − (USB_DM)|	0.2	—	—	V
Differential common mode range	V_{FSCM}	—	0.8	—	2.5	V
Output low level voltage	V_{FSOL}	IFSOL = 2 mA	0.0	—	0.3	V
Output high level voltage	V_{FSOH}	IFSOH = −200 µA	2.8	—	3.6	V
Output signal crossover voltage	V_{FSCRS}	—	1.3	—	2.0	V

Table 2.9 USB2.0 Host/Function-Related Pins (High Speed) (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	—	100	—	150	mV
Disconnection detection threshold voltage (differential voltage)	V_{HSDSC}	—	525	—	625	mV
Common mode voltage range	V_{HSCM}	—	−50	—	500	mV
Idle state	V_{HSOI}	—	−10.0	—	10.0	mV
Output high level voltage	V_{HSOH}	—	360	—	440	mV

Table 2.9 USB2.0 Host/Function-Related Pins (High Speed) (2 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output low level voltage	V_{HSOL}	—	−10.0	—	10.0	mV
Chirp J output voltage (differential)	V_{CHIRPJ}	—	700	—	1100	mV
Chirp K output voltage (differential)	V_{CHIRPK}	—	−900	—	−500	mV

Table 2.10 Supply Current

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Normal operation	I_{vdd}	ICLK = 200 MHz, CPU0CLK = 800 MHz, CPU1CLK = 800 MHz, Tj ≤ 110°C	—	—	660	mA
	I_{VCC33}	*1	—	30	—	mA
	$I_{VCC1833\_0}$	*1	—	9	—	mA
	$I_{VCC1833\_1}$	*1	—	9	—	mA
	$I_{VCC1833\_2}$	*1	—	9	—	mA
	$I_{VCC1833\_3}$	*1	—	9	—	mA
	$I_{VCC1833\_4}$	*1	—	9	—	mA
	I_{VCC18_PLL0}	—	—	—	6	mA
	I_{VCC18_PLL1}	—	—	—	6	mA
	I_{VCC18_USB}	—	—	—	39	mA
	I_{VCC18_ADC0}	—	—	—	3	mA
	I_{VCC18_ADC1}	—	—	—	3	mA
	I_{VCC18_TSU}		—	—	2	mA
	I_{VCC33_USB}	—	—	—	6	mA
Low power consumption mode*2	I_{vdd}	All modules inactive	—	15	—	mA
	I_{VCC33}	—	—	6	—	mA
	$I_{VCC1833\_0}$	—	—	2	—	mA
	$I_{VCC1833\_1}$	—	—	2	—	mA
	$I_{VCC1833\_2}$	—	—	2	—	mA
	$I_{VCC1833\_3}$	—	—	2	—	mA
	$I_{VCC1833\_4}$	—	—	2	—	mA
	I_{VCC18_PLL0}	—	—	3.5	—	mA
	I_{VCC18_PLL1}	—	—	0.1	—	mA
	I_{VCC18_USB}	—	—	0.5	—	mA
	I_{VCC18_ADC0}	—	—	0.2	—	mA
	I_{VCC18_ADC1}	—	—	0.2	—	mA
	I_{VCC18_TSU}	—	—	0.1	—	mA
	I_{VCC33_USB}	—	—	0.3	—	mA

Note: These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.

Note 1. IO supply current (I_{VCC33}, $I_{VCC1833\_n\ (n = 0\ to\ 4)}$) should be 80 mA or less. (ΣIOH in Table 2.11)

Note 2. All applicable modules are stopped or standby mode with the lowest clock frequency setting, no pull-up/down or operation for all I/O ports, and room temperature.

Table 2.11 Permissible Output Currents

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Permissible output low current (max. value per pin)	IOL	All output pins	—	—	12	mA
Permissible output low current (total)	ΣIOL	Sum of all output pins	—	—	80	mA
Permissible output high current (max. value per pin)	IOH	All output pins	—	—	-12	mA
Permissible output high current (total)	ΣIOH	Sum of all output pins	—	—	-80	mA

Note: All output current values shall be within the values in this table to ensure the reliability of this LSI.

Table 2.12 Thermal Resistance value (Reference)

Item	Symbol	Package	Max.	Unit
Thermal Resistance	Θja	320 pin FBGA 17 × 17 mm, 0.8-mm pitch	25.0	°C/W
		225 pin FBGA 13 × 13 mm, 0.8-mm pitch	25.3	°C/W
	Ψjt	320 pin FBGA 17 × 17 mm, 0.8-mm pitch	0.30	°C/W
		225 pin FBGA 13 × 13 mm, 0.8-mm pitch	0.31	°C/W

Note: Package thermal resistance values above are based on EIA/JESD51-9 (2s2p) condition and reference only.

2.5 AC Characteristics

Table 2.13 Operating frequency

Parameter		Symbol	Min.	Max.	Unit
Operating frequency	CPU clock (CPUnCLK, n = 0, 1)	f	150 200	600 800	MHz
	System clock (ICLK)		150	200	
	Peripheral module clock H (PCLKH)		150	200	
	Peripheral module clock M (PCLKM)		75	100	
	Peripheral module clock L (PCLKL)		37.5	50	
	Peripheral module clock for ADC (PCLKADC)		18.75	25	
	Peripheral module clock for SCIn (PCLKSCIn, n = 0 to 5)		75	100	
	Peripheral module clock for SPIn (PCLKSPIn, n = 0 to 3)		75	100	
	External bus clock output (CKIO)		18.75	100	
	Ethernet PHY reference clock (ETHn_REFCLK, n = 0 to 2)		25		
	Ethernet PHY reference clock (RMIIn_REFCLK, n = 0 to 2)		50		

AC Characteristics are defined in condition of the IO setting (DRCTLm register setting) show in Table 2.14.

Table 2.14 IO setting (DRCTLm register setting) condition (1 of 2)

Module	Signal		IO type	Voltage	DRCTLm register		
					DRVn	SRn	SMTn
Bus	CKIO	SDRAM and High drive	—	3.3 V	High	Fast	—
		Other than the above	—	3.3 V	Middle	Fast	—
	Other than the above		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
DMAC, MTU3, IIC, CANFD, DSMIF	All signals		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable

Table 2.14 IO setting (DRCTLm register setting) condition (2 of 2)

Module	Signal	IO type	Voltage	DRCTLm register		
				DRVn	SRn	SMTn
GPT (n = 0 to 17) (m = 0, 1)	GTIOCnA, GTIOCnB	Type A	3.3 V	Middle	Slow	Disable
		Type B	3.3 V	Low	Slow	Disable
	GTADSMLm, GTADSMPm	—	3.3 V	Low	Slow	Disable
SCI, SPI	All signals	—	3.3 V	High	Fast	Disable
xSPI (n = 0, 1; m = 0, 1)	XSPIn_CKP, XSPIn_CKN, XSPIn_IO[7:0], XSPIn_CSm#, XSPIn_DS	—	1.8 V	High	Fast	Disable
		—	3.3 V	High	Fast	Enable
	Other than the above	—	—	Low	Slow	Disable
Ethernet Interface (n = 0 to 2)	ETHn_TXCLK, ETHn_TXD[3:0]	—	1.8 V/3.3 V	High	Fast	Disable
	ETHn_TXER	—	3.3 V	Middle	Fast	—
	ETHn_RXCLK, ETHn_RXD[3:0]	—	1.8 V/3.3 V	—	—	Disable
	ETHn_RXER, ETHn_COL, ETHn_CRS	—	3.3 V	—	—	Disable
	ETHn_REFCLK, RMIIn_REFCLK	—	3.3 V	High	Fast	—
	Other than the above	—	—	Low	Slow	Disable
Debug Interface	TRACECLK, TRACECTL,TRACEDATA[7:0], TDO, TMS	—	3.3 V	High	Fast	Disable
	Other than the above	—	—	Low	Slow	Disable
Other than the above		—	—	Low	Slow	Disable

2.5.1 Clock Timing

2.5.1.1 CKIO Pin Output Timing

Table 2.15 CKIO pin output timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CKIO pin output cycle time	t_{CKcyc}	Figure 2.2	10	—	53.4	ns
CKIO pin output high level pulse width	t_{CKH}		t_{CKcyc} / 2 − t_{CKr}	—	—	ns
CKIO pin output low level pulse width	t_{CKL}		t_{CKcyc} / 2 − t_{CKf}	—	—	ns
CKIO pin output rising time 1	t_{CKr}	CKIO: High drive output Setting	—	—	3.8	ns
CKIO pin output falling time 1	t_{CKf}		—	—	3.8	ns
CKIO pin output rising time 2	t_{CKr}	CKIO: Normal output setting	—	—	9	ns
CKIO pin output falling time 2	t_{CKf}		—	—	9	ns

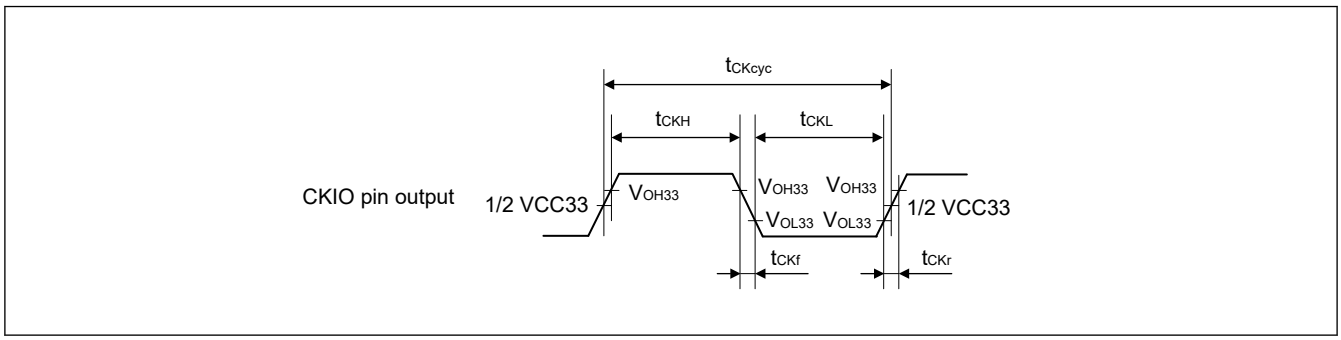


Figure 2.2 CKIO pin output timing

2.5.1.2 Ethernet PHY Reference Clock Output Timing

Conditions:

C = 30 pF (ETHn_REFCLK)

C = 20 pF (RMIIn_REFCLK)

Table 2.16 Ethernet PHY reference clock output timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ETHn_REFCLK cycle time	t_{CK}	Figure 2.3	40	—	—	ns
ETHn_REFCLK frequency	—		25.00 ± 50 ppm			MHz
ETHn_REFCLK duty	—		45	—	55	%
ETHn_REFCLK rising/falling time	t_{CKr} / t_{CKf}		0.5	—	4.0	ns
RMIIn_REFCLK cycle time	t_{CK}		20	—	—	ns
RMIIn_REFCLK frequency	—		50.00 ± 50 ppm			MHz
RMIIn_REFCLK duty	—		45	—	55	%
RMIIn_REFCLK rising/falling time	t_{CKr} / t_{CKf}		0.5	—	3.5	ns

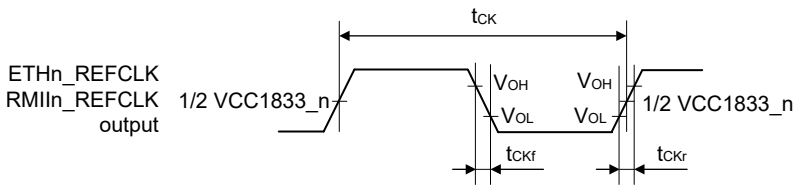


Figure 2.3 Ethernet PHY reference clock output timing

2.5.1.3 EXTCLKIN External Clock Input

Table 2.17 EXTCLKIN clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTCLKIN external clock frequency	$f_{EXTCLKIN}$	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
EXTCLKIN duty	$r_{EXTCLKIN}$	—	±5%			—
EXTCLKIN rising time	$t_{rEXTCLKIN}$	—	0	—	5	ns
EXTCLKIN falling time	$t_{fEXTCLKIN}$	—	0	—	5	ns

Note: When using crystal resonator (i.e. EXTA/XTAL clock is used), EXTCLKIN should be driven low.

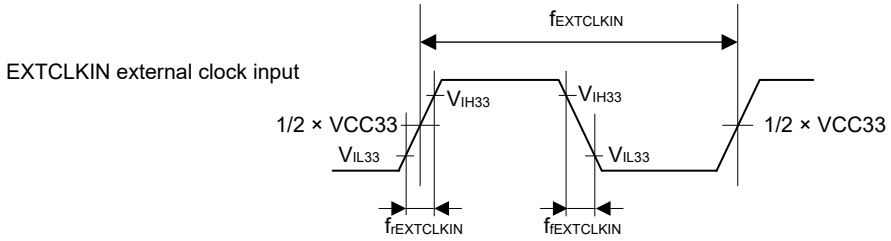


Figure 2.4 EXTCLKIN external clock input timing

2.5.1.4 EXTAL/XTAL Clock Timing

Table 2.18 EXTAL/XTAL clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTAL/XTAL clock frequency*1	f_{XTAL}	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz

Note: When using an external oscillator, be sure to leave XTAL open-circuit and make sure that EXTAL is driven low.
Note 1. When using the EXTAL/XTAL clock (i.e. crystal resonator), ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.

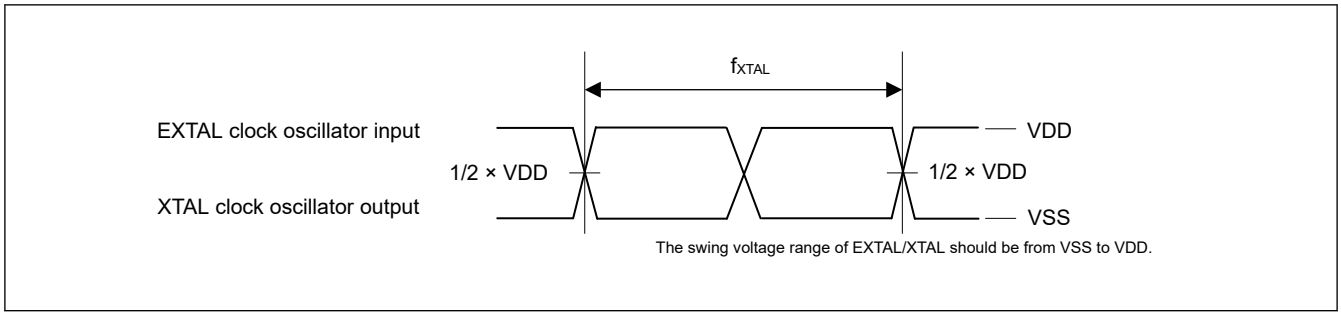


Figure 2.5 EXTAL clock oscillator input and XTAL clock oscillator output timing

2.5.1.5 LOCO Clock Timing

Table 2.19 LOCO clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOCO clock cycle time	t_{Lcyc}	—	4.62	4.17	3.79	µs
LOCO clock oscillation frequency	t_{LOCO}	—	216	240	264	kHz
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	—	40	µs

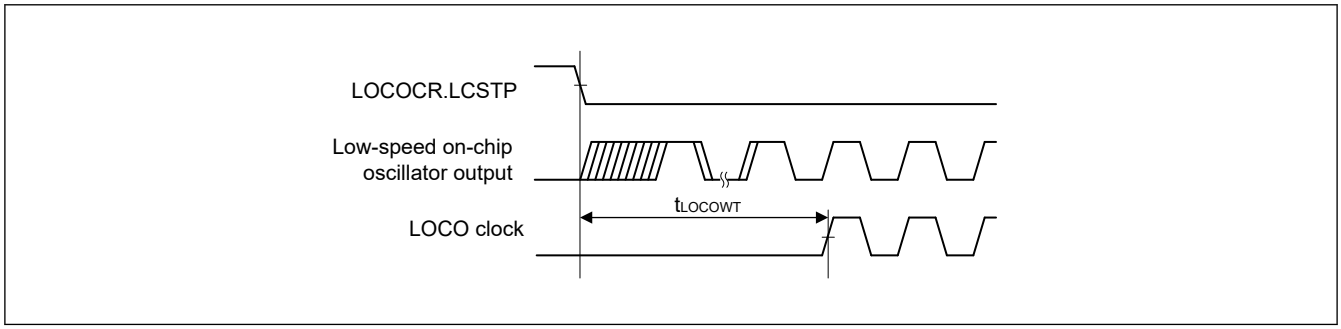


Figure 2.6 LOCO clock oscillation start timing

2.5.2 Reset, Interrtup, and Mode Timing

Table 2.20 Reset, interrupt, and mode timing (1 of 2)

Parameter		Symbol	Conditions	Min.*1	Typ.	Max.	Unit
RES# pulse width	At power on	$t_{dlyreset}$	Figure 2.7	10	—	—	ms
	Other than above	$t_{dlyreset2}$		1	—	—	ms
RES# rising time		$t_{risereset}$		—	—	150	µs
TRST# pulse width	At power on	$t_{dlyreset}$		10	—	—	ms
	Other than above	$t_{dlyreset2}$		1	—	—	ms
TRST# rising time		$t_{risereset}$		—	—	150	µs

Table 2.20 Reset, interrupt, and mode timing (2 of 2)

Parameter		Symbol	Conditions	Min.*1	Typ.	Max.	Unit
NMI pulse width		t_{NMIW}	Figure 2.8	t_{Icyc} × 2	—	—	ns
IRQ pulse width		t_{IRQW}	Figure 2.9	t_{Icyc} × 2	—	—	ns
Mode hold time (to RES#)	At power on	t_{MDH}	Figure 2.10	250	—	—	ns

Note 1. t_{Icyc}: ICLK cycle

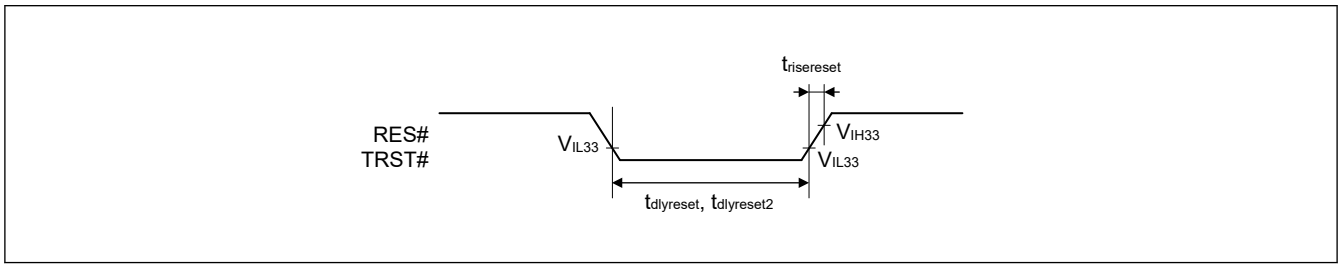


Figure 2.7 Reset input timing

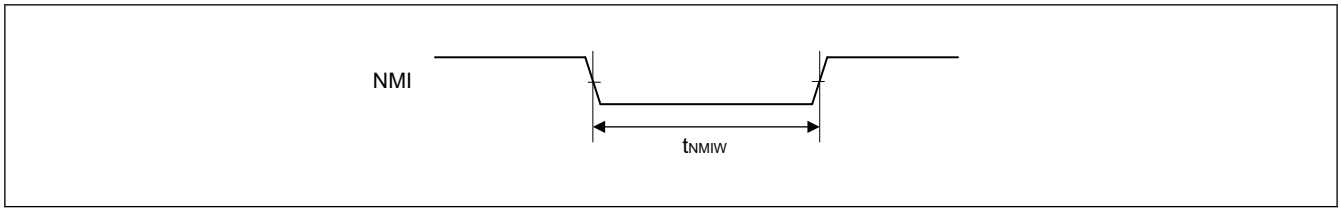


Figure 2.8 NMI interrupt input timing

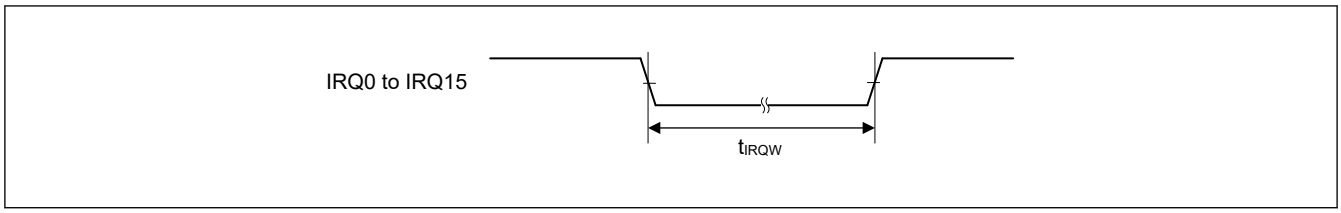


Figure 2.9 IRQ interrupt input timing

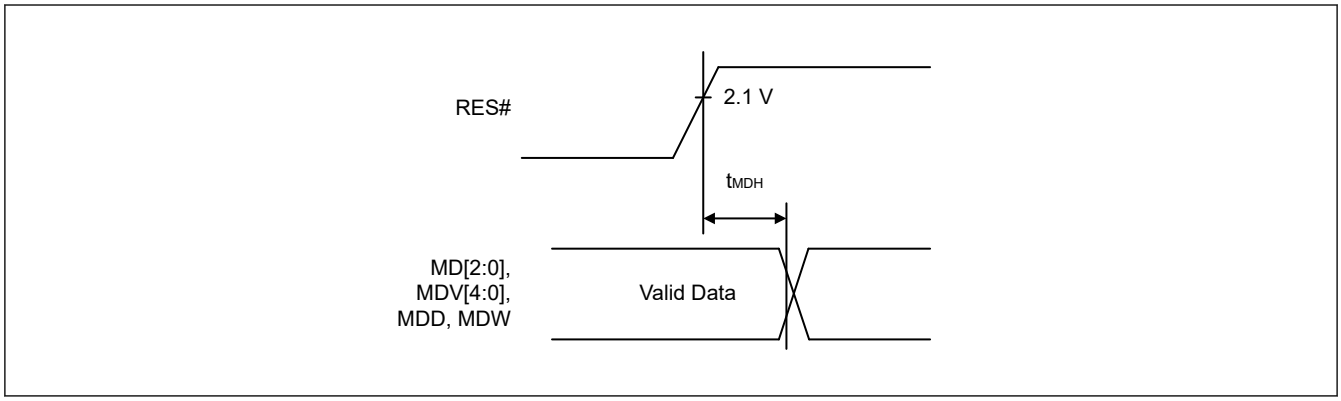


Figure 2.10 Mode input timing

2.5.3 Bus Timing

Table 2.21 Bus timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter		Symbol	CKIO = $1/t_{CKcyc}$ *1 (Max 66 MHz)		Unit	Reference Figure
			Min.	Max.		
Address delay time 1	SDRAM*2	t_{AD1}	2	11	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	10	ns	
Address delay time 2		t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.18
Address setup time		t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Chip enable setup time		t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Address hold time		t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time		t_{BSD}	—	11	ns	Figure 2.11 to Figure 2.32
CSn# delay time 1	SDRAM*2	t_{CSD1}	2	11	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	10	ns	
Read/write delay time 1	SDRAM*2	t_{RWD1}	2	11	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	10	ns	
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.11 to Figure 2.18
Read data setup time 1*3	High-drive output	t_{RDS1}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.11 to Figure 2.17
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data setup time 2*3	High-drive output	t_{RDS2}	6.6	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data setup time 3*3	High-drive output	t_{RDS3}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Read data hold time 2		t_{RDH2}	2.5	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2		t_{WED2}	—	11	ns	Figure 2.17
Write data delay time 1		t_{WDD1}	—	11	ns	Figure 2.11 to Figure 2.17
Write data delay time 2		t_{WDD2}	—	11	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 2		t_{WDH2}	2	—	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 4		t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time*3	High-drive output	t_{WTS}	$1/2t_{CKcyc}$ + 4.5	—	ns	Figure 2.12 to Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 8	—	ns	
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.12 to Figure 2.18
RAS# delay time 1		t_{RASD1}	2	11	ns	Figure 2.19 to Figure 2.35
CAS# delay time 1		t_{CASD1}	2	11	ns	Figure 2.19 to Figure 2.35

Table 2.21 Bus timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter	Symbol	CKIO = $1/t_{CKcyc}$ *1 (Max 66 MHz)		Unit	Reference Figure
		Min.	Max.		
DQM delay time 1	t_{DQMD1}	2	11	ns	Figure 2.19 to Figure 2.32
CKE delay time 1	t_{CKED1}	2	11	ns	Figure 2.34
AH# delay time	t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.15
Multiplex address delay time	t_{MAD}	—	10	ns	Figure 2.15
Multiplex address hold time	t_{MAH}	1	—	ns	Figure 2.15
Address setup time to AH#	t_{AVVH}	$1/2t_{CKcyc}$ − 2	—	ns	Figure 2.15
DACK/TEND delay time	t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.32

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the fmax value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, select high drive output.

Note 2. These are values when SDRAM (CSnBCR.TYPE[2:0] = 100b) is selected in the CSn space bus control register (CSnBCR) and high-drive output is selected for CKIO.

Note 3. These are values when high-drive output and normal output are respectively selected for CKIO.

Table 2.22 Bus timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), $T_j$min = −20°C

Parameter		Symbol	CKIO = $1/t_{CKcyc}$ *1 (Max 100 MHz)		Unit	Reference Figure
			Min.	Max.		
Address delay time 1	SDRAM*2	t_{AD1}	1.3	8	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	8	ns	
Address delay time 2		t_{AD2}	$1/2t_{CKcyc}$ - 0.5	$1/2t_{CKcyc}$ + 8	ns	Figure 2.18
Address setup time		t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Chip enable setup time		t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Address hold time		t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time		t_{BSD}	—	8	ns	Figure 2.11 to Figure 2.32
CSn# delay time 1	SDRAM*2	t_{CSD1}	1.3	8	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	8	ns	
Read/write delay time 1	SDRAM*2	t_{RWD1}	1.3	8	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	8	ns	
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.11 to Figure 2.18
Read data setup time 1*3	High-drive output	t_{RDS1}	$1/2t_{CKcyc}$ + 4.5	—	ns	Figure 2.11 to Figure 2.17
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data setup time 2*3	High-drive output	t_{RDS2}	3.5	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data setup time 3*3	High-drive output	t_{RDS3}	$1/2t_{CKcyc}$ + 4.5	—	ns	Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17

Table 2.22 Bus timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), $T_j$min = −20°C

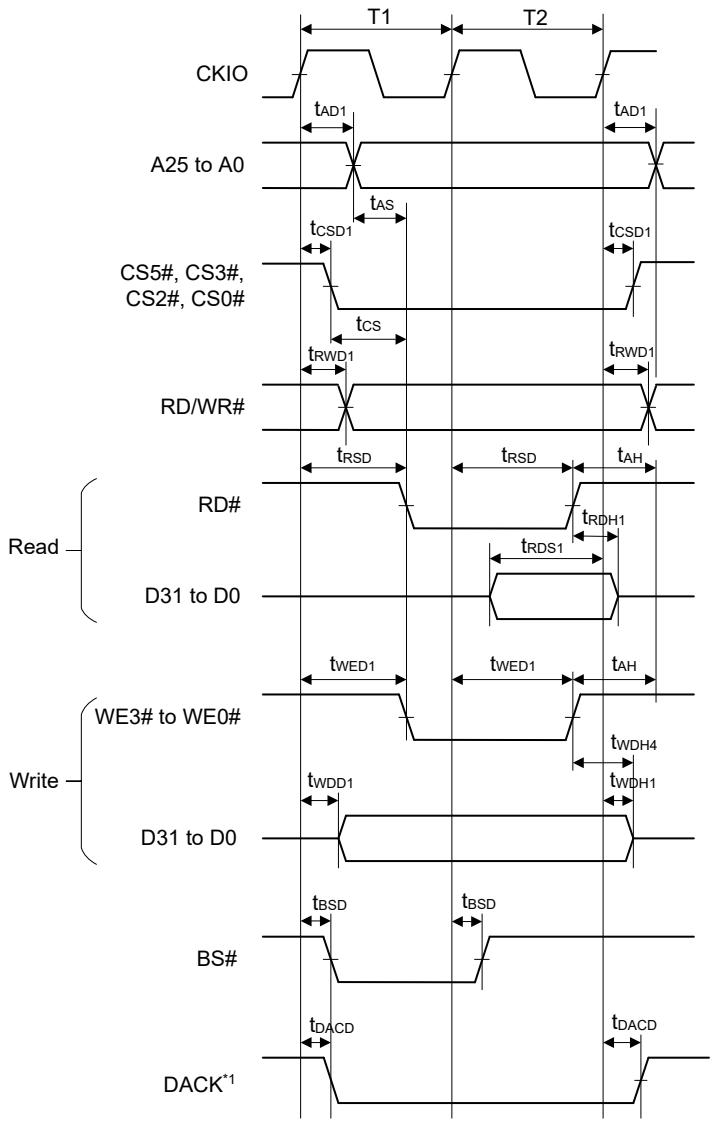
Parameter		Symbol	CKIO = $1/t_{CKcyc}$ *1 (Max 100 MHz)		Unit	Reference Figure
			Min.	Max.		
Read data hold time 2		t_{RDH2}	2.5	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2		t_{WED2}	—	9	ns	Figure 2.17
Write data delay time 1		t_{WDD1}	—	8	ns	Figure 2.11 to Figure 2.17
Write data delay time 2		t_{WDD2}	—	8	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 2		t_{WDH2}	1.3	—	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 4		t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time*3	High-drive output	t_{WTS}	$1/2t_{CKcyc}$ + 4.5	—	ns	Figure 2.12 to Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 8	—	ns	
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.12 to Figure 2.18
RAS# delay time 1		t_{RASD1}	1.3	8	ns	Figure 2.19 to Figure 2.35
CAS# delay time 1		t_{CASD1}	1.3	8	ns	Figure 2.19 to Figure 2.35
DQM delay time 1		t_{DQMD1}	1.3	8	ns	Figure 2.19 to Figure 2.32
CKE delay time 1		t_{CKED1}	1.3	8	ns	Figure 2.34
AH# delay time		t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 8	ns	Figure 2.15
Multiplex address delay time		t_{MAD}	—	8	ns	Figure 2.15
Multiplex address hold time		t_{MAH}	1	—	ns	Figure 2.15
Address setup time to AH#		t_{AVVH}	$1/2t_{CKcyc}$ − 2	—	ns	Figure 2.15
DACK/TEND delay time		t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.32

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the fmax value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, select high drive output.

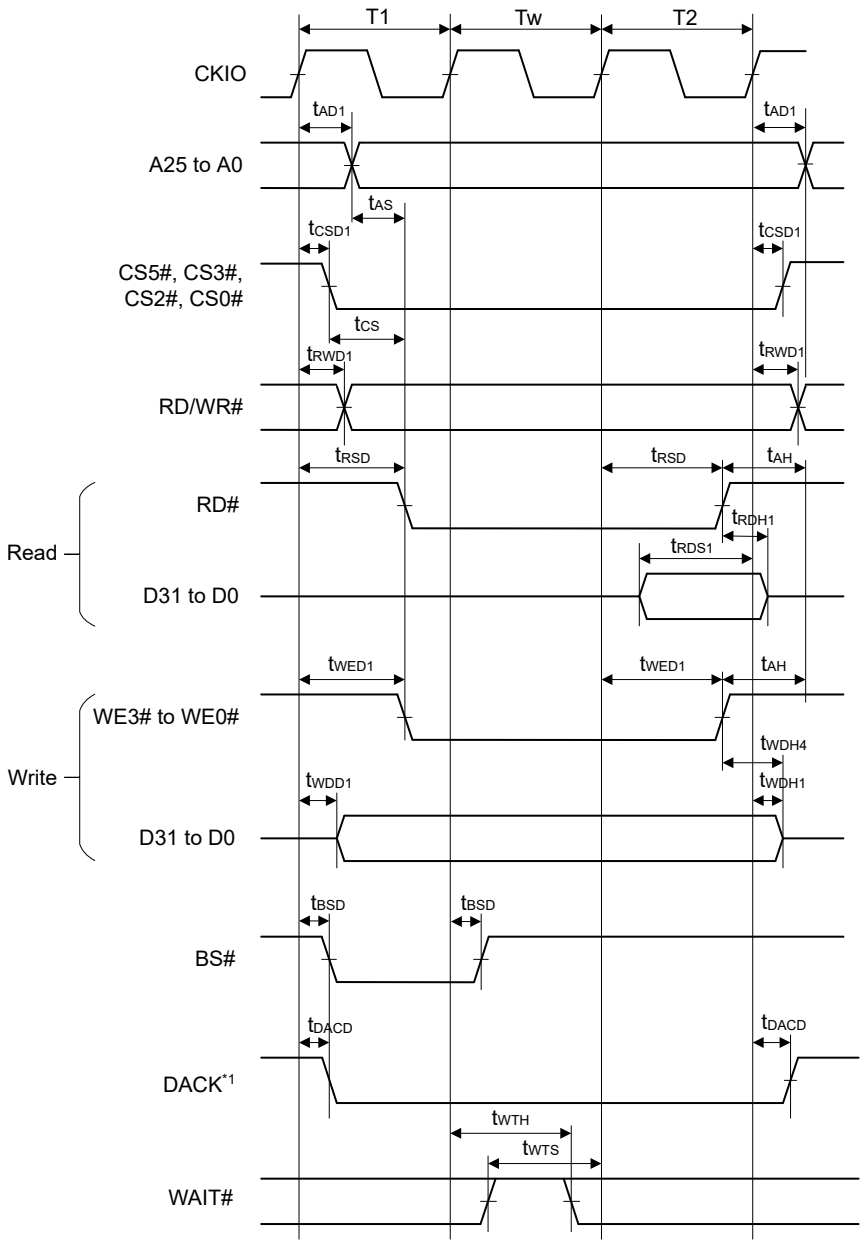
Note 2. These are values when SDRAM (CSnBCR.TYPE[2:0] = 100b) is selected in the CSn space bus control register (CSnBCR) and high-drive output is selected for CKIO.

Note 3. These are values when high-drive output and normal output are respectively selected for CKIO.



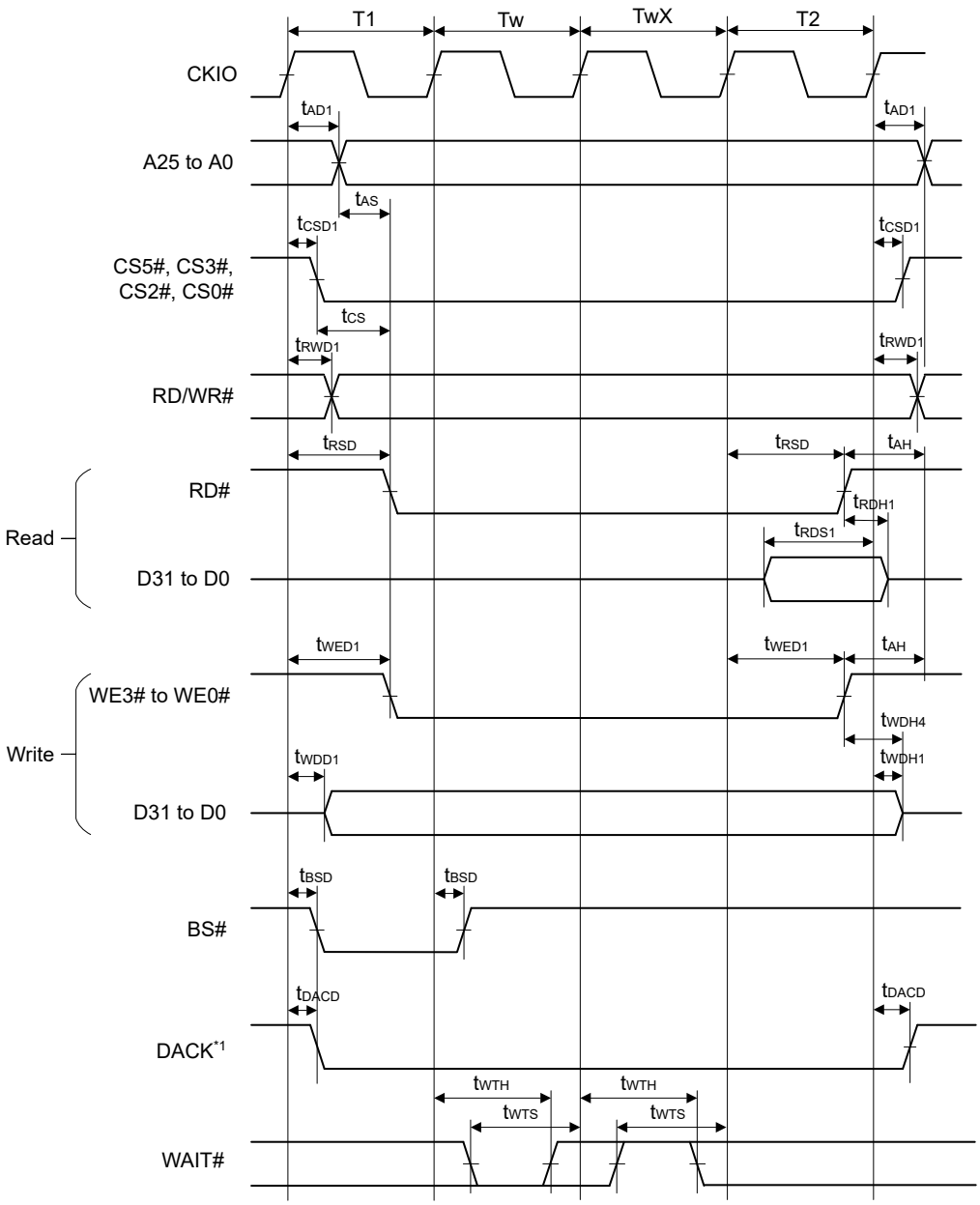
Note 1. DACK is waveform when active-low is specified.

Figure 2.11 SRAM interface basic bus cycle (no wait)



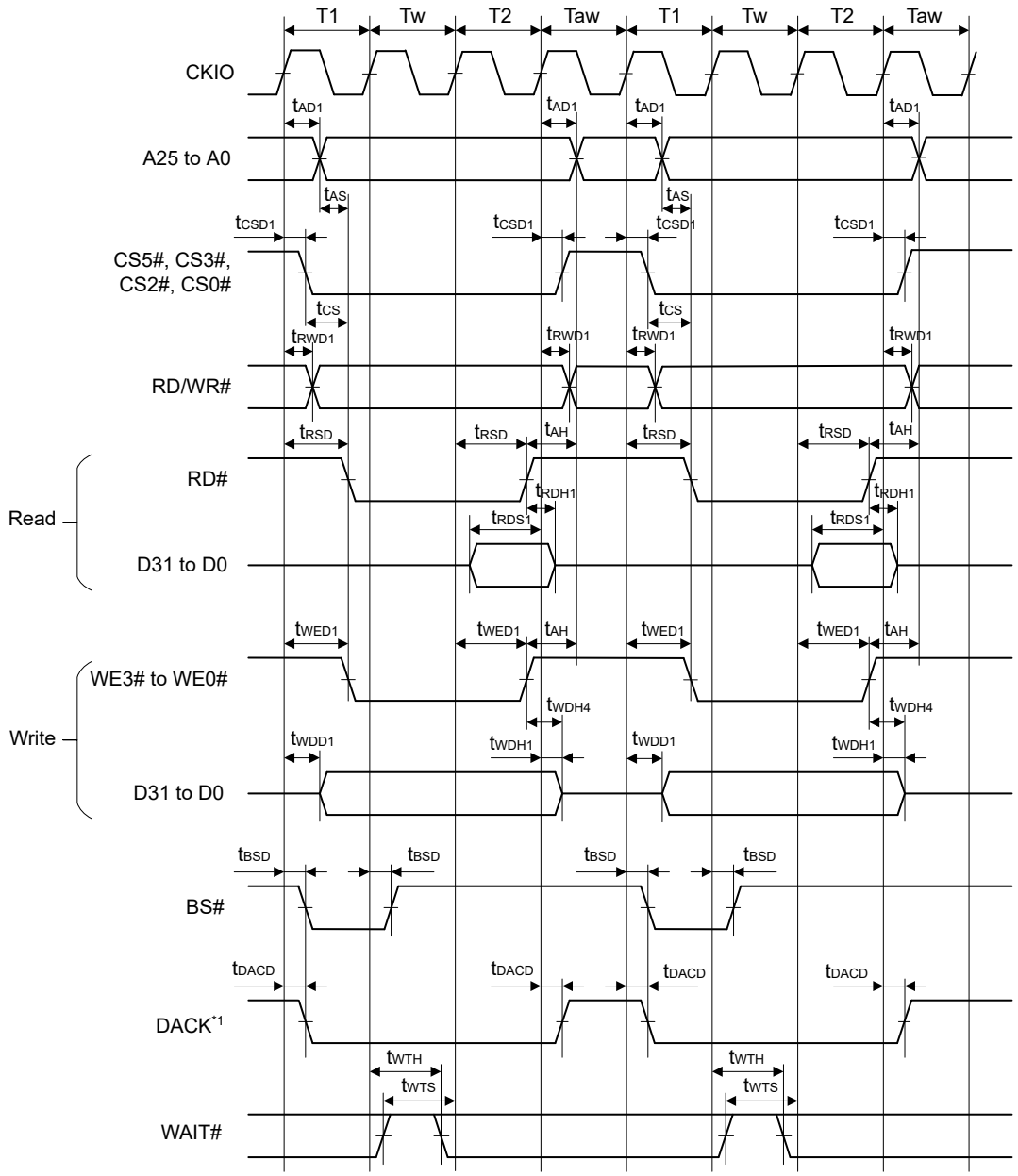
Note 1. DACK is waveform when active-low is specified.

Figure 2.12 SRAM interface basic bus cycle (software wait 1)



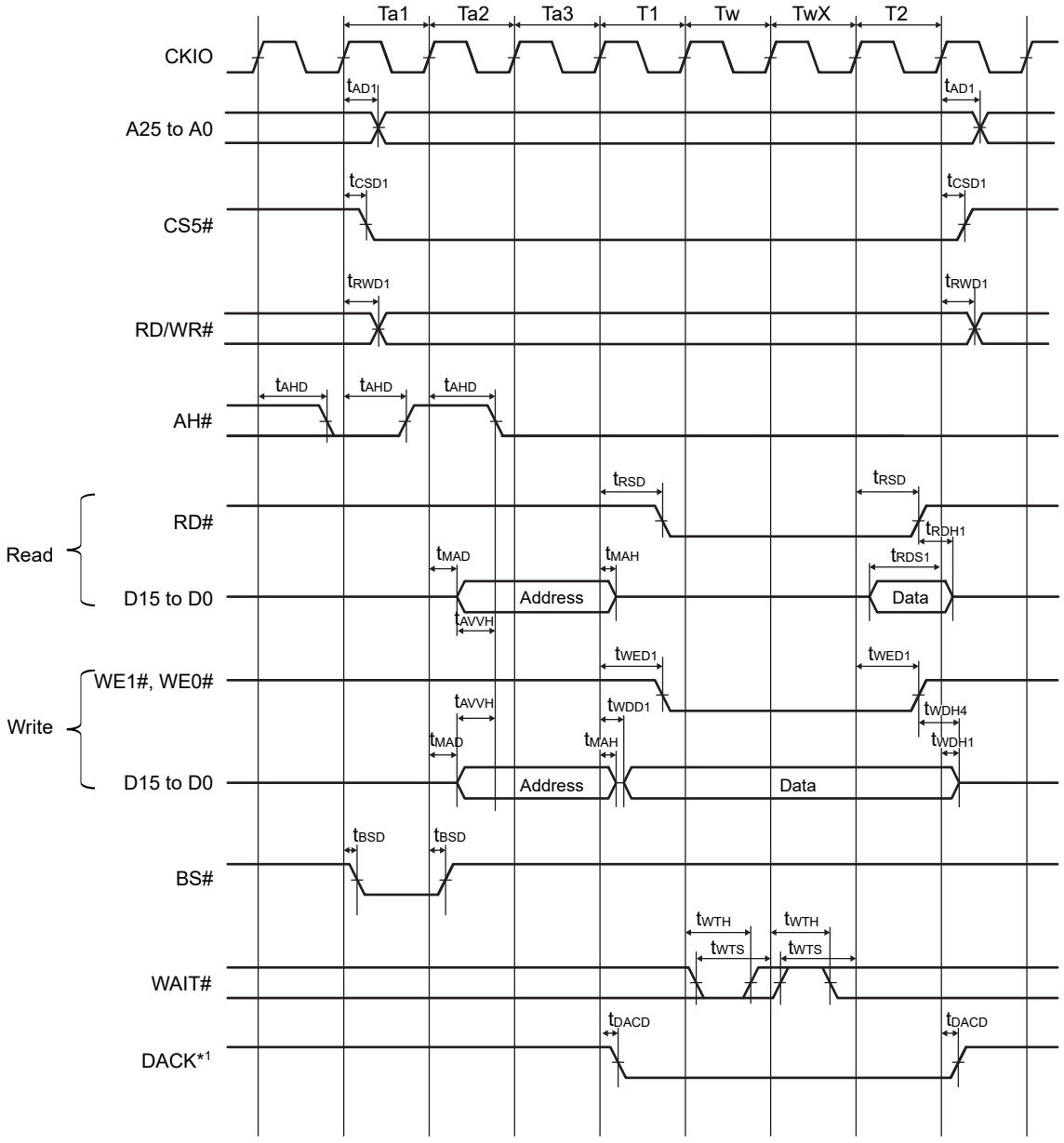
Note 1. DACK is waveform when active-low is specified.

Figure 2.13 SRAM interface basic bus cycle (software wait 1, external wait 1 inserted)



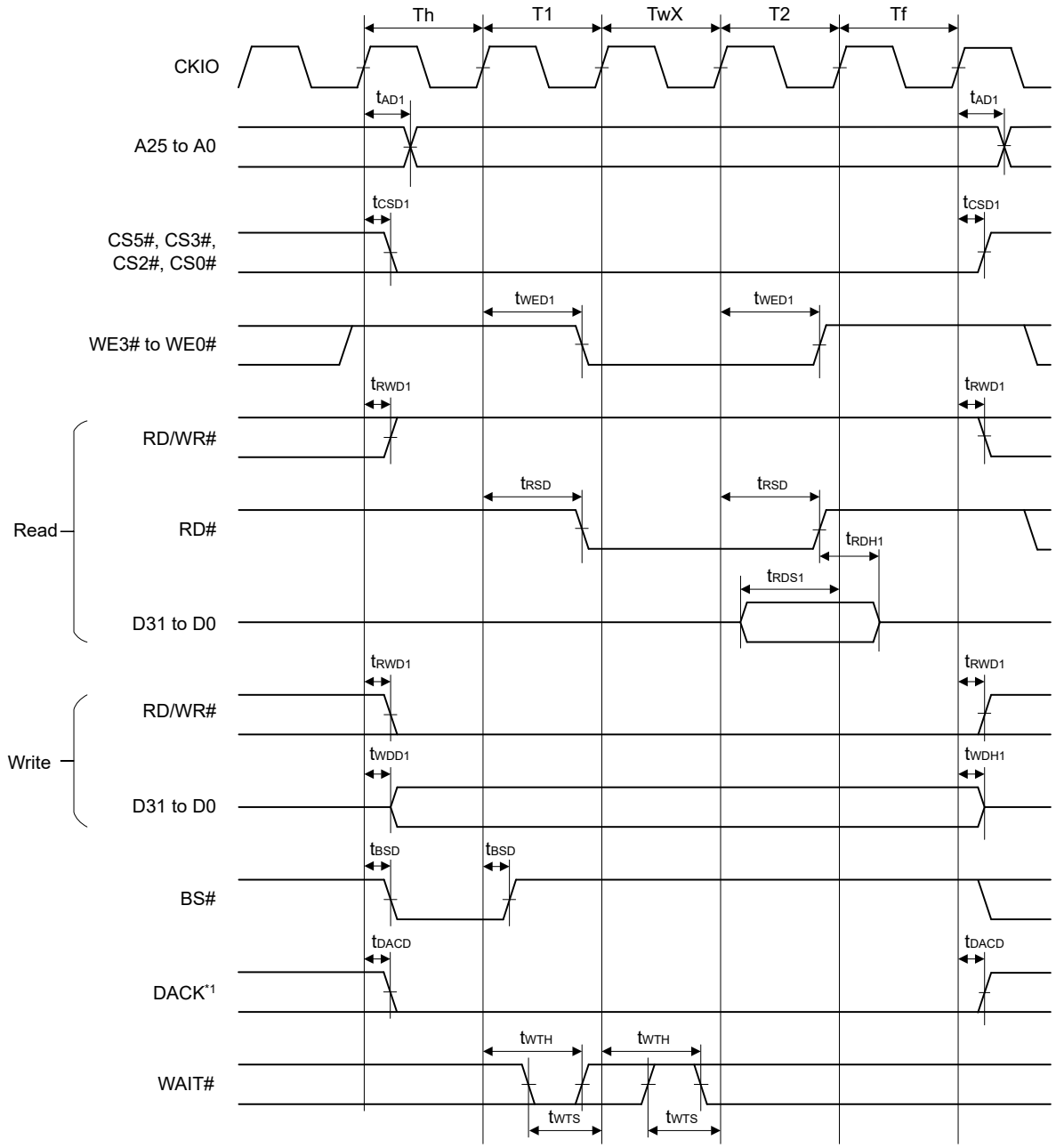
Note 1. DACK is waveform when active-low is specified.

Figure 2.14 SRAM interface basic bus cycle (software wait 1, external wait enabled (WM = 0), no idle cycle)



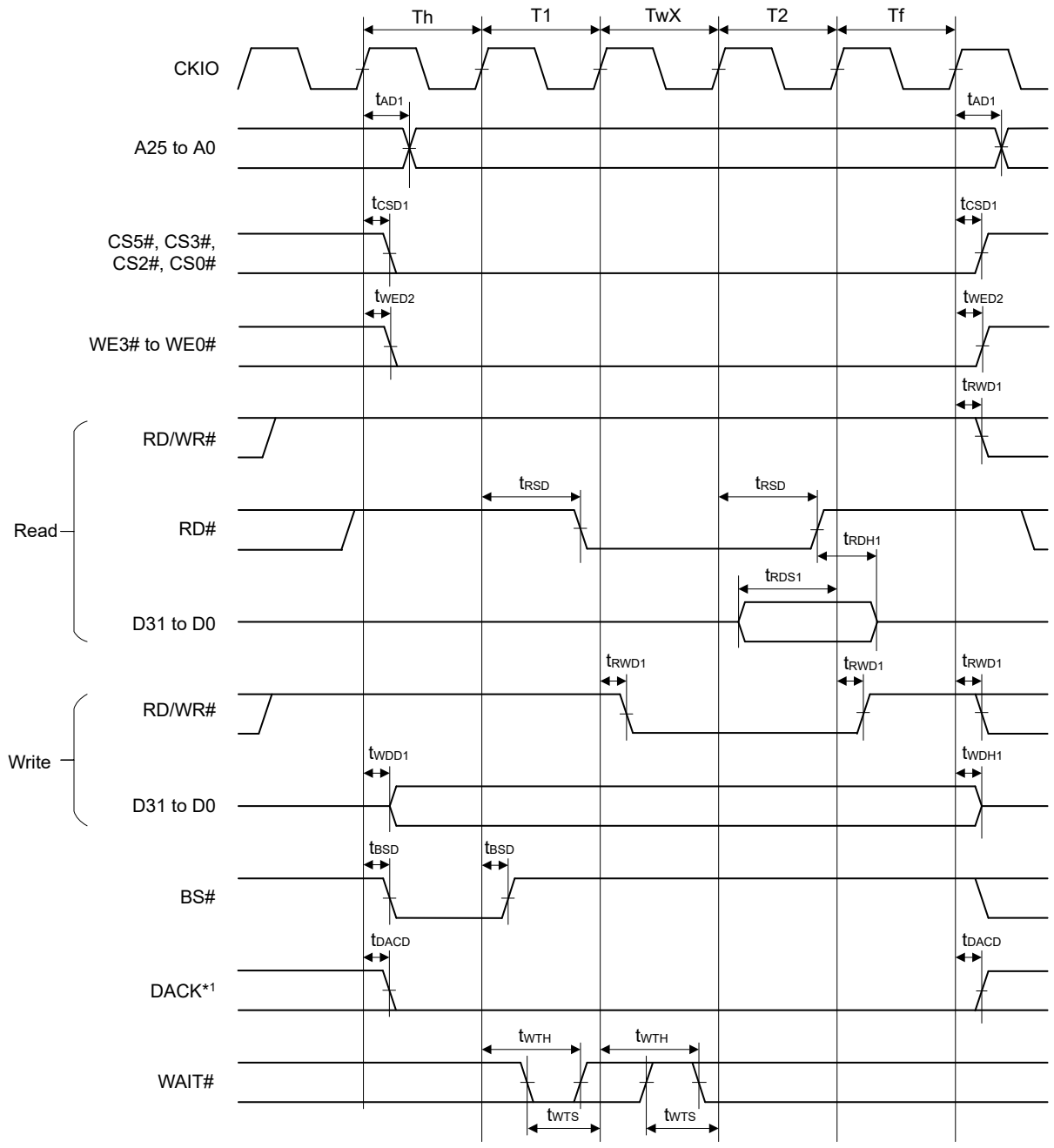
Note 1. DACK is waveform when active-low is specified.

Figure 2.15 MPX-I/O interface bus cycle (address cycle 3, software wait 1, external wait 1 inserted)



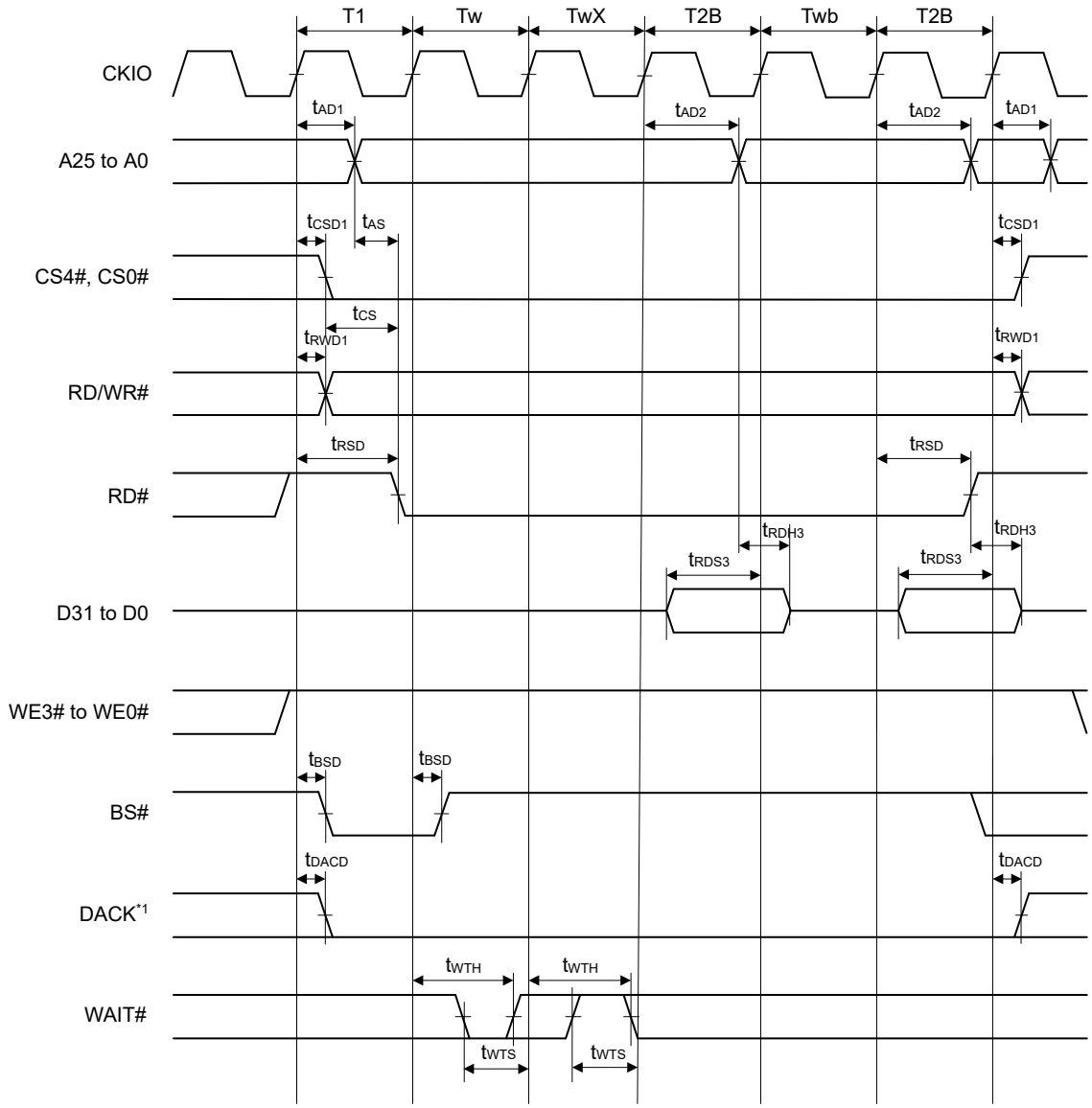
Note 1. DACK is waveform when active-low is specified.

Figure 2.16 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 0 (write cycle UB/LB control))



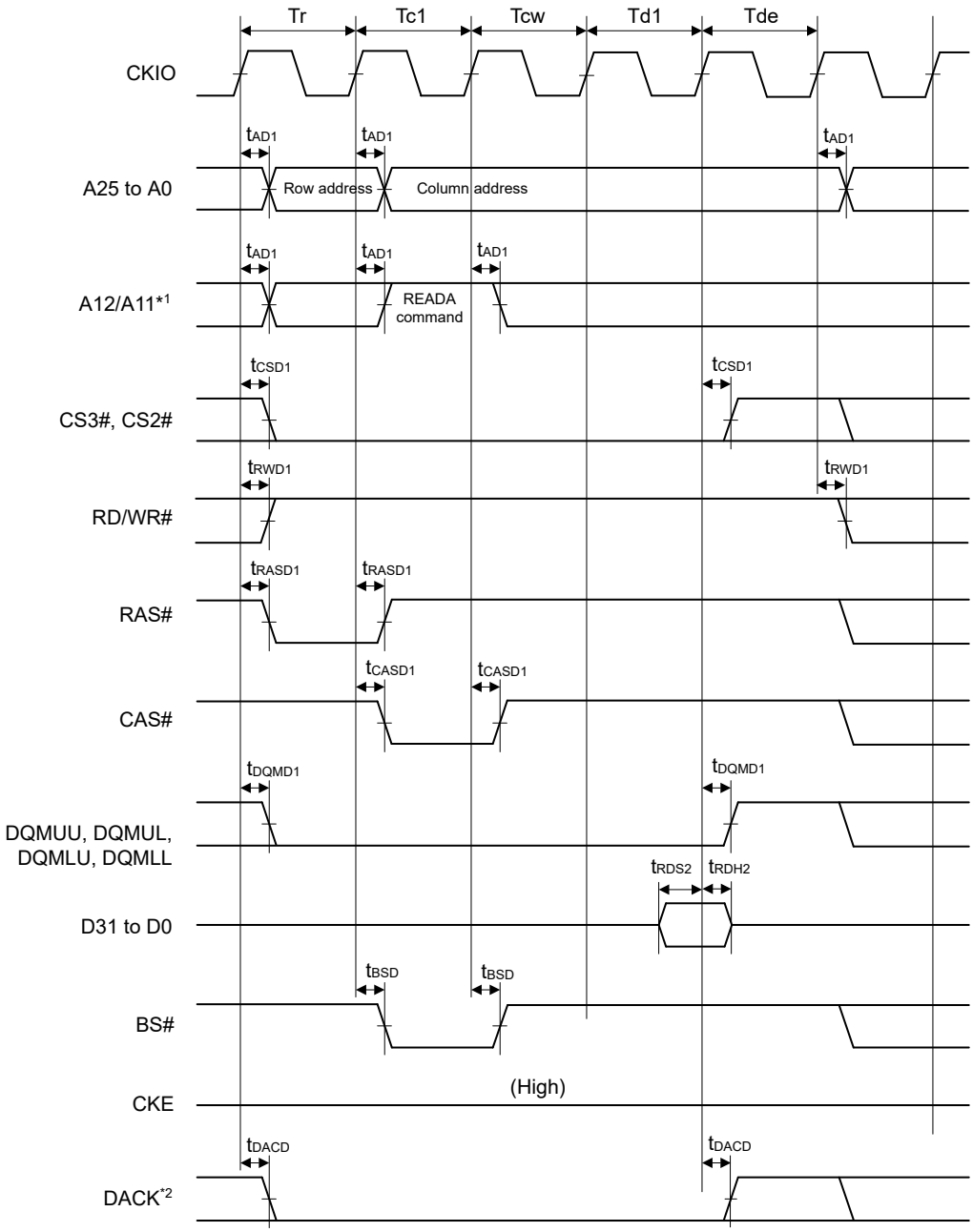
Note 1. DACK is waveform when active-low is specified.

Figure 2.17 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 1 (write cycle WE control))



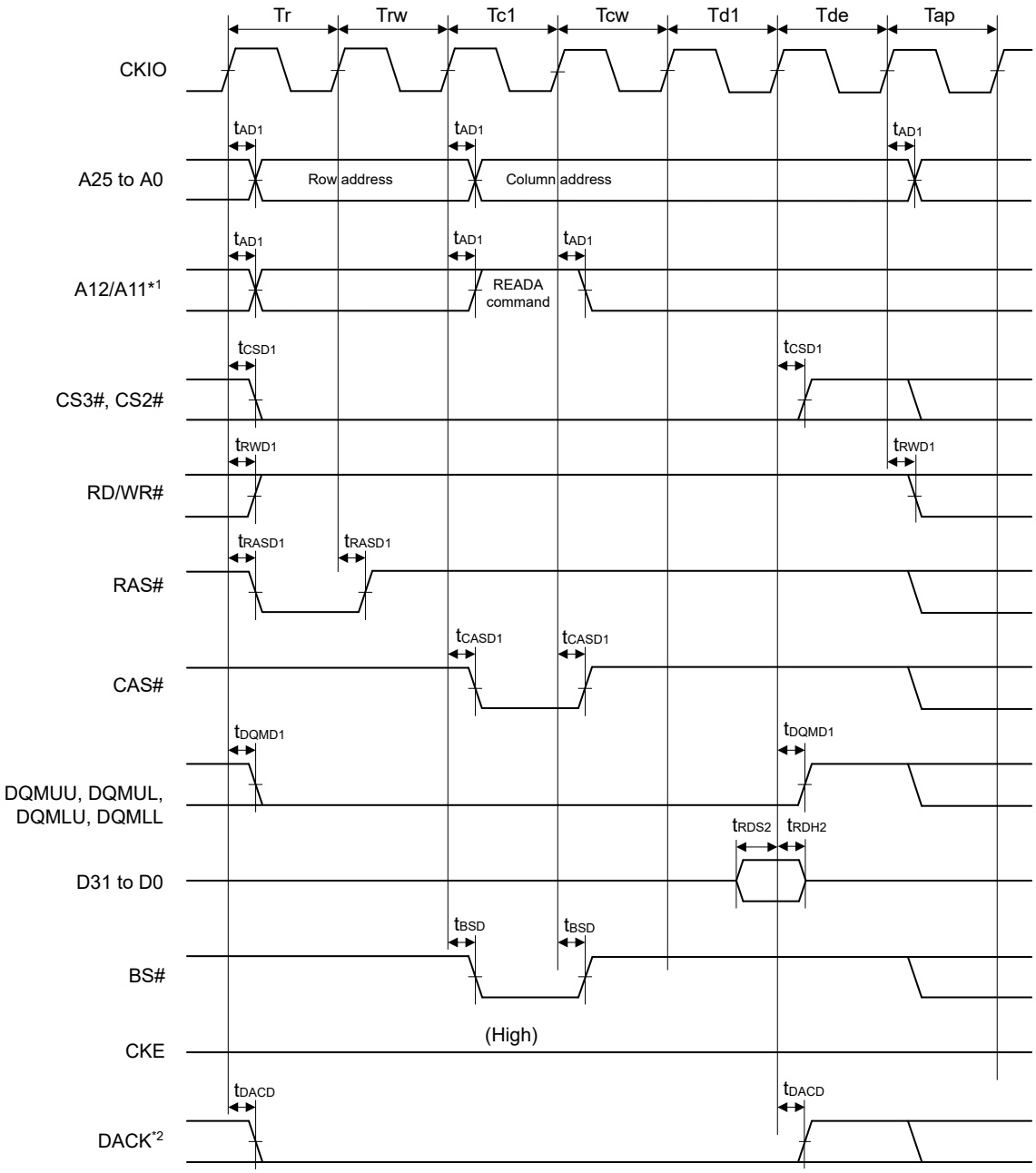
Note 1. DACK is waveform when active-low is specified.

Figure 2.18 Burst ROM read cycle (software wait 1, asynchronous external wait 1 inserted, burst wait 1, 2)



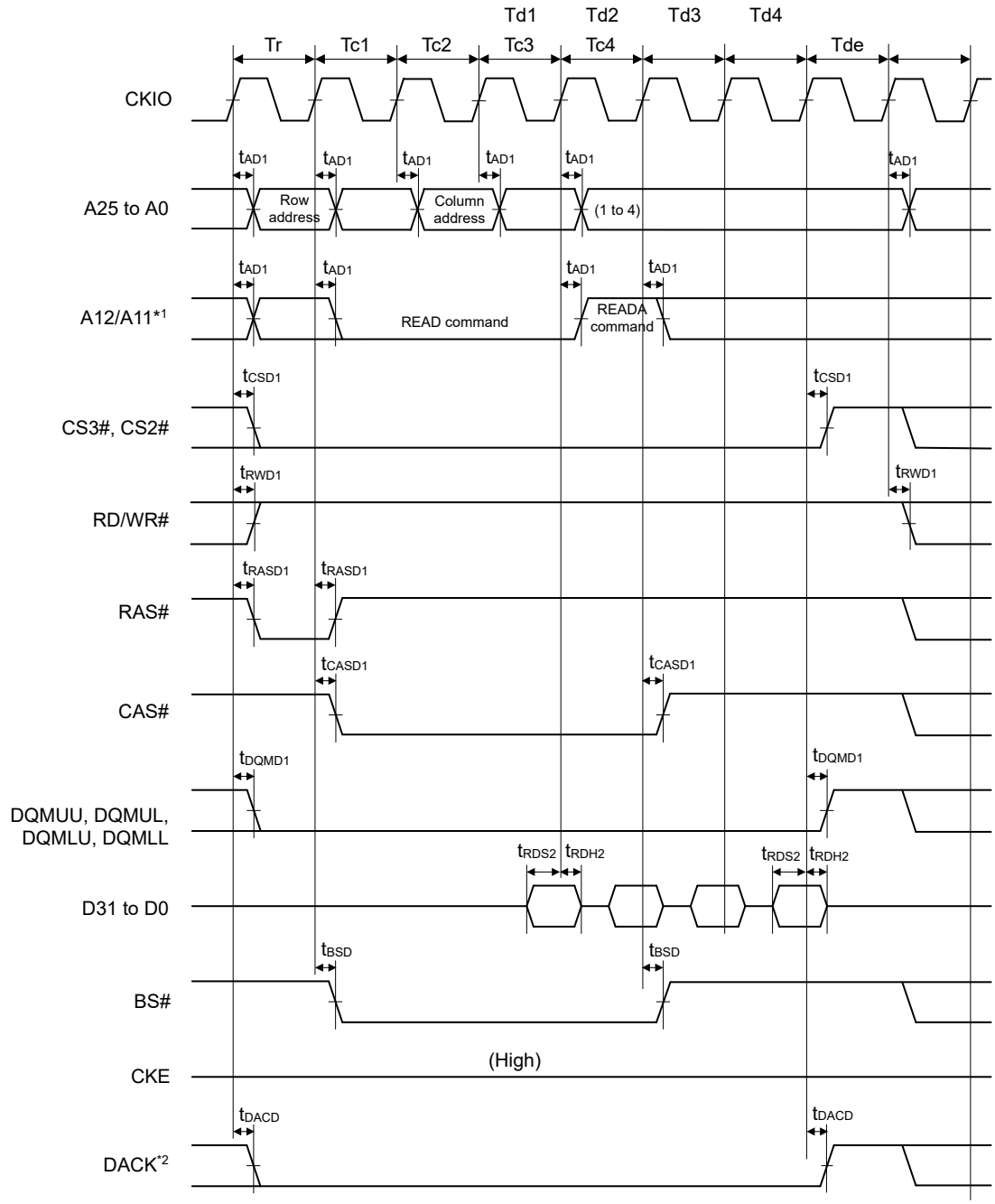
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.19 Synchronous DRAM single-read bus cycle (with auto precharge, CAS latency 2, WTRCD = 0 cycles, WTRP = 0 cycles)



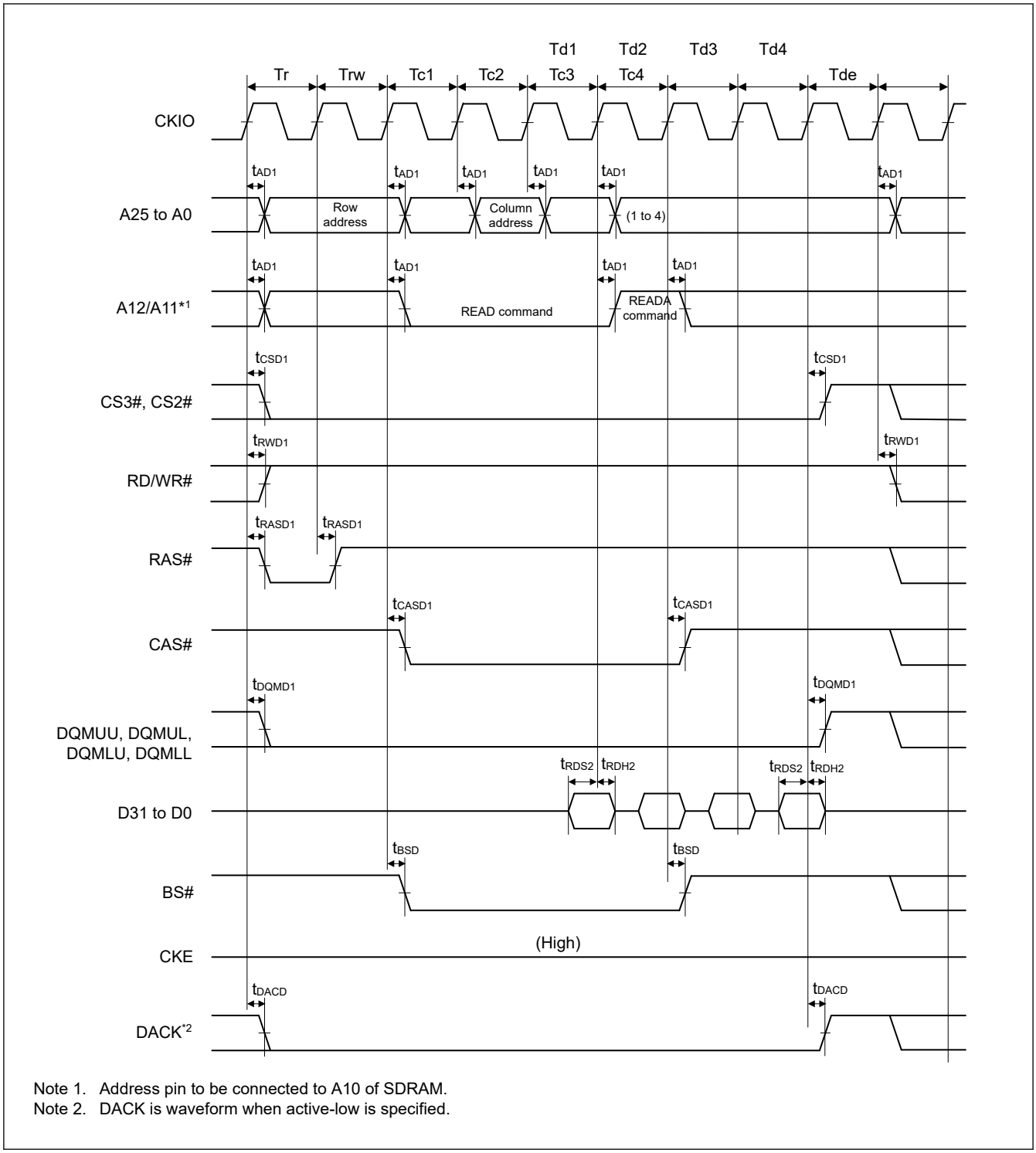
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.20 Synchronous DRAM single-read bus cycle (with auto precharge, CAS latency 2, WTRCD = 1 cycle, WTRP = 1 cycle)



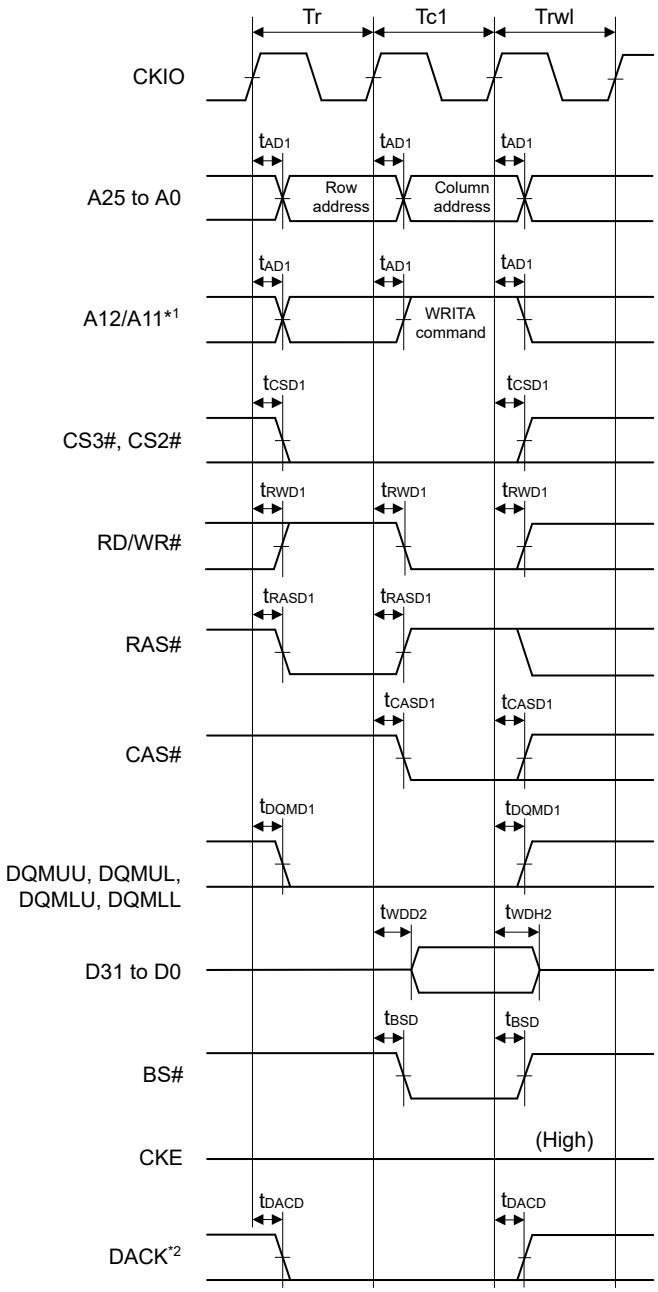
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.21 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (with auto precharge, CAS latency 2, WTRCD = 0 cycles, WTRP = 1 cycle)



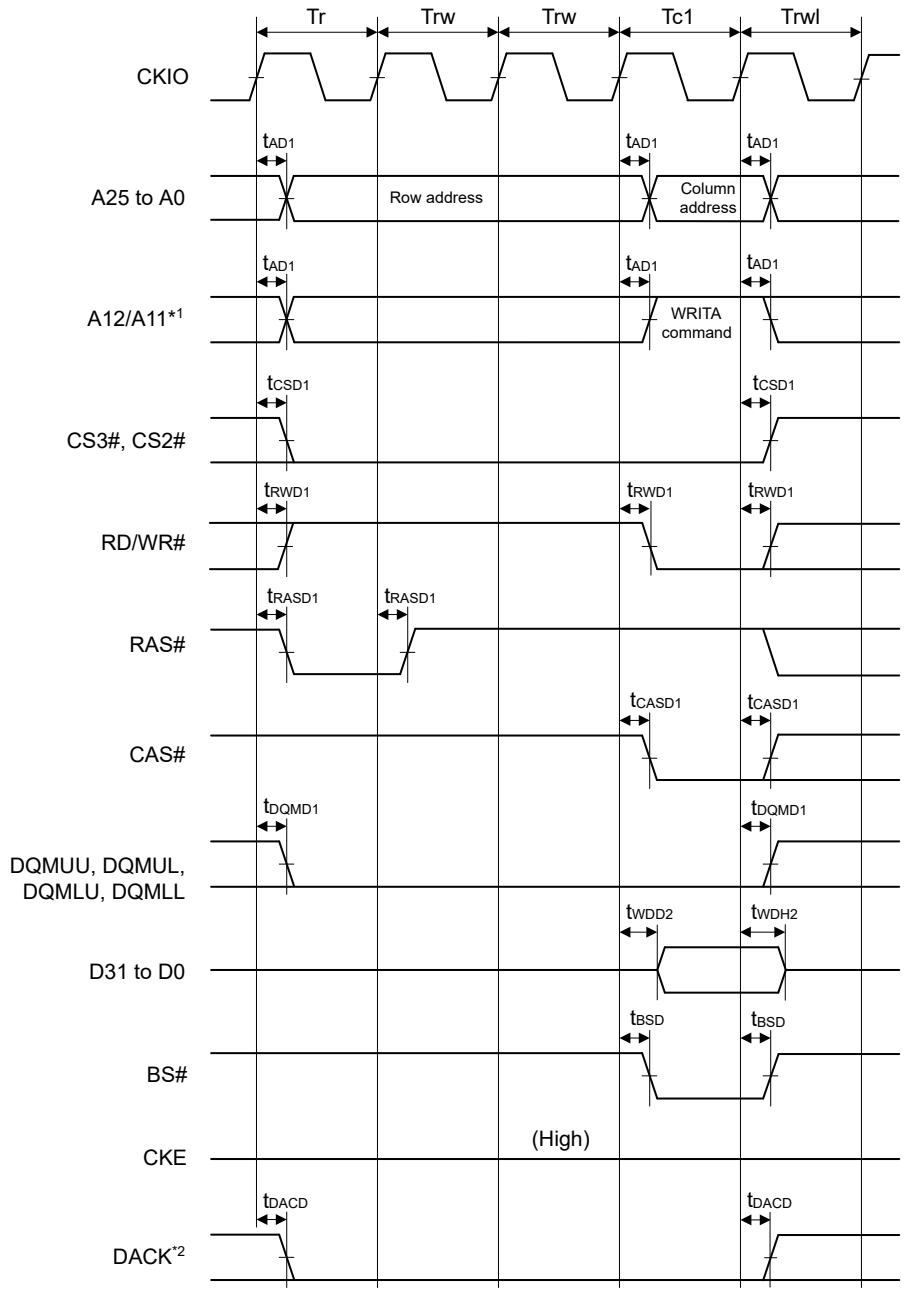
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.22 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (with auto precharge, CAS latency 2, WTRCD = 1 cycle, WTRP = 0 cycles)



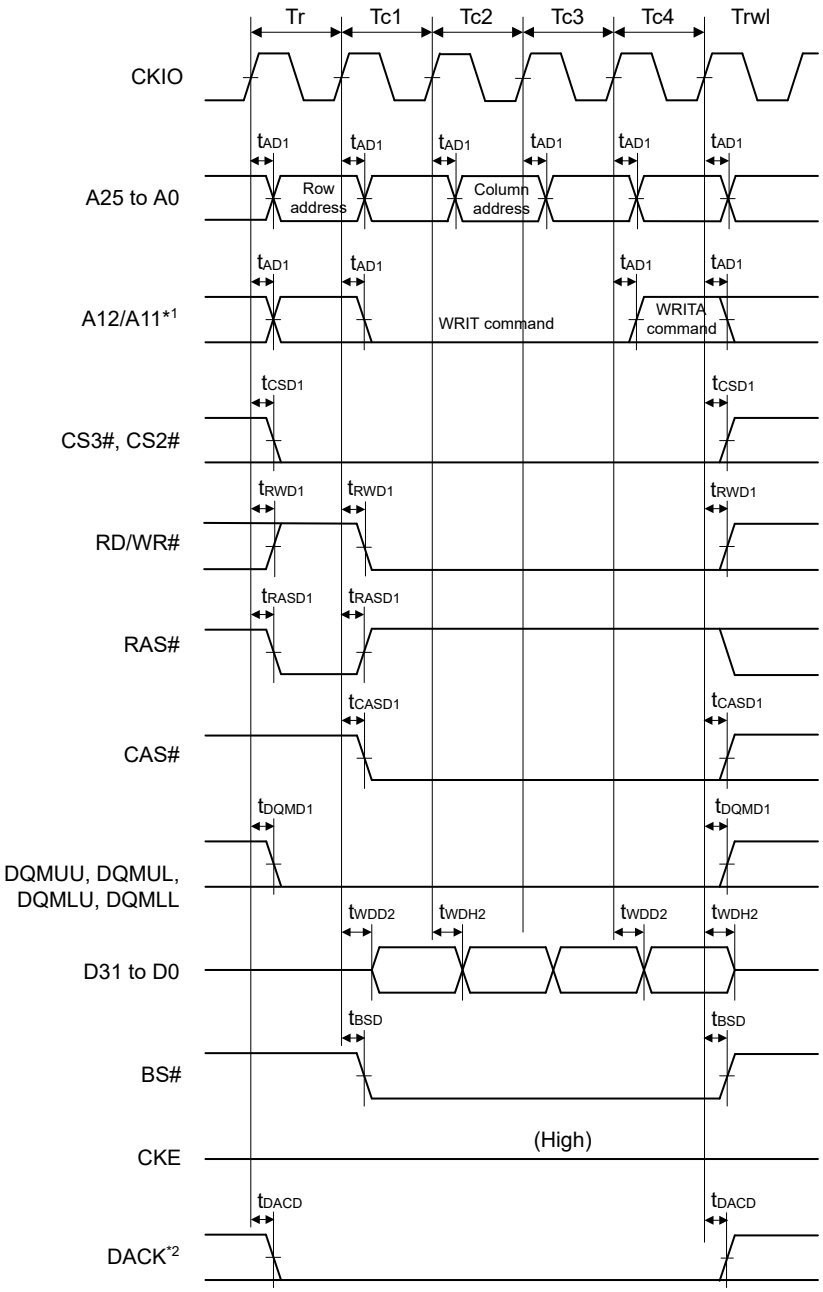
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.23 Synchronous DRAM single-write bus cycle (with auto precharge, TRWL = 1 cycle)



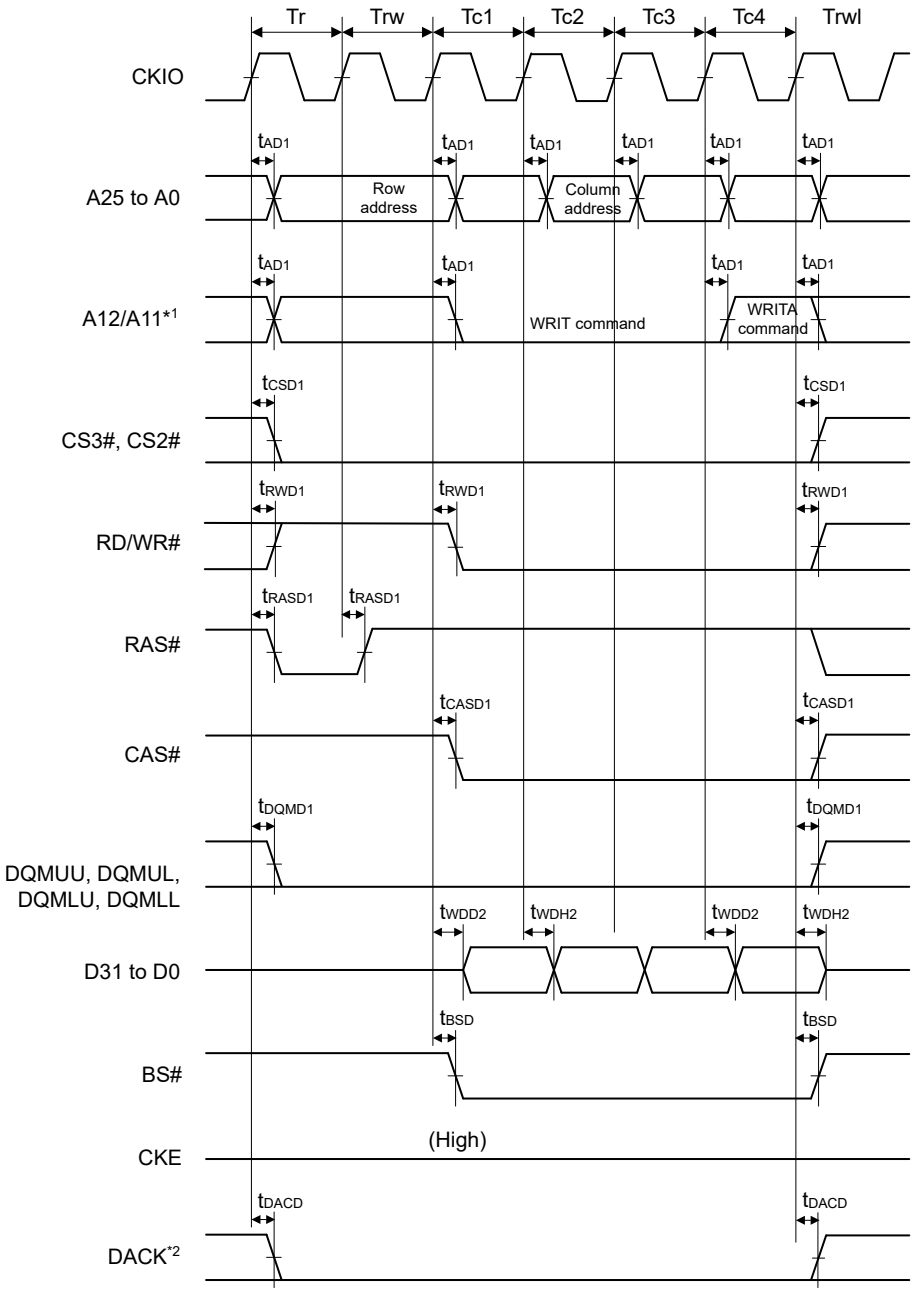
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.24 Synchronous DRAM single-write bus cycle (with auto precharge, WTRCD = 2 cycles, TRWL = 1 cycle)



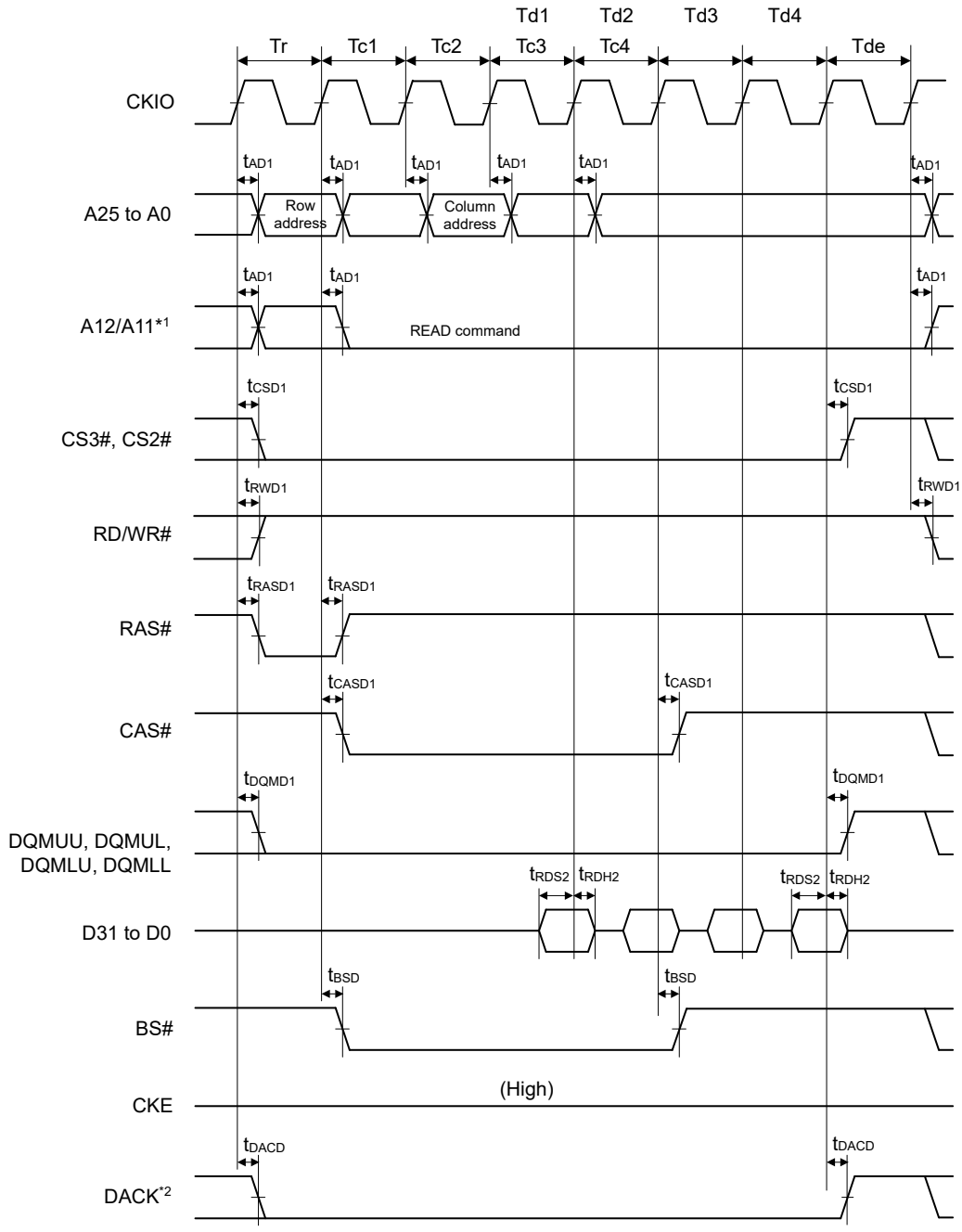
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.25 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (with auto precharge, WTRCD = 0 cycles, TRWL = 1 cycle)



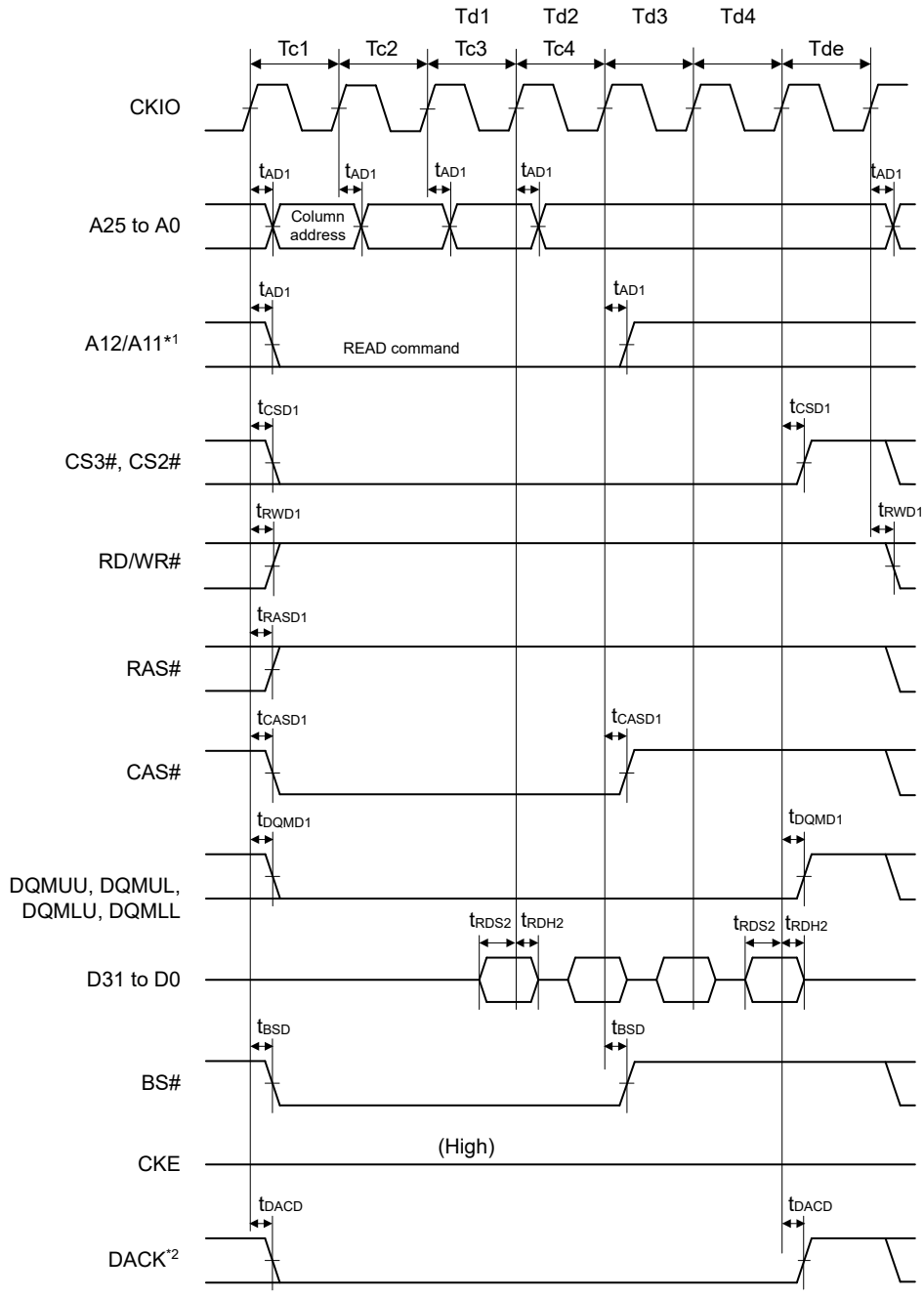
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.26 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (with auto precharge, WTRCD = 1 cycle, TRWL = 1 cycle)



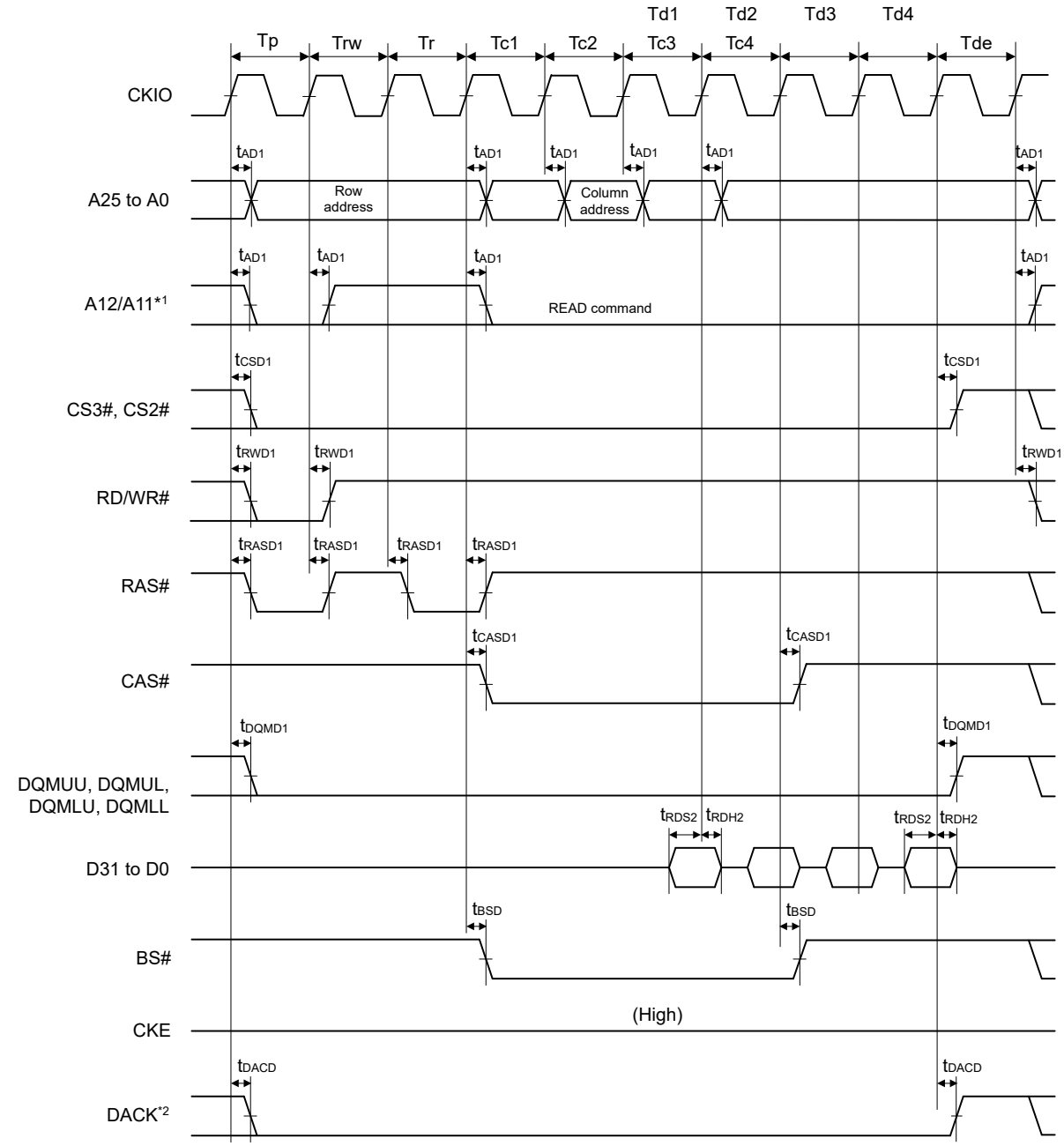
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.27 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (bank active mode: ACT + READ command, CAS latency 2, WTRCD = 0 cycles)



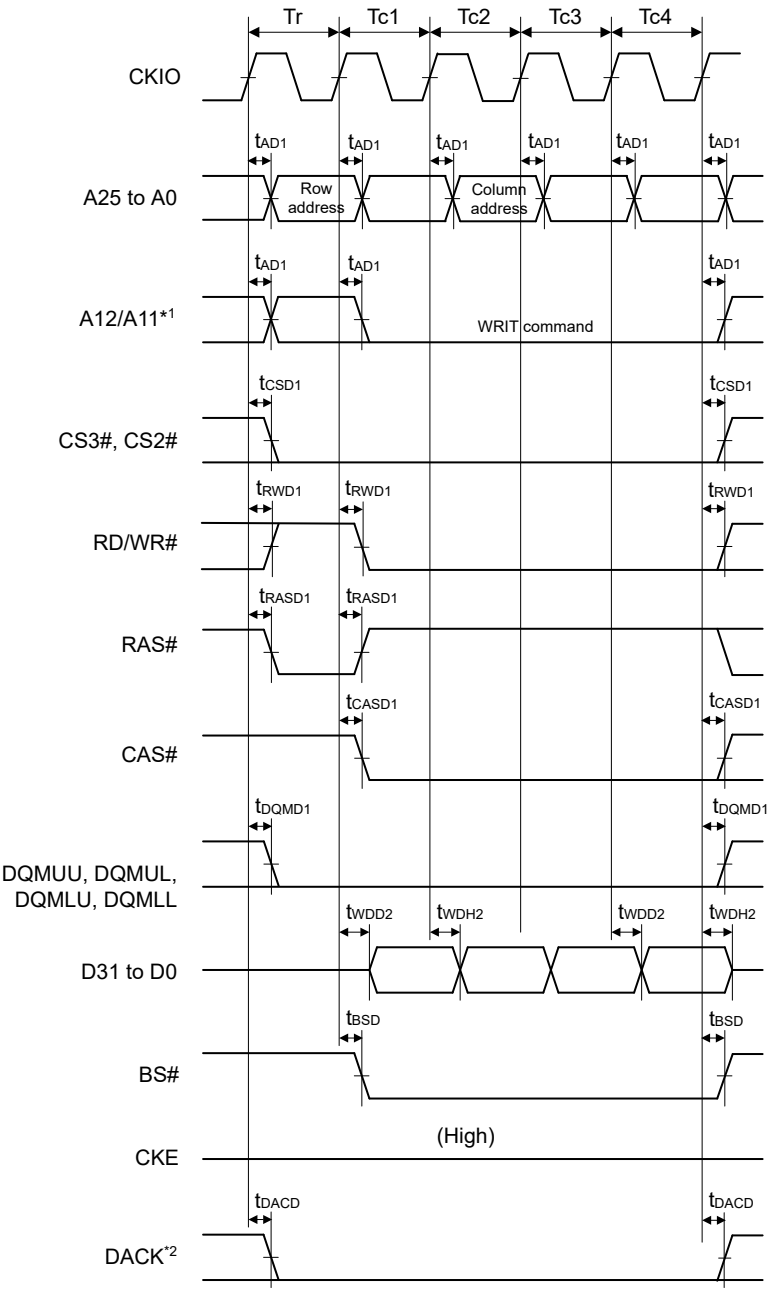
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.28 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (bank active mode: READ command, same row address, CAS latency 2, WTRCD = 0 cycles)



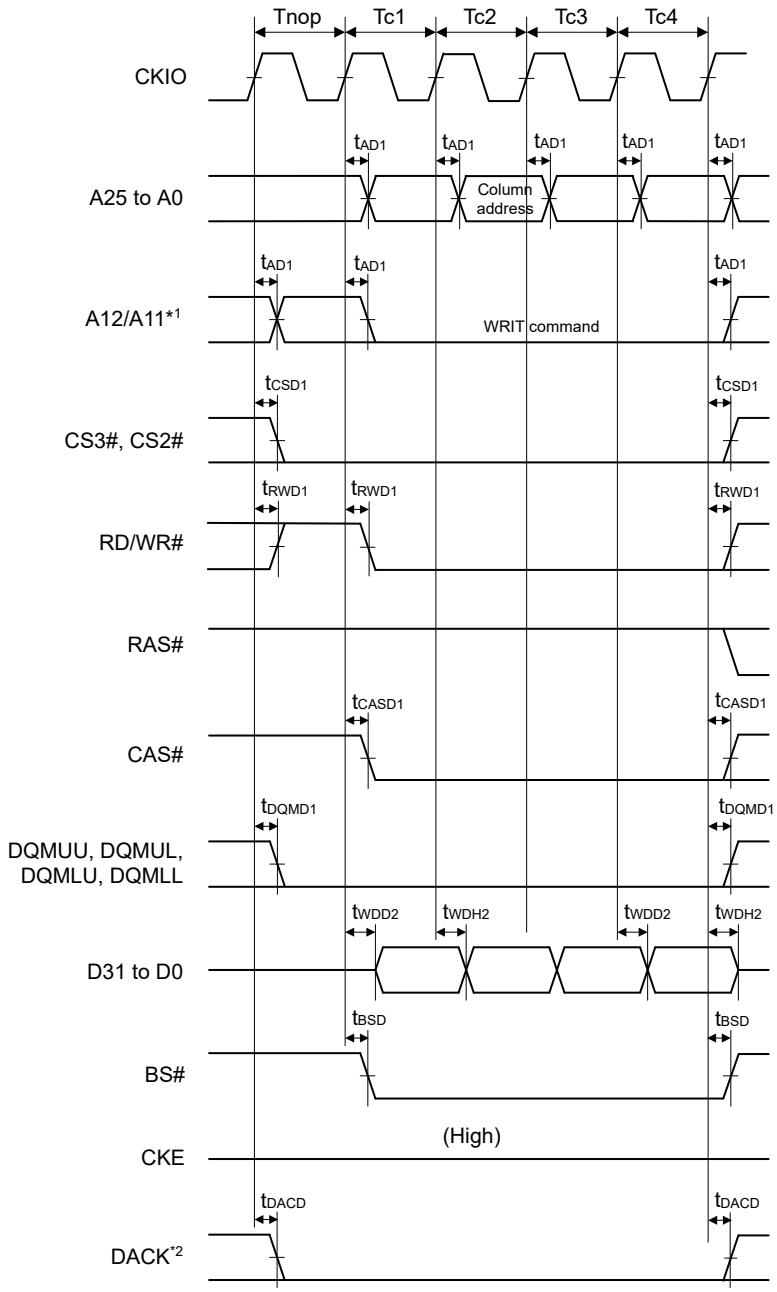
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.29 Synchronous DRAM burst-read bus Cycle (read for 4 cycles) (bank active mode: PRE + ACT + READ command, different row address, CAS latency 2, WTRCD = 0 cycles)



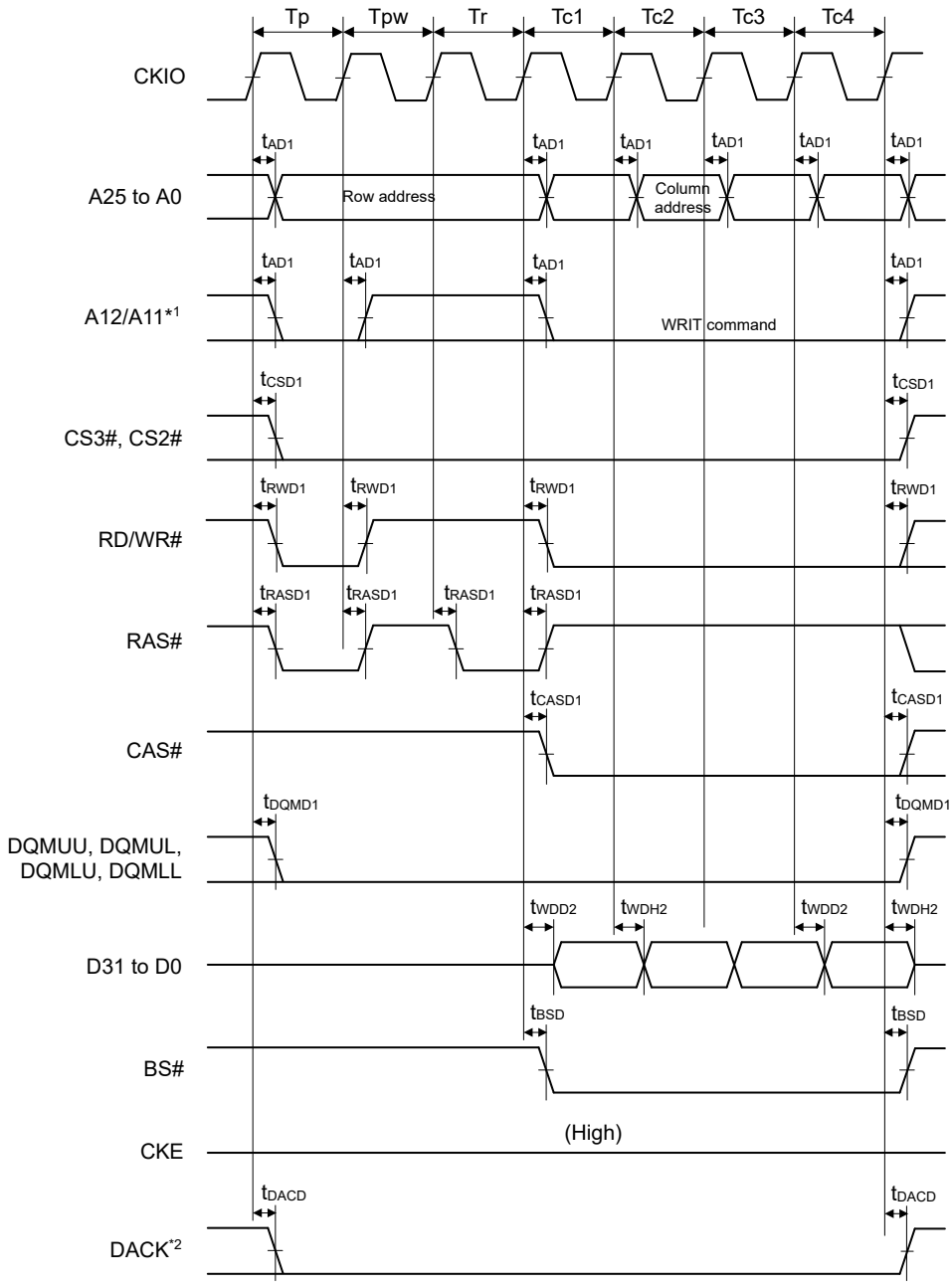
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.30 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (bank active mode: ACT + WRITE command, WTRCD = 0 cycles, TRWL = 0 cycles)



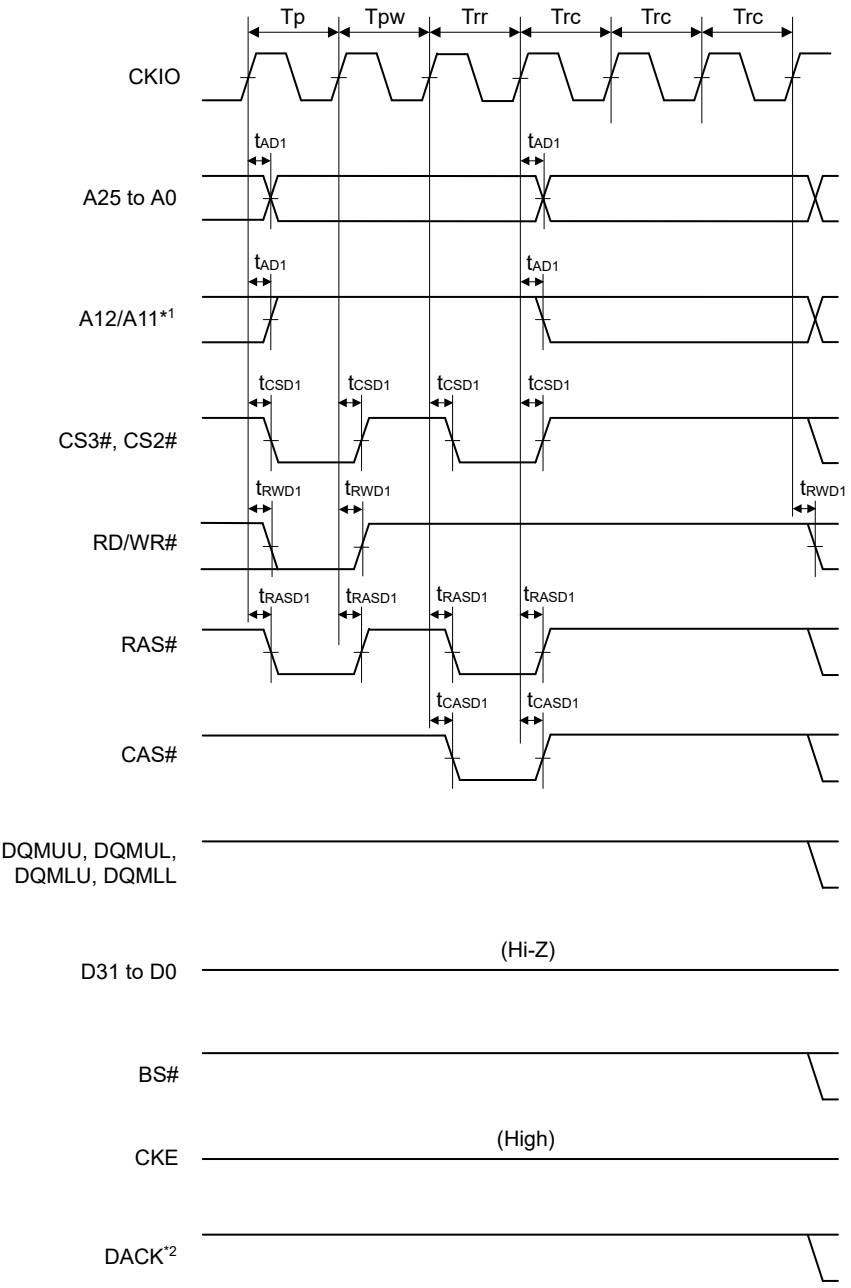
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.31 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (bank active mode: WRITE command, same row address, WTRCD = 0 cycles, TRWL = 0 cycles)



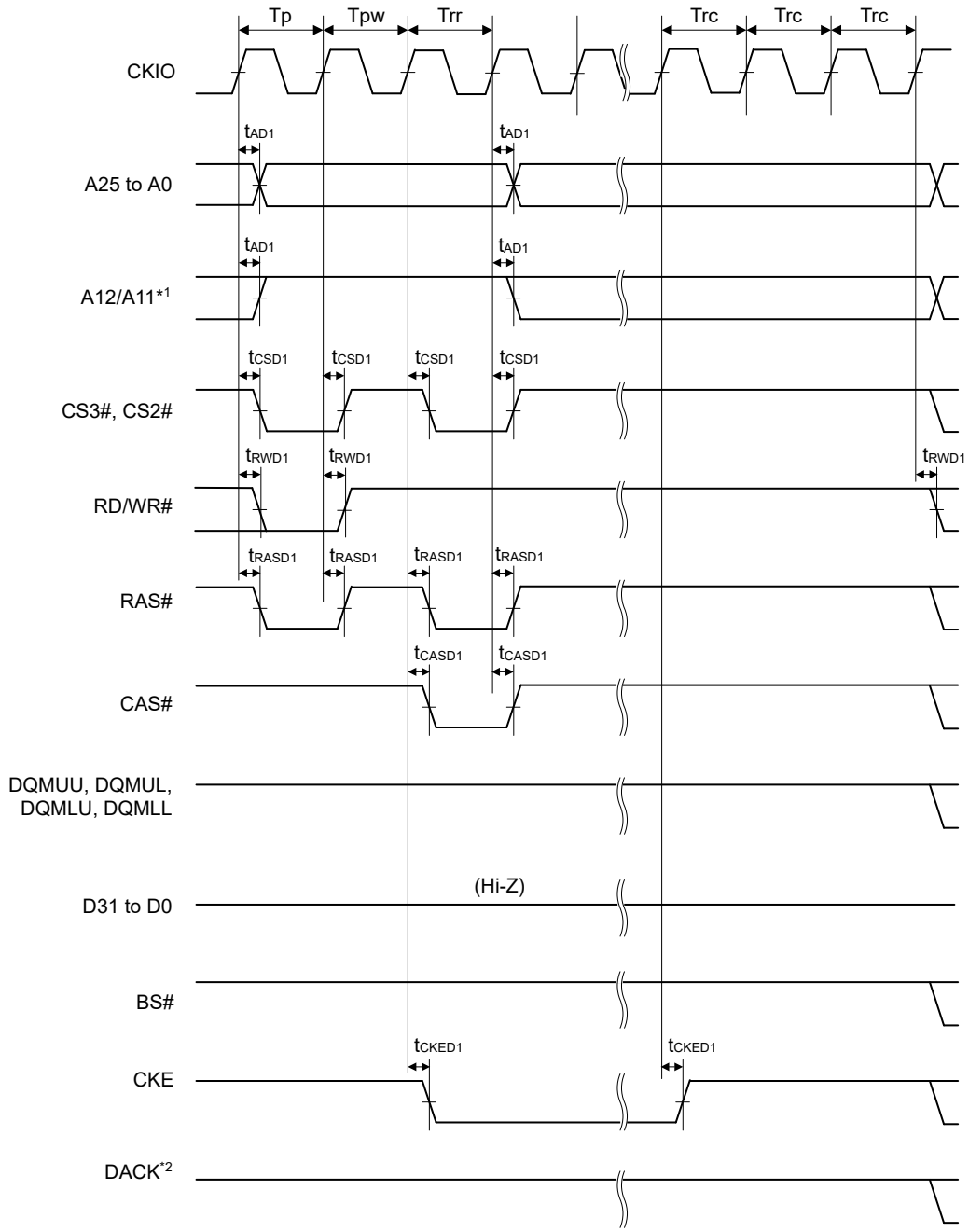
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.32 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (bank active mode: PRE + ACT + WRITE command, different row address, WTRCD = 0 cycles, TRWL = 0 cycles)



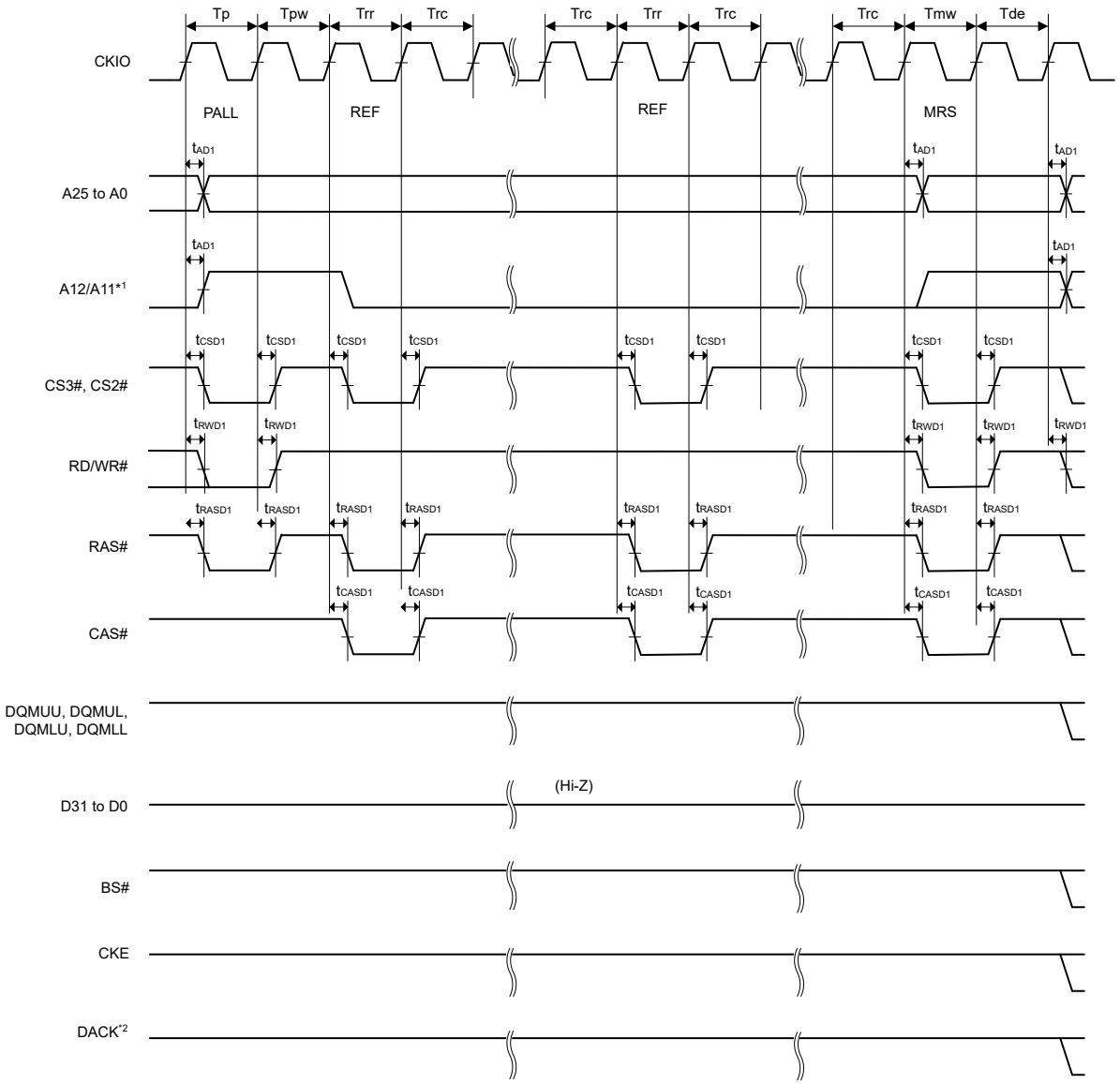
Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.33 Synchronous DRAM auto-refresh timing (WTRP = 1 cycle, WTRC = 3 cycles)



Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.34 Synchronous DRAM self-refresh timing (WTRP = 1 cycle)



Note 1. Address pin to be connected to A10 of SDRAM.
Note 2. DACK is waveform when active-low is specified.

Figure 2.35 Synchronous DRAM mode register set timing (WTRP = 1 cycle)

2.5.4 DMAC Timing

Table 2.23 DMAC timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	t_{PLcyc} × 2	—	ns	Figure 2.36
	DACK and TEND delay time	t_{DACD}	0	10	ns	Figure 2.37

Note 1. t_{PLcyc}: PCLKL cycle

Table 2.24 DMAC timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), $T_j$min = −20°C

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	t_{PLcyc} × 2	—	ns	Figure 2.36
	DACK and TEND delay time	t_{DACD}	-0.5	8	ns	Figure 2.37

Note 1. t_{PLcyc}: PCLKL cycle

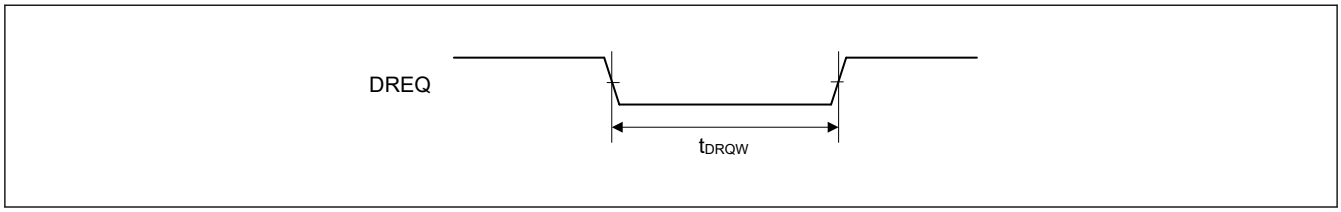


Figure 2.36 DREQ input timing

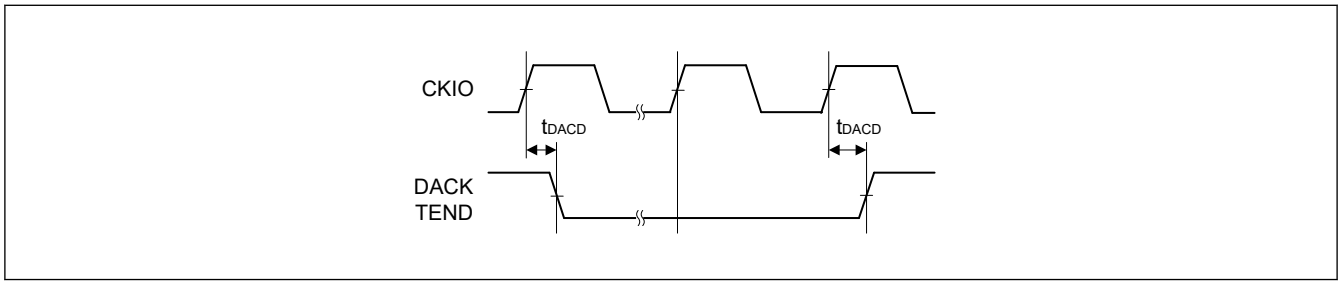


Figure 2.37 DACK and TEND output timing

2.5.5 On-Chip Peripheral Module Timing

2.5.5.1 I/O Port Timing

Table 2.25 I/O port timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PLcyc}	Figure 2.38

Note 1. t_{PLcyc}: PCLKL cycle

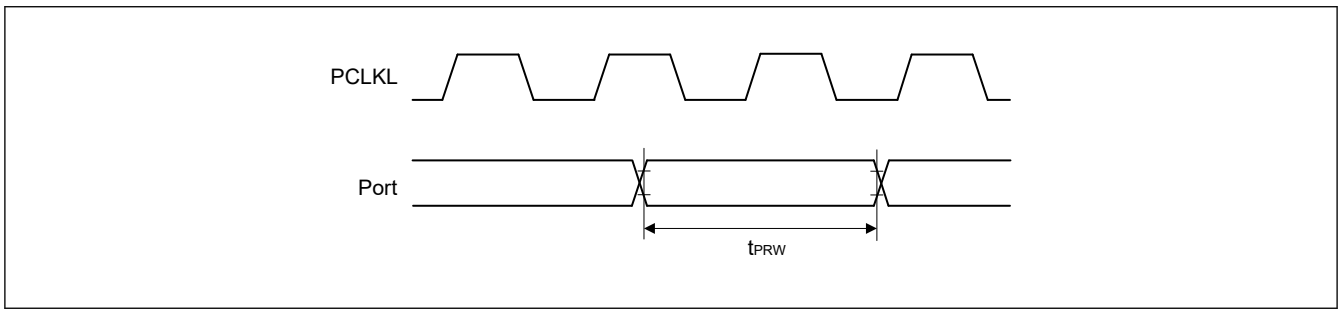


Figure 2.38 I/O port input timing

2.5.5.2 CMTW Timing

Table 2.26 CMTW timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PLcyc}	Figure 2.39
		Both-edge setting		2.5	—		

Note 1. t_{PLcyc}: PCLKL cycle

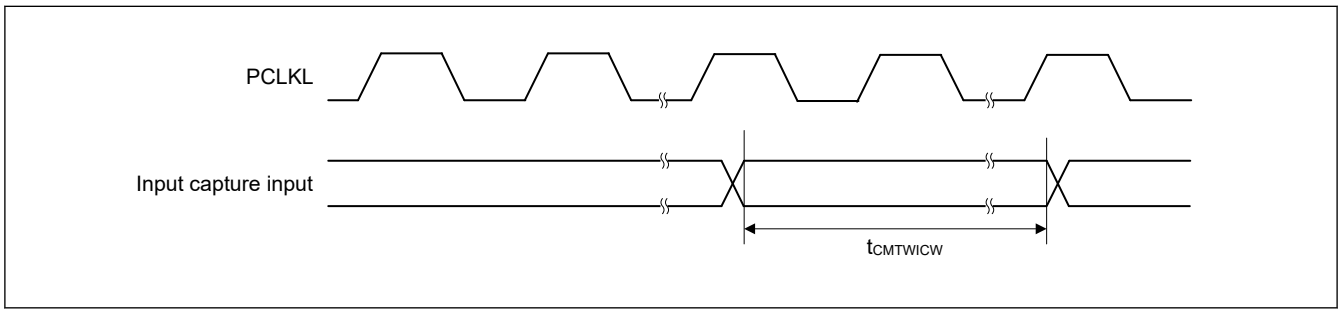


Figure 2.39 CMTW input capture input timing

2.5.5.3 MTU3 Timing

Table 2.27 MTU3 timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	2.5	—	t_{PHcyc}	Figure 2.40
		Both-edge setting		3.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	2.5	—	t_{PHcyc}	Figure 2.41
		Both-edge setting		3.5	—		
		Phase counting mode		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle

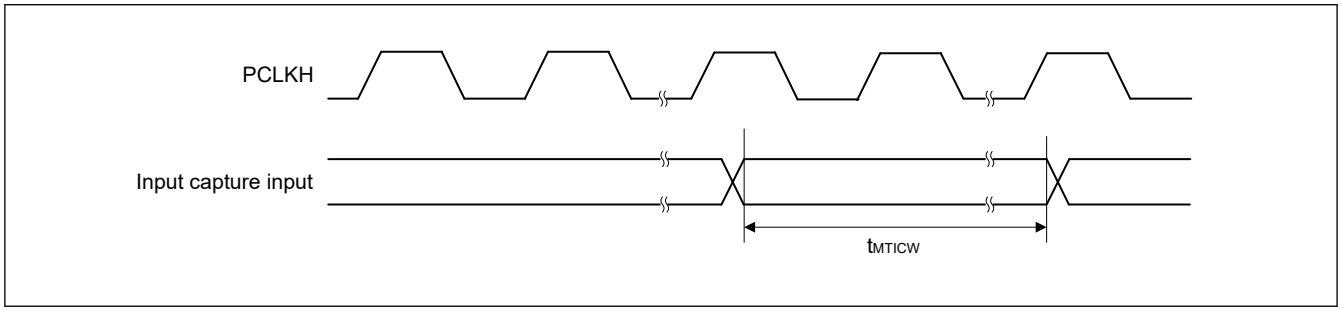


Figure 2.40 MTU3 input capture input timing

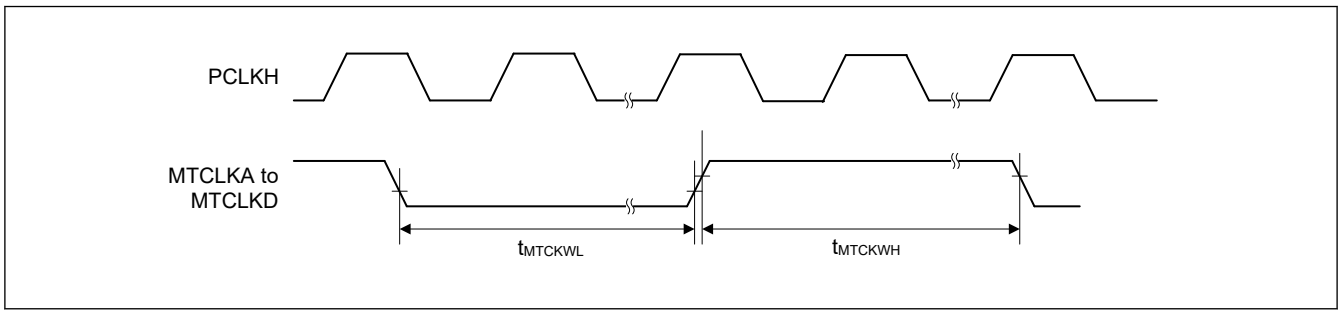


Figure 2.41 MTU3 clock input timing

2.5.5.4 POE3 Timing

Table 2.28 POE3 timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
POE3	POEn# input pulse width		t_{POEW}	2.5	—	t_{PHcyc}	Figure 2.42
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	5 × PCLKH + 0.1	µs	Figure 2.43
		Simultaneous conduction of output pins	t_{POEDO}	—	3 × PCLKH + 0.1	µs	Figure 2.44
		Register setting	t_{POEDS}	—	PCLKH + 0.1	µs	Figure 2.45
		Oscillation stop detection	t_{POEDOS}	—	74	µs	Figure 2.46

Note 1. t_{PHcyc}: PCLKH cycle

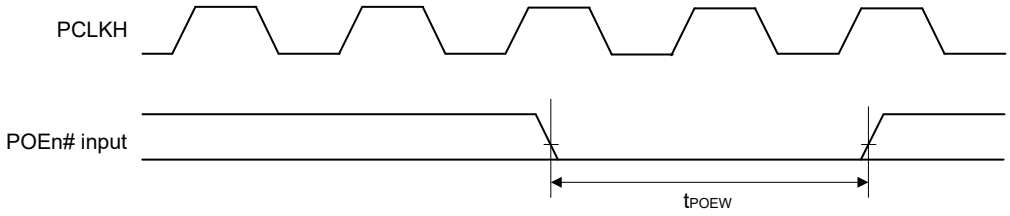


Figure 2.42 POEn# input pulse timing

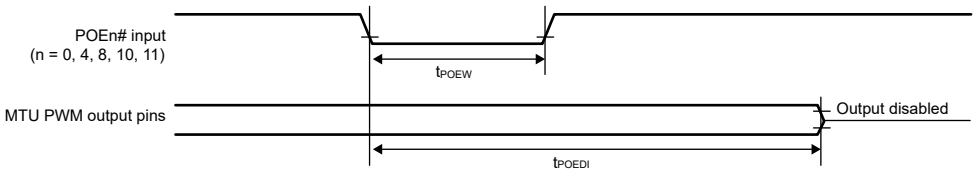
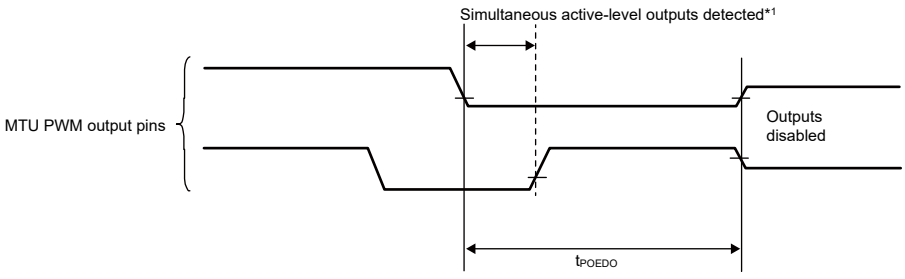


Figure 2.43 Output disable time for POE in response to transition of the POEn# signal level



Note 1. When the active level is set to low.

Figure 2.44 Output disable time for POE in response to the simultaneous conduction of output pins

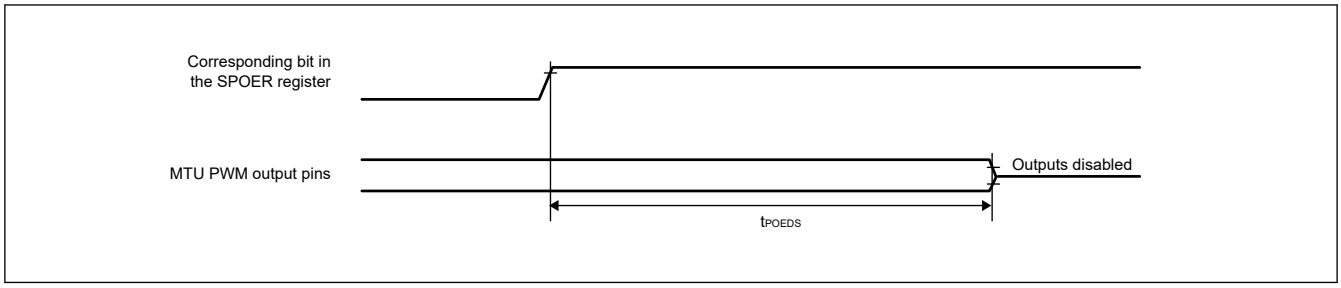


Figure 2.45 Output disable time for POE in response to the register setting

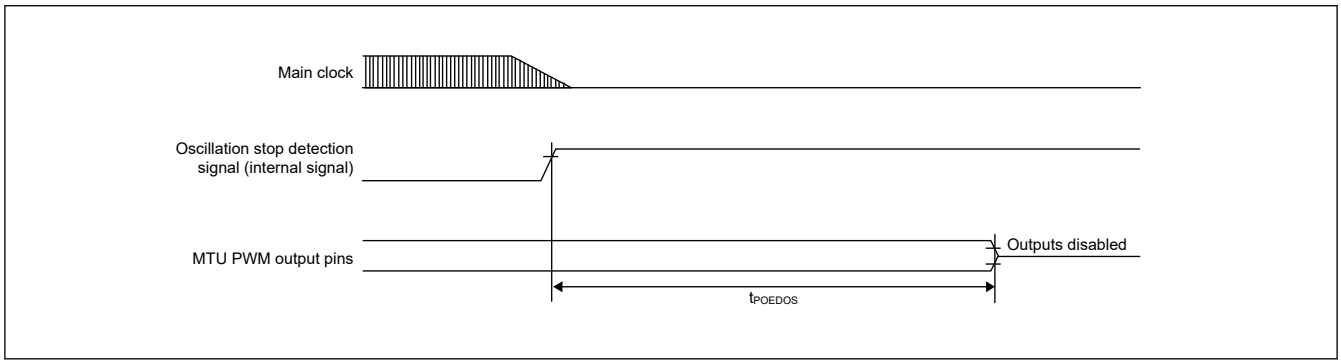


Figure 2.46 Output disable time for POE in response to the oscillation stop detection

2.5.5.5 GPT Timing

Table 2.29 GPT timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	2.5	—	t_{PHcyc}	Figure 2.47
		Both-edge setting		3.5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	2.5	—	t_{PHcyc}	Figure 2.48
		Both-edge setting		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKM cycle (Other channels)

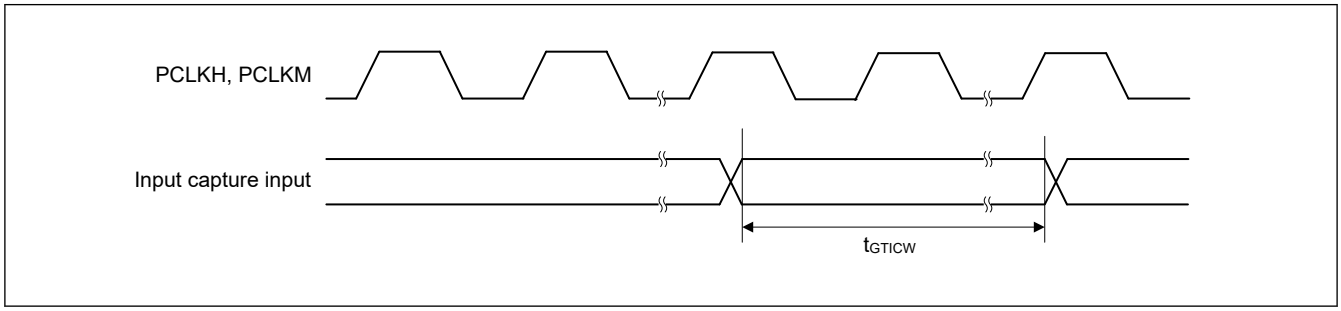


Figure 2.47 GPT input capture input timing

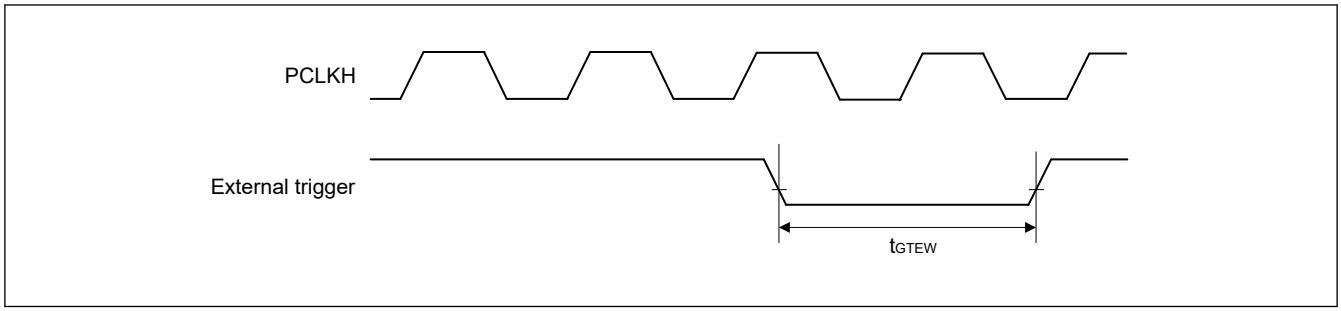


Figure 2.48 GPT external trigger input timing

2.5.5.6 POEG Timing

Table 2.30 POEG timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	2.5	—	t_{PHcyc}	Figure 2.49
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	3 × PCLKH + 0.1	µs	Figure 2.50
		Detection of the output stopping signal from GPT (dead time error, simultaneous high output, or simultaneous low output)	t_{POEGDO}	—	0.1	µs	Figure 2.51
		Register setting	t_{POEGDS}	—	PCLKH + 0.1	µs	Figure 2.52
		Oscillation stop detection	$t_{POEGDOS}$	—	74	µs	Figure 2.53

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKL cycle (Other channels)

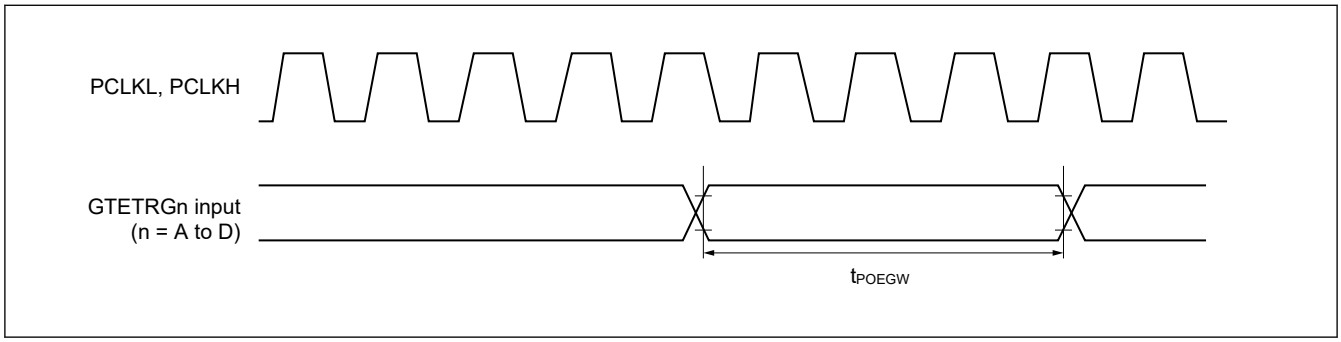


Figure 2.49 POEG input timing

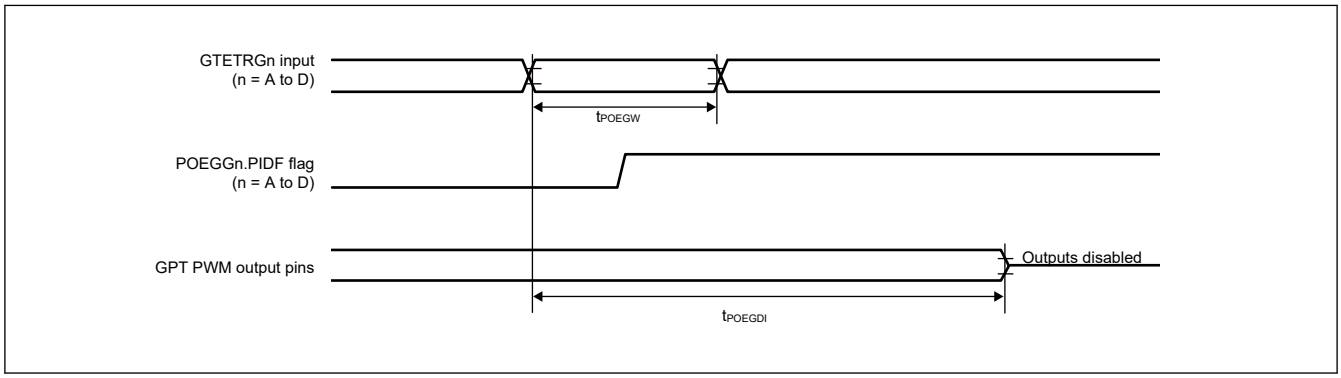
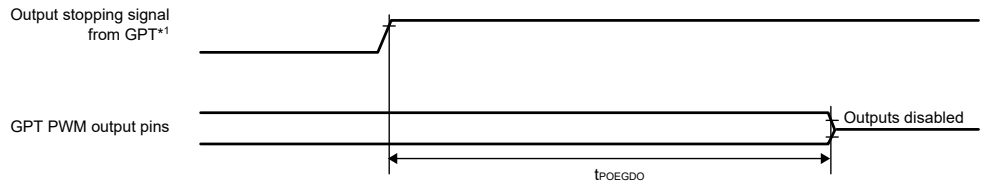


Figure 2.50 Output disable time for POEG via detection flag in response to the input level detection of the GTETRGn pin



Note 1. GPTn.GTST.DTEF (dead time error flag), GPTn.GTST.OABLF (simultaneous low out flag), or GPTn.GTST.OABHF (simultaneous high output flag)

Figure 2.51 Output disable time for POEG in response to detection of the output stopping signal from GPT

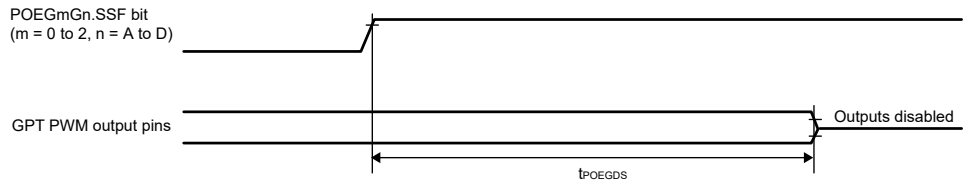


Figure 2.52 Output disable time for POEG in response to the register setting

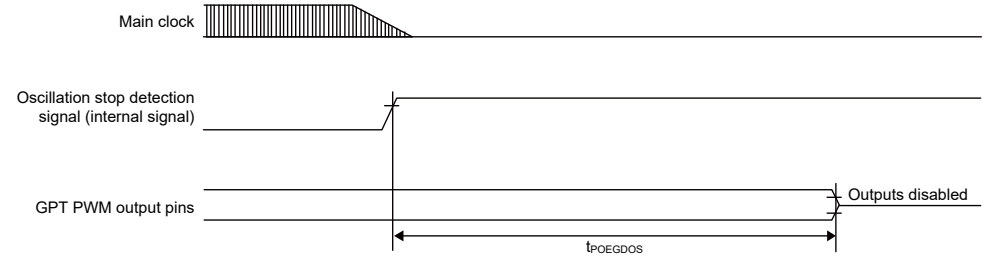


Figure 2.53 Output disable time for POEG in response to the oscillation stop detection

2.5.5.7 A/D Converter Trigger Timing

Table 2.31 A/D converter trigger timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
A/D converter	A/D converter trigger input pulse width	ADTRG0#, ADTRG1#	t_{TRGW}	1.5	—	$t_{PADCcyc}$	Figure 2.54

Note 1. $t_{PADCcyc}$: PCLKADC cycle

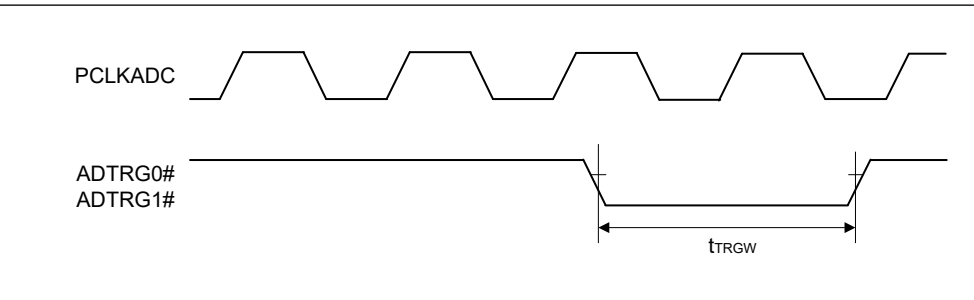


Figure 2.54 A/D converter trigger input timing (ADTRG0#, ADTRG1#)

2.5.5.8 SCI Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (except Simple I2C)

Table 2.32 SCI timing (1 of 2)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
SCI (Asynchronous)	Input clock cycle	t_{Scyc}	4	—	$t_{PSCIcyc}$	Figure 2.55
	Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time	t_{SCKr}	—	3	ns	
	Input clock fall time	t_{SCKf}	—	3	ns	
	Output clock cycle	t_{Scyc}	6	—	$t_{PSCIcyc}$	
	Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	t_{SCKr}	—	3	ns	
	Output clock fall time	t_{SCKf}	—	3	ns	
SCI (Simple I2C, Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.56
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$2 \times NF_{cyc}$ *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
SCI (Simple I2C, Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.56
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$2 \times NF_{cyc}$ *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 2.32 SCI timing (2 of 2)

Parameter			Symbol	Min.	Max.	Unit	Reference figure
SCI (Clock sync, Simple SPI)	SCK output clock cycle (master)		t_{SPcyc}	2	65536	$t_{PSCIcyc}$	Figure 2.57 to Figure 2.62
	SCK input clock cycle (slave)			2	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKR}, t_{SPCKF}	—	3	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		3	—		
	Data input hold time	Internal clock	t_H	3	—	ns	
		External clock		3	—		
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	12		
	Data output hold time	Internal clock	t_{OH}	0	—	ns	
		External clock		0	—		
	Data rise/fall time		t_{DR}, t_{DF}	—	3	ns	
	Slave access time	Internal clock	t_{SA}	—	$3 \times t_{PSCIcyc} + 12$	ns	
		External clock		—	$3 \times t_{PSCIcyc} + 12$		
	Slave output release time	Internal clock	t_{REL}	—	$3 \times t_{PSCIcyc} + 12$	ns	
		External clock		—	$3 \times t_{PSCIcyc} + 12$		
SCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}, t_{SSF}	—	3	ns	

Note: $t_{PSCIcyc}$: PCLKSCIn cycle

Note 1. $N_{Fcyc} = 4^n \times 2^{m-1} \times t_{PSCIcyc}$
n: CCR2.CKS[1:0] (n = 0, 1, 2, 3)
m: CCR1.NFCS[2:0] (m = 1, 2, 3, 4)

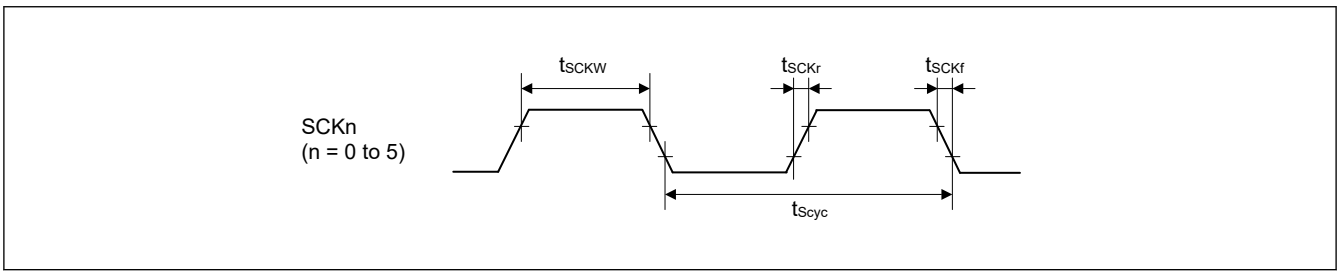
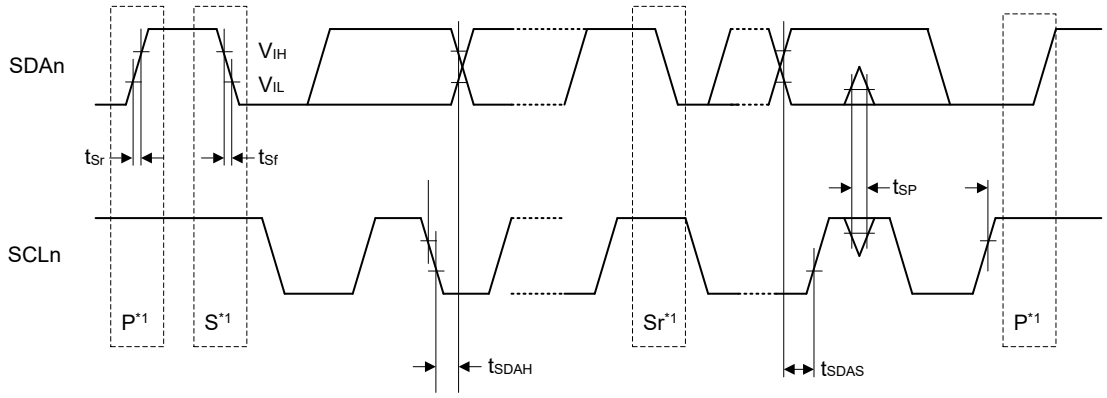


Figure 2.55 SCK clock input/output timing



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.56 SCI simple I2C mode timing

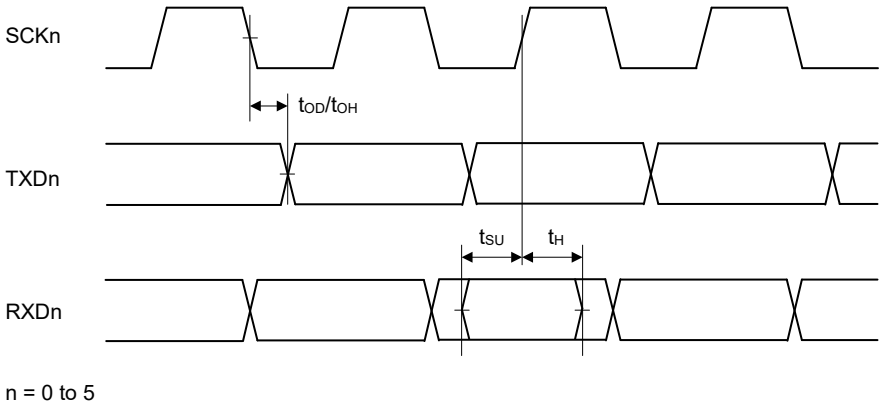
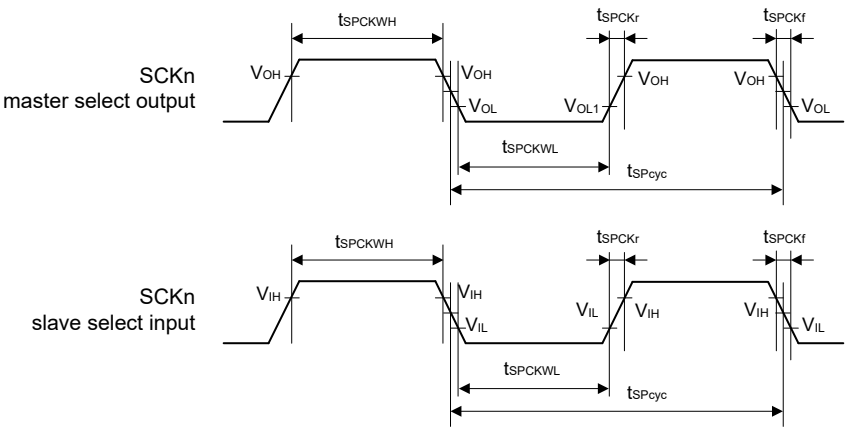


Figure 2.57 SCI input/output timing in clock synchronous mode



$V_{OH} = 0.7 \times VCC33$, $V_{OL} = 0.3 \times VCC33$, $V_{IH} = 0.7 \times VCC33$, $V_{IL} = 0.3 \times VCC33$

Figure 2.58 SCI simple SPI mode clock timing

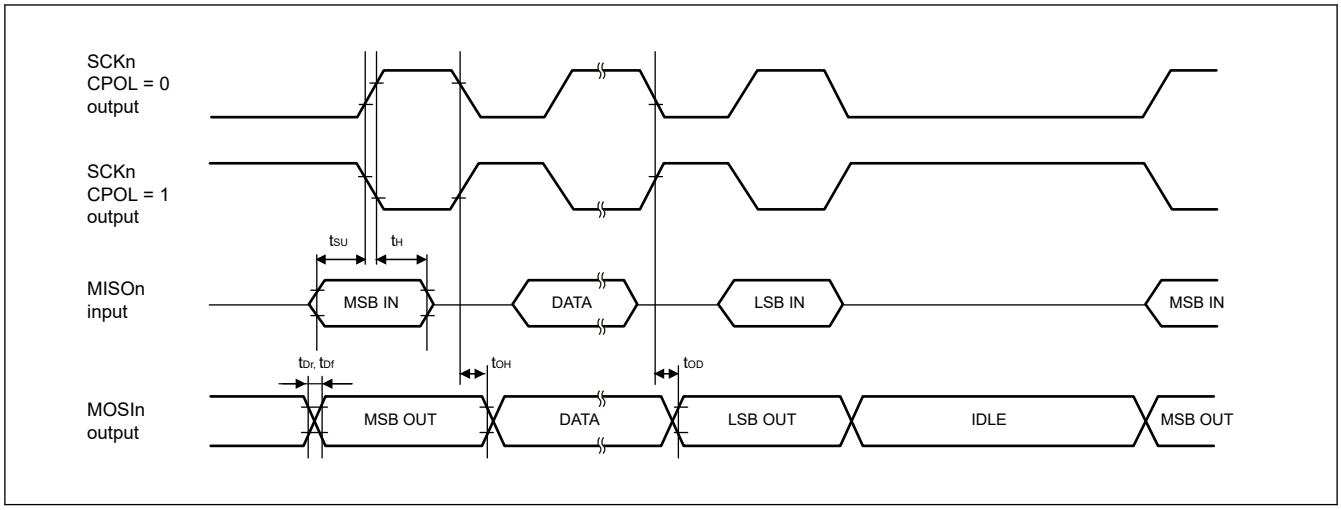


Figure 2.59 SCI simple SPI mode timing for master when CPHA = 0

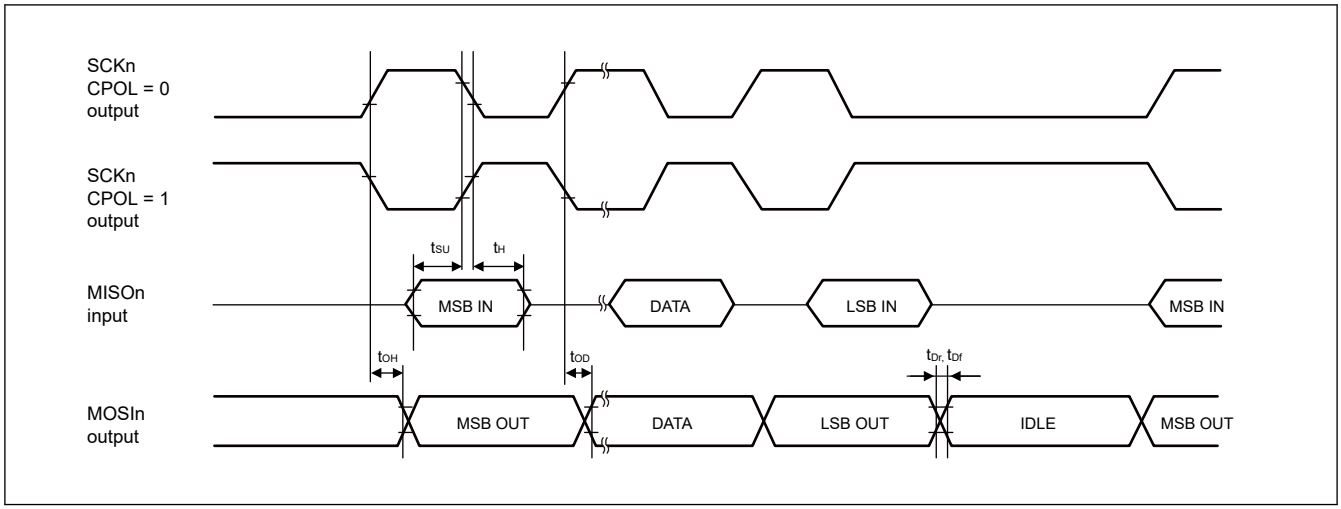


Figure 2.60 SCI simple SPI mode timing for master when CPHA = 1

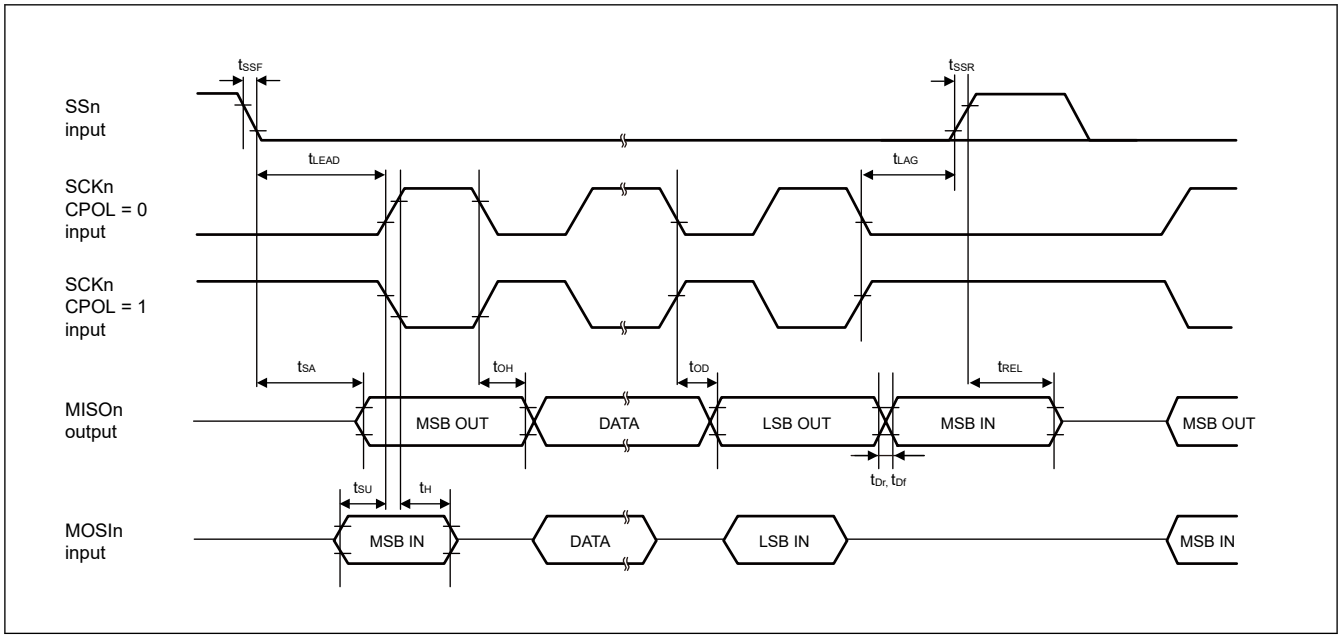


Figure 2.61 SCI simple SPI mode timing for slave when CPHA = 0

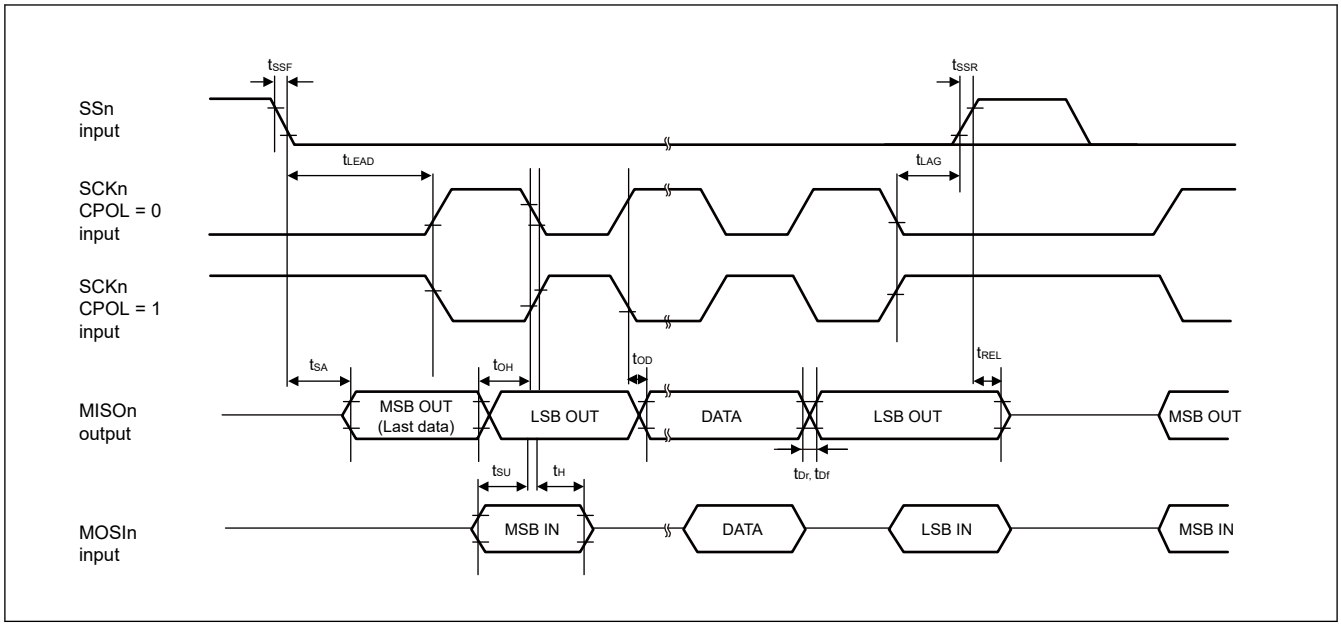


Figure 2.62 SCI simple SPI mode timing for slave when CPHA = 1

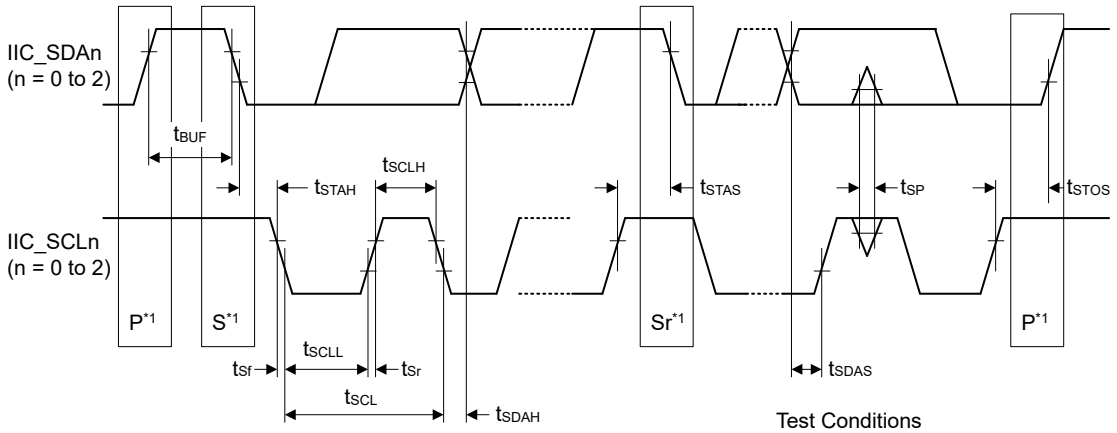
2.5.5.9 IIC Timing

Conditions: V_{OL} = 0.4 V, I_{OL} = 4 mA

Table 2.33 IIC timing

Parameter		Symbol	Min.*1 *2	Max.*1 *2	Unit	Reference figure
IIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.63
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc}: IIC internal reference clock (IICΦ) cycle
Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.
Note 4. The minimum values are not specified for t_{sr} and t_{sf} in Fast-mode.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.63 IIC bus interface input/output timing

2.5.5.10 CANFD Timing

Table 2.34 CANFD timing

Parameter		Symbol	CAN		CANFD		Unit	Reference figure
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}	—	100	—	50	ns	Figure 2.64
	Transmission rate	—	—	1	—	8	Mbps	

Note: Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

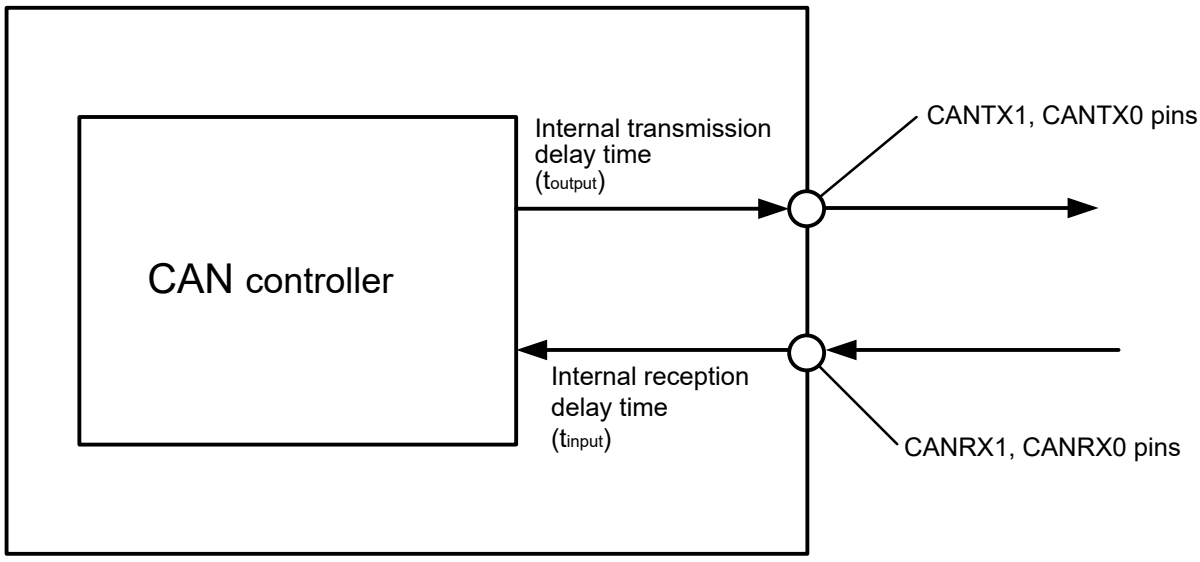


Figure 2.64 CAN interface condition

2.5.5.11 SPI Timing

Table 2.35 SPI timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF

Parameter		Symbol	Min.*1	Max.*1	Unit*1	Reference figure
RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{SPIcyc}	Figure 2.65
	Slave		2	4096		
RSPCK clock high level pulse width	Master	t_{SPCKWH}	(t_{SPcyc} − t_{SPCKr} − t_{SPCKf}) / 2 − 2.5	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock low level pulse width	Master	t_{SPCKWL}	(t_{SPcyc} − t_{SPCKr} − t_{SPCKf}) / 2 − 2.5	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock rising/falling time	Output	t_{SPCKr}, t_{SPCKf}	—	3	ns	
	Input		—	1	ns	
Data input setup time	Master	t_{SU}	5	—	ns	Figure 2.66 to Figure 2.72
	Slave		3	—		
Data input hold time	Master	t_H	3	—	ns	
	Slave		3	—		
SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} − 3*2	N × t_{SPcyc} + 3*2	ns	Figure 2.66 to Figure 2.69
	Slave		4	—	t_{SPIcyc}	
SSL hold time	Master	t_{LAG}	N × t_{SPcyc} − 3*3	N × t_{SPcyc} + 3*3	ns	
	Slave		4	—	t_{SPIcyc}	
Continuous transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{SPIcyc}	8 × t_{SPcyc} + 2 × t_{SPIcyc}	ns	
	Slave		t_{SPcyc} + 5 × t_{SPIcyc}	—		
TI-SSP SS input setup time		t_{TISS}	3	—	ns	Figure 2.70 to Figure 2.72
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M*4	—	t_{SPIcyc}	
TI-SSP Master SS output delay		t_{TISSOD}	-3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	12	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	8	ns	
Data output delay time	Master	t_{OD}	—	3	ns	Figure 2.66 to Figure 2.72
	Slave		—	12	ns	
Data output hold time	Master	t_{OH}	-3	—	ns	
	Slave		3	—		
MOSI, MISO rising/falling time	Output	t_{Dr}, t_{Df}	—	3	ns	
	Input		—	1	µs	
SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	3	ns	Figure 2.66, Figure 2.67
	Input		—	1	µs	

Table 2.35 SPI timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF

Parameter	Symbol	Min.*1	Max.*1	Unit*1	Reference figure
Slave access time	t_{SA}	—	12	ns	Figure 2.68, Figure 2.69
Slave output release time	t_{REL}	—	12	ns	

Note 1. t_{SPIcyc}: PCLKSPIn cycle
Note 2. SPCKD set value + 1 (1 to 8)
Note 3. SSLND set value + 1 (1 to 8)
Note 4. SSLND set value + 2 (2 to 9)

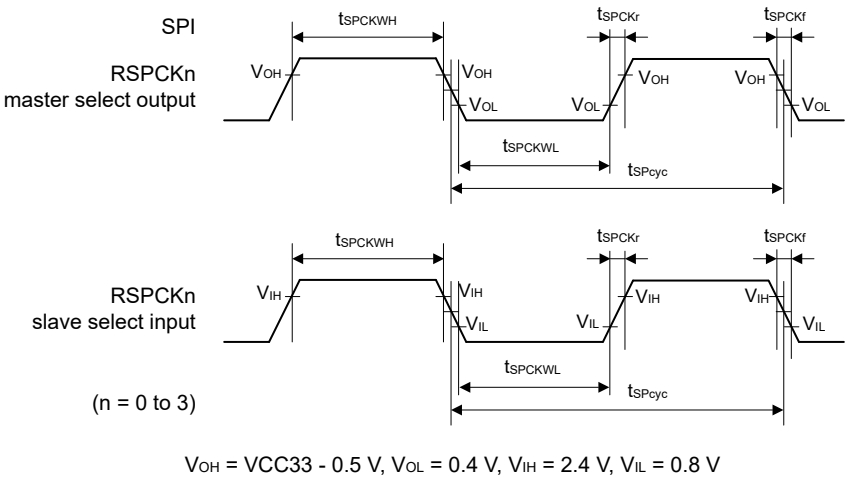


Figure 2.65 SPI clock timing

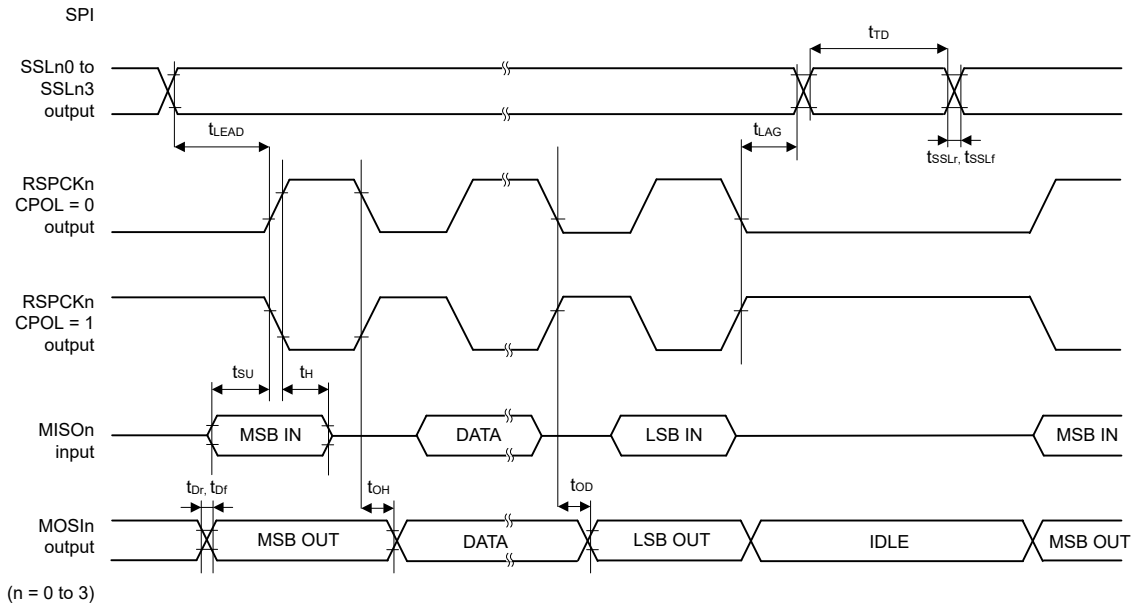


Figure 2.66 SPI timing (Master, Motorola SPI, CPHA = 0)

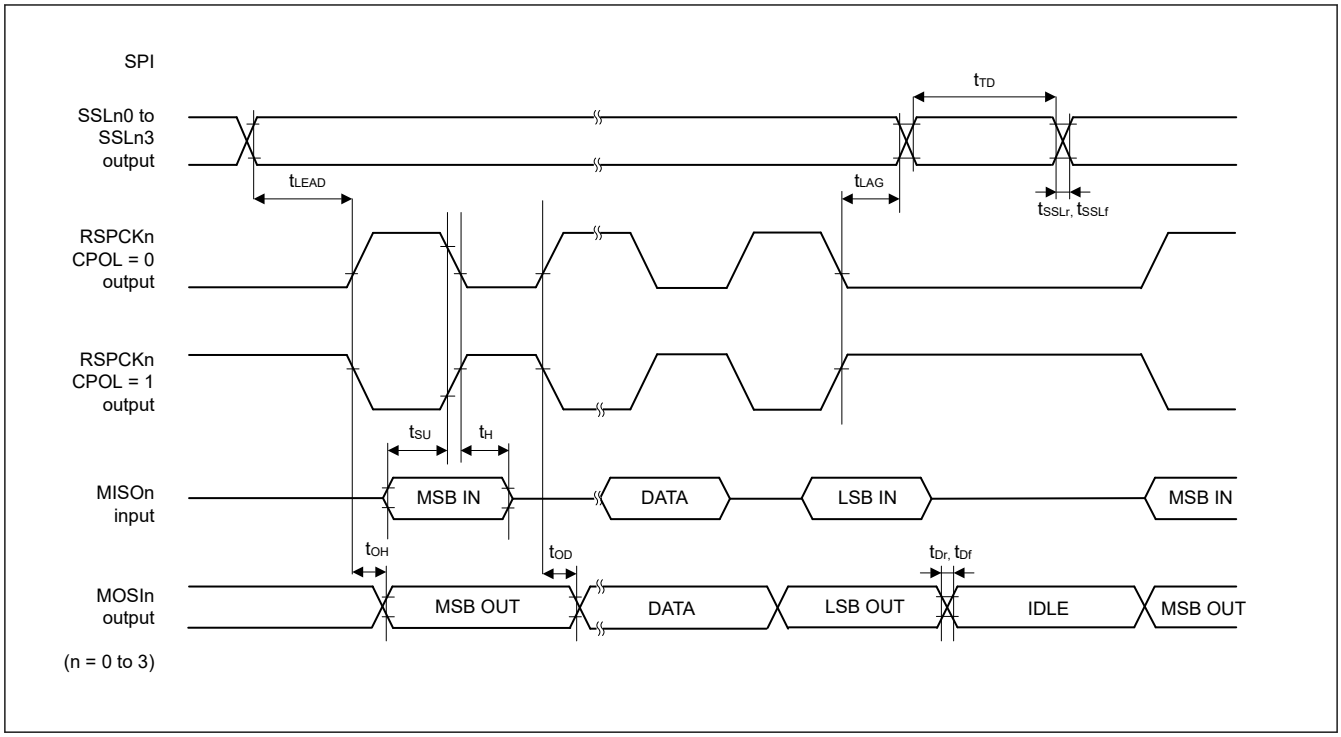


Figure 2.67 SPI timing (Master, Motorola SPI, CPHA = 1)

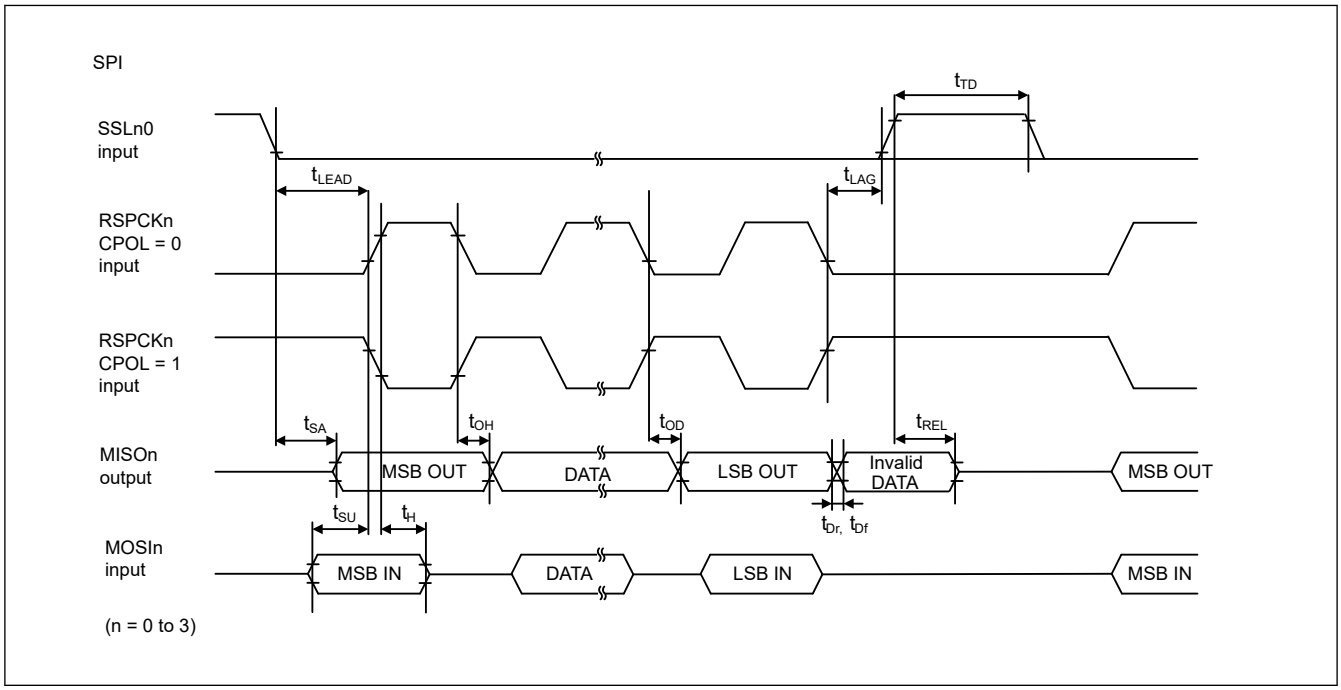


Figure 2.68 SPI timing (Slave, Motorola SPI, CPHA = 0)

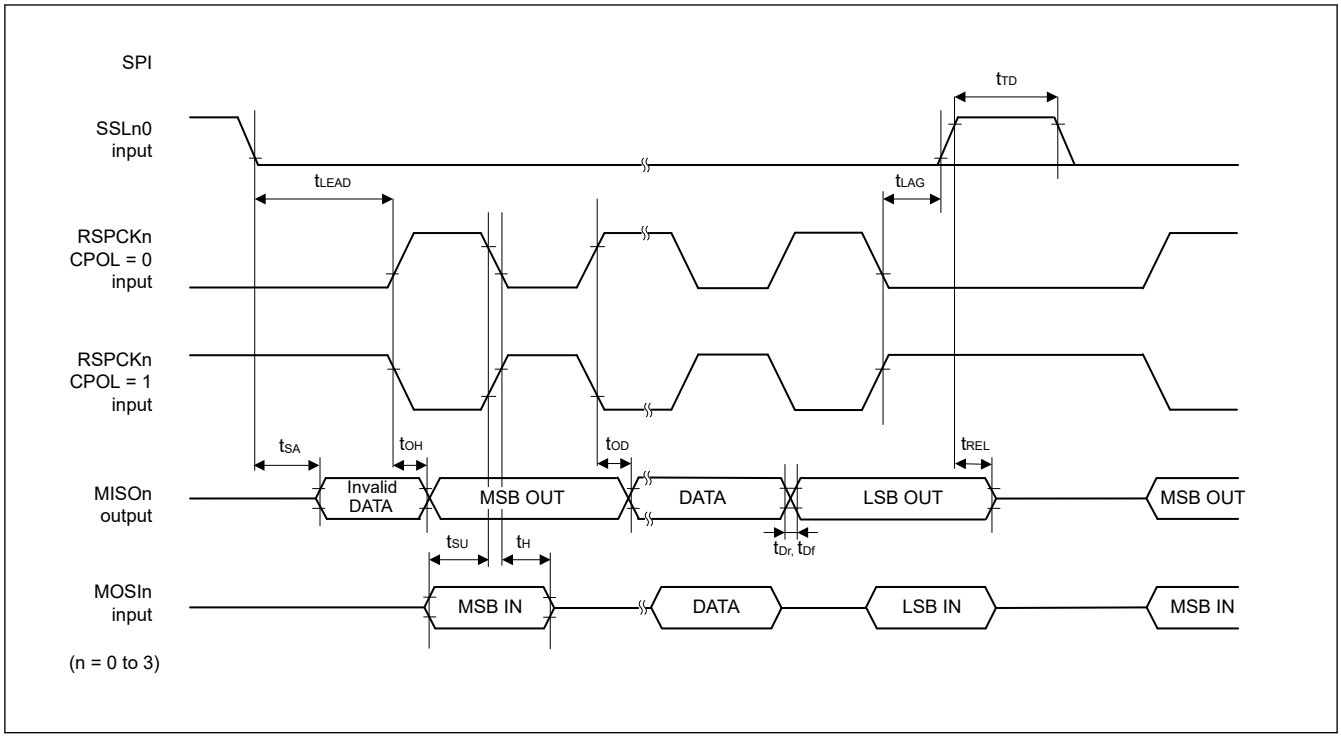


Figure 2.69 SPI timing (Slave, Motorola SPI, CPHA = 1)

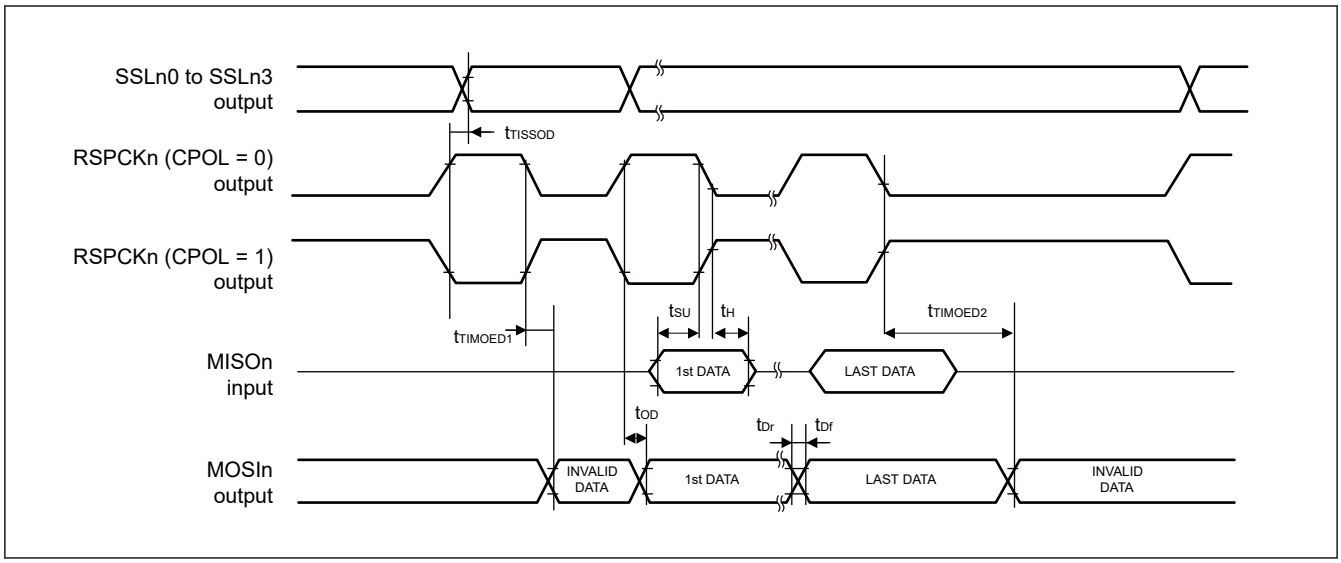


Figure 2.70 SPI timing (Master, TI SSP)

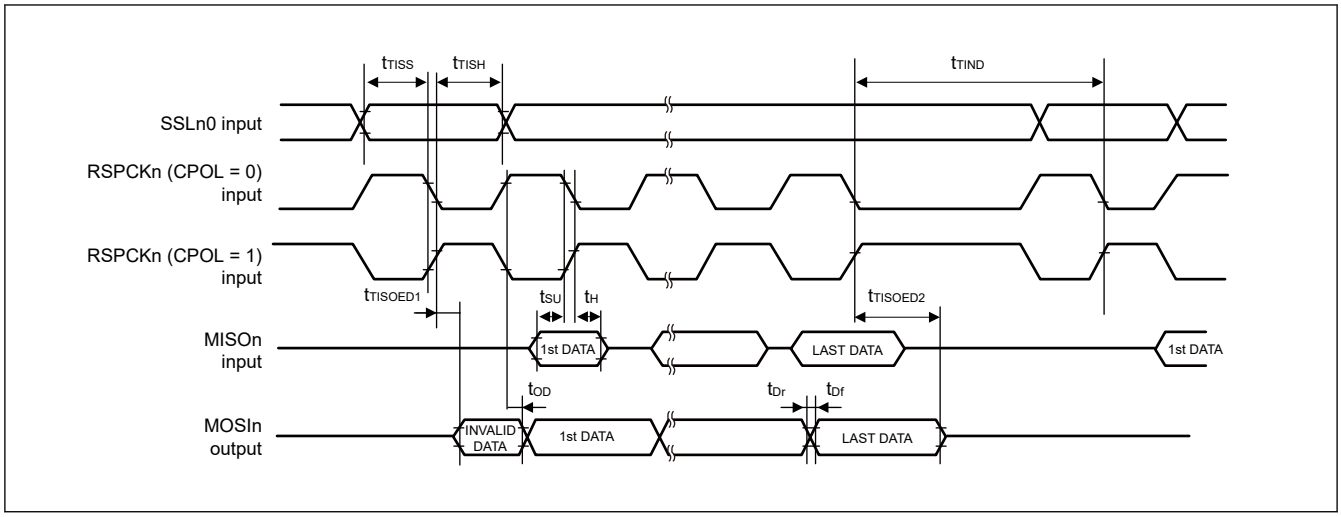


Figure 2.71 SPI timing (Slave, TI-SSP, with delay in burst transfer)

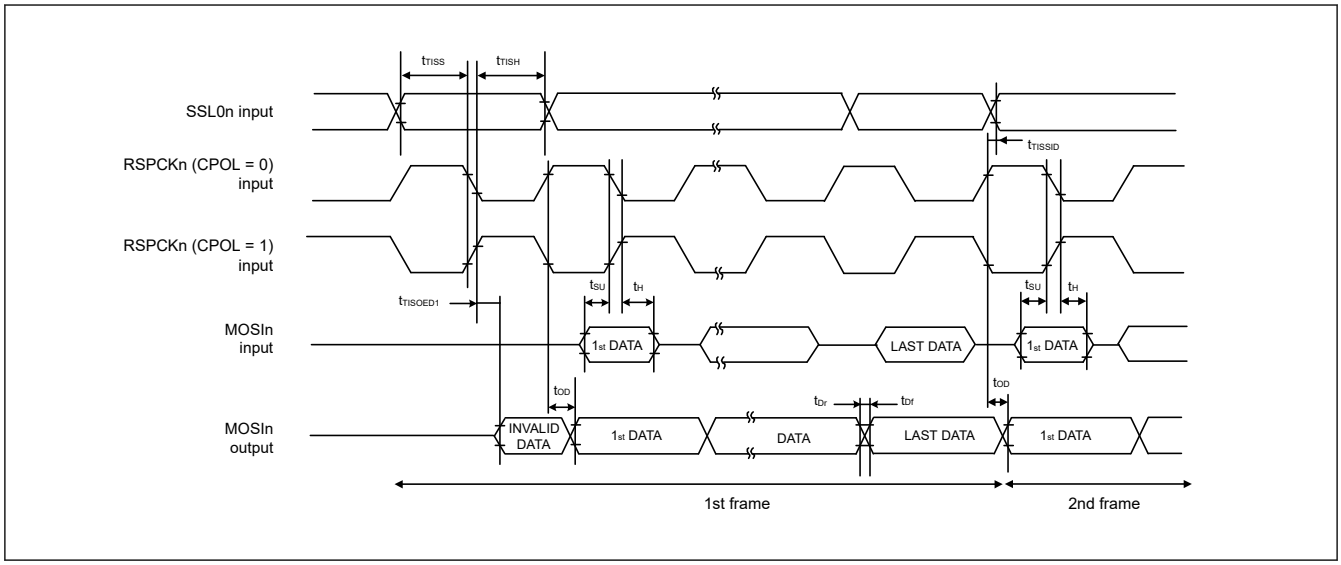


Figure 2.72 SPI timing (Slave, TI-SSP, without delay in burst transfer)

2.5.5.12 xSPI Timing

Conditions:

Single end Clock

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 15 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (3.3 V)

Data

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 15 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (3.3 V)

Table 2.36 xSPI timing

Parameter		Symbol	1.8 V		3.3 V		Unit	Reference figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t_{PERIOD}	7.5	—	13.3	—	ns	Figure 2.73
	DDR		10.0	—	13.3	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*2	—	0.56	—	V/ns	
Clock Duty cycle distortion		t_{CKDCD}	0.0	t_{PERIOD} × 0.05	0.0	t_{PERIOD} × 0.05	ns	
Clock Minimum Pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	0.4 × VCC18	0.6 × VCC18	—	—	V	
DS Duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS Minimum Pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	0.56	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.4	—	ns	Figure 2.74
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.0*3	—	1.4*3	ns	
Data output hold time		t_{OH}	-1.0	—	-2.3	—	ns	
Data output buffer off time		t_{BOFF}	-1.0	—	-2.3	—	ns	
Data input setup time (to DS)	DDR*1 *3	t_{SU}	-0.8	—	-0.8	—	ns	Figure 2.75, Figure 2.76
Data input hold time (to DS)		t_{H}	t_{PERIOD} × 0.41 - 0.8	—	t_{PERIOD} × 0.41 - 0.8	—	ns	
Data output setup time (to CK)		t_{SUO}	1.0	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	1.0	—	1.0	—	ns	
CS Low to Clock High		t_{CSLCKH}	6.0/8.0*2 *4	—	8.0*4	—	ns	Figure 2.74 to Figure 2.76
Clock Low to CS High		t_{CKLCSH}	6.0/8.0*2	—	8.0	—	ns	
CS High time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS Low to CS High		t_{DSLCSH}	6.0/8.0*2	—	10.6	—	ns	Figure 2.77
CS High to DS Tri-State		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS Low to DS Low		t_{CSLDSL}	0.0	—	0.0	—	ns	
DS Tri-State to CS Low		t_{DSTCSL}	0.0	—	0.0	—	ns	

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 01000b for xSPI200.
Note 2. Specification at 133 MHz / Specification at 100 MHz
Note 3. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1).
Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1).

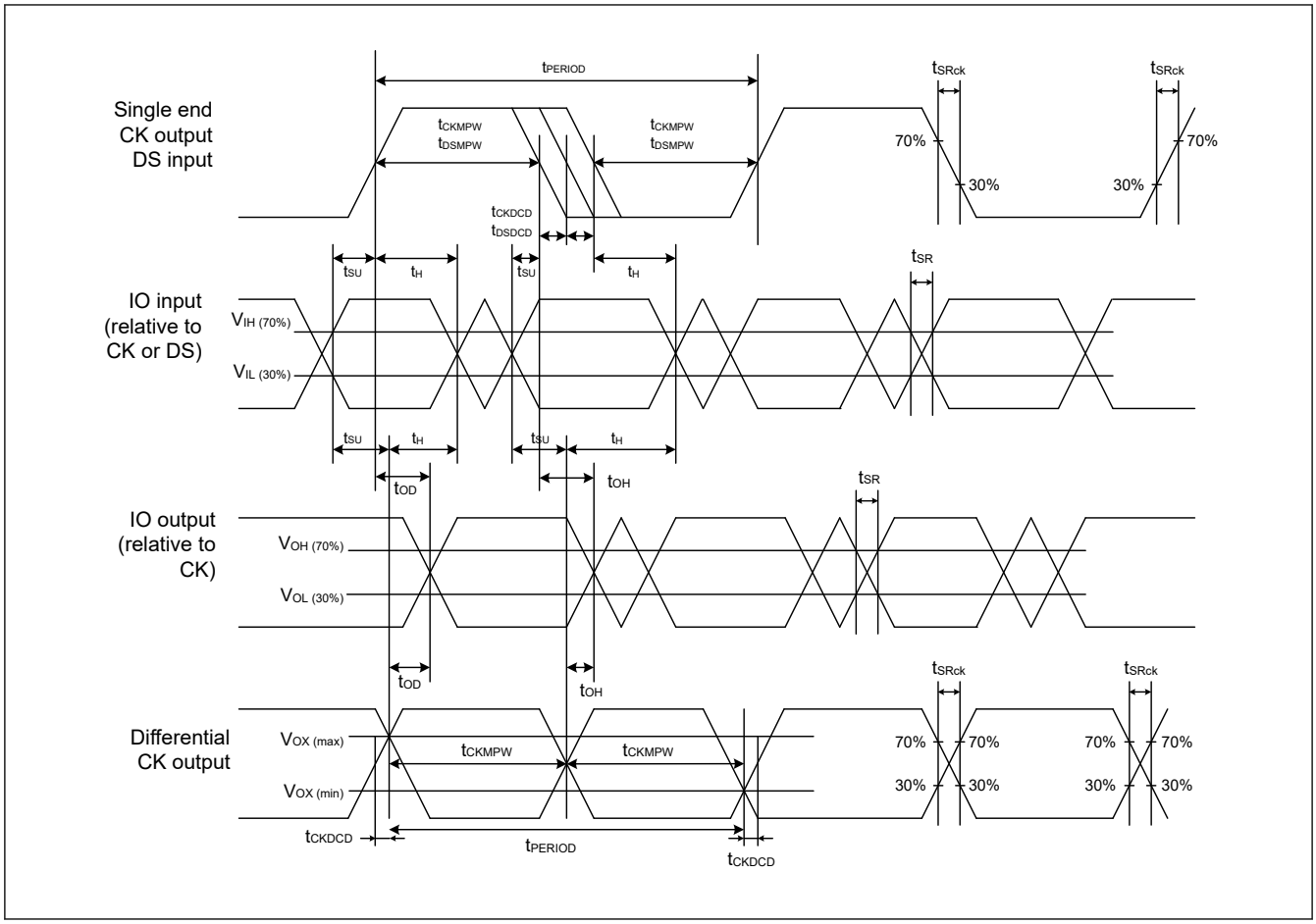


Figure 2.73 xSPI clock / DS timing

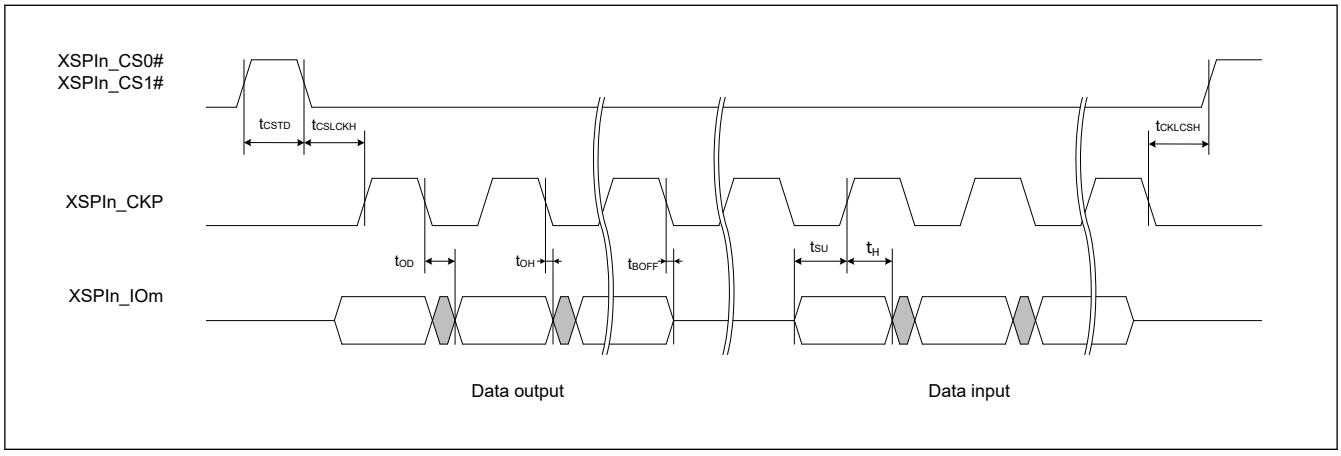


Figure 2.74 SDR transmit/receive timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

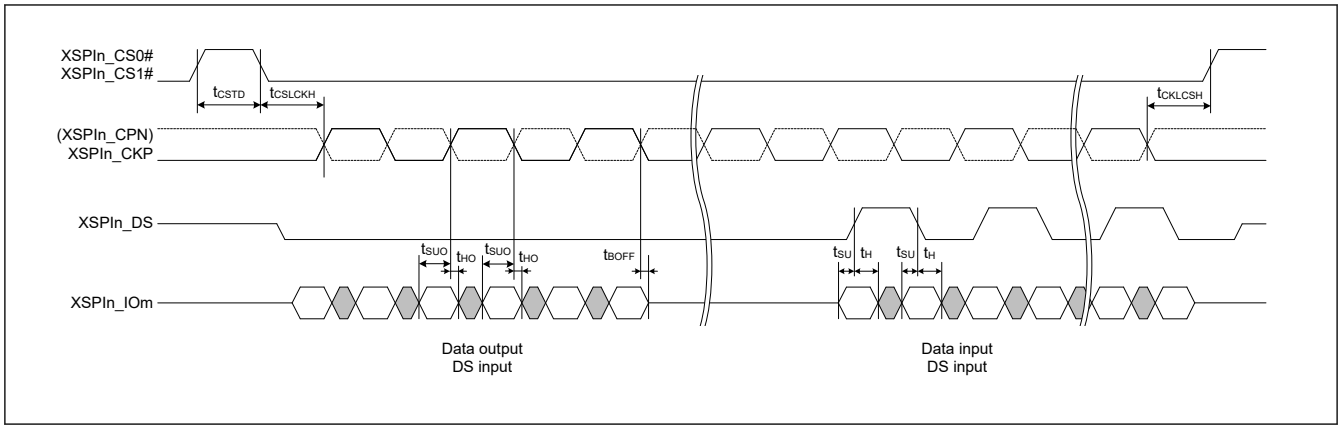


Figure 2.75 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

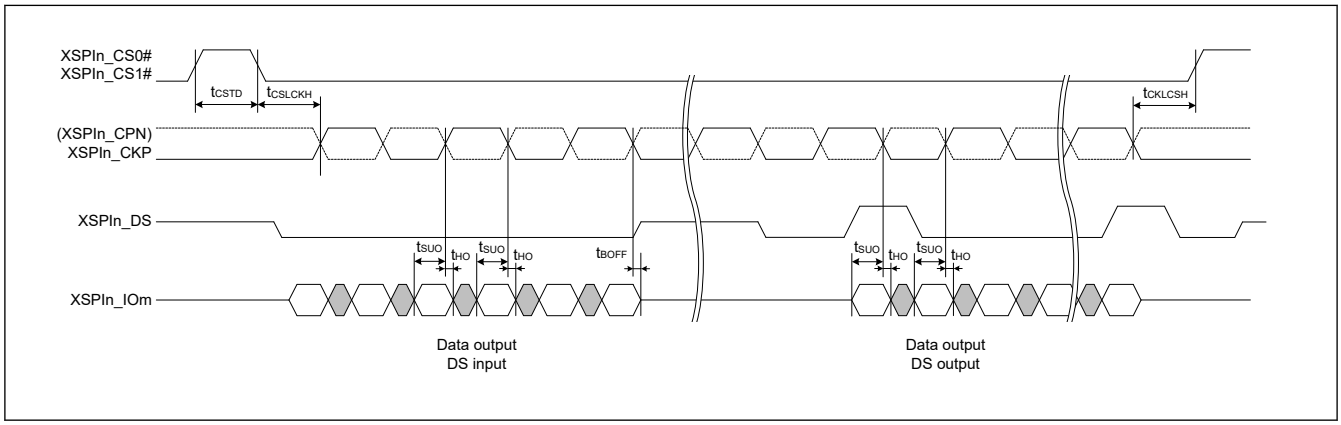


Figure 2.76 DDR transmit/receive timing (HyperRAM write)

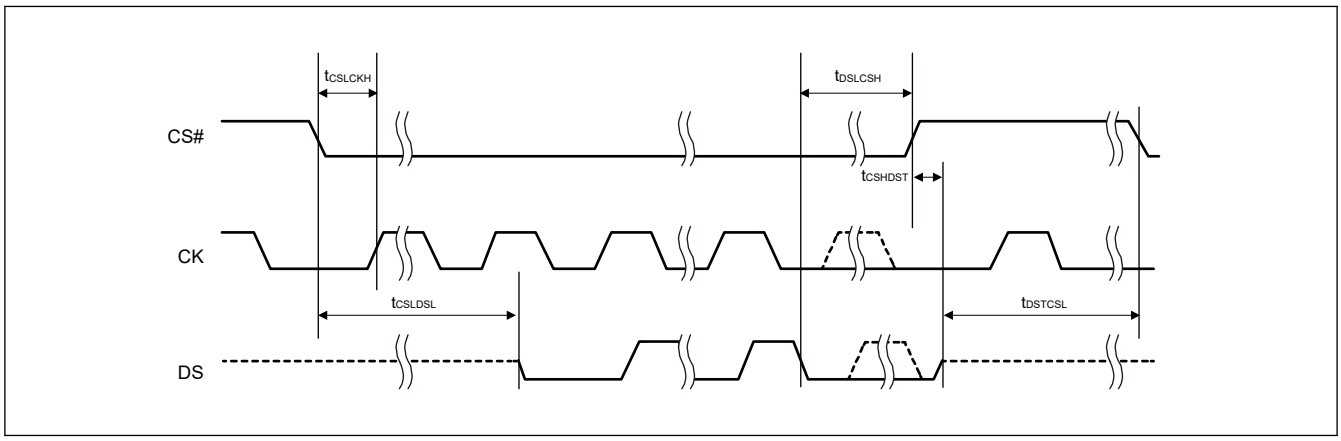


Figure 2.77 DS to CS signal timing

2.5.5.13 Delta-Sigma Interface Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF

Table 2.37 ΔΣ interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
DSMIF	Clock cycle	Master	t_{DScyc}	40	200	ns	Figure 2.78
		Slave		40	200		
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—		
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—		
	Setup time	Master	t_{SU}	15	—	ns	Figure 2.79, Figure 2.80
		Slave		5	—		
	Hold time	Master	t_H	0	—	ns	
		Slave		5	—		

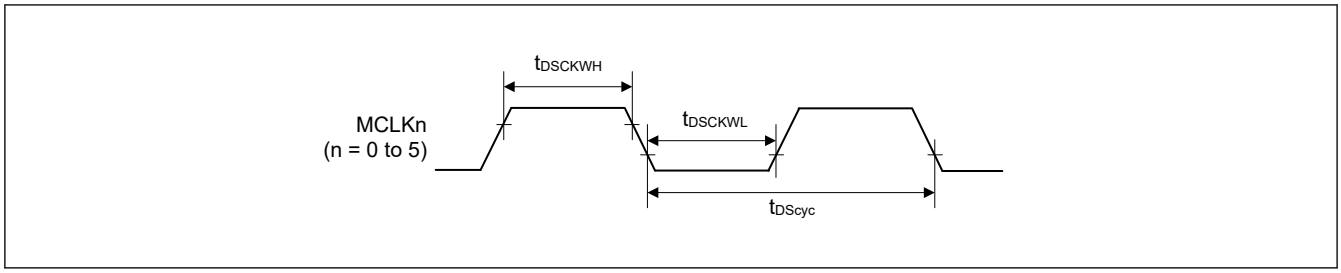


Figure 2.78 Clock input/output timing

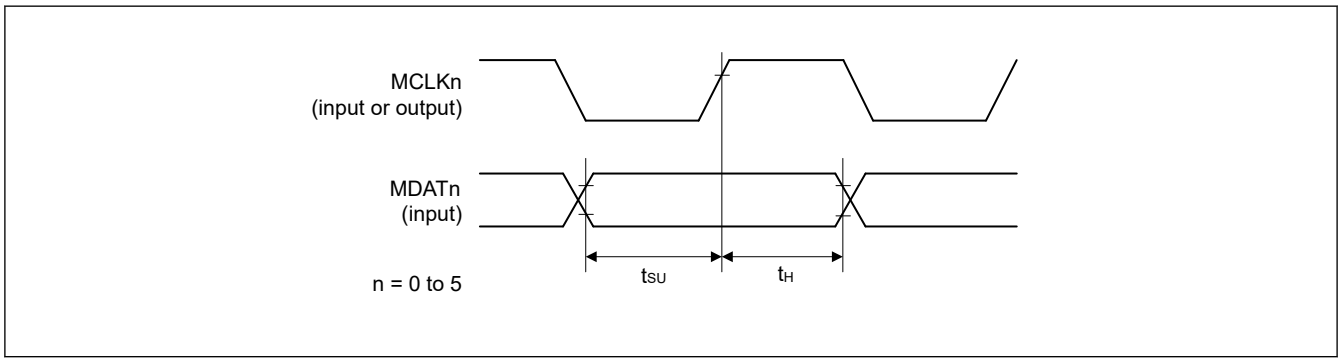


Figure 2.79 Reception timing (MCLKn rising synchronous)

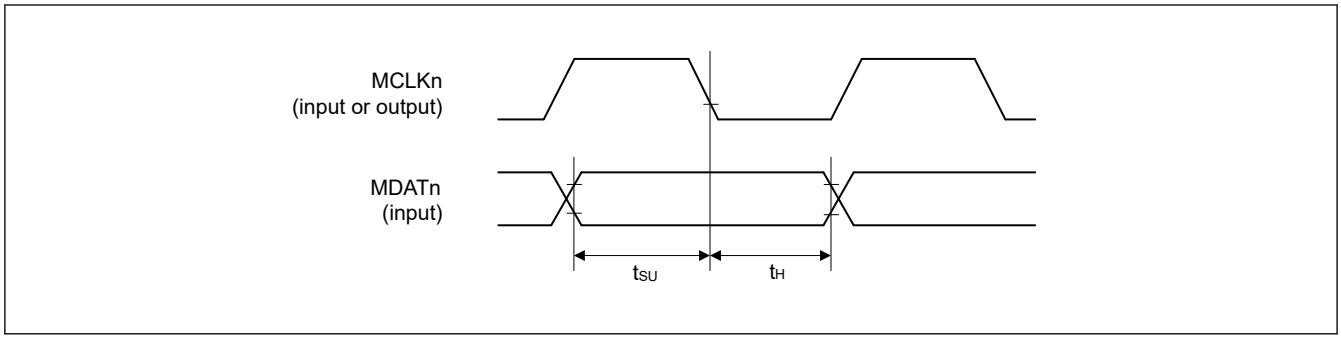


Figure 2.80 Reception timing (MCLKn falling synchronous)

2.5.5.14 Ethernet Interface Timing

Conditions:

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 15 pF (RGMII)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 25 pF (RMII)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (MII)

Table 2.38 Ethernet interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
Ethernet (RGMII)	ETHn_TXCLK, ETHn_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	Figure 2.81
		100 Mbps		36	44		
		10 Mbps		360	440		
	ETHn_TXCLK, ETHn_RXCLK frequency	1 Gbps	—	125 − 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 − 50 ppm	25 + 50 ppm		
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm		
	ETHn_TXCLK, ETHn_RXCLK duty clcle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps		40	60		
	ETHn_TXCLK, ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL), ETHn_RXCLK, ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) rise/fall time		t_{RGMIIr}, t_{RGMIIf}	—	0.75	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) to ETHn_TXCLK output skew		$t_{RGMIIos}$	−0.5	0.5	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) setup time		t_{RGMIIs}	1	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) hold time		t_{RGMIIh}	1	—	ns	
Ethernet (RMII)	ETHn_RXCLK cycle time		t_{RMIIck}	20	—	ns	Figure 2.82
	ETHn_RXCLK frequency Typ. 50 MHz		—	50 − 50 ppm	50 + 50 ppm	MHz	
	ETHn_RXCLK duty		—	35	65	%	
	ETHn_RXCLK rise/fall time		$t_{RMIIckr}$, $t_{RMIIckf}$	0.5	3.5	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN output delay time		t_{RMIId}	2.5	12	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time		t_{RMIIs}	4	—	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) hold time		t_{RMIIh}	2	—	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN, ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) rise/fall time		t_{RMIIr}, t_{RMIIf}	0.5	4	ns	
Ethernet (MII)	ETHn_TXCLK, ETHn_RXCLK cycle time	100 Mbps	t_{MIIck}	40	—	ns	Figure 2.83
		10 Mbps		400	—		
	ETHn_TXCLK, ETHn_RXCLK frequency	100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm		
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN, ETHn_TXER output delay time		t_{MIId}	1	20	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER setup time		t_{MIIs}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER hold time		t_{MIIh}	10	—	ns	

Table 2.39 Ethernet interface timing (MAC to MAC connection mode)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
Ethernet (RGMII)	ETH2_TXCLK, ETH2_RXCLK cycle time	$t_{MRGMIIck}$	7.2	8.8	ns	Figure 2.84
	ETH2_TXCLK, ETH2_RXCLK frequency Typ. 125 MHz	—	125 − 50 ppm	125 + 50 ppm	MHz	
	ETH2_TXCLK, ETH2_RXCLK duty clcle	—	45	55	%	
	ETH2_TXCLK, ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN (TX_CTL), ETH2_RXCLK, ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV (RX_CTL) rise/fall time	$t_{MRGMIIr}$, $t_{MRGMIIf}$	—	0.75	ns	
	ETH2_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) output skew	$t_{MRGMIIos}$	—	0.6	ns	
	ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN (TX_CTL) output setup time	$t_{MRGMIIso}$	1.1	—	ns	
	ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN (TX_CTL) output hold time	$t_{MRGMIIho}$	1.1	—	ns	
	ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV (RX_CTL) input setup time	$t_{MRGMIIsi}$	-0.7	—	ns	
	ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV (RX_CTL) input hold time	$t_{MRGMIIhi}$	2.9	—	ns	
Ethernet (MII)	ETH2_REFCLK cycle time	t_{MMIIck}	40	—	ns	Figure 2.85
	ETH2_REFCLK frequency Typ. 25 MHz	—	25 − 50 ppm	25 + 50 ppm	MHz	
	ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN, ETH2_TXER output delay time	t_{MMIId}	11	25	ns	
	ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV, ETH2_RXER setup time	t_{MMIIs}	10	—	ns	
	ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV, ETH2_RXER hold time	t_{MMIIh}	0	—	ns	

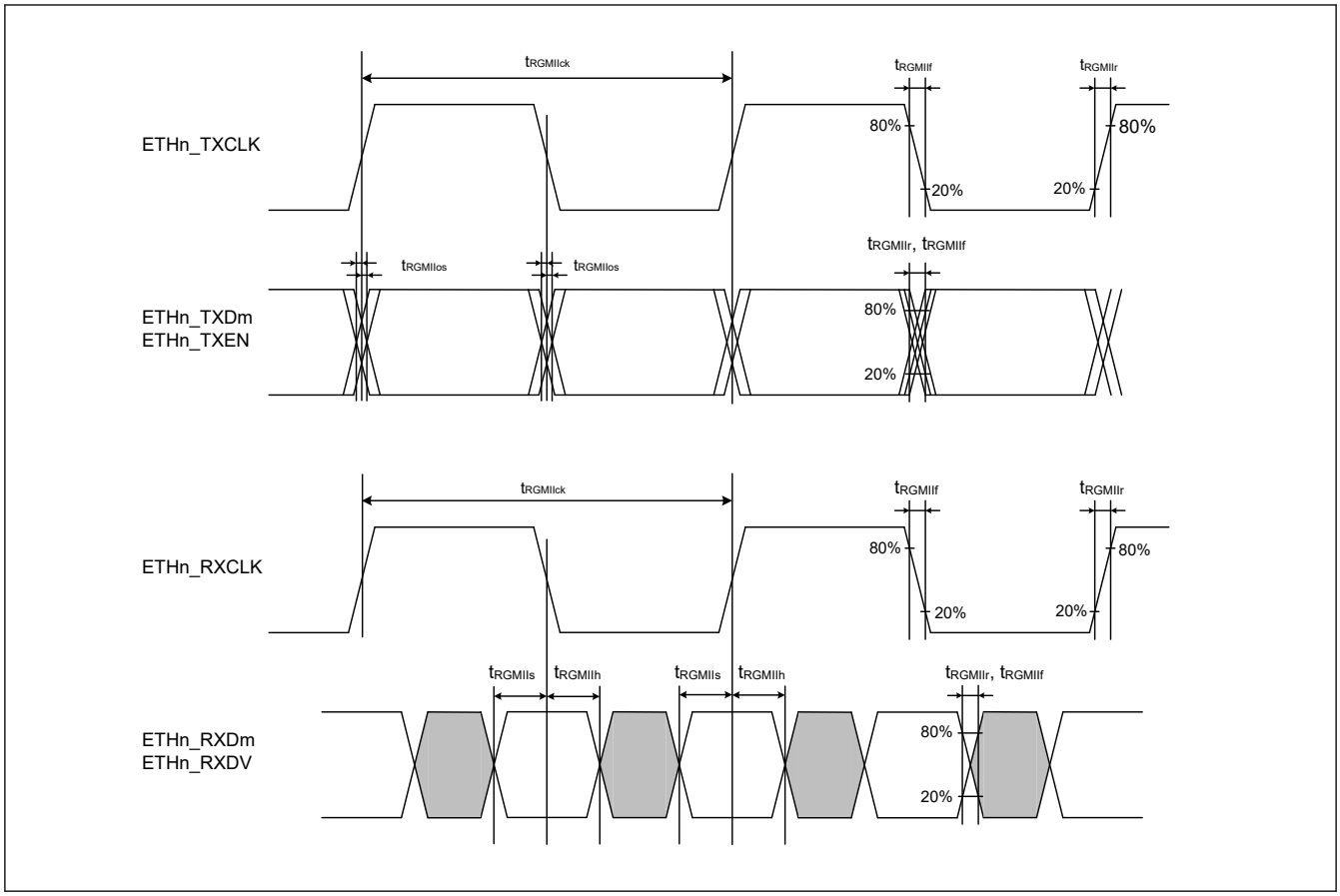


Figure 2.81 RGMII transmission and reception timing (n = 0 to 2, m = 0 to 3)

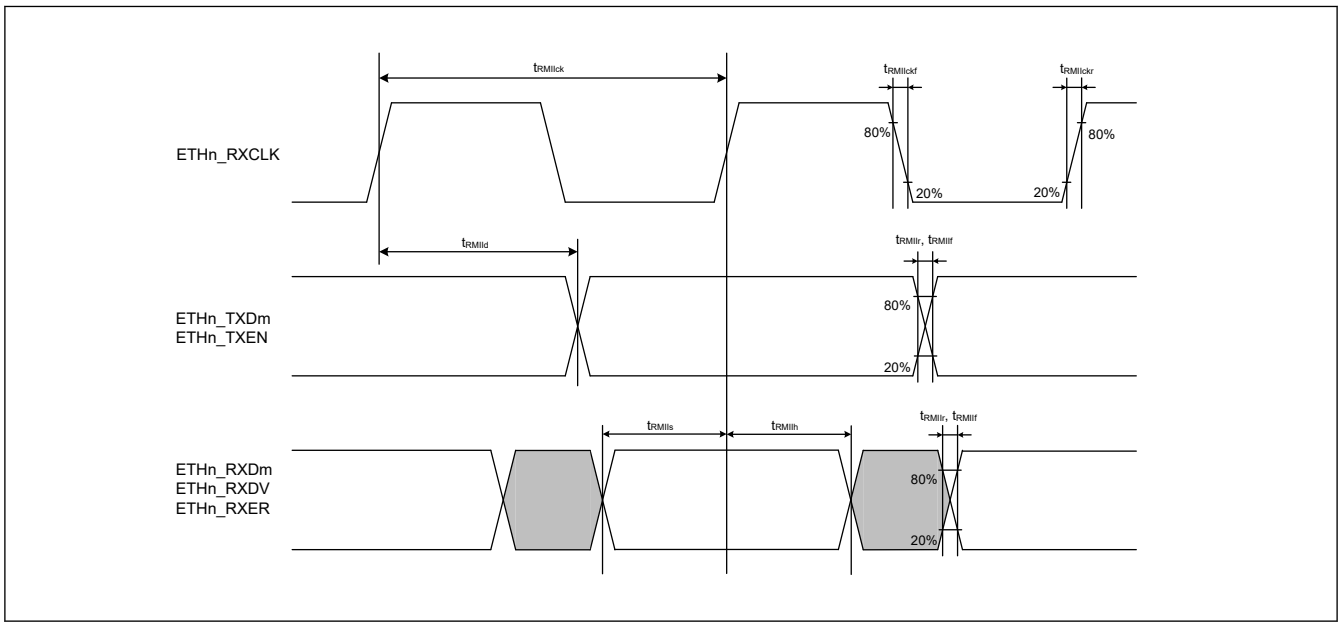


Figure 2.82 RMII transmission and reception timing (n = 0 to 2, m = 0 to 1)

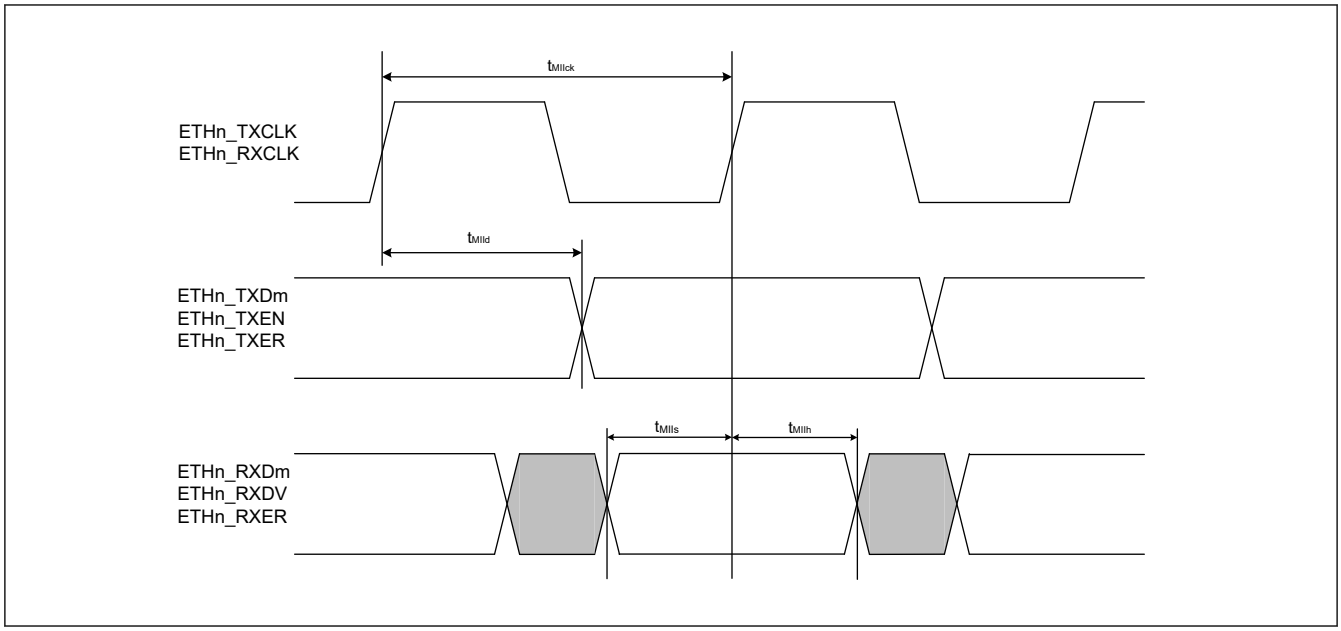


Figure 2.83 MII transmission and reception timing (n = 0 to 2, m = 0 to 3)

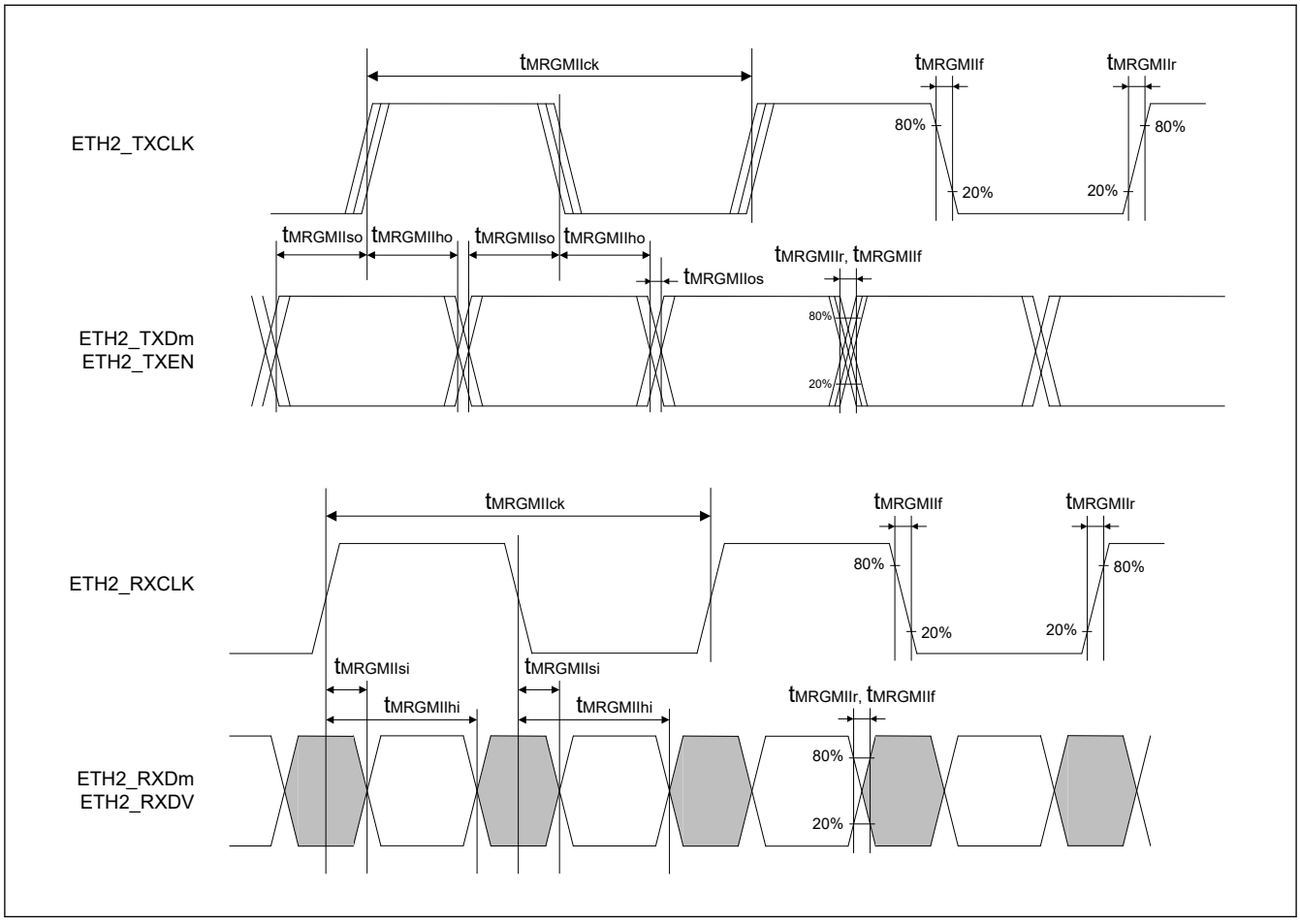


Figure 2.84 RGMII transmission and reception timing (MAC to MAC connection mode) (m = 0 to 3)

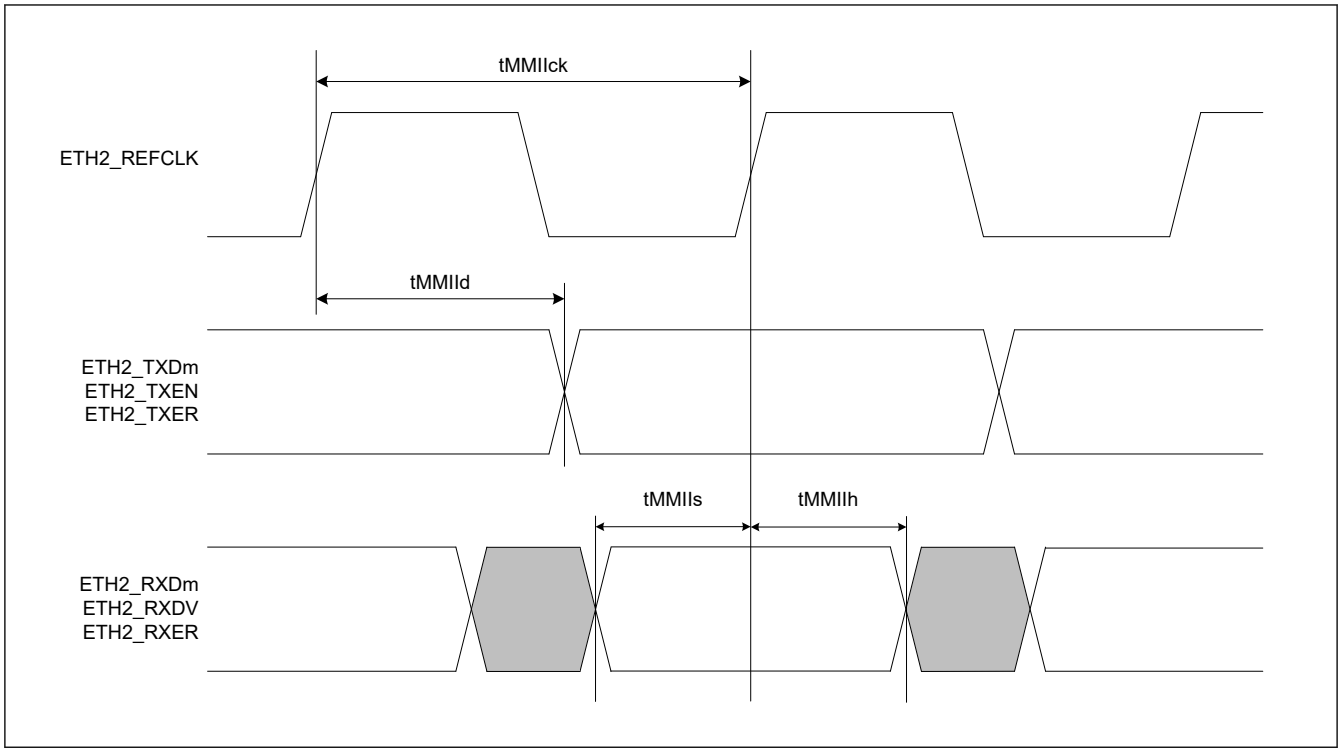


Figure 2.85 MII transmission and reception timing (MAC to MAC connection mode) (m = 0 to 3)

2.5.5.15 Serial Management Interface Timing

Conditions:

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (3.3 V)

Table 2.40 Serial management interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
MDIO	MDC output cycle time	GMAC_MDC, ETHSW_MDC	T_{MDCck}	80	—	ns	Figure 2.86
		ESC_MDC		400	—	ns	
	MDIO output delay time (for MDC fall)*1		T_{MDIOd}	—	20	ns	
	MDIO input setup time (for MDC rise)	GMAC_MDC, ETHSW_MDC	T_{MDIOs}	18	—	ns	
		ESC_MDC		70	—	ns	
	MDIO input hold time (for MDC rise)		T_{MDIOh}	0	—	ns	

Note 1. The output timing from ETHSW is based on the rising edge of MDC, and the output delay can be set in the register.

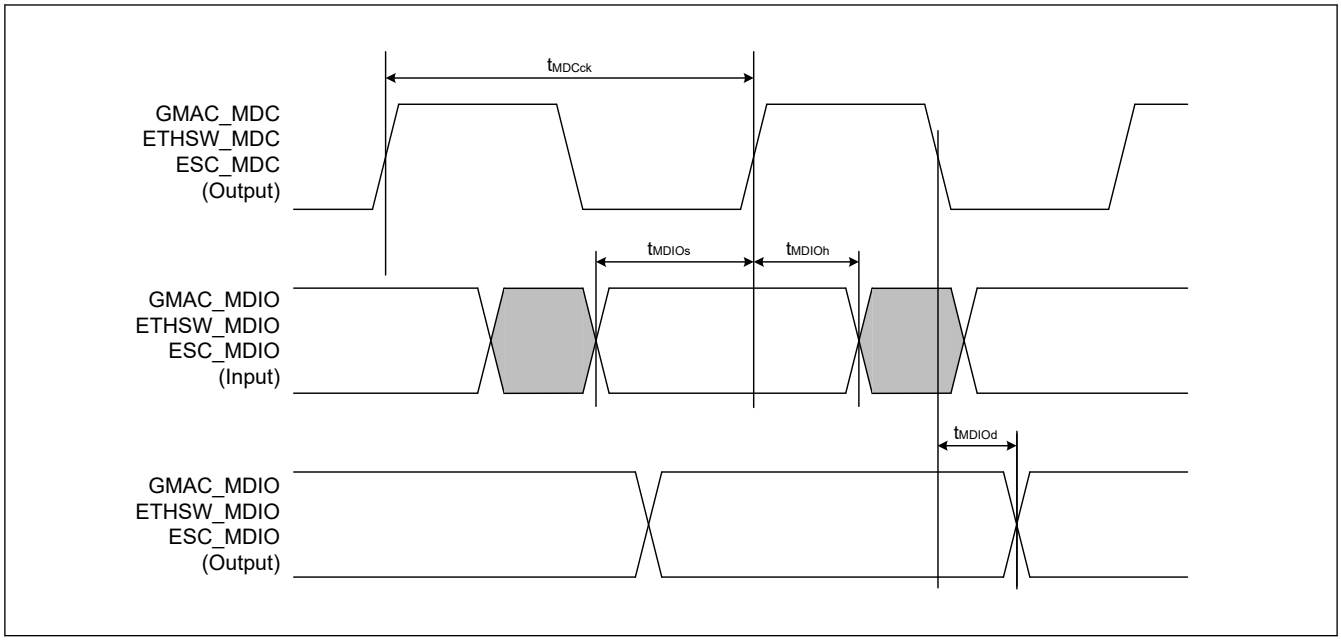


Figure 2.86 Serial management interface timing

2.6 USB Characteristics

Table 2.41 On-chip USB low-speed (host only) characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{LR}	75	—	300	ns	Figure 2.87, Figure 2.88
Falling time	t_{LF}	75	—	300	ns	
Rising/falling time ratio	t_{LR}/t_{LF}	80	—	125	%	

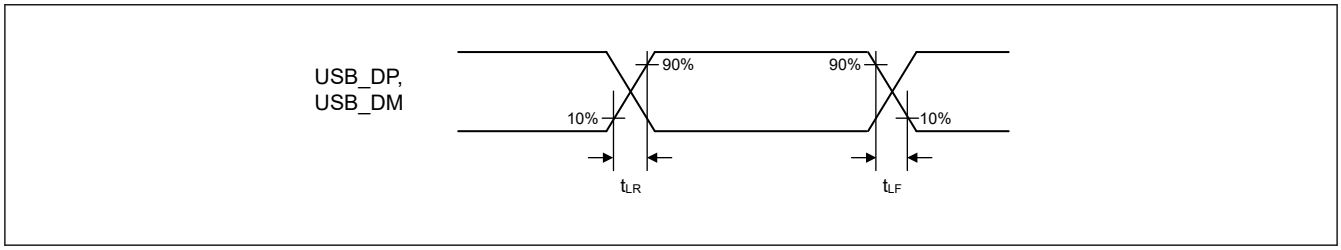


Figure 2.87 USB_DP, USB_DM output timing (low-speed/host only)

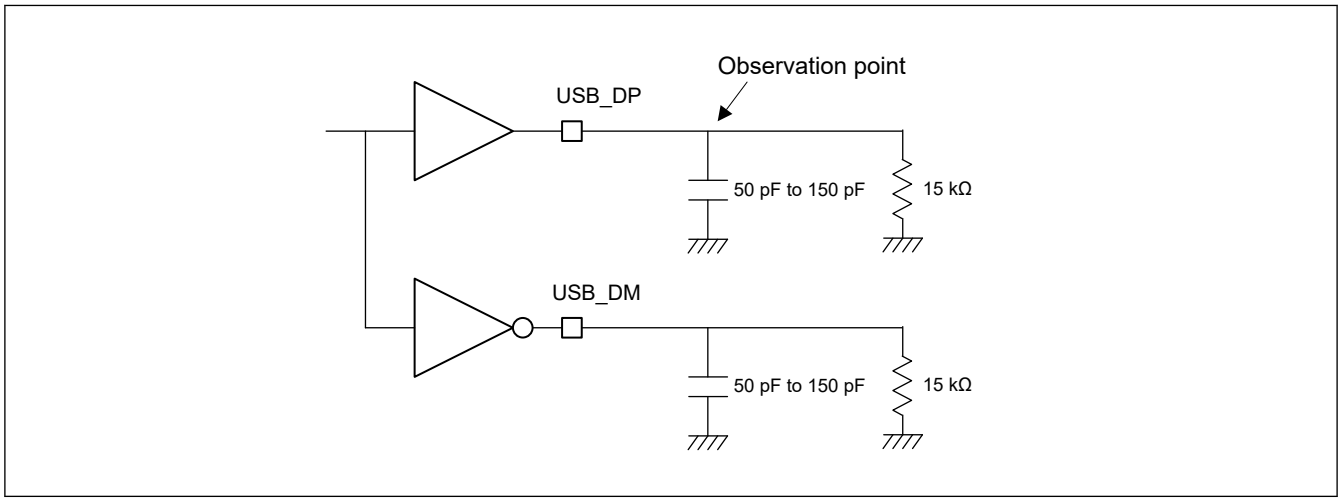


Figure 2.88 Measurement circuit (low-speed/host only)

Table 2.42 On-chip USB full-speed characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{FR}	4	—	20	ns	Figure 2.89, Figure 2.90
Falling time	t_{FF}	4	—	20	ns	
Rising/falling time ratio	t_{FR}/t_{FF}	90	—	111.11	%	

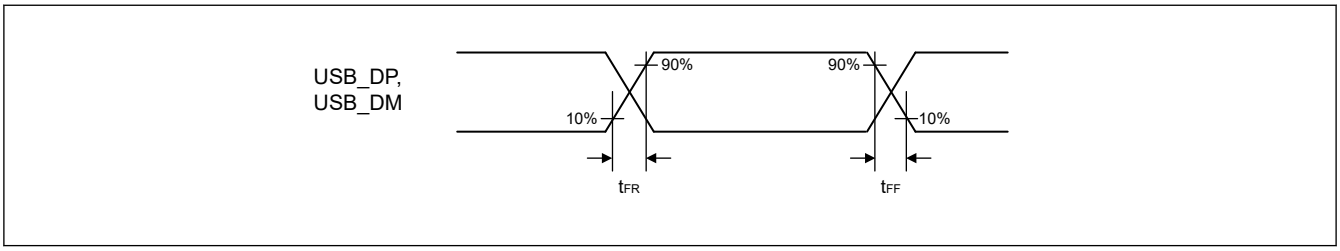


Figure 2.89 USB_DP, USB_DM output timing (full speed)

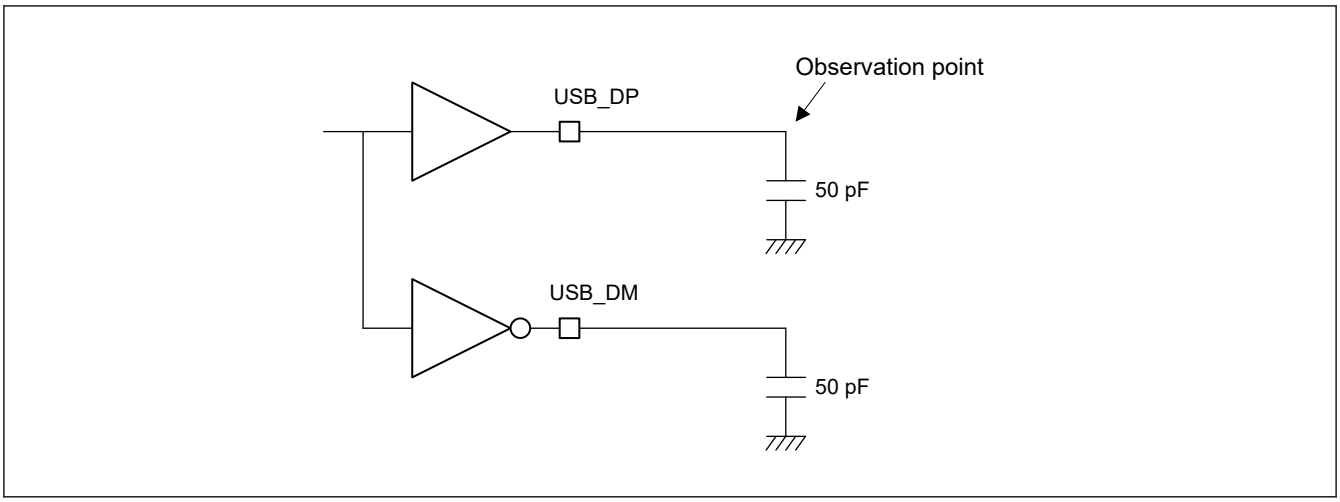


Figure 2.90 Measurement circuit (full speed)

Table 2.43 On-chip USB high-speed characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{HSR}	—	—	2.133	V/µs	Figure 2.91, Figure 2.92
Falling time	t_{HSF}	—	—	2.133	V/µs	
Output resistors (also used as high-speed terminating resistor)	Z_{HSDRV}	40.5	—	49.5	Ω	—

Note: The output resistors (ZHSDRV) for connection to the USB_DP and USB_DM pins are within the LSI.

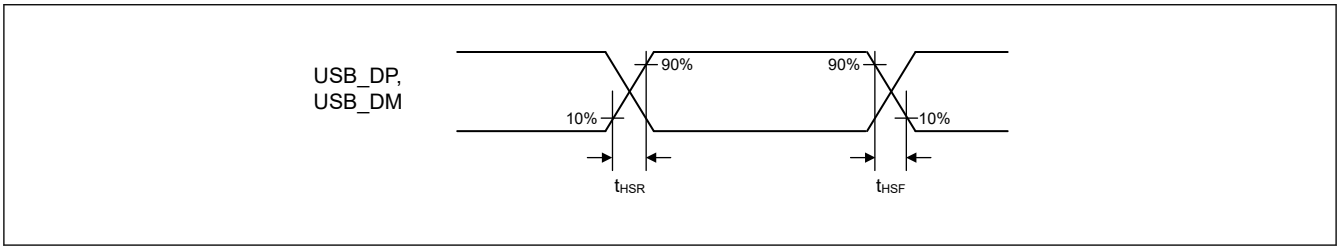


Figure 2.91 USB_DP, USB_DM output timing (high speed)

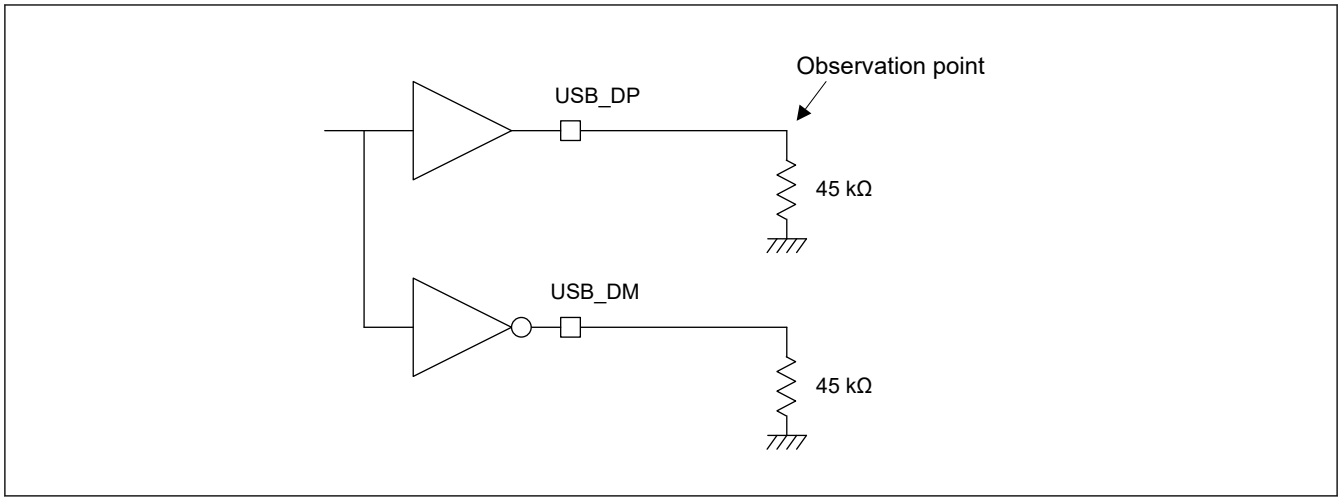


Figure 2.92 Measurement circuit (high speed)

2.7 A/D Conversion Characteristics

Table 2.44 12-Bit A/D (unit 0) conversion characteristics (1 of 2)

Parameter			Min.	Typ.	Max.	Unit	Reference figure
Resolution			12			bits	—
Analog input capacitance		BGA package	—	—	13	pF	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time[*1] Permissible signal source impedance Max. = 1.0 kΩ		1.52	—	—	µs	—
	Offset error		—	—	±13	LSB	—
	Full-scale error		—	—	±13	LSB	—
	Quantization error		—	±0.5	—	LSB	—
	Absolute accuracy	BGA package	—	—	±14	LSB	—
	DNL differential non-linearity error	BGA package	—	—	±3	LSB	—
	INL integral non-linearity error	BGA package	—	—	±4	LSB	—
	Holding characteristics of sample-and-hold circuits		—	—	2.67	µs	—
	Dynamic range		0.15	—	VREFH0 - 0.15	V	—

Table 2.44 12-Bit A/D (unit 0) conversion characteristics (2 of 2)

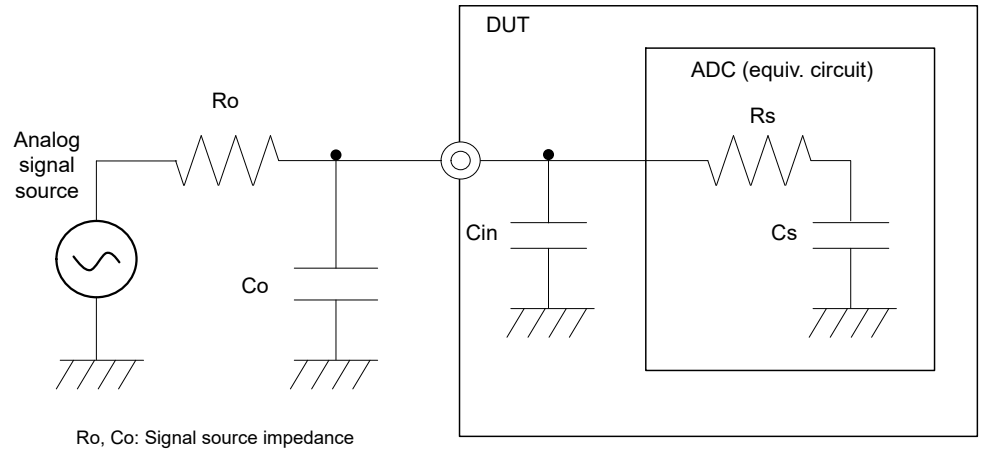
Parameter			Min.	Typ.	Max.	Unit	Reference figure
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ		0.84	—	—	µs	—
	Offset error		—	—	±11	LSB	—
	Full-scale error		—	—	±11	LSB	—
	Quantization error		—	±0.5	—	LSB	—
	Absolute accuracy	BGA package	—	—	±12	LSB	—
	DNL differential non-linearity error	BGA package	—	—	±3	LSB	—
	INL integral non-linearity error	BGA package	—	—	±4	LSB	—

Note: The specified values in the table apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the specified ranges.
Note 1. The conversion time is the total of the sampling time and the comparison time.

Table 2.45 12-Bit A/D (unit 1) conversion characteristics

Parameter		Min.	Typ.	Max.	Unit	Reference figure
Resolution		12			bits	—
Conversion time*1	Permissible signal source impedance Max = 1.0 kΩ	0.84	—	—	µs	—
Analog input capacitance		—	—	13	pF	—
Offset error		—	—	±11	LSB	—
Full-scale error		—	—	±11	LSB	—
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	—	±12	LSB	—
DNL differential non-linearity error		—	—	±3	LSB	—
INL integral non-linearity error		—	—	±4	LSB	—

Note: The specified values in the table apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the specified ranges.
Note 1. The conversion time is the total of the sampling time and the comparison time.



Ro, Co: Signal source impedance
Cin: Internal parasitic capacitance (package, I/O, etc.)
Rs, Cs: ADC equivalent circuit impedance (With sample-and-hold circuits: Rs = 1.5 kΩ and Cs = 4 pF.
Without sample-and-hold circuits: Rs = 0.75 kΩ and Cs = 3 pF. (Typical))

Figure 2.93 A/D converter equivalent circuit and peripheral configuration diagram

2.8 Temperature Sensor Characteristics

Table 2.46 Temperature sensor characteristics

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	*1
Temperature slope	—	0.0625	—	°C/LSB	—
Output code (at 25°C)	—	1545 (decimal)	—	—	TSUSAD register

Note 1. 2-point calibration (Tj = 25°C and Tj = 85°C) and 8 times averaging.

2.9 Debug Interface Timing

Condition: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5

Table 2.47 Debug interface timing (1 of 2)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
TCK cycle time	With an ICE connected	t_{TCKcyc}	30*1	—	ns	Figure 2.94
	For use in BSCAN		80	—		
TCK high pulse width		t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width		t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time		t_{TDIS}	5	—	ns	Figure 2.95 Output load: 30 pF
TDI hold time		t_{TDIH}	5	—	ns	
TMS/SWDIO setup time		t_{TMSS}	5	—	ns	
TMS/SWDIO hold time		t_{TMSH}	5	—	ns	
SWDIO delay time		t_{SWDO}	—	15	ns	
TDO delay time	With an ICE connected	t_{TDOD}	—	15	ns	
	For use in BSCAN		—	22		
Capture register setup time		t_{CAPTS}	5	—	ns	Figure 2.96
Capture register hold time		t_{CAPTH}	5	—	ns	
Update register delay time		$t_{UPDATED}$	—	15	ns	

Table 2.47 Debug interface timing (2 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
Trace clock cycle	t_{TCYC}	20	—	ns	Figure 2.97 Output load: 15 pF
Trace data delay time	t_{TDT}	-1.5	4.0	ns	

Note 1. This value is the minimum cycle time for the normal operation of internal circuits.
The actual cycle time should be determined in consideration of the TCK capture edge timing and cable length of the connected ICE.

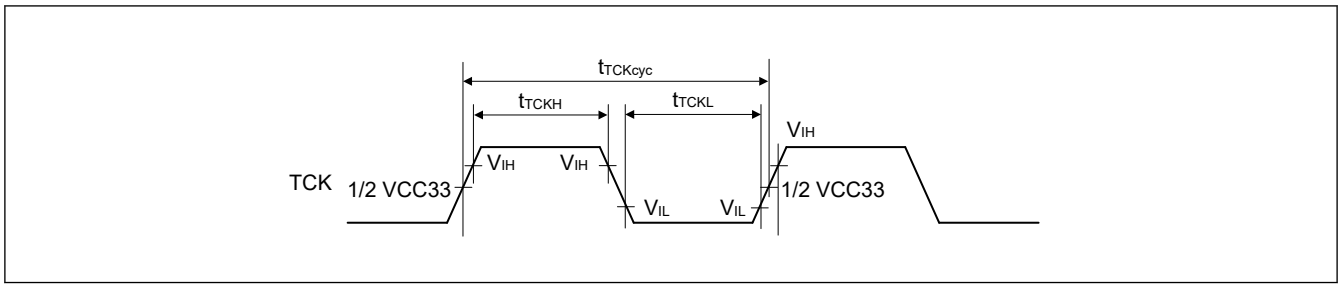


Figure 2.94 TCK input timing

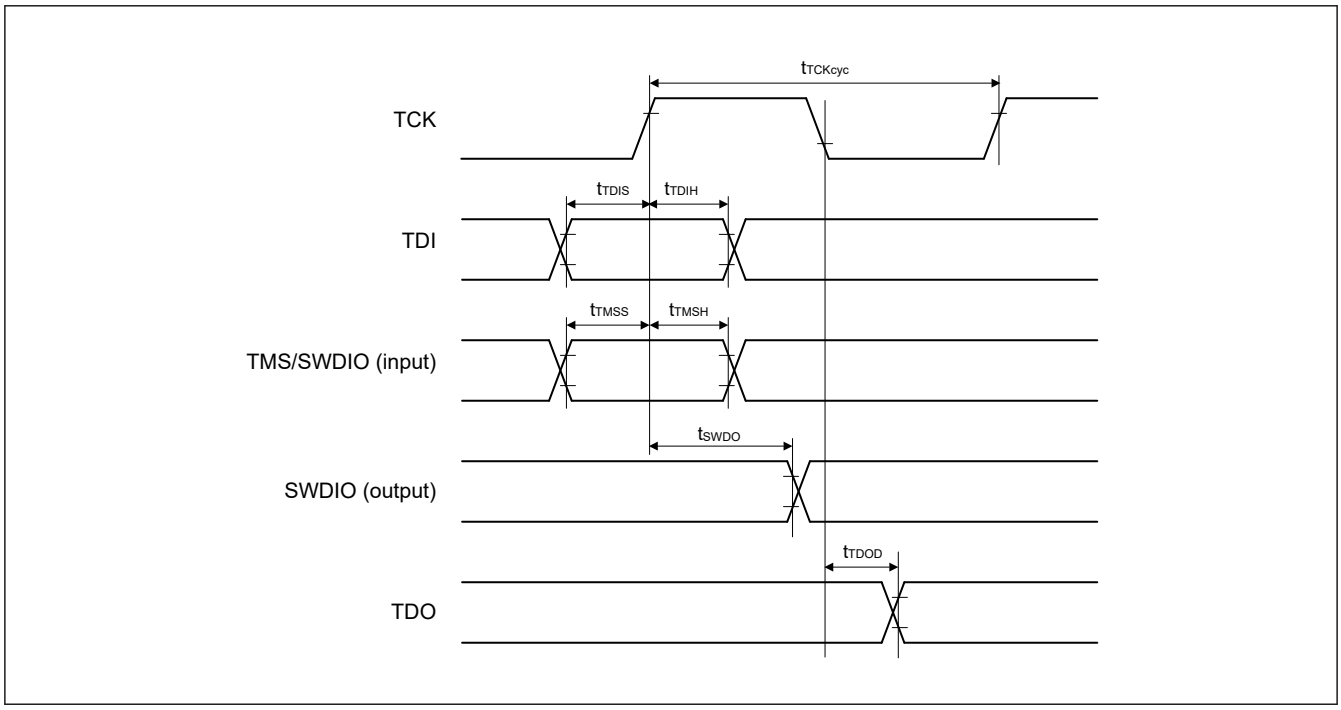


Figure 2.95 Data transfer timing

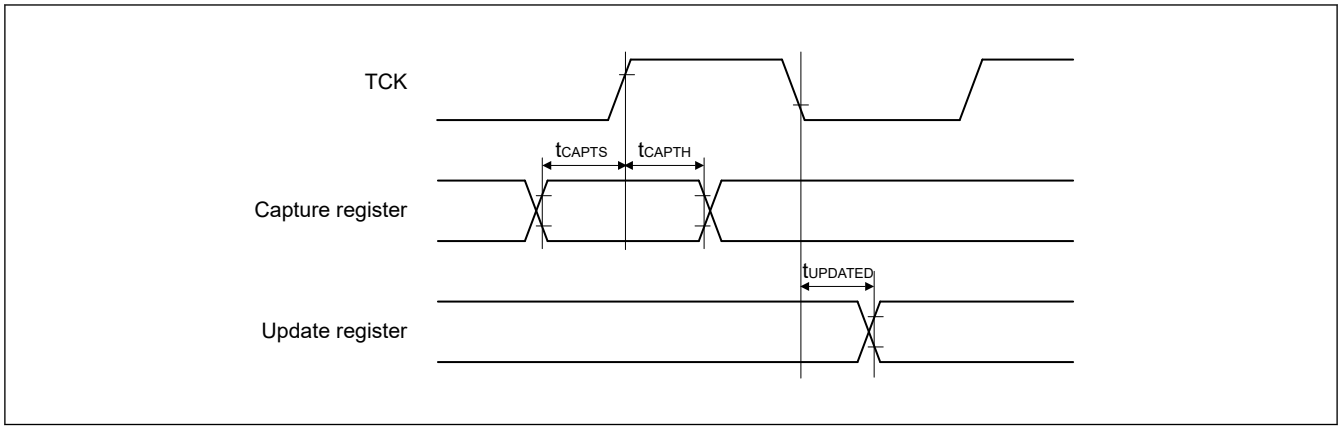


Figure 2.96 Boundary scan input/output timing

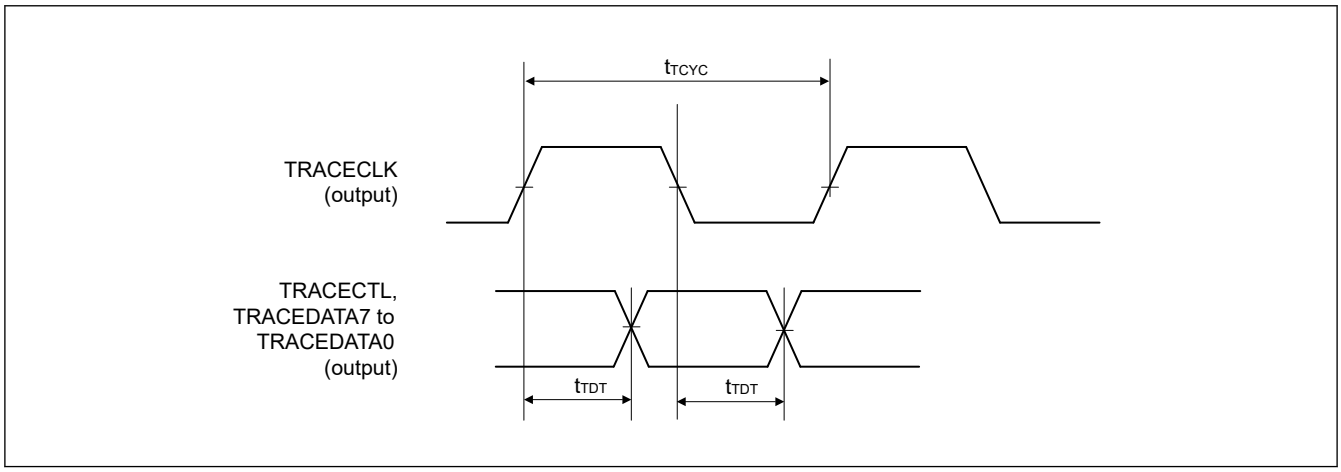
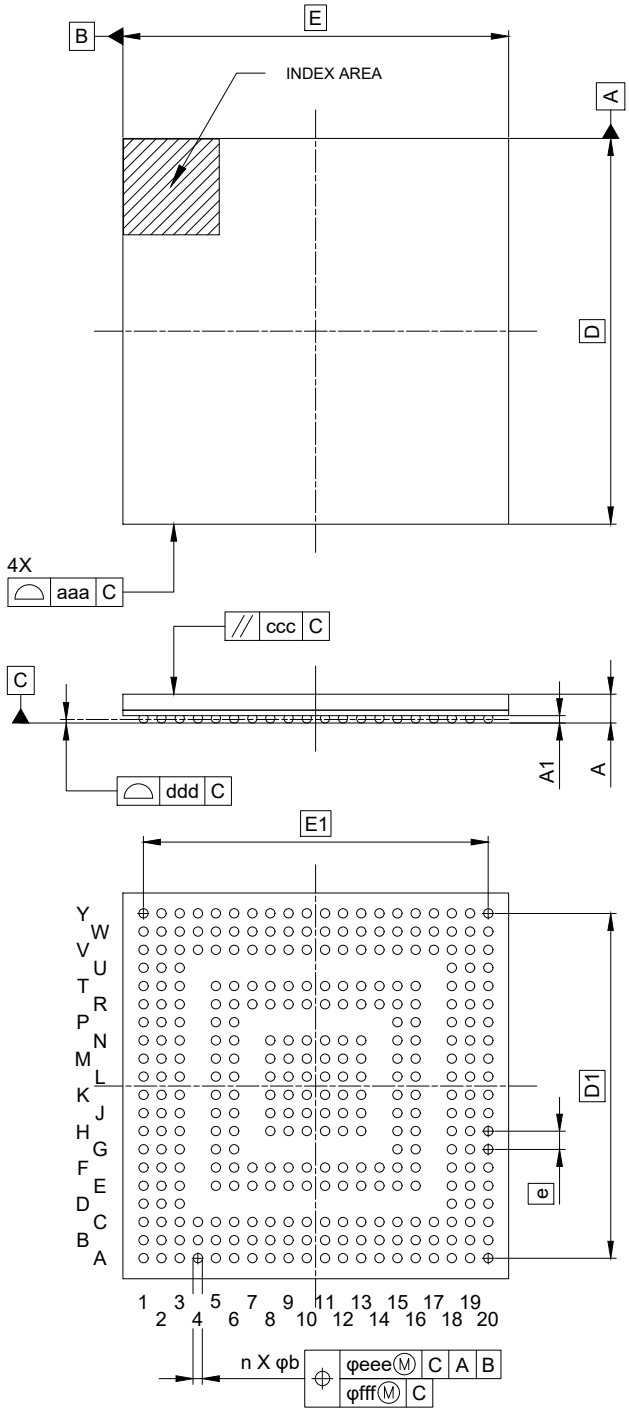


Figure 2.97 Trace interface timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

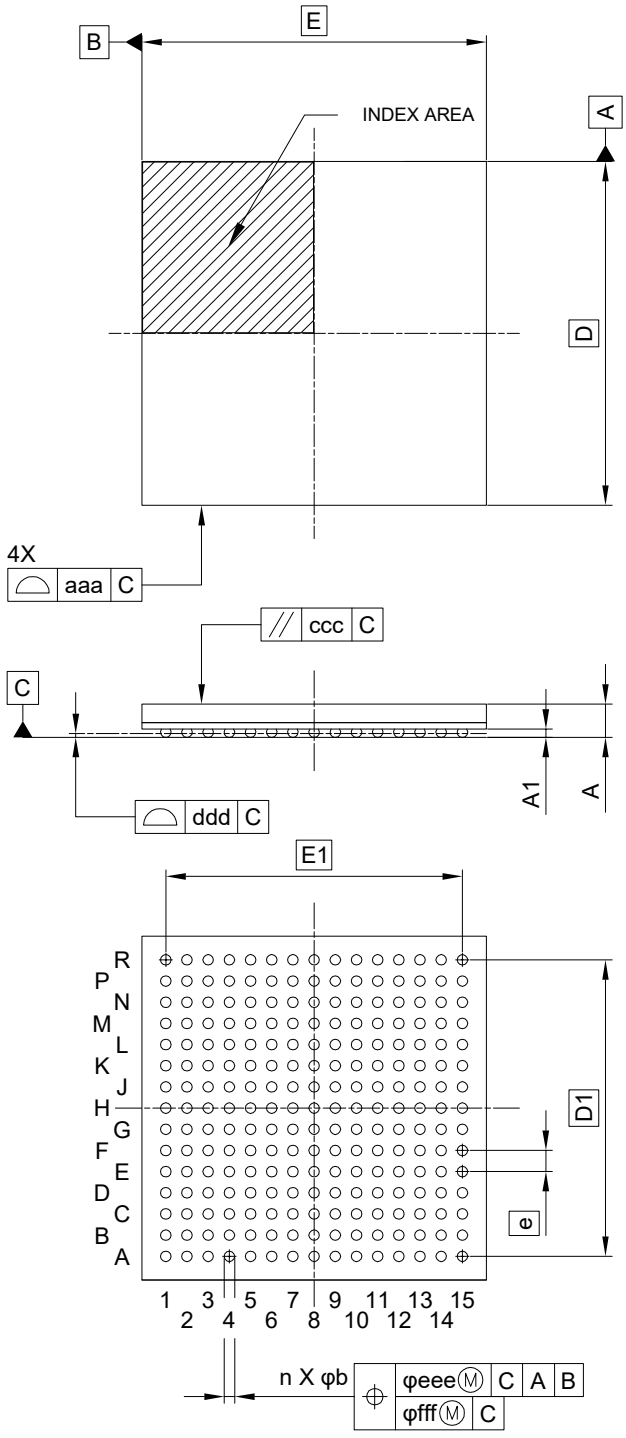
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA320-17x17-0.80	PLBG0320GA-A	0.66



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	17.00	—
E	—	17.00	—
D1	—	15.20	—
E1	—	15.20	—
A	—	—	1.40
A1	0.27	—	—
b	0.38	0.43	0.48
e	—	0.80	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.15
eee	—	—	0.15
fff	—	—	0.08
n	—	320	—

Figure 1.1 320-pin FBGA

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA225-13x13-0.80	PLBG0225GB-A	0.39



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	13.00	—
E	—	13.00	—
D1	—	11.20	—
E1	—	11.20	—
A	—	—	1.40
A1	0.27	—	—
b	0.38	0.43	0.48
e	—	0.80	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.12
eee	—	—	0.15
fff	—	—	0.08
n	—	225	—

Figure 1.2 225-pin FBGA

Revision History

Revision 1.00 — June 28, 2024

Initial release

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