

## SLG46533-E

GreenPAK Programmable Mixed-Signal Matrix with Extended Temperature Range

The SLG46533-E provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG46533-E. This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

### Features

- Four Analog Comparators (ACMP)
- Two Voltage References ( $V_{REF}$ )
- Twenty-six Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - Twelve Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Five 8-bit delays/counters or 3-bit LUTs
  - Two 16-bit delays/counters or 4-bit LUTs
  - Two Deglitch Filters with Edge Detectors
- Combinatorial Logic
  - One 4-bit LUT
- Serial Communications
  - I<sup>2</sup>C Protocol Compliant
- 16x8 RAM Memory with Defined NVM OTP Initial State
- Pipe Delay – 16 Stage/3 Output (Part of Combination Function Macrocell)
- Programmable Delay
- Two Oscillators
  - Configurable 25 kHz or 2 MHz
  - 25 MHz Oscillator
- Power-On Reset (POR)
- Analog Temperature Sensor
- Logic and Mixed-Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- Power Supply
  - 1.8 V ( $\pm 5\%$ ) to 5.0 V ( $\pm 10\%$ )  $V_{DD}$
- Ambient Operating Temperature Range: -40 °C to +105 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - 20-pin STQFN: 2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm pitch

### Applications

- Outdoors Electronics
- Factory Automation
- Servers and Networking Equipment
- Chargers

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# 1. Block Diagram

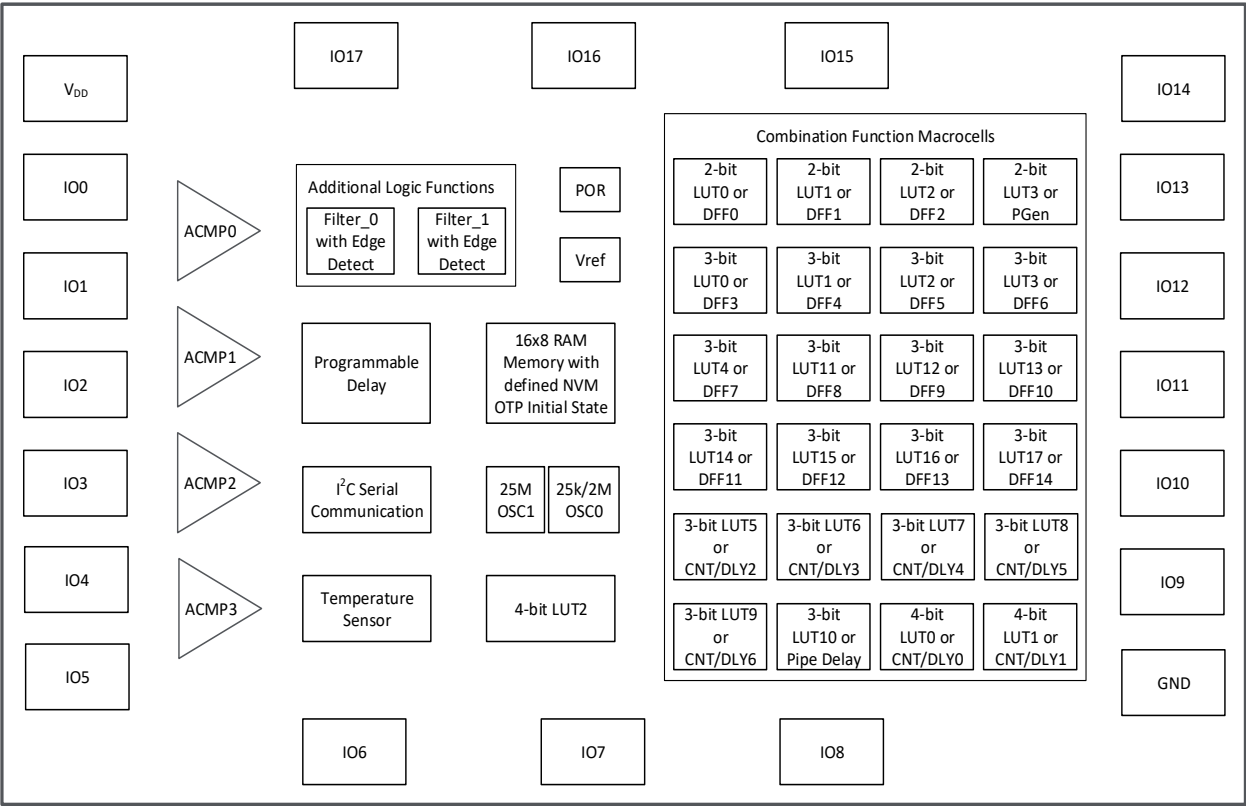


Figure 1. Block Diagram

## 2. Pin Information

### 2.1 Pin Assignments

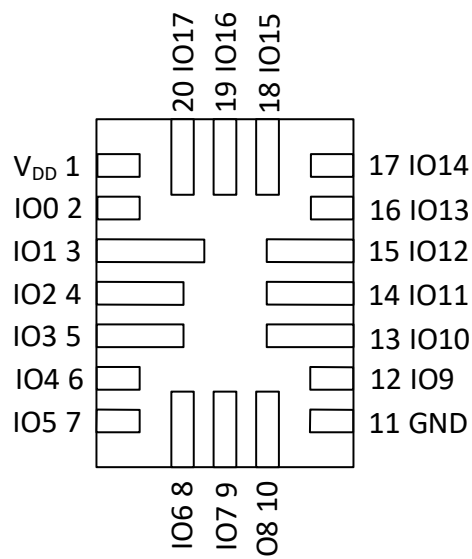


Figure 2. Pin Assignments - STQFN-20 (Top View)

### 2.2 Pin Descriptions

Table 1. Pin Description

| Pin Number | Pin Name        | Description                              |
|------------|-----------------|------------------------------------------|
| 1          | V <sub>DD</sub> | Power Supply                             |
| 2          | IO0             | GPI                                      |
| 3          | IO1             | GPIO with OE                             |
| 4          | IO2             | GPIO                                     |
| 5          | IO3             | GPIO with OE                             |
| 6          | IO4             | GPIO/ACMP0+                              |
| 7          | IO5             | GPIO with OE/ACMP0-                      |
| 8          | IO6             | GPIO/SCL                                 |
| 9          | IO7             | GPIO/SDA                                 |
| 10         | IO8             | GPIO with OE/ACMP1+                      |
| 11         | GND             | GND                                      |
| 12         | IO9             | GPIO/ACMP0-/ACMP1-/ACMP2-/ACMP3-         |
| 13         | IO10            | GPIO with OE/ACMP2+/ACMP3+               |
| 14         | IO11            | GPIO with OE/ACMP2-/ACMP3-               |
| 15         | IO12            | GPIO/ACMP3+                              |
| 16         | IO13            | GPIO with OE                             |
| 17         | IO14            | GPIO/EXT_CLK0                            |
| 18         | IO15            | GPIO with OE/V <sub>REF</sub> 1/EXT_CLK1 |

Table 1. Pin Description (Cont.)

| Pin Number | Pin Name | Description                    |
|------------|----------|--------------------------------|
| 19         | IO16     | GPIO with OE/V <sub>REF0</sub> |
| 20         | IO17     | GPIO/EXT_CLK2                  |

Table 2. Pin Type Definitions

| Pin type        | Definition     |
|-----------------|----------------|
| V <sub>DD</sub> | Power Supply   |
| IO              | Input/Output   |
| GND             | General Ground |

Table 3. Functional Pin Description

| STQFN<br>20L Pin # | Pin Name        | Signal Name     | Function                       | Input Options                         | Output Options            |
|--------------------|-----------------|-----------------|--------------------------------|---------------------------------------|---------------------------|
| 1                  | V <sub>DD</sub> | V <sub>DD</sub> | Power Supply                   | --                                    | --                        |
| 2                  | IO0             | IO0             | General Purpose Input          | Digital Input without Schmitt Trigger | --                        |
|                    |                 |                 |                                | Digital Input with Schmitt Trigger    | --                        |
|                    |                 |                 |                                | Low Voltage Digital Input             | --                        |
| 3                  | IO1             | IO1             | General Purpose IO with OE [1] | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x)       |
|                    |                 |                 |                                | Digital Input with Schmitt Trigger    | Open-Drain NMOS (1x) (2x) |
|                    |                 |                 |                                | Low Voltage Digital Input             | --                        |
| 4                  | IO2             | IO2             | General Purpose IO             | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x)       |
|                    |                 |                 |                                | Digital Input with Schmitt Trigger    | Open-Drain NMOS (1x) (2x) |
|                    |                 |                 |                                | Low Voltage Digital Input             | Open-Drain PMOS (1x) (2x) |
| 5                  | IO3             | IO3             | General Purpose IO with OE [1] | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x)       |
|                    |                 |                 |                                | Digital Input with Schmitt Trigger    | Open-Drain NMOS (1x) (2x) |
|                    |                 |                 |                                | Low Voltage Digital Input             | --                        |

Table 3. Functional Pin Description (Cont.)

| STQFN<br>20L Pin # | Pin Name | Signal Name | Function                                  | Input Options                         | Output Options            |
|--------------------|----------|-------------|-------------------------------------------|---------------------------------------|---------------------------|
| 6                  | IO4      | IO4         | General Purpose IO                        | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x)       |
|                    |          |             |                                           | Digital Input with Schmitt Trigger    | Open-Drain NMOS (1x) (2x) |
|                    |          |             |                                           | Low Voltage Digital Input             | Open-Drain PMOS (1x) (2x) |
|                    |          | ACMP0+      | Analog Comparator 0 Positive Input        | Analog                                | --                        |
| 7                  | IO5      | IO5         | General Purpose IO with OE <sup>[1]</sup> | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x)       |
|                    |          |             |                                           | Digital Input with Schmitt Trigger    | Open-Drain NMOS (1x) (2x) |
|                    |          |             |                                           | Low Voltage Digital Input             | --                        |
|                    |          | ACMP0-      | Analog Comparator 0 Negative Input        | Analog                                | --                        |
| 8                  | IO6      | IO6         | General Purpose IO                        | Digital Input without Schmitt Trigger | Open-Drain NMOS (1x) (2x) |
|                    |          |             |                                           | Digital Input with Schmitt Trigger    | --                        |
|                    |          |             |                                           | Low Voltage Digital Input             | --                        |
|                    |          | SCL         | I <sup>2</sup> C Serial Clock             | Digital Input without Schmitt Trigger | Open-Drain NMOS           |
|                    |          |             |                                           | Digital Input with Schmitt Trigger    | Open-Drain NMOS           |
|                    |          |             |                                           | Low Voltage Digital Input             | Open-Drain NMOS           |
| 9                  | IO7      | IO7         | General Purpose IO                        | Digital Input without Schmitt Trigger | Open-Drain NMOS (1x) (2x) |
|                    |          |             |                                           | Digital Input with Schmitt Trigger    | --                        |
|                    |          |             |                                           | Low Voltage Digital Input             | --                        |
|                    |          | SDA         | I <sup>2</sup> C Serial Data              | Digital Input without Schmitt Trigger | Open-Drain NMOS           |
|                    |          |             |                                           | Digital Input with Schmitt Trigger    | Open-Drain NMOS           |
|                    |          |             |                                           | Low Voltage Digital Input             | Open-Drain NMOS           |

Table 3. Functional Pin Description (Cont.)

| STQFN<br>20L Pin # | Pin Name | Signal Name | Function                              | Input Options                            | Output Options                    |
|--------------------|----------|-------------|---------------------------------------|------------------------------------------|-----------------------------------|
| 10                 | IO8      | IO8         | General Purpose IO<br>with OE [1]     | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)               |
|                    |          |             |                                       | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x) (4x) |
|                    |          |             |                                       | Low Voltage Digital Input                | Open-Drain PMOS<br>(1x) (2x)      |
|                    |          | ACMP1+      | Analog Comparator 1<br>Positive Input | Analog                                   | --                                |
| 11                 | GND      | GND         | Ground                                | --                                       | --                                |
| 12                 | IO9      | IO9         | General Purpose IO                    | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)               |
|                    |          |             |                                       | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x) (4x) |
|                    |          |             |                                       | Low Voltage Digital Input                | --                                |
|                    |          | EXT_VREF    | Analog Comparator<br>Negative Input   | Analog                                   | --                                |
| 13                 | IO10     | IO10        | General Purpose IO<br>with OE [1]     | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)               |
|                    |          |             |                                       | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x)      |
|                    |          |             |                                       | Low Voltage Digital Input                | --                                |
|                    |          | ACMP2+      | Analog Comparator 2<br>Positive Input | Analog                                   | --                                |
|                    |          | ACMP3+      | Analog Comparator 3<br>Positive Input | Analog                                   | --                                |
| 14                 | IO11     | IO11        | General Purpose IO<br>with OE [1]     | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)               |
|                    |          |             |                                       | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x)      |
|                    |          |             |                                       | Low Voltage Digital Input                |                                   |
|                    |          | ACMP2-      | Analog Comparator 2<br>Negative Input | Analog                                   |                                   |
|                    |          | ACMP3-      | Analog Comparator 3<br>Negative Input | Analog                                   |                                   |
| 15                 | IO12     | IO12        | General Purpose IO                    | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)               |
|                    |          |             |                                       | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x)      |
|                    |          |             |                                       | Low Voltage Digital Input                | Open-Drain PMOS<br>(1x) (2x)      |
|                    |          | ACMP3+      | Analog Comparator 3<br>Positive Input | Analog                                   | --                                |

Table 3. Functional Pin Description (Cont.)

| STQFN<br>20L Pin # | Pin Name | Signal Name       | Function                          | Input Options                            | Output Options               |
|--------------------|----------|-------------------|-----------------------------------|------------------------------------------|------------------------------|
| 16                 | IO13     | IO13              | General Purpose IO<br>with OE [1] | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)          |
|                    |          |                   |                                   | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x) |
|                    |          |                   |                                   | Low Voltage Digital Input                | --                           |
| 17                 | IO14     | IO14              | General Purpose IO                | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)          |
|                    |          |                   |                                   | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x) |
|                    |          |                   |                                   | Low Voltage Digital Input                | Open-Drain PMOS<br>(1x) (2x) |
|                    |          | EXT_CLK0          | External Clock<br>Connection 0    | Digital Input without<br>Schmitt Trigger | --                           |
|                    |          |                   |                                   | Digital Input<br>with Schmitt Trigger    | --                           |
|                    |          |                   |                                   | Low Voltage Digital Input                | --                           |
| 18                 | IO15     | IO15              | General Purpose IO<br>with OE [1] | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)          |
|                    |          |                   |                                   | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x) |
|                    |          |                   |                                   | Low Voltage<br>Digital Input             | --                           |
|                    |          | V <sub>REF1</sub> | Voltage Reference 1<br>Output     | --                                       | Analog                       |
|                    |          | EXT_CLK1          | External Clock<br>Connection 1    | Digital Input without<br>Schmitt Trigger | --                           |
|                    |          |                   |                                   | Digital Input<br>with Schmitt Trigger    | --                           |
|                    |          |                   |                                   | Low Voltage Digital Input                | --                           |
| 19                 | IO16     | IO16              | General Purpose IO<br>with OE [1] | Digital Input without<br>Schmitt Trigger | Push-Pull (1x) (2x)          |
|                    |          |                   |                                   | Digital Input<br>with Schmitt Trigger    | Open-Drain NMOS<br>(1x) (2x) |
|                    |          |                   |                                   | Low Voltage Digital Input                | --                           |
|                    |          | V <sub>REF0</sub> | Voltage Reference 0 Output        | --                                       | Analog                       |

Table 3. Functional Pin Description (Cont.)

| STQFN<br>20L Pin #                                                                                                                                     | Pin Name | Signal Name | Function                    | Input Options                         | Output Options            |
|--------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------|-----------------------------|---------------------------------------|---------------------------|
| 20                                                                                                                                                     | IO17     | IO17        | General Purpose IO          | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x)       |
|                                                                                                                                                        |          |             |                             | Digital Input with Schmitt Trigger    | Open-Drain NMOS (1x) (2x) |
|                                                                                                                                                        |          |             |                             | Low Voltage Digital Input             | Open-Drain PMOS (1x) (2x) |
|                                                                                                                                                        |          | EXT_CLK2    | External Clock Connection 2 | Digital Input without Schmitt Trigger | --                        |
|                                                                                                                                                        |          |             |                             | Digital Input with Schmitt Trigger    | --                        |
|                                                                                                                                                        |          |             |                             | Low Voltage Digital Input             | --                        |
| [1] General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure. |          |             |                             |                                       |                           |

### 3. Specifications

#### 3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

| Parameter                                  |                                      | Min       | Max                        | Unit               |
|--------------------------------------------|--------------------------------------|-----------|----------------------------|--------------------|
| Supply voltage on $V_{DD}$ relative to GND |                                      | -0.5      | 7.0                        | V                  |
| DC Input voltage                           | IOs 0, 6, 7                          | GND - 0.5 | 7.0                        | V                  |
|                                            | IOs 1-5, 8, 10-17                    |           | $V_{DD} + 0.5$ , up to 7.0 |                    |
| $V_{DD}$ DC Current                        | $T_J = +85\text{ }^{\circ}\text{C}$  | --        | 45                         | mA                 |
|                                            | $T_J = +110\text{ }^{\circ}\text{C}$ | --        | 22                         | mA                 |
| GND DC Current                             | $T_J = +85\text{ }^{\circ}\text{C}$  | --        | 86                         | mA                 |
|                                            | $T_J = +110\text{ }^{\circ}\text{C}$ | --        | 41                         | mA                 |
| GPIO DC Current<br>(Through pin)           | Push-Pull 1x                         | --        | 11                         | mA                 |
|                                            | Push-Pull 2x                         | --        | 16                         |                    |
|                                            | OD 1x                                | --        | 11                         |                    |
|                                            | OD 2x                                | --        | 21                         |                    |
|                                            | OD 4x                                | --        | 43                         |                    |
| Current at Input Pin                       |                                      | -1.0      | 1.0                        | mA                 |
| Storage Temperature Range                  |                                      | -65       | +150                       | $^{\circ}\text{C}$ |
| Junction Temperature                       |                                      | --        | +150                       | $^{\circ}\text{C}$ |
| Moisture Sensitivity Level                 |                                      | 1         |                            |                    |

## 3.2 Electrostatic Discharge Ratings

| Parameter                             | Min  | Max | Unit |
|---------------------------------------|------|-----|------|
| ESD Protection (Human Body Model)     | 2000 | --  | V    |
| ESD Protection (Charged Device Model) | 1300 | --  | V    |

## 3.3 Recommended Operating Conditions

| Parameter                                                  | Condition                              | Min  | Max      | Unit |
|------------------------------------------------------------|----------------------------------------|------|----------|------|
| Supply Voltage ( $V_{DD}$ )                                |                                        | 1.71 | 5.5      | V    |
| Operating Ambient Temperature Range                        |                                        | -40  | +105     | °C   |
| Maximal Voltage Applied to any PIN in High Impedance State |                                        | --   | $V_{DD}$ | V    |
| Capacitor Value at $V_{DD}$                                |                                        | 0.1  | --       | μF   |
| Analog Input Common Mode Range                             | Allowable Input Voltage at Analog Pins | 0    | $V_{DD}$ | V    |

## 3.4 Electrical Specifications

### 3.4.1 Logic IO Specifications

$T_A = -40\text{ °C}$  to  $+105\text{ °C}$ ,  $V_{DD} = 1.71\text{ V}$  to  $5.5\text{ V}$ , unless otherwise noted.

| Parameter                          | Symbol     | Condition                                                          | Min                  | Typ                  | Max                  | Unit |
|------------------------------------|------------|--------------------------------------------------------------------|----------------------|----------------------|----------------------|------|
| ACMP Input Voltage Range           | $V_{ACMP}$ | Positive Input                                                     | 0                    | --                   | $V_{DD}$             | V    |
|                                    |            | Negative Input                                                     | 0                    | --                   | 1.2                  | V    |
| HIGH-Level Input Voltage           | $V_{IH}$   | Logic Input [1]                                                    | $0.7 \times V_{DD}$  | --                   | $V_{DD} + 0.3$       | V    |
|                                    |            | Logic Input with Schmitt Trigger                                   | $0.8 \times V_{DD}$  | --                   | $V_{DD} + 0.3$       | V    |
|                                    |            | Low-Level Logic Input [1]                                          | 1.25                 | --                   | $V_{DD} + 0.3$       | V    |
| LOW-Level Input Voltage            | $V_{IL}$   | Logic Input [1]                                                    | GND - 0.3            | --                   | $0.3 \times V_{DD}$  | V    |
|                                    |            | Logic Input with Schmitt Trigger                                   | GND - 0.3            | --                   | $0.2 \times V_{DD}$  | V    |
|                                    |            | Low-Level Logic Input [1]                                          | GND - 0.3            | --                   | 0.5                  | V    |
| Schmitt Trigger Hysteresis Voltage | $V_{HYS}$  | Logic Input with Schmitt Trigger, $V_{DD} = 1.8\text{ V} \pm 5\%$  | $0.19 \times V_{DD}$ | $0.26 \times V_{DD}$ | $0.31 \times V_{DD}$ | V    |
|                                    |            | Logic Input with Schmitt Trigger, $V_{DD} = 3.3\text{ V} \pm 10\%$ | $0.16 \times V_{DD}$ | $0.21 \times V_{DD}$ | $0.26 \times V_{DD}$ | V    |
|                                    |            | Logic Input with Schmitt Trigger, $V_{DD} = 5.0\text{ V} \pm 10\%$ | $0.15 \times V_{DD}$ | $0.18 \times V_{DD}$ | $0.22 \times V_{DD}$ | V    |
| Input leakage (Absolute Value)     | $I_{LKG}$  |                                                                    | --                   | --                   | 1000                 | nA   |

| Parameter                 | Symbol   | Condition                                                                   | Min                   | Typ                   | Max                   | Unit |
|---------------------------|----------|-----------------------------------------------------------------------------|-----------------------|-----------------------|-----------------------|------|
| HIGH-Level Output Voltage | $V_{OH}$ | Push-Pull, $I_{OH} = 100 \mu A$ , 1x Drive, $V_{DD} = 1.8 V \pm 5 \%$       | $0.992 \times V_{DD}$ | $0.994 \times V_{DD}$ | --                    | V    |
|                           |          | Push-Pull, $I_{OH} = 3 mA$ , 1x Drive, $V_{DD} = 3.3 V \pm 10 \%$           | $0.931 \times V_{DD}$ | $0.948 \times V_{DD}$ | --                    | V    |
|                           |          | Push-Pull, $I_{OH} = 5 mA$ , 1x Drive, $V_{DD} = 5.0 V \pm 10 \%$           | $0.945 \times V_{DD}$ | $0.958 \times V_{DD}$ | --                    | V    |
|                           |          | PMOS OD, $I_{OH} = 100 \mu A$ , 1x Drive, $V_{DD} = 1.8 V \pm 5 \%$         | $0.992 \times V_{DD}$ | $0.99 \times V_{DD}$  | --                    | V    |
|                           |          | PMOS OD, $I_{OH} = 3 mA$ , 1x Drive, $V_{DD} = 3.3 V \pm 10 \%$             | $0.931 \times V_{DD}$ | $0.95 \times V_{DD}$  | --                    | V    |
|                           |          | PMOS OD, $I_{OH} = 5 mA$ , 1x Drive, $V_{DD} = 5.0 V \pm 10 \%$             | $0.945 \times V_{DD}$ | $0.96 \times V_{DD}$  | --                    | V    |
|                           |          | Push-Pull, $I_{OH} = 100 \mu A$ , 2x Drive, $V_{DD} = 1.8 V \pm 5 \%$       | $0.996 \times V_{DD}$ | $0.997 \times V_{DD}$ | --                    | V    |
|                           |          | Push-Pull, $I_{OH} = 3 mA$ , 2x Drive, $V_{DD} = 3.3 V \pm 10 \%$           | $0.966 \times V_{DD}$ | $0.974 \times V_{DD}$ | --                    | V    |
|                           |          | Push-Pull, $I_{OH} = 5 mA$ , 2x Drive, $V_{DD} = 5.0 V \pm 10 \%$           | $0.972 \times V_{DD}$ | $0.979 \times V_{DD}$ | --                    | V    |
|                           |          | PMOS OD, $I_{OH} = 100 \mu A$ , 2x Drive, $V_{DD} = 1.8 V \pm 5 \%$         | $0.996 \times V_{DD}$ | $0.997 \times V_{DD}$ | --                    | V    |
|                           |          | PMOS OD, $I_{OH} = 3 mA$ , 2x Drive, $V_{DD} = 3.3 V \pm 10 \%$             | $0.966 \times V_{DD}$ | $0.974 \times V_{DD}$ | --                    | V    |
|                           |          | PMOS OD, $I_{OH} = 5 mA$ , 2x Drive, $V_{DD} = 5.0 V \pm 10 \%$             | $0.972 \times V_{DD}$ | $0.979 \times V_{DD}$ | --                    | V    |
| LOW-Level Output Voltage  | $V_{OL}$ | Push-Pull, $I_{OL} = 100 \mu A$ , 1x Drive, $V_{DD} = 1.8 V \pm 5 \%$       | --                    | $0.004 \times V_{DD}$ | $0.006 \times V_{DD}$ | V    |
|                           |          | Push-Pull, $I_{OL} = 3 mA$ , 1x Drive, $V_{DD} = 3.3 V \pm 10 \%$           | --                    | $0.038 \times V_{DD}$ | $0.054 \times V_{DD}$ | V    |
|                           |          | Push-Pull, $I_{OL} = 5 mA$ , 1x Drive, $V_{DD} = 5.0 V \pm 10 \%$           | --                    | $0.033 \times V_{DD}$ | $0.046 \times V_{DD}$ | V    |
|                           |          | Push-Pull, $I_{OL} = 100 \mu A$ , 2x Drive, $V_{DD} = 1.8 V \pm 5 \%$       | --                    | $0.002 \times V_{DD}$ | $0.003 \times V_{DD}$ | V    |
|                           |          | Push-Pull, $I_{OL} = 3 mA$ , 2x Drive, $V_{DD} = 3.3 V \pm 10 \%$           | --                    | $0.019 \times V_{DD}$ | $0.026 \times V_{DD}$ | V    |
|                           |          | Push-Pull, $I_{OL} = 5 mA$ , 2x Drive, $V_{DD} = 5.0 V \pm 10 \%$           | --                    | $0.017 \times V_{DD}$ | $0.023 \times V_{DD}$ | V    |
|                           |          | NMOS Open-Drain, $I_{OL} = 100 \mu A$ , 1x Drive, $V_{DD} = 1.8 V \pm 5 \%$ | --                    | $0.003 \times V_{DD}$ | $0.004 \times V_{DD}$ | V    |
|                           |          | NMOS Open-Drain, $I_{OL} = 3 mA$ , 1x Drive, $V_{DD} = 3.3 V \pm 10 \%$     | --                    | $0.025 \times V_{DD}$ | $0.035 \times V_{DD}$ | V    |
|                           |          | NMOS Open-Drain, $I_{OL} = 5 mA$ , 1x Drive, $V_{DD} = 5.0 V \pm 10 \%$     | --                    | $0.022 \times V_{DD}$ | $0.03 \times V_{DD}$  | V    |
|                           |          | NMOS Open-Drain, $I_{OL} = 100 \mu A$ , 2x Drive, $V_{DD} = 1.8 V \pm 5 \%$ | --                    | $0.002 \times V_{DD}$ | $0.002 \times V_{DD}$ | V    |

| Parameter                           | Symbol   | Condition                                                                                    | Min    | Typ                   | Max                   | Unit |
|-------------------------------------|----------|----------------------------------------------------------------------------------------------|--------|-----------------------|-----------------------|------|
| LOW-Level Output Voltage            | $V_{OL}$ | NMOS Open-Drain, $I_{OL} = 3 \text{ mA}$ , 2x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$      | --     | $0.013 \times V_{DD}$ | $0.018 \times V_{DD}$ | V    |
|                                     |          | NMOS Open-Drain, $I_{OL} = 5 \text{ mA}$ , 2x Drive, $V_{DD} = 5.0 \text{ V} \pm 10 \%$      | --     | $0.011 \times V_{DD}$ | $0.015 \times V_{DD}$ | V    |
|                                     |          | Open-Drain NMOS 4x, IOs 8, 9, $I_{OL} = 100 \mu\text{A}$ , $V_{DD} = 1.8 \text{ V} \pm 5 \%$ | --     | $0.001 \times V_{DD}$ | $0.001 \times V_{DD}$ | V    |
|                                     |          | Open-Drain NMOS 4x, IOs 8, 9, $I_{OL} = 3 \text{ mA}$ , $V_{DD} = 3.3 \text{ V} \pm 10 \%$   | --     | $0.007 \times V_{DD}$ | $0.009 \times V_{DD}$ | V    |
|                                     |          | Open-Drain NMOS 4x, IOs 8, 9, $I_{OL} = 5 \text{ mA}$ , $V_{DD} = 5.0 \text{ V} \pm 10 \%$   | --     | $0.006 \times V_{DD}$ | $0.008 \times V_{DD}$ | V    |
| HIGH-Level Output Pulse Current [2] | $I_{OH}$ | Push-Pull, $V_{OH} = V_{DD} - 0.2$ , 1x Drive, $V_{DD} = 1.8 \text{ V} \pm 5 \%$             | 0.963  | 1.331                 | --                    | mA   |
|                                     |          | Push-Pull, $V_{OH} = 2.4 \text{ V}$ , 1x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$           | 5.219  | 12.234                | --                    | mA   |
|                                     |          | Push-Pull, $V_{OH} = 2.4 \text{ V}$ , 1x Drive, $V_{DD} = 5.0 \text{ V} \pm 10 \%$           | 19.403 | 32.766                | --                    | mA   |
|                                     |          | PMOS OD, $V_{OH} = V_{DD} - 0.2$ , 1x Drive, $V_{DD} = 1.8 \text{ V} \pm 5 \%$               | 0.973  | 1.331                 | --                    | mA   |
|                                     |          | PMOS OD, $V_{OH} = 2.4 \text{ V}$ , 1x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$             | 5.243  | 12.234                | --                    | mA   |
|                                     |          | PMOS OD, $V_{OH} = 2.4 \text{ V}$ , 1x Drive, $V_{DD} = 5.0 \text{ V} \pm 10 \%$             | 19.478 | 32.771                | --                    | mA   |
|                                     |          | Push-Pull, $V_{OH} = V_{DD} - 0.2$ , 2x Drive, $V_{DD} = 1.8 \text{ V} \pm 5 \%$             | 1.902  | 2.642                 | --                    | mA   |
|                                     |          | Push-Pull, $V_{OH} = 2.4 \text{ V}$ , 2x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$           | 10.29  | 24.137                | --                    | mA   |
|                                     |          | Push-Pull, $V_{OH} = 2.4 \text{ V}$ , 2X Drive, $V_{DD} = 5.0 \text{ V} \pm 10 \%$           | 37.967 | 64.23                 | --                    | mA   |
|                                     |          | PMOS OD, $V_{OH} = V_{DD} - 0.2$ , 2x Drive, $V_{DD} = 1.8 \text{ V} \pm 5 \%$               | 1.926  | 3.643                 | --                    | mA   |
|                                     |          | PMOS OD, $V_{OH} = 2.4 \text{ V}$ , 2x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$             | 10.389 | 24.148                | --                    | mA   |
|                                     |          | PMOS OD, $V_{OH} = 2.4 \text{ V}$ , 2x Drive, $V_{DD} = 5.0 \text{ V} \pm 10 \%$             | 38.275 | 64.275                | --                    | mA   |
| LOW-Level Output Pulse Current [2]  | $I_{OL}$ | Push-Pull, $V_{OL} = 0.15 \text{ V}$ , 1x Drive, $V_{DD} = 1.8 \text{ V} \pm 5 \%$           | 0.92   | 1.562                 | --                    | mA   |
|                                     |          | Push-Pull, $V_{OL} = 0.4 \text{ V}$ , 1x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$           | 4.769  | 7.847                 | --                    | mA   |
|                                     |          | Push-Pull, $V_{OL} = 0.4 \text{ V}$ , 1x Drive, $V_{DD} = 5.0 \text{ V} \pm 10 \%$           | 6.364  | 10.359                | --                    | mA   |
|                                     |          | Push-Pull, $V_{OL} = 0.15 \text{ V}$ , 2x Drive, $V_{DD} = 1.8 \text{ V} \pm 5 \%$           | 1.83   | 3.114                 | --                    | mA   |
|                                     |          | Push-Pull, $V_{OL} = 0.4 \text{ V}$ , 2x Drive, $V_{DD} = 3.3 \text{ V} \pm 10 \%$           | 9.537  | 15.515                | --                    | mA   |

| Parameter                          | Symbol       | Condition                                                                                | Min    | Typ    | Max   | Unit       |
|------------------------------------|--------------|------------------------------------------------------------------------------------------|--------|--------|-------|------------|
| LOW-Level Output Pulse Current [2] | $I_{OL}$     | Push-Pull, $V_{OL} = 0.4\text{ V}$ , 2x Drive, $V_{DD} = 5.0\text{ V} \pm 10\%$          | 12.669 | 20.367 | --    | mA         |
|                                    |              | NMOS Open-Drain, $V_{OL} = 0.15\text{ V}$ , 1x Drive, $V_{DD} = 1.8\text{ V} \pm 5\%$    | 1.38   | 2.37   | --    | mA         |
|                                    |              | NMOS Open-Drain, $V_{OL} = 0.4\text{ V}$ , 1x Drive, $V_{DD} = 3.3\text{ V} \pm 10\%$    | 7.31   | 11.873 | --    | mA         |
|                                    |              | NMOS Open-Drain, $V_{OL} = 0.4\text{ V}$ , 1X Drive, $V_{DD} = 5.0\text{ V} \pm 10\%$    | 9.825  | 15.654 | --    | mA         |
|                                    |              | NMOS Open-Drain, $V_{OL} = 0.15\text{ V}$ , 2x Drive, $V_{DD} = 1.8\text{ V} \pm 5\%$    | 2.75   | 4.644  | --    | mA         |
|                                    |              | NMOS Open-Drain, $V_{OL} = 0.4\text{ V}$ , 2x Drive, $V_{DD} = 3.3\text{ V} \pm 10\%$    | 14.472 | 22.973 | --    | mA         |
|                                    |              | NMOS Open-Drain, $V_{OL} = 0.4\text{ V}$ , 2X Drive, $V_{DD} = 5.0\text{ V} \pm 10\%$    | 17.34  | 30.033 | --    | mA         |
|                                    |              | Open-Drain NMOS 4x, IOs 8, 9, $V_{OL} = 0.15\text{ V}$ , $V_{DD} = 1.8\text{ V} \pm 5\%$ | 6.897  | 9.202  | --    | mA         |
|                                    |              | Open-Drain NMOS 4x, IOs 8, 9, $V_{OL} = 0.4\text{ V}$ , $V_{DD} = 3.3\text{ V} \pm 10\%$ | 28.502 | 45.065 | --    | mA         |
|                                    |              | Open-Drain NMOS 4x, IOs 8, 9, $V_{OL} = 0.4\text{ V}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$ | 37.33  | 58.499 | --    | mA         |
| Startup Time                       | $T_{SU}$     | From $V_{DD}$ rising past $PON_{THR}$                                                    | 0.61   | 1.311  | 1.913 | ms         |
| Power-On Threshold                 | $PON_{THR}$  | $V_{DD}$ Level Required to Start Up the Chip                                             | 0.852  | 1.553  | 1.715 | V          |
| Power-Off Threshold                | $POFF_{THR}$ | $V_{DD}$ Level Required to Switch Off the Chip                                           | 0.879  | 1.167  | 1.405 | V          |
| Pull-up or Pull-down Resistance    | $R_{PULL}$   | 1 M $\Omega$ Pull-up: $V_{IN} = GND$ ,<br>1 M $\Omega$ Pull-down: $V_{IN} = V_{DD}$      | --     | 1000   | --    | k $\Omega$ |
|                                    |              | 100 k $\Omega$ Pull-up: $V_{IN} = GND$ ,<br>100 k $\Omega$ Pull-down: $V_{IN} = V_{DD}$  | --     | 100    | --    | k $\Omega$ |
|                                    |              | 10 k $\Omega$ Pull-up: $V_{IN} = GND$ ,<br>10 k $\Omega$ Pull-down: $V_{IN} = V_{DD}$    | --     | 10     | --    | k $\Omega$ |
| Input Capacitance                  | $C_{IN}$     |                                                                                          | --     | 4      | --    | pF         |

[1] No hysteresis.

[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

### 3.4.2 I<sup>2</sup>C Pins Electrical Specifications

$T_A = -40\text{ }^{\circ}\text{C}$  to  $105\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.71\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

| Parameter                                                                                                                                       | Symbol              | Condition                                                         | Fast-Mode              |                       | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------------------------------------------------------------------|------------------------|-----------------------|------|
|                                                                                                                                                 |                     |                                                                   | Min                    | Max                   |      |
| IO Stage                                                                                                                                        |                     |                                                                   |                        |                       |      |
| LOW-level Input Voltage                                                                                                                         | V <sub>IL</sub>     |                                                                   | -0.5                   | 0.3 x V <sub>DD</sub> | V    |
| HIGH-level Input Voltage                                                                                                                        | V <sub>IH</sub>     |                                                                   | 0.7 x V <sub>DD</sub>  | V <sub>DD</sub> + 0.5 | V    |
| Hysteresis of Schmitt Trigger Inputs                                                                                                            | V <sub>HYS</sub>    |                                                                   | 0.05 x V <sub>DD</sub> | --                    | V    |
| LOW-Level Output Voltage 1                                                                                                                      | V <sub>OL1</sub>    | (Open-Drain) at 3 mA sink current, V <sub>DD</sub> > 2 V          | 0                      | 0.4                   | V    |
| LOW-Level Output Voltage 2                                                                                                                      | V <sub>OL2</sub>    | (Open-Drain) at 2 mA sink current, V <sub>DD</sub> ≤ 2 V          | 0                      | 0.2 x V <sub>DD</sub> | V    |
| LOW-Level Output Current                                                                                                                        | I <sub>OL</sub>     | V <sub>OL</sub> = 0.4 V                                           | 3                      | --                    | mA   |
|                                                                                                                                                 |                     | V <sub>OL</sub> = 0.6 V                                           | 6                      | --                    | mA   |
| Output Fall Time from V <sub>IHmin</sub> to V <sub>ILmax</sub> [1]                                                                              | t <sub>of</sub>     |                                                                   | 0.3                    | 250                   | ns   |
| Pulse Width of Spikes that must be suppressed by the Input Filter                                                                               | t <sub>SP</sub>     | SDA line                                                          | 0                      | 50                    | ns   |
|                                                                                                                                                 |                     | SCL line                                                          | 0                      | 20 [1]                |      |
| Input Current Each IO Pin                                                                                                                       | I <sub>i</sub>      | 0.1 x V <sub>DD</sub> < V <sub>I</sub> < 0.9 x V <sub>DDmax</sub> | -10                    | +10                   | μA   |
| Capacitance for Each IO Pin                                                                                                                     | C <sub>i</sub>      |                                                                   | --                     | 10                    | pF   |
| Timing (see Figure 96 for Diagram)                                                                                                              |                     |                                                                   |                        |                       |      |
| Clock Frequency, SCL                                                                                                                            | F <sub>SCL</sub>    |                                                                   | --                     | 400                   | kHz  |
| Clock Pulse Width Low                                                                                                                           | t <sub>LOW</sub>    |                                                                   | 1300                   | --                    | ns   |
| Clock Pulse Width High                                                                                                                          | t <sub>HIGH</sub>   |                                                                   | 600                    | --                    | ns   |
| Data Valid Acknowledge Time                                                                                                                     | t <sub>VD_ACK</sub> |                                                                   | --                     | 900                   | ns   |
| Data Valid Time                                                                                                                                 | t <sub>VD_DAT</sub> |                                                                   | --                     | 900                   | ns   |
| Bus Free Time between Stop and Start                                                                                                            | t <sub>BUF</sub>    |                                                                   | 1300                   | --                    | ns   |
| Start Hold Time                                                                                                                                 | t <sub>HD_STA</sub> |                                                                   | 600                    | --                    | ns   |
| Start Set-up Time                                                                                                                               | t <sub>SU_STA</sub> |                                                                   | 600                    | --                    | ns   |
| Data Hold Time                                                                                                                                  | t <sub>HD_DAT</sub> |                                                                   | 0                      | --                    | ns   |
| Data Set-up Time                                                                                                                                | t <sub>SU_DAT</sub> |                                                                   | 100                    | --                    | ns   |
| Inputs Rise Time                                                                                                                                | t <sub>R</sub>      |                                                                   | --                     | 300                   | ns   |
| Inputs Fall Time                                                                                                                                | t <sub>F</sub>      |                                                                   | --                     | 300                   | ns   |
| Stop Set-up Time                                                                                                                                | t <sub>SU_STO</sub> |                                                                   | 600                    | --                    | ns   |
| Data Out Hold Time                                                                                                                              | t <sub>DH</sub>     |                                                                   | 50                     | --                    | ns   |
| [1] Does not meet standard I <sup>2</sup> C specifications: t <sub>of</sub> = 20x(V <sub>DD</sub> /5.5 V) (min), t <sub>SP</sub> = 50 ns (max). |                     |                                                                   |                        |                       |      |

### 3.4.3 Macrocells Current Consumption

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Parameter | Symbol   | Note                         | $V_{DD} = 1.8\text{ V}$ | $V_{DD} = 3.3\text{ V}$ | $V_{DD} = 5.0\text{ V}$ | Unit          |
|-----------|----------|------------------------------|-------------------------|-------------------------|-------------------------|---------------|
| Current   | $I_{DD}$ | Chip Quiescent, $I_{DD}$     | 0.28                    | 0.52                    | 0.81                    | $\mu\text{A}$ |
|           |          | OSC 2 MHz, pre-divide = 1    | 32.73                   | 50.92                   | 76.79                   |               |
|           |          | OSC 2 MHz, pre-divide = 8    | 19.36                   | 24.90                   | 34.48                   |               |
|           |          | OSC 25 kHz, pre-divide = 1   | 5.39                    | 6.11                    | 7.34                    |               |
|           |          | OSC 25 kHz, pre-divide = 8   | 5.23                    | 5.79                    | 6.84                    |               |
|           |          | OSC 25 MHz, pre-divide = 1   | 76.84                   | 204.45                  | 375.54                  |               |
|           |          | OSC 25 MHz, pre-divide = 8   | 68.18                   | 181.65                  | 341.65                  |               |
|           |          | ACMP (each)                  | 47.22                   | 43.87                   | 51.98                   |               |
|           |          | ACMP with buffer (each)      | 62.46                   | 59.52                   | 68.18                   |               |
|           |          | $V_{REF}$ (each)             | 43.19                   | 39.78                   | 47.88                   |               |
|           |          | $V_{REF}$ with buffer (each) | 51.88                   | 48.80                   | 57.08                   |               |

### 3.4.4 Estimated Typical Delay of Each Macrocell

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Parameter              | Symbol          | Note                                        | V <sub>DD</sub> = 1.8 V |         | V <sub>DD</sub> = 3.3 V |         | V <sub>DD</sub> = 5.0 V |         | Unit |
|------------------------|-----------------|---------------------------------------------|-------------------------|---------|-------------------------|---------|-------------------------|---------|------|
|                        |                 |                                             | Rising                  | Falling | Rising                  | Falling | Rising                  | Falling |      |
| GPI and GPIO Macrocell |                 |                                             |                         |         |                         |         |                         |         |      |
| Propagation Delay      | t <sub>PD</sub> | Digital Input to PP 1x                      | 46                      | 48      | 20                      | 20      | 14                      | 15      | ns   |
|                        |                 | Digital Input with Schmitt Trigger to PP 1x | 45                      | 47      | 19                      | 20      | 14                      | 14      |      |
|                        |                 | Low Voltage Digital input to PP 1x          | 51                      | 468     | 23                      | 186     | 18                      | 120     |      |
|                        |                 | Digital input to PMOS output                | 41                      | -       | 18                      | -       | 13                      | -       |      |
|                        |                 | Digital input to NMOS output                | -                       | 78      | -                       | 29      | -                       | 19      |      |
|                        |                 | Output enable from pin, OE Hi-Z to 1        | 46                      | -       | 19                      | -       | 14                      | -       |      |
|                        |                 | Output enable from pin, OE Hi-Z to 0        | 43                      | -       | 19                      | -       | 14                      | -       |      |
| Pulse Width            | t <sub>W</sub>  | IO with 1x Push-Pull (min transmitted)      | 20                      | 20      | 20                      | 20      | 20                      | 20      | ns   |

| Parameter                      | Symbol          | Note                                  | V <sub>DD</sub> = 1.8 V |         | V <sub>DD</sub> = 3.3 V |         | V <sub>DD</sub> = 5.0 V |         | Unit |
|--------------------------------|-----------------|---------------------------------------|-------------------------|---------|-------------------------|---------|-------------------------|---------|------|
|                                |                 |                                       | Rising                  | Falling | Rising                  | Falling | Rising                  | Falling |      |
| Combination Function Macrocell |                 |                                       |                         |         |                         |         |                         |         |      |
| Propagation Delay              | t <sub>PD</sub> | 2-bit LUT (LATCH)                     | 34                      | 34      | 14                      | 13      | 10                      | 9       | ns   |
|                                |                 | LATCH (2-bit LUT)                     | 30                      | 32      | 12                      | 13      | 9                       | 9       |      |
|                                |                 | 3-bit LUT(LATCH)                      | 31                      | 33      | 13                      | 13      | 9                       | 9       |      |
|                                |                 | LATCH+nRESET(3-bit LUT)               | 37                      | 36      | 15                      | 14      | 11                      | 10      |      |
|                                |                 | 4-bit LUT                             | 29                      | 35      | 12                      | 13      | 9                       | 9       |      |
|                                |                 | 2-bit LUT                             | 30                      | 32      | 12                      | 13      | 9                       | 9       |      |
|                                |                 | 3-bit LUT                             | 31                      | 33      | 13                      | 13      | 9                       | 9       |      |
|                                |                 | CNT/DLY Logic                         | 60                      | 60      | 25                      | 25      | 17                      | 17      |      |
| Programmable Delay             |                 |                                       |                         |         |                         |         |                         |         |      |
| Propagation Delay              | t <sub>PD</sub> | P_DLY1C                               | 377                     | 369     | 167                     | 164     | 123                     | 121     | ns   |
|                                |                 | P_DLY2C                               | 689                     | 682     | 309                     | 305     | 229                     | 226     |      |
|                                |                 | P_DLY3C                               | 1002                    | 995     | 450                     | 447     | 334                     | 331     |      |
|                                |                 | P_DLY4C                               | 1311                    | 1303    | 590                     | 586     | 438                     | 435     |      |
| Pipe Delay                     |                 |                                       |                         |         |                         |         |                         |         |      |
| Propagation Delay              | t <sub>PD</sub> | Pipe Delay OUT0                       | 48                      | 42      | 20                      | 18      | 14                      | 13      | ns   |
|                                |                 | Pipe Delay OUT1                       | 45                      | 39      | 19                      | 16      | 13                      | 12      |      |
| Filter/Edge Detector           |                 |                                       |                         |         |                         |         |                         |         |      |
| Propagation Delay              | t <sub>PD</sub> | Filter 0                              | 225                     | 205     | 86                      | 80      | 56                      | 52      | ns   |
|                                |                 | Filter 1                              | 175                     | 156     | 66                      | 61      | 43                      | 40      |      |
|                                |                 | Mode: Edge Detect 0, Any Edge Detect  | 59                      | 63      | 23                      | 24      | 16                      | 16      |      |
|                                |                 | Mode: Edge Detect 1, Any Edge Detect  | 58                      | 62      | 23                      | 23      | 16                      | 16      |      |
|                                |                 | Mode: Edge Detect 0, BothEdge Detect  | 378                     | 366     | 167                     | 162     | 123                     | 120     |      |
|                                |                 | Mode: Edge Detect 1, Both Edge Detect | 377                     | 364     | 166                     | 162     | 122                     | 119     |      |
| ACMP                           |                 |                                       |                         |         |                         |         |                         |         |      |
| Propagation Delay              | t <sub>PD</sub> | ACMP (5 mV overdrive, IN- = 600 mV)   | 3000                    | 3000    | 2000                    | 2000    | 2000                    | 2000    | ns   |

### 3.4.5 Programmable Delay Typical Delays and Widths

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Parameter   | Symbol     | Note                                        |        | $V_{DD} = 1.8\text{ V}$ | $V_{DD} = 3.3\text{ V}$ | $V_{DD} = 5.0\text{ V}$ | Unit |
|-------------|------------|---------------------------------------------|--------|-------------------------|-------------------------|-------------------------|------|
| Pulse Width | $t_w$      | Mode: (any) Edge Detect, Edge Detect Output | 1-Cell | 309                     | 139                     | 103                     | ns   |
|             |            |                                             | 2-Cell | 621                     | 280                     | 209                     |      |
|             |            |                                             | 3-Cell | 934                     | 422                     | 314                     |      |
|             |            |                                             | 4-Cell | 1243                    | 562                     | 418                     |      |
| Delay Time  | $t_{DLY1}$ | Mode: (any) Edge Detect, Edge Detect Output | 1-Cell | 55                      | 22                      | 15                      | ns   |
|             |            |                                             | 2-Cell | 55                      | 22                      | 15                      |      |
|             |            |                                             | 3-Cell | 55                      | 22                      | 15                      |      |
|             |            |                                             | 4-Cell | 55                      | 22                      | 15                      |      |
|             | $t_{DLY2}$ | Mode: Both Edge Delay, Edge Detect Output   | 1-Cell | 373                     | 165                     | 122                     | ns   |
|             |            |                                             | 2-Cell | 685                     | 307                     | 227                     |      |
|             |            |                                             | 3-Cell | 998                     | 448                     | 332                     |      |
|             |            |                                             | 4-Cell | 1307                    | 588                     | 437                     |      |

### 3.4.6 Typical Filter Rejection Pulse Width

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Parameter                         | $V_{DD} = 1.8\text{ V}$ | $V_{DD} = 3.3\text{ V}$ | $V_{DD} = 5.0\text{ V}$ | Unit |
|-----------------------------------|-------------------------|-------------------------|-------------------------|------|
| Filtered Pulse Width for Filter 0 | < 143                   | < 58                    | < 37                    | ns   |
| Filtered Pulse Width for Filter 1 | < 97                    | < 40                    | < 26                    | ns   |

### 3.4.7 Counter/Delay Specifications

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Parameter                            | OSC Freq         | OSC Power | $V_{DD} = 1.8\text{ V}$ | $V_{DD} = 3.3\text{ V}$ | $V_{DD} = 5.0\text{ V}$ | Unit          |
|--------------------------------------|------------------|-----------|-------------------------|-------------------------|-------------------------|---------------|
| Power-On Delay Time                  | 25 kHz           | Auto      | 1.6                     | 1.6                     | 1.6                     | $\mu\text{s}$ |
| Power-On Delay Time (Fast Start)     | 25 kHz           | Auto      | 2.1                     | 2.1                     | 2.1                     | $\mu\text{s}$ |
| Power-On Delay                       | 2 MHz            | Auto      | 0.4                     | 0.2                     | 0.2                     | $\mu\text{s}$ |
| Power-On Delay Time (Fast Start)     | 2 MHz            | Auto      | 0.7                     | 0.5                     | 0.4                     | $\mu\text{s}$ |
| Power-On Delay Time                  | 25 MHz           | Auto      | 0.01                    | 0.05                    | 0.04                    | $\mu\text{s}$ |
| Frequency settling time              | 25 kHz           | Auto      | 19                      | 14                      | 12                      | $\mu\text{s}$ |
|                                      | 2 MHz            | Auto      | 14                      | 14                      | 14                      | $\mu\text{s}$ |
| Variable (CLK period)                | 25 kHz           | Forced    | 0-40                    | 0-40                    | 0-40                    | $\mu\text{s}$ |
|                                      | 2 MHz            | Forced    | 0-0.5                   | 0-0.5                   | 0-0.5                   | $\mu\text{s}$ |
|                                      | 25 MHz           | Forced    | 0-0.04                  | 0-0.04                  | 0-0.04                  | $\mu\text{s}$ |
| Propagation Delay (Non-Delayed Edge) | 25 kHz/<br>2 MHz | Either    | 35                      | 14                      | 10                      | ns            |

### 3.4.8 25 kHz OSC0 Frequency Limits

| Power Supply Range<br>(V <sub>DD</sub> ), V | Temperature Range  |                    |                    |                    |                    |                    |
|---------------------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                                             | +25 °C             |                    | 0 °C to +105 °C    |                    | -40 °C to +105 °C  |                    |
|                                             | Minimum Value, kHz | Maximum Value, kHz | Minimum Value, kHz | Maximum Value, kHz | Minimum Value, kHz | Maximum Value, kHz |
| 1.8 V ±5 %                                  | 24.317             | 25.726             | 23.576             | 26.116             | 23.576             | 27.219             |
| 3.3 V ±10 %                                 | 24.495             | 25.66              | 23.6               | 25.934             | 23.6               | 26.399             |
| 5.0 V ±10 %                                 | 24.443             | 25.698             | 23.517             | 25.978             | 23.517             | 26.567             |
| 2.5 V to 4.5 V                              | 24.493             | 25.665             | 23.59              | 25.942             | 23.59              | 26.408             |
| 1.71 V to 5.5 V                             | 24.224             | 25.698             | 23.484             | 26.257             | 23.484             | 27.225             |

### 3.4.9 25 kHz OSC0 Frequency Error

| Power Supply Range<br>(V <sub>DD</sub> ), V | Temperature Range    |                      |                      |                      |                      |                      |
|---------------------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
|                                             | +25 °C               |                      | 0 °C to +105 °C      |                      | -40 °C to +105 °C    |                      |
|                                             | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) |
| 1.8 V ±5 %                                  | -2.732               | 2.904                | -10.7                | 6.92                 | -10.7                | 16.832               |
| 3.3 V ±10 %                                 | -2.02                | 2.64                 | -10.432              | 4.772                | -10.432              | 9.66                 |
| 5.0 V ±10 %                                 | -2.228               | 2.792                | -11.064              | 4.996                | -11.064              | 10.22                |
| 2.5 V to 4.5 V                              | -2.028               | 2.66                 | -10.588              | 4.844                | -10.588              | 9.848                |
| 1.71 V to 5.5 V                             | -3.104               | 3.872                | -11.536              | 6.904                | -11.536              | 16.728               |

### 3.4.10 2 MHz OSC0 Frequency Limits

| Power Supply Range<br>(V <sub>DD</sub> ), V | Temperature Range  |                    |                    |                    |                    |                    |
|---------------------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                                             | +25 °C             |                    | 0 °C to +105 °C    |                    | -40 °C to +105 °C  |                    |
|                                             | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz |
| 1.8 V ±5 %                                  | 1.903              | 2.098              | 1.856              | 2.104              | 1.856              | 2.115              |
| 3.3 V ±10 %                                 | 1.885              | 2.115              | 1.839              | 2.123              | 1.834              | 2.132              |
| 5.0 V ±10 %                                 | 1.858              | 2.220              | 1.821              | 2.230              | 1.803              | 2.252              |
| 2.5 V to 4.5 V                              | 1.874              | 2.123              | 1.835              | 2.129              | 1.819              | 2.137              |
| 1.71 V to 5.5 V                             | 1.811              | 2.249              | 1.779              | 2.260              | 1.623              | 2.283              |

### 3.4.11 2 MHz OSC0 Frequency Error

| Power Supply Range<br>(V <sub>DD</sub> ), V | Temperature Range    |                      |                      |                      |                      |                      |
|---------------------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
|                                             | +25 °C               |                      | 0 °C to +105 °C      |                      | -40 °C to +105 °C    |                      |
|                                             | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) |
| 1.8 V ±5 %                                  | -4.85                | 4.9                  | -9.15                | 5.7                  | -10.35               | 6.95                 |
| 3.3 V ±10 %                                 | -5.75                | 5.75                 | -9.0                 | 7.05                 | -11.4                | 7.65                 |
| 5.0 V ±10 %                                 | -7.1                 | 11.0                 | -10.85               | 12.8                 | -13.1                | 14.4                 |
| 2.5 V to 4.5 V                              | -6.3                 | 6.15                 | -9.6                 | 8.0                  | -13.75               | 8.2                  |
| 1.71 V to 5.5 V                             | -9.45                | 12.45                | -15.45               | 14.25                | -30.5                | 16.0                 |

### 3.4.12 25 MHz OSC1 Frequency Limits

| Power Supply Range<br>(V <sub>DD</sub> ), V | Temperature Range  |                    |                    |                    |                    |                    |
|---------------------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                                             | +25 °C             |                    | 0 °C to +105 °C    |                    | -40 °C to +105 °C  |                    |
|                                             | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz |
| 2.5 V ±10 %                                 | 22.964             | 26.443             | 21.759             | 26.828             | 21.759             | 27.327             |
| 3.3 V ±10 %                                 | 24.056             | 25.824             | 22.655             | 26.081             | 22.655             | 26.350             |
| 5.0 V ±10 %                                 | 23.860             | 25.894             | 22.832             | 26.215             | 22.832             | 26.714             |
| 2.5 V to 4.5 V                              | 22.232             | 25.824             | 21.386             | 26.081             | 21.386             | 26.350             |
| 1.71 V to 5.5 V                             | 14.130             | 25.824             | 13.718             | 26.081             | 13.028             | 26.350             |

### 3.4.13 25 MHz OSC1 Frequency Error

| Power Supply Range<br>(V <sub>DD</sub> ), V | Temperature Range    |                      |                      |                      |                      |                      |
|---------------------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
|                                             | +25 °C               |                      | 0 °C to +105 °C      |                      | -40 °C to +105 °C    |                      |
|                                             | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) |
| 2.5 V ±10 %                                 | -8.144               | 5.772                | -17.804              | 8.74                 | -17.804              | 13.04                |
| 3.3 V ±10 %                                 | -3.776               | 3.296                | -14.96               | 5.904                | -14.96               | 8.556                |
| 5.0 V ±10 %                                 | -4.56                | 3.576                | -13.408              | 6.596                | -13.408              | 10.36                |
| 2.5 V to 4.5 V                              | -11.072              | 3.296                | -20.152              | 5.904                | -20.152              | 8.768                |
| 1.71 V to 5.5 V                             | -43.48               | 3.296                | -51.088              | 8.892                | -53.848              | 9.988                |

**Note:** 25 MHz OSC1 performance is not guaranteed at V<sub>DD</sub> < 2.5 V.

### 3.4.14 OSC Power-On Delay (Normal Mode)

**Note:** DLY/CNT Counter Data = 100, OSC Power Setting: "Auto Power-On", OSC Clock to Matrix Input: "Enable".

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Power Supply Range ( $V_{DD}$ ) V | OSC0 2 MHz        |                   | OSC0 25 kHz                  |                              | OSC1              |                   |
|-----------------------------------|-------------------|-------------------|------------------------------|------------------------------|-------------------|-------------------|
|                                   | Typical Value, ns | Maximum Value, ns | Typical Value, $\mu\text{s}$ | Maximum Value, $\mu\text{s}$ | Typical Value, ns | Maximum Value, ns |
| 1.71                              | 372.7             | 407.3             | 0.40                         | 0.57                         | 71.2              | 87.3              |
| 1.80                              | 349.2             | 379.5             | 0.38                         | 0.41                         | 65.0              | 78.7              |
| 1.89                              | 330.3             | 358.0             | 0.35                         | 0.41                         | 59.7              | 71.3              |
| 2.30                              | 277.2             | 298.1             | 0.29                         | 0.31                         | 43.0              | 54.0              |
| 2.50                              | 262.0             | 281.9             | 0.28                         | 0.30                         | 39.6              | 48.1              |
| 2.70                              | 250.2             | 269.8             | 0.26                         | 0.30                         | 36.7              | 43.5              |
| 3.00                              | 236.6             | 256.7             | 0.25                         | 0.44                         | 33.2              | 39.8              |
| 3.30                              | 226.7             | 247.4             | 0.23                         | 0.47                         | 30.4              | 36.8              |
| 3.60                              | 219.0             | 239.9             | 0.22                         | 0.46                         | 28.2              | 34.3              |
| 4.20                              | 207.4             | 229.2             | 0.37                         | 0.50                         | 25.8              | 30.6              |
| 4.50                              | 202.8             | 224.5             | 1.63                         | 1.92                         | 25.0              | 29.2              |
| 5.00                              | 196.3             | 218.7             | 1.67                         | 2.05                         | 24.3              | 27.5              |
| 5.50                              | 190.8             | 213.3             | 1.69                         | 1.99                         | 23.7              | 26.8              |

### 3.4.15 OSC Power-On Delay (Fast Start-Up Time Mode)

Typical values are at  $T_A = +25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Power Supply Range ( $V_{DD}$ ) V | OSC0 2 MHz        |                   | OSC0 25 kHz                  |                              |
|-----------------------------------|-------------------|-------------------|------------------------------|------------------------------|
|                                   | Typical Value, ns | Maximum Value, ns | Typical Value, $\mu\text{s}$ | Maximum Value, $\mu\text{s}$ |
| 1.71                              | 327.9             | 360.0             | 0.68                         | 0.76                         |
| 1.80                              | 309.9             | 338.3             | 0.64                         | 0.64                         |
| 1.89                              | 295.5             | 323.1             | 0.61                         | 0.70                         |
| 2.30                              | 254.9             | 278.1             | 0.53                         | 21.93                        |
| 2.50                              | 243.1             | 266.1             | 3.23                         | 21.88                        |
| 2.70                              | 234.1             | 257.1             | 16.68                        | 21.94                        |
| 3.00                              | 223.7             | 246.8             | 19.25                        | 21.90                        |
| 3.30                              | 215.7             | 239.1             | 19.22                        | 21.77                        |
| 3.60                              | 209.4             | 232.9             | 19.21                        | 21.74                        |
| 4.20                              | 199.5             | 223.4             | 19.17                        | 21.78                        |
| 4.50                              | 195.5             | 219.8             | 19.15                        | 21.69                        |
| 5.00                              | 189.8             | 214.6             | 19.12                        | 21.71                        |
| 5.50                              | 184.9             | 209.8             | 19.05                        | 21.75                        |

### 3.4.16 ACMP Specifications

$T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.3\text{ V}$  to  $5.5\text{ V}$ , unless otherwise noted.

| Parameter                 | Symbol       | Note                                                                                                                                                    | Conditions                                                                                                                                      | Min   | Typ   | Max      | Unit          |
|---------------------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|----------|---------------|
| ACMP Input Voltage Range  | $V_{ACMP}$   | Positive Input                                                                                                                                          | $V_{DD} = 1.8\text{ V} \pm 5\%$                                                                                                                 | 0     | --    | $V_{DD}$ | V             |
|                           |              | Negative Input                                                                                                                                          |                                                                                                                                                 | 0     | --    | 1.2      | V             |
|                           |              | Positive Input                                                                                                                                          | $V_{DD} = 3.3\text{ V} \pm 10\%$                                                                                                                | 0     | --    | $V_{DD}$ | V             |
|                           |              | Negative Input                                                                                                                                          |                                                                                                                                                 | 0     | --    | 1.2      | V             |
|                           |              | Positive Input                                                                                                                                          | $V_{DD} = 5.0\text{ V} \pm 10\%$                                                                                                                | 0     | --    | $V_{DD}$ | V             |
|                           |              | Negative Input                                                                                                                                          |                                                                                                                                                 | 0     | --    | 1.2      | V             |
| ACMP Input Offset Voltage | $V_{offset}$ | Low Bandwidth - Enable, $V_{phys} = 0\text{ mV}$ , Gain = 1, $V_{REF} = 50\text{ mV}$ to $1200\text{ mV}$ , $V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$  | $T_A = +25\text{ }^{\circ}\text{C}$                                                                                                             | -10.7 | --    | 8.4      | mV            |
|                           |              |                                                                                                                                                         | $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$                                                                           | -10.6 | --    | 7.0      | mV            |
|                           |              | Low Bandwidth - Disable, $V_{phys} = 0\text{ mV}$ , Gain = 1, $V_{REF} = 50\text{ mV}$ to $1200\text{ mV}$ , $V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$ | $T_A = +25\text{ }^{\circ}\text{C}$                                                                                                             | -10.2 | --    | 9.1      | mV            |
|                           |              |                                                                                                                                                         | $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$                                                                           | -10.3 | --    | 7.6      | mV            |
| ACMP Start Time           | $t_{start}$  | ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump set to automatic ON/OFF                    | BG = 550 $\mu\text{s}$ ,<br>$T_A = +25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$                                   | --    | 672.6 | 909.0    | $\mu\text{s}$ |
|                           |              |                                                                                                                                                         | BG = 550 $\mu\text{s}$ ,<br>$T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$<br>$V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$ | --    | 676.5 | 1033.8   | $\mu\text{s}$ |
|                           |              |                                                                                                                                                         | BG = 100 $\mu\text{s}$ ,<br>$T_A = +25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 2.7\text{ V}$ to $5.5\text{ V}$                                    | --    | 133.2 | 181.9    | $\mu\text{s}$ |
|                           |              |                                                                                                                                                         | BG = 100 $\mu\text{s}$ ,<br>$T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$<br>$V_{DD} = 2.7\text{ V}$ to $5.5\text{ V}$  | --    | 134.7 | 207.0    | $\mu\text{s}$ |
|                           |              | ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump always OFF                                 | BG = 550 $\mu\text{s}$ ,<br>$T_A = +25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$                                    | --    | 673.1 | 909.0    | $\mu\text{s}$ |
|                           |              |                                                                                                                                                         | BG = 550 $\mu\text{s}$ ,<br>$T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$  | --    | 676.9 | 1033.8   | $\mu\text{s}$ |
|                           |              |                                                                                                                                                         | BG = 100 $\mu\text{s}$ ,<br>$T_A = +25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$                                    | --    | 133.0 | 181.2    | $\mu\text{s}$ |
|                           |              |                                                                                                                                                         | BG = 100 $\mu\text{s}$ ,<br>$T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$  | --    | 134.4 | 207.0    | $\mu\text{s}$ |

| Parameter                        | Symbol    | Note                                                                                                                          | Conditions                                                        | Min     | Typ   | Max     | Unit          |
|----------------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|---------|-------|---------|---------------|
| Built-in Hysteresis              | $V_{HYS}$ | $V_{HYS} = 25 \text{ mV}$<br>$V_{IL} = V_{in} - V_{HYS}/2$<br>$V_{IH} = V_{in} + V_{HYS}/2$                                   | LB - Enabled,<br>$T_A = +25^\circ\text{C}$                        | 7.32    | --    | 35.5    | mV            |
|                                  |           |                                                                                                                               | LB - Disabled,<br>$T_A = +25^\circ\text{C}$                       | 10.0    | --    | 38.5    | mV            |
|                                  |           | $V_{HYS} = 50 \text{ mV}$<br>$V_{IL} = V_{in} - V_{HYS}$<br>$V_{IH} = V_{HYS}$                                                | LB - Enabled,<br>$T_A = +25^\circ\text{C}$                        | 42.9    | --    | 57.8    | mV            |
|                                  |           |                                                                                                                               | LB - Disabled,<br>$T_A = +25^\circ\text{C}$                       | 44.2    | --    | 54.3    | mV            |
|                                  |           | $V_{HYS} = 200 \text{ mV}$<br>$V_{IL} = V_{in} - V_{HYS}$<br>$V_{IH} = V_{HYS}$                                               | LB - Enabled,<br>$T_A = +25^\circ\text{C}$                        | 192.7   | --    | 208.7   | mV            |
|                                  |           |                                                                                                                               | LB - Disabled,<br>$T_A = +25^\circ\text{C}$                       | 193.3   | --    | 204.8   | mV            |
|                                  |           | $V_{HYS} = 25 \text{ mV}$<br>$V_{IL} = V_{in} - V_{HYS}/2$<br>$V_{IH} = V_{in} + V_{HYS}/2$                                   | LB - Enabled<br>$T_A = -40^\circ\text{C to } +105^\circ\text{C}$  | 23.745  | --    | 44.435  | mV            |
|                                  |           |                                                                                                                               | LB - Disabled<br>$T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | 3.691   | --    | 45.604  | mV            |
|                                  |           | $V_{HYS} = 50 \text{ mV}$<br>$V_{IL} = V_{in} - V_{HYS}$<br>$V_{IH} = V_{HYS}$                                                | LB - Enabled<br>$T_A = -40^\circ\text{C to } +105^\circ\text{C}$  | 48.408  | --    | 51.004  | mV            |
|                                  |           |                                                                                                                               | LB - Disabled<br>$T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | 40.130  | --    | 54.622  | mV            |
|                                  |           | $V_{HYS} = 200 \text{ mV}$<br>$V_{IL} = V_{in} - V_{HYS}$<br>$V_{IH} = V_{HYS}$                                               | LB - Enabled<br>$T_A = -40^\circ\text{C to } +105^\circ\text{C}$  | 198.131 | --    | 201.066 | mV            |
|                                  |           |                                                                                                                               | LB - Disabled<br>$T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | 189.278 | --    | 203.599 | mV            |
| Series Input Resistance          | $R_{sin}$ | Gain = 1x                                                                                                                     |                                                                   | --      | 100.0 | --      | M $\Omega$    |
|                                  |           | Gain = 0.5x                                                                                                                   |                                                                   | --      | 1.0   | --      | M $\Omega$    |
|                                  |           | Gain = 0.33x                                                                                                                  |                                                                   | --      | 0.8   | --      | M $\Omega$    |
|                                  |           | Gain = 0.25x                                                                                                                  |                                                                   | --      | 1.0   | --      | M $\Omega$    |
| Propagation Delay, Response Time | PROP      | Low Bandwidth - Enable, Gain = 1, $V_{DD} = 1.71 \text{ V to } 3.3 \text{ V}$ , Overdrive = 10 mV, $V_{REF} = 50 \text{ mV}$  | Low to High, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$     | --      | 20.14 | 224.67  | $\mu\text{s}$ |
|                                  |           |                                                                                                                               | High to Low, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$     | --      | 21.40 | 228.61  | $\mu\text{s}$ |
|                                  |           | Low Bandwidth - Enable, Gain = 1, $V_{DD} = 1.71 \text{ V to } 3.3 \text{ V}$ , Overdrive = 100 mV, $V_{REF} = 50 \text{ mV}$ | Low to High, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$     | --      | 7.11  | 86.83   | $\mu\text{s}$ |
|                                  |           |                                                                                                                               | High to Low, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$     | --      | 8.59  | 98.99   | $\mu\text{s}$ |
|                                  |           | Low Bandwidth - Disable, Gain = 1, $V_{DD} = 1.71 \text{ V to } 3.3 \text{ V}$ , Overdrive = 10 mV, $V_{REF} = 50 \text{ mV}$ | Low to High, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$     | --      | 1.14  | 12.06   | $\mu\text{s}$ |
|                                  |           |                                                                                                                               | High to Low, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$     | --      | 1.14  | 4.84    | $\mu\text{s}$ |

| Parameter                           | Symbol | Note                                                                                                                                    | Conditions                                                                          | Min | Typ   | Max    | Unit          |
|-------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|-------|--------|---------------|
| Propagation Delay,<br>Response Time | PROP   | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 50\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.46  | 1.79   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.55  | 2.60   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 50\text{ mV}$     | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 13.91 | 84.35  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 15.36 | 90.15  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 50\text{ mV}$    | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 4.97  | 31.60  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 5.98  | 39.68  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 50\text{ mV}$    | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.91  | 1.98   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.01  | 1.58   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 50\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.37  | 1.14   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.45  | 0.81   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 250\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 20.28 | 228.06 | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }105\text{ }^{\circ}\text{C}$  | --  | 21.67 | 232.39 | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 250\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 7.19  | 89.05  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 6.39  | 78.66  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 250\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.17  | 2.01   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.25  | 2.06   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 250\text{ mV}$ | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.41  | 0.68   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.39  | 0.75   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 250\text{ mV}$    | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 14.19 | 84.96  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 15.66 | 91.88  | $\mu\text{s}$ |

| Parameter                           | Symbol | Note                                                                                                                                    | Conditions                                                                          | Min | Typ   | Max    | Unit          |
|-------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|-------|--------|---------------|
| Propagation Delay,<br>Response Time | PROP   | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 250\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 5.03  | 32.06  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 4.51  | 30.70  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 250\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.10  | 1.82   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.20  | 1.94   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 250\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.35  | 0.55   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.33  | 0.64   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 600\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 20.69 | 232.09 | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 22.19 | 241.46 | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 600\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 7.28  | 90.29  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 6.47  | 79.76  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 600\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.40  | 2.85   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.45  | 2.56   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 600\text{ mV}$ | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.41  | 0.68   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.37  | 0.62   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 600\text{ mV}$    | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 14.48 | 86.02  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 16.01 | 93.69  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 600\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 5.09  | 32.43  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 4.57  | 31.06  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 600\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.34  | 2.69   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.40  | 2.50   | $\mu\text{s}$ |

| Parameter                           | Symbol | Note                                                                                                                                    | Conditions                                                                          | Min | Typ   | Max     | Unit          |
|-------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|-------|---------|---------------|
| Propagation Delay,<br>Response Time | PROP   | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 600\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.35  | 0.55    | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.31  | 0.50    | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 850\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 21.07 | 237.30  | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 22.66 | 244.72  | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 850\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 7.38  | 91.95   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 6.55  | 81.25   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 850\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.46  | 2.94    | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.51  | 2.89    | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 850\text{ mV}$ | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.42  | 0.68    | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.37  | 0.59    | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 850\text{ mV}$    | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 14.69 | 87.94   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 16.31 | 95.65   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 850\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 5.14  | 32.91   | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 4.62  | 31.59   | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 850\text{ mV}$   | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.36  | 2.81    | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 1.45  | 2.89    | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Disable, Gain = 1,<br>$V_{DD} = 3.3\text{ V to }5.5\text{ V}$ ,<br>Overdrive = 100 mV,<br>$V_{REF} = 850\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.35  | 0.53    | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 0.31  | 0.48    | $\mu\text{s}$ |
|                                     |        | Low Bandwidth -<br>Enable, Gain = 1,<br>$V_{DD} = 1.71\text{ V to }3.3\text{ V}$ ,<br>Overdrive = 10 mV,<br>$V_{REF} = 1200\text{ mV}$  | Low to High,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 27.40 | 1193.10 | $\mu\text{s}$ |
|                                     |        |                                                                                                                                         | High to Low,<br>$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --  | 28.14 | 962.09  | $\mu\text{s}$ |

| Parameter                                                                                                                          | Symbol | Note                                                                                                                         | Conditions                                                                       | Min    | Typ   | Max     | Unit          |
|------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|--------|-------|---------|---------------|
| Propagation Delay, Response Time                                                                                                   | PROP   | Low Bandwidth - Enable, Gain = 1, $V_{DD} = 1.71\text{ V to }3.3\text{ V}$ , Overdrive = 100 mV, $V_{REF} = 1200\text{ mV}$  | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 10.67 | 683.00  | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 6.98  | 108.00  | $\mu\text{s}$ |
|                                                                                                                                    |        | Low Bandwidth - Disable, Gain = 1, $V_{DD} = 1.71\text{ V to }3.3\text{ V}$ , Overdrive = 10 mV, $V_{REF} = 1200\text{ mV}$  | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 8.14  | 1078.16 | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 5.00  | 748.66  | $\mu\text{s}$ |
|                                                                                                                                    |        | Low Bandwidth - Disable, Gain = 1, $V_{DD} = 1.71\text{ V to }3.3\text{ V}$ , Overdrive = 100 mV, $V_{REF} = 1200\text{ mV}$ | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 4.07  | 648.33  | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 0.61  | 27.15   | $\mu\text{s}$ |
|                                                                                                                                    |        | Low Bandwidth - Enable, Gain = 1, $V_{DD} = 3.3\text{ V to }5.5\text{ V}$ , Overdrive = 10 mV, $V_{REF} = 1200\text{ mV}$    | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 15.28 | 99.83   | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 17.06 | 105.90  | $\mu\text{s}$ |
|                                                                                                                                    |        | Low Bandwidth - Enable, Gain = 1, $V_{DD} = 3.3\text{ V to }5.5\text{ V}$ , Overdrive = 100 mV, $V_{REF} = 1200\text{ mV}$   | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 5.38  | 37.46   | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 4.73  | 32.64   | $\mu\text{s}$ |
|                                                                                                                                    |        | Low Bandwidth - Disable, Gain = 1, $V_{DD} = 3.3\text{ V to }5.5\text{ V}$ , Overdrive = 10 mV, $V_{REF} = 1200\text{ mV}$   | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 1.82  | 11.85   | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 1.77  | 10.13   | $\mu\text{s}$ |
|                                                                                                                                    |        | Low Bandwidth - Disable, Gain = 1, $V_{DD} = 3.3\text{ V to }5.5\text{ V}$ , Overdrive = 100 mV, $V_{REF} = 1200\text{ mV}$  | Low to High, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 0.63  | 6.60    | $\mu\text{s}$ |
|                                                                                                                                    |        |                                                                                                                              | High to Low, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | --     | 0.34  | 0.78    | $\mu\text{s}$ |
| Gain error (including threshold and internal $V_{REF}$ error), $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ | G      | G = 1, $V_{DD} = 1.71\text{ V}$                                                                                              | $V_{REF} = 50\text{ mV to }1200\text{ mV}$                                       | --     | 1     | --      | %             |
|                                                                                                                                    |        | G = 1, $V_{DD} = 3.3\text{ V}$                                                                                               |                                                                                  | --     | 1     | --      |               |
|                                                                                                                                    |        | G = 1, $V_{DD} = 5.5\text{ V}$                                                                                               |                                                                                  | --     | 1     | --      |               |
|                                                                                                                                    |        | G = 0.5, $V_{DD} = 1.71\text{ V}$                                                                                            |                                                                                  | -6.323 | --    | 9.895   |               |
|                                                                                                                                    |        | G = 0.5, $V_{DD} = 3.3\text{ V}$                                                                                             |                                                                                  | -6.110 | --    | 7.751   |               |
|                                                                                                                                    |        | G = 0.5, $V_{DD} = 5.5\text{ V}$                                                                                             |                                                                                  | -6.369 | --    | 7.715   |               |
|                                                                                                                                    |        | G = 0.33, $V_{DD} = 1.71\text{ V}$                                                                                           |                                                                                  | -5.028 | --    | 11.334  |               |
|                                                                                                                                    |        | G = 0.33, $V_{DD} = 3.3\text{ V}$                                                                                            |                                                                                  | -3.677 | --    | 6.273   |               |
|                                                                                                                                    |        | G = 0.33, $V_{DD} = 5.5\text{ V}$                                                                                            |                                                                                  | -5.201 | --    | 7.370   |               |
|                                                                                                                                    |        | G = 0.25, $V_{DD} = 1.71\text{ V}$                                                                                           |                                                                                  | -5.940 | --    | 7.709   |               |
|                                                                                                                                    |        | G = 0.25, $V_{DD} = 3.3\text{ V}$                                                                                            |                                                                                  | -5.910 | --    | 7.353   |               |
|                                                                                                                                    |        | G = 0.25, $V_{DD} = 5.5\text{ V}$                                                                                            |                                                                                  | -5.793 | --    | 4.990   |               |

| Parameter                                                      | Symbol                         | Note                               | Conditions                         | Min   | Typ  | Max  | Unit |
|----------------------------------------------------------------|--------------------------------|------------------------------------|------------------------------------|-------|------|------|------|
| Internal V <sub>REF</sub> error,<br>V <sub>REF</sub> = 1200 mV | V <sub>REF</sub>               | V <sub>DD</sub> = 1.8 V ± 5 %      | T <sub>A</sub> = +25 °C            | -0.25 | --   | 0.50 | %    |
|                                                                |                                |                                    | T <sub>A</sub> = -40 °C to +105 °C | -2.25 | --   | 0.67 |      |
|                                                                |                                | V <sub>DD</sub> = 3.3 V ± 10 %     | T <sub>A</sub> = +25 °C            | -0.33 | --   | 0.42 |      |
|                                                                |                                |                                    | T <sub>A</sub> = -40 °C to +105 °C | -2.50 | --   | 0.58 |      |
|                                                                |                                | V <sub>DD</sub> = 5.0 V ± 10 %     | T <sub>A</sub> = +25 °C            | -0.50 | --   | 0.33 |      |
|                                                                |                                |                                    | T <sub>A</sub> = -40 °C to +105 °C | -2.08 | --   | 0.50 |      |
| Internal V <sub>REF</sub> error,<br>V <sub>REF</sub> = 1000 mV |                                | V <sub>DD</sub> = 1.8 V ± 5 %      | T <sub>A</sub> = +25 °C            | -0.10 | --   | 0.70 |      |
|                                                                |                                |                                    | T <sub>A</sub> = -40 °C to +105 °C | -7.30 | --   | 0.80 |      |
|                                                                |                                | V <sub>DD</sub> = 3.3 V ± 10 %     | T <sub>A</sub> = +25 °C            | -0.20 | --   | 0.60 |      |
|                                                                |                                |                                    | T <sub>A</sub> = -40 °C to +105 °C | -2.10 | --   | 0.70 |      |
|                                                                |                                | V <sub>DD</sub> = 5.0 V ± 10 %     | T <sub>A</sub> = +25 °C            | -0.40 | --   | 0.50 |      |
|                                                                |                                |                                    | T <sub>A</sub> = -40 °C to +105 °C | -1.60 | --   | 0.60 |      |
| Internal V <sub>REF</sub> error,<br>V <sub>REF</sub> = 500 mV  | V <sub>DD</sub> = 1.8 V ± 5 %  | T <sub>A</sub> = +25 °C            | -0.40                              | --    | 0.60 |      |      |
|                                                                |                                | T <sub>A</sub> = -40 °C to +105 °C | -3.00                              | --    | 0.80 |      |      |
|                                                                | V <sub>DD</sub> = 3.3 V ± 10 % | T <sub>A</sub> = +25 °C            | -0.60                              | --    | 0.40 |      |      |
|                                                                |                                | T <sub>A</sub> = -40 °C to +105 °C | -2.60                              | --    | 0.60 |      |      |
|                                                                | V <sub>DD</sub> = 5.0 V ± 10 % | T <sub>A</sub> = +25 °C            | -0.60                              | --    | 0.40 |      |      |
|                                                                |                                | T <sub>A</sub> = -40 °C to +105 °C | -2.20                              | --    | 0.60 |      |      |

### 3.4.17 Analog Temperature Sensor Specifications

TS Output vs. Temperature (Output Range 1).

| $T_J$ , °C | Target<br>$V_{TS\_OUT}$ , V | $V_{TS\_OUT}$ , V |       | Calculated $T_J$ , °C |       | $T_J$ Accuracy, °C |      |
|------------|-----------------------------|-------------------|-------|-----------------------|-------|--------------------|------|
|            |                             | Min               | Max   | Min                   | Max   | Min                | Max  |
| -40        | 1.192                       | 1.153             | 1.224 | -49.1                 | -28.8 | -9.1               | 11.2 |
| -30        | 1.157                       | 1.119             | 1.189 | -39.1                 | -19.1 | -9.1               | 10.9 |
| -20        | 1.122                       | 1.085             | 1.155 | -29.4                 | -9.4  | -9.4               | 10.6 |
| -10        | 1.087                       | 1.051             | 1.121 | -19.7                 | 0.3   | -9.7               | 10.3 |
| 0          | 1.052                       | 1.017             | 1.086 | -9.7                  | 10.1  | -9.7               | 10.1 |
| 10         | 1.017                       | 0.982             | 1.051 | 0.3                   | 20.1  | -9.7               | 10.1 |
| 20         | 0.982                       | 0.948             | 1.016 | 10.3                  | 29.8  | -9.7               | 9.8  |
| 25         | 0.965                       | 0.930             | 0.999 | 15.2                  | 34.9  | -9.8               | 9.9  |
| 30         | 0.947                       | 0.913             | 0.982 | 20.1                  | 39.8  | -9.9               | 9.8  |
| 40         | 0.912                       | 0.879             | 0.947 | 30.1                  | 49.5  | -9.9               | 9.5  |
| 50         | 0.877                       | 0.844             | 0.912 | 40.1                  | 59.5  | -9.9               | 9.5  |
| 60         | 0.842                       | 0.809             | 0.877 | 50.1                  | 69.5  | -9.9               | 9.5  |
| 70         | 0.807                       | 0.773             | 0.841 | 60.3                  | 79.8  | -9.7               | 9.8  |
| 80         | 0.772                       | 0.738             | 0.806 | 70.3                  | 89.8  | -9.7               | 9.8  |
| 85         | 0.755                       | 0.720             | 0.787 | 75.8                  | 94.9  | -9.2               | 9.9  |

| $T_J, ^\circ\text{C}$ | Target<br>$V_{TS\_OUT}, \text{V}$ | $V_{TS\_OUT}, \text{V}$ |       | Calculated $T_J, ^\circ\text{C}$ |       | $T_J$ Accuracy, $^\circ\text{C}$ |      |
|-----------------------|-----------------------------------|-------------------------|-------|----------------------------------|-------|----------------------------------|------|
|                       |                                   | Min                     | Max   | Min                              | Max   | Min                              | Max  |
| 90                    | 0.737                             | 0.702                   | 0.769 | 80.9                             | 100.1 | -9.1                             | 10.1 |
| 100                   | 0.702                             | 0.668                   | 0.734 | 90.9                             | 109.8 | -9.1                             | 9.8  |
| 105                   | 0.685                             | 0.647                   | 0.716 | 96.1                             | 115.8 | -8.9                             | 10.8 |

TS Output vs. Temperature (Output Range 2).

| $T_J, ^\circ\text{C}$ | Target<br>$V_{TS\_OUT}, \text{V}$ | $V_{TS\_OUT}, \text{V}$ |       | Calculated $T_J, ^\circ\text{C}$ |       | $T_J$ Accuracy, $^\circ\text{C}$ |      |
|-----------------------|-----------------------------------|-------------------------|-------|----------------------------------|-------|----------------------------------|------|
|                       |                                   | Min                     | Max   | Min                              | Max   | Min                              | Max  |
| -40                   | 0.983                             | 0.949                   | 1.008 | -48.6                            | -28.3 | -8.6                             | 11.7 |
| -30                   | 0.954                             | 0.921                   | 0.979 | -38.6                            | -18.6 | -8.6                             | 11.4 |
| -20                   | 0.925                             | 0.893                   | 0.952 | -29.3                            | -9.0  | -9.3                             | 11.0 |
| -10                   | 0.896                             | 0.865                   | 0.923 | -19.3                            | 0.7   | -9.3                             | 10.7 |
| 0                     | 0.867                             | 0.837                   | 0.895 | -9.7                             | 10.3  | -9.7                             | 10.3 |
| 10                    | 0.838                             | 0.809                   | 0.866 | 0.3                              | 20.0  | -9.7                             | 10.0 |
| 20                    | 0.809                             | 0.781                   | 0.837 | 10.3                             | 29.7  | -9.7                             | 9.7  |
| 25                    | 0.795                             | 0.766                   | 0.823 | 15.2                             | 34.8  | -9.8                             | 9.8  |
| 30                    | 0.780                             | 0.752                   | 0.809 | 20.0                             | 39.7  | -10.0                            | 9.7  |
| 40                    | 0.751                             | 0.724                   | 0.780 | 30.0                             | 49.3  | -10.0                            | 9.3  |
| 50                    | 0.722                             | 0.695                   | 0.751 | 40.0                             | 59.3  | -10.0                            | 9.3  |
| 60                    | 0.693                             | 0.666                   | 0.722 | 50.0                             | 69.3  | -10.0                            | 9.3  |
| 70                    | 0.664                             | 0.636                   | 0.693 | 60.0                             | 79.7  | -10.0                            | 9.7  |
| 80                    | 0.635                             | 0.608                   | 0.664 | 70.0                             | 89.3  | -10.0                            | 9.3  |
| 85                    | 0.621                             | 0.593                   | 0.648 | 75.5                             | 94.5  | -9.5                             | 9.5  |
| 90                    | 0.606                             | 0.578                   | 0.633 | 80.7                             | 99.7  | -9.3                             | 9.7  |
| 100                   | 0.577                             | 0.550                   | 0.605 | 90.3                             | 109.3 | -9.7                             | 9.3  |
| 105                   | 0.563                             | 0.533                   | 0.590 | 95.5                             | 115.2 | -9.5                             | 10.2 |

## 4. User Programmability

The SLG46533-E is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the IO Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

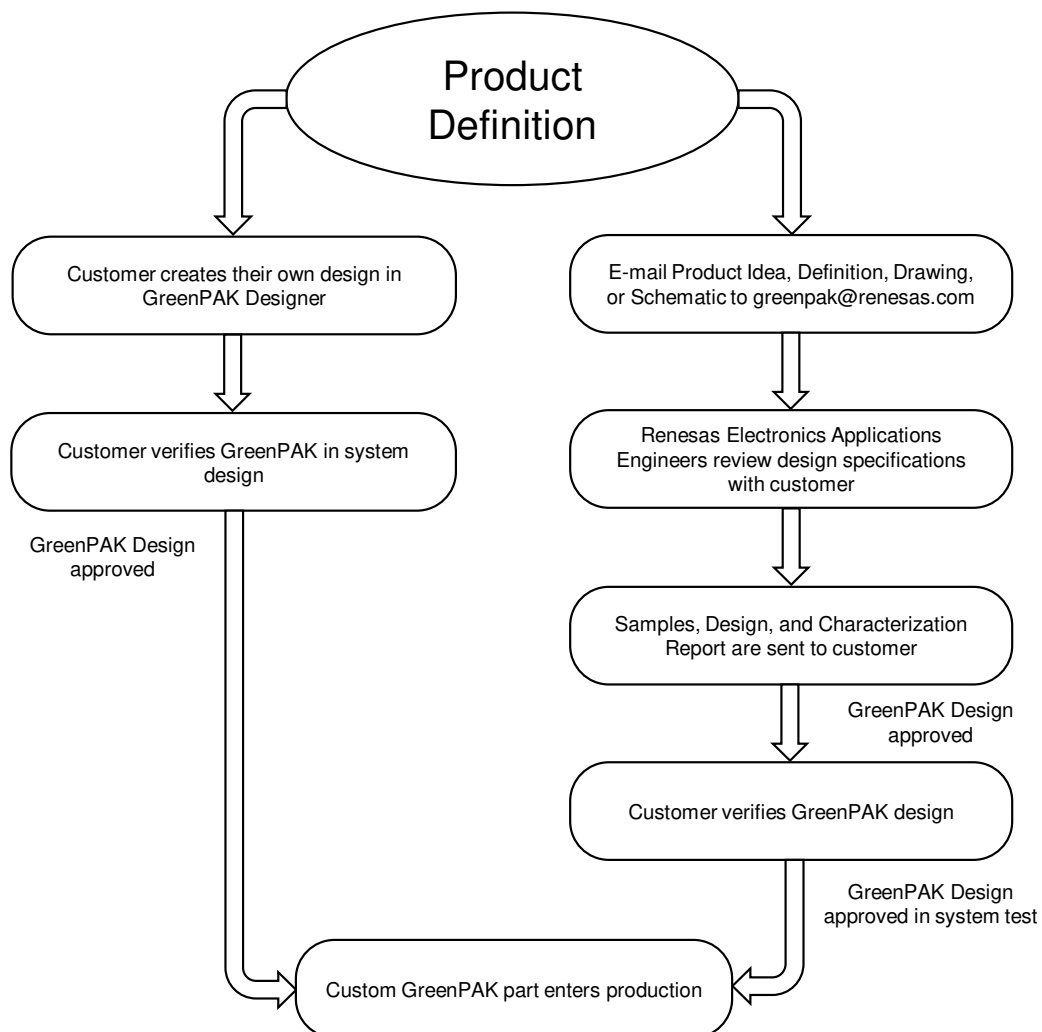


Figure 3. Steps to Create a Custom GreenPAK Device

## 5. Input/Output Pins

The SLG46533-E has a total of 18 multi-function IO pins which can function as either a user defined Input or Output, as well as serving as a special function (such as voltage reference output), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Refer to section 2. Pin Information for normal mode pin definitions.

Normal Mode pin definitions are as follows:

- $V_{DD}$ :  $V_{DD}$  power supply
- IO0: general purpose input
- IO1: general purpose input or output with OE
- IO2: general purpose input or output
- IO3: general purpose input or output with OE
- IO4: general purpose input or output or analog comparator 0(+)
- IO5: general purpose input or output with OE or analog comparator 0(-)
- IO6: general purpose input or OD output I<sup>2</sup>C SCL
- IO7: general purpose input or OD output I<sup>2</sup>C SDA
- IO8: general purpose input or output with OE or analog comparator 1(+)
- GND: ground
- IO9: general purpose input or output or analog comparator 1(-)
- IO10: general purpose input or output with OE or analog comparator 2(+)
- IO11: general purpose input or output with OE or analog comparator 2(-)
- IO12: general purpose input or output or analog comparator 3(+)
- IO13: general purpose input or output with OE
- IO14: general purpose input or output
- IO15: general purpose input or output with OE and  $V_{REF}$  output ( $V_{REF1}$ )
- IO16: general purpose input or output with OE and  $V_{REF}$  output ( $V_{REF0}$ )
- IO17: general purpose input or output or external clock input

Of the 18 user defined IO pins on the SLG46533-E, all but one of the pins (IO0) can serve as both digital input and digital output. IO0 can only serve as a digital input pin.

### 5.1 Input Modes

Each IO pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. IOs 4, 5, 8, 9, 10, 11, and 12 can also be configured to serve as analog inputs to the on-chip comparators. IOs 15 and 16 can also be configured as analog reference voltage inputs.

### 5.2 Output Modes

IOs 1, 2, 3, 4, 5, 6, 7, 8, 8, 10, 11, 12, 13, 14, 15, 16, and 17 can all be configured as digital output pins.

### 5.3 Pull-Up/Down Resistors

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 k $\Omega$ , 100 k $\Omega$ , and 1 M $\Omega$ . In the case of IO0, the resistors are fixed to a pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either pull-up or pull-downs.

## 5.4 GPI Structure

### 5.4.1 GPI Structure (for IO0)

Input Mode [1:0]

00: Digital In without Schmitt Trigger, wosmt\_en = 1, OE = 0

01: Digital In with Schmitt Trigger, smt\_en = 1, OE = 0

10: Low Voltage Digital In mode, lv\_en = 1, OE = 0

11: Reserved

Note 1: OE cannot be selected by user.

Note 2: OE is Matrix output, Digital In is Matrix input.

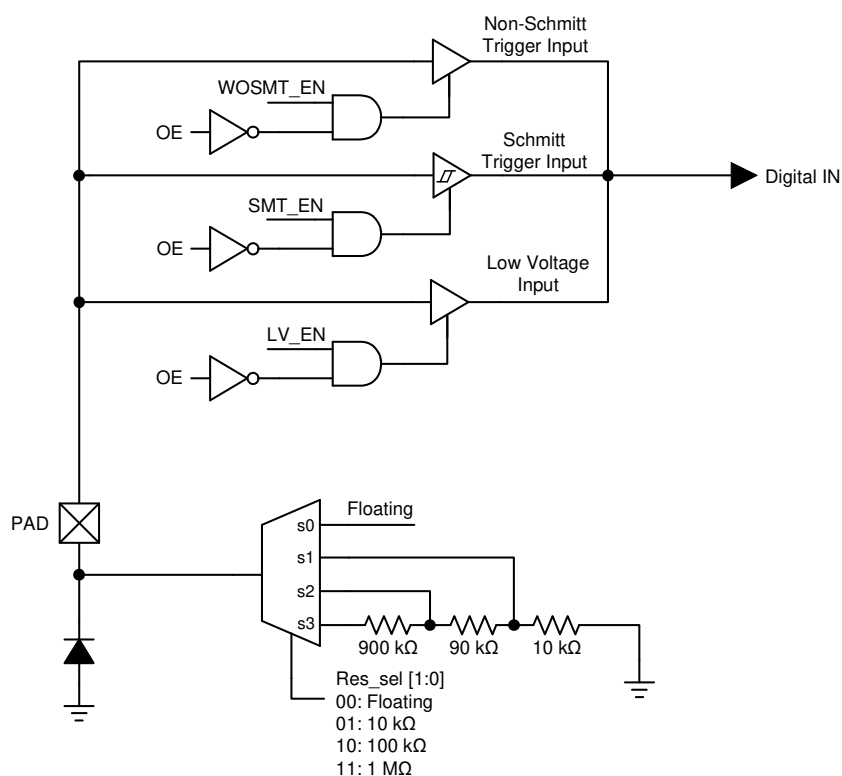


Figure 4. IO0 GPI Structure Diagram

## 5.5 Matrix OE IO Structure

### 5.5.1 Matrix OE IO Structure (for IOs 1, 3, 5, 10, 11, 13, 15, 16)

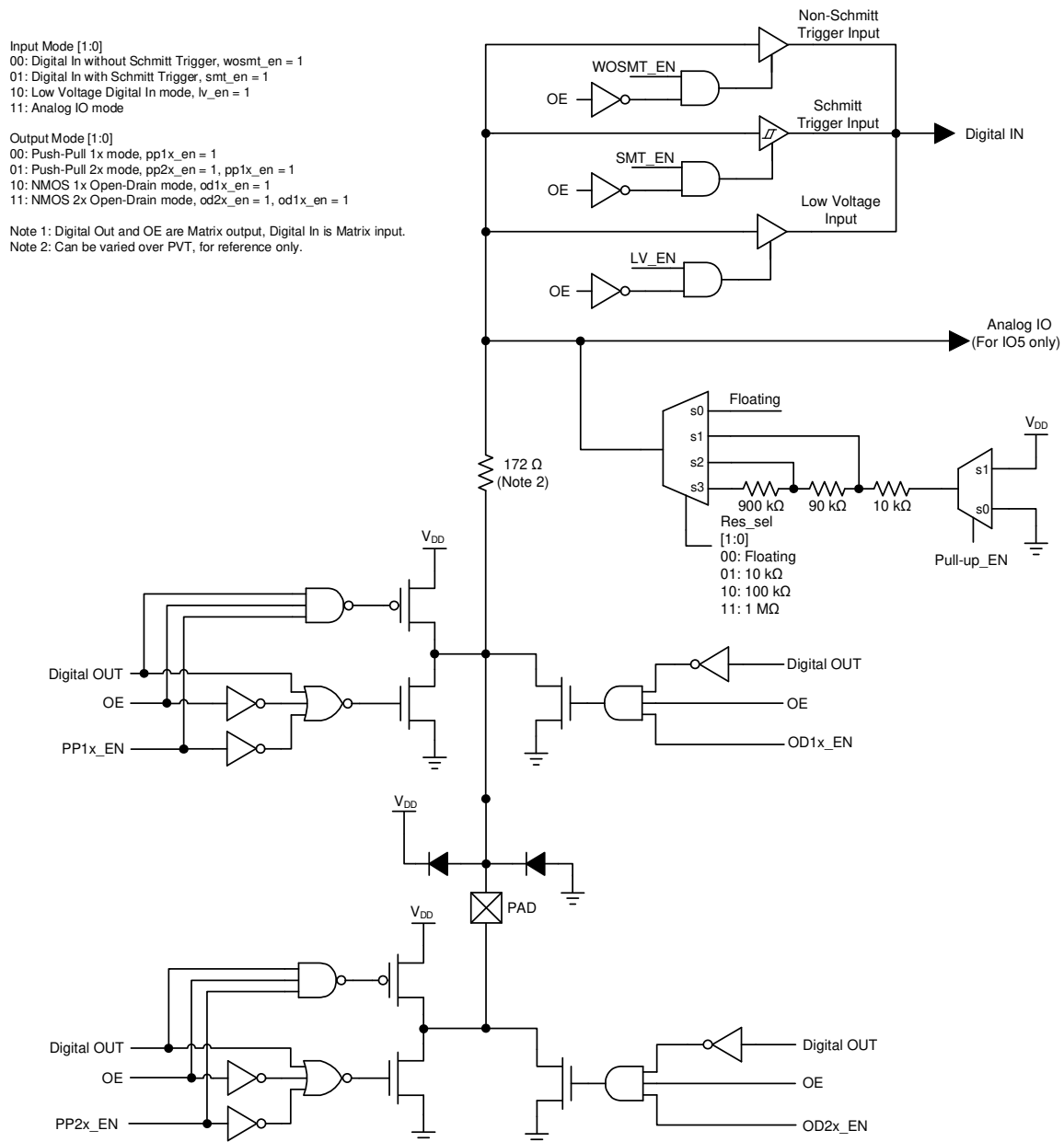


Figure 5. Matrix OE IO Structure Diagram

## 5.5.2 Matrix OE IO Structure (for IOs 6 and 7)

IO6, IO7 Mode [2:0]

000: Digital Input without Schmitt Trigger

001: Digital Input with Schmitt Trigger

010: Low Voltage Digital Input

011: Reserved

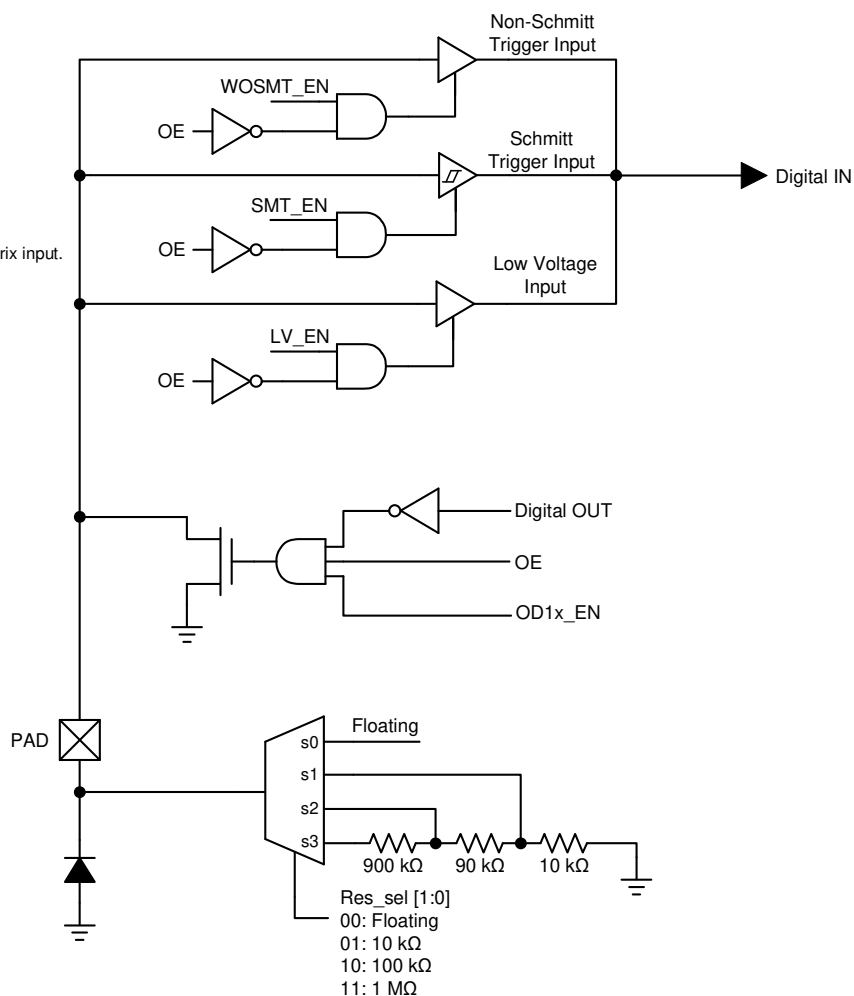
100: Reserved

101: Open-Drain NMOS

110: Reserved

111: Reserved

Note: Digital Out and OE are Matrix output, Digital In is Matrix input.



### 5.5.3 Matrix OE 4x Drive Structure (for IO8)

#### Input Mode [1:0]

00: Digital In without Schmitt Trigger, wosmt\_en = 1  
 01: Digital In with Schmitt Trigger, smt\_en = 1  
 10: Low Voltage Digital In mode, lv\_en = 1  
 11: Analog IO mode

#### Output Mode [1:0]

00: Push-Pull 1x mode, pp1x\_en = 1  
 01: Push-Pull 2x mode, pp2x\_en = 1, pp1x\_en = 1  
 10: NMOS Open-Drain 1x mode, od1x\_en = 1, odn\_en = 1  
 11: NMOS Open-Drain 2x mode, od2x\_en = 1, od1x\_en = 1, odn\_en = 1

Note 1: Digital Out and OE are Matrix output, Digital In is Matrix input.  
 Note 2: Can be varied over PVT, for reference only.

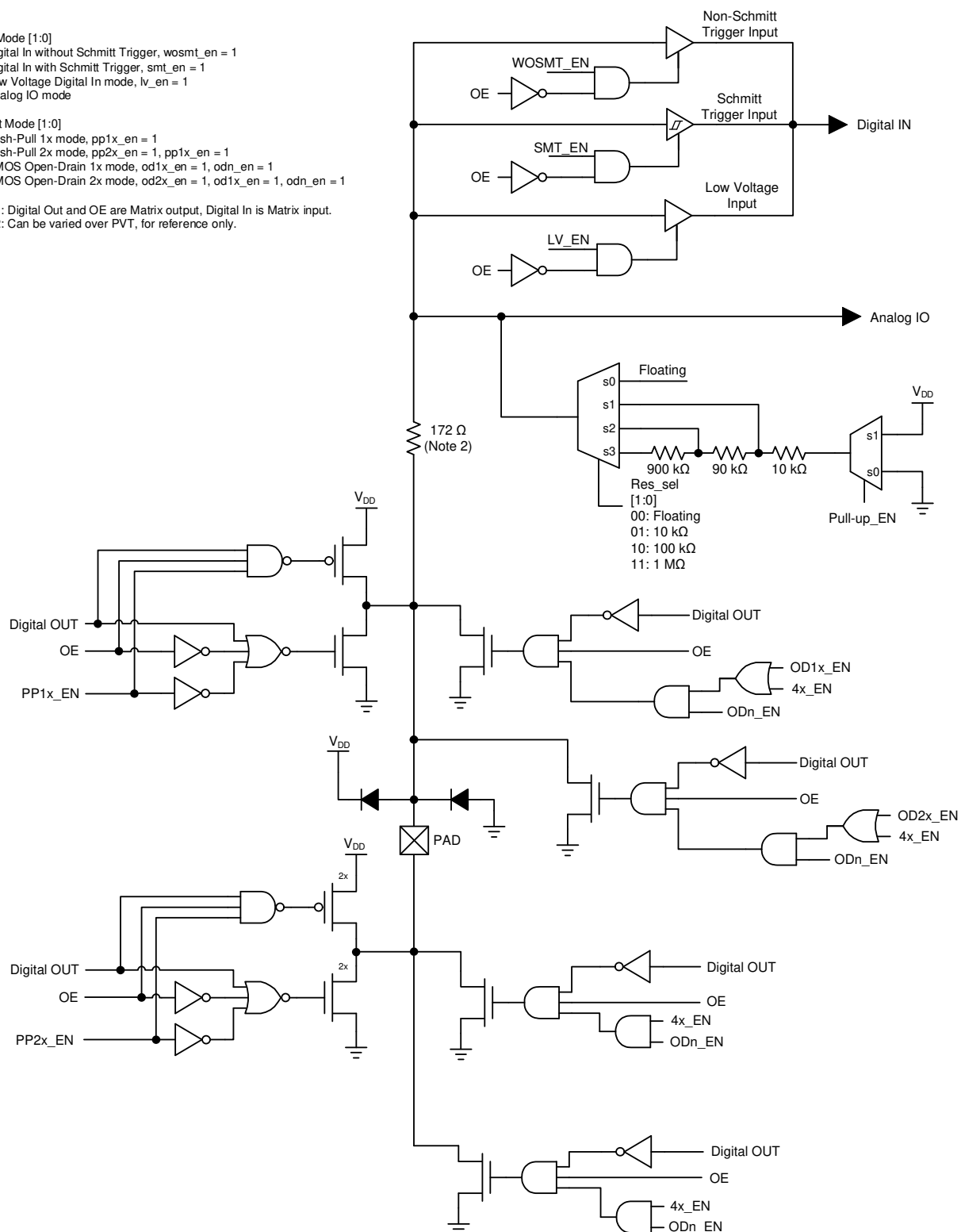


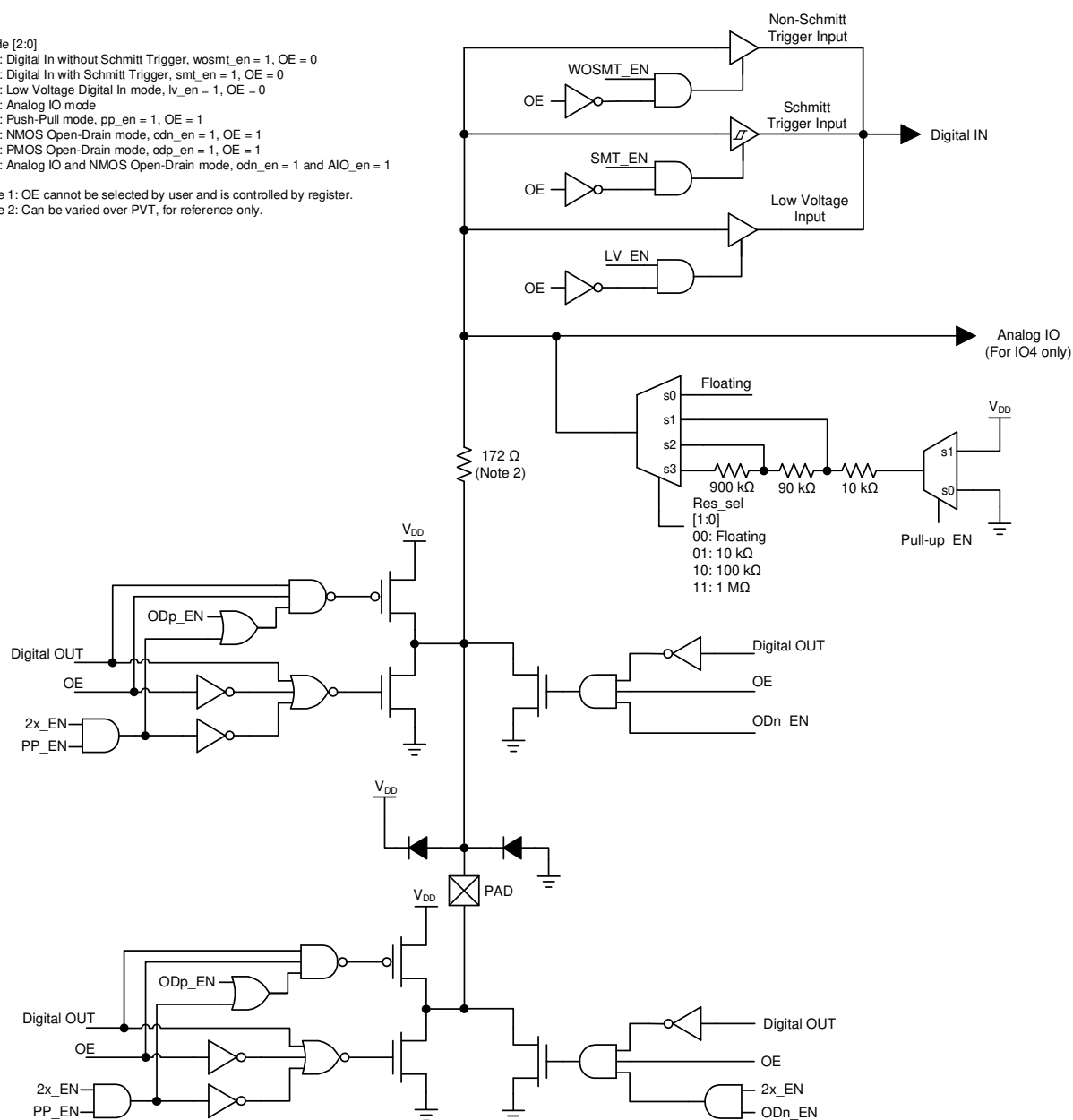
Figure 7. Matrix OE IO 4x Drive Structure Diagram

## 5.6 IO Structure

### 5.6.1 IO Structure (for IOs 2, 4, 12, 14, 17)

```
Mode [2:0]
000: Digital In without Schmitt Trigger, wsmt_en = 1, OE = 0
001: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
010: Low Voltage Digital In mode, lv_en = 1, OE = 0
011: Analog IO mode
100: Push-Pull mode, pp_en = 1, OE = 1
101: NMOS Open-Drain mode, odn_en = 1, OE = 1
110: PMOS Open-Drain mode, odp_en = 1, OE = 1
111: Analog IO and NMOS Open-Drain mode, odn_en = 1 and AIO_en = 1
```

Note 1: OE cannot be selected by user and is controlled by register.  
Note 2: Can be varied over PVT. for reference only.



### Figure 8. IO Structure Diagram

## 5.6.2 4x Drive Structure (for IO9)

Mode [2:0]

000: Digital In without Schmitt Trigger, wosmt\_en = 1, OE = 0

001: Digital In with Schmitt Trigger, smt\_en = 1, OE = 0

010: Low Voltage Digital In mode, lv\_en = 1, OE = 0

011: Analog IO mode

100: Push-Pull mode, pp\_en = 1, OE = 1

101: NMOS Open-Drain mode, odn\_en = 1, OE = 1

110: PMOS Open-Drain mode, odp\_en = 1, OE = 1

111: Analog IO and NMOS Open-Drain mode, odn\_en = 1 and AIO\_en = 1

Note 1: OE cannot be selected by user.

Note 2: Digital Out and OE are Matrix output, Digital In is Matrix input.

Note 3: Can be varied over PVT, for reference only.

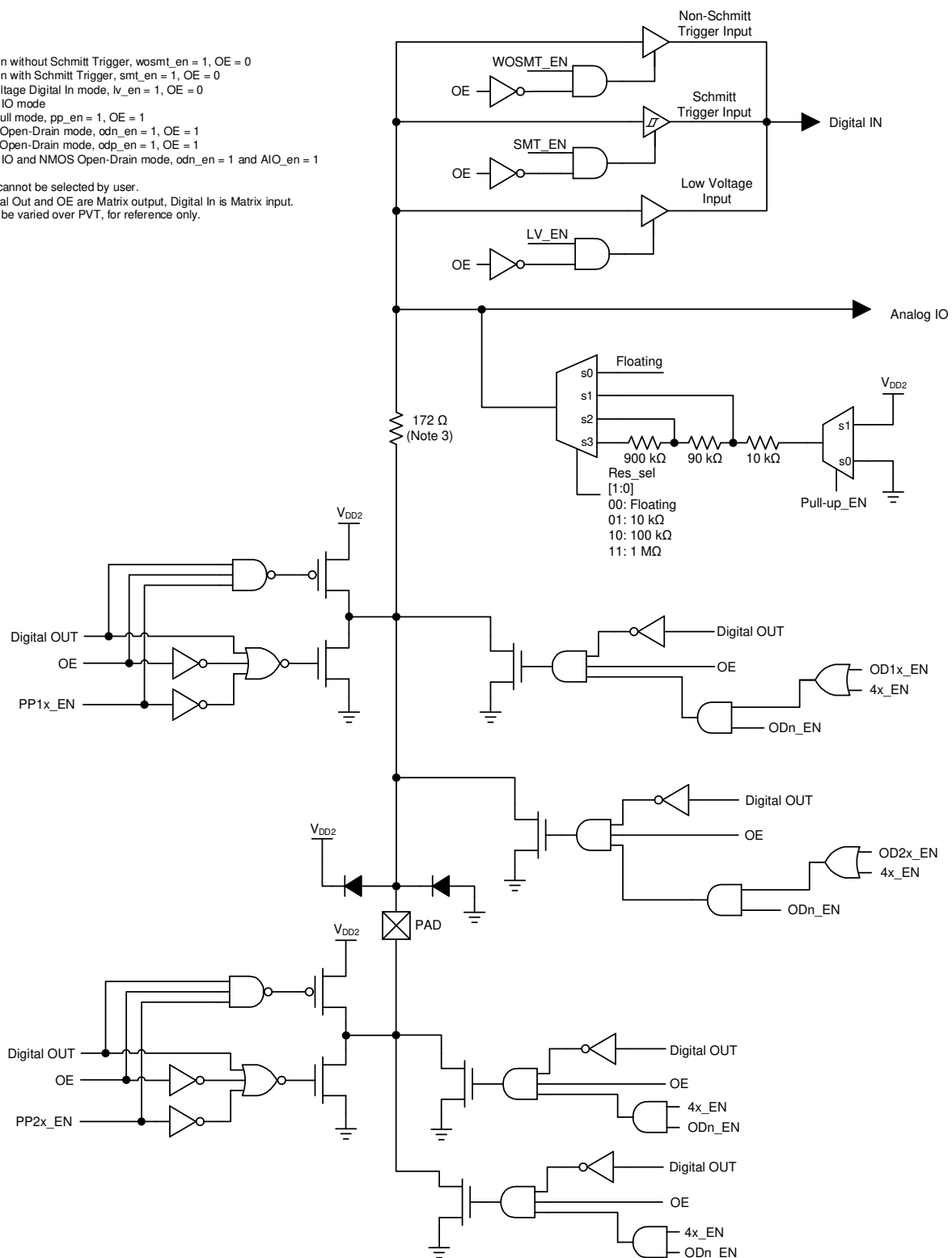


Figure 9. IO 4x Drive Structure Diagram

## 6. Connection Matrix

The Connection Matrix in the SLG46533-E is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46533-E has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the SLG46533-E are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 110 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V<sub>DD</sub> and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46533-E's register table, see section 17. [Register Definitions](#).

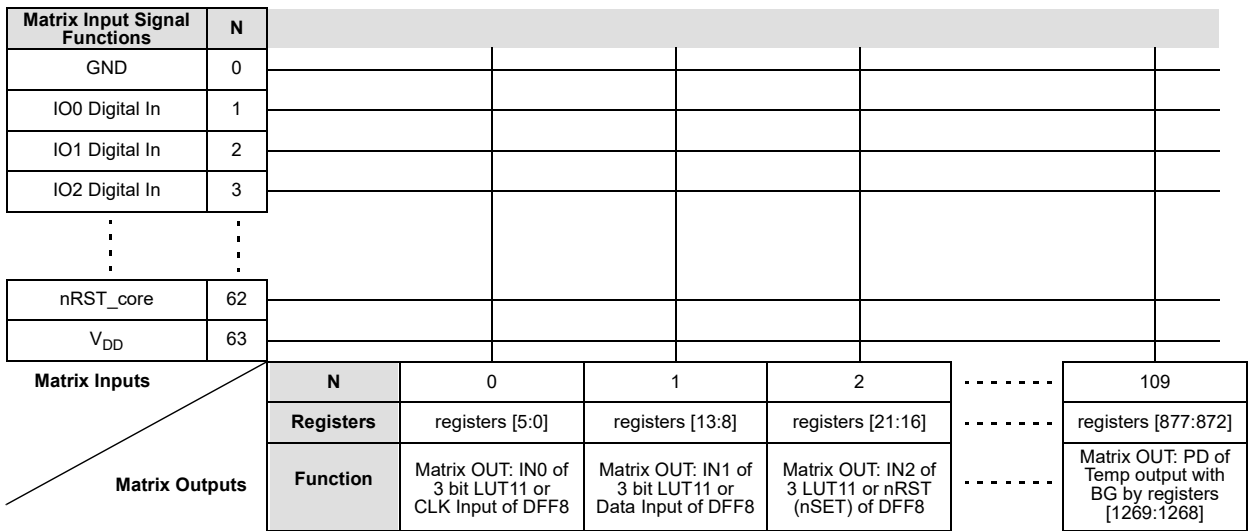


Figure 10. Connection Matrix

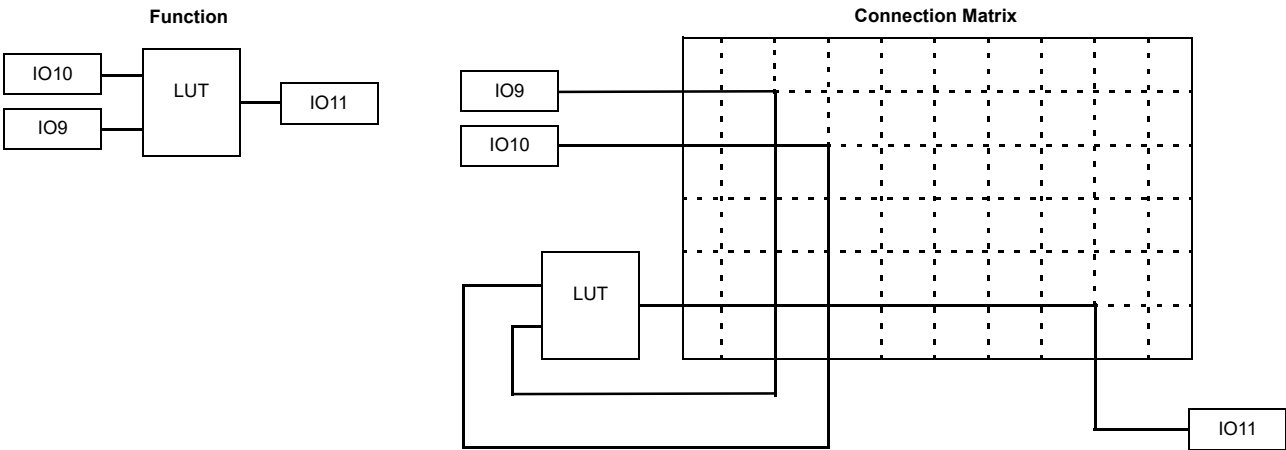


Figure 11. Connection Matrix Example

## 6.1 Matrix Input Table

Table 4. Matrix Input Table

| Matrix Input Number | Matrix Input Signal Function                                          | Matrix Decode |   |   |   |   |   |
|---------------------|-----------------------------------------------------------------------|---------------|---|---|---|---|---|
|                     |                                                                       | 5             | 4 | 3 | 2 | 1 | 0 |
| 0                   | GND                                                                   | 0             | 0 | 0 | 0 | 0 | 0 |
| 1                   | IO0 Digital Input                                                     | 0             | 0 | 0 | 0 | 0 | 1 |
| 2                   | IO1 Digital Input                                                     | 0             | 0 | 0 | 0 | 1 | 0 |
| 3                   | IO2 Digital Input                                                     | 0             | 0 | 0 | 0 | 1 | 1 |
| 4                   | IO3 Digital Input                                                     | 0             | 0 | 0 | 1 | 0 | 0 |
| 5                   | IO4 Digital Input                                                     | 0             | 0 | 0 | 1 | 0 | 1 |
| 6                   | IO5 Digital Input                                                     | 0             | 0 | 0 | 1 | 1 | 0 |
| 7                   | IO8 Digital Input                                                     | 0             | 0 | 0 | 1 | 1 | 1 |
| 8                   | 2-bit LUT0/DFF0 Output                                                | 0             | 0 | 1 | 0 | 0 | 0 |
| 9                   | 2-bit LUT1/DFF1 Output                                                | 0             | 0 | 1 | 0 | 0 | 1 |
| 10                  | 2-bit LUT2/DFF2 Output                                                | 0             | 0 | 1 | 0 | 1 | 0 |
| 11                  | 2-bit LUT3/PGen Output                                                | 0             | 0 | 1 | 0 | 1 | 1 |
| 12                  | 3-bit LUT0/DFF3 (SET/RST) Output                                      | 0             | 0 | 1 | 1 | 0 | 0 |
| 13                  | 3-bit LUT1/DFF4 (SET/RST) Output                                      | 0             | 0 | 1 | 1 | 0 | 1 |
| 14                  | 3-bit LUT2/DFF5 (SET/RST) Output                                      | 0             | 0 | 1 | 1 | 1 | 0 |
| 15                  | 3-bit LUT3/DFF6 (SET/RST) Output                                      | 0             | 0 | 1 | 1 | 1 | 1 |
| 16                  | 3-bit LUT4/DFF7 (SET/RST) Output                                      | 0             | 1 | 0 | 0 | 0 | 0 |
| 17                  | 3-bit LUT5/CNT_DLY2(8bit) Output                                      | 0             | 1 | 0 | 0 | 0 | 1 |
| 18                  | 3-bit LUT6/CNT_DLY3(8bit) Output                                      | 0             | 1 | 0 | 0 | 1 | 0 |
| 19                  | 3-bit LUT7/CNT_DLY4(8bit) Output                                      | 0             | 1 | 0 | 0 | 1 | 1 |
| 20                  | 3-bit LUT8/CNT_DLY5(8bit) Output                                      | 0             | 1 | 0 | 1 | 0 | 0 |
| 21                  | 3-bit LUT9/CNT_DLY6(8bit) Output                                      | 0             | 1 | 0 | 1 | 0 | 1 |
| 22                  | 4-bit LUT0/CNT_DLY0(16bit) Output                                     | 0             | 1 | 0 | 1 | 1 | 0 |
| 23                  | 4-bit LUT1/CNT_DLY1(16bit) Output                                     | 0             | 1 | 0 | 1 | 1 | 1 |
| 24                  | 3-bit LUT10/Pipe Delay (1 <sup>st</sup> stage) Output                 | 0             | 1 | 1 | 0 | 0 | 0 |
| 25                  | Pipe Delay Output0                                                    | 0             | 1 | 1 | 0 | 0 | 1 |
| 26                  | Pipe Delay Output1                                                    | 0             | 1 | 1 | 0 | 1 | 0 |
| 27                  | Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25 kHz/2 MHz) | 0             | 1 | 1 | 0 | 1 | 1 |
| 28                  | Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25 kHz/2 MHz) | 0             | 1 | 1 | 1 | 0 | 0 |
| 29                  | Internal OSC Pre-Divided by 1/2/4/8 Output (25 MHz)                   | 0             | 1 | 1 | 1 | 0 | 1 |
| 30                  | Filter0/Edge Detect0 Output                                           | 0             | 1 | 1 | 1 | 1 | 0 |
| 31                  | Filter1/Edge Detect1 Output                                           | 0             | 1 | 1 | 1 | 1 | 1 |
| 32                  | IO6 Digital or I <sup>2</sup> C_virtual_0 Input                       | 1             | 0 | 0 | 0 | 0 | 0 |
| 33                  | IO7 Digital or I <sup>2</sup> C_virtual_1 Input                       | 1             | 0 | 0 | 0 | 0 | 1 |

Table 4. Matrix Input Table (Cont.)

| Matrix Input Number | Matrix Input Signal Function                 | Matrix Decode |   |   |   |   |   |
|---------------------|----------------------------------------------|---------------|---|---|---|---|---|
|                     |                                              | 5             | 4 | 3 | 2 | 1 | 0 |
| 34                  | I <sup>2</sup> C_virtual_2 Input             | 1             | 0 | 0 | 0 | 1 | 0 |
| 35                  | I <sup>2</sup> C_virtual_3 Input             | 1             | 0 | 0 | 0 | 1 | 1 |
| 36                  | I <sup>2</sup> C_virtual_4 Input             | 1             | 0 | 0 | 1 | 0 | 0 |
| 37                  | I <sup>2</sup> C_virtual_5 Input             | 1             | 0 | 0 | 1 | 0 | 1 |
| 38                  | I <sup>2</sup> C_virtual_6 Input             | 1             | 0 | 0 | 1 | 1 | 0 |
| 39                  | I <sup>2</sup> C_virtual_7 Input             | 1             | 0 | 0 | 1 | 1 | 1 |
| 40                  | 3-bit LUT11/DFF8 (SET/RST) Output            | 1             | 0 | 1 | 0 | 0 | 0 |
| 41                  | 3-bit LUT12/DFF9 (SET/RST) Output            | 1             | 0 | 1 | 0 | 0 | 1 |
| 42                  | 3-bit LUT13/DFF10 (SET/RST) Output           | 1             | 0 | 1 | 0 | 1 | 0 |
| 43                  | 3-bit LUT14/DFF11 (SET/RST) Output           | 1             | 0 | 1 | 0 | 1 | 1 |
| 44                  | 3-bit LUT15/DFF12 (SET/RST) Output           | 1             | 0 | 1 | 1 | 0 | 0 |
| 45                  | 3-bit LUT16/DFF13 (SET/RST) Output           | 1             | 0 | 1 | 1 | 0 | 1 |
| 46                  | 3-bit LUT17/DFF14 (SET/RST) Output           | 1             | 0 | 1 | 1 | 1 | 0 |
| 47                  | 4-bit LUT2 Output                            | 1             | 0 | 1 | 1 | 1 | 1 |
| 48                  | IO9 Digital Input                            | 1             | 1 | 0 | 0 | 0 | 0 |
| 49                  | IO10 Digital Input                           | 1             | 1 | 0 | 0 | 0 | 1 |
| 50                  | IO11 Digital Input                           | 1             | 1 | 0 | 0 | 1 | 0 |
| 51                  | IO12 Digital Input                           | 1             | 1 | 0 | 0 | 1 | 1 |
| 52                  | IO13 Digital Input                           | 1             | 1 | 0 | 1 | 0 | 0 |
| 53                  | IO14 Digital Input                           | 1             | 1 | 0 | 1 | 0 | 1 |
| 54                  | IO15 Digital Input                           | 1             | 1 | 0 | 1 | 1 | 0 |
| 55                  | IO16 Digital Input                           | 1             | 1 | 0 | 1 | 1 | 1 |
| 56                  | IO17 Digital Input                           | 1             | 1 | 1 | 0 | 0 | 0 |
| 57                  | ACMP_0 Output                                | 1             | 1 | 1 | 0 | 0 | 1 |
| 58                  | ACMP_1 Output                                | 1             | 1 | 1 | 0 | 1 | 0 |
| 59                  | ACMP_2 Output                                | 1             | 1 | 1 | 0 | 1 | 1 |
| 60                  | ACMP_3 Output                                | 1             | 1 | 1 | 1 | 0 | 0 |
| 61                  | Programmable Delay with Edge Detector Output | 1             | 1 | 1 | 1 | 0 | 1 |
| 62                  | nRST_core (POR) as matrix input              | 1             | 1 | 1 | 1 | 1 | 0 |
| 63                  | V <sub>DD</sub>                              | 1             | 1 | 1 | 1 | 1 | 1 |

## 6.2 Matrix Output Table

Table 5. Matrix Output Table

| Register Bit Address | Matrix Output Signal Function                                                 | Matrix Output Number |
|----------------------|-------------------------------------------------------------------------------|----------------------|
| [7:0]                | Matrix OUT: IN0 of 3-bit LUT11 or Clock Input of DFF8                         | 0                    |
| [15:8]               | Matrix OUT: IN1 of 3-bit LUT11 or Data Input of DFF8                          | 1                    |
| [23:16]              | Matrix OUT: IN2 of 3-bit LUT11 or nRST (nSET) of DFF8                         | 2                    |
| [31:24]              | Matrix OUT: IN0 of 3-bit LUT12 or Clock Input of DFF9                         | 3                    |
| [39:32]              | Matrix OUT: IN1 of 3-bit LUT12 or Data Input of DFF9                          | 4                    |
| [47:40]              | Matrix OUT: IN2 of 3-bit LUT12 or nRST (nSET) of DFF9                         | 5                    |
| [55:48]              | Matrix OUT: IN0 of 3-bit LUT13 or Clock Input of DFF10                        | 6                    |
| [63:56]              | Matrix OUT: IN1 of 3-bit LUT13 or Data Input of DFF10                         | 7                    |
| [71:64]              | Matrix OUT: IN2 of 3-bit LUT13 or nRST (nSET) of DFF10                        | 8                    |
| [79:72]              | Matrix OUT: IN0 of 3-bit LUT14 or Clock Input of DFF11                        | 9                    |
| [87:80]              | Matrix OUT: IN1 of 3-bit LUT14 or Data Input of DFF11                         | 10                   |
| [95:88]              | Matrix OUT: IN2 of 3-bit LUT14 or nRST (nSET) of DFF11                        | 11                   |
| [103:96]             | Matrix OUT: IN0 of 3-bit LUT15 or Clock Input of DFF12                        | 12                   |
| [111:104]            | Matrix OUT: IN1 of 3-bit LUT15 or Data Input of DFF12                         | 13                   |
| [119:112]            | Matrix OUT: IN2 of 3-bit LUT15 or nRST (nSET) of DFF12                        | 14                   |
| [127:120]            | Matrix OUT: IN0 of 3-bit LUT16 or Clock Input of DFF13                        | 15                   |
| [135:128]            | Matrix OUT: IN1 of 3-bit LUT16 or Data Input of DFF13                         | 16                   |
| [143:136]            | Matrix OUT: IN2 of 3-bit LUT16 or nRST (nSET) of DFF13                        | 17                   |
| [151:144]            | Matrix OUT: IN0 of 3-bit LUT17 or Clock Input of DFF14                        | 18                   |
| [159:152]            | Matrix OUT: IN1 of 3-bit LUT17 or Data Input of DFF14                         | 19                   |
| [167:160]            | Matrix OUT: IN2 of 3-bit LUT17 or nRST (nSET) of DFF14                        | 20                   |
| [175:168]            | Matrix OUT: IN0 of 4-bit LUT2                                                 | 21                   |
| [183:176]            | Matrix OUT: IN1 of 4-bit LUT2                                                 | 22                   |
| [191:184]            | Matrix OUT: IN2 of 4-bit LUT2                                                 | 23                   |
| [199:192]            | Matrix OUT: IN3 of 4-bit LUT2                                                 | 24                   |
| [207:200]            | Matrix OUT: IO1 Digital Output Source                                         | 25                   |
| [215:208]            | Matrix OUT: IO1 Output Enable                                                 | 26                   |
| [223:216]            | Matrix OUT: IO2 Digital Output Source                                         | 27                   |
| [231:224]            | Matrix OUT: IO3 Digital Output Source                                         | 28                   |
| [239:232]            | Matrix OUT: IO3 Output Enable                                                 | 29                   |
| [247:240]            | Matrix OUT: IO4 Digital Output Source                                         | 30                   |
| [255:248]            | Matrix OUT: IO5 Digital Output Source                                         | 31                   |
| [263:256]            | Matrix OUT: IO5 Output Enable                                                 | 32                   |
| [271:264]            | Matrix OUT: IO6 Digital Output Source (SCL with VI/Input and NMOS open-drain) | 33                   |
| [279:272]            | Matrix OUT: IO7 Digital Output Source (SDA with VI/Input and NMOS open-drain) | 34                   |

Table 5. Matrix Output Table (Cont.)

| Register Bit Address | Matrix Output Signal Function                               | Matrix Output Number |
|----------------------|-------------------------------------------------------------|----------------------|
| [287:280]            | Matrix OUT: IO8 Digital Output Source                       | 35                   |
| [295:288]            | Matrix OUT: IO8 Output Enable                               | 36                   |
| [303:296]            | Matrix OUT: IO9 Digital Output Source                       | 37                   |
| [311:304]            | Matrix OUT: IO10 Digital Output Source                      | 38                   |
| [319:312]            | Matrix OUT: IO10 Output Enable                              | 39                   |
| [327:320]            | Matrix OUT: IO11 Digital Output Source                      | 40                   |
| [335:328]            | Matrix OUT: IO11 Output Enable                              | 41                   |
| [343:336]            | Matrix OUT: IO12 Digital Output Source                      | 42                   |
| [351:344]            | Matrix OUT: IO13 Digital Output Source                      | 43                   |
| [359:352]            | Matrix OUT: IO13 Output Enable                              | 44                   |
| [367:360]            | Matrix OUT: IO14 Digital Output Source                      | 45                   |
| [375:368]            | Matrix OUT: IO15 Digital Output Source                      | 46                   |
| [383:376]            | Matrix OUT: IO15 Output Enable                              | 47                   |
| [391:384]            | Matrix OUT: IO16 Digital Output Source                      | 48                   |
| [399:392]            | Matrix OUT: IO16 Output Enable                              | 49                   |
| [407:400]            | Matrix OUT: IO17 Digital Output Source                      | 50                   |
| [415:408]            | Matrix OUT: ACMP0 nPD (Power-Down)                          | 51                   |
| [423:416]            | Matrix OUT: ACMP1 nPD (Power-Down)                          | 52                   |
| [431:424]            | Matrix OUT: ACMP2 nPD (Power-Down)                          | 53                   |
| [439:432]            | Matrix OUT: ACMP3 nPD (Power-Down)                          | 54                   |
| [447:440]            | Matrix OUT: Input of Filter_0 with fixed time edge detector | 55                   |
| [455:448]            | Matrix OUT: Input of Filter_1 with fixed time edge detector | 56                   |
| [463:456]            | Matrix OUT: Input of Programmable Delay and Edge Detector   | 57                   |
| [471:464]            | Matrix OUT: OSC 25 kHz/2 MHz nPD (Power-Down)               | 58                   |
| [479:472]            | Matrix OUT: OSC 25 MHz nPD (Power-Down)                     | 59                   |
| [487:480]            | Matrix OUT: IN0 of 2-bit LUT0 or Clock Input of DFF0        | 60                   |
| [495:488]            | Matrix OUT: IN1 of 2-bit LUT0 or Data Input of DFF0         | 61                   |
| [503:496]            | Matrix OUT: IN0 of 2-bit LUT1 or Clock Input of DFF1        | 62                   |
| [511:504]            | Matrix OUT: IN1 of 2-bit LUT1 or Data Input of DFF1         | 63                   |
| [519:512]            | Matrix OUT: IN0 of 2-bit LUT2 or Clock Input of DFF2        | 64                   |
| [527:520]            | Matrix OUT: IN1 of 2-bit LUT2 or Data Input of DFF2         | 65                   |
| [535:528]            | Matrix OUT: IN0 of 2-bit LUT3 or Clock Input of PGen        | 66                   |
| [543:536]            | Matrix OUT: IN1 of 2-bit LUT3 or nRST of PGen               | 67                   |
| [551:544]            | Matrix OUT: IN0 of 3-bit LUT0 or Clock Input of DFF3        | 68                   |
| [559:552]            | Matrix OUT: IN1 of 3-bit LUT0 or Data Input of DFF3         | 69                   |
| [567:560]            | Matrix OUT: IN2 of 3-bit LUT0 or nRST (nSET) of DFF3        | 70                   |

Table 5. Matrix Output Table (Cont.)

| Register Bit Address | Matrix Output Signal Function                                                 | Matrix Output Number |
|----------------------|-------------------------------------------------------------------------------|----------------------|
| [575:568]            | Matrix OUT: IN0 of 3-bit LUT1 or Clock Input of DFF4                          | 71                   |
| [583:576]            | Matrix OUT: IN1 of 3-bit LUT1 or Data Input of DFF4                           | 72                   |
| [591:584]            | Matrix OUT: IN2 of 3-bit LUT1 or nRST (nSET) of DFF4                          | 73                   |
| [599:592]            | Matrix OUT: IN0 of 3-bit LUT2 or Clock Input of DFF5                          | 74                   |
| [607:600]            | Matrix OUT: IN1 of 3-bit LUT2 or Data Input of DFF5                           | 75                   |
| [615:608]            | Matrix OUT: IN2 of 3-bit LUT2 or nRST (nSET) of DFF5                          | 76                   |
| [623:616]            | Matrix OUT: IN0 of 3-bit LUT3 or Clock Input of DFF6                          | 77                   |
| [631:624]            | Matrix OUT: IN1 of 3-bit LUT3 or Data Input of DFF6                           | 78                   |
| [639:632]            | Matrix OUT: IN2 of 3-bit LUT3 or nRST (nSET) of DFF6                          | 79                   |
| [647:640]            | Matrix OUT: IN0 of 3-bit LUT4 or Clock Input of DFF7                          | 80                   |
| [655:648]            | Matrix OUT: IN1 of 3-bit LUT4 or Data Input of DFF7                           | 81                   |
| [663:656]            | Matrix OUT: IN2 of 3-bit LUT4 or nRST (nSET) of DFF7                          | 82                   |
| [671:664]            | Matrix OUT: IN0 of 3-bit LUT5 or Delay2 Input (or Counter2 RST Input)         | 83                   |
| [679:672]            | Matrix OUT: IN1 of 3-bit LUT5 or External Clock Input of Delay2 (or Counter2) | 84                   |
| [687:680]            | Matrix OUT: IN2 of 3-bit LUT5                                                 | 85                   |
| [695:688]            | Matrix OUT: IN0 of 3-bit LUT6 or Delay3 Input (or Counter3 RST Input)         | 86                   |
| [703:696]            | Matrix OUT: IN1 of 3-bit LUT6 or External Clock Input of Delay3 (or Counter3) | 87                   |
| [711:704]            | Matrix OUT: IN2 of 3-bit LUT6                                                 | 88                   |
| [719:712]            | Matrix OUT: IN0 of 3-bit LUT7 or Delay4 Input (or Counter4 RST Input)         | 89                   |
| [727:720]            | Matrix OUT: IN1 of 3-bit LUT7 or External Clock Input of Delay4 (or Counter4) | 90                   |
| [735:728]            | Matrix OUT: IN2 of 3-bit LUT7                                                 | 91                   |
| [743:736]            | Matrix OUT: IN0 of 3-bit LUT8 or Delay5 Input (or Counter5 RST Input)         | 92                   |
| [751:744]            | Matrix OUT: IN1 of 3-bit LUT8 or External Clock Input of Delay5 (or Counter5) | 93                   |
| [759:752]            | Matrix OUT: IN2 of 3-bit LUT8                                                 | 94                   |
| [767:760]            | Matrix OUT: IN0 of 3-bit LUT9 or Delay6 Input (or Counter6 RST Input)         | 95                   |
| [775:768]            | Matrix OUT: IN1 of 3-bit LUT9 or External Clock Input of Delay6 (or Counter6) | 96                   |
| [783:776]            | Matrix OUT: IN2 of 3-bit LUT9                                                 | 97                   |
| [791:784]            | Matrix OUT: IN0 of 3-bit LUT10 or Input of Pipe Delay                         | 98                   |
| [799:792]            | Matrix OUT: IN1 of 3-bit LUT10 or nRST of Pipe Delay                          | 99                   |
| [807:800]            | Matrix OUT: IN2 of 3-bit LUT10 or Clock of Pipe Delay                         | 100                  |
| [815:808]            | Matrix OUT: IN0 of 4-bit LUT0 or Delay0 Input (or Counter0 RST/SET Input)     | 101                  |
| [823:816]            | Matrix OUT: IN1 of 4-bit LUT0 or External Clock Input of Delay0 (or Counter0) | 102                  |
| [831:824]            | Matrix OUT: IN2 of 4-bit LUT0 or UP Input of FSM0                             | 103                  |
| [839:832]            | Matrix OUT: IN3 of 4-bit LUT0 or KEEP Input of FSM0                           | 104                  |
| [847:840]            | Matrix OUT: IN0 of 4-bit LUT1 or Delay1 Input (or Counter1 RST/SET Input)     | 105                  |
| [855:848]            | Matrix OUT: IN1 of 4-bit LUT1 or External Clock Input of Delay1 (or Counter1) | 106                  |

Table 5. Matrix Output Table (Cont.)

| Register Bit Address                                            | Matrix Output Signal Function                                  | Matrix Output Number |
|-----------------------------------------------------------------|----------------------------------------------------------------|----------------------|
| [863:856]                                                       | Matrix OUT: IN2 of 4-bit LUT1 or UP Input of FSM1              | 107                  |
| [871:864]                                                       | Matrix OUT: IN3 of 4-bit LUT1 or KEEP Input of FSM1            | 108                  |
| [879:872]                                                       | Matrix OUT: PD of Temp output with BG by registers [1269:1268] | 109                  |
| [1] For each address, the two most significant bits are unused. |                                                                |                      |

### 6.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I<sup>2</sup>C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I<sup>2</sup>C address for reading and writing these register values is at byte 0244.

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I<sup>2</sup>C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs, (IO6 Digital or I<sup>2</sup>C\_virtual\_0 Input) and (IO7 Digital or I<sup>2</sup>C\_virtual\_1 Input). If the virtual input mode is selected, an I<sup>2</sup>C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. Two register bits select whether the Connection Matrix input comes from the pin input or from the virtual register:

- register [1074] Select SCL and Virtual Input 0 or IO6
- register [1082] Select SDA and Virtual Input 1 or IO7.

See [Table 6](#) for Connection Matrix Virtual Inputs.

Table 6. Connection Matrix Virtual Inputs

| Matrix Input Number | Matrix Input Signal Function     | Register Bit Addresses (d) |
|---------------------|----------------------------------|----------------------------|
| 32                  | I <sup>2</sup> C_virtual_0 Input | [1952]                     |
| 33                  | I <sup>2</sup> C_virtual_1 Input | [1953]                     |
| 34                  | I <sup>2</sup> C_virtual_2 Input | [1954]                     |
| 35                  | I <sup>2</sup> C_virtual_3 Input | [1955]                     |
| 36                  | I <sup>2</sup> C_virtual_4 Input | [1956]                     |
| 37                  | I <sup>2</sup> C_virtual_5 Input | [1957]                     |
| 38                  | I <sup>2</sup> C_virtual_6 Input | [1958]                     |
| 39                  | I <sup>2</sup> C_virtual_7 Input | [1959]                     |

## 6.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I<sup>2</sup>C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I<sup>2</sup>C addresses for reading these register values are at bytes 0240 to 0247. Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0244).

## 7. Combination Function Macrocells

The SLG46533-E has twenty-four combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops.
- Twelve macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay.
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen).
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter/Delays.
- Two macrocells that can serve as either 4-bit LUTs or as 16-Bit Counter/Delays.

Inputs/Outputs for the 24 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices - AND, NAND, OR, NOR, XOR, XNOR.

### 7.1 2-Bit LUT or D Flip-Flop Macrocells

There are three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
- LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

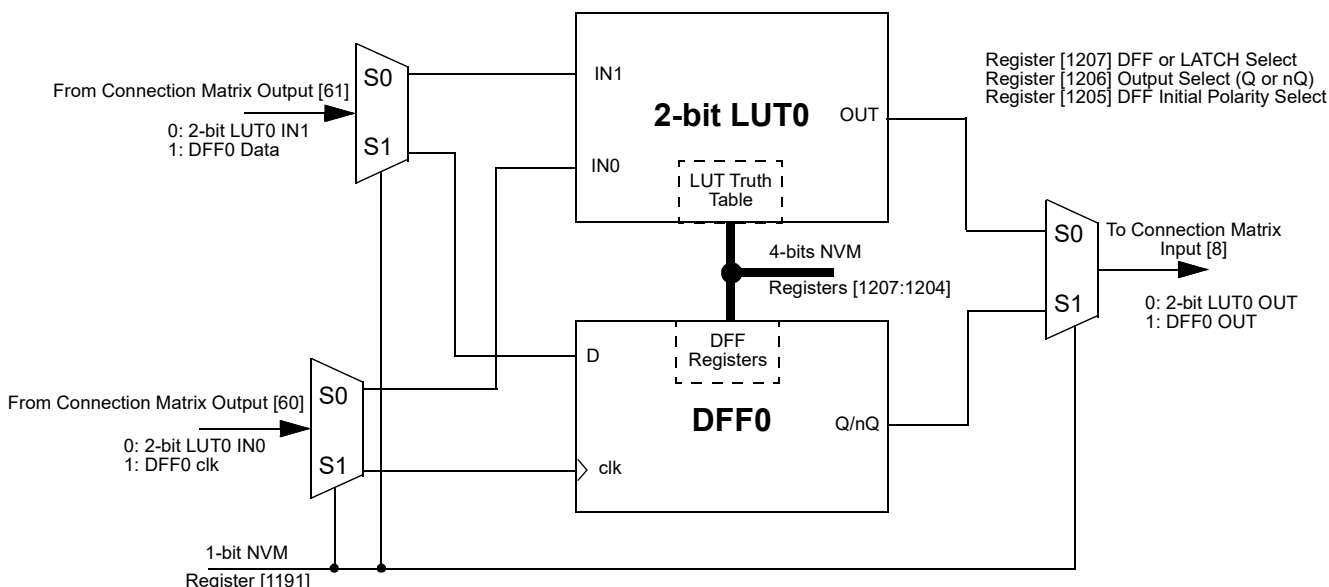
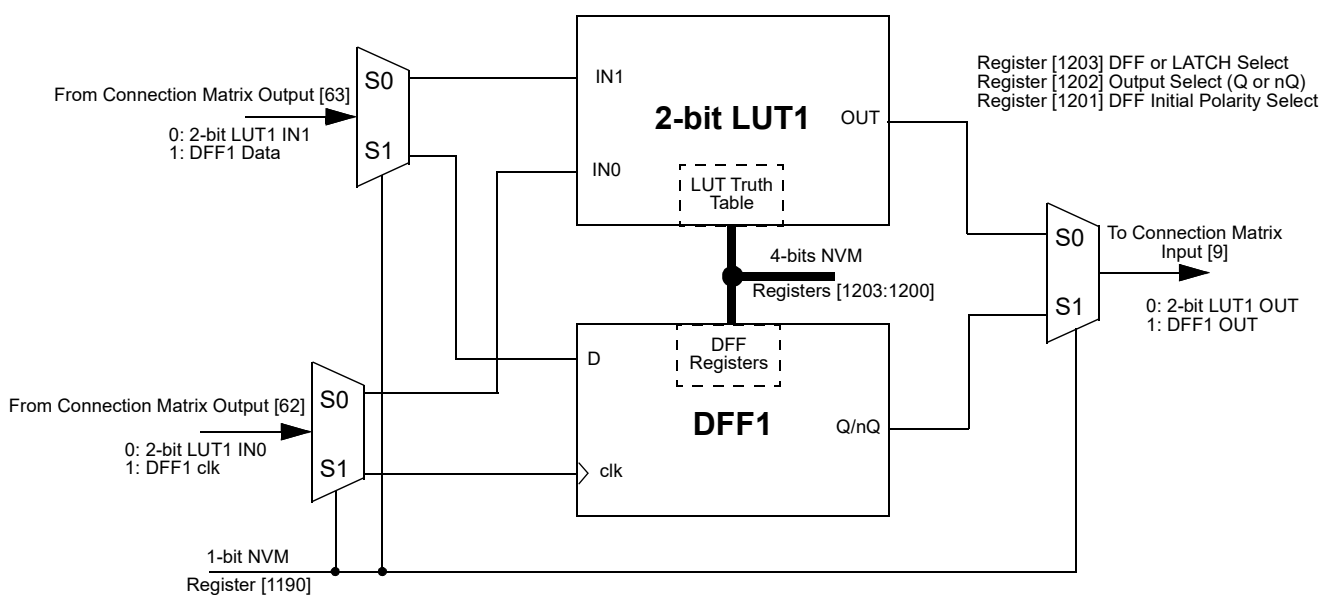
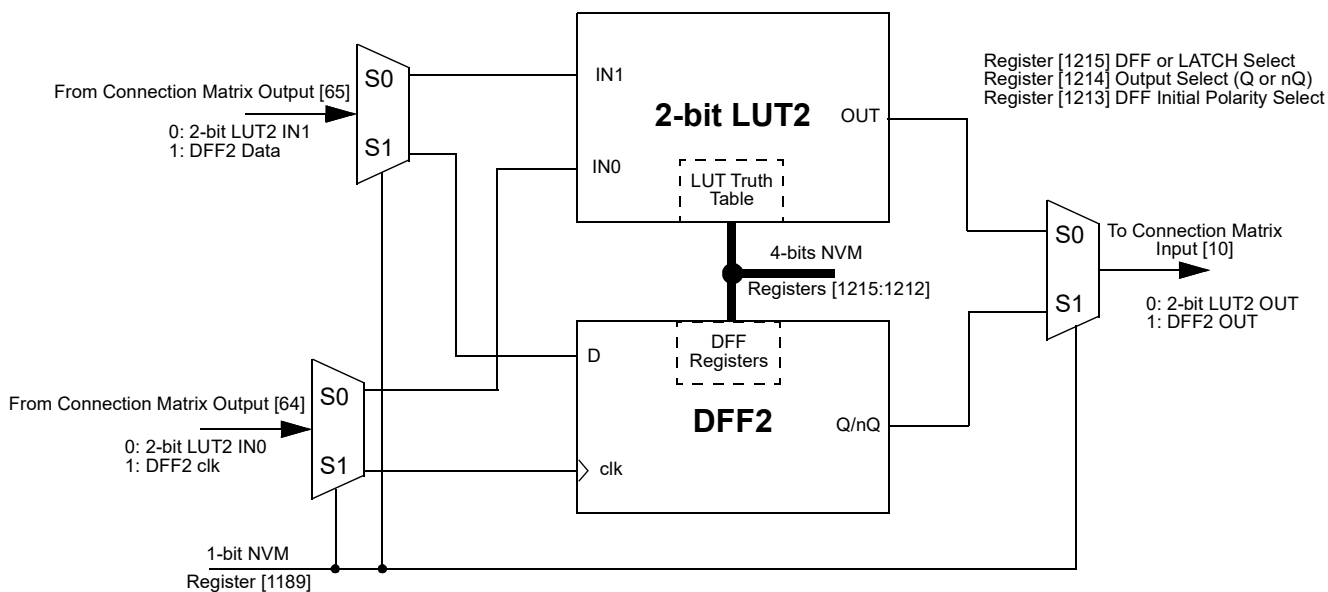


Figure 12. 2-bit LUT0 or DFF0



**Figure 13. 2-bit LUT1 or DFF1**



**Figure 14. 2-bit LUT2 or DFF2**

### 7.1.1 2-Bit LUT or D Flip-Flop Macrocells Used as 2-Bit LUTs

Table 7. 2-bit LUT0 Truth Table

| IN1 | IN0 | OUT             |     |
|-----|-----|-----------------|-----|
| 0   | 0   | register [1204] | LSB |
| 0   | 1   | register [1205] |     |
| 1   | 0   | register [1206] |     |
| 1   | 1   | register [1207] | MSB |

Table 9. 2-bit LUT2 Truth Table

| IN1 | IN0 | OUT             |     |
|-----|-----|-----------------|-----|
| 0   | 0   | register [1212] | LSB |
| 0   | 1   | register [1213] |     |
| 1   | 0   | register [1214] |     |
| 1   | 1   | register [1215] | MSB |

Table 8. 2-bit LUT1 Truth Table

| IN1 | IN0 | OUT             |     |
|-----|-----|-----------------|-----|
| 0   | 0   | register [1200] | LSB |
| 0   | 1   | register [1201] |     |
| 1   | 0   | register [1202] |     |
| 1   | 1   | register [1203] | MSB |

Each macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT0 is defined by registers [1207:1204]
- 2-bit LUT1 is defined by registers [1203:1200]
- 2-bit LUT2 is defined by registers [1215:1212].

Table 10 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 10. 2-bit LUT Standard Digital Functions

| Function | MSB |   |   | LSB |
|----------|-----|---|---|-----|
| AND-2    | 1   | 0 | 0 | 0   |
| NAND-2   | 0   | 1 | 1 | 1   |
| OR-2     | 1   | 1 | 1 | 0   |
| NOR-2    | 0   | 0 | 0 | 1   |
| XOR-2    | 0   | 1 | 1 | 0   |
| XNOR-2   | 1   | 0 | 0 | 1   |

## 7.1.2 Initial Polarity Operations

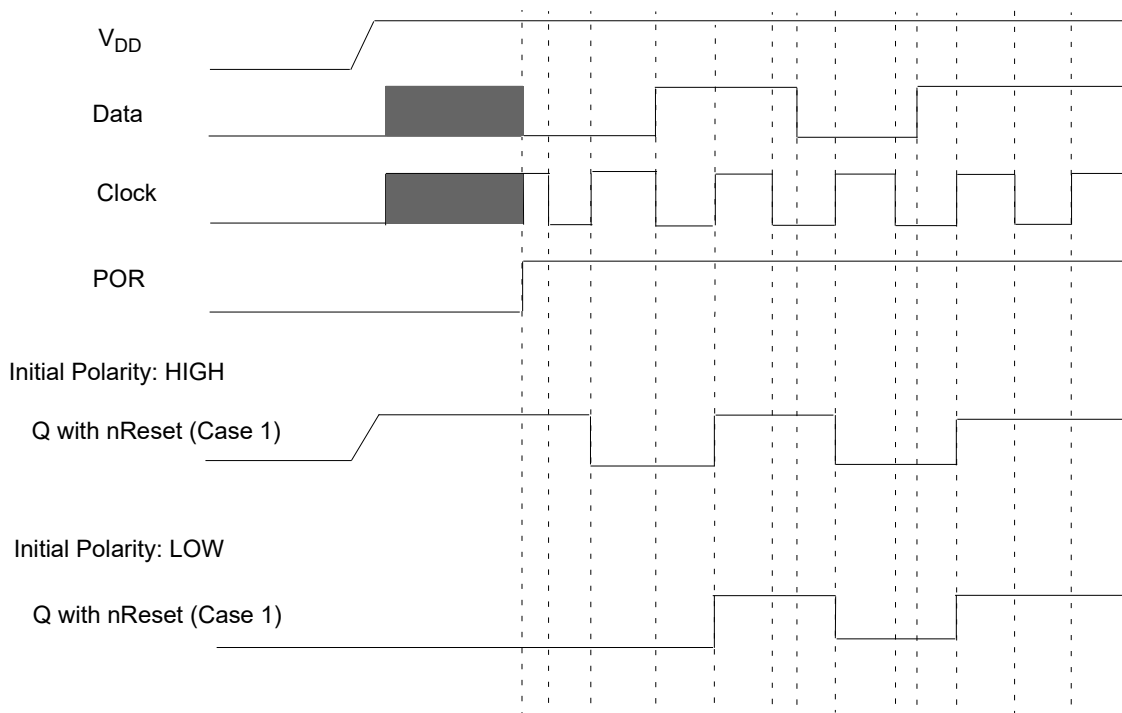


Figure 15. DFF Polarity Operations

## 7.2 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are twelve macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (rRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

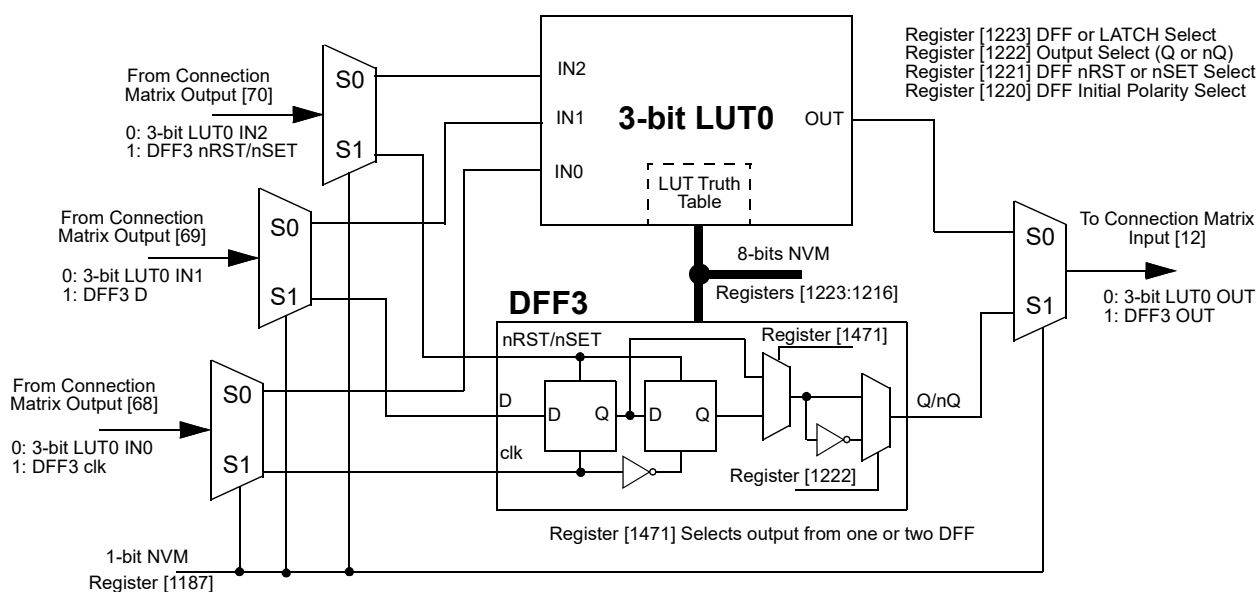


Figure 16. 3-bit LUT0 or DFF3 with RST/SET

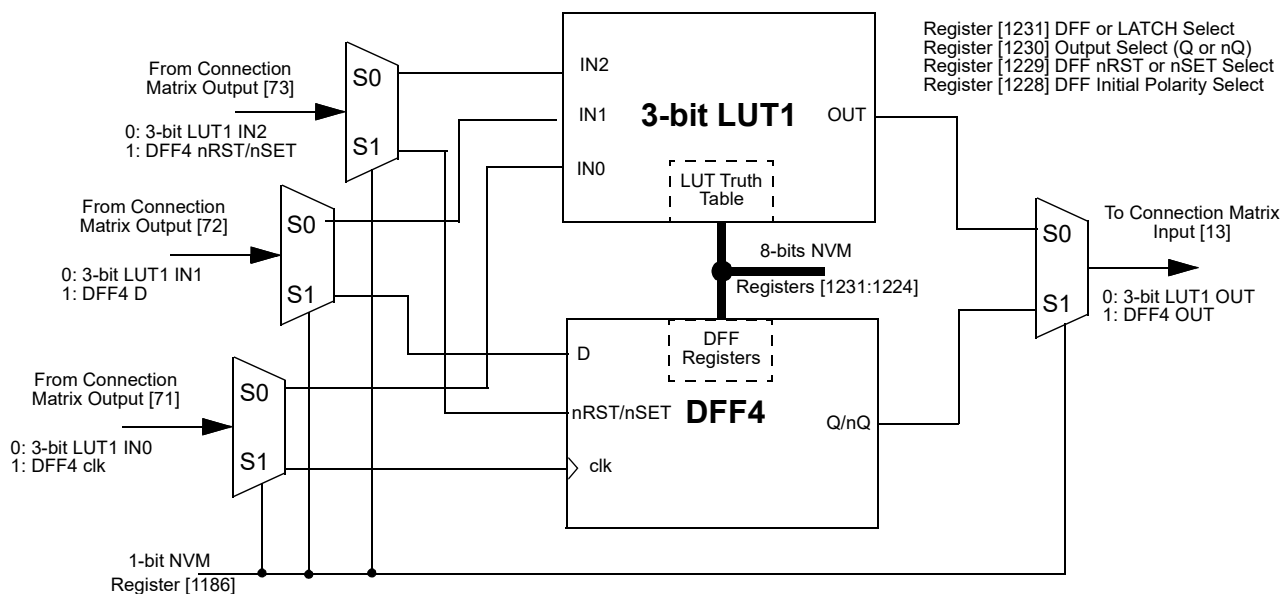


Figure 17. 3-bit LUT1 or DFF4 with RST/SET

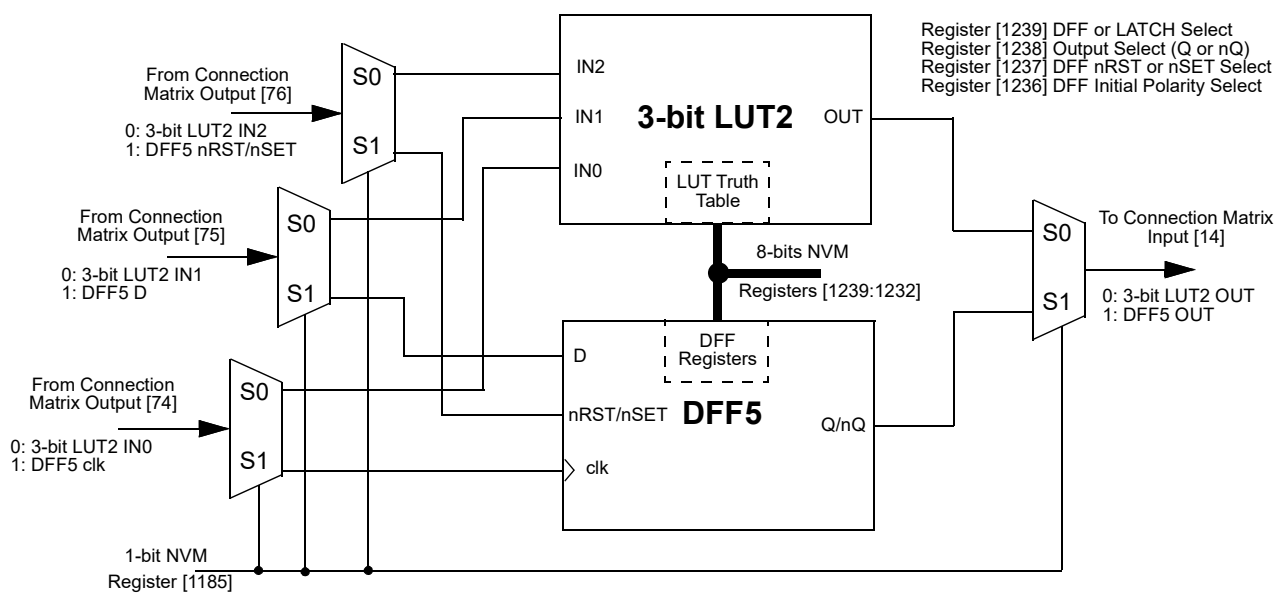


Figure 18. 3-bit LUT2 or DFF5 with RST/SET

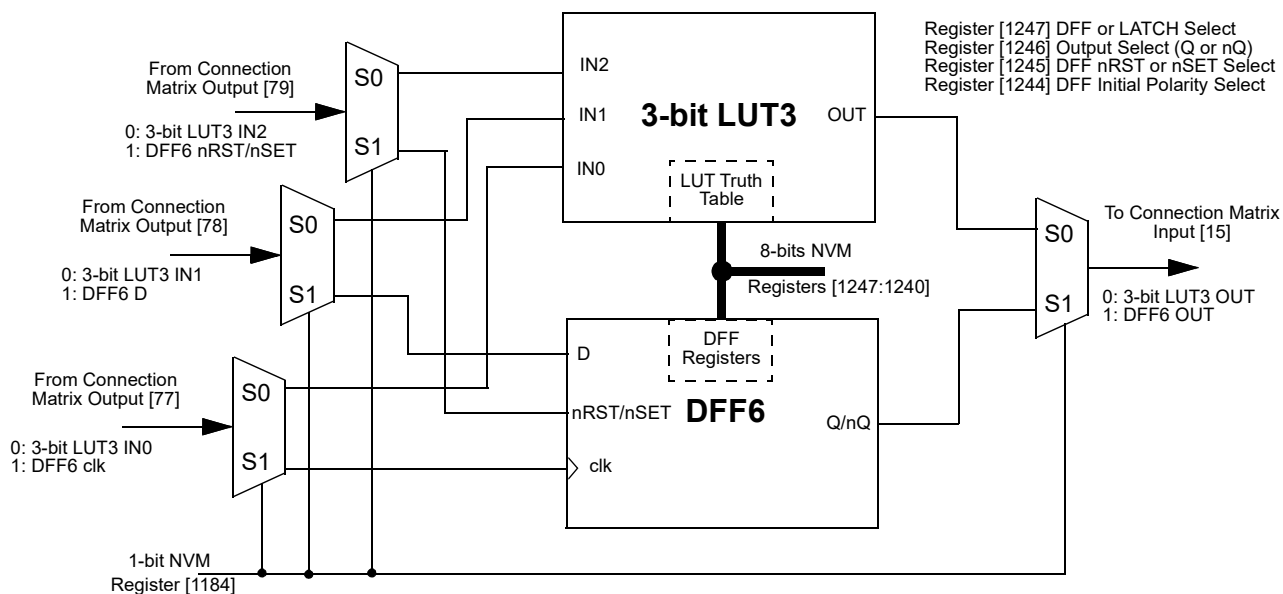


Figure 19. 3-bit LUT3 or DFF6 with RST/SET

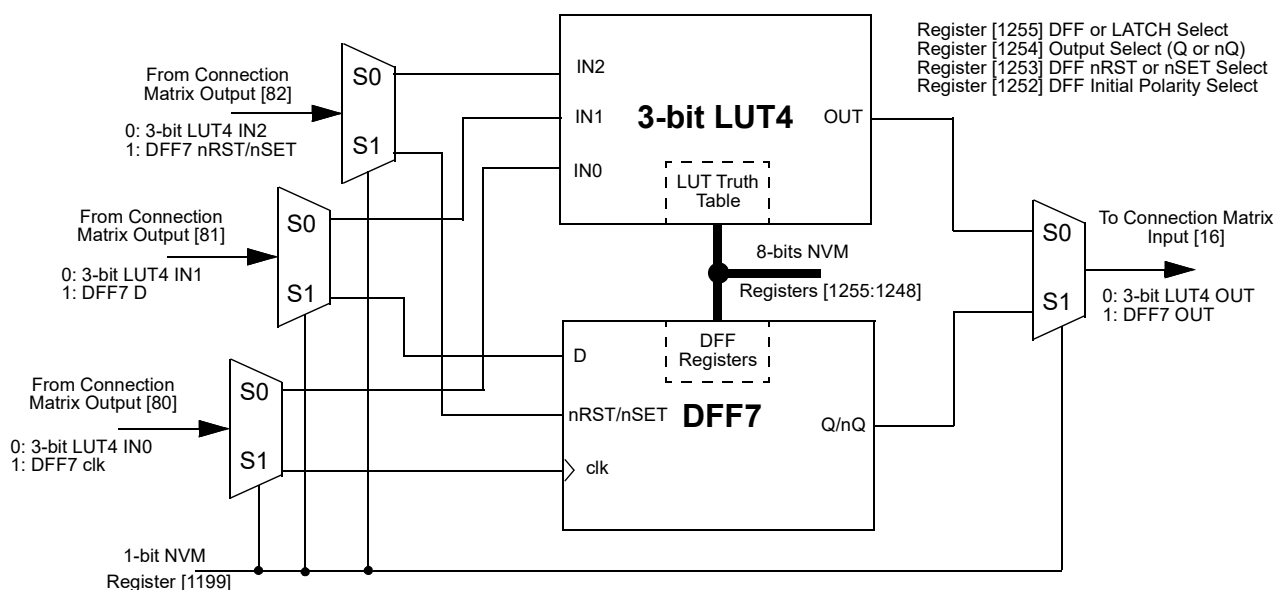


Figure 20. 3-bit LUT4 or DFF7 with RST/SET

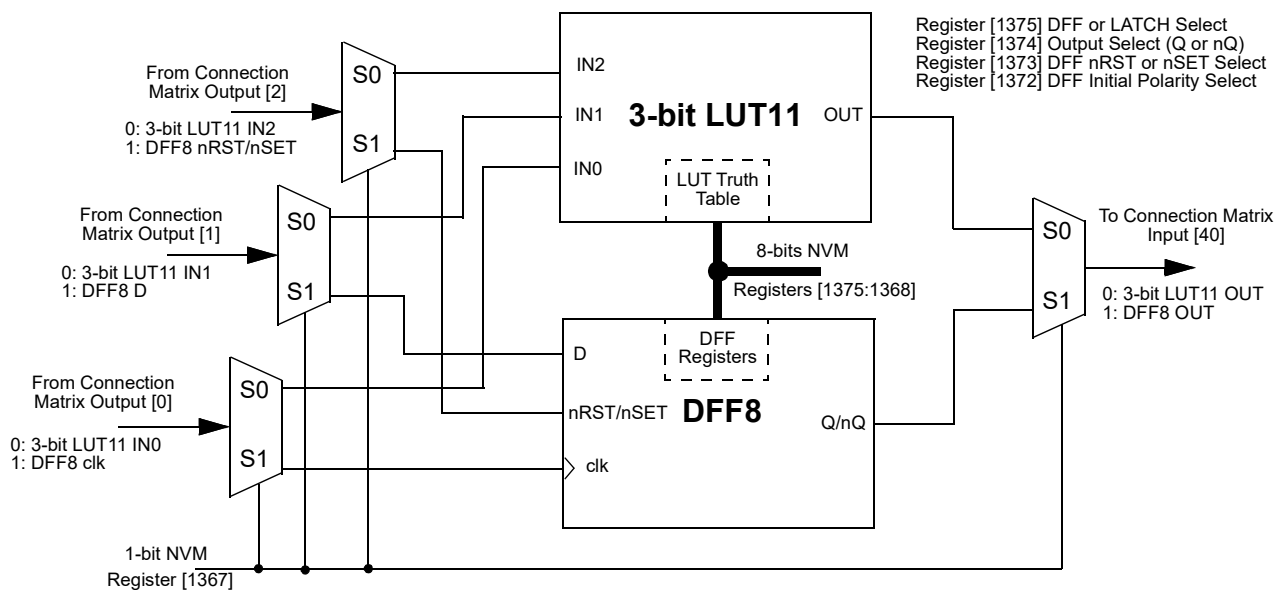


Figure 21. 3-bit LUT11 or DFF8 with RST/SET

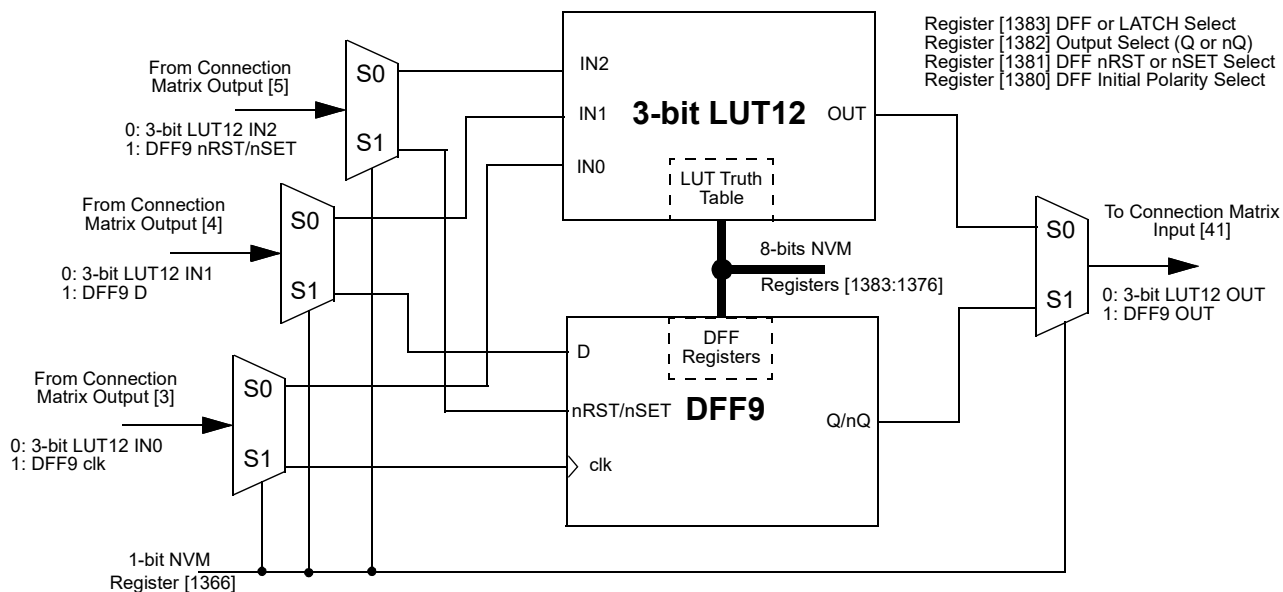


Figure 22. 3-bit LUT12 or DFF9 with RST/SET

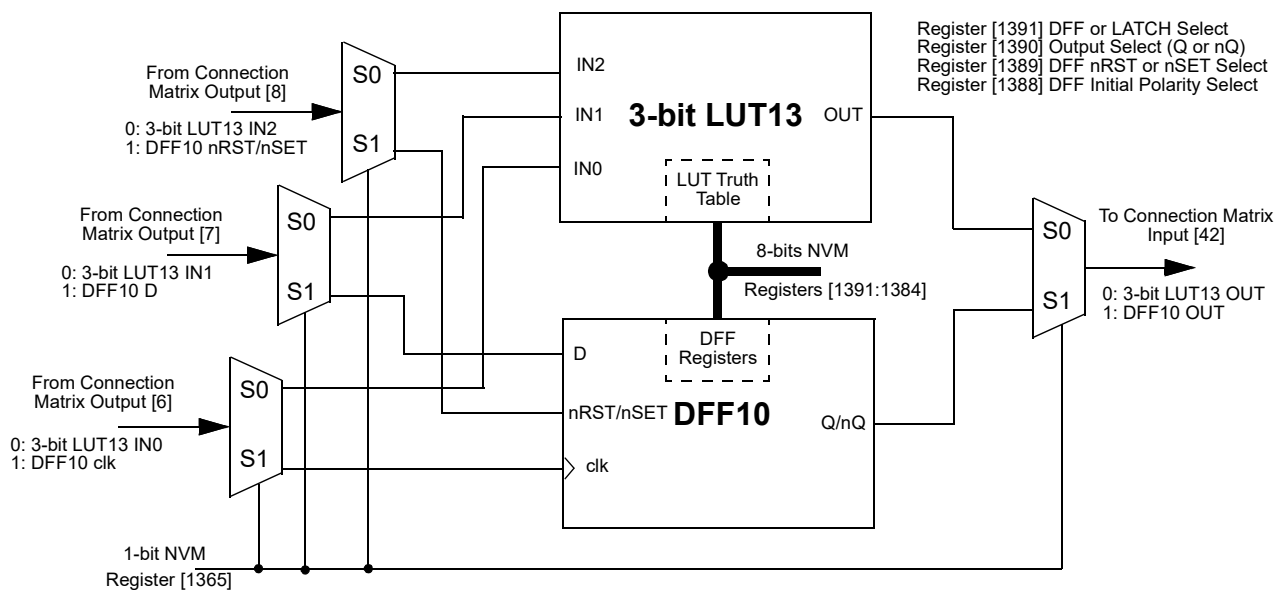


Figure 23. 3-bit LUT13 or DFF10 with RST/SET

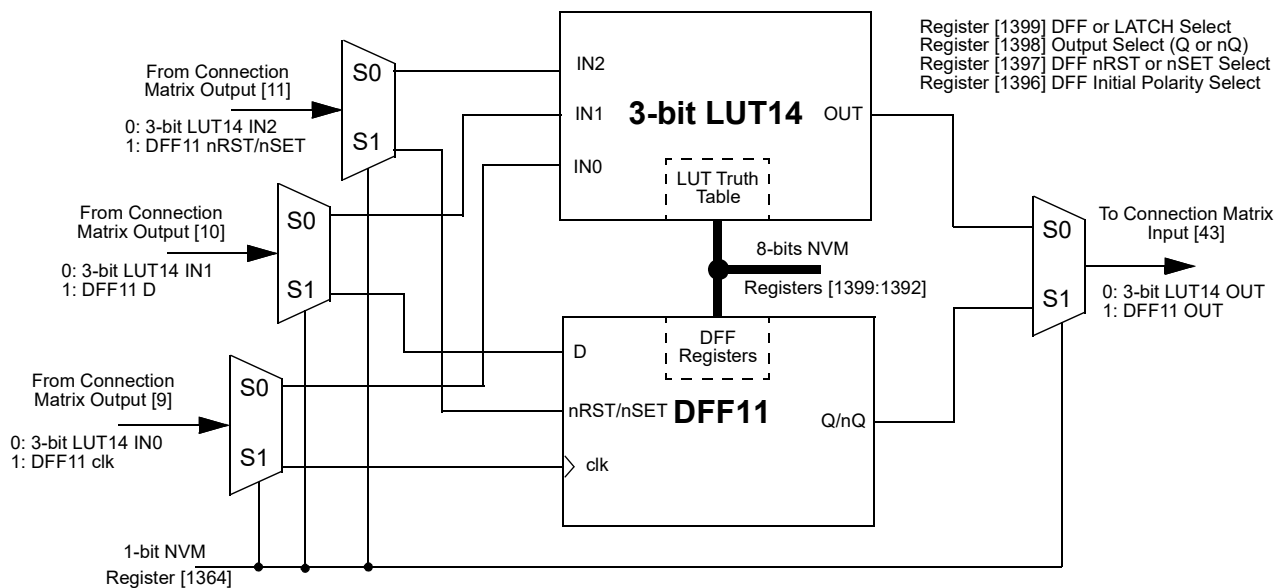


Figure 24. 3-bit LUT14 or DFF11 with RST/SET

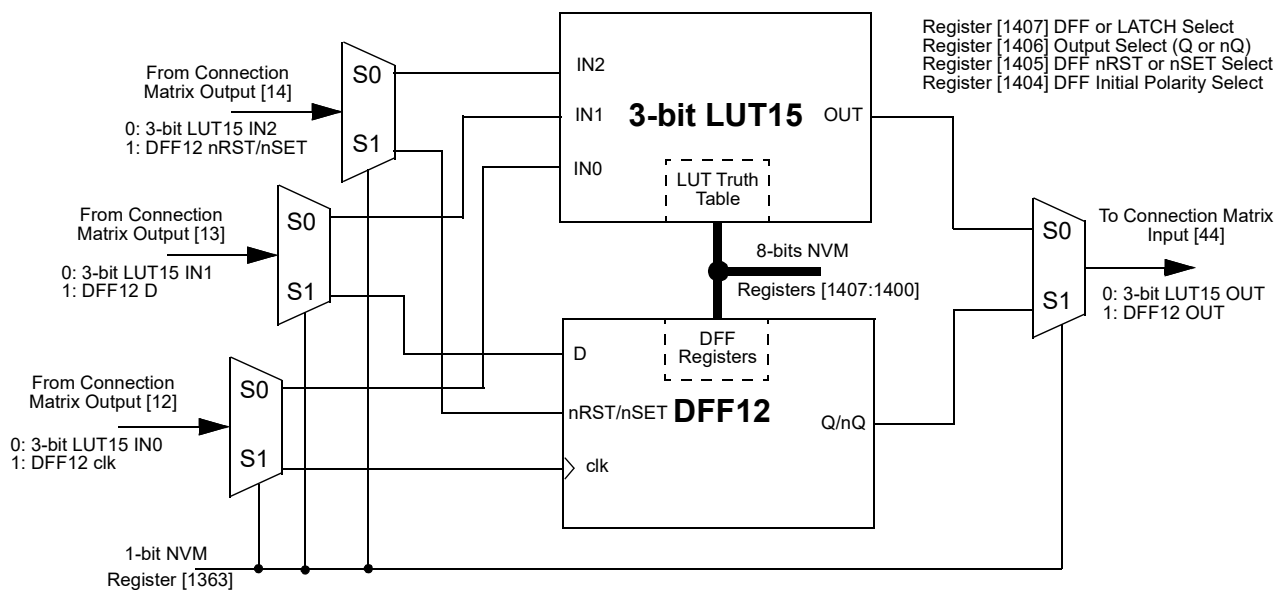


Figure 25. 3-bit LUT15 or DFF12 with RST/SET

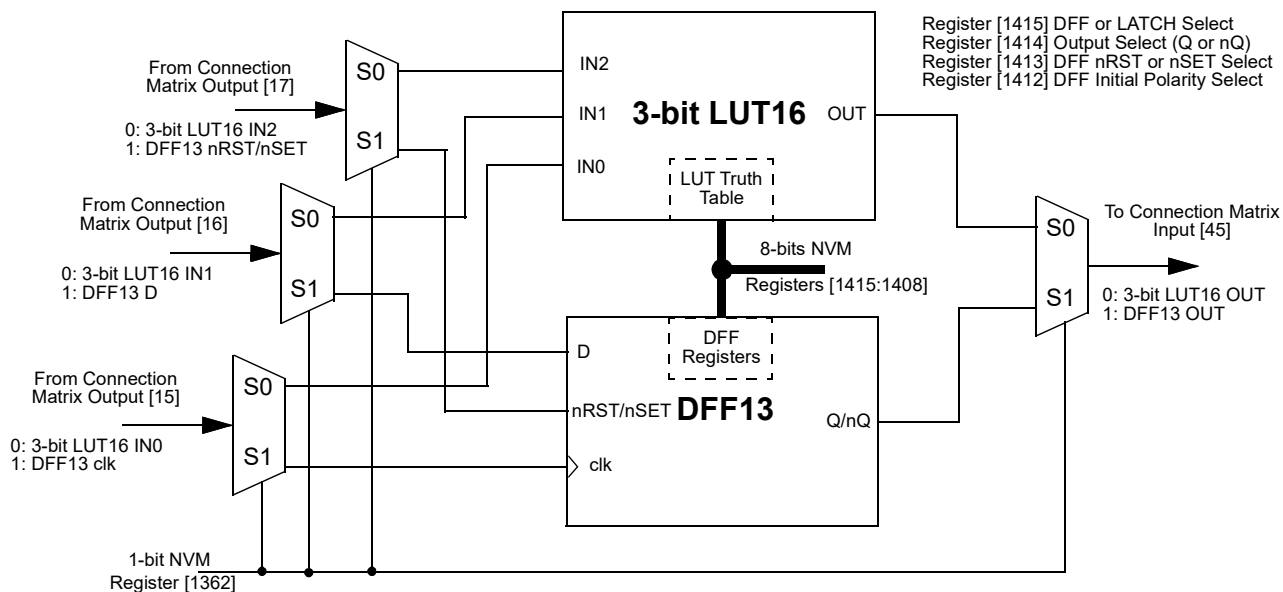
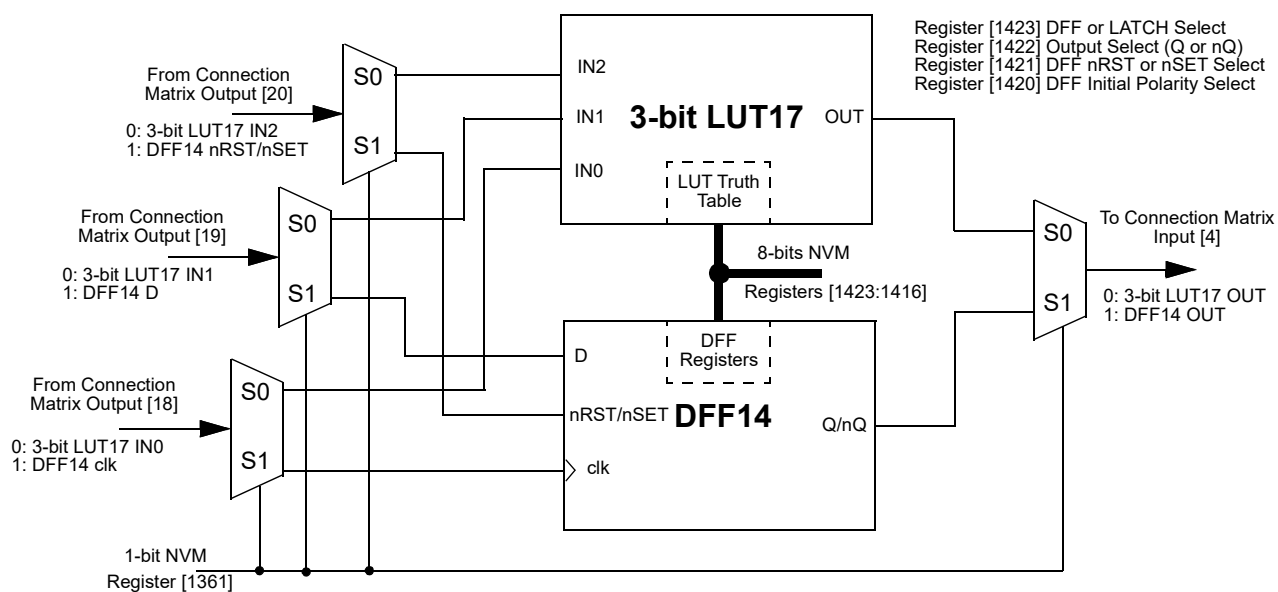


Figure 26. 3-bit LUT16 or DFF13 with RST/SET



**Figure 27. 3-bit LUT17 or DFF14 with RST/SET**

## 7.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 11. 3-bit LUT0 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1216] | LSB |
| 0   | 0   | 1   | register [1217] |     |
| 0   | 1   | 0   | register [1218] |     |
| 0   | 1   | 1   | register [1219] |     |
| 1   | 0   | 0   | register [1220] |     |
| 1   | 0   | 1   | register [1221] |     |
| 1   | 1   | 0   | register [1222] |     |
| 1   | 1   | 1   | register [1223] | MSB |

Table 14. 3-bit LUT3 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1240] | LSB |
| 0   | 0   | 1   | register [1241] |     |
| 0   | 1   | 0   | register [1242] |     |
| 0   | 1   | 1   | register [1243] |     |
| 1   | 0   | 0   | register [1244] |     |
| 1   | 0   | 1   | register [1245] |     |
| 1   | 1   | 0   | register [1246] |     |
| 1   | 1   | 1   | register [1247] | MSB |

Table 12. 3-bit LUT1 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1224] | LSB |
| 0   | 0   | 1   | register [1225] |     |
| 0   | 1   | 0   | register [1226] |     |
| 0   | 1   | 1   | register [1227] |     |
| 1   | 0   | 0   | register [1228] |     |
| 1   | 0   | 1   | register [1229] |     |
| 1   | 1   | 0   | register [1230] |     |
| 1   | 1   | 1   | register [1231] | MSB |

Table 15. 3-bit LUT4 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1248] | LSB |
| 0   | 0   | 1   | register [1249] |     |
| 0   | 1   | 0   | register [1250] |     |
| 0   | 1   | 1   | register [1251] |     |
| 1   | 0   | 0   | register [1252] |     |
| 1   | 0   | 1   | register [1253] |     |
| 1   | 1   | 0   | register [1254] |     |
| 1   | 1   | 1   | register [1255] | MSB |

Table 13. 3-bit LUT2 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1232] | LSB |
| 0   | 0   | 1   | register [1233] |     |
| 0   | 1   | 0   | register [1234] |     |
| 0   | 1   | 1   | register [1235] |     |
| 1   | 0   | 0   | register [1236] |     |
| 1   | 0   | 1   | register [1237] |     |
| 1   | 1   | 0   | register [1238] |     |
| 1   | 1   | 1   | register [1239] | MSB |

Table 16. 3-bit LUT11 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1368] | LSB |
| 0   | 0   | 1   | register [1369] |     |
| 0   | 1   | 0   | register [1370] |     |
| 0   | 1   | 1   | register [1371] |     |
| 1   | 0   | 0   | register [1372] |     |
| 1   | 0   | 1   | register [1373] |     |
| 1   | 1   | 0   | register [1374] |     |
| 1   | 1   | 1   | register [1375] | MSB |

Table 17. 3-bit LUT12 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1376] | LSB |
| 0   | 0   | 1   | register [1377] |     |
| 0   | 1   | 0   | register [1378] |     |
| 0   | 1   | 1   | register [1379] |     |
| 1   | 0   | 0   | register [1380] |     |
| 1   | 0   | 1   | register [1381] |     |
| 1   | 1   | 0   | register [1382] |     |
| 1   | 1   | 1   | register [1383] | MSB |

Table 20. 3-bit LUT15 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1400] | LSB |
| 0   | 0   | 1   | register [1401] |     |
| 0   | 1   | 0   | register [1402] |     |
| 0   | 1   | 1   | register [1403] |     |
| 1   | 0   | 0   | register [1404] |     |
| 1   | 0   | 1   | register [1405] |     |
| 1   | 1   | 0   | register [1406] |     |
| 1   | 1   | 1   | register [1407] | MSB |

Table 18. 3-bit LUT13 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1384] | LSB |
| 0   | 0   | 1   | register [1385] |     |
| 0   | 1   | 0   | register [1386] |     |
| 0   | 1   | 1   | register [1387] |     |
| 1   | 0   | 0   | register [1388] |     |
| 1   | 0   | 1   | register [1389] |     |
| 1   | 1   | 0   | register [1390] |     |
| 1   | 1   | 1   | register [1391] | MSB |

Table 21. 3-bit LUT16 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1408] | LSB |
| 0   | 0   | 1   | register [1409] |     |
| 0   | 1   | 0   | register [1410] |     |
| 0   | 1   | 1   | register [1411] |     |
| 1   | 0   | 0   | register [1412] |     |
| 1   | 0   | 1   | register [1413] |     |
| 1   | 1   | 0   | register [1414] |     |
| 1   | 1   | 1   | register [1415] | MSB |

Table 19. 3-bit LUT14 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1392] | LSB |
| 0   | 0   | 1   | register [1393] |     |
| 0   | 1   | 0   | register [1394] |     |
| 0   | 1   | 1   | register [1395] |     |
| 1   | 0   | 0   | register [1396] |     |
| 1   | 0   | 1   | register [1397] |     |
| 1   | 1   | 0   | register [1398] |     |
| 1   | 1   | 1   | register [1399] | MSB |

Table 22. 3-bit LUT17 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1416] | LSB |
| 0   | 0   | 1   | register [1417] |     |
| 0   | 1   | 0   | register [1418] |     |
| 0   | 1   | 1   | register [1419] |     |
| 1   | 0   | 0   | register [1420] |     |
| 1   | 0   | 1   | register [1421] |     |
| 1   | 1   | 0   | register [1422] |     |
| 1   | 1   | 1   | register [1423] | MSB |

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-bit LUT0 is defined by registers [1223:1216]
- 3-bit LUT1 is defined by registers [1231:1224]
- 3-bit LUT2 is defined by registers [1239:1232]
- 3-bit LUT3 is defined by registers [1247:1240]
- 3-bit LUT4 is defined by registers [1255:1248]
- 3-bit LUT11 is defined by registers [1375:1368]

- 3-bit LUT12 is defined by registers [1383:1376]
- 3-bit LUT13 is defined by registers [1391:1384]
- 3-bit LUT14 is defined by registers [1399:1392]
- 3-bit LUT15 is defined by registers [1407:1400]
- 3-bit LUT16 is defined by registers [1415:1408]
- 3-bit LUT17 is defined by registers [1423:1416].

Table 23 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

**Table 23. 3-bit LUT Standard Digital Functions**

| Function | MSB |   |   |   |   |   |   | LSB |
|----------|-----|---|---|---|---|---|---|-----|
| AND-3    | 1   | 0 | 0 | 0 | 0 | 0 | 0 | 0   |
| NAND-3   | 0   | 1 | 1 | 1 | 1 | 1 | 1 | 1   |
| OR-3     | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 0   |
| NOR-3    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1   |
| XOR-3    | 1   | 0 | 0 | 1 | 0 | 1 | 1 | 0   |
| XNOR-3   | 0   | 1 | 1 | 0 | 1 | 0 | 0 | 1   |

## 7.2.2 Initial Polarity Operations

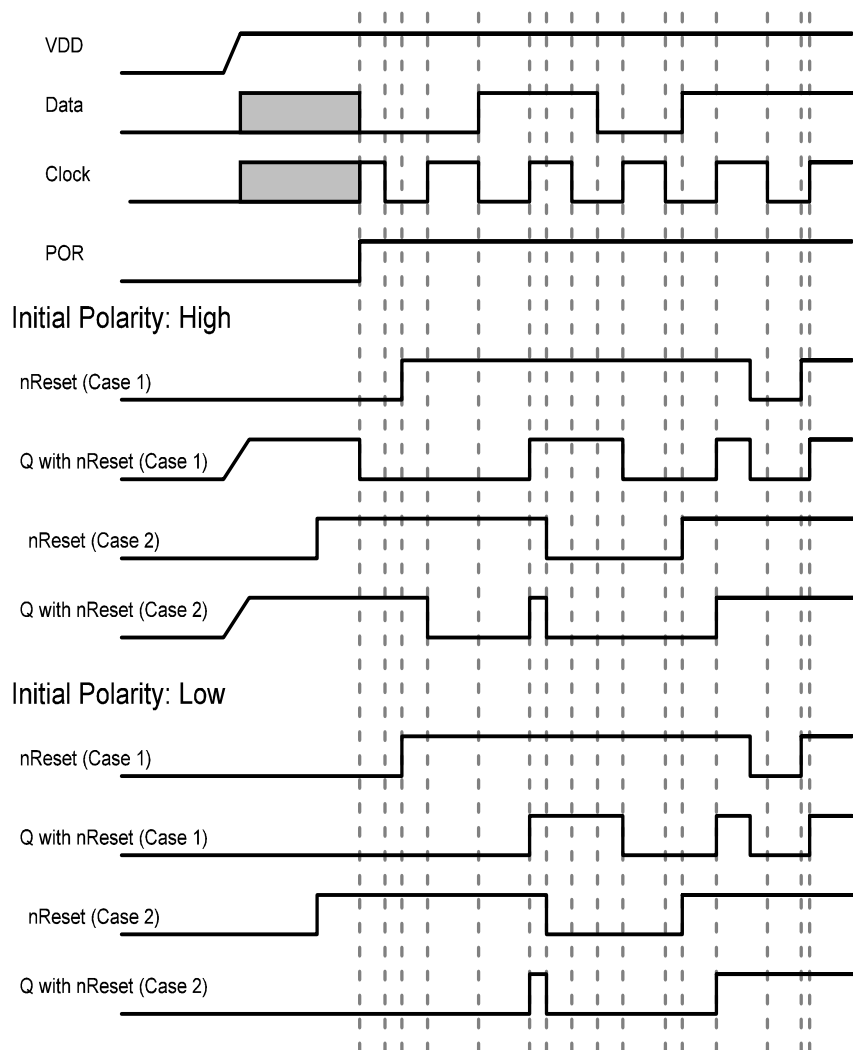


Figure 28. DFF Polarity Operations with nReset

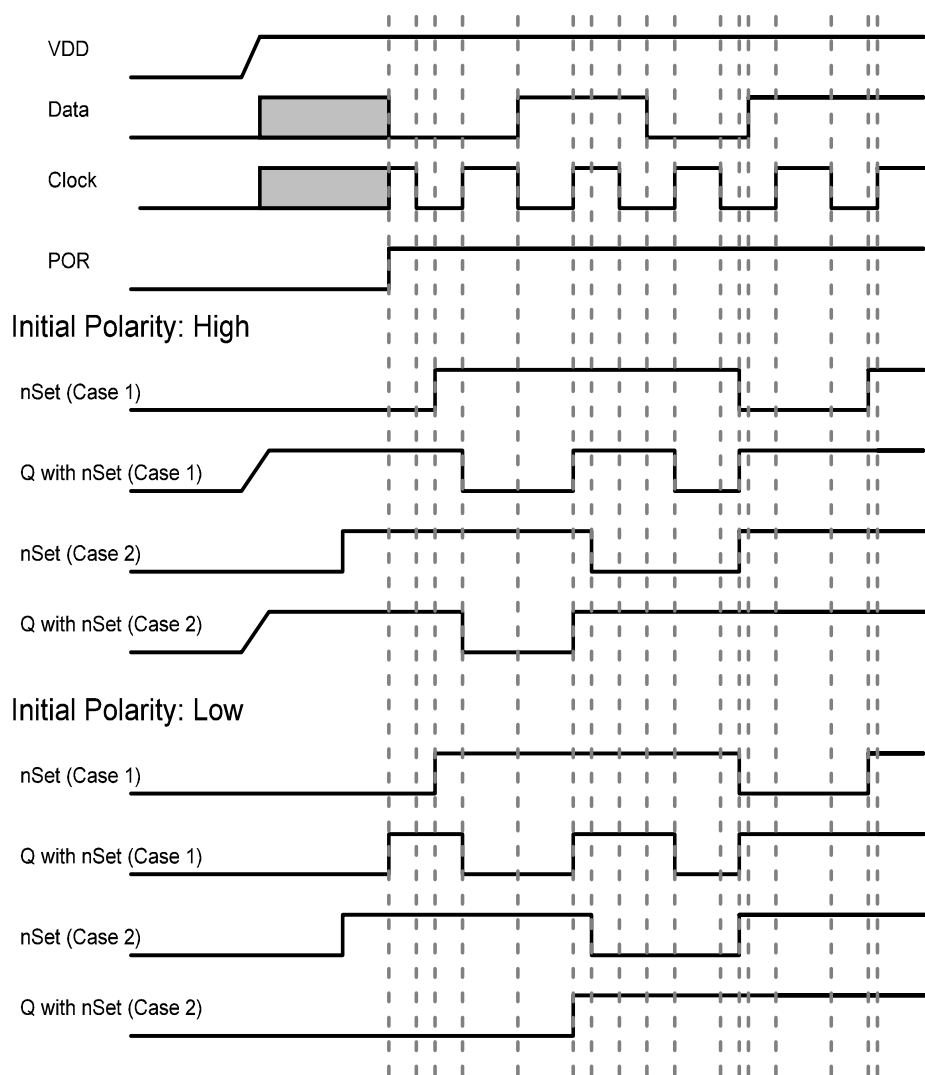


Figure 29. DFF Polarity Operations with nSet

### 7.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three input signals from the matrix: Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (OUT2) is fixed at the output of the first Flip-Flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 16-input mux that is controlled by registers [1259:1256] for OUT0 and registers [1263:1260] for OUT1. The 16-input mux is used to select the amount of delay.

The overall time of the delay is based on the clock used in the SLG46533-E design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the Oscillator within the SLG46533-E). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

**Note:** CLK is rising edge triggered.

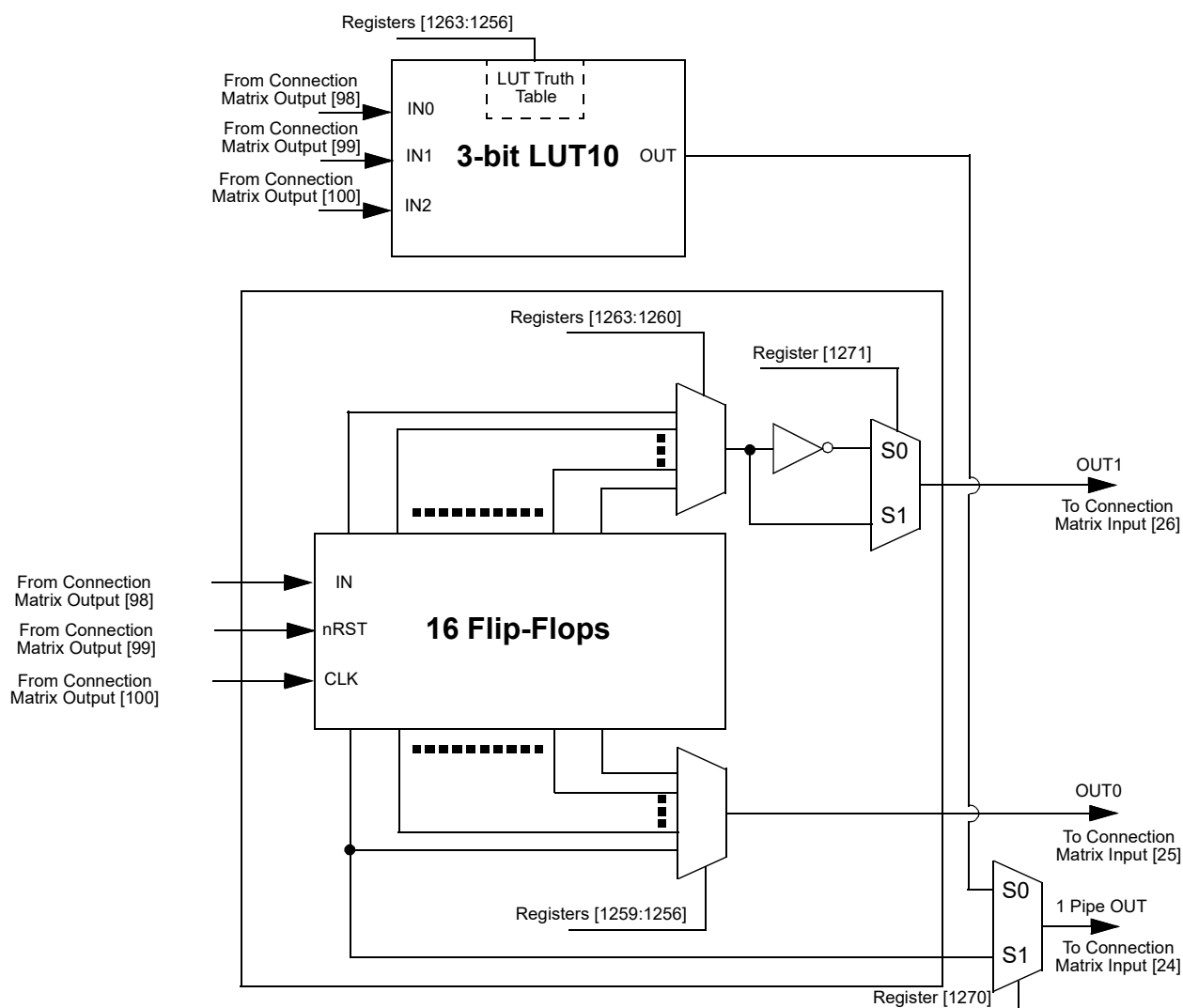


Figure 30. 3-bit LUT10 or Pipe Delay

### 7.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 24. 3-bit LUT10 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1256] | LSB |
| 0   | 0   | 1   | register [1257] |     |
| 0   | 1   | 0   | register [1258] |     |
| 0   | 1   | 1   | register [1259] |     |
| 1   | 0   | 0   | register [1260] |     |
| 1   | 0   | 1   | register [1261] |     |
| 1   | 1   | 0   | register [1262] |     |
| 1   | 1   | 1   | register [1263] | MSB |

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-bit LUT10 is defined by registers [1263:1256].

## 7.4 3-Bit LUT or 8-Bit Counter/Delay Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as Counter/Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter/Delay function, two of the three input signals from the connection matrix go to the external clock (EXT\_CLK) and reset (DLY\_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

For timing diagrams refer to section [7.6 CNT/DLY/FSM Timing Diagrams](#)

**Note:** Counters initialize with counter data after POR.

Two of the five macrocells can have their active count value read via I<sup>2</sup>C (CNT4 and CNT6). See section [15.6.1 Reading Counter Data via I2C](#) for further details.

### 7.4.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

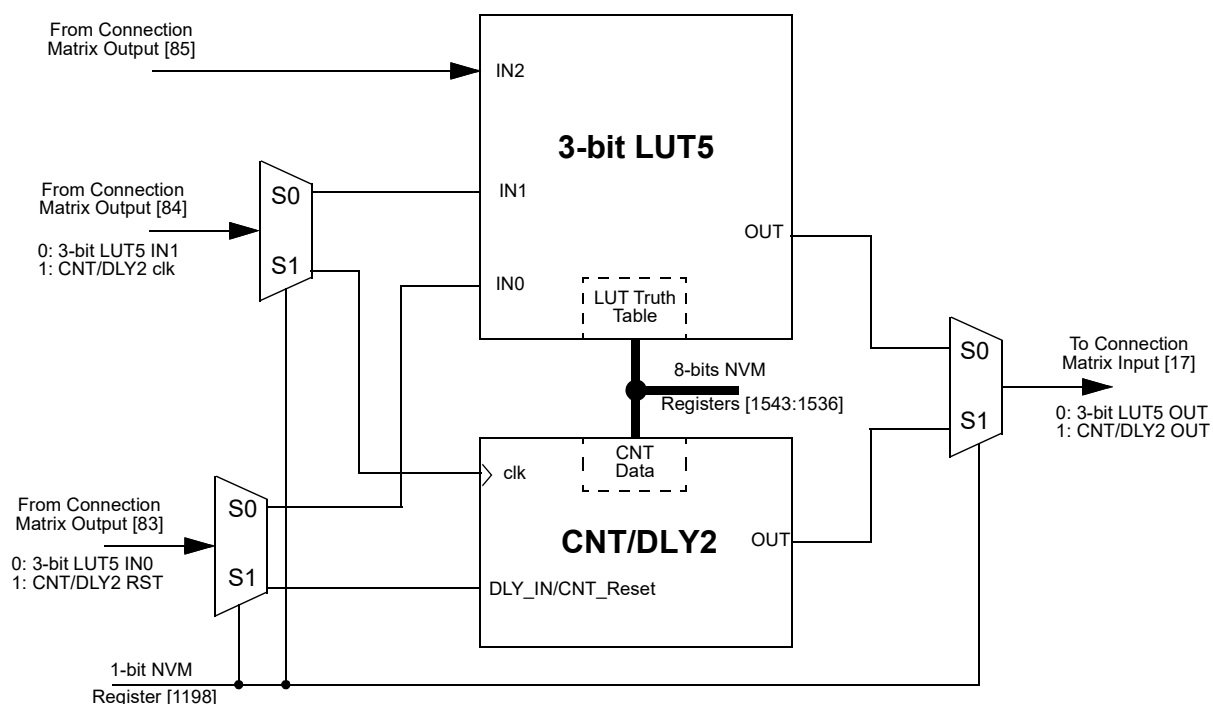


Figure 31. 3-bit LUT5 or CNT/DLY2

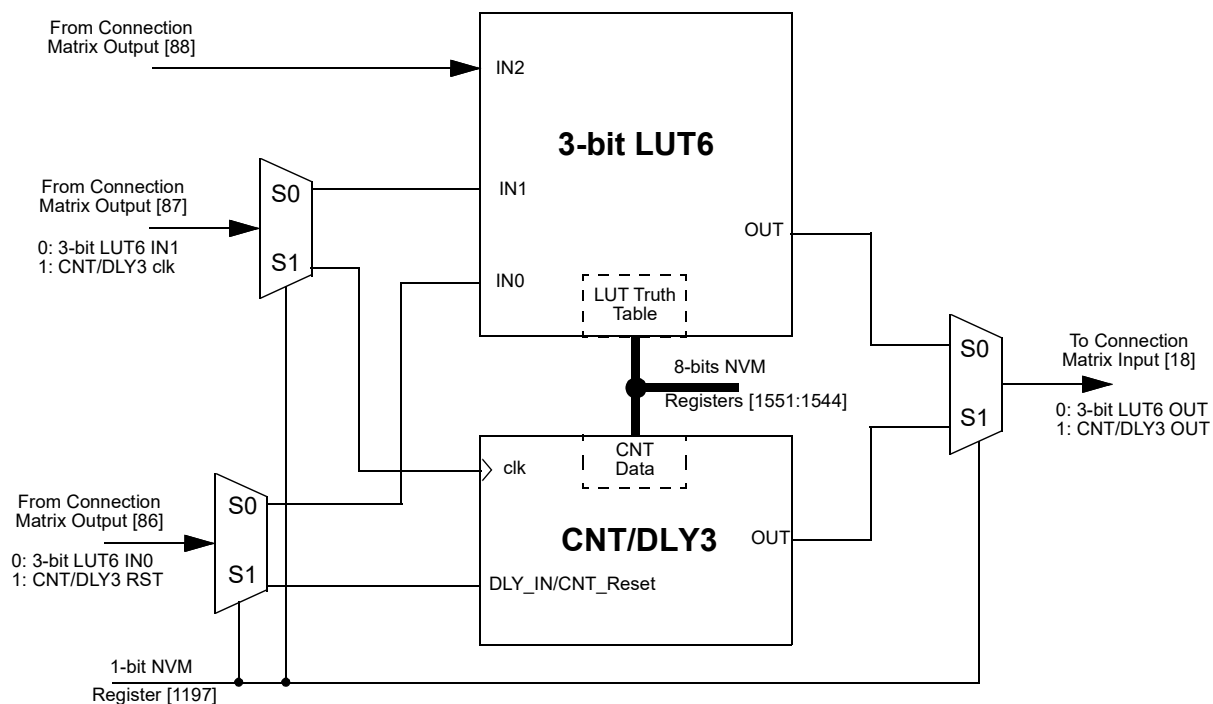


Figure 32. 3-bit LUT6 or CNT/DLY3

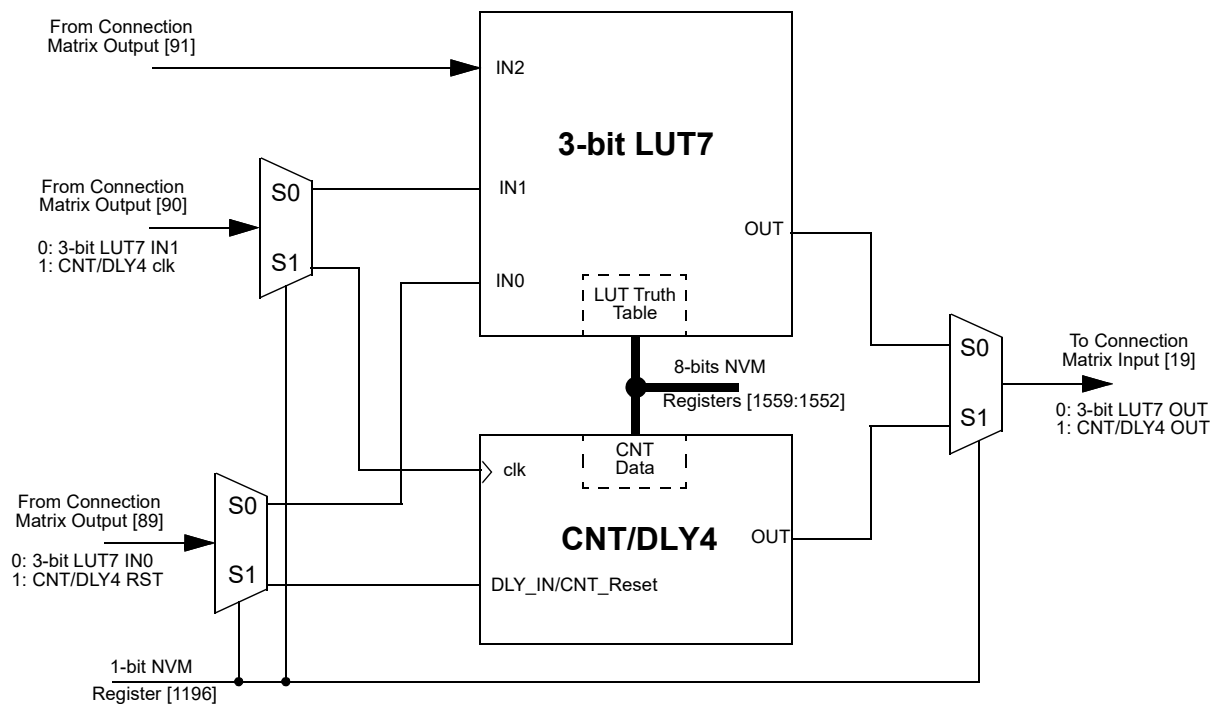


Figure 33. 3-bit LUT7 or CNT/DLY4

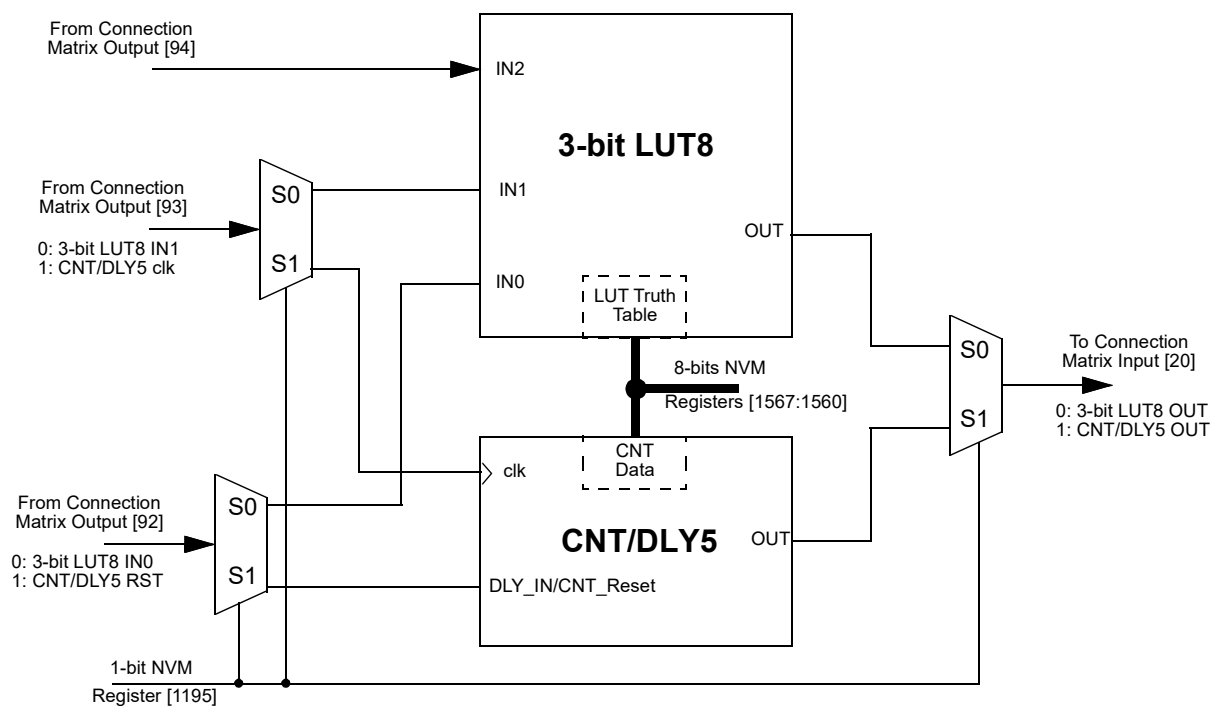


Figure 34. 3-bit LUT8 or CNT/DLY5

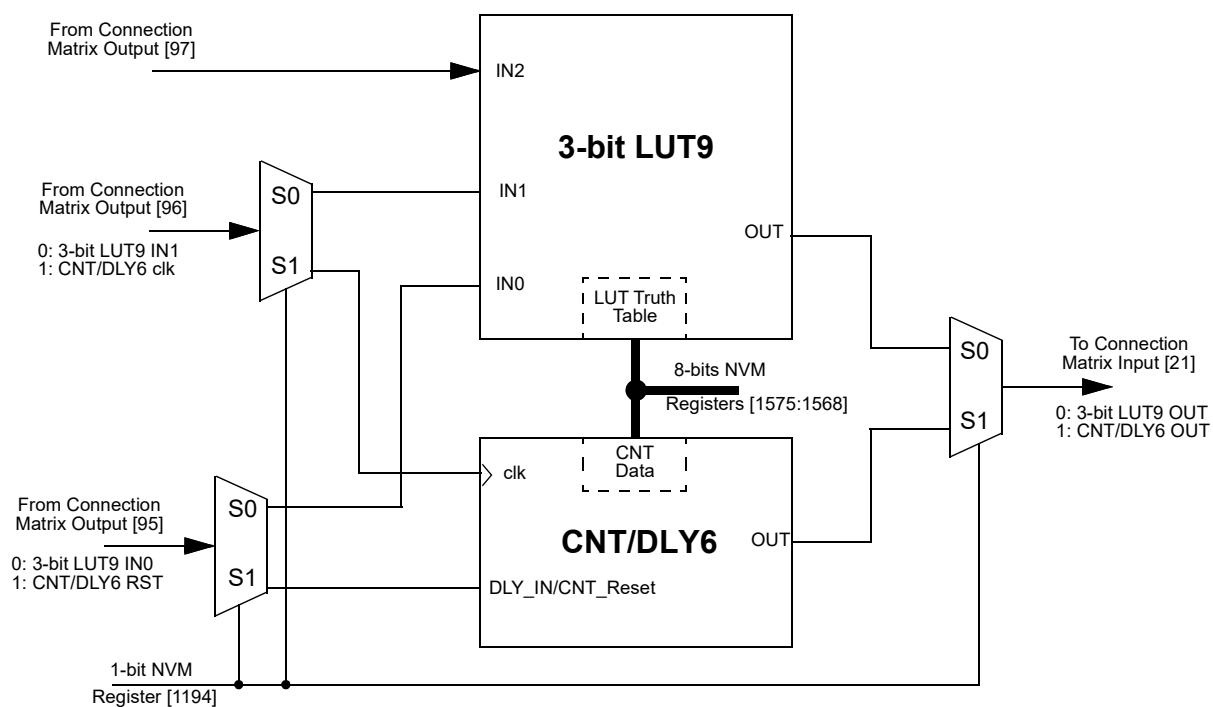


Figure 35. 3-bit LUT9 or CNT/DLY6

## 7.4.2 3-Bit LUT or Counter/Delay Macrocells Used as 3-Bit LUTs

Table 25. 3-bit LUT5 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1536] | LSB |
| 0   | 0   | 1   | register [1537] |     |
| 0   | 1   | 0   | register [1538] |     |
| 0   | 1   | 1   | register [1539] |     |
| 1   | 0   | 0   | register [1540] |     |
| 1   | 0   | 1   | register [1541] |     |
| 1   | 1   | 0   | register [1542] |     |
| 1   | 1   | 1   | register [1543] | MSB |

Table 28. 3-bit LUT8 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1560] | LSB |
| 0   | 0   | 1   | register [1561] |     |
| 0   | 1   | 0   | register [1562] |     |
| 0   | 1   | 1   | register [1563] |     |
| 1   | 0   | 0   | register [1564] |     |
| 1   | 0   | 1   | register [1565] |     |
| 1   | 1   | 0   | register [1566] |     |
| 1   | 1   | 1   | register [1567] | MSB |

Table 26. 3-bit LUT6 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1544] | LSB |
| 0   | 0   | 1   | register [1545] |     |
| 0   | 1   | 0   | register [1546] |     |
| 0   | 1   | 1   | register [1547] |     |
| 1   | 0   | 0   | register [1548] |     |
| 1   | 0   | 1   | register [1549] |     |
| 1   | 1   | 0   | register [1550] |     |
| 1   | 1   | 1   | register [1551] | MSB |

Table 29. 3-bit LUT9 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1568] | LSB |
| 0   | 0   | 1   | register [1569] |     |
| 0   | 1   | 0   | register [1570] |     |
| 0   | 1   | 1   | register [1571] |     |
| 1   | 0   | 0   | register [1572] |     |
| 1   | 0   | 1   | register [1573] |     |
| 1   | 1   | 0   | register [1574] |     |
| 1   | 1   | 1   | register [1575] | MSB |

Table 27. 3-bit LUT7 Truth Table

| IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | register [1552] | LSB |
| 0   | 0   | 1   | register [1553] |     |
| 0   | 1   | 0   | register [1554] |     |
| 0   | 1   | 1   | register [1555] |     |
| 1   | 0   | 0   | register [1556] |     |
| 1   | 0   | 1   | register [1557] |     |
| 1   | 1   | 0   | register [1558] |     |
| 1   | 1   | 1   | register [1559] | MSB |

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-bit LUT5 is defined by registers [1543:1536]
- 3-bit LUT6 is defined by registers [1551:1544]
- 3-bit LUT7 is defined by registers [1559:1552]
- 3-bit LUT8 is defined by registers [1567:1560]
- 3-bit LUT9 is defined by registers [1575:1568].

Table 30 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

**Table 30. 3-bit LUT Standard Digital Functions**

| Function | MSB |   |   |   |   |   |   | LSB |
|----------|-----|---|---|---|---|---|---|-----|
| AND-3    | 1   | 0 | 0 | 0 | 0 | 0 | 0 | 0   |
| NAND-3   | 0   | 1 | 1 | 1 | 1 | 1 | 1 | 1   |
| OR-3     | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 0   |
| NOR-3    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1   |
| XOR-3    | 1   | 0 | 0 | 1 | 0 | 1 | 1 | 0   |
| XNOR-3   | 0   | 1 | 1 | 0 | 1 | 0 | 0 | 1   |

## 7.5 4-Bit LUT or 16-Bit Counter/Delay Macrocells

There are two macrocells that can serve as either 4-bit LUTs or as 16-bit Counter/Delays. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, four input signals from the connection matrix go to the external clock (EXT\_CLK) and reset (DLY\_IN/CNT\_Reset), Keep and Up for the Counter/Delay, with the output going back to the connection matrix.

These two macrocells have an optional Finite State Machine (FSM) function. There are two matrix inputs for Up and Keep to support FSM functionality. Any counter within GreenPAK is counting down by default. In FSM mode (CNT/DLY0 and CNT/DLY1) it is possible to reverse counting by applying High level to Up input. Also, there is a possibility to pause counting by applying High level to Keep input, after the level goes Low, the counter will proceed counting.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection.

Delay time and Output Period can be calculated using the following formulas:

- Delay time:  $[(\text{Counter data} + 2)/\text{CLK input frequency} - \text{Offset}^*]$
- Output Period:  $[(\text{Counter data} + 1)/\text{CLK input frequency} - \text{Offset}^*]$ .

One Shot pulse width can be calculated using formula:

- Pulse width =  $[(\text{Counter Data} + 2)/\text{CLK input frequency} - \text{Offset}^*]$ .

\*Offset is the asynchronous time offset between the input signal and the first clock pulse.

**Note:** Counters initialize with counter data after POR

For timing diagrams refer to section [7.6 CNT/DLY/FSM Timing Diagrams](#).

Both of these macrocells can have their active count value read via I<sup>2</sup>C. See section [15.6.1 Reading Counter Data via I<sup>2</sup>C](#) for further details.

### 7.5.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

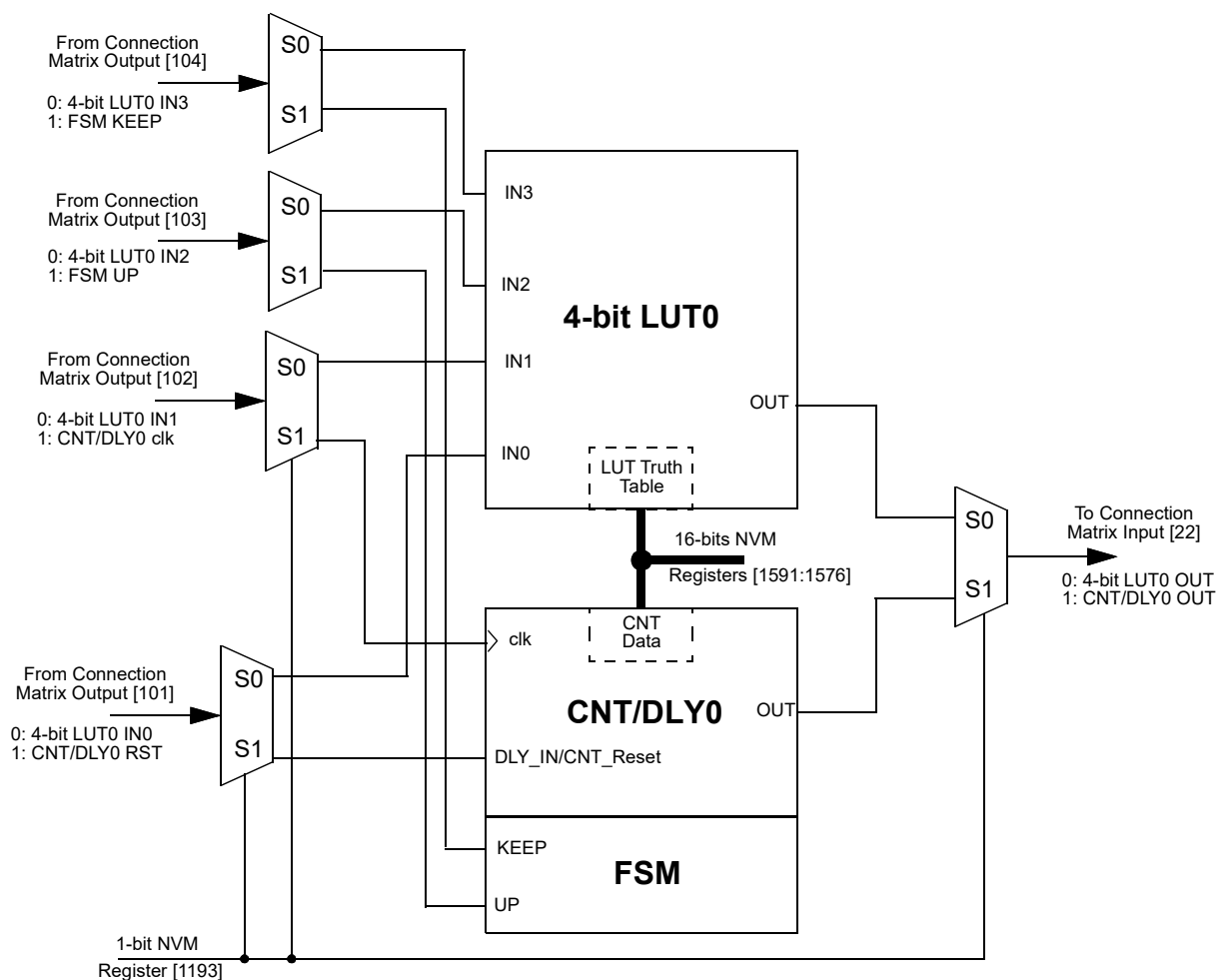


Figure 36. 4-bit LUT0 or CNT/DLY0

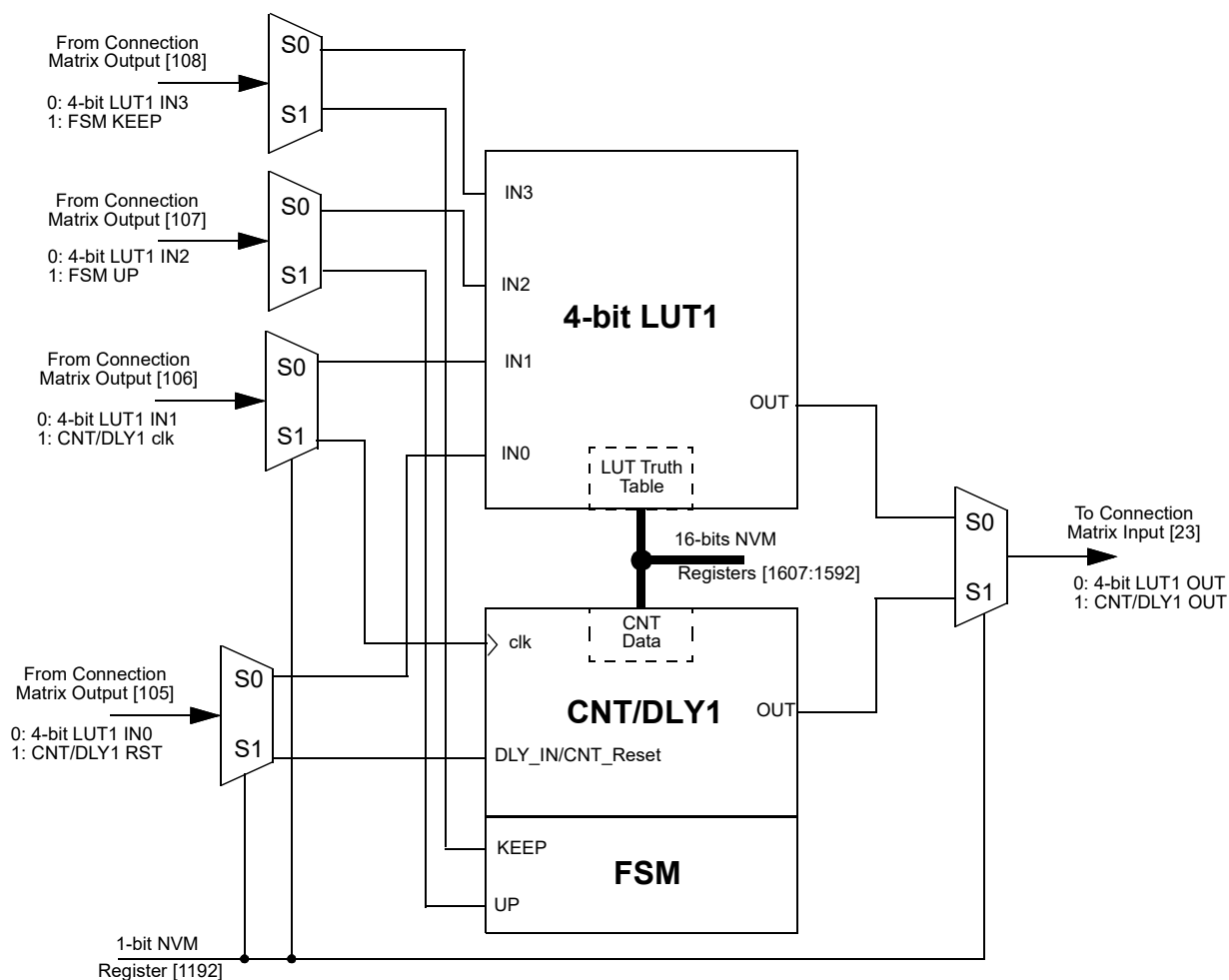


Figure 37. 4-bit LUT1 or CNT/DLY1

## 7.5.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 31. 4-bit LUT0 Truth Table

| IN3 | IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | 0   | register [1576] | LSB |
| 0   | 0   | 0   | 1   | register [1577] |     |
| 0   | 0   | 1   | 0   | register [1578] |     |
| 0   | 0   | 1   | 1   | register [1579] |     |
| 0   | 1   | 0   | 0   | register [1580] |     |
| 0   | 1   | 0   | 1   | register [1581] |     |
| 0   | 1   | 1   | 0   | register [1582] |     |
| 0   | 1   | 1   | 1   | register [1583] |     |
| 1   | 0   | 0   | 0   | register [1584] |     |
| 1   | 0   | 0   | 1   | register [1585] |     |
| 1   | 0   | 1   | 0   | register [1586] |     |
| 1   | 0   | 1   | 1   | register [1587] |     |
| 1   | 1   | 0   | 0   | register [1588] |     |
| 1   | 1   | 0   | 1   | register [1589] |     |
| 1   | 1   | 1   | 0   | register [1590] |     |
| 1   | 1   | 1   | 1   | register [1591] | MSB |

Table 32. 4-bit LUT1 Truth Table

| IN3 | IN2 | IN1 | IN0 | OUT             |     |
|-----|-----|-----|-----|-----------------|-----|
| 0   | 0   | 0   | 0   | register [1592] | LSB |
| 0   | 0   | 0   | 1   | register [1593] |     |
| 0   | 0   | 1   | 0   | register [1594] |     |
| 0   | 0   | 1   | 1   | register [1595] |     |
| 0   | 1   | 0   | 0   | register [1596] |     |
| 0   | 1   | 0   | 1   | register [1597] |     |
| 0   | 1   | 1   | 0   | register [1598] |     |
| 0   | 1   | 1   | 1   | register [1599] |     |
| 1   | 0   | 0   | 0   | register [1600] |     |
| 1   | 0   | 0   | 1   | register [1601] |     |
| 1   | 0   | 1   | 0   | register [1602] |     |
| 1   | 0   | 1   | 1   | register [1603] |     |
| 1   | 1   | 0   | 0   | register [1604] |     |
| 1   | 1   | 0   | 1   | register [1605] |     |
| 1   | 1   | 1   | 0   | register [1606] |     |
| 1   | 1   | 1   | 1   | register [1607] | MSB |

Each macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-bit LUT0 is defined by registers [1591:1576]
- 4-bit LUT1 is defined by registers [1607:1592].

Table 33. 4-bit LUT Standard Digital Functions

| Function | MSB |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LSB |
|----------|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|
| AND-4    | 1   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   |
| NAND-4   | 0   | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1   |
| OR-4     | 1   | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0   |
| NOR-4    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1   |
| XOR-4    | 0   | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0   |
| XNOR-4   | 1   | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1   |

## 7.6 CNT/DLY/FSM Timing Diagrams

### 7.6.1 Delay Mode (Edge Select: Both, Counter Data: 3) CNT/DLY2 to CNT/DLY6

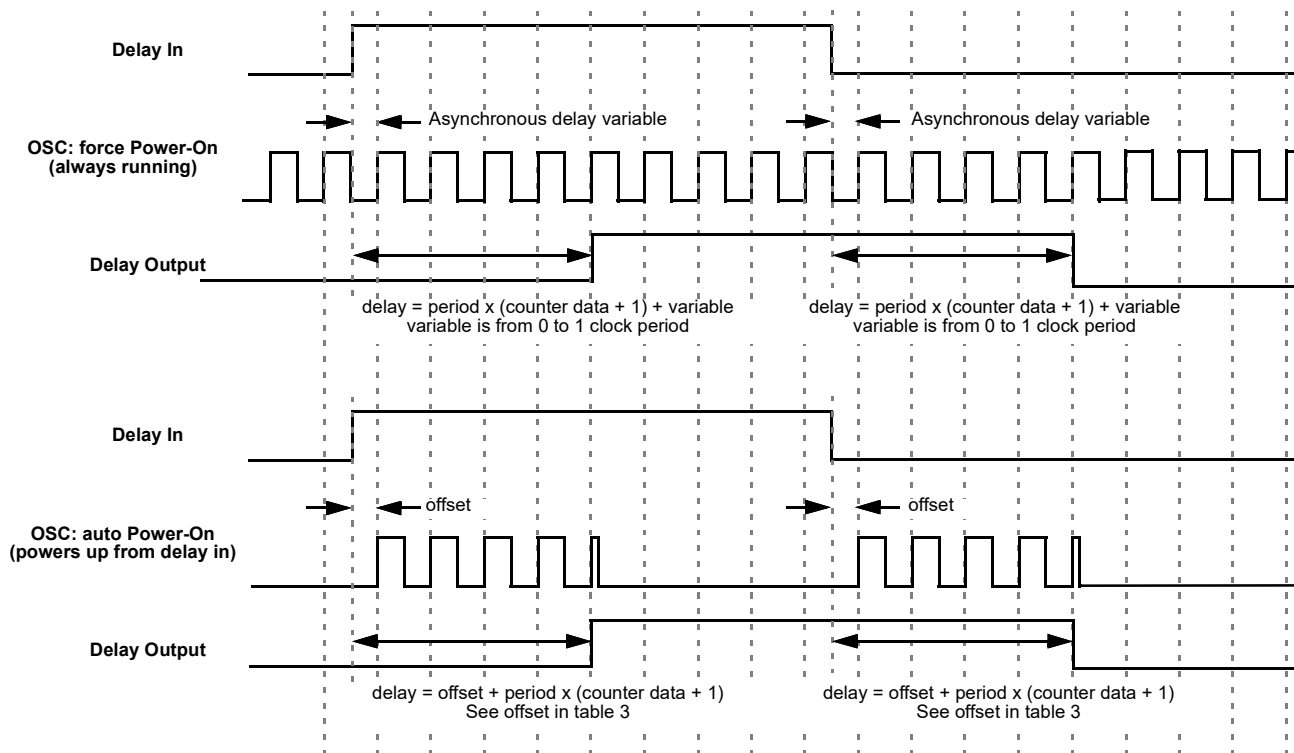


Figure 38. Delay Mode Timing Diagram

### 7.6.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY2 to CNT/DLY6

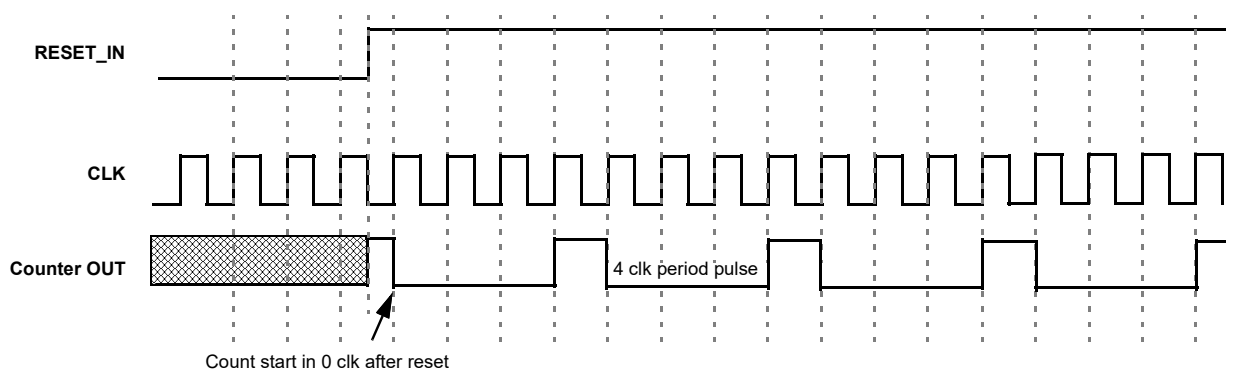


Figure 39. Counter Mode Timing Diagram

### 7.6.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

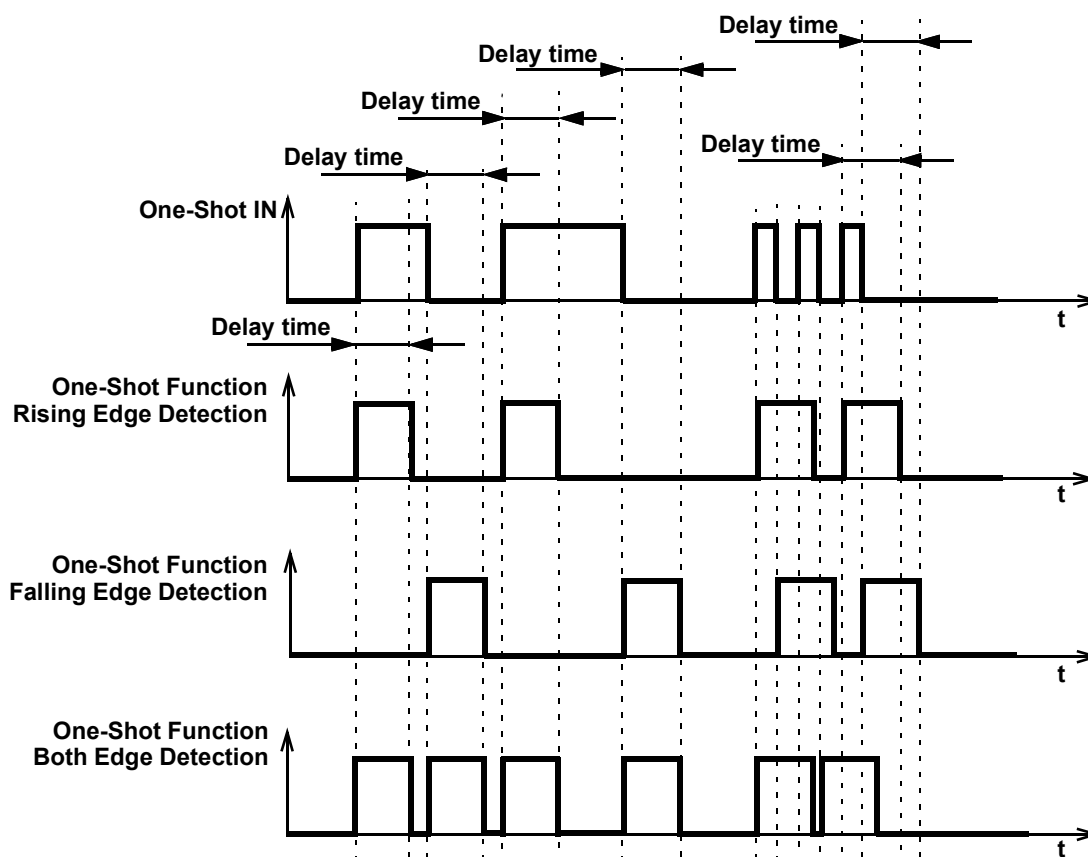


Figure 40. One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

#### 7.6.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

**Rising Edge:** The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

**Falling Edge:** The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

**Both Edge:** The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

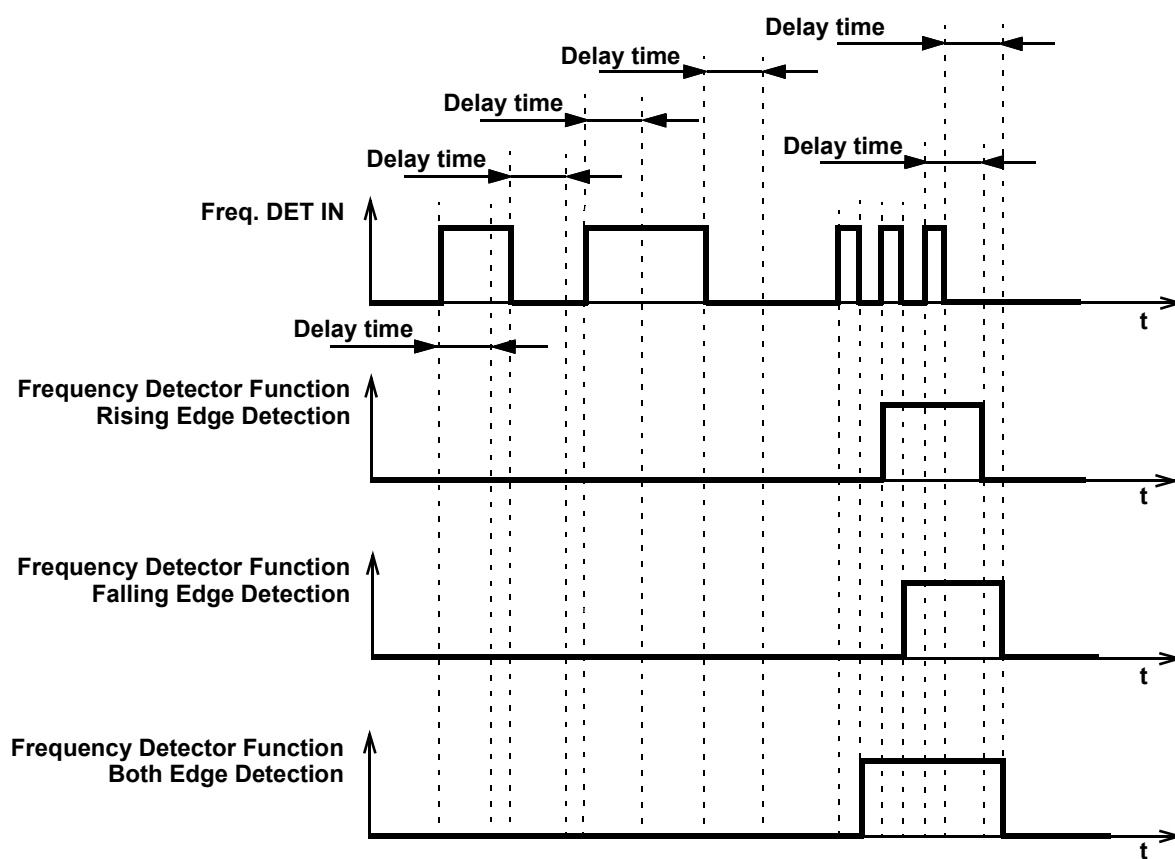


Figure 41. Frequency Detection Mode Timing Diagram

### 7.6.5 Edge Detection Mode CNT/DLY2 to CNT/DLY6

The macrocell generates high level short pulse when detecting the respective edge.

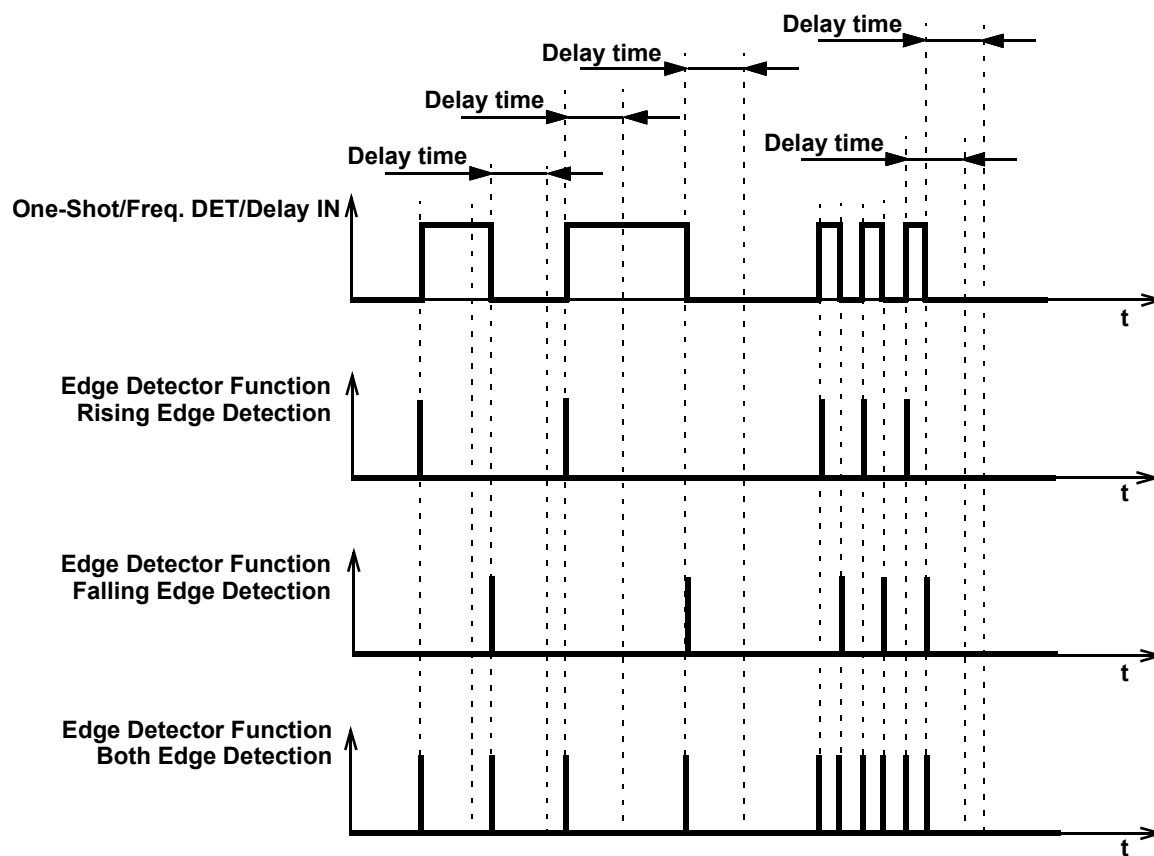


Figure 42. Edge Detection Mode Timing Diagram

### 7.6.6 Delay Mode CNT/DLY0 to CNT/DLY6

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

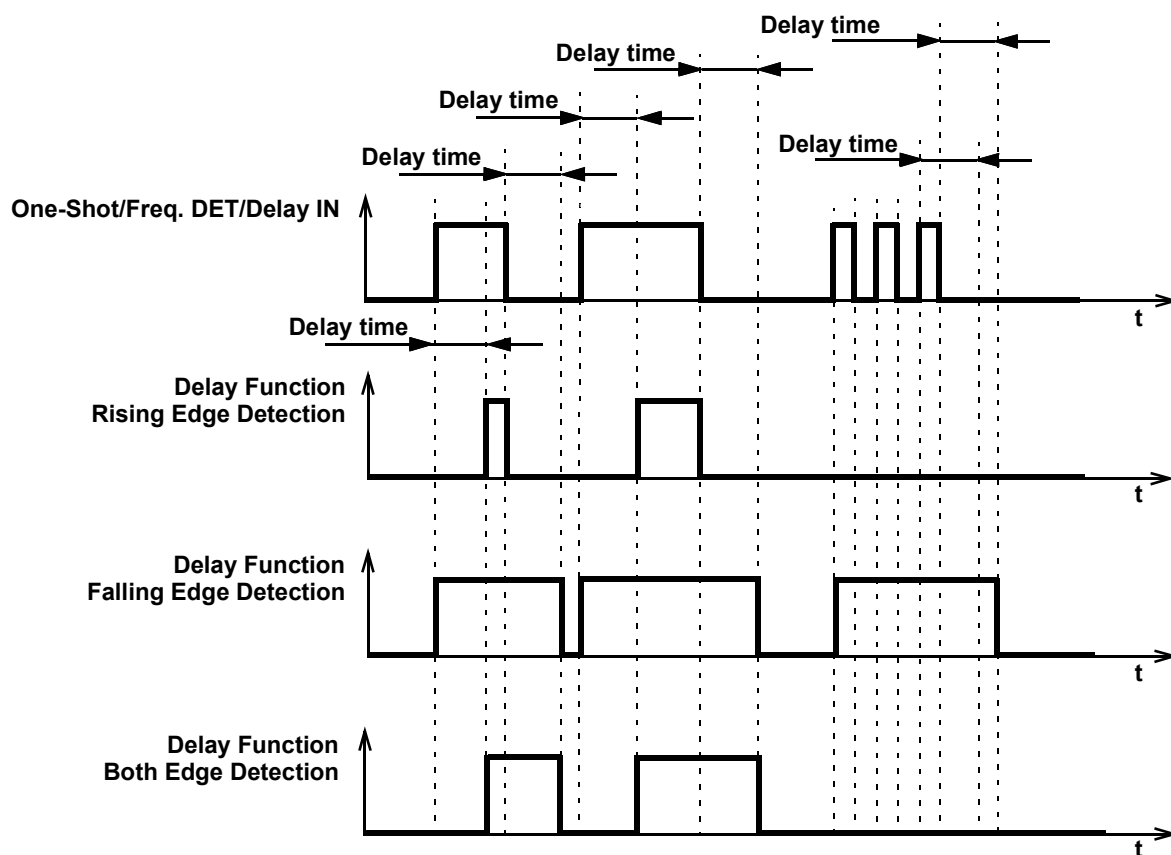


Figure 43. Delay Mode Timing Diagram

7.6.7 CNT/FSM Mode CNT/DLY0, CNT/DLY1

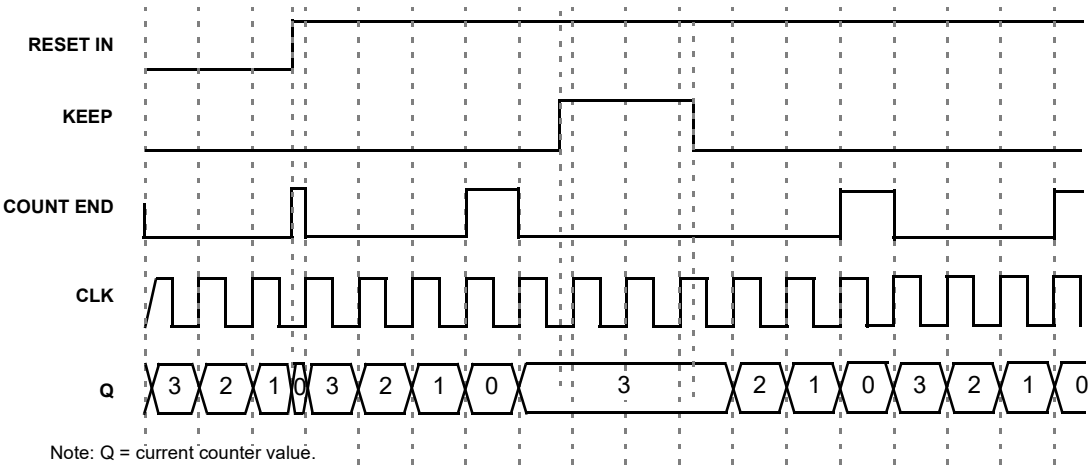


Figure 44. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

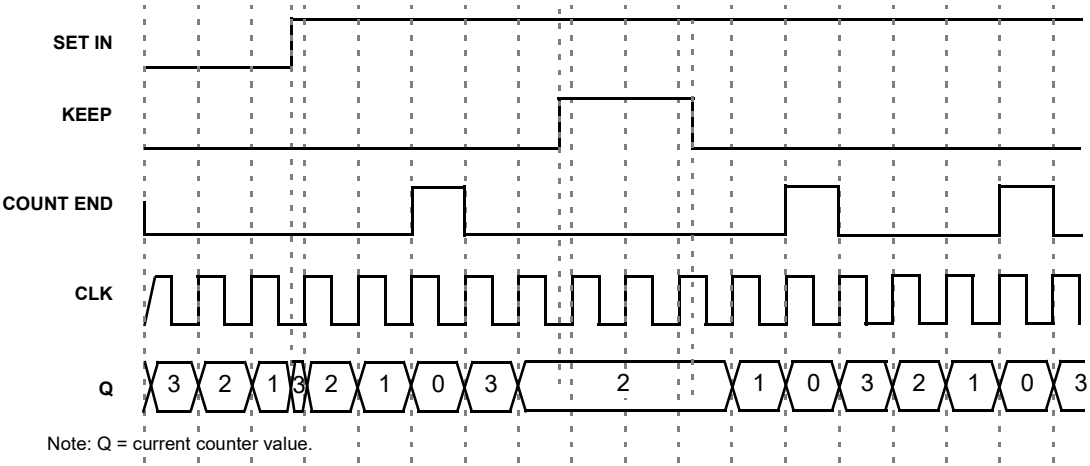


Figure 45. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

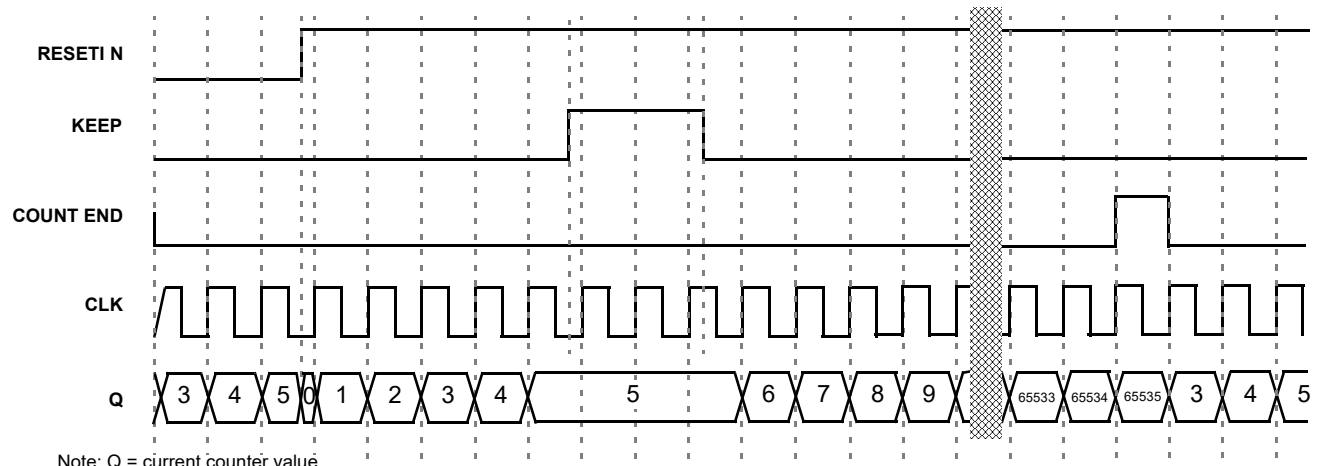


Figure 46. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

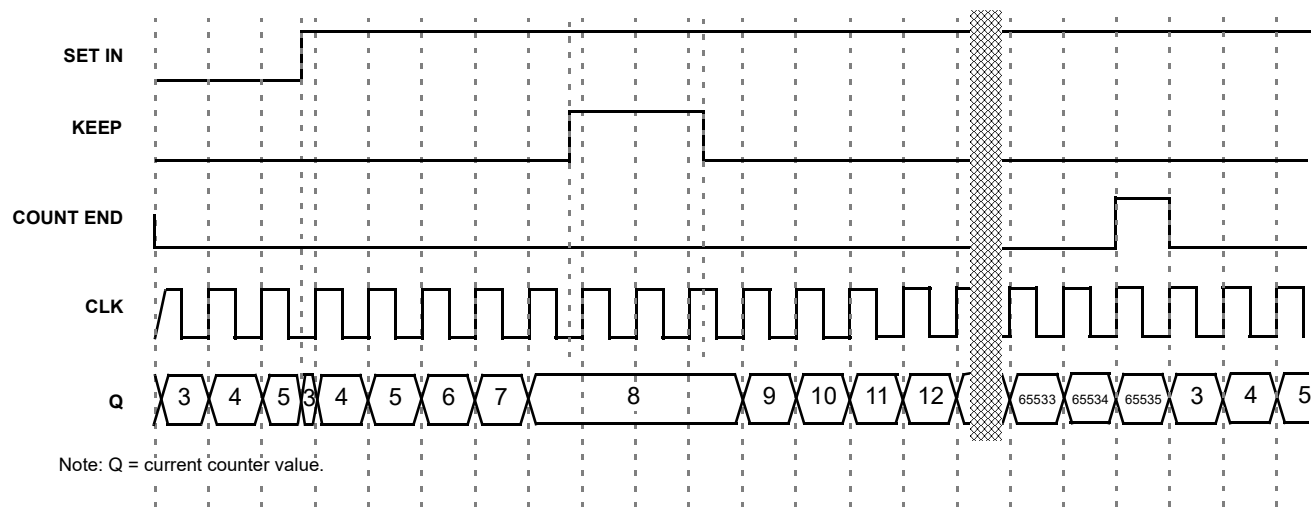


Figure 47. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

7.6.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See [Figure 48](#).

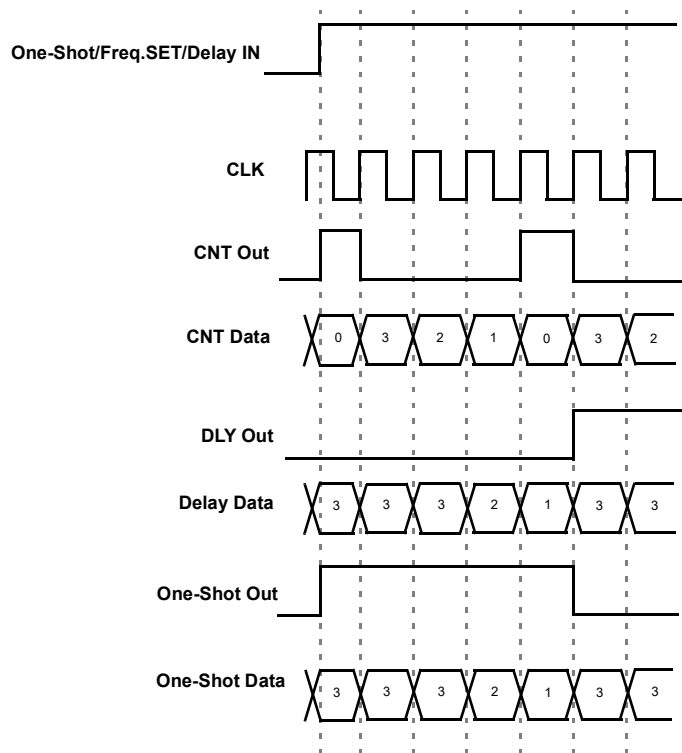


Figure 48. Counter Value, Counter Data = 3

## 7.7 2-bit LUT or Programmable Pattern Generator

The SLG46533-E has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices - AND, NAND, OR, NOR, XOR, XNOR. The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats. See [Figure 50](#).

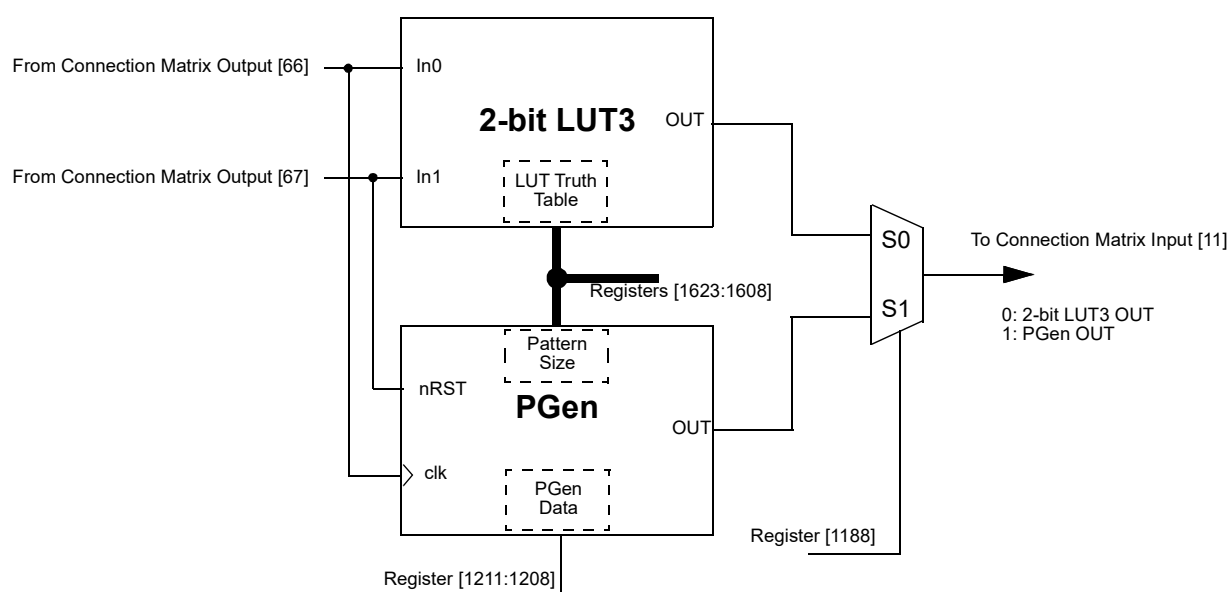


Figure 49. 2-bit LUT3 or PGen

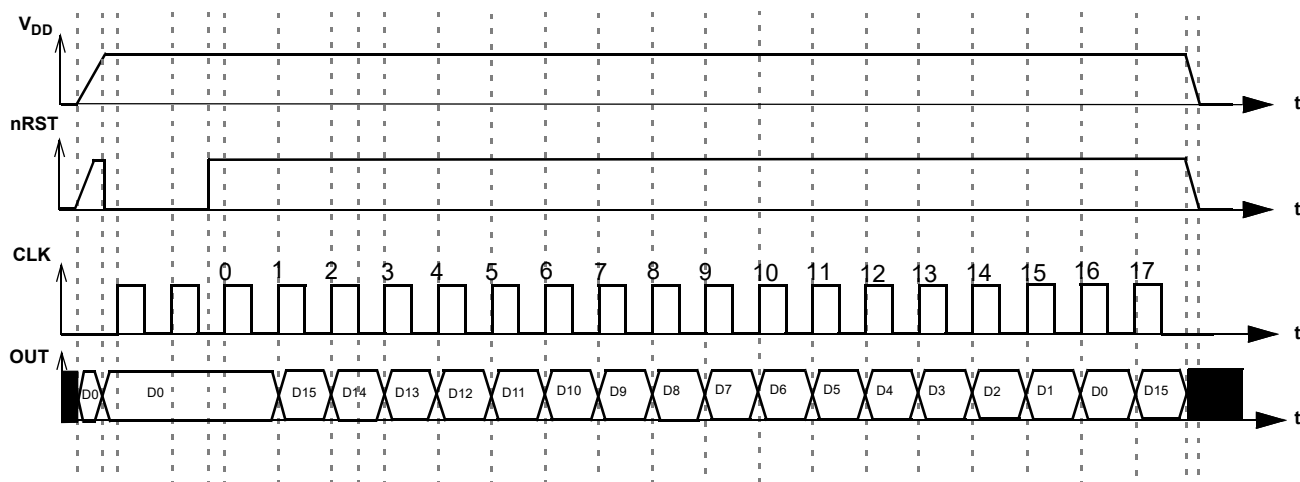


Figure 50. PGen Timing Diagram

## 7.8 Wake and Sleep Controller

The SLG46533-E has a Wake and Sleep (WS) function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1319:1318] = 11 and registers [1495] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

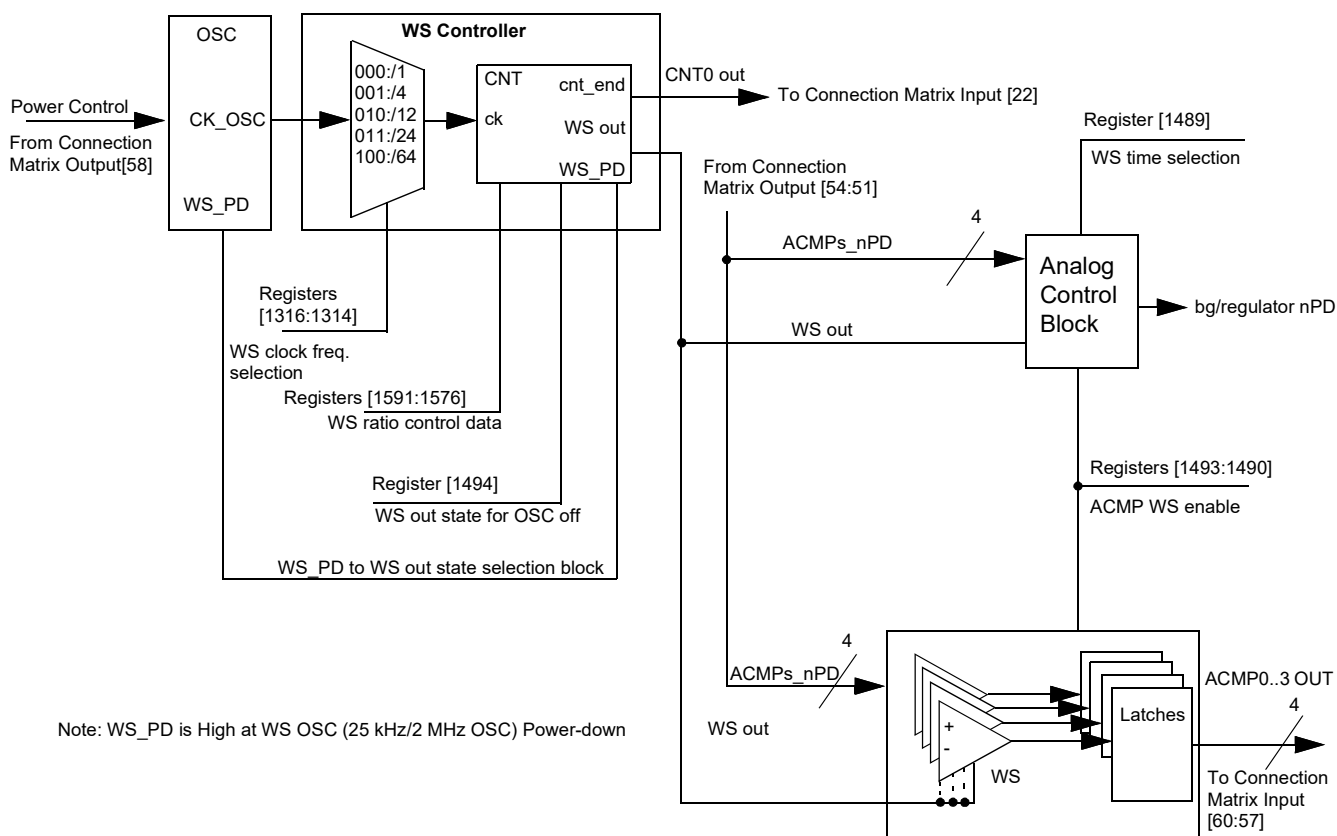


Figure 51. Wake/Sleep Controller

To use any ACMP under WS controller the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately)
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS => enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs)
- In case of using OSC1 (25 MHz), OSC0 must be set to Force Power-On.

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMPs are sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)

If OSC is powered off (Power-Down option is selected; power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.

If OSC is powered off (Power-Down option is selected; power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.

Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)

User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears

Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go Low and turn the ACMPs off until the counter counts up to the end.

Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will go on counting and High level signal will turn the ACMPs on while counter is counting up to the end.

- Edge Select defines the edge for Q mode

High level Set/Reset - switches mode Set/Reset when level is High.

**Note:** Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPs on

Normal Wake Time - when WS signal is High, it takes a BG time (100/550  $\mu$ s) to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

Short Wake Time - when WS signal is High, it takes a BG time (100/550  $\mu$ s) to turn the ACMPs on. They will stay on for 1  $\mu$ s and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1

- Up - reverses counting

If Up = 1, CNT is counting up from user selected value to 65535.

If Up = 0, CNT is counting down from user selected value to 1.

## 8. Analog Comparators

There are four Analog Comparator (ACMP) macrocells in the SLG46533-E. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx\_nPD) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. Also, all ACMPs have Wake and Sleep function (WS), see section [7.8 Wake and Sleep Controller](#). When ACMP is powered down, output is low.

PWR UP = 1 – ACMP is powered up.

PWR UP = 0 – ACMP is powered down.

During ACMP power up, its output will remain low, and then becomes valid 1 ms (max) after ACMP power up signal goes high, see [Figure 56](#). The ACMP cells have an input "Low bandwidth" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the  $V_{DD}$  signal.

**Note:** Regulator and Charge Pump set to automatic ON/OFF.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 k $\Omega$  (typ) resistors. IN- voltage range: 0 - 1.2 V. Can use  $V_{REF}$  selection  $V_{DD}/4$  and  $V_{DD}/3$  to maintain this input range.

Input bias current < 1 nA (typ).

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV, 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be  $V_{REF}$  (high threshold) and  $V_{REF}$  - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within threshold window (between  $V_{REF}$  and  $V_{REF}$  - hysteresis). Please note: for the 25 mV hysteresis option threshold levels will be  $V_{REF} + \text{hysteresis}/2$  (high threshold) and  $V_{REF} - \text{hysteresis}/2$  (low threshold).

**Note:** Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on  $V_{REF}$  even when the Force BandGap option is set as Disabled.

For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer. However, this will add some offset, see [Figure 57](#) and [Figure 58](#). It is not recommended to use ACMP buffer when  $V_{DD} < 2.5$  V.

## 8.1 ACMP0 Block Diagram

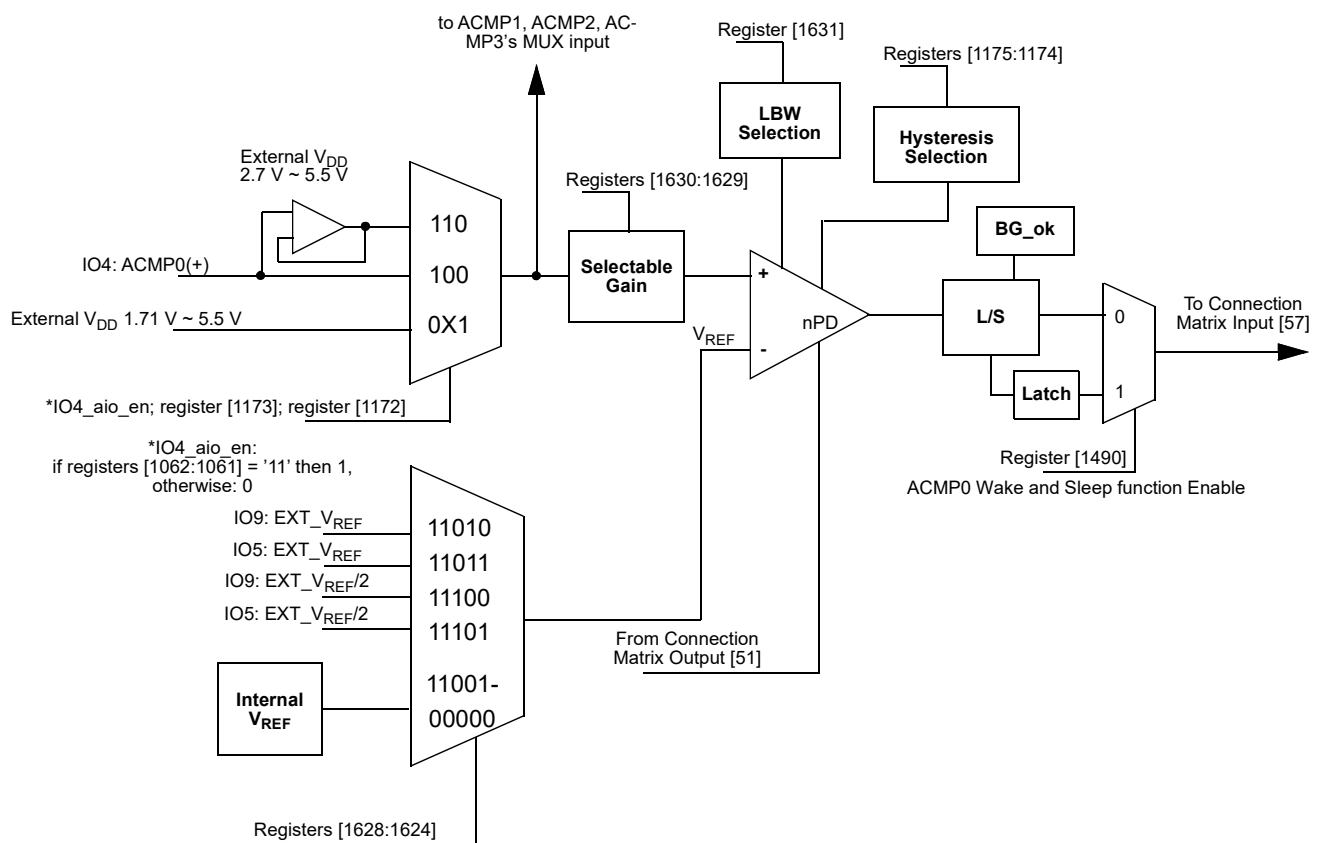


Figure 52. ACMP0 Block Diagram

## 8.2 ACMP1 Block Diagram

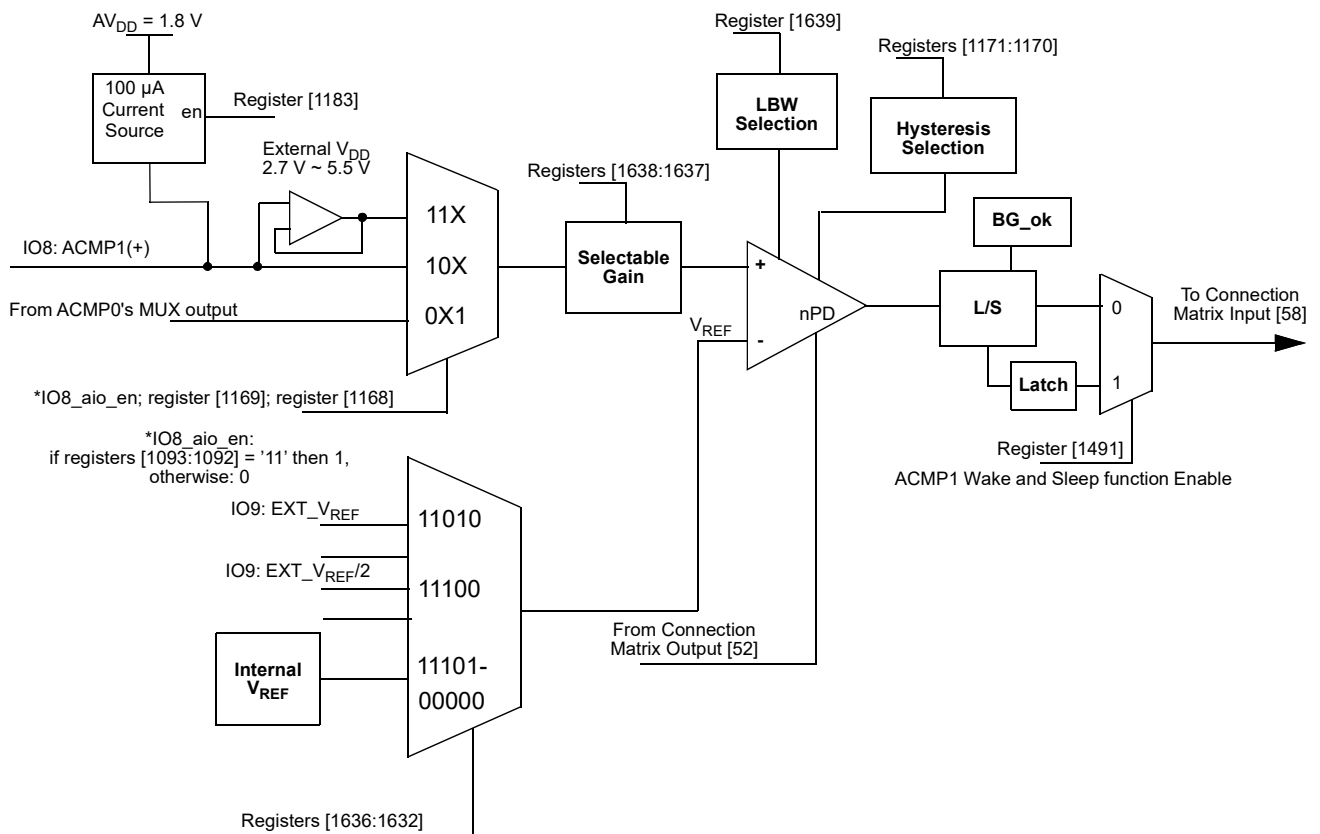


Figure 53. ACMP1 Block Diagram

### 8.3 ACMP2 Block Diagram

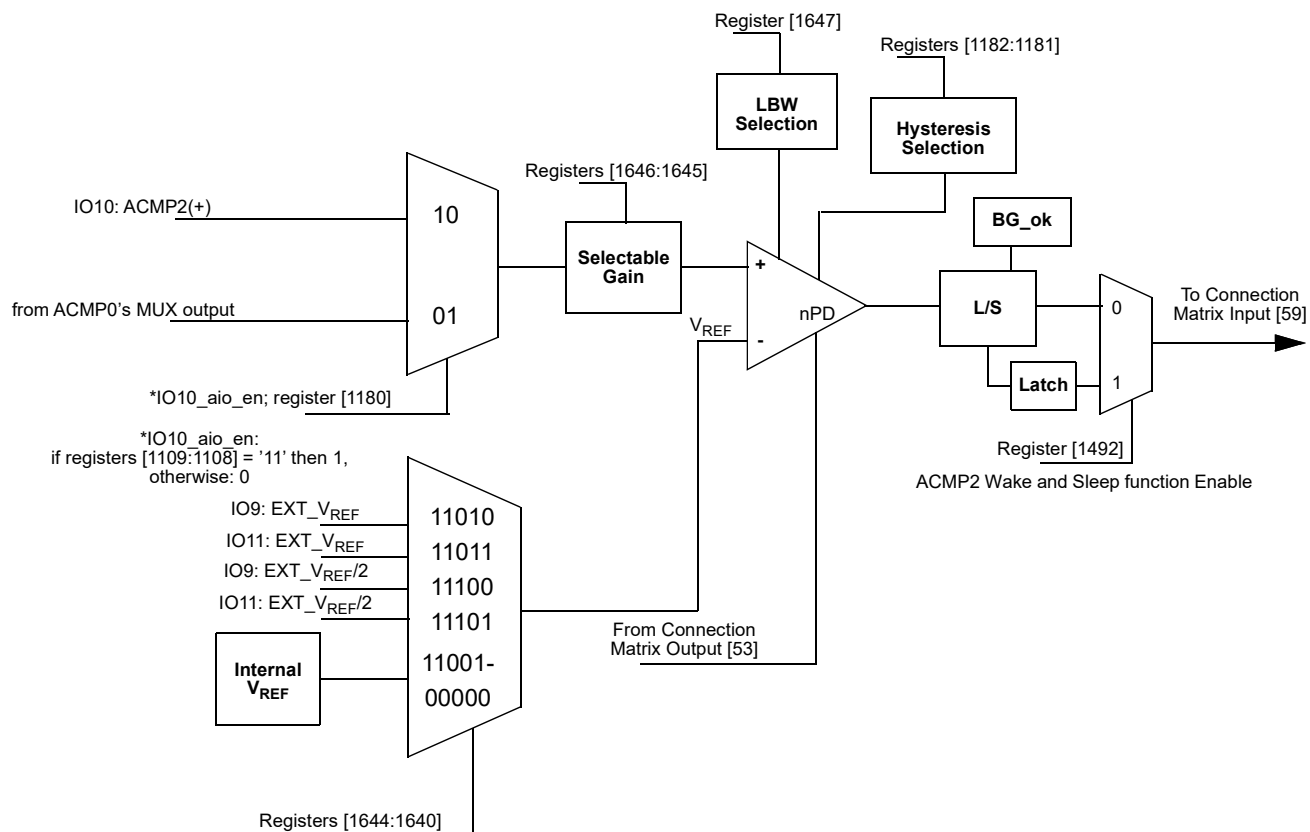


Figure 54. ACMP2 Block Diagram

## 8.4 ACMP3 Block Diagram

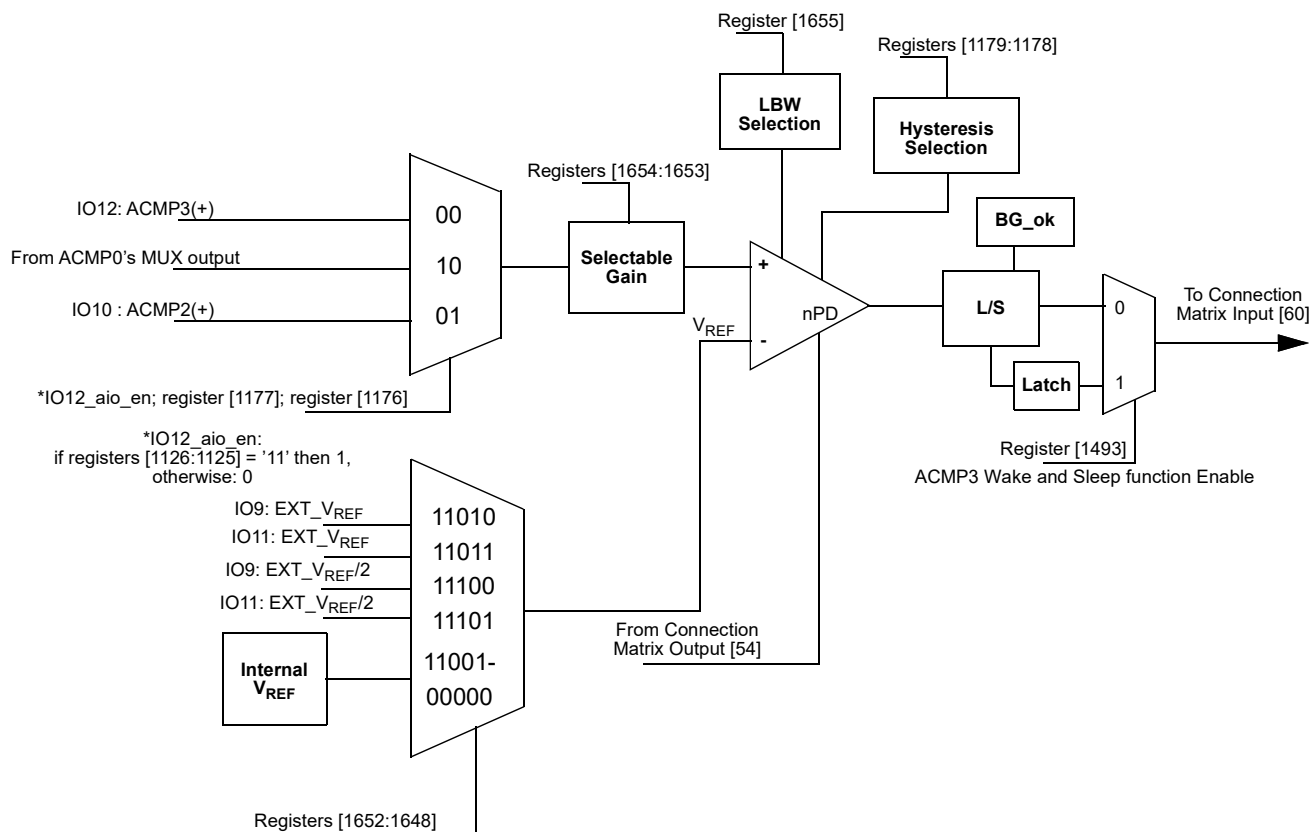
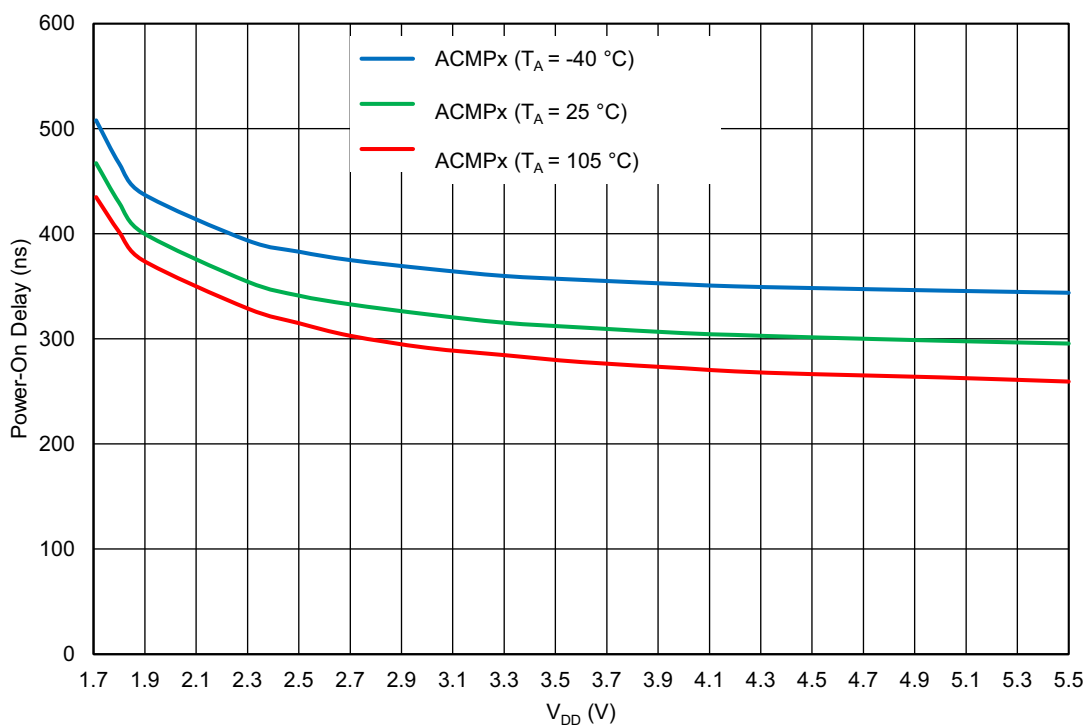


Figure 55. ACMP3 Block Diagram

## 8.5 ACMP Typical Performance

Figure 56. ACMPx Power-On Delay vs. V<sub>DD</sub>, BG Delay – Any

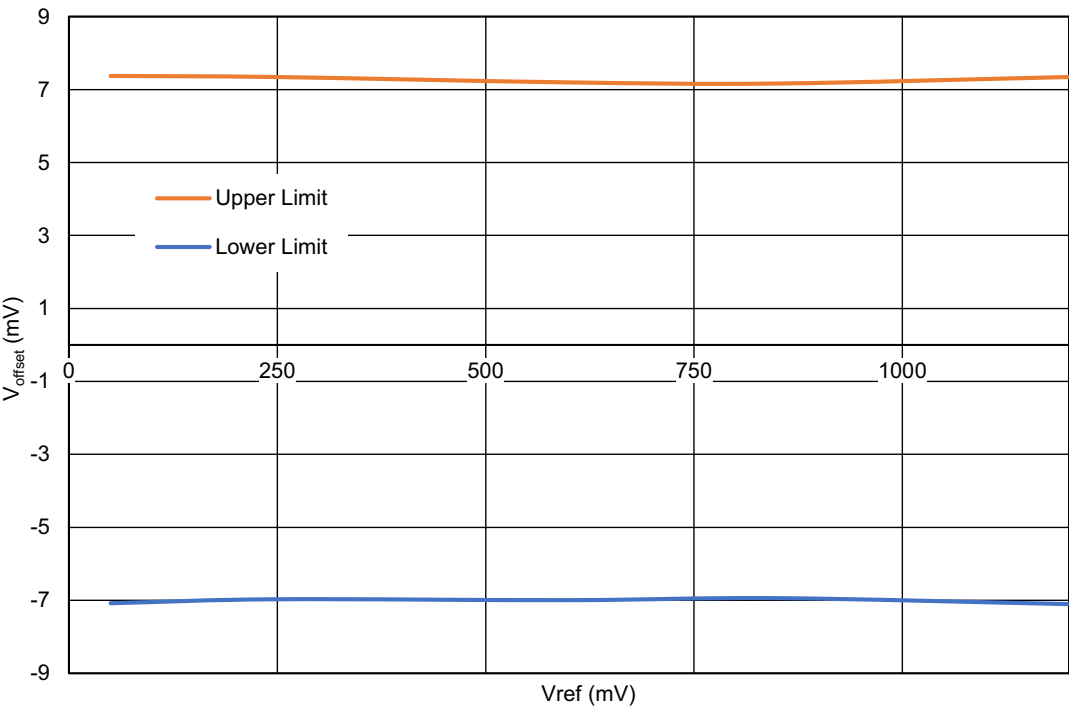


Figure 57. ACMPx Input Offset Voltage vs.  $V_{REF}$  at  $V_{DD} = 1.71\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$

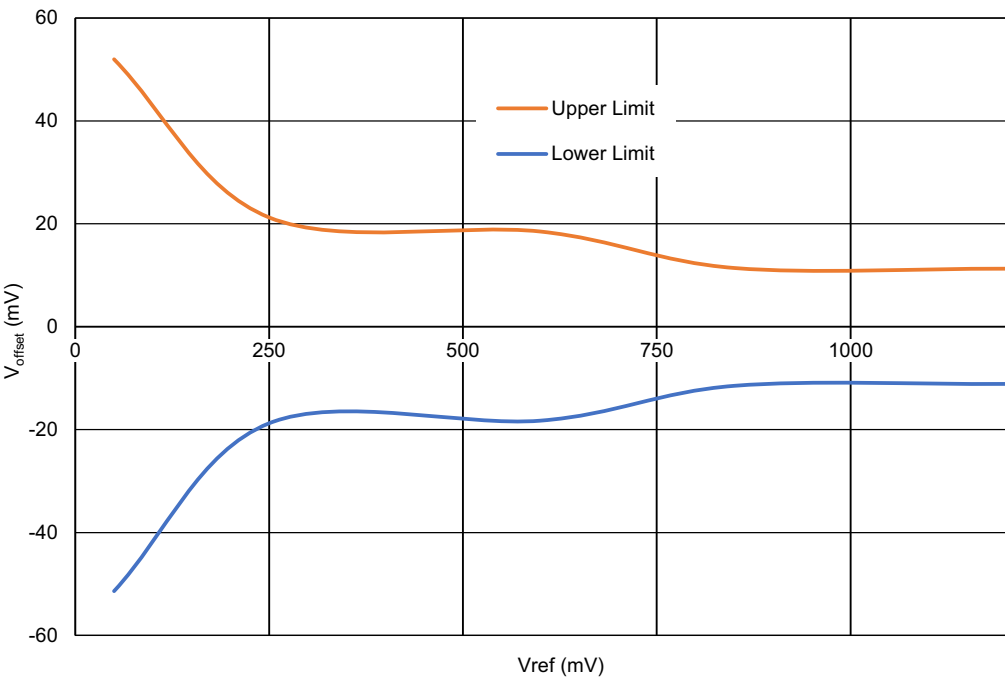


Figure 58. ACMPx Buffer Input Offset Voltage vs.  $V_{REF}$  at  $V_{DD} = 1.71\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$

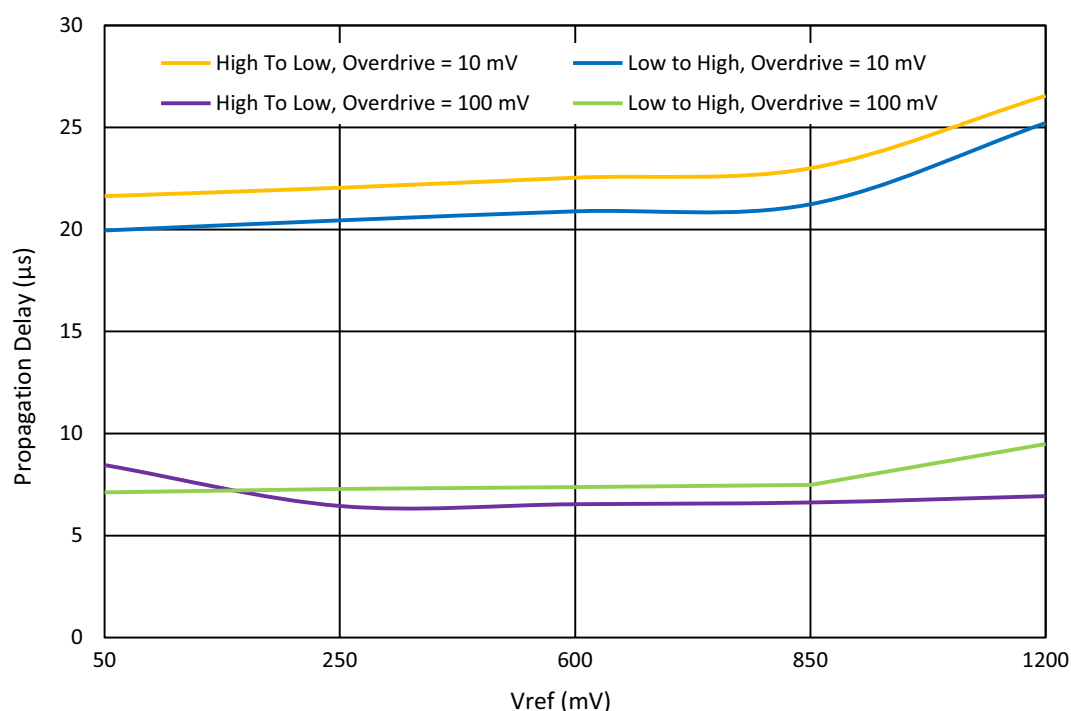


Figure 59. ACMPx Typical Propagation Delay at  $T_A = +25\text{ }^{\circ}\text{C}$ , Gain = 1, Hysteresis = 0,  $V_{DD} = 1.71\text{ V to }5.5\text{ V}$ , LPF-Enable

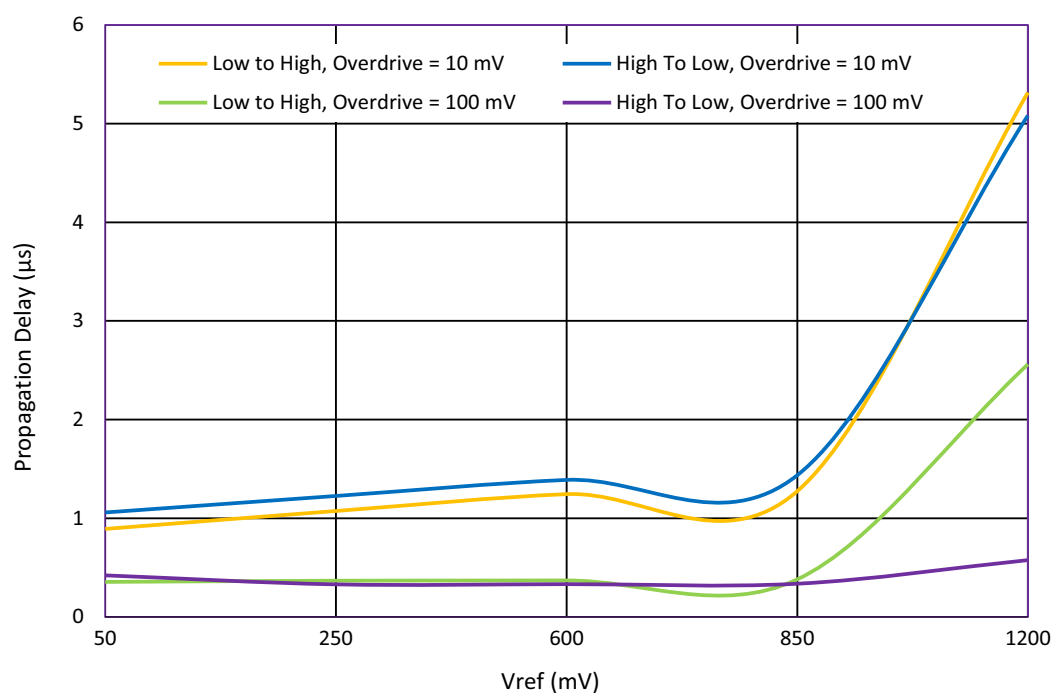


Figure 60. ACMPx Typical Propagation Delay at  $T_A = +25\text{ }^{\circ}\text{C}$ , Gain = 1, Hysteresis = 0,  $V_{DD} = 1.71\text{ V to }5.5\text{ V}$ , LPF-Disable

**Note:** When  $V_{DD} < 1.8\text{ V}$  voltage reference should not exceed 1100 mV.

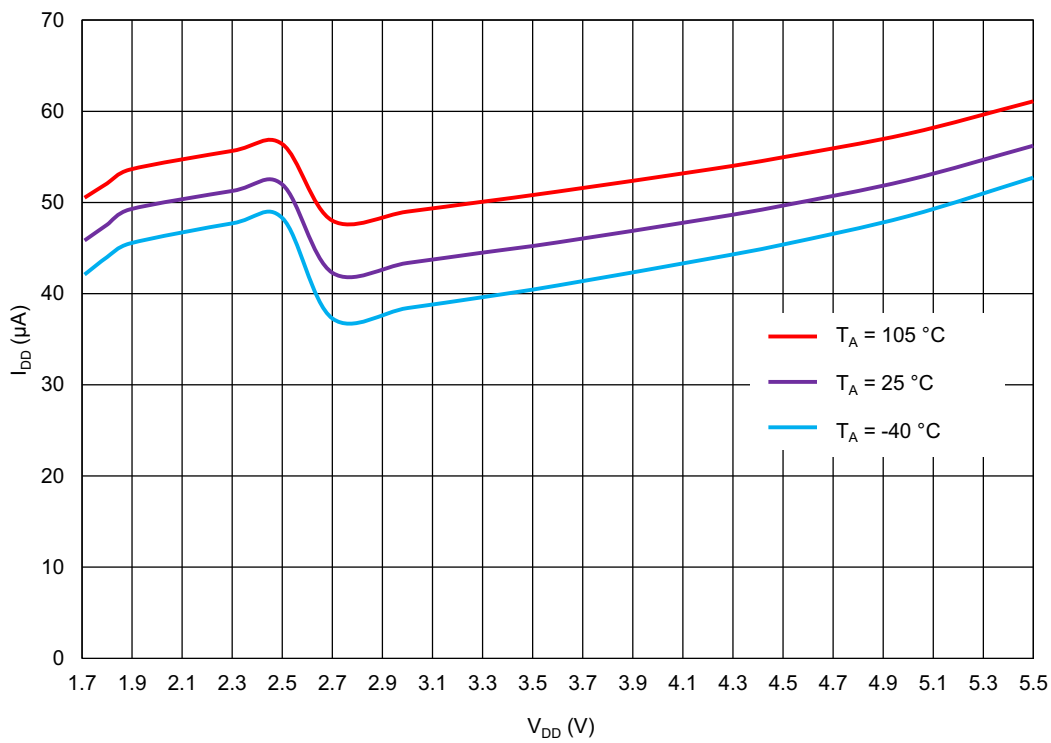


Figure 61. ACMPx Current Consumption vs.  $V_{DD}$  at  $V_{IN+}$  Connected to  $V_{DD}$ , Internal  $V_{REF} = 50$  mV

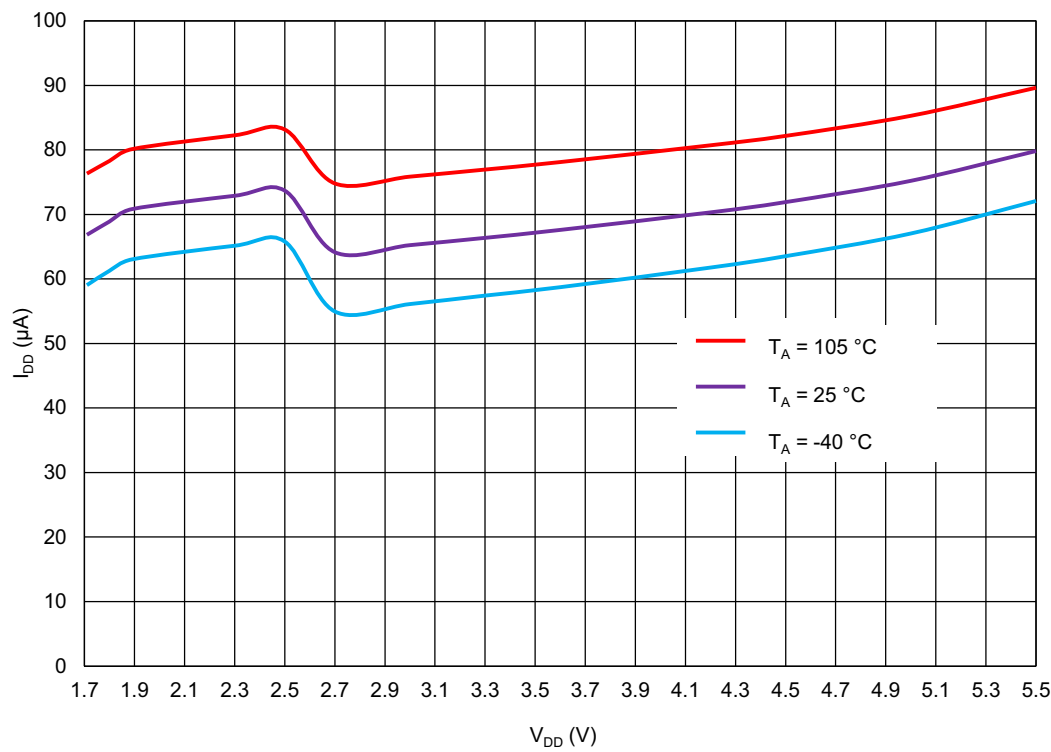


Figure 62. Buffered ACMPx Current Consumption vs.  $V_{DD}$  at  $V_{IN+}$  Connected to  $V_{DD}$ , Internal  $V_{REF} = 50$  mV

## 9. Pipe Delay

The SLG46533-E has a pipe delay logic cell that is shared with the 3-bit LUT10 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see section [7.3 3-Bit LUT or Pipe Delay Macrocell](#) for the description of this Combination Function macrocell.

## 10. Programmable Delay/Edge Detector

The SLG46533-E has a programmable time delay logic cell available, that can generate a delay, that is selectable from one of four timings configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. See [Figure 63](#) and [Figure 64](#) for further information.

**Note:** The input signal must be longer than the delay, otherwise it will be filtered out.

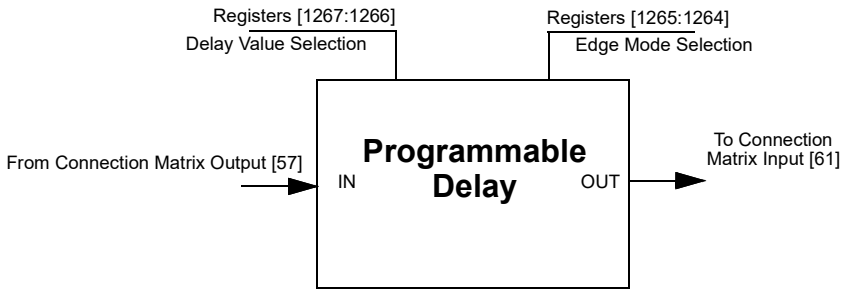


Figure 63. Programmable Delay

### 10.1 Programmable Delay Timing Diagram - Edge Detector Output

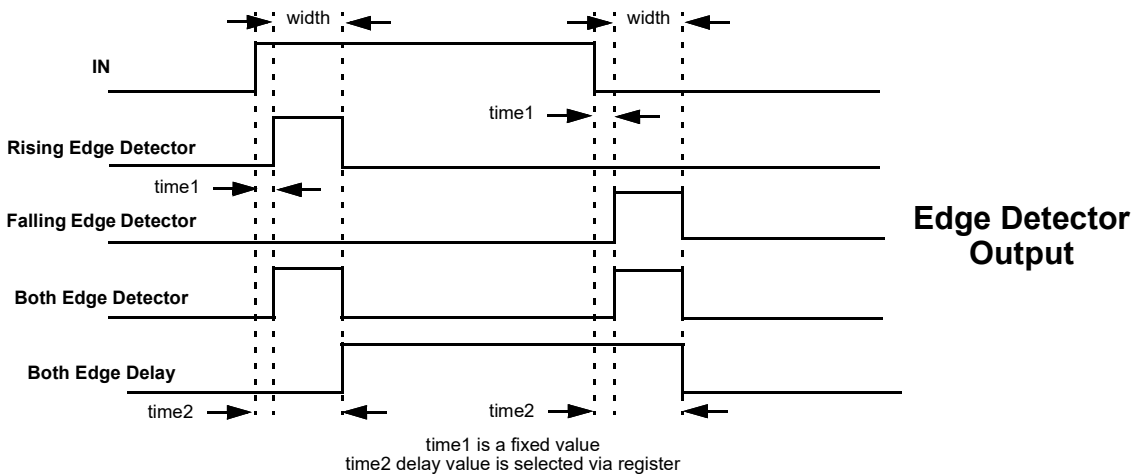


Figure 64. Edge Detector Output

Please refer to section [3.4.4 Estimated Typical Delay of Each Macrocell](#).

## 11. Additional Logic Function. Deglitch Filter

The SLG46533-E has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions. See section [3.4.4 Estimated Typical Delay of Each Macrocell](#).

### 11.1 Deglitch Filter/Edge Detector

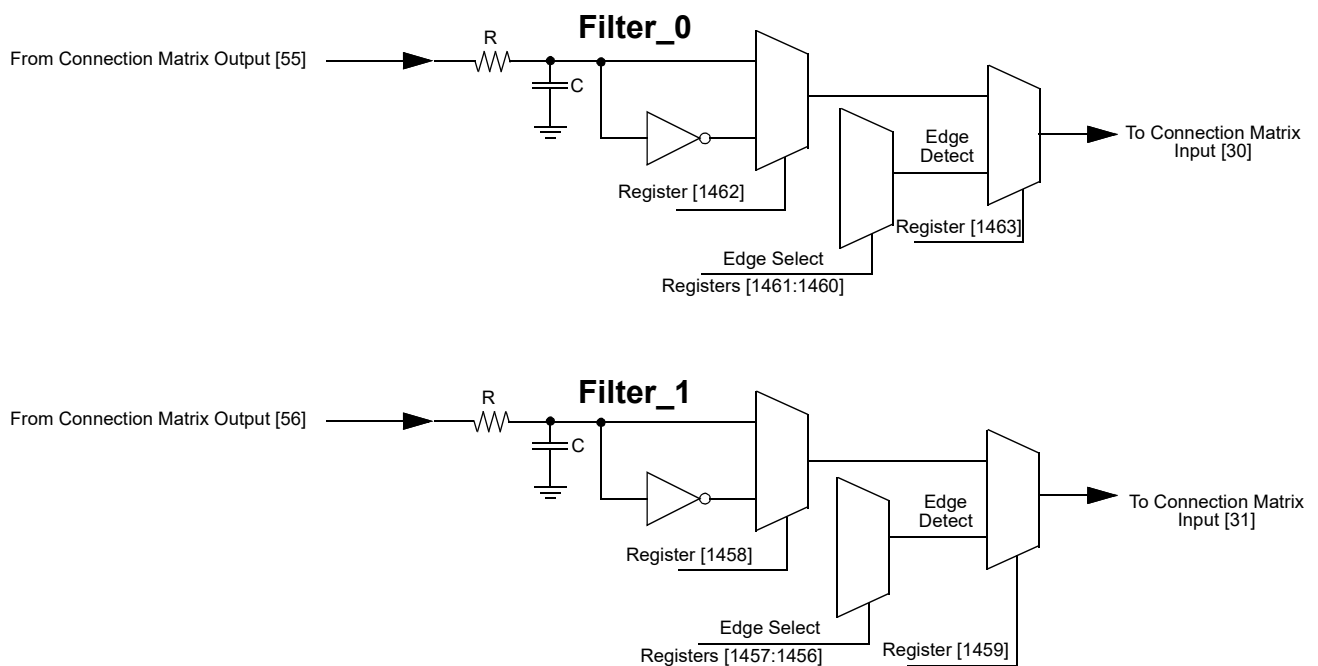


Figure 65. Deglitch Filter/Edge Detector

## 12. Voltage Reference

### 12.1 Voltage Reference Overview

The SLG46533-E has a Voltage Reference ( $V_{REF}$ ) Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references,  $/3$  and  $/4$  reference off of the  $V_{DD}$  power supply to the device, and externally supplied voltage references from IOs 5, 9, and 11. The macrocell also has an option to output reference voltages on IOs 15 and 16. See [Table 34](#) for the available selections for each analog comparator. Also, see [Figure 66](#), which shows the reference output structure.

### 12.2 $V_{REF}$ Selection Table

Table 34.  $V_{REF}$  Selection Table

| SEL[4:0] | ACMP0_ $V_{REF}$      | ACMP1_ $V_{REF}$      | ACMP2_ $V_{REF}$       | ACMP3_ $V_{REF}$       |
|----------|-----------------------|-----------------------|------------------------|------------------------|
| 11101    | IO5: EXT_ $V_{REF}/2$ | Reserved              | IO11: EXT_ $V_{REF}/2$ | IO11: EXT_ $V_{REF}/2$ |
| 11100    | IO9: EXT_ $V_{REF}/2$ | IO9: EXT_ $V_{REF}/2$ | IO9: EXT_ $V_{REF}/2$  | IO9: EXT_ $V_{REF}/2$  |
| 11011    | IO5: EXT_ $V_{REF}$   | Reserved              | IO11: EXT_ $V_{REF}$   | IO11: EXT_ $V_{REF}$   |
| 11010    | IO9: EXT_ $V_{REF}$   | IO9: EXT_ $V_{REF}$   | IO9: EXT_ $V_{REF}$    | IO9: EXT_ $V_{REF}$    |
| 11001    | $V_{DD}/4$            | $V_{DD}/4$            | $V_{DD}/4$             | $V_{DD}/4$             |
| 11000    | $V_{DD}/3$            | $V_{DD}/3$            | $V_{DD}/3$             | $V_{DD}/3$             |
| 10111    | 1.20                  | 1.20                  | 1.20                   | 1.20                   |
| 10110    | 1.15                  | 1.15                  | 1.15                   | 1.15                   |
| 10101    | 1.10                  | 1.10                  | 1.10                   | 1.10                   |
| 10100    | 1.05                  | 1.05                  | 1.05                   | 1.05                   |
| 10011    | 1.00                  | 1.00                  | 1.00                   | 1.00                   |
| 10010    | 0.95                  | 0.95                  | 0.95                   | 0.95                   |
| 10001    | 0.90                  | 0.90                  | 0.90                   | 0.90                   |
| 10000    | 0.85                  | 0.85                  | 0.85                   | 0.85                   |
| 01111    | 0.80                  | 0.80                  | 0.80                   | 0.80                   |
| 01110    | 0.75                  | 0.75                  | 0.75                   | 0.75                   |
| 01101    | 0.70                  | 0.70                  | 0.70                   | 0.70                   |
| 01100    | 0.65                  | 0.65                  | 0.65                   | 0.65                   |
| 01011    | 0.60                  | 0.60                  | 0.60                   | 0.60                   |
| 01010    | 0.55                  | 0.55                  | 0.55                   | 0.55                   |
| 01001    | 0.50                  | 0.50                  | 0.50                   | 0.50                   |
| 01000    | 0.45                  | 0.45                  | 0.45                   | 0.45                   |
| 00111    | 0.40                  | 0.40                  | 0.40                   | 0.40                   |
| 00110    | 0.35                  | 0.35                  | 0.35                   | 0.35                   |
| 00101    | 0.30                  | 0.30                  | 0.30                   | 0.30                   |
| 00100    | 0.25                  | 0.25                  | 0.25                   | 0.25                   |
| 00011    | 0.20                  | 0.20                  | 0.20                   | 0.20                   |

Table 34.  $V_{REF}$  Selection Table (Cont.)

| SEL[4:0] | ACMP0_ $V_{REF}$ | ACMP1_ $V_{REF}$ | ACMP2_ $V_{REF}$ | ACMP3_ $V_{REF}$ |
|----------|------------------|------------------|------------------|------------------|
| 00010    | 0.15             | 0.15             | 0.15             | 0.15             |
| 00001    | 0.10             | 0.10             | 0.10             | 0.10             |
| 00000    | 0.05             | 0.05             | 0.05             | 0.05             |

Table 35. Practical  $V_{REF}$  Range of Voltage Reference Macrocell

| $V_{DD}$      | Practical $V_{REF}$ Range | Note                       |
|---------------|---------------------------|----------------------------|
| 2.0 V - 5.5 V | 50 mV ~ 1.2 V             |                            |
| 1.7 V - 2.0 V | 50 mV ~ 1.0 V             | Do not operate above 1.0 V |

## 12.3 $V_{REF}$ Block Diagram

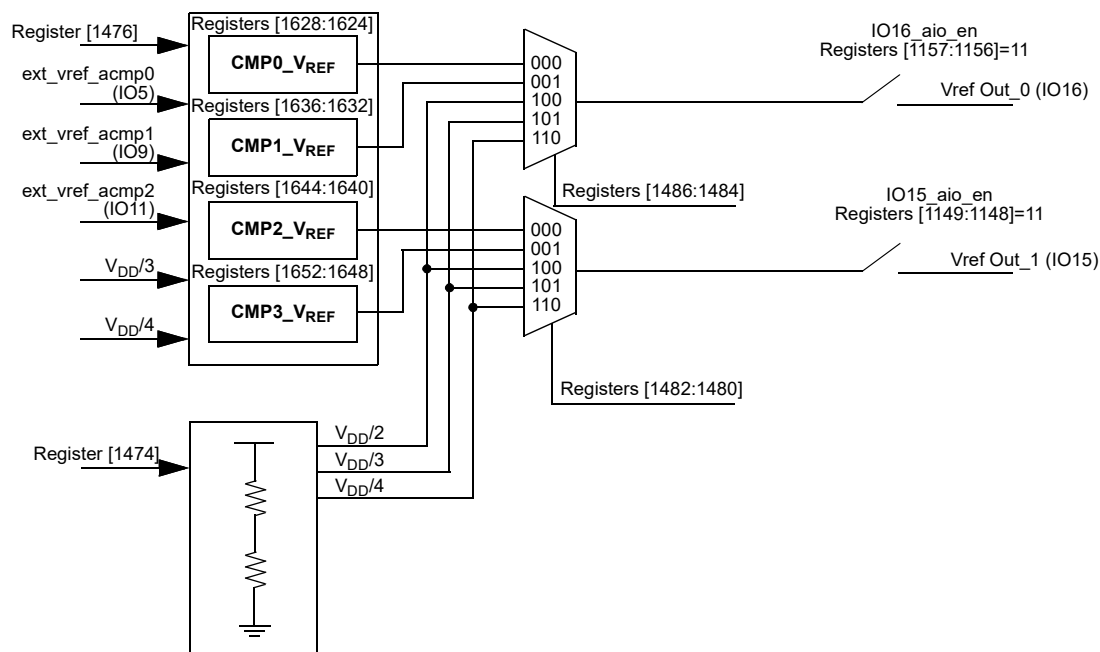


Figure 66. Voltage Reference Block Diagram

### 12.4 V<sub>REF</sub> Load Regulation

**Note 1:** V<sub>REF</sub> buffer performance is not guaranteed at V<sub>DD</sub> < 2.7 V.

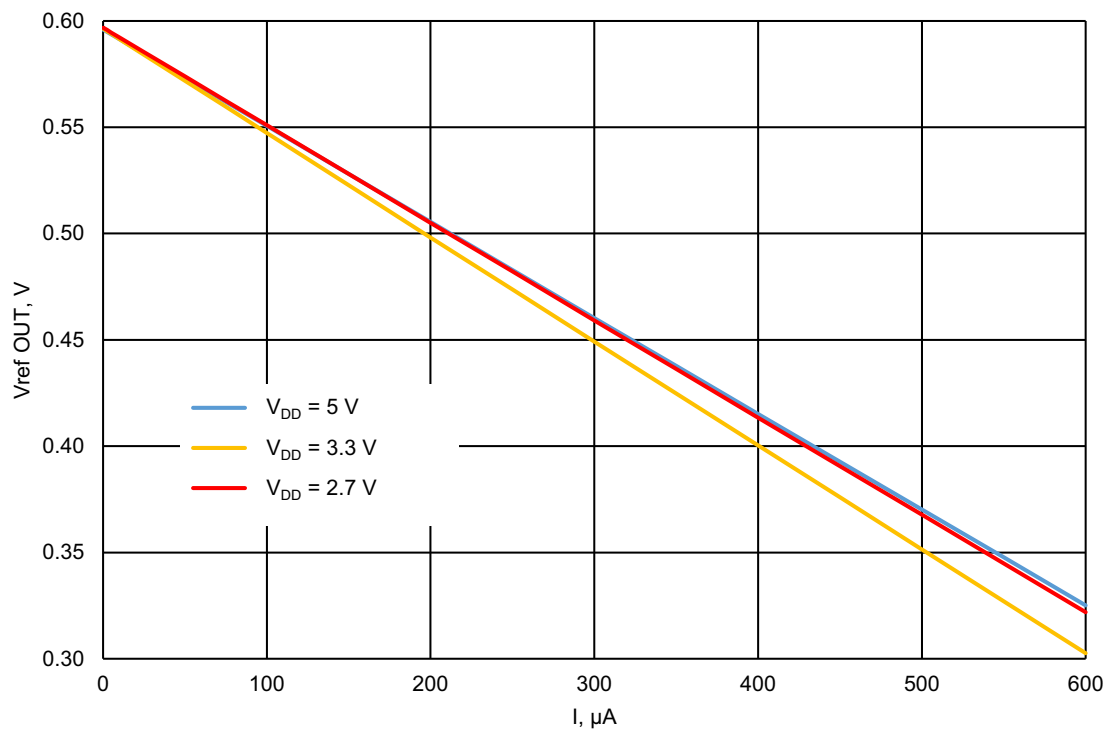


Figure 67. Typical Load Regulation, V<sub>REF</sub> = 600 mV, T<sub>A</sub> = -40 °C to +105 °C, Buffer - Enable

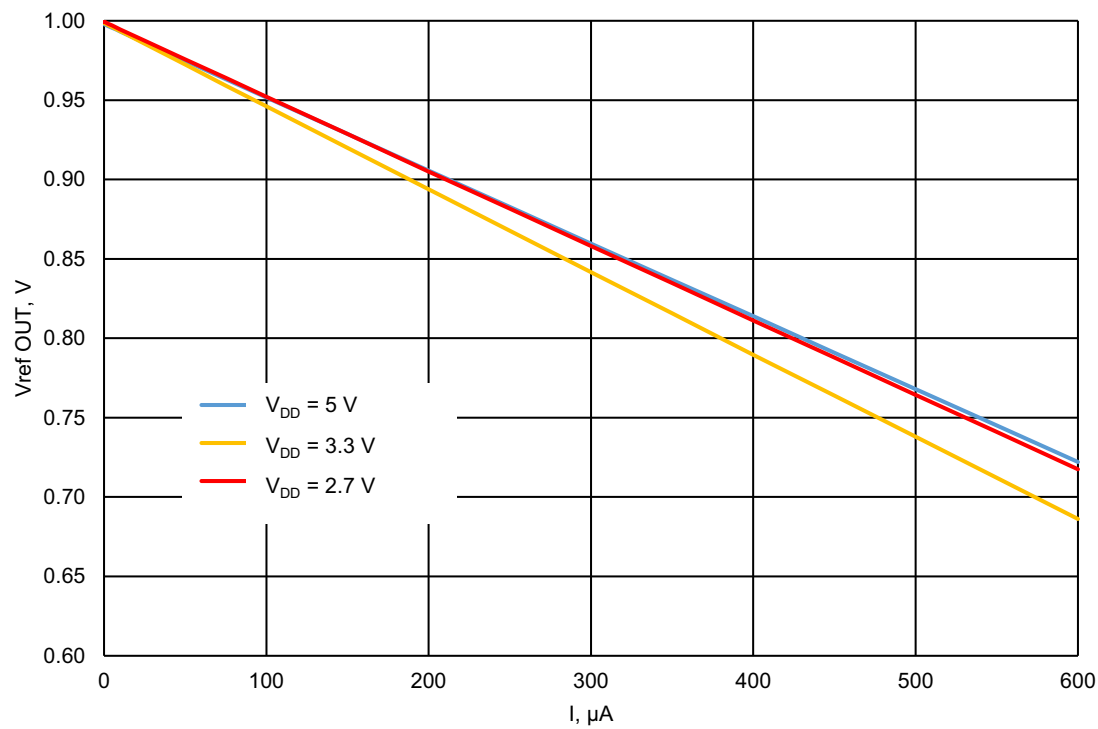


Figure 68. Typical Load Regulation, V<sub>REF</sub> = 1000 mV, T<sub>A</sub> = -40 °C to +105 °C, Buffer - Enable

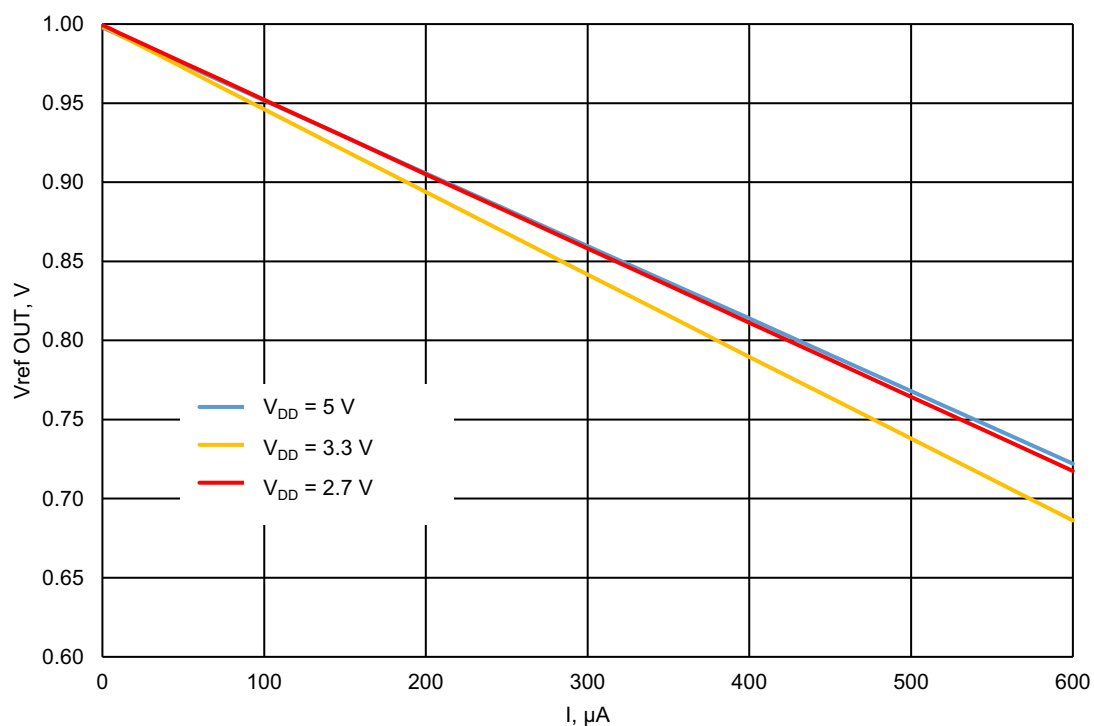


Figure 69. Typical Load Regulation,  $V_{REF} = 1200$  mV,  $T_A = -40$  °C to  $+105$  °C, Buffer - Enable

## 13. Clocking

### 13.1 OSC General Description

The SLG46533-E has two internal oscillators. Oscillator that runs at 25 kHz/2 MHz (OSC0) and Oscillator that runs at 25 MHz (OSC1). It is possible to use OSC0 and OSC1 simultaneously. The fundamental frequency can also come from clock input (IO15 or IO17 for 25 kHz/2 MHz and IO14 for 25 MHz), see section [13.3 External Clocking](#).

### 13.2 25 kHz/2 MHz and 25 MHz Oscillators

There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The pre-divider allows the selection of /1, /2, /4, or /8 divide down frequency from the fundamental. The second stage divider (only for 25 kHz/2 MHz Oscillator) has an input of frequency from the pre-divider, and outputs one of seven different frequencies on Connection Matrix Input lines [27] (OUT0) and [28] (OUT1). See [Figure 70](#) and [Figure 71](#) for details.

There are two modes of the POWER CONTROL pin, (register [1658] for 25 kHz/2 MHz OSC and register [1657] for 25 MHz OSC):

- **POWER-DOWN [0]**. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned on. If PWR CONTROL input of oscillator is HIGH the oscillator will be turned off and OSC divider will reset.
- **FORCE ON [1]**. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned on. If PWR CONTROL input of oscillator is LOW the oscillator will be turned off.

The PWR CONTROL signal has the highest priority.

The SLG46533-E has a 25 kHz/2 MHz OSC FAST START-UP function register [1338] (1 – on, 0 – off). It allows the OSC to run immediately after power-up this decreases the settling time. Note that when OSC FAST START-UP is on, the current consumption will rise.

The user can select two OSC POWER MODEs (register [1343] for 25 kHz/2 MHz OSC and register [1341] for 25 MHz OSC):

- If **AUTO POWER-ON [0]** is selected, the OSC will run when any macrocell that uses OSC is powered on.
- If **FORCE POWER-ON [1]** is selected, the OSC will run when the SLG46533-E is powered on.

OSC can be turned on by:

- Register control (force Power-On)
- Delay mode, when delay requires OSC
- CNT/FSM.

The Power-Down Mode is paired with temperature sensor, section [16. Analog Temperature Sensor](#).

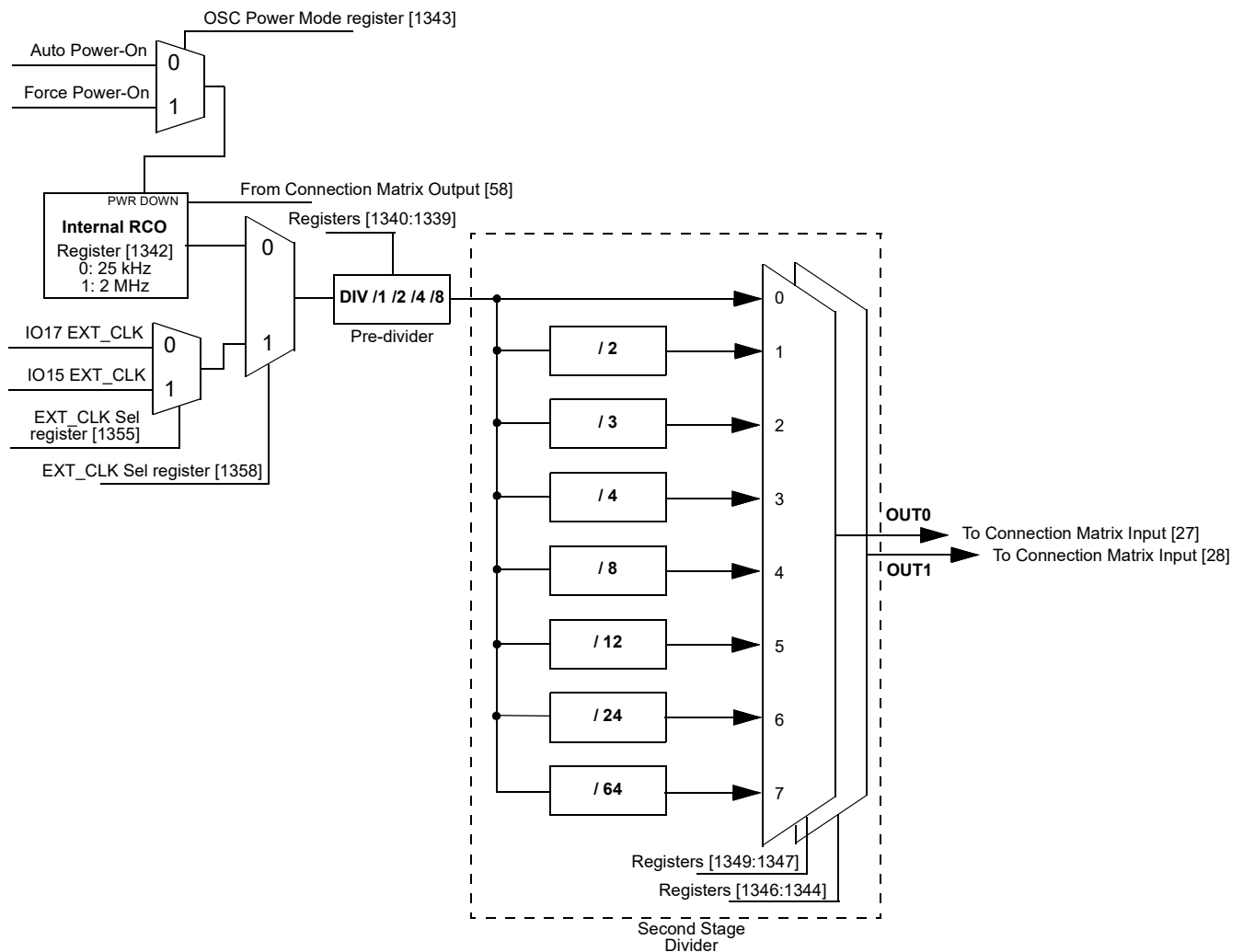


Figure 70. 25 kHz/2 MHz OSC Block Diagram

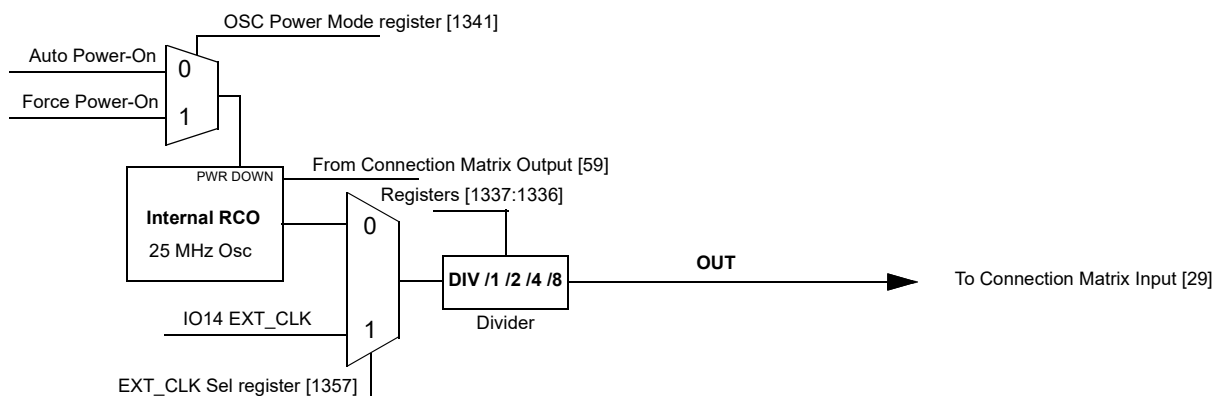


Figure 71. 25 MHz OSC Block Diagram

### 13.3 External Clocking

The SLG46533-E supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

### 13.3.1 IO17 or IO15 Source for 25 kHz/2 MHz Clock

When register [1358] is set to 1, an external clocking signal on IOs 15 or 17 will be routed in place of the internal oscillator derived 25 kHz/2 MHz clock source. When register [1355] is set to 0, IO17 is in use, when set to 1, IO15 is in use. See Figure 70. The high and low limits for external frequency that can be selected are 0 MHz and 77 MHz.

### 13.3.2 IO14 Source for 25 MHz Clock

When register [1357] is set to 1, an external clocking signal on IO14 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 71. The high and low limits for external frequency that can be selected are 0 MHz and 84 MHz.

## 13.4 Oscillators Power-On Delay

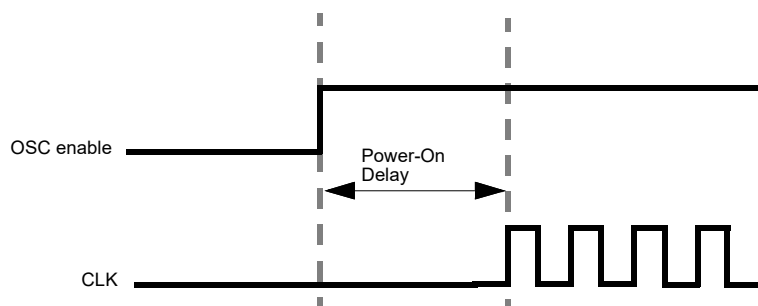


Figure 72. Oscillator Startup Diagram

**Note 1:** OSC power mode: “Auto Power-On”.

**Note 2:** “OSC enable” signal appears when any macrocell that uses OSC is powered on.

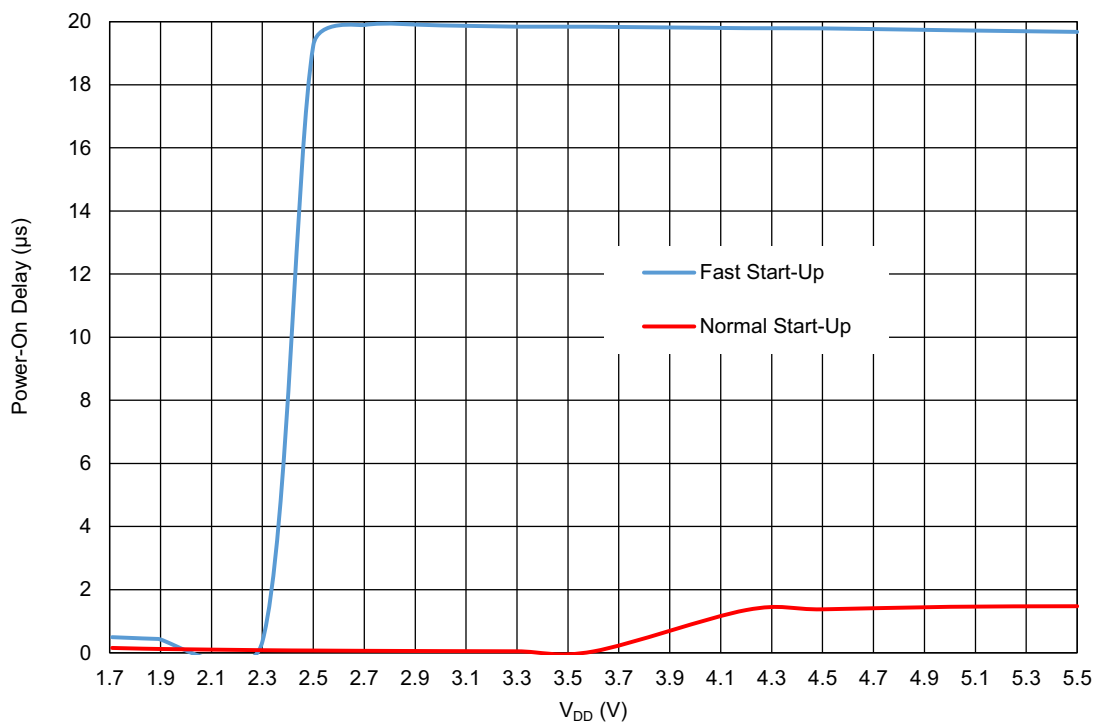


Figure 73. Oscillator Maximum Power-On Delay vs.  $V_{DD}$  at  $T_A = +25\text{ }^{\circ}\text{C}$ , OSC0 = 25 kHz

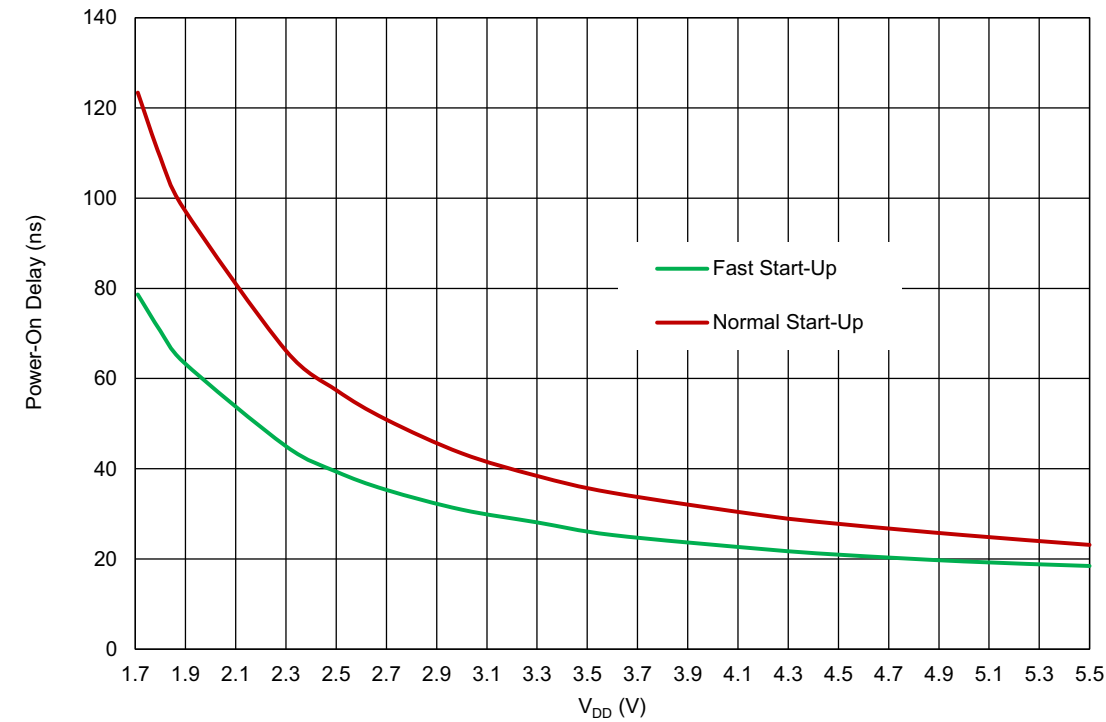


Figure 74. Oscillator Maximum Power-On Delay vs. V<sub>DD</sub> at T<sub>A</sub> = +25 °C, OSC0 = 2 MHz

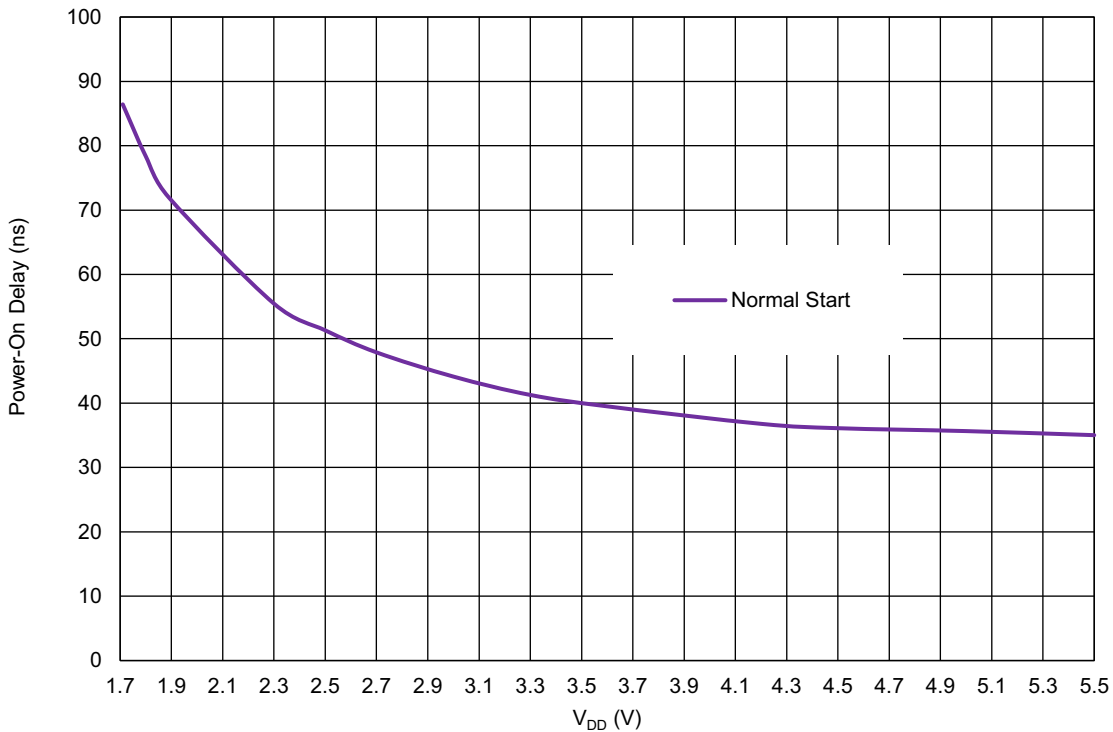


Figure 75. Oscillator Maximum Power-On Delay vs. V<sub>DD</sub> at T<sub>A</sub> = +25 °C, OSC1 = 25 MHz

## 13.5 Oscillators Accuracy

**Note 1:** OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

**Note 2:** For more information see sections [3.4.8 25 kHz OSC0 Frequency Limits](#), [3.4.10 2 MHz OSC0 Frequency Limits](#), [3.4.12 25 MHz OSC1 Frequency Limits](#).

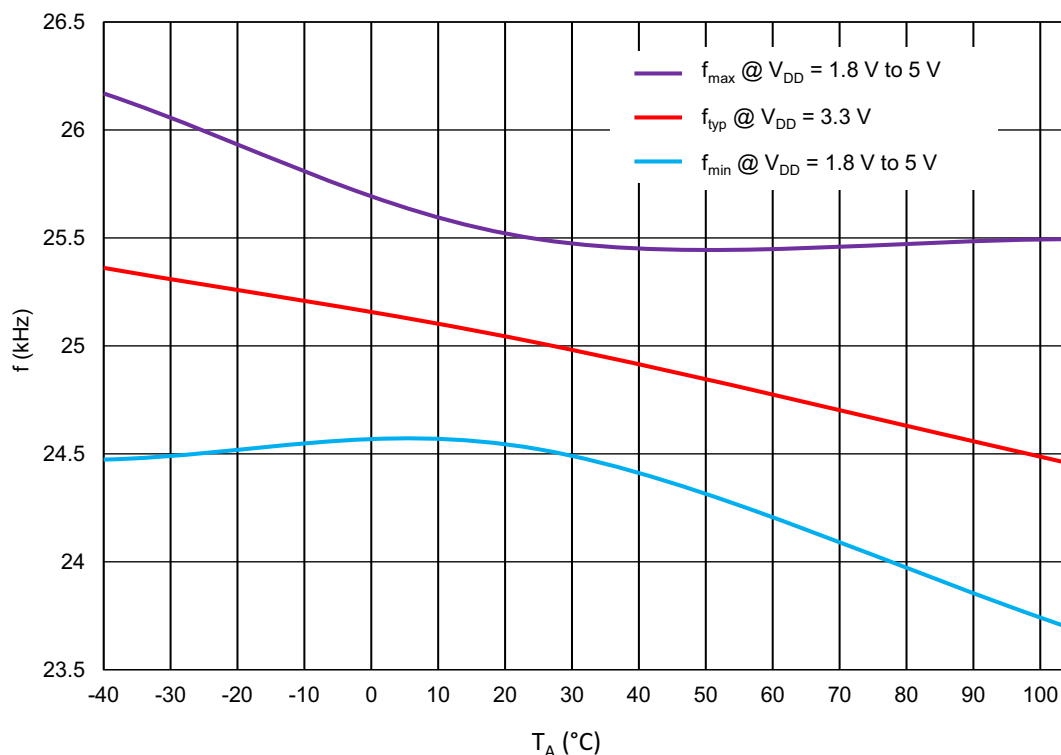


Figure 76. Oscillator Frequency vs. Ambient Temperature, OSC0 = 25 kHz

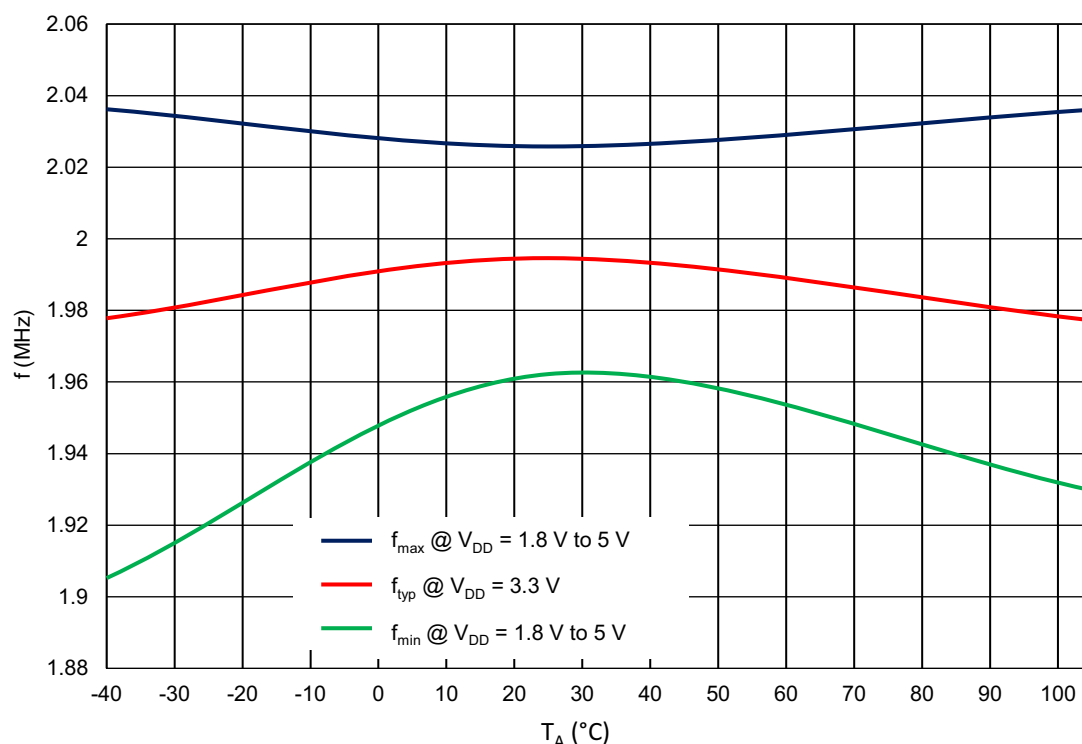


Figure 77. Oscillator Frequency vs. Ambient Temperature, OSC0 = 2 MHz

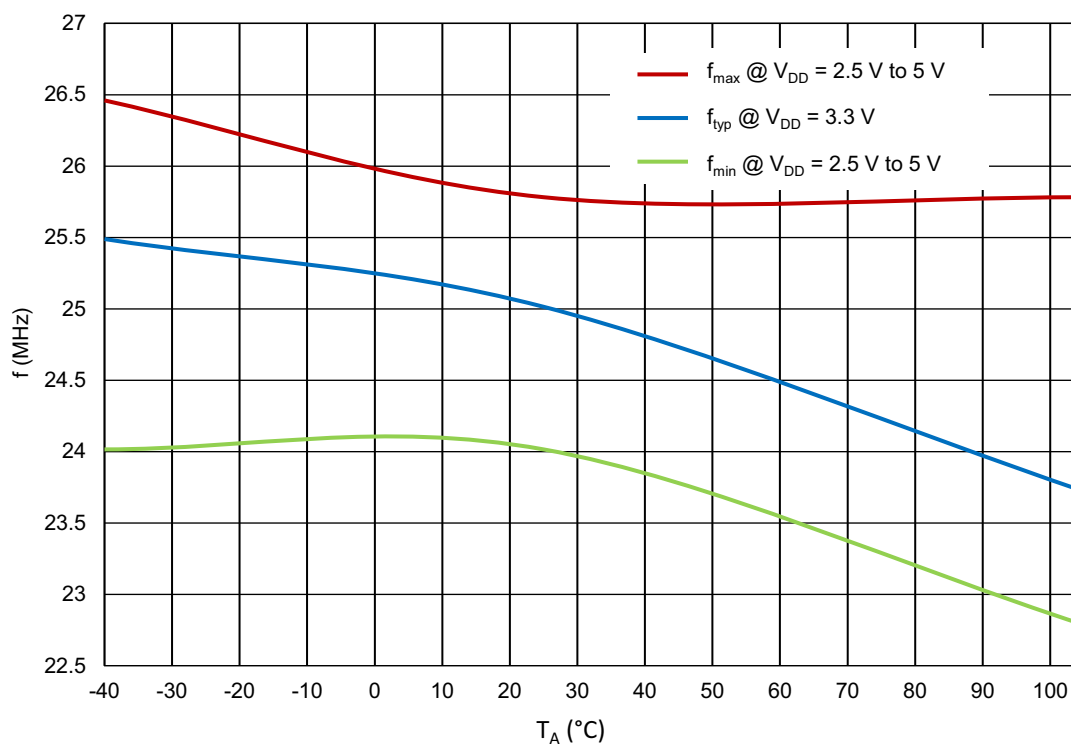


Figure 78. Oscillator Frequency vs. Ambient Temperature, OSC1 = 25 MHz

**Note:** 25 MHz OSC1 performance is not guaranteed at  $V_{DD} < 2.5 \text{ V}$ .

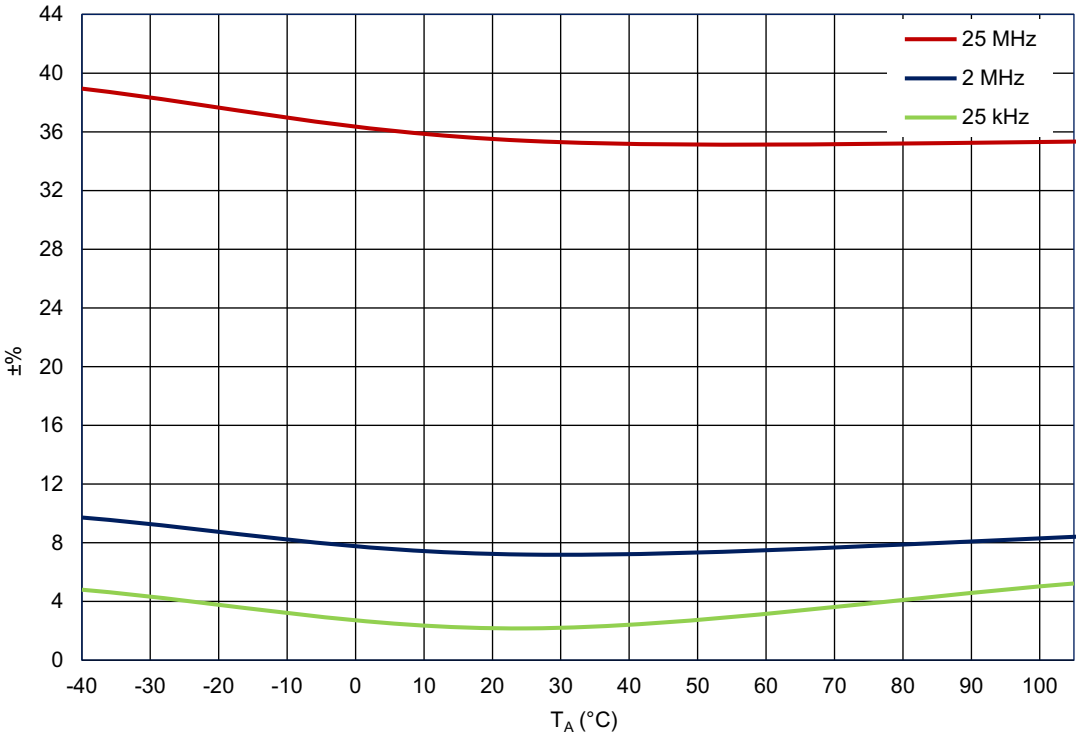


Figure 79. Oscillators Total Error vs. Ambient Temperature

13.6 Oscillators Settling Time

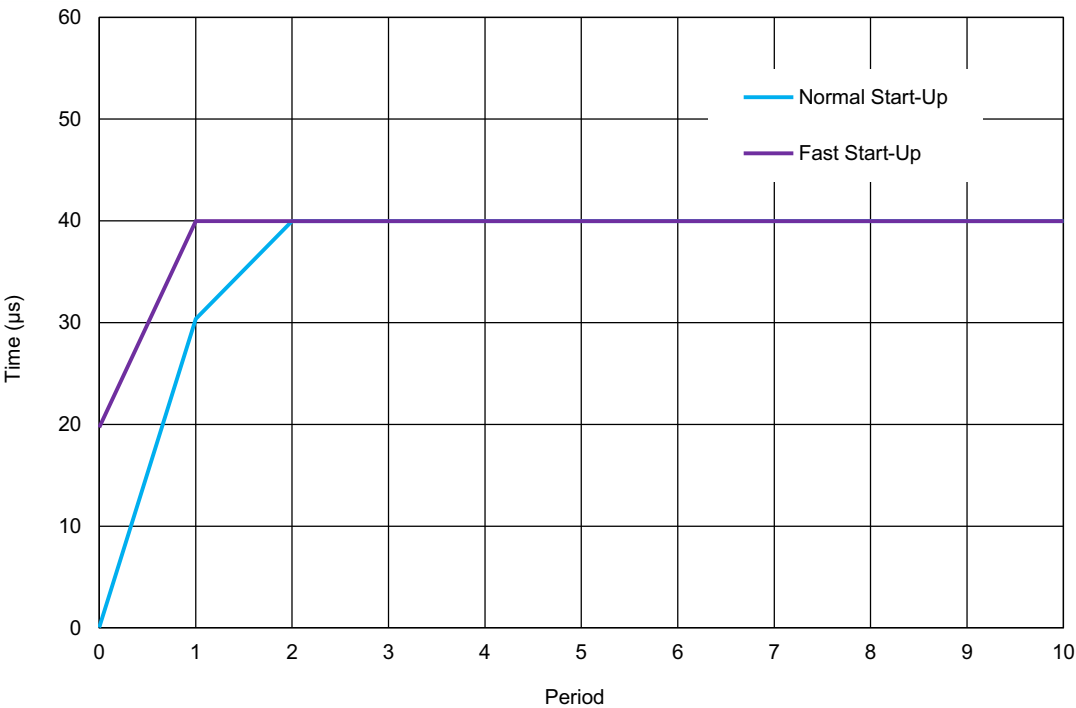


Figure 80. Oscillator0 Settling Time,  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $\text{OSC0} = 2\text{ kHz}$

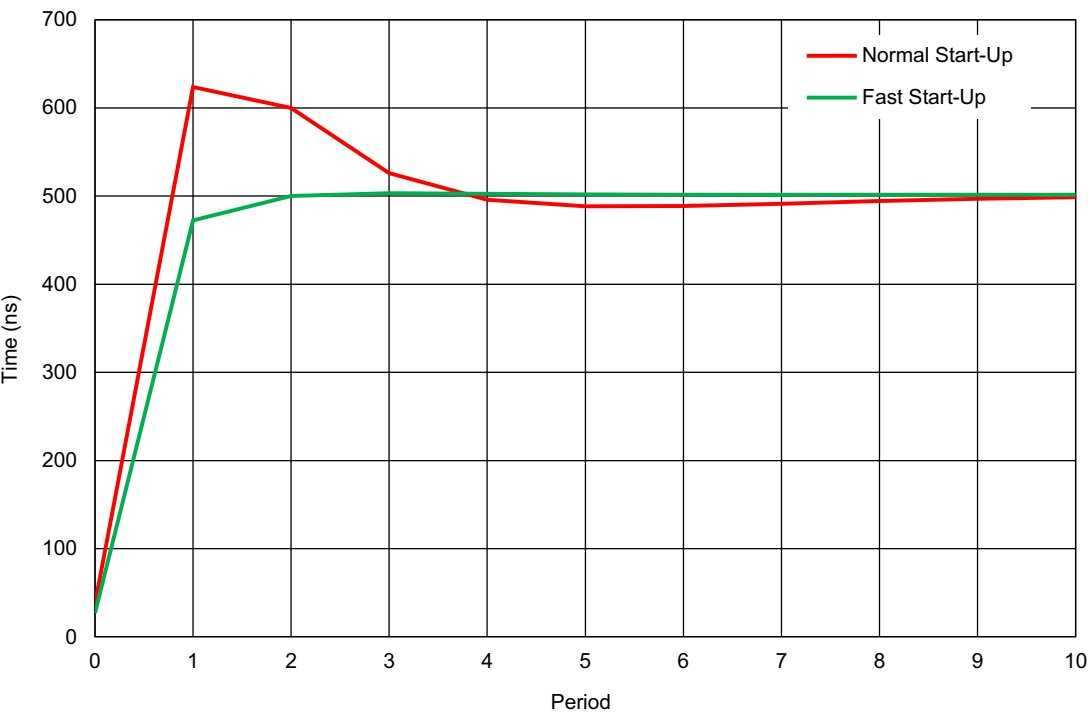


Figure 81. Oscillator0 Settling Time,  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $\text{OSC0} = 2\text{ MHz}$

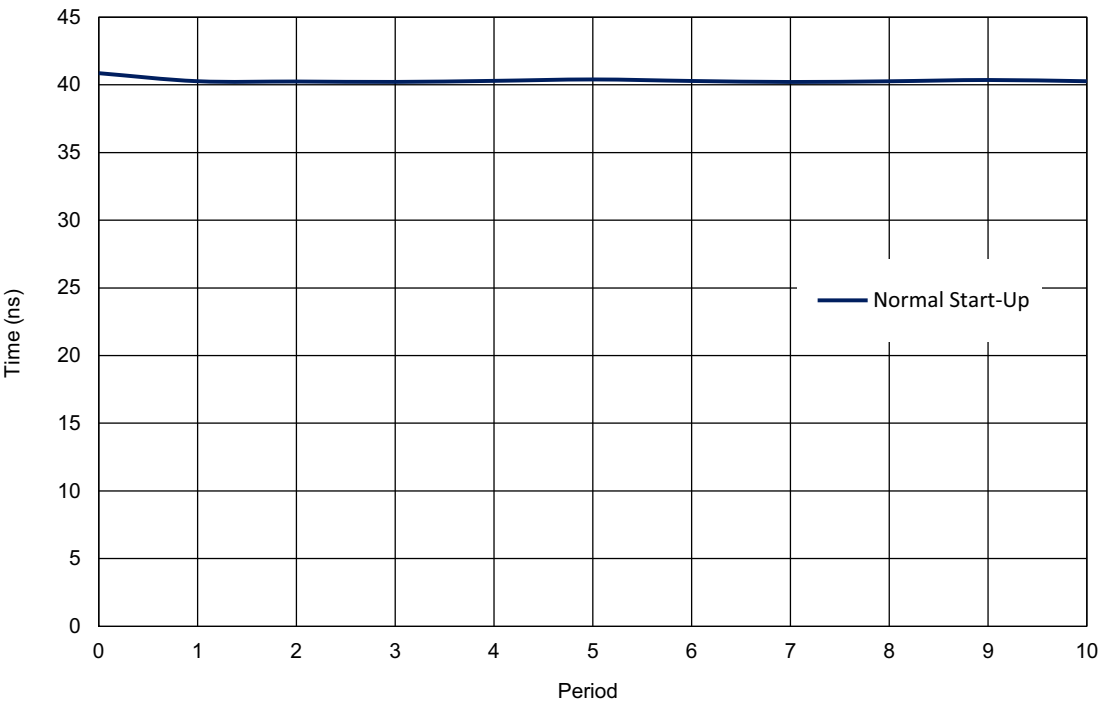


Figure 82. Oscillator1 Settling Time,  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25\text{ }^{\circ}\text{C}$ , OSC2 = 25 MHz

13.7 Oscillators Current Consumption

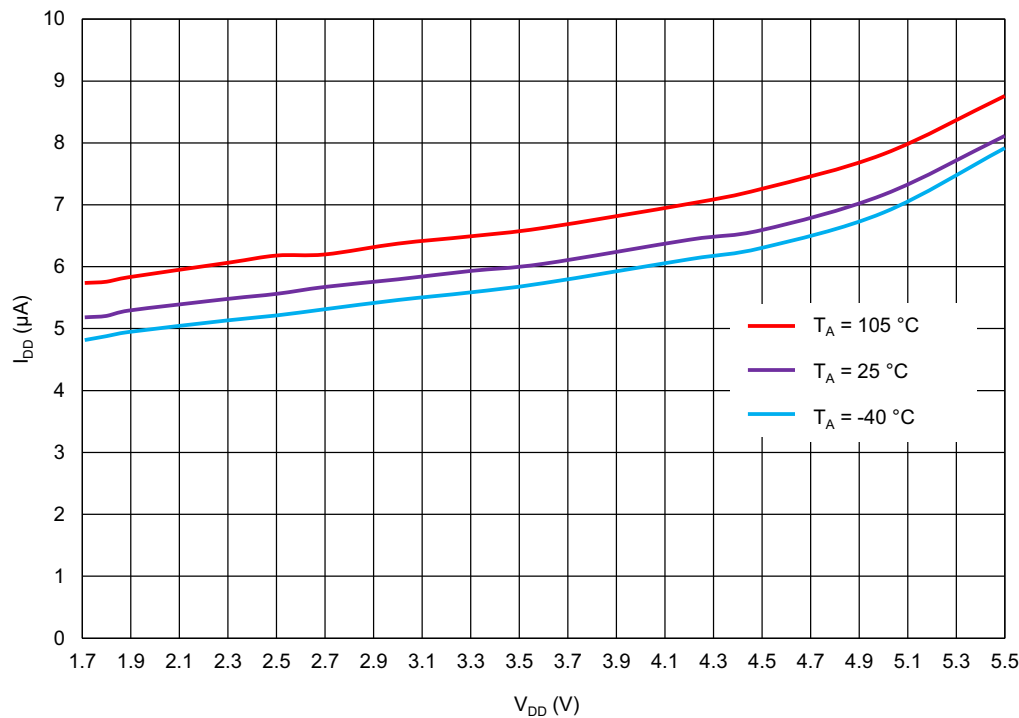


Figure 83. OSC0 (25 kHz) Current Consumption vs.  $V_{DD}$ , All Pre-Dividers

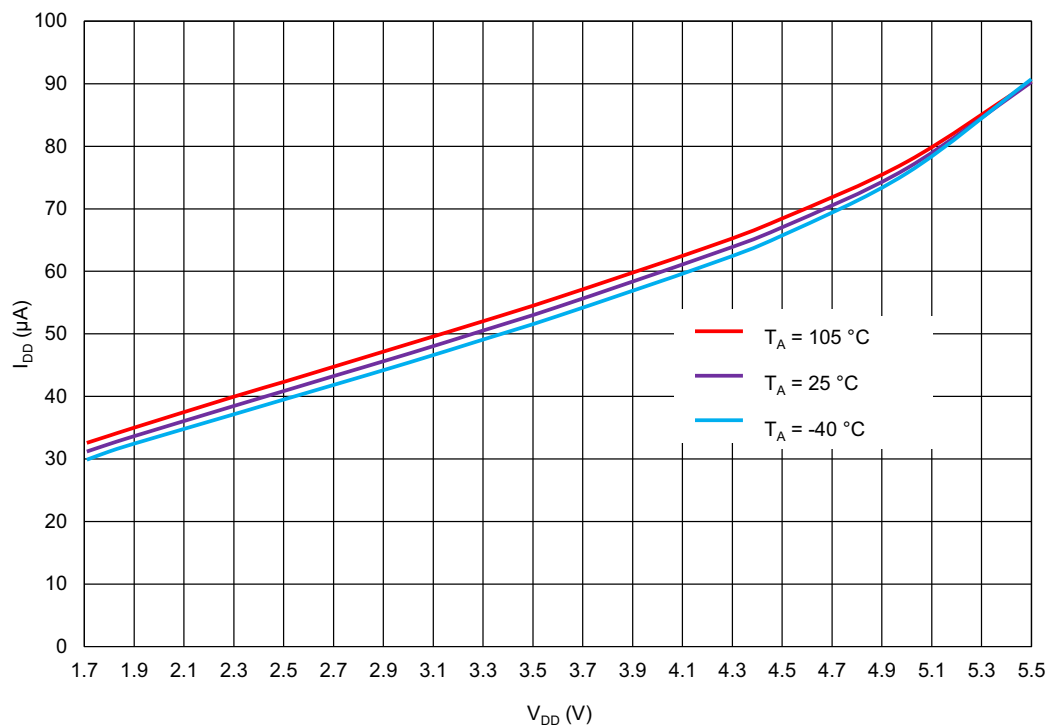


Figure 84. OSC0 (2 MHz) Current Consumption vs.  $V_{DD}$ , Pre-Divider = 1

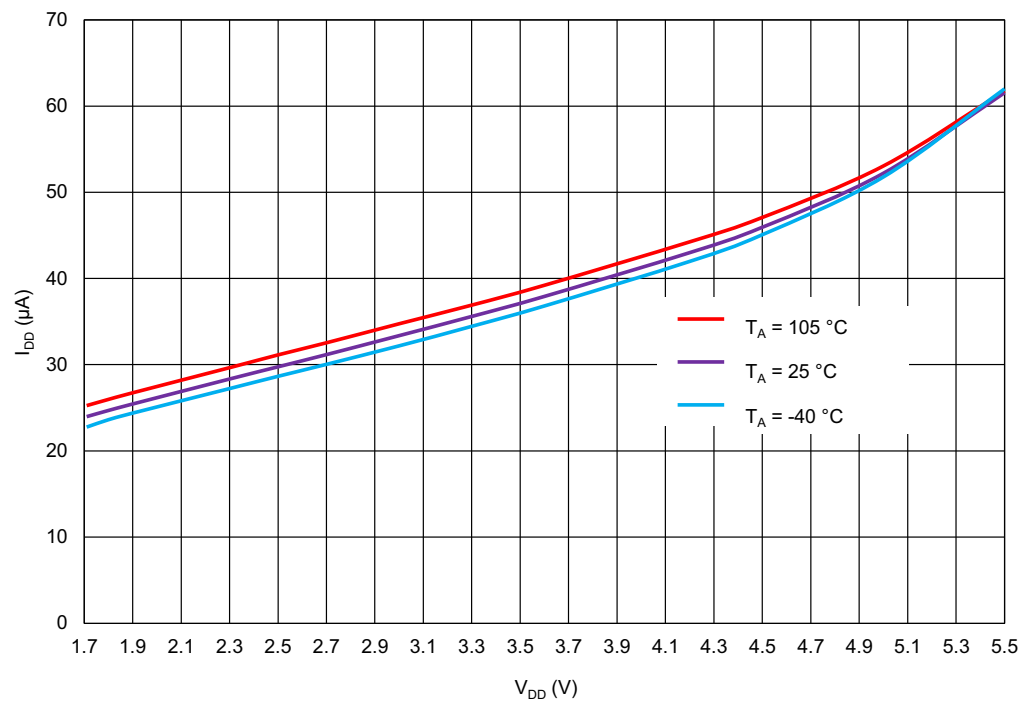


Figure 85. OSC0 (2 MHz) Current Consumption vs. V<sub>DD</sub>, Pre-Divider = 2

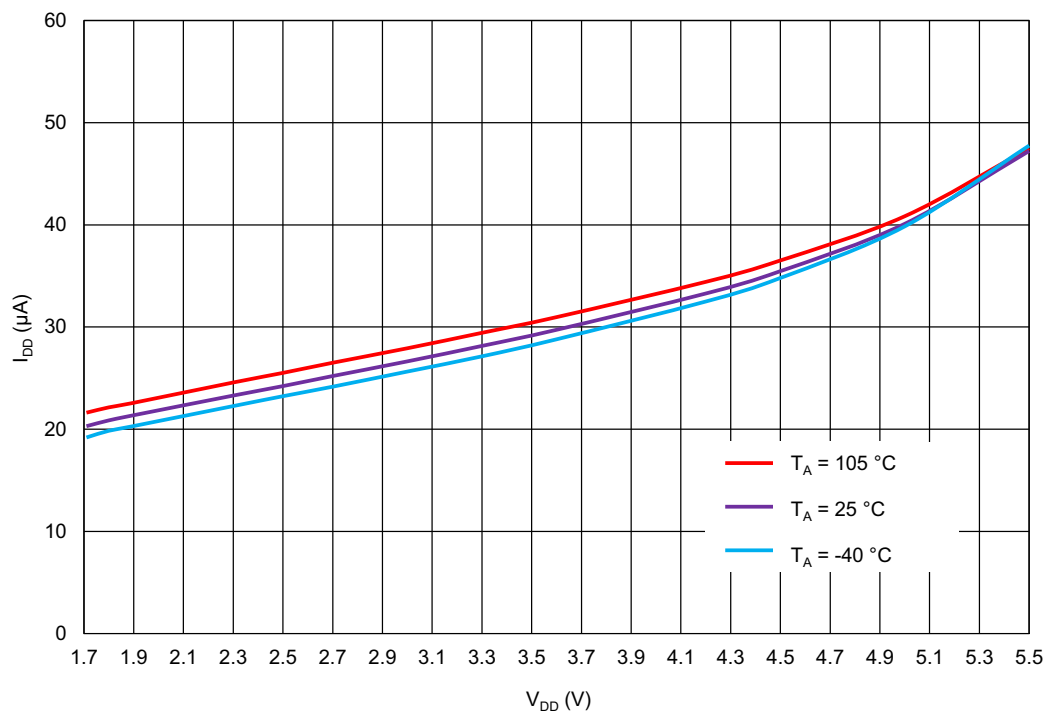


Figure 86. OSC0 (2 MHz) Current Consumption vs. V<sub>DD</sub>, Pre-Divider = 4

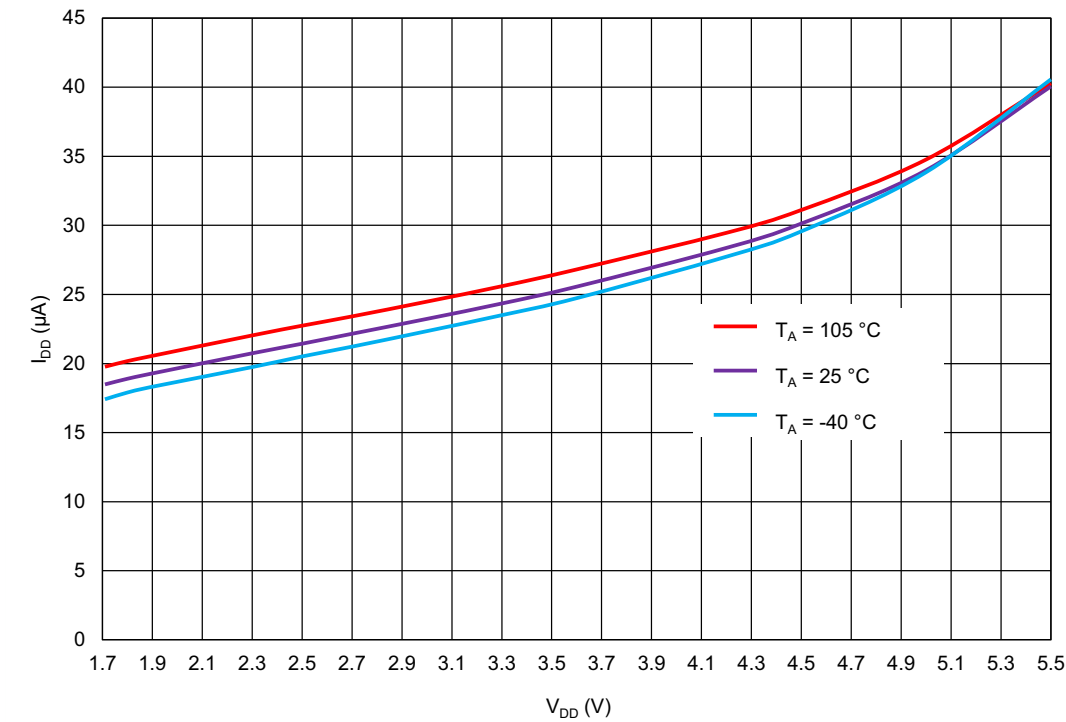


Figure 87. OSC0 (2 MHz) Current Consumption vs.  $V_{DD}$ , Pre-Divider = 8

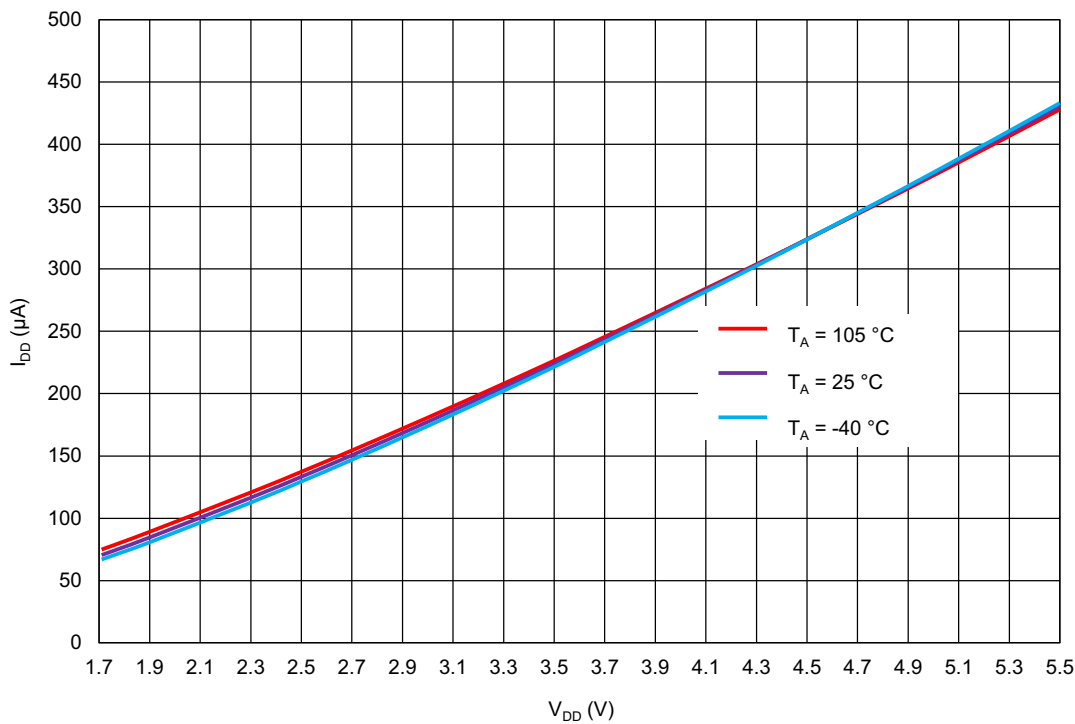


Figure 88. OSC1 (25 MHz) Current Consumption vs.  $V_{DD}$ , Pre-Divider = 1

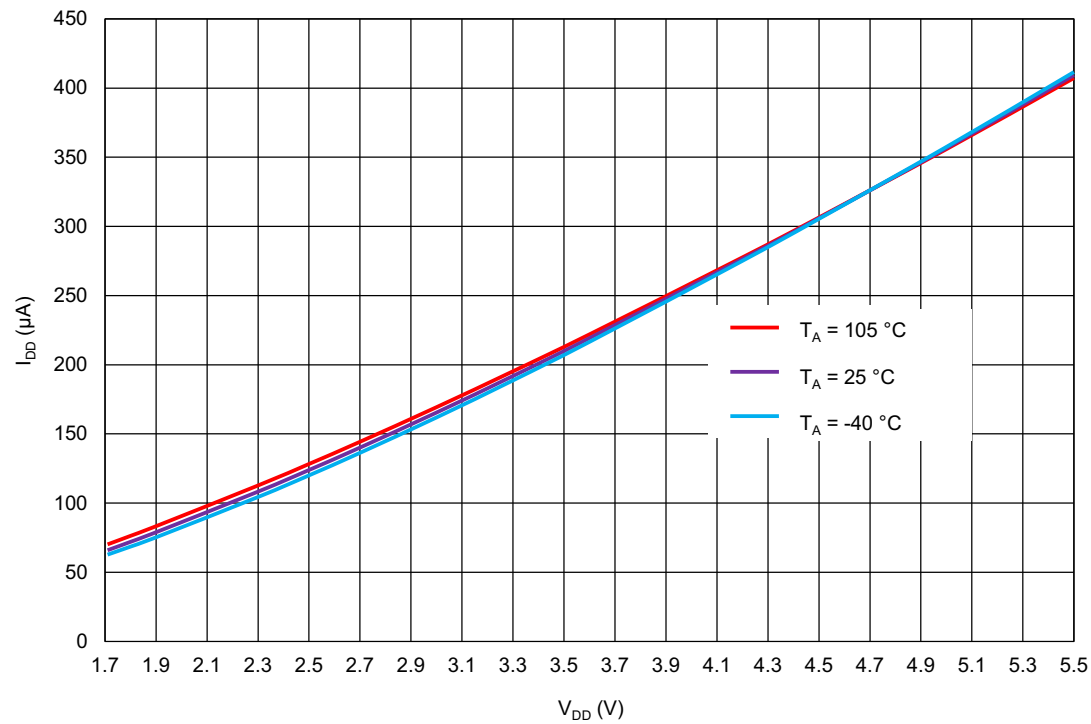


Figure 89. OSC1 (25 MHz) Current Consumption vs.  $V_{DD}$ , Pre-Divider = 2

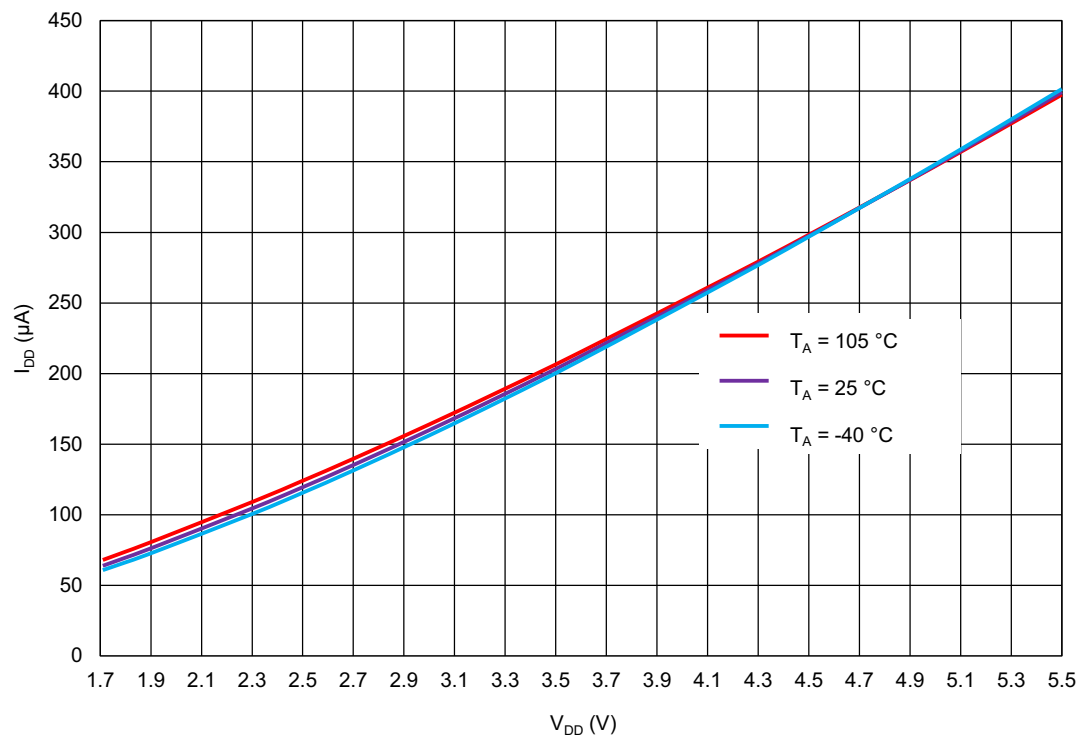


Figure 90. OSC1 (25 MHz) Current Consumption vs.  $V_{DD}$ , Pre-Divider = 4

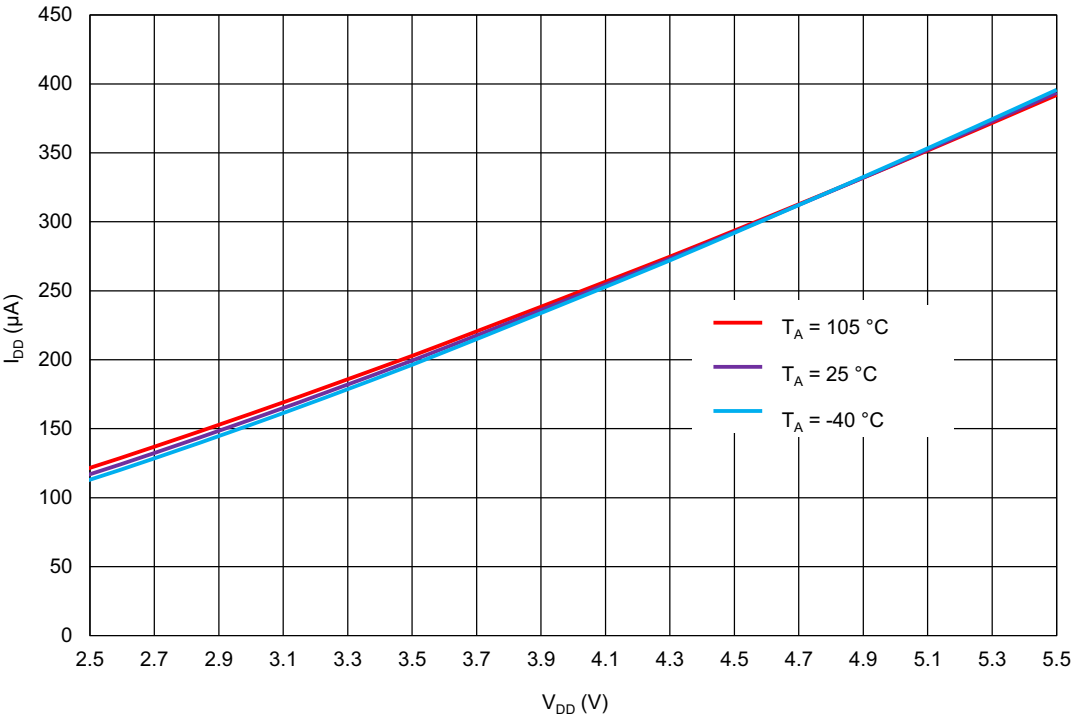


Figure 91. OSC1 (25 MHz) Current Consumption vs.  $V_{DD}$ , Pre-Divider = 8

## 14. Power-On Reset

The SLG46533-E has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the  $V_{DD}$  power is first ramping to the device, and also while the  $V_{DD}$  is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

### 14.1 General Operation

To start the POR sequence in the SLG46533-E, the voltage applied on the  $V_{DD}$  should be higher than the Power-On Threshold (**Note 1**). The full operational  $V_{DD}$  range for the SLG46533-E is 1.71 V to 5.5 V (1.8 V  $\pm 5\%$  to 5.0 V  $\pm 10\%$ ). This means that the  $V_{DD}$  voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the  $V_{DD}$  voltage rises to the Power-On Threshold. After the POR sequence has started, the SLG46533-E will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

The SLG46533-E is guaranteed to be powered down and nonoperational when the  $V_{DD}$  voltage (voltage on  $V_{DD}$ ) is less than Power-Off Threshold (see in Electrical Specifications table), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher than the  $V_{DD}$  voltage is applied to any other PIN (**Note 2**). For example, if  $V_{DD}$  voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

**Note 1:** The Power-On Threshold is defined in Electrical Specifications table.

**Note 2:** There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.

To power down the chip the  $V_{DD}$  voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on PINs can't be bigger than the  $V_{DD}$ , this rule also applies to the case when the chip is powered on.

## 14.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 92.

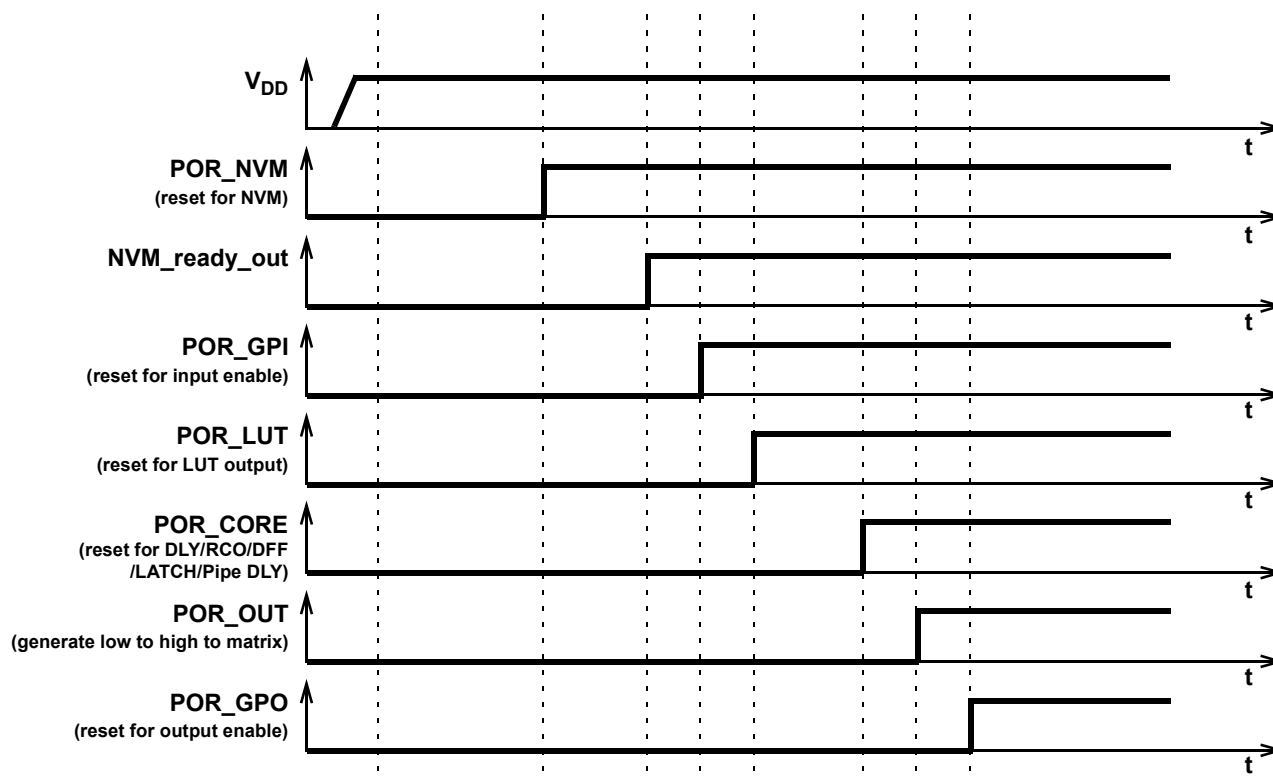


Figure 92. POR Sequence

As can be seen from Figure 92 after the  $V_{DD}$  has start ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSC, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate,  $V_{DD}$  value, temperature, and even will vary from chip to chip (process influence).

## 14.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46533-E operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 93 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

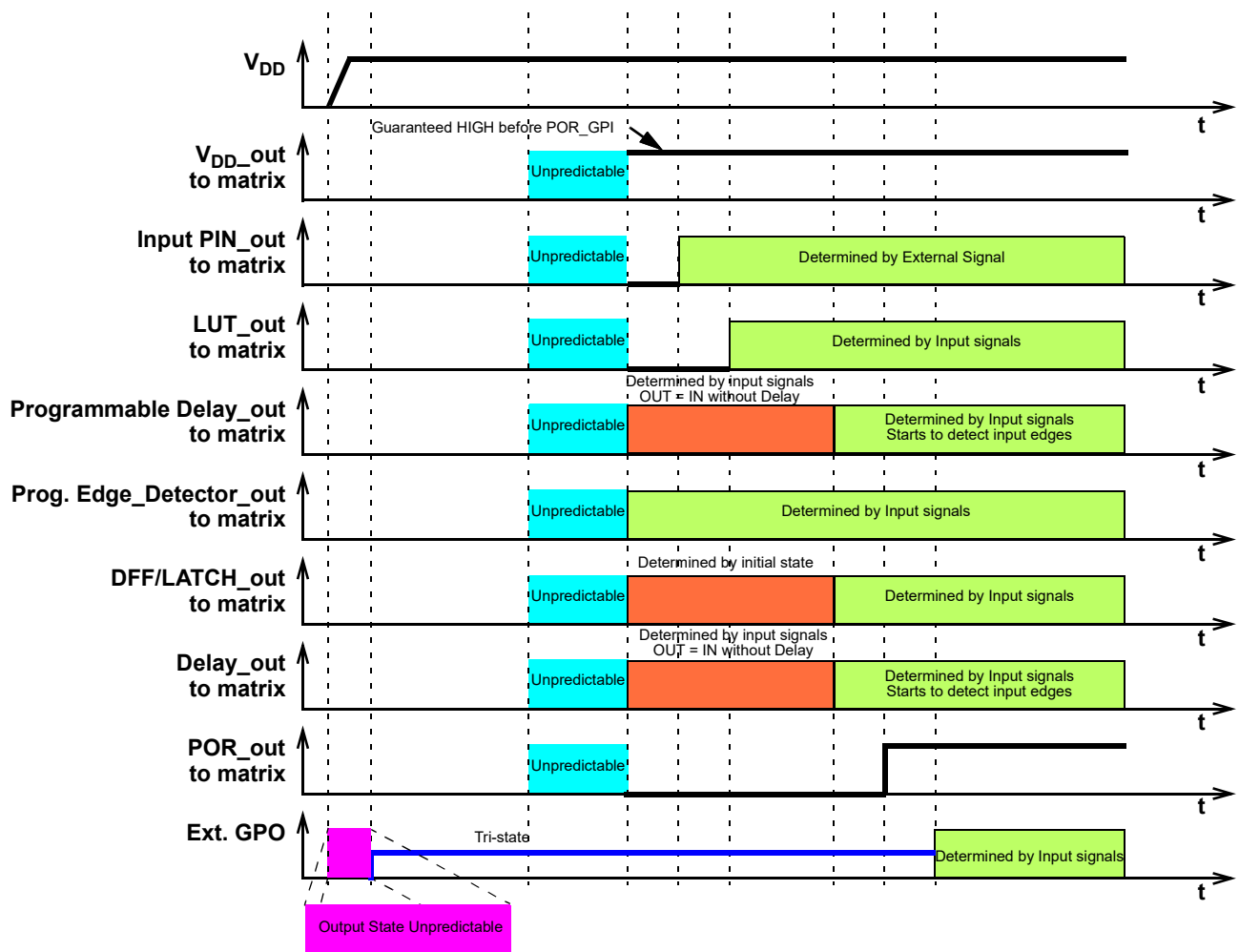


Figure 93. Internal Macrocell States during POR Sequence

### 14.3.1 Initialization

All internal macrocells by default have initial LOW level. Starting from indicated power-up time of 1.15 V to 1.6 V, macrocells in GPAK are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

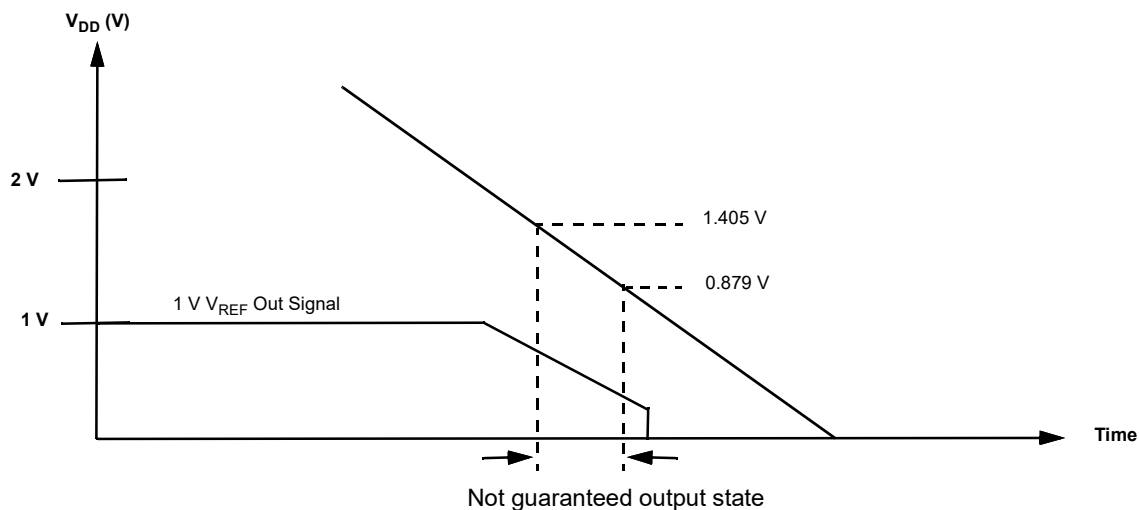
1. I<sup>2</sup>C.
2. Input PINs, ACMP, Pull-up/down.
3. LUTs.
4. DFFs, Delays/Counters, Pipe Delay.
5. POR output to matrix.
6. Output PIN corresponds to the internal logic.

The  $V_{REF}$  output pin driving signal can precede POR output signal going high by 3  $\mu$ s - 5  $\mu$ s. The POR signal going high indicates the mentioned power-up sequence is complete.

**Note:** The maximum voltage applied to any PIN should not be higher than the  $V_{DD}$  level. There are ESD Diodes between  $PIN \rightarrow V_{DD}$  and  $PIN \rightarrow GND$  on each PIN. So, if the input signal applied to PIN is higher than  $V_{DD}$ , then current will sink through the diode to  $V_{DD}$ . Exceeding  $V_{DD}$  results in leakage current on the input PIN, and  $V_{DD}$  will

be pulled up, following the voltage on the input PIN. There is no effect from input pin when input voltage is applied at the same time as  $V_{DD}$ .

### 14.3.2 Power-Down



**Figure 94. Power-Down**

During power-down, macrocells in SLG46533-E are powered off after  $V_{DD}$  falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

## 15. I<sup>2</sup>C Serial Communications Macrocell

### 15.1 I<sup>2</sup>C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I<sup>2</sup>C Serial Communications Macrocell in this device allows an I<sup>2</sup>C bus Controller to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I<sup>2</sup>C bus Controller is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I<sup>2</sup>C bus Controller the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits register [1832], register [1870], and register [1871]. See section [15.5 I<sup>2</sup>C Serial Command Register Protection](#) for more details on I<sup>2</sup>C read/write memory protection.

**Note:** GreenPAK I<sup>2</sup>C is fully compatible with standard I<sup>2</sup>C protocol.

### 15.2 I<sup>2</sup>C Serial Communications Device Addressing

Each command to the I<sup>2</sup>C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in [Figure 95](#). After the Start bit, the first four bits are a control code, which can be set by the user in registers [1867:1864]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I<sup>2</sup>C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I<sup>2</sup>C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device chooses to set the Control Code to either "1111" or "0000" in a system with other target device, please consult the I<sup>2</sup>C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I<sup>2</sup>C Macrocell on the SLG46533-E are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46533-E.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. [Figure 95](#) shows this basic command structure.

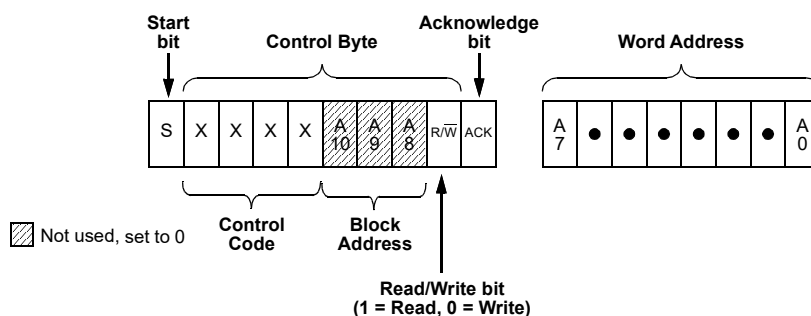
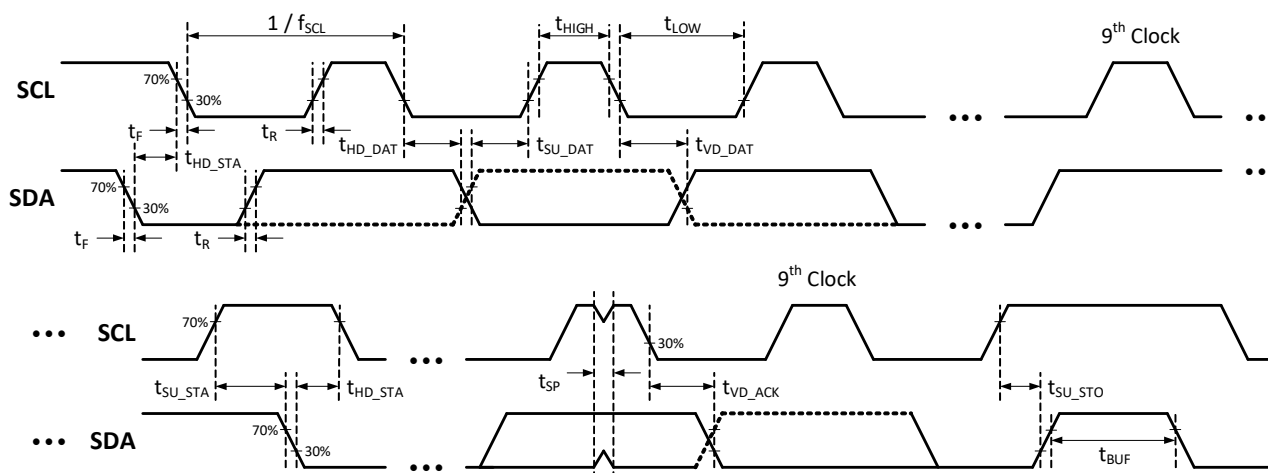


Figure 95. Basic Command Structure

## 15.3 I<sup>2</sup>C Serial General Timing

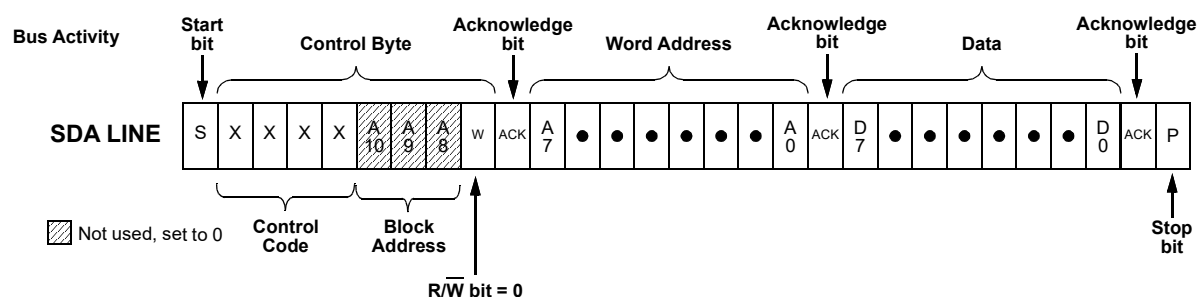
General timing characteristics for the I<sup>2</sup>C Serial Communications macrocell are shown in Figure 96. Timing specifications can be found in section 3.4 Electrical Specifications.

Figure 96. I<sup>2</sup>C General Timing Characteristics

## 15.4 I<sup>2</sup>C Serial Communications Commands

### 15.4.1 Byte Write Command

Following the Start condition from the Controller, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to "0"), are placed onto the I<sup>2</sup>C bus by the Controller. After the SLG46533-E sends an Acknowledge bit (ACK), the next byte transmitted by the Controller is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46533-E, where the data byte is to be written. After the SLG46533-E sends another Acknowledge bit, the Controller will transmit the data byte to be written into the addressed memory location. The SLG46533-E again provides an Acknowledge bit and then the Controller generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46533-E generates the Acknowledge bit.

Figure 97. Byte Write Command,  $\overline{R/W} = 0$ 

### 15.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG46533-E in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Controller continues to transmit data bytes to the SLG46533-E. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46533-E generates the Acknowledge bit.

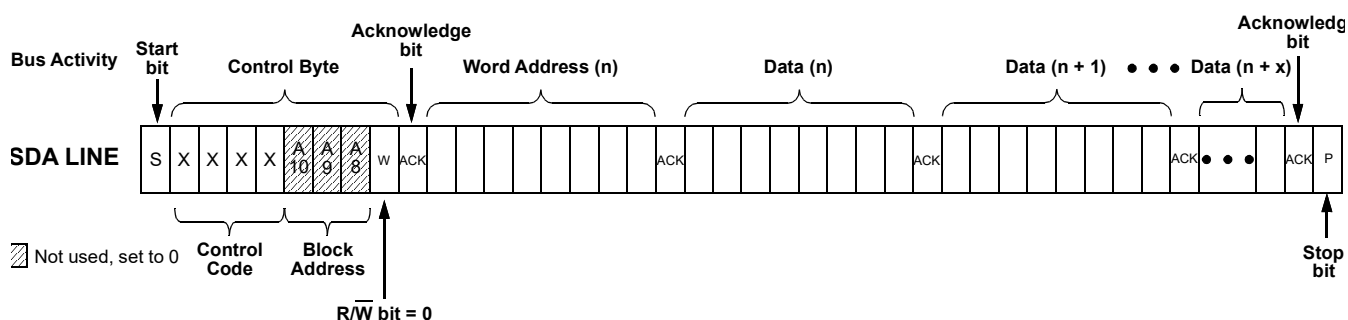
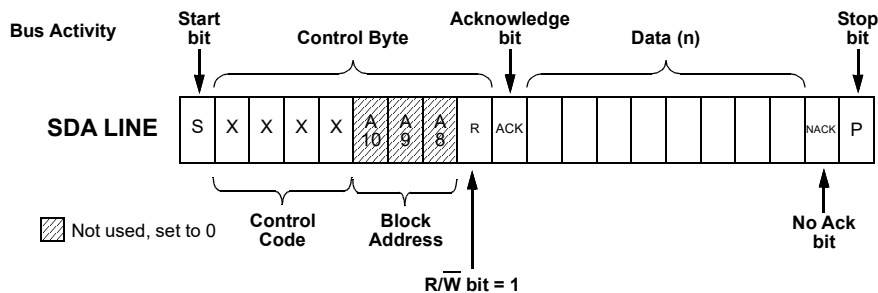


Figure 98. Sequential Write Command

### 15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address  $n$ , the address pointer would get incremented to  $n + 1$  upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at  $n + 1$ . The Current Address Read Command contains the Control Byte sent by the Controller, with the  $\overline{R/W}$  bit = "1". The SLG46533-E will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Controller will not issue an Acknowledge bit, and follow immediately with a Stop condition.

Figure 99. Current Address Read Command,  $R/\bar{W} = 1$ 

#### 15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Controller issues a second control byte with the R/W bit set to “1”, after which the SLG46533-E issues an Acknowledge bit, followed by the requested eight data bits.

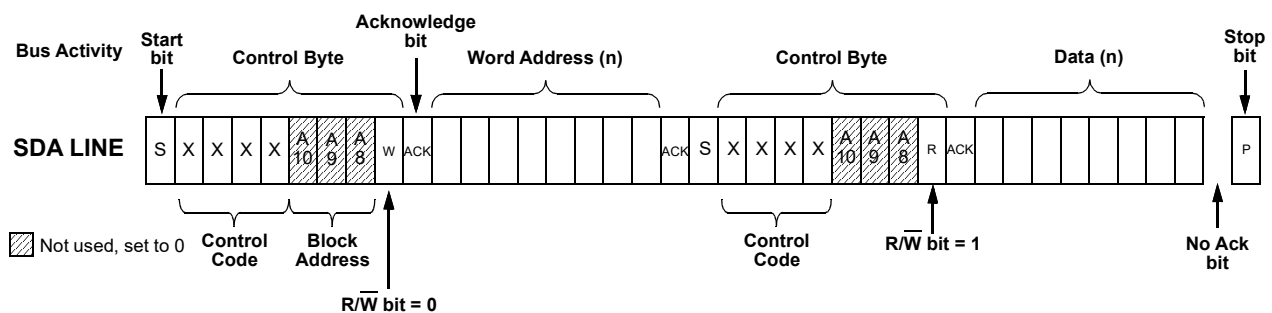


Figure 100. Random Read Command

#### 15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Current Address Read or Random Read command, except that once the SLG46533-E transmits the first data byte, the Controller issues an Acknowledge bit as opposed to a Stop condition in a random read. The Controller can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

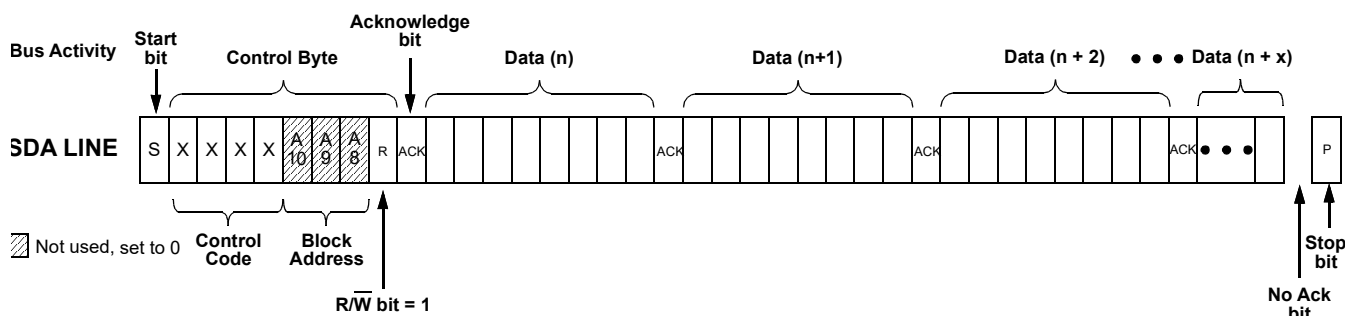


Figure 101. Sequential Read Command

### 15.4.6 I<sup>2</sup>C Serial Command Address Space

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I<sup>2</sup>C Macrocell on the SLG46533-E are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be “0” for all commands to the SLG46533-E.

### 15.4.7 I<sup>2</sup>C Serial Command Register Map

These register addresses are broken down into four Banks to give the user greater control on access to reading and writing information in each bank. Each of the four banks is 512 bits (64 bytes) in length. Writing information to register bits in these Banks will change the configuration of the device, resulting in either a change in the interconnection options provided by the Connection Matrix, or by changing the configuration of individual macrocells. During device use, all register bits can be read or written via I<sup>2</sup>C, unless protection bits are set to prevent this.

See section [17. Register Definitions](#) for detailed information on all register bits.

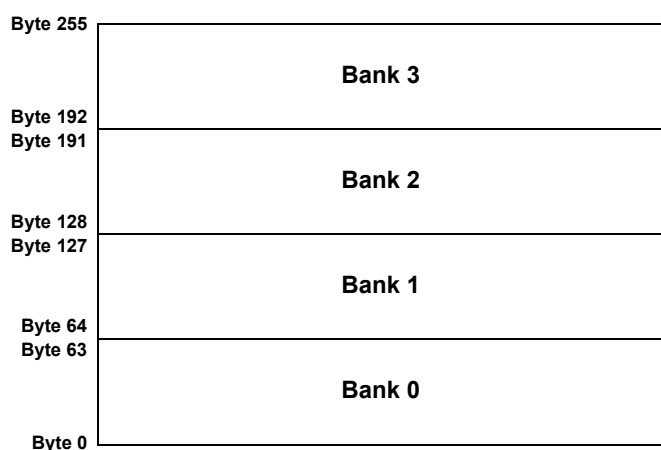


Figure 102. Register Bank Map

## 15.5 I<sup>2</sup>C Serial Command Register Protection

The memory space is divided into four banks, each of which has 512 bits (64 bytes). There are three bits that allow the user to define rules for reading and writing bits in each of these banks via I<sup>2</sup>C:

- register [1832] I<sup>2</sup>C lock for read bits [1535:0] (Bank 0/1/2). If the system provides any read commands to the addresses in these three banks, the device will respond with 'FFH' in data field.
- register [1871] I<sup>2</sup>C lock for write bits [1535:0] (Bank 0/1/2). If the system provides any write commands to the addresses in these three banks, the device will acknowledge these commands, but will not do internal writes to the register space.
- register [1870] I<sup>2</sup>C lock for write all bits (Bank 0/1/2/3). If the system provides any write commands to the addresses in these four banks, the device will acknowledge these commands, but will not do internal writes to the register space.

**Note 1:** register [1870] is higher priority than register [1871], and if register [1870] is set, then register [1871] does not have any effect.

**Note 2:** If the user sets IOs 6 and 7 function to a selection other than SDA and SCL, all access via I<sup>2</sup>C will be disabled.

If register [1870] is not set, register bits in Bank 3 are open to read and write commands via I<sup>2</sup>C with the following exceptions:

- register [1871] Bank 0/1/2 I<sup>2</sup>C-write protection bit is always protected from I<sup>2</sup>C write
- registers [1867:1864] I<sup>2</sup>C Control Code Bit [3:0] is always protected from I<sup>2</sup>C write.

**Note:** Any write commands that come to the device via I<sup>2</sup>C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See section [17. Register Definitions](#) for detailed information on all registers.

### 15.5.1 Register Read/Write Protection

There are six read/write protect modes for the design sequence from being corrupted or copied. See [Table 36](#) for details.

**Table 36. Read/Write Protection Options**

| Bank | Byte    | Bits            | Description                                                                                | Lock Status                                 |                                             |                                             |                                             |                                             |                                                  |
|------|---------|-----------------|--------------------------------------------------------------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|--------------------------------------------------|
|      |         |                 |                                                                                            | Unlocked                                    | Locked for read bits [1535:0]               | Locked for write bits [1535:0]              | Locked for write all bits                   | Locked for read and write bits [1535:0]     | Locked for read bits [1535:0] and write all bits |
|      |         |                 |                                                                                            | register [1832] = 0, [1871] = 0, [1870] = 0 | register [1832] = 1, [1871] = 0, [1870] = 0 | register [1832] = 0, [1871] = 1, [1870] = 0 | register [1832] = 0, [1871] = x, [1870] = 1 | register [1832] = 1, [1871] = 1, [1870] = 0 | register [1832] = 1, [1871] = x, [1870] = 1      |
| 0    | 0-63    | 511-0           | Connection Matrix                                                                          | R/W                                         | W                                           | R                                           | R                                           | -                                           | -                                                |
| 1    | 64-109  | 879-512         | Outputs Configuration                                                                      | R/W                                         | W                                           | R                                           | R                                           | -                                           | -                                                |
|      | 110-127 | 880-1023        | Reserved                                                                                   | -                                           | -                                           | -                                           | -                                           | -                                           | -                                                |
| 2    | 128-186 | 1495-1024       | Function Configuration for PINs, LUTs/DFFs, OSC, ASM and some configuration for DLYs, ACMP | R/W                                         | W                                           | R                                           | R                                           | -                                           | -                                                |
|      | 187-191 | 1535-1496       | Reserved                                                                                   | -                                           | -                                           | -                                           | -                                           | -                                           | -                                                |
| 3    | 192-206 | 1655-1536       | CNT/DLY counter data and some LUTs truth table, ACMP V <sub>REF</sub>                      | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 207     | 1662            | I <sup>2</sup> C reset bit with reloading NVM into Data register                           | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      |         | 1661-1659, 1663 | Reserved                                                                                   | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      |         | 1658-1656       | OSC Power Control                                                                          | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |

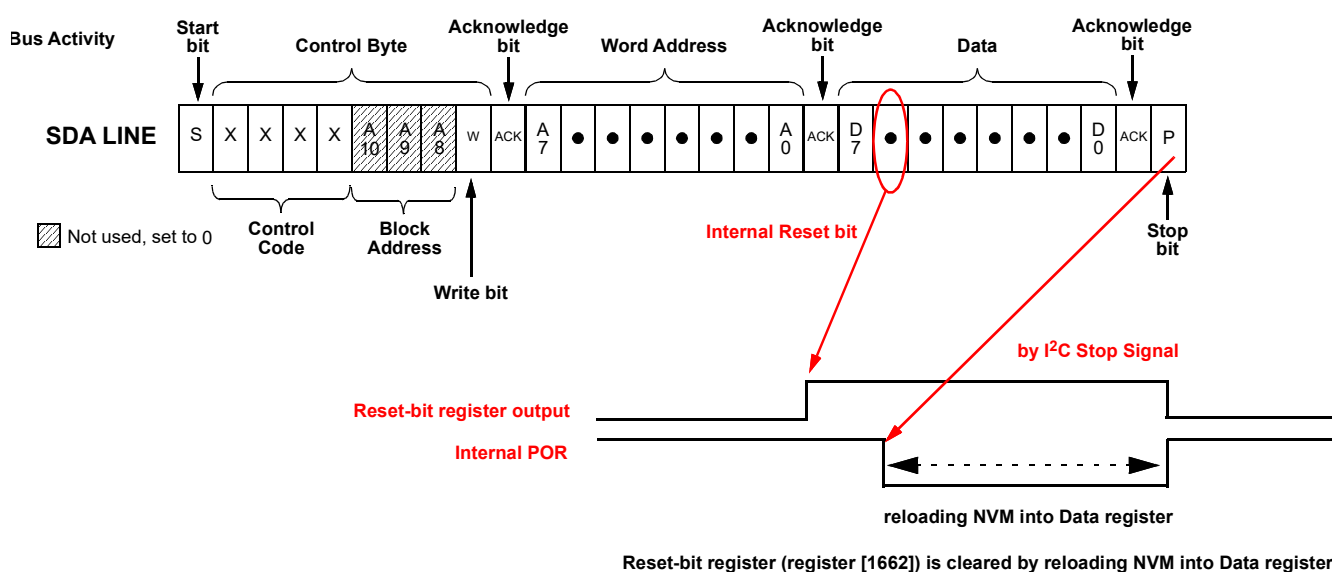
Table 36. Read/Write Protection Options (Cont.)

| Bank | Byte    | Bits                                     | Description                                         | Lock Status                                 |                                             |                                             |                                             |                                             |                                                  |
|------|---------|------------------------------------------|-----------------------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|--------------------------------------------------|
|      |         |                                          |                                                     | Unlocked                                    | Locked for read bits [1535:0]               | Locked for write bits [1535:0]              | Locked for write all bits                   | Locked for read and write bits [1535:0]     | Locked for read bits [1535:0] and write all bits |
|      |         |                                          |                                                     | register [1832] = 0, [1871] = 0, [1870] = 0 | register [1832] = 1, [1871] = 0, [1870] = 0 | register [1832] = 0, [1871] = 1, [1870] = 0 | register [1832] = 0, [1871] = x, [1870] = 1 | register [1832] = 1, [1871] = 1, [1870] = 0 | register [1832] = 1, [1871] = x, [1870] = 1      |
| 3    | 208-223 | 1791-1664                                | ASM output RAM and User configurable RAM/OTP        | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 224-227 | 1823-1792                                | Reserved                                            | -                                           | -                                           | -                                           | -                                           | -                                           | -                                                |
|      | 228     | 1831-1824                                | Reserved                                            | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 229     | 1839-1836                                | Product Family ID                                   | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      |         | 1835-1834                                | Reserved                                            | -                                           | -                                           | -                                           | -                                           | -                                           | -                                                |
|      |         | 1833                                     | Reserved                                            | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      |         | 1832                                     | I <sup>2</sup> C Lock for read bits [1535:0]        | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 230     | 1847-1840                                | Pattern ID                                          | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 231     | 1855-1848                                | Reserved                                            | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 232     | 1863-1856                                | Reserved                                            | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 233     | 1871                                     | I <sup>2</sup> C Lock for write bits [1535:0]       | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      |         | 1870                                     | I <sup>2</sup> C Lock for write all bits            | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      |         | 1869-1868                                | Reserved                                            | -                                           | -                                           | -                                           | -                                           | -                                           | -                                                |
|      |         | 1867-1864                                | I <sup>2</sup> C Control Code                       | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 234-239 | 1919-1872                                | Counter Current Value                               | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 240-243 | 1951-1920                                | Macrocells Output Values (Connection Matrix Inputs) | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 244     | 1959-1952                                | Connection Matrix Virtual Inputs                    | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 245-247 | 1983-1960                                | Macrocells Output Values (Connection Matrix Inputs) | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 248-250 | 2007-1984                                | Reserved                                            | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
| 3    | 251     | 2015-2008                                | Reserved                                            | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 252-253 | 2031-2016                                | Reserved                                            | R                                           | R                                           | R                                           | R                                           | R                                           | R                                                |
|      | 254     | 2039-2032                                | Reserved                                            | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
|      | 255     | 2047-2040                                | Reserved                                            | R/W                                         | R/W                                         | R/W                                         | R                                           | R/W                                         | R                                                |
| R/W  |         | Allow Read and Write Data                |                                                     |                                             |                                             |                                             |                                             |                                             |                                                  |
| W    |         | Allow Write Data Only                    |                                                     |                                             |                                             |                                             |                                             |                                             |                                                  |
| R    |         | Allow Read Data Only                     |                                                     |                                             |                                             |                                             |                                             |                                             |                                                  |
| -    |         | The Data is protected for Read and Write |                                                     |                                             |                                             |                                             |                                             |                                             |                                                  |

## 15.5.2 I<sup>2</sup>C Serial Reset Command

If I<sup>2</sup>C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1662] I<sup>2</sup>C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1662] will be set to “0” automatically. Figure 103 illustrates the sequence of events for this reset function.

**Note:** I<sup>2</sup>C Serial Reset Command is not available during emulation.



- 1) I<sup>2</sup>C write with register [1662] = 1 (I<sup>2</sup>C reset bit with reloading NVM into Data register).
- 2) POR go to LOW and reloading NVM into Data register start after “STOP” of I<sup>2</sup>C.
- 3) POR go to HIGH after reloading NVM into Data register.

Figure 103. Reset Command Timing

## 15.6 I<sup>2</sup>C Additional Options

### 15.6.1 Reading Counter Data via I<sup>2</sup>C

The current count value in four counters in the device can be read via I<sup>2</sup>C. The counters that have this additional functionality are 16-bit CNT0 and CNT1, and 8-bit counters CNT4 and CNT6.

### 15.6.2 User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I<sup>2</sup>C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User Configurable RAM/OTP Byte 0) is located at I<sup>2</sup>C address 0xD8, and the highest order byte in this array is located at I<sup>2</sup>C address 0xDF.

Table 37. RAM Array Table

| I <sup>2</sup> C Address<br>(hex) | Highest Bit<br>Address | Lowest Bit<br>Address | Memory Byte                       |
|-----------------------------------|------------------------|-----------------------|-----------------------------------|
| D0                                | 1671                   | 1664                  | User Configurable RAM/OTP Byte 8  |
| D1                                | 1679                   | 1672                  | User Configurable RAM/OTP Byte 9  |
| D2                                | 1687                   | 1680                  | User Configurable RAM/OTP Byte 10 |
| D3                                | 1695                   | 1688                  | User Configurable RAM/OTP Byte 11 |
| D4                                | 1703                   | 1696                  | User Configurable RAM/OTP Byte 12 |
| D5                                | 1711                   | 1704                  | User Configurable RAM/OTP Byte 13 |
| D6                                | 1719                   | 1712                  | User Configurable RAM/OTP Byte 14 |
| D7                                | 1727                   | 1720                  | User Configurable RAM/OTP Byte 15 |
| D8                                | 1735                   | 1728                  | User Configurable RAM/OTP Byte 0  |

## 16. Analog Temperature Sensor

The SLG46533-E has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS is rated to operate over a -40 °C to +105 °C temperature range. The error in the Output Range 1 does not exceed ±11.2 °C. The error in the Output Range 2 does not exceed ±11.7 °C. For more detail refer to section [3.4.17 Analog Temperature Sensor Specifications](#).

The equations below calculates the typical analog voltage ( $V_{TS\_OUT}$ ) passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS1\_OUT} = -0.0035 \times T_J + 1.0522$$

$$V_{TS2\_OUT} = -0.0029 \times T_J + 0.8670$$

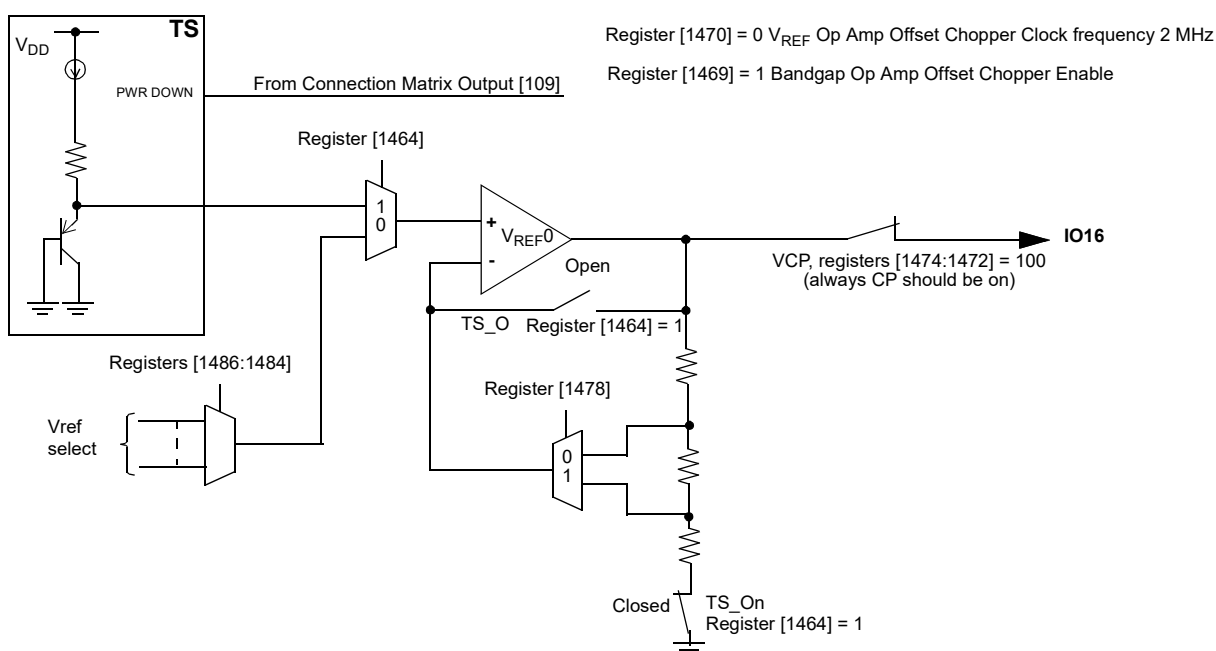


Figure 104. Analog Temperature Sensor Structure Diagram

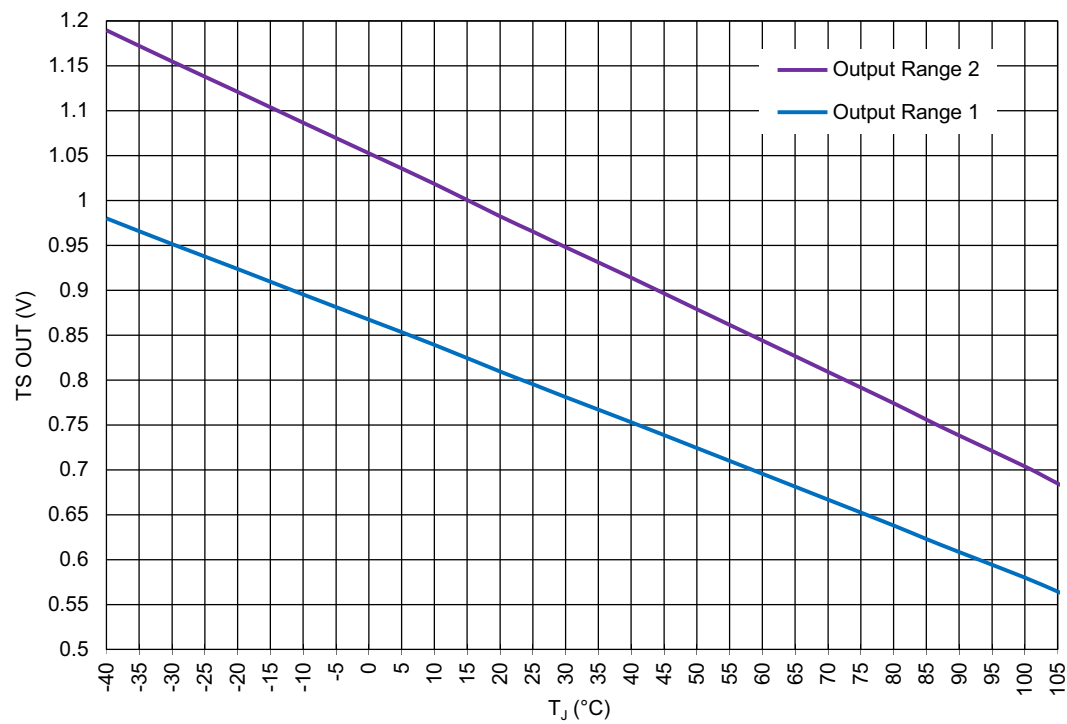


Figure 105. TS Output vs. Junction Temperature, V<sub>DD</sub> = 1.71 V to 5.5 V

## 17. Register Definitions

### 17.1 Register Map

Table 38. Register Map

| Address                                                                                                                                                                   |              | Signal Function | Register Bit Definition                    | I <sup>2</sup> C Interface |       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------------|--------------------------------------------|----------------------------|-------|
| Byte                                                                                                                                                                      | Register Bit |                 |                                            | Read                       | Write |
| Note: For register [0] to register [1495], I <sup>2</sup> C Read is valid (assuming register [1832] = 0), I <sup>2</sup> C Write is valid (assuming register [1871] = 0). |              |                 |                                            |                            |       |
| Matrix Output                                                                                                                                                             |              |                 |                                            |                            |       |
| 00                                                                                                                                                                        | 5:0          | Matrix OUT      | IN0 of 3-bit LUT11 or Clock Input of DFF8  | Valid                      | Valid |
|                                                                                                                                                                           | 7:6          | Reserved        |                                            | Valid                      | Valid |
| 01                                                                                                                                                                        | 13:8         | Matrix OUT      | IN1 of 3-bit LUT11 or Data Input of DFF8   | Valid                      | Valid |
|                                                                                                                                                                           | 15:14        | Reserved        |                                            | Valid                      | Valid |
| 02                                                                                                                                                                        | 21:16        | Matrix OUT      | IN2 of 3-bit LUT11 or nRST (nSET) of DFF8  | Valid                      | Valid |
|                                                                                                                                                                           | 23:22        | Reserved        |                                            | Valid                      | Valid |
| 03                                                                                                                                                                        | 29:24        | Matrix OUT      | IN0 of 3-bit LUT12 or Clock Input of DFF9  | Valid                      | Valid |
|                                                                                                                                                                           | 31:30        | Reserved        |                                            | Valid                      | Valid |
| 04                                                                                                                                                                        | 37:32        | Matrix OUT      | IN1 of 3-bit LUT12 or Data Input of DFF9   | Valid                      | Valid |
|                                                                                                                                                                           | 39:38        | Reserved        |                                            | Valid                      | Valid |
| 05                                                                                                                                                                        | 45:40        | Matrix OUT      | IN2 of 3-bit LUT12 or nRST (nSET) of DFF9  | Valid                      | Valid |
|                                                                                                                                                                           | 47:46        | Reserved        |                                            | Valid                      | Valid |
| 06                                                                                                                                                                        | 53:48        | Matrix OUT      | IN0 of 3-bit LUT13 or Clock Input of DFF10 | Valid                      | Valid |
|                                                                                                                                                                           | 55:54        | Reserved        |                                            | Valid                      | Valid |
| 07                                                                                                                                                                        | 61:56        | Matrix OUT      | IN1 of 3-bit LUT13 or Data Input of DFF10  | Valid                      | Valid |
|                                                                                                                                                                           | 63:62        | Reserved        |                                            | Valid                      | Valid |
| 08                                                                                                                                                                        | 69:64        | Matrix OUT      | IN2 of 3-bit LUT13 or nRST (nSET) of DFF10 | Valid                      | Valid |
|                                                                                                                                                                           | 71:70        | Reserved        |                                            | Valid                      | Valid |
| 09                                                                                                                                                                        | 77:72        | Matrix OUT      | IN0 of 3-bit LUT14 or Clock Input of DFF11 | Valid                      | Valid |
|                                                                                                                                                                           | 79:78        | Reserved        |                                            | Valid                      | Valid |
| 0A                                                                                                                                                                        | 85:80        | Matrix OUT      | IN1 of 3-bit LUT14 or Data Input of DFF11  | Valid                      | Valid |
|                                                                                                                                                                           | 87:86        | Reserved        |                                            | Valid                      | Valid |
| 0B                                                                                                                                                                        | 93:88        | Matrix OUT      | IN2 of 3-bit LUT14 or nRST (nSET) of DFF11 | Valid                      | Valid |
|                                                                                                                                                                           | 95:94        | Reserved        |                                            | Valid                      | Valid |
| 0C                                                                                                                                                                        | 101:96       | Matrix OUT      | IN0 of 3-bit LUT15 or Clock Input of DFF12 | Valid                      | Valid |
|                                                                                                                                                                           | 103:102      | Reserved        |                                            | Valid                      | Valid |
| 0D                                                                                                                                                                        | 109:104      | Matrix OUT      | IN1 of 3-bit LUT15 or Data Input of DFF12  | Valid                      | Valid |
|                                                                                                                                                                           | 111:110      | Reserved        |                                            | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function | Register Bit Definition                    | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------|--------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                 |                                            | Read                       | Write |
| 0E      | 117:112      | Matrix OUT      | IN2 of 3-bit LUT15 or nRST (nSET) of DFF12 | Valid                      | Valid |
|         | 119:118      | Reserved        |                                            | Valid                      | Valid |
| 0F      | 125:120      | Matrix OUT      | IN0 of 3-bit LUT16 or Clock Input of DFF13 | Valid                      | Valid |
|         | 127:126      | Reserved        |                                            | Valid                      | Valid |
| 10      | 133:128      | Matrix OUT      | IN1 of 3-bit LUT16 or Data Input of DFF13  | Valid                      | Valid |
|         | 135:134      | Reserved        |                                            | Valid                      | Valid |
| 11      | 141:136      | Matrix OUT      | IN2 of 3-bit LUT16 or nRST (nSET) of DFF13 | Valid                      | Valid |
|         | 143:142      | Reserved        |                                            | Valid                      | Valid |
| 12      | 149:144      | Matrix OUT      | IN0 of 3-bit LUT17 or Clock Input of DFF14 | Valid                      | Valid |
|         | 151:150      | Reserved        |                                            | Valid                      | Valid |
| 13      | 157:152      | Matrix OUT      | IN1 of 3-bit LUT17 or Data Input of DFF14  | Valid                      | Valid |
|         | 159:158      | Reserved        |                                            | Valid                      | Valid |
| 14      | 165:160      | Matrix OUT      | IN2 of 3-bit LUT17 or nRST (nSET) of DFF14 | Valid                      | Valid |
|         | 167:166      | Reserved        |                                            | Valid                      | Valid |
| 15      | 173:168      | Matrix OUT      | IN0 of 4-bit LUT2                          | Valid                      | Valid |
|         | 175:174      | Reserved        |                                            | Valid                      | Valid |
| 16      | 181:176      | Matrix OUT      | IN1 of 4-bit LUT2                          | Valid                      | Valid |
|         | 183:182      | Reserved        |                                            | Valid                      | Valid |
| 17      | 189:184      | Matrix OU       | IN2 of 4-bit LUT2                          | Valid                      | Valid |
|         | 191:190      | Reserved        |                                            | Valid                      | Valid |
| 18      | 197:192      | Matrix OUT      | IN3 of 4-bit LUT2                          | Valid                      | Valid |
|         | 199:198      | Reserved        |                                            | Valid                      | Valid |
| 19      | 205:200      | Matrix OUT      | IO1 Digital Output Source                  | Valid                      | Valid |
|         | 207:206      | Reserved        |                                            | Valid                      | Valid |
| 1A      | 213:208      | Matrix OUT      | IO1 Output Enable                          | Valid                      | Valid |
|         | 215:214      | Reserved        |                                            | Valid                      | Valid |
| 1B      | 221:216      | Matrix OUT      | IO2 Digital Output Source                  | Valid                      | Valid |
|         | 223:222      | Reserved        |                                            | Valid                      | Valid |
| 1C      | 229:224      | Matrix OUT      | IO3 Digital Output Source                  | Valid                      | Valid |
|         | 231:230      | Reserved        |                                            | Valid                      | Valid |
| 1D      | 237:232      | Matrix OUT      | IO3 Output Enable                          | Valid                      | Valid |
|         | 239:238      | Reserved        |                                            | Valid                      | Valid |
| 1E      | 245:240      | Matrix OUT      | IO4 Digital Output Source                  | Valid                      | Valid |
|         | 247:246      | Reserved        |                                            | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function | Register Bit Definition                                           | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------|-------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                 |                                                                   | Read                       | Write |
| 1F      | 253:248      | Matrix OUT      | IO5 Digital Output Source                                         | Valid                      | Valid |
|         | 255:254      | Reserved        |                                                                   | Valid                      | Valid |
| 20      | 261:256      | Matrix OUT      | IO5 Output Enable                                                 | Valid                      | Valid |
|         | 263:262      | Reserved        |                                                                   | Valid                      | Valid |
| 21      | 269:264      | Matrix OUT      | IO6 Digital Output Source (SCL with VI/Input and NMOS open-drain) | Valid                      | Valid |
|         | 271:270      | Reserved        |                                                                   | Valid                      | Valid |
| 22      | 277:272      | Matrix OUT      | IO7 Digital Output Source (SDA with VI/Input and NMOS open-drain) | Valid                      | Valid |
|         | 279:278      | Reserved        |                                                                   | Valid                      | Valid |
| 23      | 285:280      | Matrix OUT      | IO8 Digital Output Source                                         | Valid                      | Valid |
|         | 287:286      | Reserved        |                                                                   | Valid                      | Valid |
| 24      | 293:288      | Matrix OUT      | IO8 Output Enable                                                 | Valid                      | Valid |
|         | 295:294      | Reserved        |                                                                   | Valid                      | Valid |
| 25      | 301:296      | Matrix OUT      | IO9 Digital Output Source                                         | Valid                      | Valid |
|         | 303:302      | Reserved        |                                                                   | Valid                      | Valid |
| 26      | 309:304      | Matrix OUT      | IO10 Digital Output Source                                        | Valid                      | Valid |
|         | 311:310      | Reserved        |                                                                   | Valid                      | Valid |
| 27      | 317:312      | Matrix OUT      | IO10 Output Enable                                                | Valid                      | Valid |
|         | 319:318      | Reserved        |                                                                   | Valid                      | Valid |
| 28      | 325:320      | Matrix OUT      | IO11 Digital Output Source                                        | Valid                      | Valid |
|         | 327:326      | Reserved        |                                                                   | Valid                      | Valid |
| 29      | 333:328      | Matrix OUT      | IO11 Output Enable                                                | Valid                      | Valid |
|         | 335:334      | Reserved        |                                                                   | Valid                      | Valid |
| 2A      | 341:336      | Matrix OUT      | IO12 Digital Output Source                                        | Valid                      | Valid |
|         | 343:342      | Reserved        |                                                                   | Valid                      | Valid |
| 2B      | 349:344      | Matrix OUT      | IO13 Digital Output Source                                        | Valid                      | Valid |
|         | 351:350      | Reserved        |                                                                   | Valid                      | Valid |
| 2C      | 357:352      | Matrix OUT      | IO13 Output Enable                                                | Valid                      | Valid |
|         | 359:358      | Reserved        |                                                                   | Valid                      | Valid |
| 2D      | 365:360      | Matrix OUT      | IO14 Digital Output Source                                        | Valid                      | Valid |
|         | 367:366      | Reserved        |                                                                   | Valid                      | Valid |
| 2E      | 373:368      | Matrix OUT      | IO15 Digital Output Source                                        | Valid                      | Valid |
|         | 375:374      | Reserved        |                                                                   | Valid                      | Valid |
| 2F      | 381:376      | Matrix OUT      | IO15 Output Enable                                                | Valid                      | Valid |
|         | 383:382      | Reserved        |                                                                   | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function | Register Bit Definition                         | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------|-------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                 |                                                 | Read                       | Write |
| 30      | 389:384      | Matrix OUT      | IO16 Digital Output Source                      | Valid                      | Valid |
|         | 391:390      | Reserved        |                                                 | Valid                      | Valid |
| 31      | 397:392      | Matrix OUT      | IO16 Output Enable                              | Valid                      | Valid |
|         | 399:398      | Reserved        |                                                 | Valid                      | Valid |
| 32      | 405:400      | Matrix OUT      | IO17 Digital Output Source                      | Valid                      | Valid |
|         | 407:406      | Reserved        |                                                 | Valid                      | Valid |
| 33      | 413:408      | Matrix OUT      | ACMP0 nPD (Power-Down)                          | Valid                      | Valid |
|         | 415:414      | Reserved        |                                                 | Valid                      | Valid |
| 34      | 421:416      | Matrix OUT      | ACMP1 nPD (Power-Down)                          | Valid                      | Valid |
|         | 423:422      | Reserved        |                                                 | Valid                      | Valid |
| 35      | 429:424      | Matrix OUT      | ACMP2 nPD (Power-Down)                          | Valid                      | Valid |
|         | 431:430      | Reserved        |                                                 | Valid                      | Valid |
| 36      | 437:432      | Matrix OUT      | ACMP3 nPD (Power-Down)                          | Valid                      | Valid |
|         | 439:438      | Reserved        |                                                 | Valid                      | Valid |
| 37      | 445:440      | Matrix OUT      | Input of Filter_0 with fixed time edge detector | Valid                      | Valid |
|         | 447:446      | Reserved        |                                                 | Valid                      | Valid |
| 38      | 453:448      | Matrix OUT      | Input of Filter_1 with fixed time edge detector | Valid                      | Valid |
|         | 455:454      | Reserved        |                                                 | Valid                      | Valid |
| 39      | 461:456      | Matrix OUT      | Input of Programmable Delay and Edge Detector   | Valid                      | Valid |
|         | 463:462      | Reserved        |                                                 | Valid                      | Valid |
| 3A      | 469:464      | Matrix OUT      | OSC 25 kHz/2 MHz PD (Power-Down)                | Valid                      | Valid |
|         | 471:470      | Reserved        |                                                 | Valid                      | Valid |
| 3B      | 477:472      | Matrix OUT      | OSC 25 MHz PD (Power-Down)                      | Valid                      | Valid |
|         | 479:478      | Reserved        |                                                 | Valid                      | Valid |
| 3C      | 485:480      | Matrix OUT      | IN0 of 2-bit LUT0 or Clock Input of DFF0        | Valid                      | Valid |
|         | 487:486      | Reserved        |                                                 | Valid                      | Valid |
| 3D      | 493:488      | Matrix OUT      | IN1 of 2-bit LUT0 or Data Input of DFF0         | Valid                      | Valid |
|         | 495:494      | Reserved        |                                                 | Valid                      | Valid |
| 3E      | 501:496      | Matrix OUT      | IN0 of 2-bit LUT1 or Clock Input of DFF1        | Valid                      | Valid |
|         | 503:502      | Reserved        |                                                 | Valid                      | Valid |
| 3F      | 509:504      | Matrix OUT      | IN1 of 2-bit LUT1 or Data Input of DFF1         | Valid                      | Valid |
|         | 511:510      | Reserved        |                                                 | Valid                      | Valid |
| 40      | 517:512      | Matrix OUT      | IN0 of 2-bit LUT2 or Clock Input of DFF2        | Valid                      | Valid |
|         | 519:518      | Reserved        |                                                 | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function | Register Bit Definition                  | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------|------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                 |                                          | Read                       | Write |
| 41      | 525:520      | Matrix OUT      | IN1 of 2-bit LUT2 or Data Input of DFF2  | Valid                      | Valid |
|         | 527:526      | Reserved        |                                          | Valid                      | Valid |
| 42      | 533:528      | Matrix OUT      | IN0 of 2-bit LUT3 or Clock Input of PGen | Valid                      | Valid |
|         | 535:534      | Reserved        |                                          | Valid                      | Valid |
| 43      | 541:536      | Matrix OUT      | IN1 of 2-bit LUT3 or nRST of PGen        | Valid                      | Valid |
|         | 543:542      | Reserved        |                                          | Valid                      | Valid |
| 44      | 549:544      | Matrix OUT      | IN0 of 3-bit LUT0 or Clock Input of DFF3 | Valid                      | Valid |
|         | 551:550      | Reserved        |                                          | Valid                      | Valid |
| 45      | 557:552      | Matrix OUT      | IN1 of 3-bit LUT0 or Data Input of DFF3  | Valid                      | Valid |
|         | 559:558      | Reserved        |                                          | Valid                      | Valid |
| 46      | 565:560      | Matrix OUT      | IN2 of 3-bit LUT0 or nRST (nSET) of DFF3 | Valid                      | Valid |
|         | 567:566      | Reserved        |                                          | Valid                      | Valid |
| 47      | 573:568      | Matrix OUT      | IN0 of 3-bit LUT1 or Clock Input of DFF4 | Valid                      | Valid |
|         | 575:574      | Reserved        |                                          | Valid                      | Valid |
| 48      | 581:576      | Matrix OUT      | IN1 of 3-bit LUT1 or Data Input of DFF4  | Valid                      | Valid |
|         | 583:582      | Reserved        |                                          | Valid                      | Valid |
| 49      | 589:584      | Matrix OUT      | IN2 of 3-bit LUT1 or nRST (nSET) of DFF4 | Valid                      | Valid |
|         | 591:590      | Reserved        |                                          | Valid                      | Valid |
| 4A      | 597:592      | Matrix OUT      | IN0 of 3-bit LUT2 or Clock Input of DFF5 | Valid                      | Valid |
|         | 599:598      | Reserved        |                                          | Valid                      | Valid |
| 4B      | 605:600      | Matrix OUT      | IN1 of 3-bit LUT2 or Data Input of DFF5  | Valid                      | Valid |
|         | 607:606      | Reserved        |                                          | Valid                      | Valid |
| 4C      | 613:608      | Matrix OUT      | IN2 of 3-bit LUT2 or nRST (nSET) of DFF5 | Valid                      | Valid |
|         | 615:614      | Reserved        |                                          | Valid                      | Valid |
| 4D      | 621:616      | Matrix OUT      | IN0 of 3-bit LUT3 or Clock Input of DFF6 | Valid                      | Valid |
|         | 623:622      | Reserved        |                                          | Valid                      | Valid |
| 4E      | 629:624      | Matrix OUT      | IN1 of 3-bit LUT3 or Data Input of DFF6  | Valid                      | Valid |
|         | 631:630      | Reserved        |                                          | Valid                      | Valid |
| 4F      | 637:632      | Matrix OUT      | IN2 of 3-bit LUT3 or nRST (nSET) of DFF6 | Valid                      | Valid |
|         | 639:638      | Reserved        |                                          | Valid                      | Valid |
| 50      | 645:640      | Matrix OUT      | IN0 of 3-bit LUT4 or Clock Input of DFF7 | Valid                      | Valid |
|         | 647:646      | Reserved        |                                          | Valid                      | Valid |
| 51      | 653:648      | Matrix OUT      | IN1 of 3-bit LUT4 or Data Input of DFF7  | Valid                      | Valid |
|         | 655:654      | Reserved        |                                          | Valid                      | Valid |
| 52      | 661:656      | Matrix OUT      | IN2 of 3-bit LUT4 or nRST (nSET) of DFF7 | Valid                      | Valid |
|         | 663:662      | Reserved        |                                          | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function | Register Bit Definition                                           | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------|-------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                 |                                                                   | Read                       | Write |
| 53      | 669:664      | Matrix OUT      | IN0 of 3-bit LUT5 or Delay2 Input (or Counter2 RST Input)         | Valid                      | Valid |
|         | 671:670      | Reserved        |                                                                   | Valid                      | Valid |
| 54      | 677:672      | Matrix OUT      | IN1 of 3-bit LUT5 or External Clock Input of Delay2 (or Counter2) | Valid                      | Valid |
|         | 679:678      | Reserved        |                                                                   | Valid                      | Valid |
| 55      | 685:680      | Matrix OUT      | IN2 of 3-bit LUT5                                                 | Valid                      | Valid |
|         | 687:686      | Reserved        |                                                                   | Valid                      | Valid |
| 56      | 693:688      | Matrix OUT      | IN0 of 3-bit LUT6 or Delay3 Input (or Counter3 RST Input)         | Valid                      | Valid |
|         | 695:694      | Reserved        |                                                                   | Valid                      | Valid |
| 57      | 701:696      | Matrix OUT      | IN1 of 3-bit LUT6 or External Clock Input of Delay3 (or Counter3) | Valid                      | Valid |
|         | 703:702      | Reserved        |                                                                   | Valid                      | Valid |
| 58      | 709:704      | Matrix OUT      | IN2 of 3-bit LUT6                                                 | Valid                      | Valid |
|         | 711:710      | Reserved        |                                                                   | Valid                      | Valid |
| 59      | 717:712      | Matrix OUT      | IN0 of 3-bit LUT7 or Delay4 Input (or Counter4 RST Input)         | Valid                      | Valid |
|         | 719:718      | Reserved        |                                                                   | Valid                      | Valid |
| 5A      | 725:720      | Matrix OUT      | IN1 of 3-bit LUT7 or External Clock Input of Delay4 (or Counter4) | Valid                      | Valid |
|         | 727:726      | Reserved        |                                                                   | Valid                      | Valid |
| 5B      | 733:728      | Matrix OUT      | IN2 of 3-bit LUT7                                                 | Valid                      | Valid |
|         | 735:734      | Reserved        |                                                                   | Valid                      | Valid |
| 5C      | 741:736      | Matrix OUT      | IN0 of 3-bit LUT8 or Delay5 Input (or Counter5 RST Input)         | Valid                      | Valid |
|         | 743:742      | Reserved        |                                                                   | Valid                      | Valid |
| 5D      | 749:744      | Matrix OUT      | IN1 of 3-bit LUT8 or External Clock Input of Delay5 (or Counter5) | Valid                      | Valid |
|         | 751:750      | Reserved        |                                                                   | Valid                      | Valid |
| 5E      | 757:752      | Matrix OUT      | IN2 of 3-bit LUT8                                                 | Valid                      | Valid |
|         | 759:758      | Reserved        |                                                                   | Valid                      | Valid |
| 5F      | 765:760      | Matrix OUT      | IN0 of 3-bit LUT9 or Delay6 Input (or Counter6 RST Input)         | Valid                      | Valid |
|         | 767:766      | Reserved        |                                                                   | Valid                      | Valid |
| 60      | 773:768      | Matrix OUT      | IN1 of 3-bit LUT9 or External Clock Input of Delay6 (or Counter6) | Valid                      | Valid |
|         | 775:774      | Reserved        |                                                                   | Valid                      | Valid |
| 61      | 781:776      | Matrix OUT      | IN2 of 3-bit LUT9                                                 | Valid                      | Valid |
|         | 783:782      | Reserved        |                                                                   | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address  |              | Signal Function | Register Bit Definition                                           | I <sup>2</sup> C Interface |         |
|----------|--------------|-----------------|-------------------------------------------------------------------|----------------------------|---------|
| Byte     | Register Bit |                 |                                                                   | Read                       | Write   |
| 62       | 789:784      | Matrix OUT      | IN0 of 3-bit LUT10 or Input of Pipe Delay                         | Valid                      | Valid   |
|          | 791:790      | Reserved        |                                                                   | Valid                      | Valid   |
| 63       | 797:792      | Matrix OUT      | IN1 of 3-bit LUT10 or nRST of Pipe Delay                          | Valid                      | Valid   |
|          | 799:798      | Reserved        |                                                                   | Valid                      | Valid   |
| 64       | 805:800      | Matrix OUT      | IN2 of 3-bit LUT10 or Clock of Pipe Delay                         | Valid                      | Valid   |
|          | 807:806      | Reserved        |                                                                   | Valid                      | Valid   |
| 65       | 813:808      | Matrix OUT      | IN0 of 4-bit LUT0 or Delay0 Input (or Counter0 RST/SET Input)     | Valid                      | Valid   |
|          | 815:814      | Reserved        |                                                                   | Valid                      | Valid   |
| 66       | 821:816      | Matrix OUT      | IN1 of 4-bit LUT0 or External Clock Input of Delay0 (or Counter0) | Valid                      | Valid   |
|          | 823:822      | Reserved        |                                                                   | Valid                      | Valid   |
| 67       | 829:824      | Matrix OUT      | IN2 of 4-bit LUT0 or UP Input of FSM0                             | Valid                      | Valid   |
|          | 831:830      | Reserved        |                                                                   | Valid                      | Valid   |
| 68       | 837:832      | Matrix OUT      | IN3 of 4-bit LUT0 or KEEP Input of FSM0                           | Valid                      | Valid   |
|          | 839:838      | Reserved        |                                                                   | Valid                      | Valid   |
| 69       | 845:840      | Matrix OUT      | IN0 of 4-bit LUT1 or Delay1 Input (or Counter1 RST/SET Input)     | Valid                      | Valid   |
|          | 847:846      | Reserved        |                                                                   | Valid                      | Valid   |
| 6A       | 853:848      | Matrix OUT      | IN1 of 4-bit LUT1 or External Clock Input of Delay1 (or Counter1) | Valid                      | Valid   |
|          | 855:854      | Reserved        |                                                                   | Valid                      | Valid   |
| 6B       | 861:856      | Matrix OUT      | IN2 of 4-bit LUT1 or UP Input of FSM1                             | Valid                      | Valid   |
|          | 863:862      | Reserved        |                                                                   | Valid                      | Valid   |
| 6C       | 869:864      | Matrix OUT      | IN3 of 4-bit LUT1 or KEEP Input of FSM1                           | Valid                      | Valid   |
|          | 871:870      | Reserved        |                                                                   | Valid                      | Valid   |
| 6D       | 877:872      | Matrix OUT      | PD of Temp output with BG by registers [1269:1268]                | Valid                      | Valid   |
|          | 879:878      | Reserved        |                                                                   | Valid                      | Valid   |
| Reserved |              |                 |                                                                   |                            |         |
| 6E       | 887:880      | Reserved        |                                                                   | Invalid                    | Invalid |
| 6F       | 895:888      | Reserved        |                                                                   | Invalid                    | Invalid |
| 70       | 903:896      | Reserved        |                                                                   | Invalid                    | Invalid |
| 71       | 911:904      | Reserved        |                                                                   | Invalid                    | Invalid |
| 72       | 919:912      | Reserved        |                                                                   | Invalid                    | Invalid |
| 73       | 927:920      | Reserved        |                                                                   | Invalid                    | Invalid |
| 74       | 935:928      | Reserved        |                                                                   | Invalid                    | Invalid |
| 75       | 943:936      | Reserved        |                                                                   | Invalid                    | Invalid |

Table 38. Register Map (Cont.)

| Address    |              | Signal Function                           | Register Bit Definition                                                                                                                | I <sup>2</sup> C Interface |         |
|------------|--------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|----------------------------|---------|
| Byte       | Register Bit |                                           |                                                                                                                                        | Read                       | Write   |
| 76         | 951:944      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 77         | 959:952      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 78         | 967:960      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 79         | 975:968      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 7A         | 983:976      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 7B         | 991:984      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 7C         | 999:992      | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 7D         | 1007:1000    | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 7E         | 1015:1008    | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| 7F         | 1023:1016    | Reserved                                  |                                                                                                                                        | Invalid                    | Invalid |
| <b>IO0</b> |              |                                           |                                                                                                                                        |                            |         |
| 80         | 1024         | Reserved                                  |                                                                                                                                        | Valid                      | Valid   |
|            | 1025         | Reserved                                  |                                                                                                                                        | Valid                      | Valid   |
|            | 1027:1026    | Reserved                                  |                                                                                                                                        | Valid                      | Valid   |
|            | 1029:1028    | IO0 Pull-Down Resistor Value Selection    | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                       | Valid                      | Valid   |
|            | 1031:1030    | IO0 Mode Control                          | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved   | Valid                      | Valid   |
| <b>IO1</b> |              |                                           |                                                                                                                                        |                            |         |
| 81         | 1032         | Reserved                                  |                                                                                                                                        | Valid                      | Valid   |
|            | 1033         | IO1 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                           | Valid                      | Valid   |
|            | 1035:1034    | IO1 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                       | Valid                      | Valid   |
|            | 1037:1036    | IO1 Mode Control (sig_io1_oe = 0)         | 00: Digital Input without Schmitt Trigger,<br>01: Digital Input with Schmitt Trigger,<br>10: Low Voltage Digital Input<br>11: Reserved | Valid                      | Valid   |
|            | 1039:1038    | IO1 Mode Control (sig_io1_oe = 1)         | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                               | Valid                      | Valid   |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                           | Register Bit Definition                                                                                                                                                                                                     | I <sup>2</sup> C Interface |       |
|---------|--------------|-------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                           |                                                                                                                                                                                                                             | Read                       | Write |
| IO2     |              |                                           |                                                                                                                                                                                                                             |                            |       |
| 82      | 1040         | Reserved                                  |                                                                                                                                                                                                                             | Valid                      | Valid |
|         | 1041         | IO2 Driver Strength Selection             | 0: 1x<br>1: 2x                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1042         | IO2 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                | Valid                      | Valid |
|         | 1044:1043    | IO2 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                            | Valid                      | Valid |
|         | 1047:1045    | IO2 Mode Control                          | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push-Pull<br>101: Open-Drain NMOS<br>110: Open-Drain PMOS<br>111: Reserved | Valid                      | Valid |
| IO3     |              |                                           |                                                                                                                                                                                                                             |                            |       |
| 83      | 1048         | Reserved                                  |                                                                                                                                                                                                                             | Valid                      | Valid |
|         | 1049         | IO3 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                | Valid                      | Valid |
|         | 1051:1050    | IO3 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                            | Valid                      | Valid |
|         | 1053:1052    | IO3 Mode Control (sig_io3_oe = 0)         | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved                                                                                        | Valid                      | Valid |
|         | 1055:1054    | IO3 Mode Control (sig_io3_oe = 1)         | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                                                                                                    | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                           | Register Bit Definition                                                                                                                                                                                                                                   | I <sup>2</sup> C Interface |       |
|---------|--------------|-------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                           |                                                                                                                                                                                                                                                           | Read                       | Write |
| IO4     |              |                                           |                                                                                                                                                                                                                                                           |                            |       |
| 84      | 1056         | Reserved                                  |                                                                                                                                                                                                                                                           | Valid                      | Valid |
|         | 1057         | IO4 Driver Strength Selection             | 0: 1x<br>1: 2x                                                                                                                                                                                                                                            | Valid                      | Valid |
|         | 1058         | IO4 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1060:1059    | IO4 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                                                          | Valid                      | Valid |
|         | 1063:1061    | IO4 Mode Control                          | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push-Pull<br>101: Open-Drain NMOS<br>110: Open-Drain PMOS<br>111: Analog Input and Open-Drain | Valid                      | Valid |
| IO5     |              |                                           |                                                                                                                                                                                                                                                           |                            |       |
| 85      | 1064         | Reserved                                  |                                                                                                                                                                                                                                                           | Valid                      | Valid |
|         | 1065         | IO5 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1067:1066    | IO5 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                                                          | Valid                      | Valid |
|         | 1069:1068    | IO5 Mode Control (sig_io5_oe = 0)         | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output                                                                                                           | Valid                      | Valid |
|         | 1071:1070    | IO5 Mode Control (sig_io5_oe = 1)         | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                                                                                                                                  | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                                                                                                 | Register Bit Definition                                                                                                                                                                                             | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                                                                                                 |                                                                                                                                                                                                                     | Read                       | Write |
| IO6     |              |                                                                                                                 |                                                                                                                                                                                                                     |                            |       |
| 86      | 1072         | Reserved                                                                                                        |                                                                                                                                                                                                                     | Valid                      | Valid |
|         | 1073         | IO6 Driver Strength Selection                                                                                   | 0: 1x<br>1: 2x                                                                                                                                                                                                      | Valid                      | Valid |
|         | 1074         | Select SCL and Virtual Input 0 or IO6                                                                           | 0: SCL and Virtual Input 0<br>1: IO6                                                                                                                                                                                | Valid                      | Valid |
|         | 1076:1075    | IO6 Pull-Down Resistor Value Selection                                                                          | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                    | Valid                      | Valid |
|         | 1079:1077    | IO6 (or SCL) Mode Control<br>(input mode is selected by register at SCL)                                        | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Reserved<br>101: Open-Drain NMOS<br>110: Reserved<br>111: Reserved | Valid                      | Valid |
| IO7     |              |                                                                                                                 |                                                                                                                                                                                                                     |                            |       |
| 87      | 1080         | Reserved                                                                                                        |                                                                                                                                                                                                                     | Valid                      | Valid |
|         | 1081         | IO7 (or SDA) Driver Strength Selection                                                                          | 0: 1x<br>1: 2x                                                                                                                                                                                                      | Valid                      | Valid |
|         | 1082         | Select SDA and Virtual Input 1 or IO7                                                                           | 0: SDA and Virtual Input 1<br>1: IO7                                                                                                                                                                                | Valid                      | Valid |
|         | 1084:1083    | IO7 Pull-Down Resistor Value Selection                                                                          | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                    | Valid                      | Valid |
|         | 1087:1085    | IO7 (or SDA) Mode Control<br>(input mode is selected by register at SDA, but output mode is fixed as OD at SDA) | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Reserved<br>101: Open-Drain NMOS<br>110: Reserved<br>111: Reserved | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                                 | Register Bit Definition                                                                                                                                                                                                                                   | I <sup>2</sup> C Interface |       |
|---------|--------------|-------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                                 |                                                                                                                                                                                                                                                           | Read                       | Write |
| IO8     |              |                                                 |                                                                                                                                                                                                                                                           |                            |       |
| 88      | 1088         | IO8 Super Drive (4x, NMOS Open-Drain) Selection | 0: Super Drive OFF<br>1: Super Drive ON (if sig_io8_oe = '1' and IO8 Mode Control = '1x')                                                                                                                                                                 | Valid                      | Valid |
|         | 1089         | IO8 Pull-Up/Down Resistor Selection             | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1091:1090    | IO8 Pull-Up/Down Resistor Value Selection       | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                                                          | Valid                      | Valid |
|         | 1093:1092    | IO8 Mode Control (sig_io8_oe = 0)               | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output                                                                                                           | Valid                      | Valid |
|         | 1095:1094    | IO8 Mode Control (sig_io8_oe = 1)               | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                                                                                                                                  | Valid                      | Valid |
| IO9     |              |                                                 |                                                                                                                                                                                                                                                           |                            |       |
| 89      | 1096         | IO9 Super Drive (4x, NMOS Open-Drain) Selection | 0: Super Drive OFF<br>1: Super Drive ON (if IO9 Mode Control = '101')                                                                                                                                                                                     | Valid                      | Valid |
|         | 1097         | IO9 Driver Strength Selection                   | 0: 1x<br>1: 2x                                                                                                                                                                                                                                            | Valid                      | Valid |
|         | 1098         | IO9 Pull-Up/Down Resistor Selection             | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1100:1099    | IO9 Pull-Up/Down Resistor Value Selection       | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                                                          | Valid                      | Valid |
|         | 1103:1101    | IO9 Mode Control                                | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push-Pull<br>101: Open-Drain NMOS<br>110: Open-Drain PMOS<br>111: Analog Input and Open-Drain | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                            | Register Bit Definition                                                                                                                         | I <sup>2</sup> C Interface |       |
|---------|--------------|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                            |                                                                                                                                                 | Read                       | Write |
| IO10    |              |                                            |                                                                                                                                                 |                            |       |
| 8A      | 1104         | Reserved                                   |                                                                                                                                                 | Valid                      | Valid |
|         | 1105         | IO10 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                    | Valid                      | Valid |
|         | 1107:1106    | IO10 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                | Valid                      | Valid |
|         | 1109:1108    | IO10 Mode Control (sig_io10_oe = 0)        | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid                      | Valid |
|         | 1111:1110    | IO10 Mode Control (sig_io10_oe = 1)        | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                        | Valid                      | Valid |
| IO11    |              |                                            |                                                                                                                                                 |                            |       |
| 8B      | 1112         | Reserved                                   |                                                                                                                                                 | Valid                      | Valid |
|         | 1113         | IO11 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                    | Valid                      | Valid |
|         | 1115:1114    | IO11 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                | Valid                      | Valid |
|         | 1117:1116    | IO11 Mode Control (sig_io11_oe = 0)        | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid                      | Valid |
|         | 1119:1118    | IO11 Mode Control (sig_io11_oe = 1)        | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                        | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                            | Register Bit Definition                                                                                                                                                                                                                                   | I <sup>2</sup> C Interface |       |
|---------|--------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                            |                                                                                                                                                                                                                                                           | Read                       | Write |
| IO12    |              |                                            |                                                                                                                                                                                                                                                           |                            |       |
| 8C      | 1120         | Reserved                                   |                                                                                                                                                                                                                                                           | Valid                      | Valid |
|         | 1121         | IO12 Driver Strength Selection             | 0: 1x<br>1: 2x                                                                                                                                                                                                                                            | Valid                      | Valid |
|         | 1122         | IO12 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1124:1123    | IO12 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                                                          | Valid                      | Valid |
|         | 1127:1125    | IO12 Mode Control                          | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push-Pull<br>101: Open-Drain NMOS<br>110: Open-Drain PMOS<br>111: Analog Input and Open-Drain | Valid                      | Valid |
| IO13    |              |                                            |                                                                                                                                                                                                                                                           |                            |       |
| 8D      | 1128         | Reserved                                   |                                                                                                                                                                                                                                                           | Valid                      | Valid |
|         | 1129         | IO13 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1131:1130    | IO13 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                                                          | Valid                      | Valid |
|         | 1133:1132    | IO13 Mode Control (sig_io13_oe = 0)        | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved                                                                                                                      | Valid                      | Valid |
|         | 1135:1134    | IO13 Mode Control (sig_io13_oe = 1)        | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                                                                                                                                  | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                            | Register Bit Definition                                                                                                                                                                                                     | I <sup>2</sup> C Interface |       |
|---------|--------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                            |                                                                                                                                                                                                                             | Read                       | Write |
| IO14    |              |                                            |                                                                                                                                                                                                                             |                            |       |
| 8E      | 1136         | Reserved                                   |                                                                                                                                                                                                                             | Valid                      | Valid |
|         | 1137         | IO14 Driver Strength Selection             | 0: 1x<br>1: 2x                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1138         | IO14 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                | Valid                      | Valid |
|         | 1140:1139    | IO14 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                            | Valid                      | Valid |
|         | 1143:1141    | IO14 Mode Control                          | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push-Pull<br>101: Open-Drain NMOS<br>110: Open-Drain PMOS<br>111: Reserved | Valid                      | Valid |
| IO15    |              |                                            |                                                                                                                                                                                                                             |                            |       |
| 8F      | 1144         | Reserved                                   |                                                                                                                                                                                                                             | Valid                      | Valid |
|         | 1145         | IO15 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                | Valid                      | Valid |
|         | 1147:1146    | IO15 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                            | Valid                      | Valid |
|         | 1149:1148    | IO15 Mode Control (sig_io15_oe = 0)        | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output                                                                             | Valid                      | Valid |
|         | 1151:1150    | IO15 Mode Control (sig_io15_oe = 1)        | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                                                                                                    | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                            | Register Bit Definition                                                                                                                                                                                                     | I <sup>2</sup> C Interface |       |
|---------|--------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                            |                                                                                                                                                                                                                             | Read                       | Write |
| IO16    |              |                                            |                                                                                                                                                                                                                             |                            |       |
| 90      | 1152         | Reserved                                   |                                                                                                                                                                                                                             | Valid                      | Valid |
|         | 1153         | IO16 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                | Valid                      | Valid |
|         | 1155:1154    | IO16 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                            | Valid                      | Valid |
|         | 1157:1156    | IO16 Mode Control (sig_io16_oe = 0)        | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output                                                                             | Valid                      | Valid |
|         | 1159:1158    | IO16 Mode Control (sig_ioIO1616_oe = 1)    | 00: Push-Pull 1x<br>01: Push-Pull 2x<br>10: Open-Drain NMOS 1x<br>11: Open-Drain NMOS 2x                                                                                                                                    | Valid                      | Valid |
| IO17    |              |                                            |                                                                                                                                                                                                                             |                            |       |
| 91      | 1160         | Reserved                                   |                                                                                                                                                                                                                             | Valid                      | Valid |
|         | 1161         | IO17 Driver Strength Selection             | 0: 1x<br>1: 2x                                                                                                                                                                                                              | Valid                      | Valid |
|         | 1162         | IO17 Pull-Up/Down Resistor Selection       | 0: Pull-Down Resistor<br>1: Pull-Up Resistor                                                                                                                                                                                | Valid                      | Valid |
|         | 1164:1163    | IO17 Pull-Up/Down Resistor Value Selection | 00: Floating<br>01: 10 k<br>10: 100 k<br>11: 1 M                                                                                                                                                                            | Valid                      | Valid |
|         | 1167:1165    | IO17 Mode Control                          | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push-Pull<br>101: Open-Drain NMOS<br>110: Open-Drain PMOS<br>111: Reserved | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                            | Register Bit Definition                                                                                                                                                                                                            | I <sup>2</sup> C Interface |       |
|---------|--------------|--------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                            |                                                                                                                                                                                                                                    | Read                       | Write |
| ACMP1   |              |                                            |                                                                                                                                                                                                                                    |                            |       |
| 92      | 1168         | ACMP1 Positive Input Source Select         | 0: IO8<br>1: ACMP0 IN+ source                                                                                                                                                                                                      | Valid                      | Valid |
|         | 1169         | ACMP1 Analog Buffer Enable (Max. BW 1 MHz) | 0: Disable analog buffer<br>1: Enable analog buffer                                                                                                                                                                                | Valid                      | Valid |
|         | 1171:1170    | ACMP1 Hysteresis Enable                    | 00: 0 mV<br>01: 25 mV<br>10: 50 mV<br>11: 200 mV<br>(01: for both external and internal V <sub>REF</sub> ;<br>10 and 11: for only internal V <sub>REF</sub> ; External V <sub>REF</sub> will not have 50 mV and 200 mV hysteresis) | Valid                      | Valid |
| ACMP0   |              |                                            |                                                                                                                                                                                                                                    |                            |       |
| 92      | 1172         | ACMP0 Positive Input Source Select         | 0: IO4<br>1: V <sub>DD</sub>                                                                                                                                                                                                       | Valid                      | Valid |
|         | 1173         | ACMP0 Analog Buffer Enable (Max. BW 1 MHz) | 0: Disable analog buffer<br>1: Enable analog buffer                                                                                                                                                                                | Valid                      | Valid |
|         | 1175:1174    | ACMP0 Hysteresis Enable                    | 00: 0 mV<br>01: 25 mV<br>10: 50 mV<br>11: 200 mV<br>(01: for both external and internal V <sub>REF</sub> ;<br>10 and 11: for only internal V <sub>REF</sub> ; External V <sub>REF</sub> will not have 50 mV and 200 mV hysteresis) | Valid                      | Valid |
| ACMP3   |              |                                            |                                                                                                                                                                                                                                    |                            |       |
| 93      | 1177:1176    | ACMP3 Positive Input Source Select         | 00: IO12<br>01: ACMP2 IN+ source<br>10: ACMP0 IN+ source<br>11: Reserved                                                                                                                                                           | Valid                      | Valid |
|         | 1179:1178    | ACMP3 Hysteresis Enable                    | 00: 0 mV<br>01: 25 mV<br>10: 50 mV<br>11: 200 mV<br>(01: for both external and internal V <sub>REF</sub> ;<br>10 and 11: for only internal V <sub>REF</sub> ; External V <sub>REF</sub> will not have 50 mV and 200 mV hysteresis) | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address                            |              | Signal Function                          | Register Bit Definition                                                                                                                                                                                                            | I <sup>2</sup> C Interface |       |
|------------------------------------|--------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte                               | Register Bit |                                          |                                                                                                                                                                                                                                    | Read                       | Write |
| ACMP2                              |              |                                          |                                                                                                                                                                                                                                    |                            |       |
| 93                                 | 1180         | ACMP2 Positive Input Source Select       | 0: IO10<br>1: ACMP0 IN+ source                                                                                                                                                                                                     | Valid                      | Valid |
|                                    | 1182:1181    | ACMP2 Hysteresis Enable                  | 00: 0 mV<br>01: 25 mV<br>10: 50 mV<br>11: 200 mV<br>(01: for both external and internal V <sub>REF</sub> ;<br>10 and 11: for only internal V <sub>REF</sub> ; External V <sub>REF</sub> will not have 50 mV and 200 mV hysteresis) | Valid                      | Valid |
| ACMP1 100 μA Current Source Enable |              |                                          |                                                                                                                                                                                                                                    |                            |       |
| 93                                 | 1183         | ACMP1 100 μA Current Source Enable       | 0: Disable<br>1: Enable                                                                                                                                                                                                            | Valid                      | Valid |
| 3-bit LUTx Function Select         |              |                                          |                                                                                                                                                                                                                                    |                            |       |
| 94                                 | 1184         | 3-bit LUT3 or DFF6 with nRST/nSET Select | 0: 3-bit LUT3<br>1: DFF6 with nRST/nSET                                                                                                                                                                                            | Valid                      | Valid |
|                                    | 1185         | 3-bit LUT2 or DFF5 with nRST/nSET Select | 0: 3-bit LUT2<br>1: DFF5 with nRST/nSET                                                                                                                                                                                            | Valid                      | Valid |
|                                    | 1186         | 3-bit LUT1 or DFF4 with nRST/nSET Select | 0: 3-bit LUT1<br>1: DFF4 with nRST/nSET                                                                                                                                                                                            | Valid                      | Valid |
|                                    | 1187         | 3-bit LUT0 or DFF3 with nRST/nSET Select | 0: 3-bit LUT0<br>1: DFF3 with nRST/nSET                                                                                                                                                                                            | Valid                      | Valid |
| 2-bit LUTx Function Select         |              |                                          |                                                                                                                                                                                                                                    |                            |       |
| 94                                 | 1188         | 2-bit LUT3 or PGen Select                | 0: 2-bit LUT3<br>1: PGen                                                                                                                                                                                                           | Valid                      | Valid |
|                                    | 1189         | 2-bit LUT2 or DFF2 Select                | 0: 2-bit LUT2<br>1: DFF2                                                                                                                                                                                                           | Valid                      | Valid |
|                                    | 1190         | 2-bit LUT1 or DFF1 Select                | 0: 2-bit LUT1<br>1: DFF1                                                                                                                                                                                                           | Valid                      | Valid |
|                                    | 1191         | 2-bit LUT0 or DFF0 Select                | 0: 2-bit LUT0<br>1: DFF0                                                                                                                                                                                                           | Valid                      | Valid |
| 4-bit LUTx Function Select         |              |                                          |                                                                                                                                                                                                                                    |                            |       |
| 95                                 | 1192         | 4-bit LUT1 or DLY/CNT1(16bits) Select    | 0: 4-bit LUT1<br>1: DLY/CNT1(16bits)                                                                                                                                                                                               | Valid                      | Valid |
|                                    | 1193         | 4-bit LUT0 or DLY/CNT0(16bits) Select    | 0: 4-bit LUT0<br>1: DLY/CNT0(16bits)                                                                                                                                                                                               | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address                    |              | Signal Function                                  | Register Bit Definition                 | I <sup>2</sup> C Interface |       |
|----------------------------|--------------|--------------------------------------------------|-----------------------------------------|----------------------------|-------|
| Byte                       | Register Bit |                                                  |                                         | Read                       | Write |
| 3-bit LUTx Function Select |              |                                                  |                                         |                            |       |
| 95                         | 1194         | 3-bit LUT9 or DLY/CNT6(8bits) Select             | 0: 3-bit LUT9<br>1: DLY/CNT6(8bits)     | Valid                      | Valid |
|                            | 1195         | 3-bit LUT8 or DLY/CNT5(8bits) Select             | 0: 3-bit LUT8<br>1: DLY/CNT5(8bits)     | Valid                      | Valid |
|                            | 1196         | 3-bit LUT7 or DLY/CNT4(8bits) Select             | 0: 3-bit LUT7<br>1: DLY/CNT4(8bits)     | Valid                      | Valid |
|                            | 1197         | 3-bit LUT6 or DLY/CNT3(8bits) Select             | 0: 3-bit LUT6<br>1: DLY/CNT3(8bits)     | Valid                      | Valid |
|                            | 1198         | 3-bit LUT5 or DLY/CNT2(8bits) Select             | 0: 3-bit LUT5<br>1: DLY/CNT2(8bits)     | Valid                      | Valid |
|                            | 1199         | 3-bit LUT4 or DFF7 with nRST/nSET Select         | 0: 3-bit LUT4<br>1: DFF7 with nRST/nSET | Valid                      | Valid |
| 2-bit LUT1/DFF1            |              |                                                  |                                         |                            |       |
| 96                         | 1200         | 2-bit LUT1 [0]                                   |                                         | Valid                      | Valid |
|                            | 1201         | 2-bit LUT1 [1]/DFF1 Initial Polarity Select      | 0: Low<br>1: High                       | Valid                      | Valid |
|                            | 1202         | 2-bit LUT1 [2]/DFF1 Output Select                | 0: Q output<br>1: nQ output             | Valid                      | Valid |
|                            | 1203         | 2-bit LUT1 [3]/DFF1 or LATCH Select              | 0: DFF function<br>1: LATCH function    | Valid                      | Valid |
| 2-bit LUT0/DFF0            |              |                                                  |                                         |                            |       |
| 96                         | 1204         | 2-bit LUT0 [0]                                   |                                         | Valid                      | Valid |
|                            | 1205         | 2-bit LUT0 [1]/DFF0 Initial Polarity Select      | 0: Low<br>1: High                       | Valid                      | Valid |
|                            | 1206         | 2-bit LUT0 [2]/DFF0 Output Select                | 0: Q output<br>1: nQ output             | Valid                      | Valid |
|                            | 1207         | 2-bit LUT0 [3]/DFF0 or LATCH Select              | 0: DFF function<br>1: LATCH function    | Valid                      | Valid |
| 2-bit LUT3/PGen            |              |                                                  |                                         |                            |       |
| 97                         | 1211:1208    | 2-bit LUT3 [3:0] or PGen 4bit counter data [3:0] |                                         | Valid                      | Valid |
| 2-bit LUT2/DFF2            |              |                                                  |                                         |                            |       |
| 97                         | 1212         | 2-bit LUT2 [0]                                   |                                         | Valid                      | Valid |
|                            | 1213         | 2-bit LUT2 [1]/DFF2 Initial Polarity Select      | 0: Low<br>1: High                       | Valid                      | Valid |
|                            | 1214         | 2-bit LUT2 [2]/DFF2 Output Select                | 0: Q output<br>1: nQ output             | Valid                      | Valid |
|                            | 1215         | 2-bit LUT2 [3]/DFF2 or LATCH Select              | 0: DFF function<br>1: LATCH function    | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address         |              | Signal Function                             | Register Bit Definition                                  | I <sup>2</sup> C Interface |       |
|-----------------|--------------|---------------------------------------------|----------------------------------------------------------|----------------------------|-------|
| Byte            | Register Bit |                                             |                                                          | Read                       | Write |
| 3-bit LUT0/DFF3 |              |                                             |                                                          |                            |       |
| 98              | 1219:1216    | 3-bit LUT0 [3:0]                            |                                                          | Valid                      | Valid |
|                 | 1220         | 3-bit LUT0 [4]/DFF3 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|                 | 1221         | 3-bit LUT0 [5]/DFF3 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|                 | 1222         | 3-bit LUT0 [6]/DFF3 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|                 | 1223         | 3-bit LUT0 [7]/DFF3 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| 3-bit LUT1/DFF4 |              |                                             |                                                          |                            |       |
| 99              | 1227:1224    | 3-bit LUT1 [3:0]                            |                                                          | Valid                      | Valid |
|                 | 1228         | 3-bit LUT1 [4]/DFF4 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|                 | 1229         | 3-bit LUT1 [5]/DFF4 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|                 | 1230         | 3-bit LUT1 [6]/DFF4 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|                 | 1231         | 3-bit LUT1 [7]/DFF4 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| 3-bit LUT2/DFF5 |              |                                             |                                                          |                            |       |
| 9A              | 1235:1232    | 3-bit LUT2 [3:0]                            |                                                          | Valid                      | Valid |
|                 | 1236         | 3-bit LUT2 [4]/DFF5 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|                 | 1237         | 3-bit LUT2 [5]/DFF5 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|                 | 1238         | 3-bit LUT2 [6]/DFF5 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|                 | 1239         | 3-bit LUT2 [7]/DFF5 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| 3-bit LUT3/DFF6 |              |                                             |                                                          |                            |       |
| 9B              | 1243:1240    | 3-bit LUT3 [3:0]                            |                                                          | Valid                      | Valid |
|                 | 1244         | 3-bit LUT3 [4]/DFF6 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|                 | 1245         | 3-bit LUT3 [5]/DFF6 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|                 | 1246         | 3-bit LUT3 [6]/DFF6 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|                 | 1247         | 3-bit LUT3 [7]/DFF6 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address                |              | Signal Function                                                                                | Register Bit Definition                                                                                | I <sup>2</sup> C Interface |       |
|------------------------|--------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte                   | Register Bit |                                                                                                |                                                                                                        | Read                       | Write |
| 3-bit LUT4/DFF7        |              |                                                                                                |                                                                                                        |                            |       |
| 9C                     | 1251:1248    | 3-bit LUT4 [3:0]                                                                               |                                                                                                        | Valid                      | Valid |
|                        | 1252         | 3-bit LUT4 [4]/DFF7 Initial Polarity Select                                                    | 0: Low<br>1: High                                                                                      | Valid                      | Valid |
|                        | 1253         | 3-bit LUT4 [5]/DFF7 nRST or nSET Select                                                        | 0: nRST from Matrix Output<br>1: nSET from Matrix Output                                               | Valid                      | Valid |
|                        | 1254         | 3-bit LUT4 [6]/DFF7 Output Select                                                              | 0: Q output<br>1: nQ output                                                                            | Valid                      | Valid |
|                        | 1255         | 3-bit LUT4 [7]/DFF7 or LATCH Select                                                            | 0: DFF function<br>1: LATCH function                                                                   | Valid                      | Valid |
| 3-bit LUT10/Pipe Delay |              |                                                                                                |                                                                                                        |                            |       |
| 9D                     | 1259:1256    | 3-bit LUT10 [3:0]/Pipe Delay OUT0 Select                                                       |                                                                                                        | Valid                      | Valid |
|                        | 1263:1260    | 3-bit LUT10 [7:4]/Pipe Delay OUT1 Select                                                       |                                                                                                        | Valid                      | Valid |
| 9E                     | 1265:1264    | Select the Edge Mode of Programmable Delay and Edge Detector                                   | 00: Rising Edge Detector<br>01: Falling Edge Detector<br>10: Both Edge Detector<br>11: Both Edge Delay | Valid                      | Valid |
|                        | 1267:1266    | Delay Value Select for Programmable Delay and Edge Detector (V <sub>DD</sub> = 3.3 V, typical) | 00: 135 ns<br>01: 270 ns<br>10: 405 ns<br>11: 540 ns                                                   | Valid                      | Valid |
|                        | 1269:1268    | Temp output Power-down enable                                                                  | 00: No matrix PD<br>01: Reserved<br>10: Matrix PD for temp sensor<br>11: Matrix PD for temp sensor     | Valid                      | Valid |
|                        | 1270         | 3-bit LUT10 or Pipe Delay Select                                                               | 0: 3-bit LUT10<br>1: Pipe Delay                                                                        | Valid                      | Valid |
|                        | 1271         | Pipe Delay OUT1 Polarity Select                                                                | 0: Non-inverted<br>1: Inverted                                                                         | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address  |              | Signal Function                                              | Register Bit Definition                                                                                                                                                                                                                                  | I <sup>2</sup> C Interface |       |
|----------|--------------|--------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte     | Register Bit |                                                              |                                                                                                                                                                                                                                                          | Read                       | Write |
| DLY/CNT2 |              |                                                              |                                                                                                                                                                                                                                                          |                            |       |
| 9F       | 1273:1272    | DLY2 Mode Select or Asynchronous CNT2 Reset                  | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|          | 1276:1274    | DLY/CNT2 Clock Source Select                                 | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter1 Overflow                                                                                             | Valid                      | Valid |
|          | 1277         | DLY/CNT2 Output Selection if DLY/CNT2 Mode Selection is "11" | 0: Default Output<br>1: Edge Detector Output                                                                                                                                                                                                             | Valid                      | Valid |
|          | 1279:1278    | DLY/CNT2 Mode Selection                                      | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |
| DLY/CNT3 |              |                                                              |                                                                                                                                                                                                                                                          |                            |       |
| A0       | 1281:1280    | DLY3 Mode Select or Asynchronous CNT3 Reset                  | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|          | 1284:1282    | DLY/CNT3 Clock Source Select                                 | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter2 Overflow                                                                                             | Valid                      | Valid |
|          | 1285         | DLY/CNT3 Output Selection if DLY/CNT3 Mode Selection is "11" | 0: Default Output<br>1: Edge Detector Output                                                                                                                                                                                                             | Valid                      | Valid |
|          | 1287:1286    | DLY/CNT3 Mode Selection                                      | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address  |              | Signal Function                                              | Register Bit Definition                                                                                                                                                                                                                                  | I <sup>2</sup> C Interface |       |
|----------|--------------|--------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte     | Register Bit |                                                              |                                                                                                                                                                                                                                                          | Read                       | Write |
| DLY/CNT4 |              |                                                              |                                                                                                                                                                                                                                                          |                            |       |
| A1       | 1289:1288    | DLY4 Mode Select or Asynchronous CNT4 Reset                  | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|          | 1292:1290    | DLY/CNT4 Clock Source Select                                 | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter3 Overflow                                                                                             | Valid                      | Valid |
|          | 1293         | DLY/CNT4 Output Selection if DLY/CNT4 Mode Selection is "11" | 0: Default Output<br>1: Edge Detector Output                                                                                                                                                                                                             | Valid                      | Valid |
|          | 1295:1294    | DLY/CNT4 Mode Selection                                      | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |
| DLY/CNT5 |              |                                                              |                                                                                                                                                                                                                                                          |                            |       |
| A2       | 1297:1296    | DLY5 Mode Select or Asynchronous CNT5 Reset                  | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|          | 1300:1298    | DLY/CNT5 Clock Source Select                                 | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter4 Overflow                                                                                             | Valid                      | Valid |
|          | 1301         | DLY/CNT5 Output Selection if DLY/CNT5 Mode Selection is "11" | 0: Default Output<br>1: Edge Detector Output                                                                                                                                                                                                             | Valid                      | Valid |
|          | 1303:1302    | DLY/CNT5 Mode Selection                                      | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address  |              | Signal Function                                                 | Register Bit Definition                                                                                                                                                                                                                                  | I <sup>2</sup> C Interface |       |
|----------|--------------|-----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte     | Register Bit |                                                                 |                                                                                                                                                                                                                                                          | Read                       | Write |
| DLY/CNT6 |              |                                                                 |                                                                                                                                                                                                                                                          |                            |       |
| A3       | 1305:1304    | DLY6 Mode Select or Asynchronous CNT6 Reset                     | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|          | 1308:1306    | DLY/CNT6 Clock Source Select                                    | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter5 Overflow                                                                                             | Valid                      | Valid |
|          | 1309         | DLY/CNT6 Output Selection if DLY/CNT6 Mode Selection is "11".   | 0: Default Output<br>1: Edge Detector Output                                                                                                                                                                                                             | Valid                      | Valid |
|          | 1311:1310    | DLY/CNT6 Mode Selection                                         | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |
| DLY/CNT0 |              |                                                                 |                                                                                                                                                                                                                                                          |                            |       |
| A4       | 1313:1312    | DLY0 Mode Select or Asynchronous CNT0 Reset (16bits)            | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|          | 1316:1314    | DLY/CNT0 Clock Source Select (16bits)                           | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter6 Overflow                                                                                             | Valid                      | Valid |
|          | 1317         | CNT0/FSM0's Q are Set to data or Reset to 0s Selection (16bits) | 0: Reset to 0 s<br>1: Set to data (Registers [1583:1576, 1591:1584])                                                                                                                                                                                     | Valid                      | Valid |
|          | 1319:1318    | DLY/CNT0 Mode Selection (16bits)                                | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address                                        |              | Signal Function                                                         | Register Bit Definition                                                                                                                                                                                                                                  | I <sup>2</sup> C Interface |       |
|------------------------------------------------|--------------|-------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte                                           | Register Bit |                                                                         |                                                                                                                                                                                                                                                          | Read                       | Write |
| DLY/CNT1                                       |              |                                                                         |                                                                                                                                                                                                                                                          |                            |       |
| A5                                             | 1321:1320    | DLY1 Mode Select or Asynchronous CNT1 Reset (16bits)                    | 00: On both Falling and Rising Edges (for Delay and Counter Reset)<br>01: on Falling Edge only (for Delay and Counter Reset)<br>10: on Rising Edge only (for Delay and Counter Reset)<br>11: No Delay on either Falling or Rising Edges/High Level Reset | Valid                      | Valid |
|                                                | 1324:1322    | DLY/CNT1 Clock Source Select (16bits)                                   | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter0 Overflow                                                                                             | Valid                      | Valid |
|                                                | 1325         | CNT1/FSM1's Q are Set to data or Reset to 0s Selection (16bits)         | 0: Reset to 0 s<br>1: Set to data (Registers [1599:1592, 1607:1600])                                                                                                                                                                                     | Valid                      | Valid |
|                                                | 1327:1326    | DLY/CNT1 Mode Selection (16bits)                                        | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode                                                                                                                                                                                   | Valid                      | Valid |
| DLY/CNTx One-Shot/Freq. Detect Output Polarity |              |                                                                         |                                                                                                                                                                                                                                                          |                            |       |
| A6                                             | 1328         | DLY/CNT0 stop and restarting enable in CNT mode when new data is loaded | 0: Disable<br>1: Enable                                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1329         | Select the Polarity of DLY/CNT6's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1330         | Select the Polarity of DLY/CNT5's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1331         | Select the Polarity of DLY/CNT4's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1332         | Select the Polarity of DLY/CNT3's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1333         | Select the Polarity of DLY/CNT2's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1334         | Select the Polarity of DLY/CNT1's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |
|                                                | 1335         | Select the Polarity of DLY/CNT0's One Shot/Freq. Detect Output          | 0: Default Output<br>1: Inverted Output                                                                                                                                                                                                                  | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address    |              | Signal Function                                                           | Register Bit Definition                                                                                         | I <sup>2</sup> C Interface |       |
|------------|--------------|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte       | Register Bit |                                                                           |                                                                                                                 | Read                       | Write |
| Oscillator |              |                                                                           |                                                                                                                 |                            |       |
| A7         | 1337:1336    | OSC Clock Pre-divider for 25 MHz                                          | 00: Div1<br>01: Div2<br>10: Div4<br>11: Div8                                                                    | Valid                      | Valid |
|            | 1338         | OSC Fast Start-Up Enable for 25 kHz/2 MHz                                 | 0: Disable<br>1: Enable                                                                                         | Valid                      | Valid |
|            | 1340:1339    | OSC Clock Pre-divider for 25 kHz/2 MHz                                    | 00: Div1<br>01: Div2<br>10: Div4<br>11: Div8                                                                    | Valid                      | Valid |
|            | 1341         | Force 25 MHz Oscillator ON                                                | 0: Auto Power-On (if any CNT/DLY use 25 MHz source)<br>1: Force Power-On                                        | Valid                      | Valid |
|            | 1342         | Oscillator (25 kHz/2 MHz OSC) Select                                      | 0: 25 kHz OSC<br>1: 2 MHz OSC                                                                                   | Valid                      | Valid |
|            | 1343         | Force 25 kHz/2 MHz Oscillator ON                                          | 0: Auto Power-On (if any CNT/DLY use 25 kHz/2 MHz source)<br>1: Force Power-On                                  | Valid                      | Valid |
| A8         | 1346:1344    | Internal OSC 25 kHz/2 MHz Frequency Divider Control for matrix input [28] | 000: OSC/1<br>001: OSC/2<br>010: OSC/3<br>011: OSC/4<br>100: OSC/8<br>101: OSC/12<br>110: OSC/24<br>111: OSC/64 | Valid                      | Valid |
|            | 1349:1347    | Internal OSC 25 kHz/2 MHz Frequency Divider Control for matrix input [27] | 000: OSC/1<br>001: OSC/2<br>010: OSC/3<br>011: OSC/4<br>100: OSC/8<br>101: OSC/12<br>110: OSC/24<br>111: OSC/64 | Valid                      | Valid |
|            | 1350         | OSC Clock 25 kHz/2 MHz to matrix input [28] enable                        | 0: Disable<br>1: Enable                                                                                         | Valid                      | Valid |
|            | 1351         | OSC Clock 25 kHz/2 MHz to matrix input [27] enable                        | 0: Disable<br>1: Enable                                                                                         | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address     |              | Signal Function                                                          | Register Bit Definition                                       | I <sup>2</sup> C Interface |       |
|-------------|--------------|--------------------------------------------------------------------------|---------------------------------------------------------------|----------------------------|-------|
| Byte        | Register Bit |                                                                          |                                                               | Read                       | Write |
| A9          | 1354:1352    | Reserved                                                                 |                                                               | Valid                      | Valid |
|             | 1355         | External oscillator pin selection for 25 kHz/2 MHz                       | 0: IO17<br>1: IO15                                            | Valid                      | Valid |
|             | 1356         | OSC Clock 25 MHz to matrix input [29] enable                             | 0: Disable<br>1: Enable                                       | Valid                      | Valid |
|             | 1357         | External Clock Source Select instead of 25 MHz                           | 0: Internal Oscillator<br>1: External Clock from IO14         | Valid                      | Valid |
|             | 1358         | External Clock Source Select instead of 25 kHz/2 MHz                     | 0: Internal Oscillator<br>1: External Clock from IO15 or IO17 | Valid                      | Valid |
|             | 1359         | DLY/CNT1 stop and restarting enable in CNT mode when new data is loaded. | 0: Disable<br>1: Enable                                       | Valid                      | Valid |
| LUT3 or DFF |              |                                                                          |                                                               |                            |       |
| AA          | 1360         | Reserved                                                                 |                                                               | Valid                      | Valid |
|             | 1361         | 3-bit LUT17 or DFF14 with nRST/nSET Select                               | 0: 3-bit LUT17<br>1: DFF14 with nRST/nSET                     | Valid                      | Valid |
|             | 1362         | 3-bit LUT16 or DFF13 with nRST/nSET Select                               | 0: 3-bit LUT16<br>1: DFF13 with nRST/nSET                     | Valid                      | Valid |
|             | 1363         | 3-bit LUT15 or DFF12 with nRST/nSET Select                               | 0: 3-bit LUT15<br>1: DFF12 with nRST/nSET                     | Valid                      | Valid |
|             | 1364         | 3-bit LUT14 or DFF11 with nRST/nSET Select                               | 0: 3-bit LUT14<br>1: DFF11 with nRST/nSET                     | Valid                      | Valid |
|             | 1365         | 3-bit LUT13 or DFF10 with nRST/nSET Select                               | 0: 3-bit LUT13<br>1: DFF10 with nRST/nSET                     | Valid                      | Valid |
|             | 1366         | 3-bit LUT12 or DFF9 with nRST/nSET Select                                | 0: 3-bit LUT12<br>1: DFF9 with nRST/nSET                      | Valid                      | Valid |
|             | 1367         | 3-bit LUT11 or DFF8 with nRST/nSET Select                                | 0: 3-bit LUT11<br>1: DFF8 with nRST/nSET                      | Valid                      | Valid |
| AB          | 1371:1368    | 3-bit LUT11 [3:0]                                                        |                                                               | Valid                      | Valid |
|             | 1372         | 3-bit LUT11 [4]/DFF8 Initial Polarity Select                             | 0: Low<br>1: High                                             | Valid                      | Valid |
|             | 1373         | 3-bit LUT11 [5]/DFF8 nRST or nSET Select                                 | 0: nRST from Matrix Output<br>1: nSET from Matrix Output      | Valid                      | Valid |
|             | 1374         | 3-bit LUT11 [6]/DFF8 Output Select                                       | 0: Q output<br>1: nQ output                                   | Valid                      | Valid |
|             | 1375         | 3-bit LUT11 [7]/DFF8 or LATCH Select                                     | 0: DFF function<br>1: LATCH function                          | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                               | Register Bit Definition                                  | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------------------------------------|----------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                               |                                                          | Read                       | Write |
| AC      | 1379:1376    | 3-bit LUT12 [3:0]                             |                                                          | Valid                      | Valid |
|         | 1380         | 3-bit LUT12 [4]/DFF9 Initial Polarity Select  | 0: Low<br>1: High                                        | Valid                      | Valid |
|         | 1381         | 3-bit LUT12 [5]/DFF9 nRST or nSET Select      | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|         | 1382         | 3-bit LUT12 [6]/DFF9 Output Select            | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|         | 1383         | 3-bit LUT12 [7]/DFF9 or LATCH Select          | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| AD      | 1387:1384    | 3-bit LUT13 [3:0]                             |                                                          | Valid                      | Valid |
|         | 1388         | 3-bit LUT13 [4]/DFF10 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|         | 1389         | 3-bit LUT13 [5]/DFF10 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|         | 1390         | 3-bit LUT13 [6]/DFF10 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|         | 1391         | 3-bit LUT13 [7]/DFF10 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| AE      | 1395:1392    | 3-bit LUT14 [3:0]                             |                                                          | Valid                      | Valid |
|         | 1396         | 3-bit LUT14 [4]/DFF11 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|         | 1397         | 3-bit LUT14 [5]/DFF11 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|         | 1398         | 3-bit LUT14 [6]/DFF11 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|         | 1399         | 3-bit LUT14 [7]/DFF11 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| AF      | 1403:1400    | 3-bit LUT15 [3:0]                             |                                                          | Valid                      | Valid |
|         | 1404         | 3-bit LUT15 [4]/DFF12 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|         | 1405         | 3-bit LUT15 [5]/DFF12 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|         | 1406         | 3-bit LUT15 [6]/DFF12 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|         | 1407         | 3-bit LUT15 [7]/DFF12 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                               | Register Bit Definition                                  | I <sup>2</sup> C Interface |       |
|---------|--------------|-----------------------------------------------|----------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                               |                                                          | Read                       | Write |
| B0      | 1411:1408    | 3-bit LUT16 [3:0]                             |                                                          | Valid                      | Valid |
|         | 1412         | 3-bit LUT16 [4]/DFF13 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|         | 1413         | 3-bit LUT16 [5]/DFF13 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|         | 1414         | 3-bit LUT16 [6]/DFF13 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|         | 1415         | 3-bit LUT16 [7]/DFF13 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| B1      | 1419:1416    | 3-bit LUT17 [3:0]                             |                                                          | Valid                      | Valid |
|         | 1420         | 3-bit LUT17 [4]/DFF14 Initial Polarity Select | 0: Low<br>1: High                                        | Valid                      | Valid |
|         | 1421         | 3-bit LUT17 [5]/DFF14 nRST or nSET Select     | 0: nRST from Matrix Output<br>1: nSET from Matrix Output | Valid                      | Valid |
|         | 1422         | 3-bit LUT17 [6]/DFF14 Output Select           | 0: Q output<br>1: nQ output                              | Valid                      | Valid |
|         | 1423         | 3-bit LUT17 [7]/DFF14 or LATCH Select         | 0: DFF function<br>1: LATCH function                     | Valid                      | Valid |
| B2      | 1431:1424    | 4-bit LUT2 [15:0] = [1439:1424]               |                                                          | Valid                      | Valid |
| B3      | 1439:1432    |                                               |                                                          | Valid                      | Valid |
| B4      | 1442:1440    | Reserved                                      |                                                          | Valid                      | Valid |
|         | 1443         | Reserved                                      |                                                          | Valid                      | Valid |
|         | 1446:1444    | Reserved                                      |                                                          | Valid                      | Valid |
|         | 1447         | Reserved                                      |                                                          | Valid                      | Valid |
| B5      | 1450:1448    | Reserved                                      |                                                          | Valid                      | Valid |
|         | 1451         | Reserved                                      |                                                          | Valid                      | Valid |
|         | 1454:1452    | Reserved                                      |                                                          | Valid                      | Valid |
|         | 1455         | Reserved                                      |                                                          | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address                   |              | Signal Function                                                                        | Register Bit Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | I <sup>2</sup> C Interface |       |
|---------------------------|--------------|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte                      | Register Bit |                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Read                       | Write |
| Filter/Edge Detector      |              |                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                            |       |
| B6                        | 1457:1456    | Select the edge mode of Edge Detector_1                                                | 00: Rising Edge<br>01: Falling Edge<br>10: Both Edge<br>11: Delay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Valid                      | Valid |
|                           | 1458         | Filter_1/Edge Detector_1 output Polarity Select                                        | 0: Filter_1 output<br>1: Filter_1 output inverted                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Valid                      | Valid |
|                           | 1459         | Filter_1or Edge Detector_1 Select (Typ. 30 ns at V <sub>DD</sub> = 3.3 V)              | 0: Filter_1<br>1: Edge Detector_1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Valid                      | Valid |
|                           | 1461:1460    | Select the edge mode of Edge Detector_0                                                | 00: Rising Edge<br>01: Falling Edge<br>10: Both Edge<br>11: Delay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Valid                      | Valid |
|                           | 1462         | Filter_0/Edge Detector_0 output Polarity Select                                        | 0: Filter_0 output<br>1: Filter_0 output inverted                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Valid                      | Valid |
|                           | 1463         | Filter_0 or Edge Detector_0 Select (Typ. 47 ns at V <sub>DD</sub> = 3.3 V)             | 0: Filter_0<br>1: Edge Detector_0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Valid                      | Valid |
| V <sub>REF</sub> /Bandgap |              |                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                            |       |
| B7                        | 1464         | Enable temp. sensor                                                                    | 0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Valid                      | Valid |
|                           | 1466:1465    | Bandgap OK for ACMP Output Delay Time Select, the start Time is "nRST_core go to High" | 00 or 10 with registers [1474:1472] = 100 (Wide V <sub>DD</sub> range, 1.7 V ~ 5.5 V):<br>Auto-delay mode, 550 μs for V <sub>DD</sub> < 2.7 V and 100 μs for 2.7 V < V <sub>DD</sub><br>00 or 10 with registers [1474:1472] = X10:<br>Always 100 μs delay for 2.7 V < V <sub>DD</sub><br>00 or 10 with registers [1474:1472] = XX1:<br>Always 550 μs delay for V <sub>DD</sub> < 2.7 V,<br>01: Always 550 μs delay regardless of registers [1474:1472] and V <sub>DD</sub> ,<br>11: Always 100 μs delay with 2.7 V < V <sub>DD</sub> regardless of registers [1474:1472] | Valid                      | Valid |
|                           | 1467         | Reserved                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Valid                      | Valid |
|                           | 1468         | Reserved                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Valid                      | Valid |
|                           | 1469         | Reserved                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Valid                      | Valid |
|                           | 1470         | Reserved                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Valid                      | Valid |
|                           | 1471         | Two consecutive DFFs enable for SM                                                     | 0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                                             | Register Bit Definition                                                                                                                       | I <sup>2</sup> C Interface |       |
|---------|--------------|-------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Byte    | Register Bit |                                                             |                                                                                                                                               | Read                       | Write |
| B8      | 1474:1472    | Power divider ( $V_{DD}/3$ , $V_{DD}/4$ ) ON/OFF            | 0XX: Power divider off (if there is no use of $V_{DD}/3$ , $V_{DD}/4$ at ACMP negative in)<br>100: Reserved<br>X10: Reserved<br>XX1: Reserved | Valid                      | Valid |
|         | 1475         | $V_{DD}$ Bypass Enable when device power is 1.8 V           | 0: Regulator Auto ON<br>1: Regulator OFF ( $V_{DD}$ Bypass)                                                                                   | Valid                      | Valid |
|         | 1476         | Force Bandgap ON                                            | 0: Auto-Mode<br>1: Enable (if chip is Power-Down, the Bandgap will Power-Down even if it is Set to 1)                                         | Valid                      | Valid |
|         | 1477         | NVM Power-Down                                              | 0: None (or Programming Enable)<br>1: Power Down (or Programming Disable)                                                                     | Valid                      | Valid |
|         | 1478         | Temp output range control (temp. detector is not available) | 0: 0.62 V ~ 0.99 V (typ)<br>1: 0.75 V ~ 1.2 V (typ)                                                                                           | Valid                      | Valid |
|         | 1479         | GPIO Quick Charge Enable                                    | 0: Disable<br>1: Enable                                                                                                                       | Valid                      | Valid |
| B9      | 1482:1480    | $V_{REF1}$ Output Source Select                             | 000: ACMP2 $V_{REF}$<br>001: ACMP3 $V_{REF}$<br>100: $V_{DD}/2$<br>101: $V_{DD}/3$<br>110: $V_{DD}/4$<br>111: Hi-Z                            | Valid                      | Valid |
|         | 1483         | Reserved                                                    |                                                                                                                                               | Valid                      | Valid |
|         | 1486:1484    | $V_{REF0}$ Output Source Select                             | 000: ACMP0 $V_{REF}$<br>001: ACMP1 $V_{REF}$<br>100: $V_{DD}/2$<br>101: $V_{DD}/3$<br>110: $V_{DD}/4$<br>111: Hi-Z                            | Valid                      | Valid |
|         | 1487         | Reserved                                                    |                                                                                                                                               | Valid                      | Valid |

Table 38. Register Map (Cont.)

| Address                  |              | Signal Function                                                                                                       | Register Bit Definition                                  | I <sup>2</sup> C Interface |         |
|--------------------------|--------------|-----------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|----------------------------|---------|
| Byte                     | Register Bit |                                                                                                                       |                                                          | Read                       | Write   |
| BA                       | 1488         | Reserved                                                                                                              |                                                          | Valid                      | Valid   |
|                          | 1489         | Wake time Selection in Wake Sleep Mode                                                                                | 0: Short wake time<br>1: Normal wake time                | Valid                      | Valid   |
|                          | 1490         | ACMP0 Wake and Sleep function Enable                                                                                  | 0: Disable<br>1: Enable                                  | Valid                      | Valid   |
|                          | 1491         | ACMP1 Wake and Sleep function Enable                                                                                  | 0: Disable<br>1: Enable                                  | Valid                      | Valid   |
|                          | 1492         | ACMP2 Wake and Sleep function Enable                                                                                  | 0: Disable<br>1: Enable                                  | Valid                      | Valid   |
|                          | 1493         | ACMP3 Wake and Sleep function Enable                                                                                  | 0: Disable<br>1: Enable                                  | Valid                      | Valid   |
|                          | 1494         | Wake Sleep Output State When WS Oscillator is OFF or DLY/CNT0 high level set/reset at DLY/CNT0 Mode Selection is "11" | 0: Low<br>1: High                                        | Valid                      | Valid   |
|                          | 1495         | Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11"                                            | 0: Default Mode<br>1: Wake Sleep Ratio Control Mode      | Valid                      | Valid   |
| BB                       | 1503:1496    | Reserved                                                                                                              |                                                          | Invalid                    | Invalid |
| BC                       | 1511:1504    | Reserved                                                                                                              |                                                          | Invalid                    | Invalid |
| BD                       | 1519:1512    | Reserved                                                                                                              |                                                          | Invalid                    | Invalid |
| BE                       | 1527:1520    | Reserved                                                                                                              |                                                          | Invalid                    | Invalid |
| BF                       | 1535:1528    | Reserved                                                                                                              |                                                          | Invalid                    | Invalid |
| LUT/DLY/CNT Control Data |              |                                                                                                                       |                                                          |                            |         |
| C0                       | 1543:1536    | 3-bit LUT5 [7:0] or DLY/CNT2 Control Data                                                                             | 1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)   | Valid                      | Valid   |
| C1                       | 1551:1544    | 3-bit LUT6 [7:0] or DLY/CNT3 Control Data                                                                             | 1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)   | Valid                      | Valid   |
| C2                       | 1559:1552    | 3-bit LUT7 [7:0] or DLY/CNT4 Control Data                                                                             | 1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)   | Valid                      | Valid   |
| C3                       | 1567:1560    | 3-bit LUT8 [7:0] or DLY/CNT5 Control Data                                                                             | 1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)   | Valid                      | Valid   |
| C4                       | 1575:1568    | 3-bit LUT9 [7:0] or DLY/CNT6 Control Data                                                                             | 1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)   | Valid                      | Valid   |
| C5                       | 1583:1576    | 4-bit LUT0 [15:0] or DLY/CNT0 (16bits, [15:0] = [1591:1576]) Control Data                                             | 1 - 65535 (Delay Time = [Counter Control Data + 2]/Freq) | Valid                      | Valid   |
| C6                       | 1591:1584    |                                                                                                                       |                                                          |                            |         |
| C7                       | 1599:1592    | 4-bit LUT1 [15:0] or DLY/CNT1 (16bits, [15:0] = [1607:1592]) Control Data                                             | 1 - 65535 (Delay Time = [Counter Control Data + 2]/Freq) | Valid                      | Valid   |
| C8                       | 1607:1600    |                                                                                                                       |                                                          |                            |         |
| C9                       | 1615:1608    | PGen pattern data [15:0] = [1623:1608]                                                                                |                                                          | Valid                      | Valid   |
| CA                       | 1623:1616    |                                                                                                                       |                                                          |                            |         |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                         | Register Bit Definition                                                                                                                                                                                                                                                                                                                                                                    | I <sup>2</sup> C Interface                                                                                                                                                                                                       |       |       |
|---------|--------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|
| Byte    | Register Bit |                                         |                                                                                                                                                                                                                                                                                                                                                                                            | Read                                                                                                                                                                                                                             | Write |       |
| ACMP0   |              |                                         |                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                  |       |       |
| CB      | 1628:1624    | ACMP0-IN Voltage Select                 | 00000: 50 mV<br>00010: 150 mV<br>00100: 250 mV<br>00110: 350 mV<br>01000: 450 mV<br>01010: 550 mV<br>01100: 650 mV<br>01110: 750 mV<br>10000: 850 mV<br>10010: 950 mV<br>10100: 1.05 V<br>10110: 1.15 V<br>11000: V <sub>DD</sub> /3<br>11010: IO9: EXT_V <sub>REF</sub><br>11011: IO5: EXT_V <sub>REF</sub><br>11100: IO9: EXT_V <sub>REF</sub> /2<br>11101: IO5: EXT_V <sub>REF</sub> /2 | 00001: 100 mV<br>00011: 200 mV<br>00101: 300 mV<br>00111: 400 mV<br>01001: 500 mV<br>01011: 600 mV<br>01101: 700 mV<br>01111: 800 mV<br>10001: 900 mV<br>10011: 1 V<br>10101: 1.1 V<br>10111: 1.2 V<br>11001: V <sub>DD</sub> /4 | Valid | Valid |
|         | 1630:1629    | ACMP0 Positive Input Divider            | 00: 1.0x<br>01: 0.5x<br>10: 0.33x<br>11: 0.25x                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                  | Valid | Valid |
|         | 1631         | ACMP0 Low Bandwidth (MAX: 1 MHz) Enable | 0: OFF<br>1: ON                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                  | Valid | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                         | Register Bit Definition                                                                                                                                                                                                                                                                                                                               | I <sup>2</sup> C Interface                                                                                                                                                                                                       |       |       |
|---------|--------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|
| Byte    | Register Bit |                                         |                                                                                                                                                                                                                                                                                                                                                       | Read                                                                                                                                                                                                                             | Write |       |
| ACMP1   |              |                                         |                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                  |       |       |
| CC      | 1636:1632    | ACMP1-IN Voltage Select                 | 00000: 50 mV<br>00010: 150 mV<br>00100: 250 mV<br>00110: 350 mV<br>01000: 450 mV<br>01010: 550 mV<br>01100: 650 mV<br>01110: 750 mV<br>10000: 850 mV<br>10010: 950 mV<br>10100: 1.05 V<br>10110: 1.15 V<br>11000: V <sub>DD</sub> /3<br>11010: IO9: EXT_V <sub>REF</sub><br>11011: Reserved<br>11100: IO9: EXT_V <sub>REF</sub> /2<br>11101: Reserved | 00001: 100 mV<br>00011: 200 mV<br>00101: 300 mV<br>00111: 400 mV<br>01001: 500 mV<br>01011: 600 mV<br>01101: 700 mV<br>01111: 800 mV<br>10001: 900 mV<br>10011: 1 V<br>10101: 1.1 V<br>10111: 1.2 V<br>11001: V <sub>DD</sub> /4 | Valid | Valid |
|         | 1638:1637    | ACMP1 Positive Input Divider            | 00: 1.0x<br>01: 0.5x<br>10: 0.33x<br>11: 0.25x                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                  | Valid | Valid |
|         | 1639         | ACMP1 Low Bandwidth (MAX: 1 MHz) Enable | 0: OFF<br>1: ON                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                  | Valid | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                         | Register Bit Definition                                                                                                                                                                                                                                                                                                                                                                      | I <sup>2</sup> C Interface                                                                                                                                                                                                       |       |       |
|---------|--------------|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|
| Byte    | Register Bit |                                         |                                                                                                                                                                                                                                                                                                                                                                                              | Read                                                                                                                                                                                                                             | Write |       |
| ACMP2   |              |                                         |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  |       |       |
| CD      | 1644:1640    | ACMP2-IN Voltage Select                 | 00000: 50 mV<br>00010: 150 mV<br>00100: 250 mV<br>00110: 350 mV<br>01000: 450 mV<br>01010: 550 mV<br>01100: 650 mV<br>01110: 750 mV<br>10000: 850 mV<br>10010: 950 mV<br>10100: 1.05 V<br>10110: 1.15 V<br>11000: V <sub>DD</sub> /3<br>11010: IO9: EXT_V <sub>REF</sub><br>11011: IO11: EXT_V <sub>REF</sub><br>11100: IO9: EXT_V <sub>REF</sub> /2<br>11101: IO11: EXT_V <sub>REF</sub> /2 | 00001: 100 mV<br>00011: 200 mV<br>00101: 300 mV<br>00111: 400 mV<br>01001: 500 mV<br>01011: 600 mV<br>01101: 700 mV<br>01111: 800 mV<br>10001: 900 mV<br>10011: 1 V<br>10101: 1.1 V<br>10111: 1.2 V<br>11001: V <sub>DD</sub> /4 | Valid | Valid |
|         | 1646:1645    | ACMP2 Positive Input Divider            | 00: 1.0x<br>01: 0.5x<br>10: 0.33x<br>11: 0.25x                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                  | Valid | Valid |
|         | 1647         | ACMP2 Low Bandwidth (MAX: 1 MHz) Enable | 0: OFF<br>1: ON                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |

Table 38. Register Map (Cont.)

| Address       |              | Signal Function                                                                          | Register Bit Definition                                                                                                                                                                                                                                                                                                                                                                      | I <sup>2</sup> C Interface                                                                                                                                                                                                       |       |       |
|---------------|--------------|------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|
| Byte          | Register Bit |                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                              | Read                                                                                                                                                                                                                             | Write |       |
| ACMP3         |              |                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  |       |       |
| CE            | 1652:1648    | ACMP3-IN Voltage Select                                                                  | 00000: 50 mV<br>00010: 150 mV<br>00100: 250 mV<br>00110: 350 mV<br>01000: 450 mV<br>01010: 550 mV<br>01100: 650 mV<br>01110: 750 mV<br>10000: 850 mV<br>10010: 950 mV<br>10100: 1.05 V<br>10110: 1.15 V<br>11000: V <sub>DD</sub> /3<br>11010: IO9: EXT_V <sub>REF</sub><br>11011: IO11: EXT_V <sub>REF</sub><br>11100: IO9: EXT_V <sub>REF</sub> /2<br>11101: IO11: EXT_V <sub>REF</sub> /2 | 00001: 100 mV<br>00011: 200 mV<br>00101: 300 mV<br>00111: 400 mV<br>01001: 500 mV<br>01011: 600 mV<br>01101: 700 mV<br>01111: 800 mV<br>10001: 900 mV<br>10011: 1 V<br>10101: 1.1 V<br>10111: 1.2 V<br>11001: V <sub>DD</sub> /4 | Valid | Valid |
|               | 1654:1653    | ACMP3 Positive Input Divider                                                             | 00: 1.0x<br>01: 0.5x<br>10: 0.33x<br>11: 0.25x                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1655         | ACMP3 Low Bandwidth (MAX: 1 MHz) Enable                                                  | 0: OFF<br>1: ON                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
| Miscellaneous |              |                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  |       |       |
| CF            | 1656         | Reserved                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1657         | Switch from “Matrix OUT: OSC 25 MHz PD” to “Matrix OUT: OSC 25 MHz Force On”             | 0: OSC PD<br>1: OSC Force On (Matrix Output [59])                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1658         | Switch from “Matrix OUT: OSC 25 kHz/2 MHz PD” to “Matrix OUT: OSC 25 kHz/2 MHz Force On” | 0: OSC PD<br>1: OSC Force On (Matrix Output [58])                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1659         | Reserved                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1660         | Reserved                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1661         | Reserved                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1662         | I <sup>2</sup> C reset bit with reloading NVM into Data register                         | 0: Keep existing condition<br>1: Reset execution                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                  | Valid | Valid |
|               | 1663         | Reserved                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
| D0            | 1671:1664    | Customer configurable RAM8                                                               |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
| D1            | 1679:1672    | Customer configurable RAM9                                                               |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
| D2            | 1687:1680    | Customer configurable RAM10                                                              |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
| D3            | 1695:1688    | Customer configurable RAM11                                                              |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |
| D4            | 1703:1696    | Customer configurable RAM12                                                              |                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                  | Valid | Valid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function                                            | Register Bit Definition                                                                | I <sup>2</sup> C Interface |         |
|---------|--------------|------------------------------------------------------------|----------------------------------------------------------------------------------------|----------------------------|---------|
| Byte    | Register Bit |                                                            |                                                                                        | Read                       | Write   |
| D5      | 1711:1704    | Customer configurable RAM13                                |                                                                                        | Valid                      | Valid   |
| D6      | 1719:1712    | Customer configurable RAM14                                |                                                                                        | Valid                      | Valid   |
| D7      | 1727:1720    | Customer configurable RAM15                                |                                                                                        | Valid                      | Valid   |
| D8      | 1735:1728    | Customer configurable RAM0                                 |                                                                                        | Valid                      | Valid   |
| D9      | 1743:1736    | Customer configurable RAM1                                 |                                                                                        | Valid                      | Valid   |
| DA      | 1751:1744    | Customer configurable RAM2                                 |                                                                                        | Valid                      | Valid   |
| DB      | 1759:1752    | Customer configurable RAM3                                 |                                                                                        | Valid                      | Valid   |
| DC      | 1767:1760    | Customer configurable RAM4                                 |                                                                                        | Valid                      | Valid   |
| DD      | 1775:1768    | Customer configurable RAM5                                 |                                                                                        | Valid                      | Valid   |
| DE      | 1783:1776    | Customer configurable RAM6                                 |                                                                                        | Valid                      | Valid   |
| DF      | 1791:1784    | Customer configurable RAM7                                 |                                                                                        | Valid                      | Valid   |
| E0      | 1799:1792    | Reserved                                                   |                                                                                        | Invalid                    | Invalid |
| E1      | 1807:1800    | Reserved                                                   |                                                                                        | Invalid                    | Invalid |
| E2      | 1815:1808    | Reserved                                                   |                                                                                        | Invalid                    | Invalid |
| E3      | 1823:1816    | Reserved                                                   |                                                                                        | Invalid                    | Invalid |
| E4      | 1831:1824    | Reserved                                                   |                                                                                        | Valid                      | Valid   |
| E5      | 1832         | I <sup>2</sup> C lock for read bits [1535:0] (Bank 0/1/2)  | 0: Disable (Programmed data can be read)<br>1: Enable (Programmed data cannot be read) | Valid                      | Invalid |
|         | 1833         | Reserved                                                   |                                                                                        | Valid                      | Invalid |
|         | 1835:1834    | Reserved                                                   |                                                                                        | Valid                      | Invalid |
|         | 1839:1836    | Reserved                                                   |                                                                                        | Valid                      | Invalid |
| E6      | 1847:1840    | 8-bit Pattern ID Byte 0 (From NVM): ID[23:16]              |                                                                                        | Valid                      | Valid   |
| E7      | 1855:1848    | Reserved                                                   |                                                                                        | Valid                      | Invalid |
| E8      | 1863:1856    | Reserved                                                   |                                                                                        | Valid                      | Invalid |
| E9      | 1867:1864    | I <sup>2</sup> C Control Code Bit [3:0]                    | Value for target address                                                               | Valid                      | Invalid |
|         | 1868         | Reserved                                                   |                                                                                        | Valid                      | Invalid |
|         | 1869         | Reserved                                                   |                                                                                        | Valid                      | Invalid |
|         | 1870         | I <sup>2</sup> C lock for write all bits (Bank 0/1/2/3)    | 0: Writable<br>1: Non-writable                                                         | Valid                      | Invalid |
|         | 1871         | I <sup>2</sup> C lock for write bits [1535:0] (Bank 0/1/2) | 0: Writable<br>1: Non-writable                                                         | Valid                      | Invalid |
| EA      | 1879:1872    | CNT4 Counted Value                                         |                                                                                        | Valid                      | Invalid |
| EB      | 1887:1880    | CNT0 (16bits) = [1895:1880] Counted Value                  |                                                                                        | Valid                      | Invalid |
| EC      | 1895:1888    |                                                            |                                                                                        | Valid                      | Invalid |
| ED      | 1903:1896    | CNT6 Counted Value                                         |                                                                                        | Valid                      | Invalid |

Table 38. Register Map (Cont.)

| Address      |              | Signal Function                           | Register Bit Definition                               | I <sup>2</sup> C Interface |         |
|--------------|--------------|-------------------------------------------|-------------------------------------------------------|----------------------------|---------|
| Byte         | Register Bit |                                           |                                                       | Read                       | Write   |
| EE           | 1911:1904    | CNT1 (16bits) = [1919:1904] Counted Value |                                                       | Valid                      | Invalid |
| EF           | 1919:1912    |                                           |                                                       | Valid                      | Invalid |
| Matrix Input |              |                                           |                                                       |                            |         |
| F0           | 1920         | Matrix Input 0                            | GND                                                   | Valid                      | Invalid |
|              | 1921         | Matrix Input 1                            | IO0 Digital Input                                     | Valid                      | Invalid |
|              | 1922         | Matrix Input 2                            | IO1 Digital Input                                     | Valid                      | Invalid |
|              | 1923         | Matrix Input 3                            | IO2 Digital Input                                     | Valid                      | Invalid |
|              | 1924         | Matrix Input 4                            | IO3 Digital Input                                     | Valid                      | Invalid |
|              | 1925         | Matrix Input 5                            | IO4 Digital Input                                     | Valid                      | Invalid |
|              | 1926         | Matrix Input 6                            | IO5 Digital Input                                     | Valid                      | Invalid |
|              | 1927         | Matrix Input 7                            | IO8 Digital Input                                     | Valid                      | Invalid |
| F1           | 1928         | Matrix Input 8                            | 2-bit LUT0/DFF0 Output                                | Valid                      | Invalid |
|              | 1929         | Matrix Input 9                            | 2-bitLUT1/DFF1 Output                                 | Valid                      | Invalid |
|              | 1930         | Matrix Input 10                           | 2-bitLUT2/DFF2 Output                                 | Valid                      | Invalid |
|              | 1931         | Matrix Input 11                           | 2-bitLUT3/PGen Output                                 | Valid                      | Invalid |
|              | 1932         | Matrix Input 12                           | 3-bit LUT0/DFF3 Output                                | Valid                      | Invalid |
|              | 1933         | Matrix Input 13                           | 3-bit LUT1/DFF4 Output                                | Valid                      | Invalid |
|              | 1934         | Matrix Input 14                           | 3-bit LUT2/DFF5 Output                                | Valid                      | Invalid |
|              | 1935         | Matrix Input 15                           | 3-bit LUT3/DFF6 Output                                | Valid                      | Invalid |
| F2           | 1936         | Matrix Input 16                           | 3-bit LUT4/DFF7 Output                                | Valid                      | Invalid |
|              | 1937         | Matrix Input 17                           | 3-bit LUT5/CNT_DLY2(8bit) Output                      | Valid                      | Invalid |
|              | 1938         | Matrix Input 18                           | 3-bit LUT6/CNT_DLY3(8bit) Output                      | Valid                      | Invalid |
|              | 1939         | Matrix Input 19                           | 3-bit LUT7/CNT_DLY4(8bit) Output                      | Valid                      | Invalid |
|              | 1940         | Matrix Input 20                           | 3-bit LUT8/CNT_DLY5(8bit) Output                      | Valid                      | Invalid |
|              | 1941         | Matrix Input 21                           | 3-bit LUT9/CNT_DLY6(8bit) Output                      | Valid                      | Invalid |
|              | 1942         | Matrix Input 22                           | 4-bit LUT0/CNT_DLY0(16bit) Output                     | Valid                      | Invalid |
|              | 1943         | Matrix Input 23                           | 4-bit LUT1/CNT_DLY1(16bit) Output                     | Valid                      | Invalid |
| F3           | 1944         | Matrix Input 24                           | 3-bit LUT10/Pipe Delay (1 <sup>st</sup> stage) Output | Valid                      | Invalid |
|              | 1945         | Matrix Input 25                           | Pipe Delay Output0                                    | Valid                      | Invalid |
|              | 1946         | Matrix Input 26                           | Pipe Delay Output1                                    | Valid                      | Invalid |
|              | 1947         | Matrix Input 27                           | Fixed "L" output because it is OSC clock.             | Valid                      | Invalid |
|              | 1948         | Matrix Input 28                           | Fixed "L" output because it is OSC clock.             | Valid                      | Invalid |
|              | 1949         | Matrix Input 29                           | Fixed "L" output because it is OSC clock.             | Valid                      | Invalid |
|              | 1950         | Matrix Input 30                           | Filter0/Edge Detect0 Output                           | Valid                      | Invalid |
|              | 1951         | Matrix Input 31                           | Filter1/Edge Detect1 Output                           | Valid                      | Invalid |

Table 38. Register Map (Cont.)

| Address  |              | Signal Function | Register Bit Definition                      | I <sup>2</sup> C Interface |         |
|----------|--------------|-----------------|----------------------------------------------|----------------------------|---------|
| Byte     | Register Bit |                 |                                              | Read                       | Write   |
| F4       | 1952         | Matrix Input 32 | Virtual Input [0]                            | Valid                      | Valid   |
|          | 1953         | Matrix Input 33 | Virtual Input [1]                            | Valid                      | Valid   |
|          | 1954         | Matrix Input 34 | Virtual Input [2]                            | Valid                      | Valid   |
|          | 1955         | Matrix Input 35 | Virtual Input [3]                            | Valid                      | Valid   |
|          | 1956         | Matrix Input 36 | Virtual Input [4]                            | Valid                      | Valid   |
|          | 1957         | Matrix Input 37 | Virtual Input [5]                            | Valid                      | Valid   |
|          | 1958         | Matrix Input 38 | Virtual Input [6]                            | Valid                      | Valid   |
|          | 1959         | Matrix Input 39 | Virtual Input [7]                            | Valid                      | Valid   |
| F5       | 1960         | Matrix Input 40 | 3-bit LUT11/DFF8 (SET/RST) Output            | Valid                      | Invalid |
|          | 1961         | Matrix Input 41 | 3-bit LUT12/DFF9 (SET/RST) Output            | Valid                      | Invalid |
|          | 1962         | Matrix Input 42 | 3-bit LUT13/DFF10 (SET/RST) Output           | Valid                      | Invalid |
|          | 1963         | Matrix Input 43 | 3-bit LUT14/DFF11 (SET/RST) Output           | Valid                      | Invalid |
|          | 1964         | Matrix Input 44 | 3-bit LUT15/DFF12 (SET/RST) Output           | Valid                      | Invalid |
|          | 1965         | Matrix Input 45 | 3-bit LUT16/DFF13 (SET/RST) Output           | Valid                      | Invalid |
|          | 1966         | Matrix Input 46 | 3-bit LUT17/DFF14 (SET/RST) Output           | Valid                      | Invalid |
|          | 1967         | Matrix Input 47 | 4-bit LUT2 Output                            | Valid                      | Invalid |
| F6       | 1968         | Matrix Input 48 | IO9 Digital Input                            | Valid                      | Invalid |
|          | 1969         | Matrix Input 49 | IO10 Digital Input                           | Valid                      | Invalid |
|          | 1970         | Matrix Input 50 | IO11 Digital Input                           | Valid                      | Invalid |
|          | 1971         | Matrix Input 51 | IO12 Digital Input                           | Valid                      | Invalid |
|          | 1972         | Matrix Input 52 | IO13 Digital Input                           | Valid                      | Invalid |
|          | 1973         | Matrix Input 53 | IO14 Digital Input                           | Valid                      | Invalid |
|          | 1974         | Matrix Input 54 | IO15 Digital Input                           | Valid                      | Invalid |
|          | 1975         | Matrix Input 55 | IO16 Digital Input                           | Valid                      | Invalid |
| F7       | 1976         | Matrix Input 56 | IO17 Digital Input                           | Valid                      | Invalid |
|          | 1977         | Matrix Input 57 | ACMP_0 Output                                | Valid                      | Invalid |
|          | 1978         | Matrix Input 58 | ACMP_1 Output                                | Valid                      | Invalid |
|          | 1979         | Matrix Input 59 | ACMP_2 Output                                | Valid                      | Invalid |
|          | 1980         | Matrix Input 60 | ACMP_3 Output                                | Valid                      | Invalid |
|          | 1981         | Matrix Input 61 | Programmable Delay with Edge Detector Output | Valid                      | Invalid |
|          | 1982         | Matrix Input 62 | nRST_core                                    | Valid                      | Invalid |
|          | 1983         | Matrix Input 63 | V <sub>DD</sub>                              | Valid                      | Invalid |
| Reserved |              |                 |                                              |                            |         |
| F8       | 1991:1984    | Reserved        |                                              | Valid                      | Invalid |
| F9       | 1999:1992    | Reserved        |                                              | Valid                      | Invalid |
| FA       | 2007:2000    | Reserved        |                                              | Valid                      | Invalid |

Table 38. Register Map (Cont.)

| Address |              | Signal Function | Register Bit Definition | I <sup>2</sup> C Interface |         |
|---------|--------------|-----------------|-------------------------|----------------------------|---------|
| Byte    | Register Bit |                 |                         | Read                       | Write   |
| FB      | 2015:2008    | Reserved        |                         | Valid                      | Valid   |
| FC      | 2023:2016    | Reserved        |                         | Valid                      | Invalid |
| FD      | 2031:2024    | Reserved        |                         | Valid                      | Invalid |
| FE      | 2039:2032    | Reserved        |                         | Valid                      | Valid   |
| FF      | 2047:2040    | Reserved        |                         | Valid                      | Valid   |

## 18. Package Top Marking Definitions

### 18.1 STQFN 20L 2.0 mm x 3.0 mm 0.4P COL Package

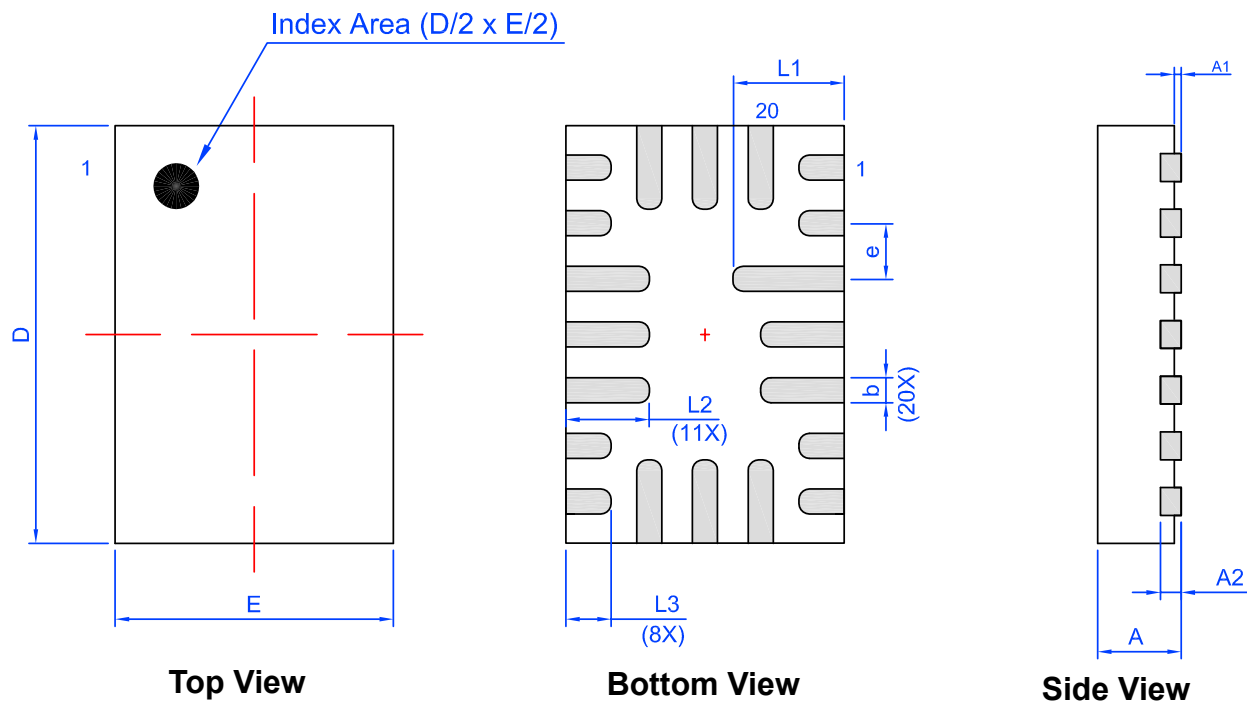
|           |        |          |
|-----------|--------|----------|
| Part Code | XXXXXX |          |
| Datecode  | DD LLL | Lot      |
| COO       | CRR    | Revision |
|           | o      |          |

- XXXXXX – Part ID Field: identifies the specific device configuration  
DD – Date Code Field: Coded date of manufacture  
LLL – Lot Code: Designates Lot #  
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin  
RR – Revision Code: Device Revision

## 19. Package Information

### 19.1 Package Outlines for STQFN 20L 2.0 mm x 3.0 mm 0.4P COL Package

JEDEC MO-220  
IC Net Weight: 0.0090 g



Unit: mm

| Symbol | Min      | Nom. | Max   | Symbol | Min   | Nom.  | Max   |
|--------|----------|------|-------|--------|-------|-------|-------|
| A      | 0.50     | 0.55 | 0.60  | D      | 2.95  | 3.00  | 3.05  |
| A1     | 0.005    | -    | 0.050 | E      | 1.95  | 2.00  | 2.05  |
| A2     | 0.10     | 0.15 | 0.20  | L1     | 0.75  | 0.80  | 0.85  |
| b      | 0.13     | 0.18 | 0.23  | L2     | 0.55  | 0.60  | 0.65  |
| e      | 0.40 BSC |      |       | L3     | 0.275 | 0.325 | 0.375 |

## 19.2 STQFN Handling

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

## 19.3 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm<sup>3</sup> (nominal) for STQFN 20L Package. More information can be found at <http://www.jedec.org>.

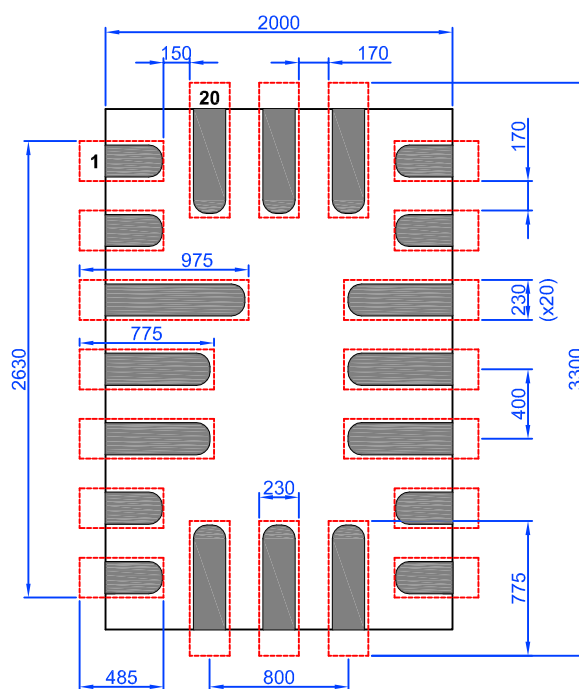
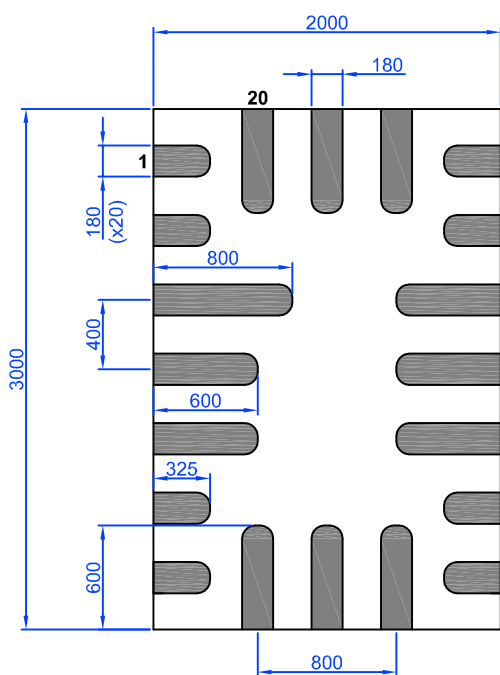
## 20. Layout Guidelines

### 20.1 STQFN-20L 2.0 mm x 3.0 mm 0.4P COL Package

 Exposed Pad  
(Top View)

 Recommended Land Pattern  
(Top View)

Units:  $\mu\text{m}$



## 21. Ordering Information

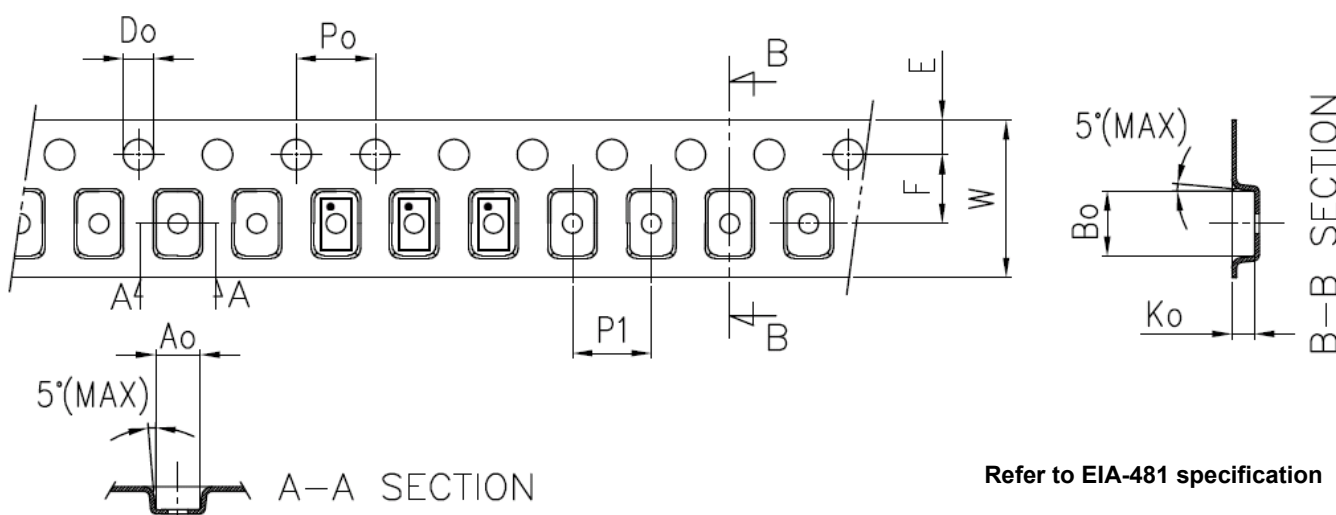
| Part Number | Package Description | Carrier Type  | Temperature Range |
|-------------|---------------------|---------------|-------------------|
| SLG46533-EV | 20-pin STQFN        | Tape and Reel | -40 °C to +105 °C |

### 21.1 Tape and Reel Specifications

| Package Type                                | # of Pins | Nominal Package Size (mm) | Max Units |         | Reel & Hub Size (mm) | Trailer (min) |             | Leader (min) |             | Tape Width (mm) | Part Pitch (mm) |
|---------------------------------------------|-----------|---------------------------|-----------|---------|----------------------|---------------|-------------|--------------|-------------|-----------------|-----------------|
|                                             |           |                           | per Reel  | per Box |                      | Pockets       | Length (mm) | Pockets      | Length (mm) |                 |                 |
| STQFN 20L<br>2.0 mm x<br>3.0 mm 0.4P<br>COL | 20        | 2.0 x 3.0 x<br>0.55       | 3,000     | 3,000   | 178/60               | 100           | 400         | 100          | 400         | 8               | 4               |

### 21.2 Carrier Tape Drawing and Dimensions

| Package Type                                | Pocket BTM Length (mm) | Pocket BTM Width (mm) | Pocket Depth (mm) | Index Hole Pitch (mm) | Pocket Pitch (mm) | Index Hole Diameter (mm) | Index Hole to Tape Edge (mm) | Index Hole to Pocket Center (mm) | Tape Width (mm) |
|---------------------------------------------|------------------------|-----------------------|-------------------|-----------------------|-------------------|--------------------------|------------------------------|----------------------------------|-----------------|
|                                             | A0                     | B0                    | K0                | P0                    | P1                | D0                       | E                            | F                                | W               |
| STQFN 20L<br>2.0 mm x<br>3.0 mm 0.4P<br>COL | 2.2                    | 3.15                  | 0.76              | 4                     | 4                 | 1.5                      | 1.75                         | 3.5                              | 8               |



## Glossary

### A

|      |                   |
|------|-------------------|
| ACK  | Acknowledge bit   |
| ACMP | Analog Comparator |

### B

|    |         |
|----|---------|
| BG | Bandgap |
|----|---------|

### C

|     |         |
|-----|---------|
| CLK | Clock   |
| CNT | Counter |

### D

|     |             |
|-----|-------------|
| DFF | D Flip-Flop |
| DLY | Delay       |

### E

|     |                           |
|-----|---------------------------|
| ES  | Electrical Specifications |
| ESD | Electrostatic discharge   |

### F

|     |                      |
|-----|----------------------|
| FSM | Finite State Machine |
|-----|----------------------|

### G

|      |                              |
|------|------------------------------|
| GPI  | General Purpose Input        |
| GPIO | General Purpose Input/Output |
| GPO  | General Purpose Output       |

### I

|    |              |
|----|--------------|
| IN | Input        |
| IO | Input/Output |

### L

|     |                       |
|-----|-----------------------|
| LB  | Low Bandwidth         |
| LSB | Least Significant Bit |
| LUT | Look Up Table         |

### M

|     |                      |
|-----|----------------------|
| MSB | Most Significant Bit |
| MUX | Multiplexer          |

**N**

|      |                     |
|------|---------------------|
| nRST | Reset               |
| NVM  | Non-Volatile Memory |

**O**

|     |                       |
|-----|-----------------------|
| OD  | Open-drain            |
| OE  | Output Enable         |
| OSC | Oscillator            |
| OTP | One Time Programmable |
| OUT | Output                |

**P**

|       |                    |
|-------|--------------------|
| PD    | Power-Down         |
| PGen  | Pattern Generator  |
| POR   | Power-On Reset     |
| PP    | Push-pull          |
| PWR   | Power              |
| P DLY | Programmable Delay |

**R**

|     |            |
|-----|------------|
| R/W | Read/Write |
|-----|------------|

**S**

|     |                                    |
|-----|------------------------------------|
| SCL | I <sup>2</sup> C Clock Input       |
| SDA | I <sup>2</sup> C Data Input/Output |

**T**

|    |                    |
|----|--------------------|
| TS | Temperature Sensor |
|----|--------------------|

**V**

|                  |                   |
|------------------|-------------------|
| V <sub>REF</sub> | Voltage Reference |
|------------------|-------------------|

**W**

|    |                           |
|----|---------------------------|
| WS | Wake and Sleep Controller |
|----|---------------------------|

## Revision History

| Revision | Date         | Description                                                                                                                                                             |
|----------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.02     | Aug 20, 2025 | Updated Ordering Information<br>Corrected part number<br>Fixed typos                                                                                                    |
| 1.01     | Feb 14, 2025 | Corrected cross-reference to figure 25 kHz/2 MHz OSC Block Diagram in subsections<br>25 kHz/2 MHz and 25 MHz Oscillators and IO17 or IO15 Source for 25 kHz/2 MHz Clock |
| 1.00     | Jan 30, 2025 | Initial release                                                                                                                                                         |

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