SLG47001-E/03-E

GreenPAK Programmable Mixed-Signal Matrix with Analog Features

Description

The SLG47001-E/03-E provides a small, low power component for commonly used analog signal processing and mixed-signal functions. Individual, tunable, analog components used in conjunction with configurable logic provide a way to solve a wide variety of tasks with minimal costs. The user creates their circuit design by programming the one-time programmable (OTP) non-volatile memory (NVM) to configure the interconnect logic, the macrocells, and the IO pins of the SLG47001-E/03-E.

Features

- Two Operational Amplifiers (OpAmp) with Ultra-low Power Consumption
  - Rail-to-Rail Input and Output (RRIO)
  - Ultra-low Offset Voltage
  - Zero Offset Voltage Drift
- Integrated Voltage Reference (V_{REF})
- Multi-channel Sampling Analog Comparator (MS-ACMP)
  - Sampling up to Six Analog Channels
  - Selectable Voltage Reference for Each Channel
  - Different Sampling Scenarios
  - Synchronous or Asynchronous Result Appearance
  - Range Comparator Mode
- Two 1024-Position 100 kΩ Digital Rheostats
  - Potentiometer Mode
  - I^2C and Manual Control Options
- Extended Pattern Generator (EPG)
  - Width Converter Option
  - 8-bit Parallel Data Output
  - Optional 1x 8-bit, 2x 4-bit, 4x 2-bit, or 8x 1-bit Serial Bitstream Output
  - 59 Bytes Pattern Stored in NVM
- 11 Combination Function Macrocells
  - Two 2-bit LUTs or DFF/LATCHs
  - Four 3-bit LUTs or DFF/LATCHs with Reset/Set
  - Four 3-bit LUTs, DFF/LATCHs, or Shift Registers
  - One 4-bit LUT or DFF/LATCH with Reset/Set
- Five Multi-Function Macrocells
  - Four Selectable DFF/LATCHs or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCHs or 3-bit LUT + 8-bit Delay/Counter/FSM
- Programmable Delay with Edge Detector Output
- Two Oscillators (OSC)
  - 2.048 kHz/10 kHz Oscillator with Ultra-low Current Consumption
  - 25 MHz Oscillator
- One Single-Pole/Single-Throw Analog Switch
- Analog Temperature Sensor
- Power-on Reset (POR) with CRC
- I^2C Compatible Serial Interface
- Read Back Protection (Read Lock)
- 2.3 V to 5.5 V of V_{DD} Range
- Operating Temperature Range: -40 °C to +105 °C
- RoHS Compliant/Halogen-Free
- Available Packages
  - 20-pin STQFN: 2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch (SLG47001-E)
  - 24-pin STQFN: 3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch (SLG47003-E)

Applications

- Consumer Electronics
- Handheld and Portable Electronics
- Industrial Automation and Process Control
- Personal Computers and Servers
- Battery Voltage and Current Monitoring
- Adjustable Precision Threshold
- Sensor Offset Trimming/Calibration
- Tunable Analog Filters
- Operational Amplifier Adjustable Gain and Offset
- Adjustable Voltage-to-Current Conversions
- Smartphones and Fitness Bands
- Notebook and Tablet PC

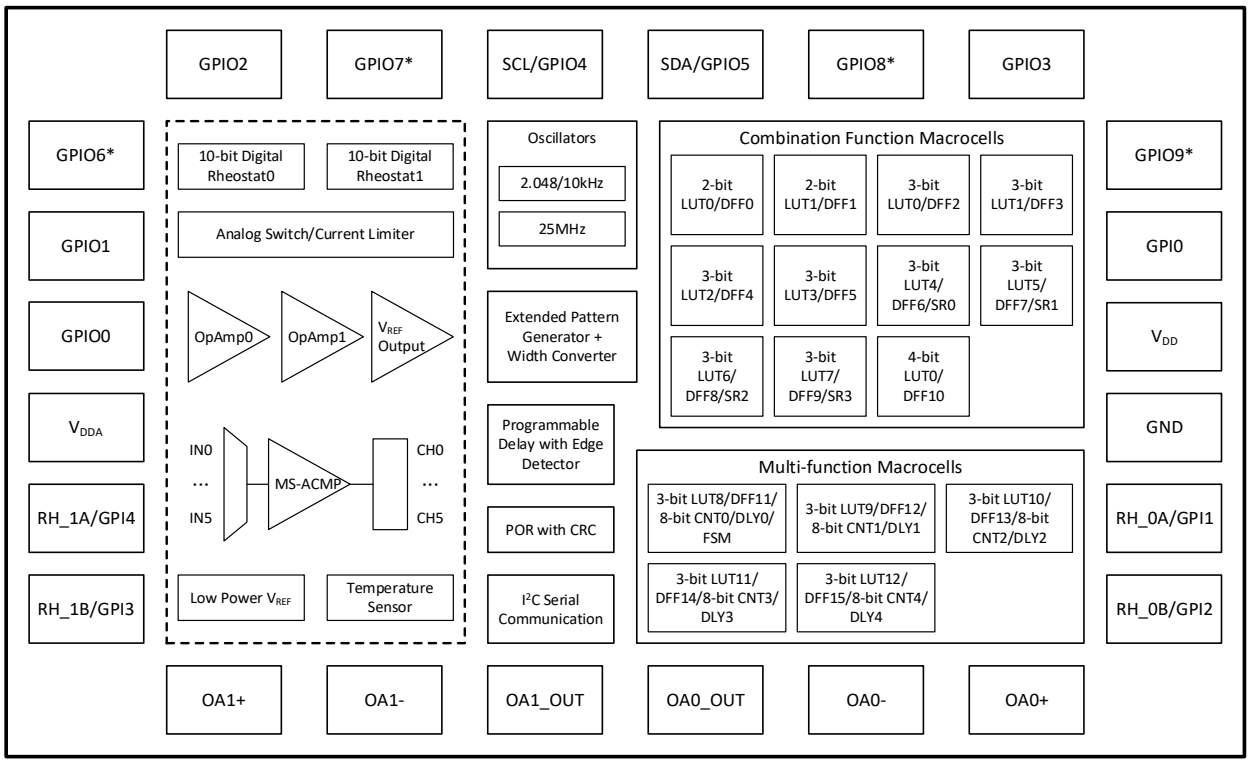
Contents

Figures

Tables

1. Overview

1.1 Block Diagram



Note*: GPIO6 – GPIO9 are available in 24-pin package (SLG47003-E) only.

Figure 1. Block Diagram

1.2 User Programmability and Customization

The SLG47001-E/03-E is a user-programmable device with one-time programmable (OTP) memory elements that can configure the connection matrix and macrocells. A programming development kit (Go Configure™ Software Hub) allows the user the ability to create initial designs. Once the design is finalized, the programming code (*.aap file) is forwarded to Renesas Electronics Corporation to integrate into the production process.

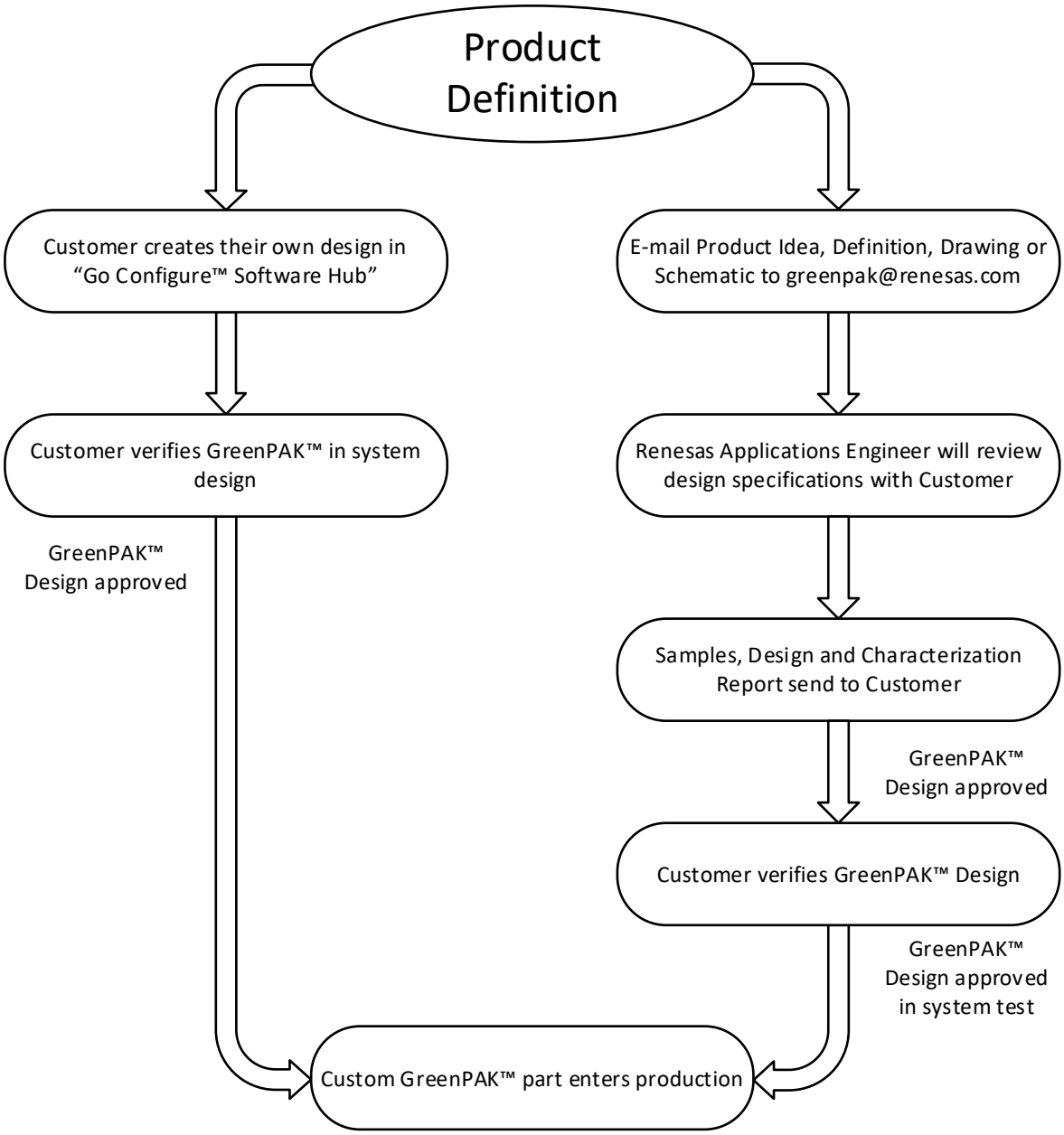


Figure 2. Device Custom Design Procedure

2. Pin Information

2.1 Pin Assignments

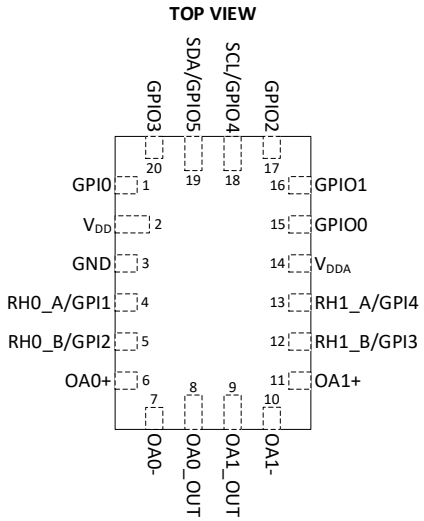


Figure 3. Pin Assignments - STQFN-20

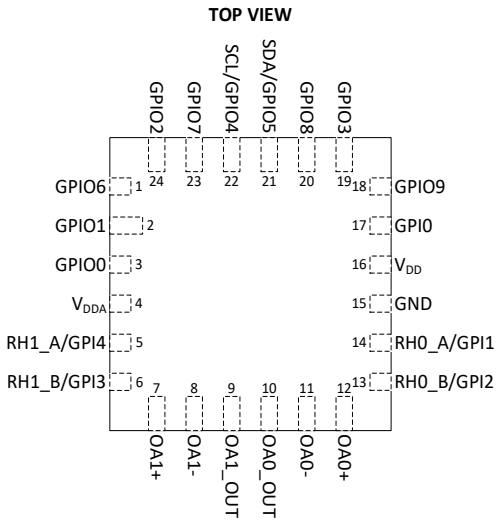


Figure 4. Pin Assignments - STQFN-24

2.2 Pin Descriptions

Table 1. Pin Assignments and Description

Pin Number		Pin Name	Pin Function
STQFN-24	STQFN-20		
15	3	GND	Ground
17	1	GPI0	GPI0, SLA_0
3	15	GPIO0	GPIO0, MS-ACMP_IN0+, EXT_OSC0_IN, ASW_A
2	16	GPIO1	GPIO1, MS-ACMP_IN1+, EXT_OSC1_IN, ASW_B
24	17	GPIO2	GPIO2, MS-ACMP_IN2+, MS-ACMP_IN-, SLA_1, AMUX_OUT
19	20	GPIO3	GPIO3, MS-ACMP_IN3+, Sink/Source Buffer Output
1	-	GPIO6	GPIO6
23	-	GPIO7	GPIO7
20	-	GPIO8	GPIO8, MS-ACMP_IN8+
18	-	GPIO9	GPIO9, MS-ACMP_IN9+
12	6	OA0+	OpAmp0 Non-Inverting Input
11	7	OA0-	OpAmp0 Inverting Input
10	8	OA0_OUT	OpAmp0_OUT, MS-ACMP_IN4+
7	11	OA1+	OpAmp1 Non-Inverting Input
8	10	OA1-	OpAmp1 Inverting Input

Pin Number		Pin Name	Pin Function
STQFN-24	STQFN-20		
9	9	OA1_OUT	OpAmp1_OUT, MS-ACMP_IN5+
14	4	RH0_A/GPI1	Digital Rheostat0 Terminal A, GPI1
13	5	RH0_B/GPI2	Digital Rheostat0 Terminal B, GPI2
5	13	RH1_A/GPI4	Digital Rheostat1 Terminal A, GPI4, MS-ACMP_IN7+
6	12	RH1_B/GPI3	Digital Rheostat1 Terminal B, GPI3, MS-ACMP_IN6+
22	18	SCL/GPIO4	I^2C_SCL, GPI_OD
21	19	SDA/GPIO5	I^2C_SDA, GPI_OD
16	2	V_{DD}	Digital Power Supply
4	14	V_{DDA}	Analog Power Supply

Table 2. Functional Pin Description

Pin Name	Signal Name	Function	Input Options	Output Options
GND	GND	Analog and Digital GND	-	-
GPI0	GPI0	General Purpose Input	Digital Input w/o Schmitt Trigger	-
			Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
	SLA_0	I^2C Target Address Bit0	Digital	-
GPIO0	GPIO0	General Purpose IO with OE	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP_IN0+	MS-ACMP Positive Input0	Analog	-
	EXT_OSC0_IN	External CLK0 Input	Digital	-
	ASW_A	Analog Switch Input A	Analog	-
GPIO1	GPIO1	General Purpose IO with OE	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP_IN1+	MS-ACMP Positive Input1	Analog	-
	EXT_OSC1_IN	External CLK1 Input	Digital	-
	ASW_B	Analog Switch Input B	Analog	-

Pin Name	Signal Name	Function	Input Options	Output Options
GPIO2	GPIO2	General Purpose IO with OE	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP_IN2+	MS-ACMP Positive Input2	Analog	-
	ACMP_IN-	MS-ACMP Negative Input	Analog	-
	SLA_1	I^2C Target Address Bit1	Digital	-
	AMUX_OUT	Analog Multiplexer Output	-	Analog
GPIO3	GPIO3	General Purpose IO with OE	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP_IN3+	MS-ACMP Positive Input3	Analog	-
	SS_BUF_OUT	Sink/Source Buffer Output	-	Analog
GPIO6	GPIO6	General Purpose IO	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
GPIO7	GPIO7	General Purpose IO	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
GPIO8	GPIO8	General Purpose IO	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP_IN8+	MS-ACMP Positive Input8	Analog	-
GPIO9	GPIO9	General Purpose IO	Digital Input w/o Schmitt Trigger	Push-pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP_IN9+	MS-ACMP Positive Input9	Analog	-
OA0+	OA0+	OpAmp0 Non-Inverting Input	Analog	-
OA0-	OA0-	OpAmp0 Inverting Input	Analog	-
OA0_OUT	OA0_OUT	OpAmp0 Output	-	Analog
	ACMP_IN4+	MS-ACMP Positive Input4	Analog	-
OA1+	OA1+	OpAmp1 Non-inverting Input	Analog	-

Pin Name	Signal Name	Function	Input Options	Output Options
OA1-	OA1-	OpAmp1 Inverting Input	Analog	-
OA1_OUT	OA1_OUT	OpAmp1 Output	-	Analog
	ACMP_IN5+	MS-ACMP Positive Input5	Analog	-
RH0_A/GPI1	RH0_A	Digital Rheostat0 Terminal A	Analog IO	-
	GPI1	General Purpose Input	Digital Input w/o Schmitt Trigger	-
			Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
RH0_B/GPI2	RH0_B	Digital Rheostat0 Terminal B	Analog IO	-
	GPI2	General Purpose Input	Digital Input w/o Schmitt Trigger	-
			Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
RH1_A/GPI4	RH1_A	Digital Rheostat1 Terminal A	Analog IO	-
	GPI4	General Purpose Input	Digital Input w/o Schmitt Trigger	-
			Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
	ACMP_IN7+	MS-ACMP Positive Input7	Analog	-
RH1_B/GPI3	RH1_B	Digital Rheostat1 Terminal B	Analog IO	-
	GPI3	General Purpose Input	Digital Input w/o Schmitt Trigger	-
			Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
	ACMP_IN6+	MS-ACMP Positive Input6	Analog	-
SCL/GPIO4	I2C_SCL	I^2C Serial Clock	Digital	-
	GPI_OD	General Purpose Input/ Open-drain Output	Digital Input w/o Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
SDA/GPIO5	I2C_SDA	I^2C Serial Data	Digital	Digital
	GPI_OD	General Purpose Input/ Open-drain Output	Digital Input w/o Schmitt Trigger	Open-drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
V_{DD}	V_{DD}	Digital Power Supply	Power	-
V_{DDA}	V_{DDA}	Analog Power Supply	Power	-

Note: It is strongly recommended to use the GPI option for the RH0_A, RH0_B, RH1_A, RH1_B pins only when all other GPIO pins are already used.

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to the absolute maximum conditions for extended periods may affect the device reliability.

Parameter		Min	Max	Unit
V_{DD} and V_{DDA} Voltage to GND		-0.5	7.0	V
Voltage Difference between V_{DD} and V_{DDA}		-0.5	0.5	V
SCL/GPIO4 and SDA/GPIO5 Voltage to GND		-0.5	7.0	V
GPIO0 – GPIO3, GPIO6- GPIO9, and GPI0 Pin Voltage to GND		-0.5	V_{DD} + 0.5, up to 7.0	V
OA0+, OA0-, OA0_OUT, OA1+, OA1-, OA1_OUT, RH0_A/GPI1, RH0_B/GPI2, RH1_A/GPI4, and RH1_B/GPI3 Pin Voltage to GND		-0.5	V_{DDA} + 0.5, up to 7.0	V
V_{DDA} Supply Voltage Slew-rate		-	2	V/µs
V_{DD} DC Current [1]		-	90	mA
V_{DDA} DC Current [1]		-	180	mA
GND DC Current [1]		-	145	mA
GPIO DC Current [1]	Push-pull 1x Output Mode	-	12	mA
	Push-pull 2x Output Mode	-	24	
	Open-drain 1x Output Mode	-	12	
	Open-drain 2x Output Mode	-	24	
	Open-drain 3.2x Output Mode	-	38	
	Analog Switch Mode	-	130	
Continuous Power Dissipation (JESD51-7, T_A = +25 ºC)	STQFN-20 (Derate 21.8 mW/°C above T_A = +25 ºC)	-	2729	mW
	STQFN-24 (Derate 12.5 mW/°C above T_A = +25 ºC)	-	1568	
Junction Temperature		-	+150	°C
Storage Temperature Range		-65	+150	°C
[1] Continuous operation at T_J = +110 ºC.				

3.2 ESD Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	-	V
ESD Protection (Charged Device Model)	1300	-	V

3.3 Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
V_{DD} Supply Voltage Range		2.3	5.5	V
V_{DDA} Supply Voltage Range		2.3	5.5	V
Voltage Difference between V_{DD} and V_{DDA}	$\lvert V_{DD} - V_{DDA} \rvert$	-0.3	0.3	V
SCL/GPIO4 and SDA/GPIO5 Voltage Range		-0.3	5.5	V
GPIO0 – GPIO3, GPIO6- GPIO9, and GPI0 Pin Voltage to GND		-0.3	V_{DD} + 0.3, up to 5.5	V
OA0+, OA0-, OA0_OUT, OA1+, OA1-, OA1_OUT, RH0_A/GPI1, RH0_B/GPI2, RH1_A/GPI4, and RH1_B/GPI3 Pin Voltage to GND		-0.3	V_{DDA} + 0.3, up to 5.5	V
Logic Input Pin Current		-	1	µA
Operating Ambient Temperature Range		-40	+105	°C
Input Capacitor at V_{DD} and V_{DDA} Pins		0.1	-	µF

3.4 Electrical Specifications

3.4.1 Logic IO Specifications

V_{DD} = 2.3 V to 5.5 V, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-level Input Voltage	V_{IH}	Logic Input [1]	0.7 x V_{DD}	-	-	V
		Logic Input with Schmitt Trigger	0.7 x V_{DD}	-	-	
		Low-voltage Logic Input [1]	1.29	-	-	
LOW-level Input Voltage	V_{IL}	Logic Input [1]	-	-	0.3 x V_{DD}	V
		Logic Input with Schmitt Trigger	-	-	0.3 x V_{DD}	
		Low-voltage Logic Input [1]	-	-	0.5	
Schmitt Trigger Hysteresis Voltage	V_{HYS}	V_{DD} = 2.5 V ±8 %	0.30	0.45	0.60	V
		V_{DD} = 3.3 V ±10 %	0.32	0.48	0.61	
		V_{DD} = 5.0 V ±10 %	0.42	0.59	0.77	
HIGH-level Output Voltage [1]	V_{OH_PP}	Push-pull, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OH} = 1 mA	2.39	-	-	V
		Push-pull, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OH} = 3 mA	3.03	-	-	
		Push-pull, 1x Drive, V_{DD} = 5.0 V ±10 %, I_{OH} = 5 mA	4.68	-	-	
		Push-pull, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OH} = 1 mA	2.44	-	-	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-level Output Voltage [1]	V_{OH_PP}	Push-pull, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OH} = 3 mA	3.17	-	-	V
		Push-pull, 2x Drive, V_{DD} = 5.0 V ±10 %, I_{OH} = 5 mA	4.84	-	-	
LOW-level Output Voltage [1]	V_{OL_PP}	Push-pull, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	-	-	0.079	V
		Push-pull, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	-	-	0.201	
		Push-pull, 1x Drive, V_{DD} = 5.0 V ±10 %, I_{OL} = 5 mA	-	-	0.256	
		Push-pull, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	-	-	0.043	
		Push-pull, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	-	-	0.107	
		Push-pull, 2x Drive, V_{DD} = 5.0 V ±10 %, I_{OL} = 5 mA	-	-	0.145	
LOW-level Output Voltage [1]	V_{OL_OD}	NMOS OD, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	-	-	0.035	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	-	-	0.088	
		NMOS OD, 1x Drive, V_{DD} = 5.0 V ±10 %, I_{OL} = 5 mA	-	-	0.121	
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	-	-	0.030	
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	-	-	0.062	
		NMOS OD, 2x Drive, V_{DD} = 5.0 V ±10 %, I_{OL} = 5 mA	-	-	0.081	
HIGH-level Output Pulse Current [1] [2]	I_{OH_PP}	Push-pull, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OH} = V_{DD} - 0.2 V	1.64	-	-	mA
		Push-pull, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OH} = 2.4 V	8.01	-	-	
		Push-pull, 1x Drive, V_{DD} = 5.0 V ±10 %, V_{OH} = 2.4 V	24.22	-	-	
		Push-pull, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OH} = V_{DD} - 0.2 V	3.23	-	-	
		Push-pull, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OH} = 2.4 V	15.73	-	-	
		Push-pull, 2x Drive, V_{DD} = 5.0 V ±10 %, V_{OH} = 2.4 V	47.02	-	-	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
LOW-level Output Pulse Current [1] [2]	I_{OL_PP}	Push-pull, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V		1.73	-	-	mA
		Push-pull, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V		5.57	-	-	
		Push-pull, 1x Drive, V_{DD} = 5.0 V ±10 %, V_{OL} = 0.4 V		7.60	-	-	
		Push-pull, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V		3.38	-	-	
		Push-pull, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V		10.84	-	-	
		Push-pull, 2x Drive, V_{DD} = 5.0 V ±10 %, V_{OL} = 0.4 V		14.65	-	-	
LOW-level Output Pulse Current [1] [2]	I_{OL_OD}	NMOS OD, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V		4.24	-	-	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V		13.54	-	-	
		NMOS OD, 1x Drive, V_{DD} = 5.0 V ±10 %, V_{OL} = 0.4 V		18.23	-	-	
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V		8.07	-	-	
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V		25.53	-	-	
		NMOS OD, 2x Drive, V_{DD} = 5.0 V ±10 %, V_{OL} = 0.4 V		33.72	-	-	
Startup Time	t_{SU}	From V_{DD} rising past V_{TH_PON}	V_{DD} Slew-rate < 1 V/ms	-	3.6	6.4	ms
			V_{DD} Slew-rate ≥ 1 V/ms	-	2.5	4.2	
Power-on Threshold	V_{TH_PON}	V_{DD} required to start up the device		1.62	1.84	2.08	V
Power-off Threshold	V_{TH_POFF}	V_{DD} to turn off the device		0.95	1.34	1.60	V
IO Pull-Up or Pull-Down Resistance [1]	R_{PU_PD}	1 MΩ Pull-Up: V_{GPIO} = GND; 1 MΩ Pull-Down: V_{GPIO} = V_{DD}		0.83	1	1.30	MΩ
		100 kΩ Pull-Up: V_{GPIO} = GND; 100 kΩ Pull-Down: V_{GPIO} = V_{DD}		84	104	131	kΩ
		10 kΩ Pull-Up: V_{GPIO} = GND; 10 kΩ Pull-Down: V_{GPIO} = V_{DD}		6.5	9.3	12.1	
Input Capacitance	C_{IN}			-	4	-	pF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current [3]	I_{LKG}	GPIO0 to GPIO9, GPI0 as Logic Input	-	-	10	nA
		GPIO1 to GPIO3, GPIO8, GPIO9 as MS-ACMP_IN+	-	-	10	
		GPIO0, GPIO1 as ASW_A, ASW_B	-	-	10	
		GPIO2 as Ext. V_{REF} Input	-	-	30	
		GPIO4, GPIO5 as SCL, SDA	-	-	10	
		RH0_A, RH0_B, RH1_A, RH1_B as Digital Rheostat Terminal	-	-	20	
		RH0_A, RH0_B as Logic Input	-	-	20	
		RH1_A, RH1_B as MS-ACMP_IN+	-	-	20	

[1] No hysteresis.

[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

[3] Guaranteed by design, not tested in production.

3.4.2 I²C Specifications

V_{DD} = 2.3 V to 5.5 V, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		Fast-Mode		Fast-Mode Plus		Unit
				Min	Max	Min	Max	
IO Stage								
LOW-level Input Voltage	V_{IL}	Schmitt Trigger Input		-	0.3 x V_{DD}	-	0.3 x V_{DD}	V
		Low-voltage Logic Input [1] [2]		-	1.0	N/A	N/A	
HIGH-level Input Voltage	V_{IH}	Schmitt Trigger Input		0.7 x V_{DD}	-	0.7 x V_{DD}	-	V
		Low-voltage Logic Input [1] [2]		1.25	-	N/A	N/A	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}			0.05 x V_{DD}	-	0.05 x V_{DD}	-	V
LOW-level Output Voltage	V_{OL}	OD at 3 mA Sink Current		0	0.4	0	0.4	V
LOW-level Output Current	I_{OL}	V_{OL} = 0.4 V	V_{DD} = 2.3 V [2]	3	-	19.5	-	mA
			V_{DD} = 3.0 V	3	-	20	-	
			V_{DD} = 4.5 V	3	-	20	-	
		V_{OL}= 0.6 V		6	-	-	-	
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ [2]	t_{OF}			14x (V_{DD}/5.5)	250	10x (V_{DD}/5.5)	120	ns
Pulse Width of Spikes that must be suppressed by the Input Filter	t_{SP}			0	50	0	50	ns
Input Current Each IO Pin	I_I	0.1 x V_{DD} < V_I < 0.9 x $V_{DD(MAX)}$		-10	+10	-10	+10	µA
Capacitance for Each IO Pin	C_I			-	10	-	10	pF
Timing (see Figure 154 for Diagram)								
SCL Clock Frequency	f_{SCL}			-	400	-	1000	kHz
Hold Time for (Repeated) START Condition	t_{HD_STA}			600	-	260	-	ns
SCL Clock, LOW Period	t_{LOW}			1300	-	500	-	ns
SCL Clock, HIGH Period	t_{HIGH}			600	-	260	-	ns
Set-up Time for Repeated START Condition	t_{SU_STA}			600	-	260	-	ns
Data Hold Time	t_{HD_DAT}			0	-	0	-	ns
		Low-voltage Logic Input Mode [2]		362	-	N/A	N/A	

Parameter	Symbol	Conditions	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
Data Set-up Time	t_{SU_DAT}		100	-	50	-	ns
		Low-voltage Logic Input Mode [2]	364	-	N/A	N/A	
SCL, SDA Rise Time	t_R		-	300	-	120	ns
SCL, SDA Fall Time [2]	t_F		-	300	-	120	ns
Set-up Time for STOP Condition	t_{SU_STO}		600	-	260	-	ns
Bus Free Time between STOP and START Conditions	t_{BUF}		1300	-	500	-	ns
Data Valid Time	t_{VD_DAT}		-	900	-	450	ns
Data Valid Acknowledge Time	t_{VD_ACK}		-	900	-	450	ns

[1] No hysteresis.
[2] Does not meet Standard I²C Specifications.
[3] For Fm+, SDA pin must be configured as NMOS 3.2x Open-drain by the SCL_I2C_MODE bit (Reg[741]).

3.4.3 Estimated Typical Current of Macrocell Configurations

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
V_{DD} + V_{DDA} Supply Current	I_{VDD} + I_{VDDA}	IC Quiescent Current	POR and I²C Enabled	60	83	138	nA
			POR, BG and I²C Enabled	362	396	482	
		OSC0 2.048 kHz	Pre-divider = 1	339	373	460	nA
			Pre-divider = 4	336	368	452	
			Pre-divider = 8	335	368	452	
		OSC0 10 kHz	Pre-divider = 1	460	506	622	nA
			Pre-divider = 4	445	484	586	
			Pre-divider = 8	440	480	580	
		OSC1 25 MHz	Pre-divider = 1	61.3	77.4	115	µA
			Pre-divider = 4	42.4	52.0	75.0	
			Pre-divider = 8	38.9	47.3	67.5	
		OpAmp Quiescent Current per Macrocell		30.1	30.8	32.6	µA

Parameter	Symbol	Conditions		V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
V_{DD} + V_{DDA} Supply Current	I_{VDD} + I_{VDDA}	MS-ACMP in Continuous Sampling Mode, Six Channels, 10 kHz CLK (Average Consumption)	V_{IN+} = 1 MΩ Pull-Up, V_{REF} = 32 mV (Int. or Ext.)	33.8	35.9	40.5	µA
			V_{IN+} = V_{REF} +10 mV, V_{REF} = 32 mV (Int. or Ext.)	39.4	42.3	48.8	
			V_{IN+} = TS_OUT, V_{REF} = 1696 mV (Int. or Ext.)	39.2	42.7	49.4	
		MS-ACMP V_{REF} Generator with Sink/Source Buffer Enabled		37.2	40.0	45.8	µA
		Temperature Sensor Output		15.8	15.9	16.1	µA
		Rheostat Quiescent Current per Macrocell		60	80	130	nA

3.4.4 Estimated Typical Delay of Each Macrocell

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
GPI and GPIO Macrocell									
Propagation Delay	t_{PD}	Digital Input to PP 1x	26	26	18	19	13	14	ns
		Digital Input to PP 2x	24	24	17	18	12	13	
		Digital Input with Schmitt Trigger to PP 1x	27	27	19	19	13	14	
		Low-voltage Digital Input to PP 1x	29	242	21	162	16	100	
		Digital Input to NMOS 1x	-	24	-	17	-	13	
		Digital Input to NMOS 2x	-	23	-	16	-	13	
		Output Enable from Pin, OE Hi-Z to 1	26	-	19	-	13	-	
		Output Enable from Pin, OE Hi-Z to 0	-	25	-	18	-	13	
		PP 1x Hi-Z to 1	26	-	19	-	13	-	
		PP 1x Hi-Z to 0	-	25	-	18	-	13	
		PP 2x Hi-Z to 1	24	-	17	-	12	-	
		PP 2x Hi-Z to 0	-	23	-	17	-	12	

Parameter	Symbol	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Combination Function Macrocell									
Propagation Delay	t_{PD}	2-bit LUT	14	14	10	10	7	7	ns
		3-bit LUT	16	15	11	11	7	8	
		4-bit LUT	16	14	11	10	7	7	
		DFF Q	17	18	12	13	8	10	
		DFF nQ	18	18	13	13	9	9	
		DFF nRST High Q	-	21	-	15	-	11	
		DFF nRST High nQ	21	-	15	-	10	-	
		DFF nRST Low Q	-	21	-	15	-	10	
		DFF nRST Low nQ	21	-	15	-	10	-	
		DFF nSET High Q	22	-	15	-	11	-	
		DFF nSET High nQ	-	22	-	16	-	12	
		DFF nSET Low Q	22	-	15	-	10	-	
		DFF nSET Low nQ	-	22	-	16	-	11	
		LATCH Q	16	17	11	12	8	8	
		LATCH nQ	17	16	12	12	8	9	
		LATCH nRST High Q	23	22	16	16	11	12	
		LATCH nRST High nQ	23	23	16	17	11	12	
		LATCH nRST Low Q	22	22	16	16	11	11	
		LATCH nRST Low nQ	23	23	16	16	11	12	
		LATCH nSET High Q	20	20	14	14	10	10	
		LATCH nSET High nQ	21	20	14	15	9	11	
		LATCH nSET Low Q	20	19	14	14	9	10	
		LATCH nSET Low nQ	20	21	14	15	10	10	
		Shift Register Transition	21	20	14	15	10	11	
		Shift Register Reset	23	23	16	16	11	12	

Parameter	Symbol	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Multi-Function Macrocell									
Propagation Delay	t_{PD}	Multi-Function 3-bit LUT	17	18	12	13	8	9	ns
		Multi-Function 3-bit LUT, CNT DLY	33	33	23	23	16	17	
		Multi-Function DFF Q	17	17	12	13	8	10	
		Multi-Function DFF nQ	18	18	13	13	9	10	
		Multi-Function DFF nRST Q	-	22	-	16	-	11	
		Multi-Function DFF nRST nQ	23	-	16	-	11	-	
		Multi-Function DFF nSET Q	23	-	16	-	11	-	
		Multi-Function DFF nSET nQ	-	24	-	17	-	12	
		Multi-Function LATCH Q	16	18	11	13	8	9	
		Multi-Function LATCH nQ	19	17	13	12	8	9	
		Multi-Function LATCH nRST Q	23	24	16	17	11	12	
		Multi-Function LATCH nRST nQ	24	23	17	17	11	12	
		Multi-Function LATCH nSET Q	22	21	15	15	10	11	
		Multi-Function LATCH nSET nQ	21	22	15	16	10	11	
Edge Detector Macrocell									
Width	t_W	Edge Detect	108	77	73	55	46	36	ns
Propagation Delay	t_{PD}	Edge Detect	33	34	24	24	16	17	ns
EPG Macrocell									
Propagation Delay	t_{PD}	CLK	468	467	487	487	510	511	ns
		nRST Hi-Z to 0	-	17	-	12	-	8	
		nRST Hi-Z to 1	19	-	12	-	8	-	

3.4.5 Typical Propagation Delay and Pulse Width

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Pulse Width	t_W	Mode: (any) Edge Detect, Edge Detect Output	1-Cell	220	161	116	ns
			2-Cell	439	321	231	
			3-Cell	657	481	346	
			4-Cell	878	641	461	
Delay Time	t_{DLY1}	Mode: (any) Edge Detect, Edge Detect Output	1-Cell	16	11	7.2	ns
			2-Cell	16	11	7.2	
			3-Cell	16	11	7.2	
			4-Cell	16	11	7.2	
	t_{DLY2}	Mode: Both Edge Detect, Edge Detect Output	1-Cell	239	174	125	ns
			2-Cell	458	334	240	
			3-Cell	676	494	354	
			4-Cell	897	654	470	

3.4.6 Typical Counter/Delay Offset

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-on Time	25 MHz	Auto	0.05	0.03	0.02	µs
	2.048 kHz	Auto	680	587	499	
	10 kHz	Auto	680	587	499	
Frequency Settling Time	25 MHz	Auto	7.1	8.4	12.8	Stabilized CLK
	2.048 kHz	Auto	2.4	2.2	1.3	
	10 kHz	Auto	7.8	6.9	6.0	
Variable (CLK Period)	25 MHz	Forced	0 to 1	0 to 1	0 to 1	Stabilized CLK
	2.048 kHz	Forced	0 to 1	0 to 1	0 to 1	
	10 kHz	Forced	0 to 1	0 to 1	0 to 1	
Propagation Delay (Non-delayed Edge)	25 MHz/2.048 kHz/ 10 kHz	Either	32	23	16	ns

3.4.7 Oscillator Frequency

V_{DD} = 2.3 V to 5.5 V, unless otherwise specified.

Parameter	T_A = +25 °C			T_A = -40 °C to +105 °C		
	Min [kHz]	Max [kHz]	Error [%]	Min [kHz]	Max [kHz]	Error [%]
2.048 kHz OSC0	2.015	2.081	+1.61	1.890	2.098	+2.44
			-1.61			-7.71
10 kHz OSC0	9.84	10.16	+1.60	9.40	10.10	+1.00
			-1.60			-6.00
25 MHz OSC1	24600	25400	+1.60	23528	25425	+1.70
			-1.60			-5.89

3.4.8 Oscillator Power-On Delay

T_A = +25 °C, OSC Power Setting: 'Auto Power-on', unless otherwise specified.

V_{DD} Range [V]	OSC0 (2.048 kHz)		OSC0 (10 kHz)		OSC1 (25 MHz)		OSC1 (25 MHz) Start with Delay	
	Typ [µs]	Max [µs]	Typ [µs]	Max [µs]	Typ [ns]	Max [ns]	Typ [ns]	Max [ns]
2.3	721	931	720	930	54	59	154	164
2.5	681	874	680	873	47	52	151	162
3.3	587	739	587	738	33	36	146	157
4.0	542	674	542	674	27	30	145	156
4.5	519	641	519	641	24	27	145	156
5.0	499	612	499	612	22	25	145	156
5.5	475	579	475	579	21	24	145	156

3.4.9 OpAmp V_{REF} Generator Specifications

V_{DDA} = 2.3 V to 5.5 V, V_{REF} = 2016 mV, V_{REF} Supply Voltage = V_{DDA}, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
OpAmp0 High-side VREFGEN							
High-side V_{REF} Accuracy	$V_{REF\_ACC\_HS}$	V_{DDA} ≥ 2.5 V, No Load	T_A = +25 °C	-0.04	-	0.03	%
			T_A = -40 °C to +105 °C	-0.07	-	0.05	%

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
OpAmp0 Low-side VREFGEN							
Low-side V_{REF} Accuracy	V_{REF_ACC}	V_{REF} = 2016 mV, No Load	T_A = +25 °C	-0.23	-	0.43	%
				-4.57	-	8.61	mV
			T_A = -40 °C to +105 °C	-0.26	-	0.87	%
				-5.27	-	17.63	mV
Low-side V_{REF} Divider Accuracy	$V_{REF\_DIV\_ACC}$	Divider Tap = 16 to 63, Fixed V_{DDA}		-0.45	-	0.40	%
		Divider Tap = 1 to 63, Fixed V_{DDA}		-1.72	-	1.38	%
OpAmp1 VREFGEN							
Low-side V_{REF} Accuracy	V_{REF_ACC}	V_{REF} = 2016 mV, No Load	T_A = +25 °C	-0.29	-	0.51	%
				-5.88	-	10.31	mV
			T_A = -40 °C to +105 °C	-0.32	-	0.96	%
				-6.05	-	19.38	mV
Low-side V_{REF} Divider Accuracy	$V_{REF\_DIV\_ACC}$	Divider Tap = 16 to 63, Fixed V_{DDA}		-0.72	-	0.52	%
		Divider Tap = 1 to 63, Fixed V_{DDA}		-1.62	-	1.35	%

3.4.10 MS-ACMP V_{REF} Generator Specifications

V_{DD} = 2.3 V to 5.5 V, V_{REF} = 2016 mV, V_{REF} Supply Voltage = V_{DDA}, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Low-side V_{REF} Accuracy	V_{REF_ACC}	V_{REF} = 2016 mV, No Load	T_A = +25 °C	-0.23	-	0.38	%
				-4.53	-	7.61	mV
			T_A = -40 °C to +105 °C	-0.25	-	0.83	%
				-5.08	-	16.71	mV
Low-side V_{REF} Divider Accuracy	$V_{REF\_DIV\_ACC}$	Divider Tap = 16 to 63, Fixed V_{DD}		-0.38	-	0.49	%
		Divider Tap = 1 to 63, Fixed V_{DD}		-1.80	-	1.50	%

3.4.11 Sink/Source Buffer Specifications

V_{DD} = 2.3 V to 5.5 V, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current	I_Q	V_{DD} = 5.0 V, V_{OUT_BUF} = 2016 mV, I_{LOAD} = 0 A	-	-	10.9	µA
		V_{DD} = 2.3 V, V_{OUT_BUF} = 2016 mV, I_{LOAD} = 0 A			10.4	
		V_{DD} = 2.3 V to 5.0 V, V_{OUT_BUF} = V_{DD}/2, I_{LOAD} = 0 A	-	-	3.8	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Load Regulation	$\Delta V_{OUT}(I_{LOAD})$	V_{DD} = 5.0 V, V_{OUT_BUF} = 500 mV to (V_{DD} – 750 mV), I_{LOAD} = 0.5 mA to 1 mA (Source and Sink)		-1.65	-	1.96	mV
		V_{DD} = 2.3 V, V_{OUT_BUF} = 500 mV to (V_{DD} – 750 mV), I_{LOAD} = 0.5 mA to 1 mA (Source and Sink)		-1.73	-	2.08	
Line Regulation	$\Delta V_{OUT}(V_{DDA})$	V_{DD} = 2.3 V to 5.5 V, V_{OUT_BUF} = V_{DD} – 750 mV, I_{LAOD} = 1 mA		-1.57	-	3.81	mV
Buffer Offset	V_{OS_BUF}	V_{IN_BUF} = 0 mV, No Load	T_A = +25 °C	-6.8	-	11.6	mV
			T_A = -40 °C to +105 °C	-7.8	-	12.4	
		32 mV ≤ V_{IN_BUF} ≤ 1024 mV, No Load	T_A = +25 °C	-11.7	-	8.9	
			T_A = -40 °C to +105 °C	-12.5	-	9.8	
		1024 mV ≤ V_{IN_BUF} ≤ 1600 mV, No Load	T_A = +25 °C	-4.4	-	4.5	
			T_A = -40 °C to +105 °C	-5.7	-	5.6	
		1600 mV ≤ V_{IN_BUF} ≤ 2016 mV, No Load	T_A = +25 °C	-5.5	-	6.3	
			T_A = -40 °C to +105 °C	-7.2	-	7.4	
		V_{IN_BUF} = V_{DD}, No Load	T_A = +25 °C	-5.4	-	6.4	
			T_A = -40 °C to +105 °C	-5.8	-	6.8	
		V_{IN_BUF} = 1024 mV to 2016 mV, V_{DD} = 3.3 V, No Load	T_A = +25 °C	-4.4	-	5.1	
			T_A = -40 °C to +105 °C	-5.9	-	6.4	
Buffer Output Source Current [1]	I_{SRC}	V_{DD} = 2.3 V to 5.0 V, V_{OUT_BUF} = 500 mV to (V_{DD} – 750 mV)		1	-	-	mA
Buffer Output Sink Current [1]	I_{SINK}	V_{DD} = 2.3 V to 5.0 V, V_{OUT_BUF} = 500 mV to (V_{DD} – 750 mV)		1	-	-	mA
Output Source Short-circuit Current	I_{SC_SRC}	V_{IN_BUF} = 2016 mV		4.4	12.0	19.7	mA
Output Sink Short-circuit Current	I_{SC_SINK}	V_{IN_BUF} = 2016 mV		4.6	13.4	21.8	mA
Buffer Output Capacitance Loading [1]	C_{CAP_BUF}	R_{LOAD} = 1 MΩ		-	-	5	pF
		R_{LOAD} = 560 kΩ		-	-	10	
		R_{LOAD} = 100 kΩ		-	-	40	
		R_{LOAD} = 10 kΩ		-	-	80	
		R_{LOAD} = 2 kΩ		-	-	120	
		R_{LOAD} = 1 kΩ, V_{REF} = 32 mV to 1024 mV		-	-	150	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Band Width [1]	BW	V_{OUT_BUF} = 50 mV to (V_{DD} - 100 mV), I_{LOAD} = 0.1 mA, C_{LOAD} = 150 pF	-	35	-	kHz
		V_{OUT_BUF} = 250 mV to (V_{DD} - 375 mV), I_{LOAD} = 0.5 mA, C_{LOAD} = 150 pF	-	60	-	
		V_{OUT_BUF} = 500 mV to (V_{DD} - 750 mV), I_{LOAD} = 1 mA, C_{LOAD} = 150 pF	-	100	-	
Buffer Output Slew-rate [1]	SR	With 1 mA, 150 pF Loading	0.06	0.10	-	V/µs
Buffer Turn-on Time	t_{ON}	With 1 mA, 150 pF Loading	-	9.42	-	µs
Buffer Turn-off Time	t_{OFF}	With 1 mA, 150 pF Loading	0.04	0.47	-	µs
[1] Guaranteed by design, not tested in production.						

3.4.12 Operational Amplifier Specifications

V_{DD} = V_{DDA} = 5.0 V, V_{CM} = V_{DDA}/2, R_{LOAD} = OPEN, T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC Performance						
Input Voltage Range	V_{DDA}		2.3	-	5.5	V
Quiescent Current	I_Q	T_A = +25 °C	-	33	46	µA
		T_A = -40 °C to +105 °C	-	-	50	
Input Offset Voltage	V_{OS}	T_A = +25 °C	-9	-3	9	µV
		T_A = -40 °C to +105 °C	-15	-	15	
Offset Drift over Temperature	dV_{OS}/dT	T_A = -40 °C to +105 °C	-	-0.001	0.089	µV/°C
Input Offset Current	I_{OFFSET}	T_A = +25 °C	-	160	-	pA
Input Bias Current [1]	I_B	T_A = +25 °C	-340	±30	440	pA
		T_A = -40 °C to +105 °C	-580	-	680	
Common-mode Input Voltage Range [1]	V_{CMR}		-0.1	-	V_{DDA} + 100 mV	V
Open Loop Gain	A_{OL}	R_{LOAD} = 1 MΩ	-	152	-	dB
Common-mode Input Resistance	R_{CM}		-	10	-	GΩ
Differential-mode Input Resistance	R_{DIFF}		-	10	-	GΩ
HIGH-level Output Voltage	V_{OH}	R_{LOAD} = 10 kΩ	4.94	-	-	V
LOW-level Output Voltage	V_{OL}	R_{LOAD} = 10 kΩ	-	-	0.045	V
Output Source Short-circuit Current	I_{SC_SRC}	Output short to GND	20	21	22	mA
Output Sink Short-circuit Current	I_{SC_SINK}	Output short to V_{DDA}	-35	-34	-32	mA

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Common-mode Rejection Ratio [1]	CMRR	V_{CM} = -0.1 V to 5.1 V	T_A = +25 °C	112	125	-	dB
			T_A = -40 °C to +105 °C	107	-	-	
Power Supply Rejection Ratio	PSRR	V_{DDA} = 2.3 V to 5.5 V	T_A = +25 °C	117	130	-	dB
			T_A = -40 °C to +105 °C	115	-	-	
Dynamic Performance							
Gain Bandwidth Product	GBP	f = 50 kHz, R_{LOAD} = 10 kΩ to V_{CM}		-	400	-	kHz
Common-mode Input Capacitance	C_{IN_CM}	f = 1 MHz		-	3.9	-	pF
Differential-mode Input Capacitance	C_{IN_DM}	f = 1 MHz		-	4.0	-	pF
Noise Performance							
Peak-to-Peak Input Noise Voltage	V_N	f = 0.1 Hz to 10 Hz		-	1.56	-	μV_{P-P}
Input Noise Voltage Density	e_N	f = 1 kHz		-	65	-	nV/√Hz
Input Noise Current Density	I_N	f = 1 kHz		-	79	-	fA/√Hz
		f = 10 Hz		-	77	-	
Total Harmonic Distortion + Noise	THD+N	$V_{OAx\_OUT(P-P)}$ = V_{DDA}/2, f = 1 kHz, R_{LOAD} = 50 kΩ		-	0.013	-	%
Timing							
Amplifier Turn-on Time [1]	t_{ON}	Time to reach 90 % of the target output voltage after turn-on, A_V = 1, R_{LOAD} = 50 kΩ			115	178	µs
Amplifier Turn-off Time [1]	t_{OFF}	Time to reach 10 % of the output voltage after turn-off, A_V = 1, R_{LOAD} = 50 kΩ			3.6	17.5	µs
Positive Slew Rate	SR+	V_{OAx_OUT} = 1 V to 4 V, A_V = 1, R_{LOAD} = 10 kΩ		-	130	-	mV/µs
Negative Slew Rate	SR-	V_{OAx_OUT} = 1 V to 4 V, A_V = 1, R_{LOAD} = 10 kΩ		-	100	-	mV/µs
Output Setting Time	t_{SETTLE}	Time to settle within 0.1 % of the target output voltage for 2 V_{P_P} of input voltage step, A_V = 1, R_{LOAD} = 10 kΩ, C_{LOAD} = 1.2 pF		-	65	165	µs

[1] Guaranteed by design, not tested in production.

3.4.13 Analog Switch Specifications

V_{DD} = 2.3 V to 5.5 V, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating Voltage Range	V_{ASW}	V_{ASW_A} or V_{ASW_B} to GND		0	-	V_{DD} + 0.3	V
PMOS ON Resistance	$R_{DS(ON)\_PMOS}$	ASW_MODE = 0, V_{DD} = 3.3 V, I_{ASW} = 10 mA, V_{ASW_A} > 1.2 V, T_A = +25 °C		-	2.5	6.0	Ω
NMOS ON Resistance	$R_{DS(ON)\_NMOS}$	ASW_MODE = 0, V_{DD} = 3.3 V, I_{ASW} = 10 mA, V_{ASW_B} < V_{DD} – 2.1 V, T_A = +25 °C		-	30	35	Ω
Maximum DC Switch Current	$I_{SW\_DC(MAX)}$	V_{ASW_A} = V_{DD}, R_{LOAD} connected between V_{ASW_B} and GND	T_J = +85 °C	-	-	300	mA
			T_J = +100 °C	-	-	180	
			T_J = +110 °C	-	-	130	
Maximum Pulse Switch Current	$I_{SW\_PULSE(MAX)}$	Pulse Duration = 1 ms, Duty Cycle < 5 %	T_J = +85 °C	-	-	600	mA
			T_J = +100 °C	-	-	360	
			T_J = +110 °C	-	-	260	
OFF Leakage Current	I_{LK_OFF}	Current from ASW_A pin to ASW_B pin (V_{ASW_A} = V_{DD}, V_{ASW_B} = GND), ASW_MODE = 0, CMO [62] = Low		-	-	67	nA
Turn-on Delay Time	$t_{TURN-ON}$	V_{ASW_A} = V_{DD}/2, R_{PU} = 100 Ω	V_{DD} = 2.3 V to 3.3 V	-	-	62	ns
			V_{DD} = 3.3 V to 5.5 V	-	-	46	
		V_{ASW_A} = V_{DD}/2, R_{PD} = 100 Ω	V_{DD} = 2.3 V to 3.3 V	-	-	1426	
			V_{DD} = 3.3 V to 5.5 V	-	-	222	
Turn-off Delay Time	$t_{TURN-OFF}$	V_{ASW_A} = V_{DD}/2, R_{PU} = 100 Ω	V_{DD} = 2.3 V to 3.3 V	-	-	35	ns
			V_{DD} = 3.3 V to 5.5 V	-	-	29	
		V_{ASW_A} = V_{DD}/2, R_{PD} = 100 Ω	V_{DD} = 2.3 V to 3.3 V	-	-	86	
			V_{DD} = 3.3 V to 5.5 V	-	-	16	
Maximum Switching Frequency	$f_{SW(MAX)}$	V_{ASW_A} = V_{DD}/2, R_{PU} = 100 Ω	V_{DD} = 2.3 V to 3.3 V	10	-	-	MHz
			V_{DD} = 3.3 V to 5.5 V	13	-	-	
		V_{ASW_A} = V_{DD}/2, R_{PD} = 100 Ω	V_{DD} = 2.3 V to 3.3 V	0.31	-	-	
			V_{DD} = 3.3 V to 5.5 V	4	-	-	

3.4.14 MS-ACMP Specifications

V_{DD} = 2.3 V to 5.5 V, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input Voltage Range	V_{ACMP}	Positive Input		0	-	V_{DD}	V
		Negative Input		0	-	V_{DD}	
MS-ACMP Input Offset	V_{OFFSET}	Ext. V_{REF} = 32 mV to (V_{DD} – 32 mV), Gain = 1	T_A = +25 °C	-0.42	0.06	0.52	mV
			T_A = -40 °C to +105 °C	-0.69	-	0.77	
		Ext. V_{REF} = 2016 mV, Gain = 1	T_A = +25 °C	-0.14	0.06	0.25	mV
			T_A = -40 °C to +105 °C	-0.28	-	0.39	
Total MS-ACMP Input Accuracy (MS-ACMP Offset + Internal V_{REF} Error)	V_{OFFSET_TOTAL}	ACMPx_H2L_VREF[5:0] = ACMPx_L2H_VREF[5:0] = 2016 mV, Gain = 1	T_A = +25 °C	0.23	-	0.39	%
				-4.67	-	7.86	mV
			T_A = -40 °C to +105 °C	-0.26	-	0.85	%
				-5.36	-	17.10	mV
Clock Frequency	f_{CLK}			-	-	10	kHz
MS-ACMP Startup Time (Power-on Delay in Sampling Mode)	t_{START}	Bandgap: Auto-ON, OSC0: Auto-ON		-	-	3.13	ms
		Bandgap: Forced-ON, OSC0: Auto-ON		-	-	1.25	
		Bandgap: Auto-ON, OSC0: Forced-ON		-	-	3.09	
		Bandgap: Forced-ON OSC0: Forced-ON		-	-	0.25	
Series Input Resistance	R_{SIN}	Gain = 1x		-	10	-	GΩ
		Gain = 0.5x		-	2	-	MΩ
		Gain = 0.33x		-	2	-	
		Gain = 0.25x		-	2	-	
Gain	G	G = 1		1	1	1	V/V
		G = 0.5, V_{REF} ≥ 128 mV		0.493	0.500	0.505	
		G = 0.33, V_{REF} ≥ 128 mV		0.328	0.333	0.338	
		G = 0.25, V_{REF} ≥ 128 mV		0.246	0.250	0.255	
Resistance from MS-ACMP Input MUX Output to GPIO2	R_{MUX_GPIO2}	ACMP_MUX_OUT = 1		590	870	1180	Ω

3.4.15 Analog Temperature Sensor Specifications

V_{DD} = 2.3 V to 5.5 V, unless otherwise specified.

T_J [°C]	Target V_{TS_OUT} [V]	V_{TS_OUT} [V]		Calculated T_J [°C]		T_J Accuracy [°C]	
		Min	Max	Min	Max	Min	Max
-40	2.017	1.994	2.024	-41.4	-35.2	-1.4	4.8
-30	1.969	1.949	1.978	-31.8	-25.8	-1.8	4.2
-20	1.921	1.905	1.933	-22.5	-16.6	-2.5	3.4
-10	1.873	1.860	1.886	-12.7	-7.3	-2.7	2.7
0	1.825	1.815	1.841	-3.3	2.1	-3.3	2.1
10	1.777	1.769	1.795	6.3	11.7	-3.7	1.7
20	1.729	1.724	1.748	16.1	21.1	-3.9	1.1
25	1.705	1.699	1.722	21.5	26.3	-3.5	1.3
30	1.681	1.677	1.702	25.7	30.9	-4.3	0.9
40	1.633	1.630	1.656	35.3	40.7	-4.8	0.7
50	1.585	1.584	1.610	44.8	50.3	-5.2	0.2
60	1.537	1.536	1.562	54.8	60.3	-5.2	0.2
70	1.489	1.488	1.515	64.6	70.3	-5.4	0.3
80	1.441	1.440	1.467	74.6	80.3	-5.4	0.3
85	1.417	1.415	1.443	79.6	85.5	-5.4	0.5
90	1.393	1.391	1.419	84.6	90.5	-5.4	0.5
100	1.345	1.338	1.367	95.5	101.5	-4.5	1.5
110	1.297	1.289	1.319	105.5	111.7	-4.5	1.7
120	1.249	1.241	1.272	115.3	121.7	-4.8	1.7
125	1.225	1.218	1.250	119.8	126.5	-5.2	1.5
130	1.201	1.190	1.226	124.8	132.3	-5.2	2.3

3.4.16 Digital Rheostat Specifications

V_{DDA} = 2.3 V to 5.5 V, T_A = -40 °C to +105 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Counter Frequency	f_{DR_CLK}	The counter is determined by user's selection	0	-	25	MHz
Rheostat Switch Speed [2]	f_{DR_SWITCH}	V_A = 5.0 V, V_B = 0 V, ±1 LSB Error Band	-	-	100	kHz

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Rheostat Settling Time	t_{SETTLE}	Code change from 0 to 1023		-	-	5.1	µs
		±1 LSB code change [3]		-	-	0.4	
Rheostat Pin Voltage Range	V_{RH}	Voltage between Any (A or B) Pins and GND		0	-	VDDA	V
Digital Rheostat Resistance	R_{RH}	Full Resistance with all Switches Open [1]		92	100	113	kΩ
Minimal Rheostat Resistance	R_{RH_MIN}	Code = 0x000	V_{DDA} < 3 V	60	-	152	Ω
			V_{DDA} ≥ 3 V	46	-	84	
Number of Taps				-	-	1024	
Mismatch between Rheostats	R_{MATCH}	Code = 0x3FF, T_A = +25 °C		-	0.033	-	%
Step Resistance	R_{STEP}			-	98.7	-	Ω
Maximum Current through Rheostat	I_{POT_MAX}	T_A = +25 °C		-	-	2	mA
Resistor Noise Voltage	e_{SW_N}	R_{AB} = 25 kΩ, f = 1 kHz		-	30	-	nV/√Hz
Maximum Capacitance on RHx_A, RHx_B Pins (Respect to GND)	C_{POT}	All switches are ON, f = 200 kHz	RHx_A	-	21	-	pF
			RHx_B	-	21	-	
Zero-Scale Error	Error ZScale	Code = 0x000		-	0.96	1.50	LSB
Integral Non-linearity	INL	V_{RHxA} - V_{RHx_B} = 1 V		-3.0	-	+2.0	LSB
Differential Non-linearity	DNL	V_{RHxA} - V_{RHx_B} = 1 V	V_{DDA} < 3 V	-1.2	-	+1.2	LSB
			V_{DDA} ≥ 3 V	-0.8	-	+0.8	
Bandwidth -3dB (C_{LOAD} = 30 pF)	BW_{CAP}	R_{RH} < 12.5 kΩ		-	167	-	kHz
		R_{RH} = 12.5 kΩ to 25 kΩ		-	85	-	
		R_{RH} = 25 kΩ to 50 kΩ		-	44	-	
		R_{RH} = 50 kΩ to 100 kΩ		-	23	-	
Resistance Temperature Coefficient	αR(T)	V_{RHxA} - V_{RHx_B} = 1 V		-84	0	166	ppm/°C

[1] The actual digital rheostat value can be calculated using calibration data from the NVM (see section 14.3 Calculating Actual Rheostat Resistance).

[2] Includes internal timing. External circuits should be counted separately.

[3] Guaranteed by design, not tested in production.

4. IO Pins

The SLG47001-E has a total of 6 GPIOs (10 GPIOs for SLG47003-E), and 5 GPI pins which can function as either user-defined inputs or outputs.

4.1 GPI Pins

The five GPIs serve as “General Purpose Input” pins.

4.1.1 GPI Structure (GPI0, RH0_A/GPI1, RH0_B/GPI2, RH1_A/GPI4, RH1_B/GPI3)

IN_MODE[1:0]
00b: Digital Input w/o Schmitt Trigger (WOSMT_EN = 1, OE = 0)
01b: Digital Input with Schmitt Trigger (SMT_EN = 1, OE = 0)
10b: Low-voltage Digital Input (LV_EN = 1, OE = 0)
11b: Analog IO

Note1:
- “OE” cannot be selected by user.
- “OE” is a Connection Matrix Output.
- “Digital IN” is a Connection Matrix Input.

Note2:
167 Ω can vary over PVT (for reference only).

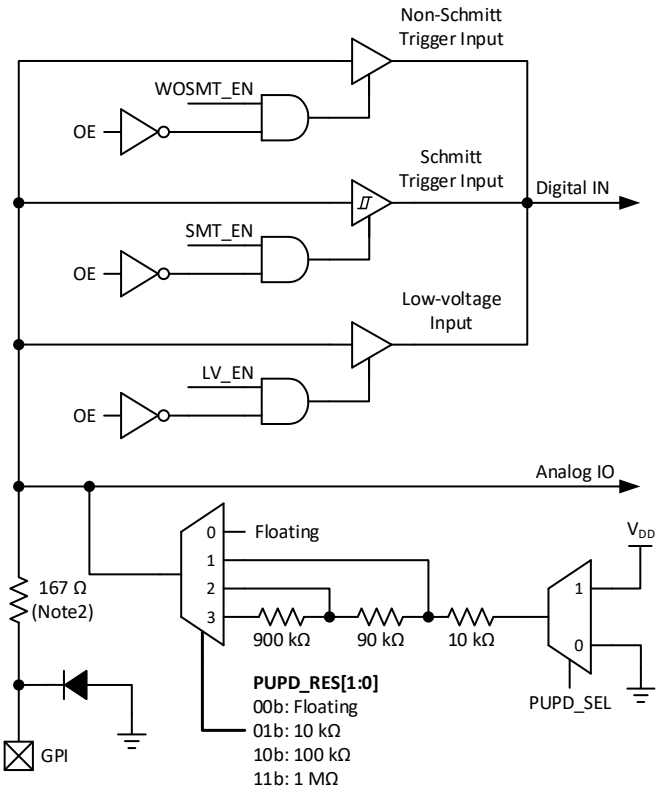


Figure 5. GPI Structure Diagram

4.2 GPIO Pins

GPIO0 to GPIO5 (GPIO0 to GPIO9 for SLG47003-E) serve as “General Purpose IO” pins. The input function of GPIO shared with I²C virtual inputs. See section 5.3 Connection Matrix Virtual Inputs.

4.2.1 GPIO with I²C Mode IO Structure (SCL/GPIO4, SDA/GPIO5)

IN_MODE[1:0]
00b: Digital Input w/o Schmitt Trigger (WOSMT_EN = 1, OE = 0)
01b: Reserved
10b: Low-voltage Digital Input (LV_EN = 1, OE = 0)
11b: Reserved

Reg[742] = 1: Open-drain NMOS for SCL/GPIO
Reg[749] = 1: Open-drain NMOS for SDA/GPIO

Note1:
- “OE” cannot be selected by user and is controlled by register.
- “Digital IN” is a Matrix Input.
- SCL/GPIO and SDA/GPIO do not support Push-pull mode.
- It is possible to apply a voltage higher than V_{DD} to SCL and SDA pins, however it must not exceed 5.5 V.

Note2:
172 Ω can vary over PVT (for reference only).

Note3:
Pull-up / Pull-down resistors are deactivated only when I²C block is disabled.

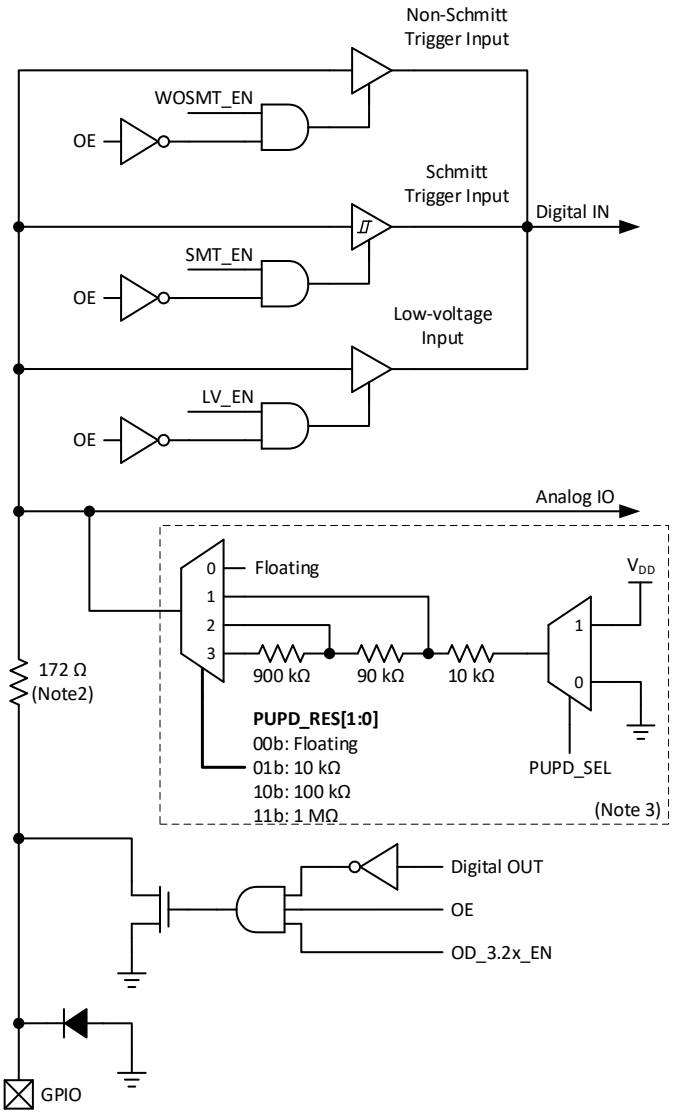


Figure 6. GPIO with I²C Mode IO Structure Diagram

4.2.2 GPIO with Matrix OE IO Structure (GPIO0 – GPIO3)

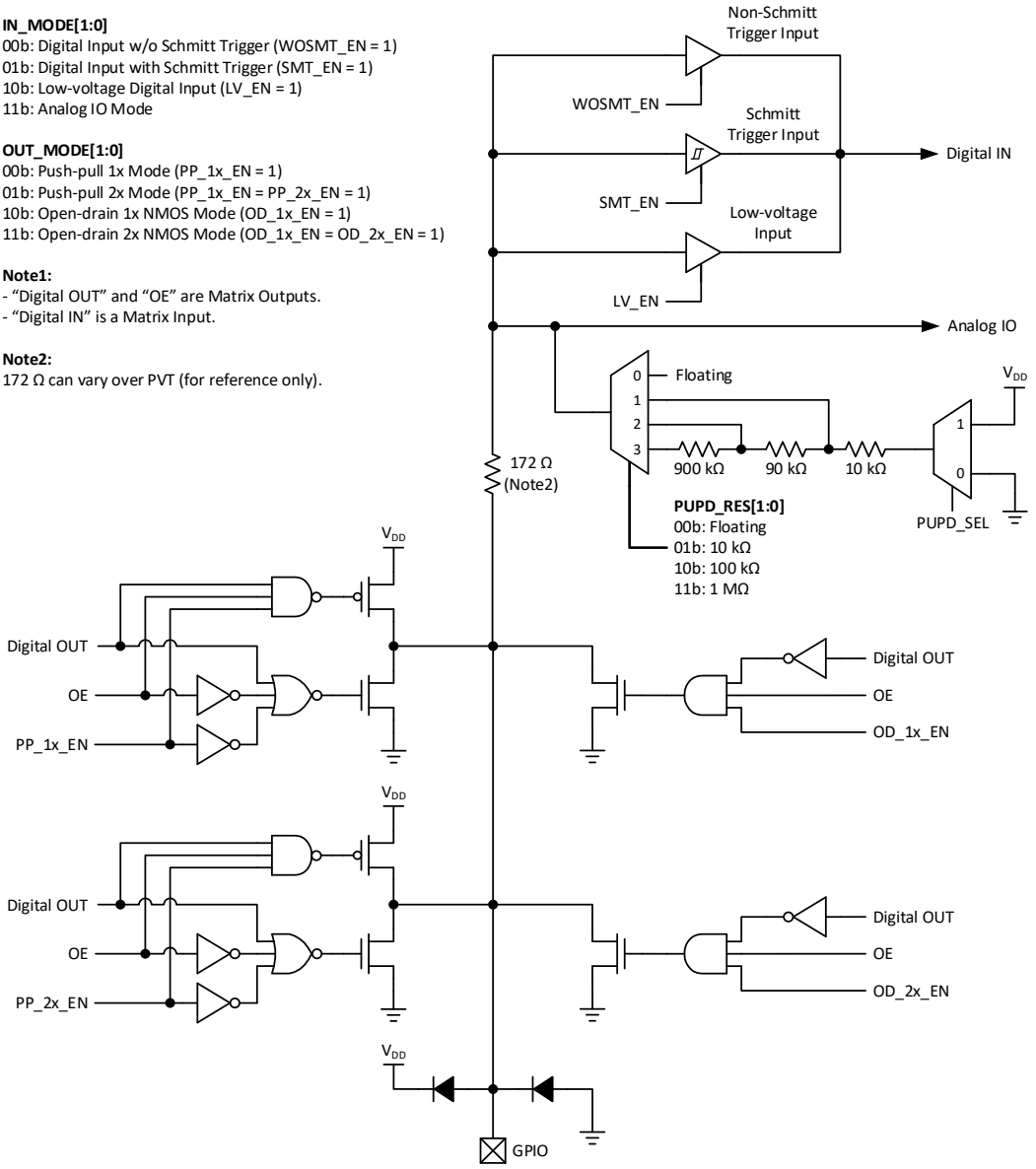


Figure 7. GPIO with Matrix OE IO Structure Diagram

4.2.3 GPIO with Register OE IO Structure (GPIO6 – GPIO9)

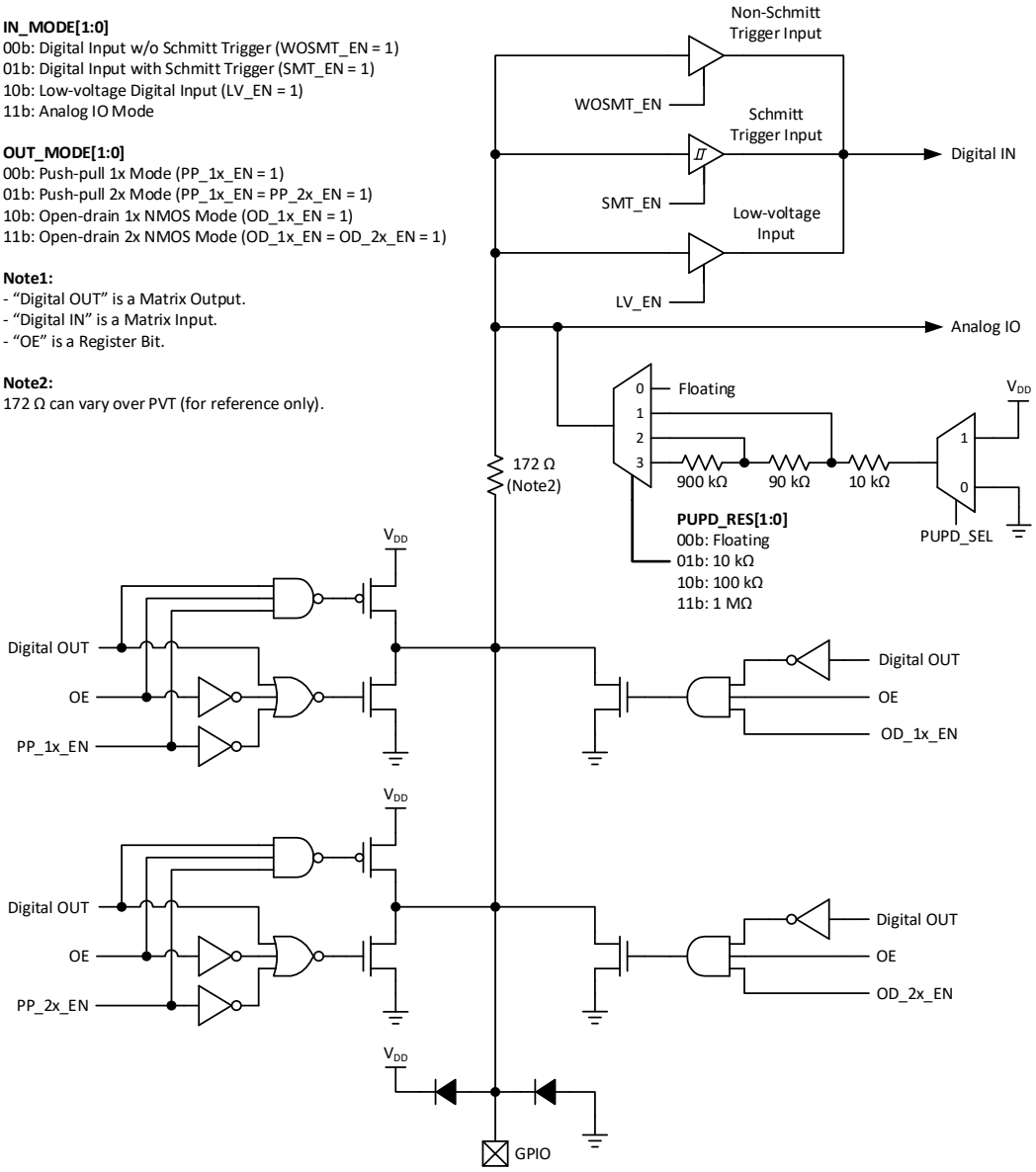


Figure 8. GPIO with Register OE IO Structure Diagram

Note that GPIO6 to GPIO9 are available in 24-pin STQFN package option (SLG47003-E) only.

4.3 Pull-Up/Pull-Down Resistors

All IO pins have the option for user-selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either pull-up or pull-down connections.

4.4 Fast Pull-Up/Pull-Down during Power-Up

During power-up, the pull-up/pull-down resistance of IOs is set to 2.6 kΩ initially and then it will switch to the normal setting values. This function is enabled by the IO_FAST_PUPD_EN bit (Reg[730]).

4.5 Typical Performance of IOs

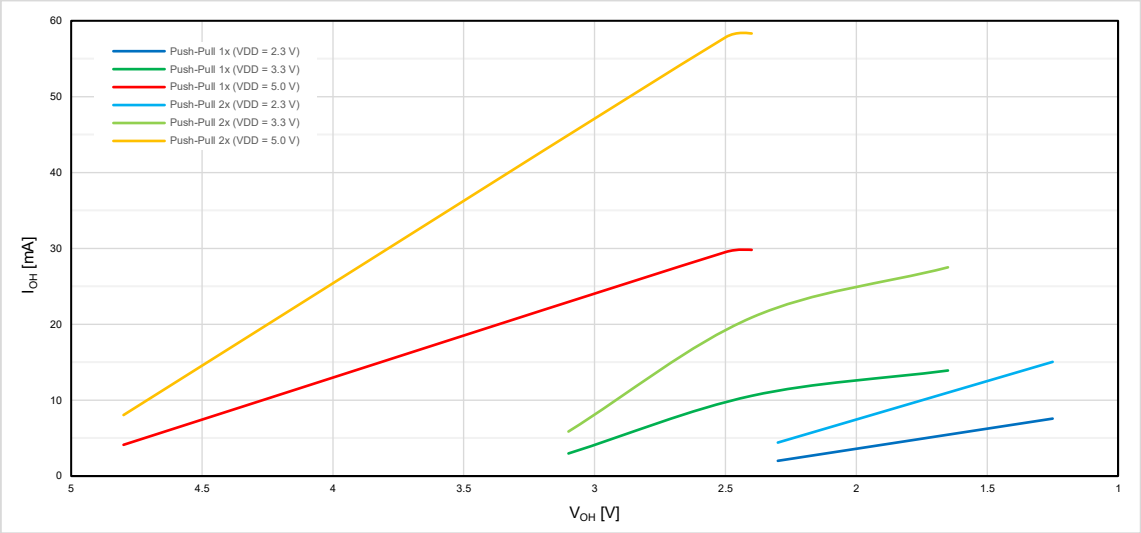


Figure 9. Typical I_{OH} vs. V_{OH} in Push-Pull Mode at T_A = +25 °C

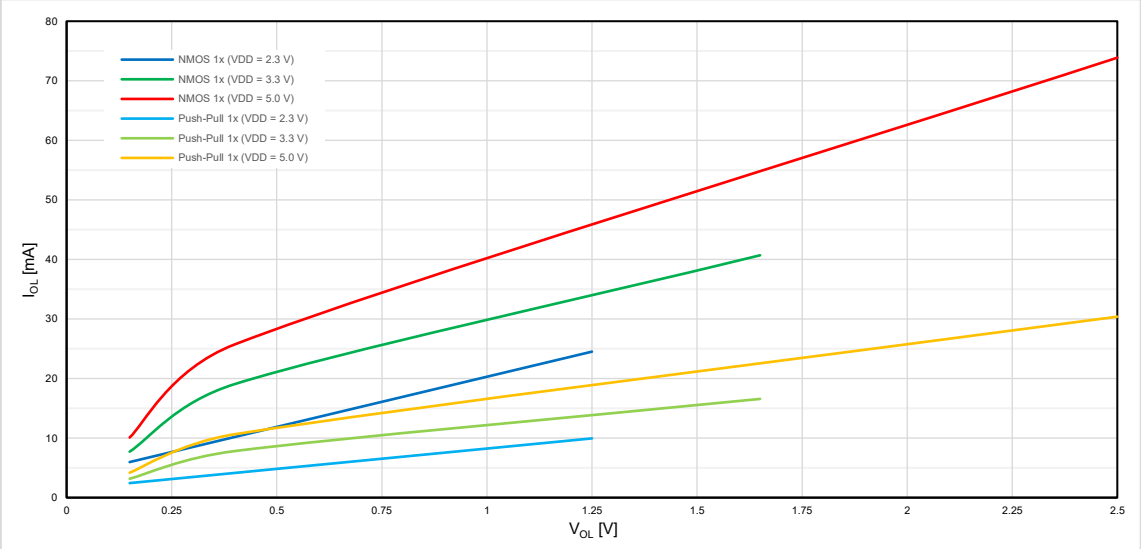


Figure 10. Typical I_{OL} vs. V_{OL} = 0.15 V to 2.5 V, 1x Drive Mode at T_A = +25 °C

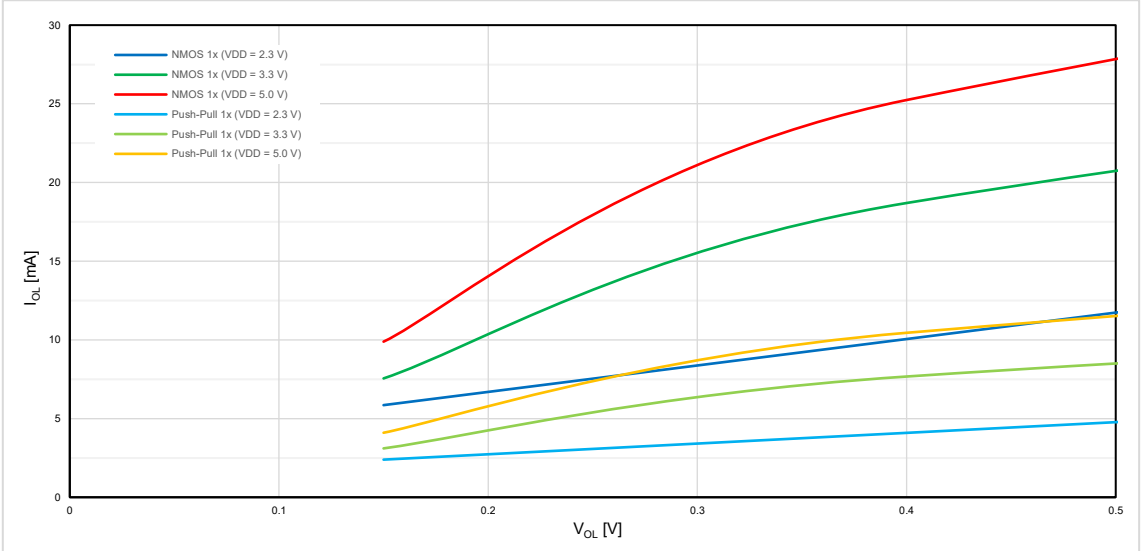


Figure 11. Typical I_{OL} vs. V_{OL} = 0.15 V to 0.5 V, 1x Drive Mode at T_A = +25 °C

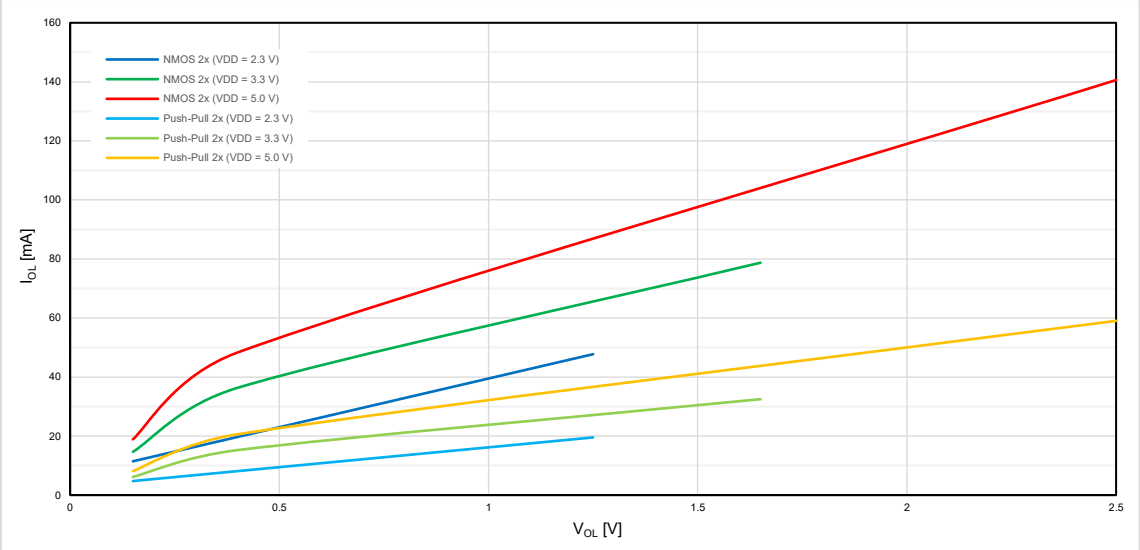


Figure 12. Typical I_{OL} vs. V_{OL} = 0.15 V to 2.5 V, 2x Drive Mode at T_A = +25 °C

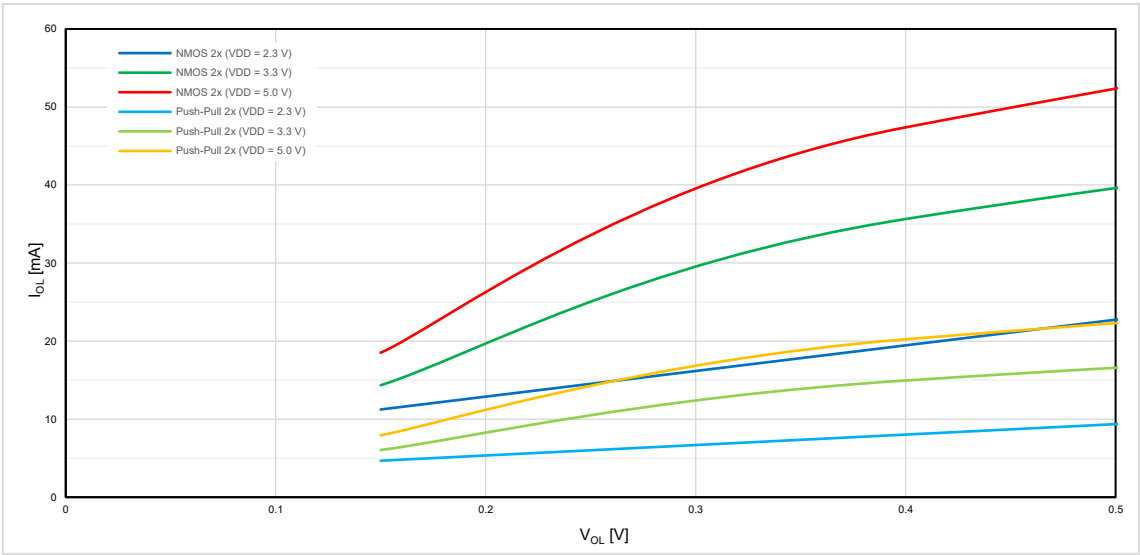


Figure 13. Typical I_{OL} vs. V_{OL} = 0.15 V to 0.5 V, 2x Drive Mode at T_A = +25 °C

5. Connection Matrix

The connection matrix in the SLG47001-E/03-E establishes the internal routings between the functional macrocells of the device. The connection matrix configuration registers are programmed onto the one-time programmable (OTP) NVM cell during ATE test at factory. The output of each functional macrocell within the SLG47001-E/03-E has a specific digital bit code assigned to it that is either set to active (High) or inactive (Low) based on the design that is created. Once the 1552 register bits within the SLG47001-E/03-E are programmed, a fully custom circuit will be created.

The connection matrix has 64 inputs and 75 outputs (79 outputs for SLG47003-E). Each of the 64 inputs to the connection matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources and V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

Matrix Input Signal	N
GND	0
2-bit LUT0/DFF0 Output	1
2-bit LUT1/DFF1 Output	2
⋮	⋮
Reserved	62
VDD	63

Matrix Input / Matrix Output	N	0	1	2	. . . .	79
	Register	[5:0]	[11:6]	[17:12]		[479:474]
	Function	IN0 of 2-bit LUT0 or CLK Input of DFF0	IN1 of 2-bit LUT0 or Data Input of DFF0	IN0 of 2-bit LUT1 or CLK Input of DFF1		GPIO7 Digital Output

Figure 14. Connection Matrix

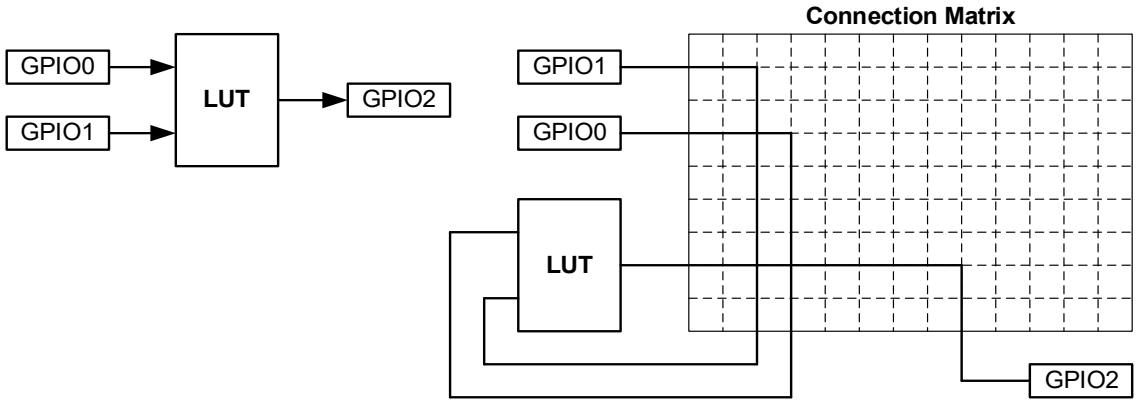


Figure 15. Connection Matrix Usage Example

5.1 Connection Matrix Input Table

Table 3. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	2-bit LUT0/DFF0 Output	0	0	0	0	0	1
2	2-bit LUT1/DFF1 Output	0	0	0	0	1	0
3	3-bit LUT0/DFF2 Output	0	0	0	0	1	1
4	3-bit LUT1/DFF3 Output	0	0	0	1	0	0
5	3-bit LUT2/DFF4 Output	0	0	0	1	0	1
6	3-bit LUT3/DFF5 Output	0	0	0	1	1	0
7	3-bit LUT4/DFF6/SR0 Output	0	0	0	1	1	1
8	3-bit LUT5/DFF7/SR1 Output	0	0	1	0	0	0
9	3-bit LUT6/DFF8/SR2 Output	0	0	1	0	0	1
10	3-bit LUT7/DFF9/SR3 Output	0	0	1	0	1	0
11	4-bit LUT0/DFF10 Output	0	0	1	0	1	1
12	CNT0 Output	0	0	1	1	0	0
13	3-bit LUT8/DFF11 Output	0	0	1	1	0	1
14	CNT1 Output	0	0	1	1	1	0
15	3-bit LUT9/DFF12 Output	0	0	1	1	1	1
16	CNT2 Output	0	1	0	0	0	0
17	3-bit LUT10/DFF13 Output	0	1	0	0	0	1
18	CNT3 Output	0	1	0	0	1	0
19	3-bit LUT11/DFF14 Output	0	1	0	0	1	1
20	CNT4 Output	0	1	0	1	0	0
21	3-bit LUT12/DFF15 Output	0	1	0	1	0	1
22	GPI of SCL/GPIO4 Pin or I^2C Virtual Input8	0	1	0	1	1	0
23	GPI of SDA/GPIO5 Pin or I^2C Virtual Input9	0	1	0	1	1	1
24	I^2C Virtual Input0	0	1	1	0	0	0
25	I^2C Virtual Input1	0	1	1	0	0	1
26	EPG OUT2 or I^2C Virtual Input2	0	1	1	0	1	0
27	EPG OUT3 or I^2C Virtual Input3	0	1	1	0	1	1
28	EPG OUT4 or I^2C Virtual Input4	0	1	1	1	0	0

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
29	EPG OUT5 or I²C Virtual Input5	0	1	1	1	0	1
30	EPG OUT6 or I²C Virtual Input6	0	1	1	1	1	0
31	EPG OUT7 or I²C Virtual Input7	0	1	1	1	1	1
32	GPI1 of RH0_A Pin	1	0	0	0	0	0
33	GPI2 of RH0_B Pin	1	0	0	0	0	1
34	GPI3 of RH1_B Pin	1	0	0	0	1	0
35	GPI4 of RH1_A Pin	1	0	0	0	1	1
36	GPI0 Digital Input	1	0	0	1	0	0
37	GPIO0 Digital Input	1	0	0	1	0	1
38	GPIO1 Digital Input	1	0	0	1	1	0
39	GPIO2 Digital input	1	0	0	1	1	1
40	GPIO3 Digital input	1	0	1	0	0	0
41	GPIO6 Digital Input [1]	1	0	1	0	0	1
42	GPIO7 Digital Input [1]	1	0	1	0	1	0
43	GPIO8 Digital Input [1]	1	0	1	0	1	1
44	GPIO9 Digital Input [1]	1	0	1	1	0	0
45	Programmable Delay Edge-Detect Output	1	0	1	1	0	1
46	Oscillator0 Output0	1	0	1	1	1	0
47	Oscillator0 Output1	1	0	1	1	1	1
48	Oscillator1 Output	1	1	0	0	0	0
49	MS-ACMP Output0	1	1	0	0	0	1
50	MS-ACMP Output1	1	1	0	0	1	0
51	MS-ACMP Output2	1	1	0	0	1	1
52	MS-ACMP Output3	1	1	0	1	0	0
53	MS-ACMP Output4	1	1	0	1	0	1
54	MS-ACMP Output5	1	1	0	1	1	0
55	MS-ACMP SYNC_RDY Output	1	1	0	1	1	1
56	Reserved	1	1	1	0	0	0
57	Reserved	1	1	1	0	0	1
58	POR	1	1	1	0	1	0

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
59	RH0 Overflow Flag	1	1	1	0	1	1
60	RH1 Overflow Flag	1	1	1	1	0	0
61	EPG OUT0	1	1	1	1	0	1
62	EPG OUT1	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1
[1] GPIO6 though GPIO9 are available in STQFN-24 package only.							

5.2 Connection Matrix Output Table

Table 4. Matrix Output Table

Matrix Output Number	Matrix Output Signal Function	Register Bit Address
0	IN0 of 2-bit LUT0 or CLK Input of DFF0	[5:0]
1	IN1 of 2-bit LUT0 or Data Input of DFF0	[11:6]
2	IN0 of 2-bit LUT1 or CLK Input of DFF1	[17:12]
3	IN1 of 2-bit LUT1 or Data Input of DFF1	[23:18]
4	IN0 of 3-bit LUT0 or CLK Input of DFF2	[29:24]
5	IN1 of 3-bit LUT0 or Data Input of DFF2	[35:30]
6	IN2 of 3-bit LUT0 or nRST (nSET) Input of DFF2	[41:36]
7	IN0 of 3-bit LUT1 or CLK Input of DFF3	[47:42]
8	IN1 of 3-bit LUT1 or Data Input of DFF3	[53:48]
9	IN2 of 3-bit LUT1 or nRST (nSET) Input of DFF3	[59:54]
10	IN0 of 3-bit LUT2 or CLK Input of DFF4	[65:60]
11	IN1 of 3-bit LUT2 or Data Input of DFF4	[71:66]
12	IN2 of 3-bit LUT2 or nRST (nSET) Input of DFF4	[77:72]
13	IN0 of 3-bit LUT3 or CLK Input of DFF5	[83:78]
14	IN1 of 3-bit LUT3 or Data Input of DFF5	[89:84]
15	IN2 of 3-bit LUT3 or nRST (nSET) Input of DFF5	[95:90]
16	IN0 of 3-bit LUT4, CLK Input of DFF6, or CLK Input of SR0	[101:96]
17	IN1 of 3-bit LUT4, Data Input of DFF6, or Data Input of SR0	[107:102]
18	IN2 of 3-bit LUT4, nRST (nSET) Input of DFF6, or nRST (nSET) Input of SR0	[113:108]
19	IN0 of 3-bit LUT5, CLK Input of DFF7, or CLK Input of SR1	[119:114]

Matrix Output Number	Matrix Output Signal Function	Register Bit Address
20	IN1 of 3-bit LUT5, Data Input of DFF7, or Data Input of SR1	[125:120]
21	IN2 of 3-bit LUT5, nRST (nSET) Input of DFF7, or nRST (nSET) Input of SR1	[131:126]
22	IN0 of 3-bit LUT6, CLK Input of DFF8, or CLK Input of SR2	[137:132]
23	IN1 of 3-bit LUT6, Data Input of DFF8, or Data Input of SR2	[143:138]
24	IN2 of 3-bit LUT6, nRST (nSET) Input of DFF8, or nRST (nSET) Input of SR2	[149:144]
25	IN0 of 3-bit LUT7, CLK Input of DFF9, or CLK Input of SR3	[155:150]
26	IN1 of 3-bit LUT7, Data Input of DFF9, or Data Input of SR3	[161:156]
27	IN2 of 3-bit LUT7, nRST (nSET) Input of DFF9, or nRST (nSET) Input of SR3	[167:162]
28	IN0 of 3-bit LUT8, CLK Input of DFF11, nRST Input of CNT0, Delay0 Input, or UP Input of FSM	[173:168]
29	IN1 of 3-bit LUT8, nRST (nSET) Input of DFF11, nRST Input of CNT0, DLY_IN Input of DLY0, or EXT_CLK Input of CNT0	[179:174]
30	IN2 of 3-bit LUT8, Data Input of DFF11, nRST Input of CNT0, or DLY_IN Input of DLY0	[185:180]
31	IN0 of 3-bit LUT9, CLK Input of DFF12, nRST Input of CNT0, or DLY_IN Input of DLY1	[191:186]
32	IN1 of 3-bit LUT9, nRST (nSET) Input of DFF12, nRST Input of CNT1, or DLY_IN Input of DLY1	[197:192]
33	IN2 of 3-bit LUT9, Data Input of DFF12, nRST Input of CNT1, or DLY_IN Input of DLY1	[203:198]
34	IN0 of 3-bit LUT10, CLK Input of DFF13, nRST Input of CNT2, or DLY_IN Input of DLY2	[209:204]
35	IN1 of 3-bit LUT10, nRST (nSET) Input of DFF13, nRST Input of CNT2, or DLY_IN Input of DLY2	[215:210]
36	IN2 of 3-bit LUT10, Data Input of DFF13, nRST Input of CNT2, or DLY_IN Input of DLY2	[221:216]
37	IN0 of 3-bit LUT11, CLK Input of DFF14, nRST Input of CNT3, or DLY_IN Input of DLY3	[227:222]
38	IN1 of 3-bit LUT11, nRST (nSET) Input of DFF14, nRST Input of CNT3, or DLY_IN Input of DLY3	[233:228]
39	IN2 of 3-bit LUT11, Data Input of DFF14, nRST Input of CNT3, or DLY_IN Input of DLY3	[239:234]
40	IN0 of 3-bit LUT12, CLK Input of DFF15, nRST Input of CNT4, or DLY_IN Input of DLY4	[245:240]
41	IN1 of 3-bit LUT12, nRST (nSET) Input of DFF15, nRST Input of CNT4, or DLY_IN Input of DLY4	[251:246]
42	IN2 of 3-bit LUT12, Data Input of DFF15, nRST Input of CNT1, or DLY_IN Input of DLY4	[257:252]
43	IN0 of 4-bit LUT0 or CLK Input of DFF10	[263:258]
44	IN1 of 4-bit LUT0 or Data Input of DFF10	[269:264]
45	IN2 of 4-bit LUT0 or nRST (nSET) Input of DFF10	[275:270]
46	IN3 of 4-bit LUT0	[281:276]
47	Programmable Delay/Edge Detect Input	[287:282]
48	GPO OD Digital Output (SDA/GPIO5 Pin)	[293:288]

Matrix Output Number	Matrix Output Signal Function	Register Bit Address
49	GPO OD Digital Output (SCL/GPIO4 Pin)	[299:294]
50	GPIO0 Digital Output	[305:300]
51	GPIO0 Digital Output OE	[311:306]
52	GPIO1 Digital Output	[317:312]
53	GPIO1 Digital Output OE	[323:318]
54	GPIO2 Digital Output	[329:324]
55	GPIO2 Digital Output OE	[335:330]
56	GPIO3 Digital Output	[341:336]
57	GPIO3 Digital Output OE	[347:342]
58	Sink/Source Buffer Enable	[353:348]
59	OpAmp V_{REF} Enable	[359:354]
60	Digital Rheostat0 Counter UP/DOWN	[365:360]
61	Digital Rheostat1 Counter UP/DOWN	[371:366]
62	Analog Switch (ASW) Enable	[377:372]
63	OpAmp0 (OpAmp ACMP0) Enable	[383:378]
64	OpAmp1 (OpAmp ACMP1) Enable	[389:384]
65	MS-ACMP Enable	[395:390]
66	MS-ACMP LATCH nRST Input	[401:396]
67	OSC0 Enable	[407:402]
68	EPG CLK Input	[413:408]
69	EPG nRST Input	[419:414]
70	Digital Rheostat0 Counter CLK Input	[425:420]
71	Digital Rheostat0 Counter Reload Input	[431:426]
72	Digital Rheostat1 Counter CLK Input	[437:432]
73	Digital Rheostat1 Counter Reload Input	[443:438]
74	OSC1 Enable	[449:444]
75	MS-ACMP External CLK Input	[455:450]
76	GPIO6 Digital Output [1]	[461:456]
77	GPIO7 Digital Output [1]	[467:462]
78	GPIO8 Digital Output [1]	[473:468]
79	GPIO9 Digital Output [1]	[479:474]

Matrix Output Number	Matrix Output Signal Function	Register Bit Address
[1] GPIO6 though GPIO9 are available in STQFN-24 package only.		

5.3 Connection Matrix Virtual Inputs

The connection matrix inputs come from the outputs of various digital macrocells on the device. As shown in Table 5, ten of the connection matrix inputs have a special characteristic that the states of these 10 signal lines come from corresponding data bits written as a register value through I²C. This gives the user the ability to write data through the serial interface, and have this information translated to the inputs of other macrocells through the connection matrix. The I²C addresses for reading and writing these register values are 0x3E and 0x3F.

An I²C write command to these register bits set the signal values going into the connection matrix to the desired state. A read command to these register bits returns either the original data values coming from the NVM bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Table 5. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Address
24	I²C Virtual Input0	[504]
25	I²C Virtual Input1	[505]
26	I²C Virtual Input2	[506]
27	I²C Virtual Input3	[507]
28	I²C Virtual Input4	[508]
29	I²C Virtual Input5	[509]
30	I²C Virtual Input6	[510]
31	I²C Virtual Input7	[511]
22	I²C Virtual Input8	[502]
23	I²C Virtual Input9	[503]

Note that I²C Virtual Input8 and I²C Virtual Input9 are available only when I²C function is not used for any other functions.

5.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the connection matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value through I²C. This option, called “Connection Matrix Virtual Outputs”, allows the user to read the value of each macrocell output. The I²C addresses for reading these register values are from 0x3C through 0x43. These registers are read-only except for the Virtual Input register bits at ADDR 0x3E and 0x3F.

6. Combination Function Macrocells

The SLG47001-E/03-E has 11 combination function macrocells that can serve more than one logic or timing function. Each macrocell can serve as a lookup table (LUT), or another logic or timing function.

See the list below for the functions that can be implemented in these macrocells:

- Two macrocells that can serve as either 2-bit LUTs or DFFs.
- Four macrocells that can serve as either 3-bit LUTs or DFFs with reset/set input.
- Four macrocells that can serve as either 3-bit LUTs, DFFs with reset/set input or SR.
- One macrocell that can serve as either a 4-bit LUT or a DFF with reset/set input.

The inputs and the outputs of those combination function macrocells are configured by the connection matrix with specific logic functions being defined by the state of configuration bits.

When the macrocell is used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

6.1 2-bit LUT or D Flip-Flop Macrocells

There are two macrocells that can serve as either 2-bit LUTs or DFFs. When the LUT function is selected, the 2-bit LUT takes two input signals from the connection matrix outputs (CMOs) and produces a single output, which goes back to the connection matrix input (CMI). When this macrocell is used to implement DFF function, the two input signals from the connection matrix go to data (D) and clock (CLK) inputs for the DFF with the output going back to the connection matrix input. The DFFx_LAT_SEL registers select either DFF or LATCH function. The operations of DFF and LATCH functions are described below:

- **DFF**: Q = D at a rising edge of CLK, otherwise Q remains its previous value.
- **LATCH**: Q = D when CLK is low, otherwise Q remains its previous value (D has no effect when CLK is high).

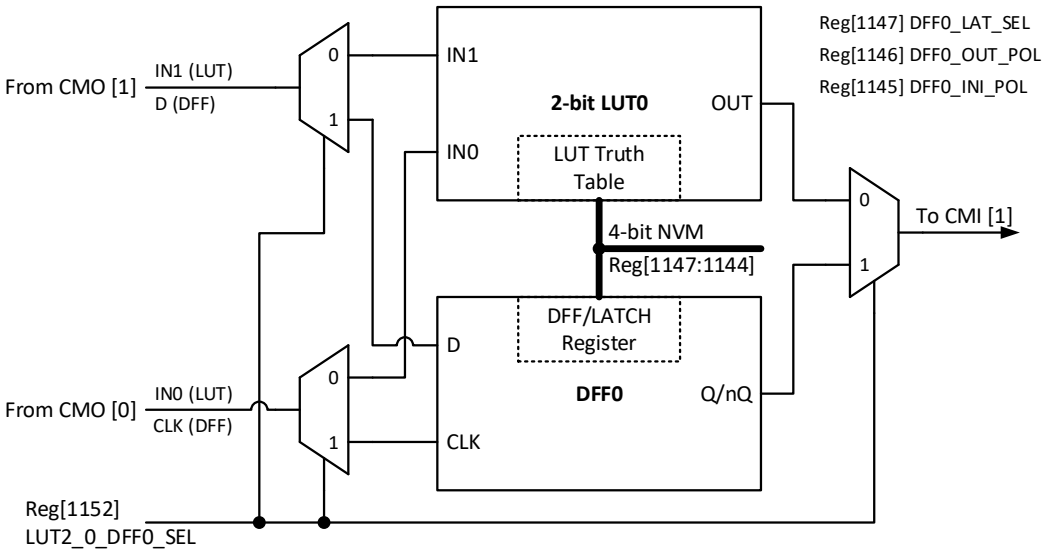


Figure 16. 2-bit LUT0 or DFF0

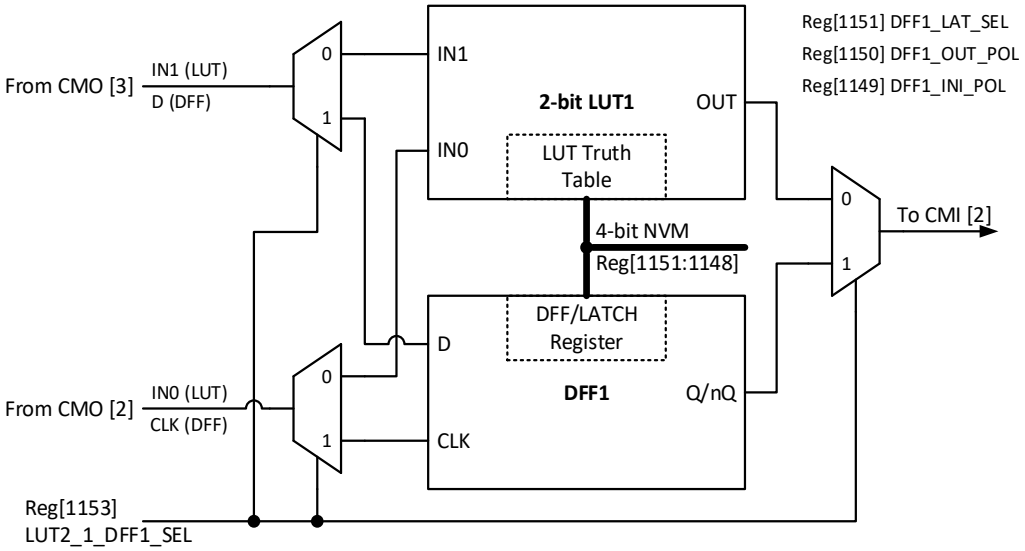


Figure 17. 2-bit LUT1 or DFF1

6.1.1 2-bit LUT or D Flip-Flop Macrocell Used as 2-bit LUT

When these macrocells are configured as LUT functions, 4-bit registers are used to define their output functions:

- 2-bit LUT0 output is defined by Reg[1147:1144]
- 2-bit LUT1 output is defined by Reg[1151:1148].

Table 6. 2-bit LUT0 and 2-bit LUT1 Truth Table

IN1	IN0	2-bit LUT0 OUT	2-bit LUT1 OUT
0	0	Reg[1144]	Reg[1148]
0	1	Reg[1145]	Reg[1149]
1	0	Reg[1146]	Reg[1150]
1	1	Reg[1147]	Reg[1151]

Table 7 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 7. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

6.2 3-bit LUT or D Flip-Flop with Reset/Set Macrocells

There are 4 macrocells that can serve as either 3-bit LUTs or DFFs with reset/set inputs. When the LUT function is selected, the 3-bit LUTs each take three input signals from the connection matrix outputs (CMOs) and produce a single output, which goes back to the connection matrix input (CMI). When DFF function is selected, the three input signals from the connection matrix outputs are connected to data (D), clock (CLK), and reset/set (nRST/nSET) inputs, and the output goes back to the connection matrix input. It is possible to select the polarity of the reset/set input of DFF/LATCH macrocell. The DFFx_RST_POL bit selects either active-high (RST/SET) or active-low (nRST/nSET) options. The DFFx_LAT_SEL registers select either DFF or LATCH function. The operations of DFF and LATCH functions are described below:

- **DFF**: Q = D at a rising edge of CLK, otherwise Q remains its previous value.
- **LATCH**: Q = D when CLK is low, otherwise Q remains its previous value (D has no effect when CLK is high).

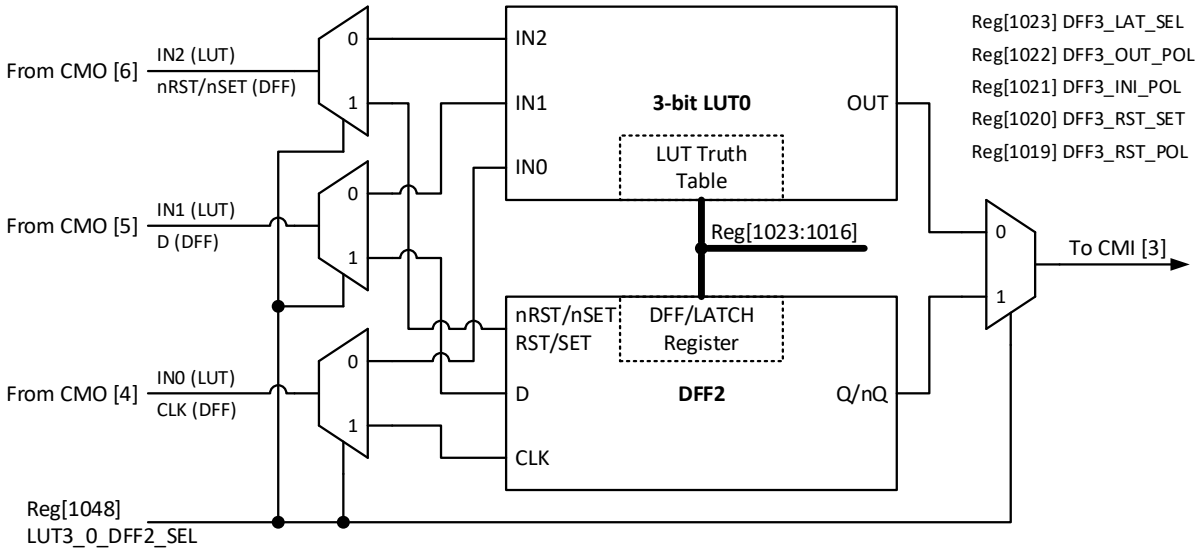


Figure 18. 3-bit LUT0 or DFF2

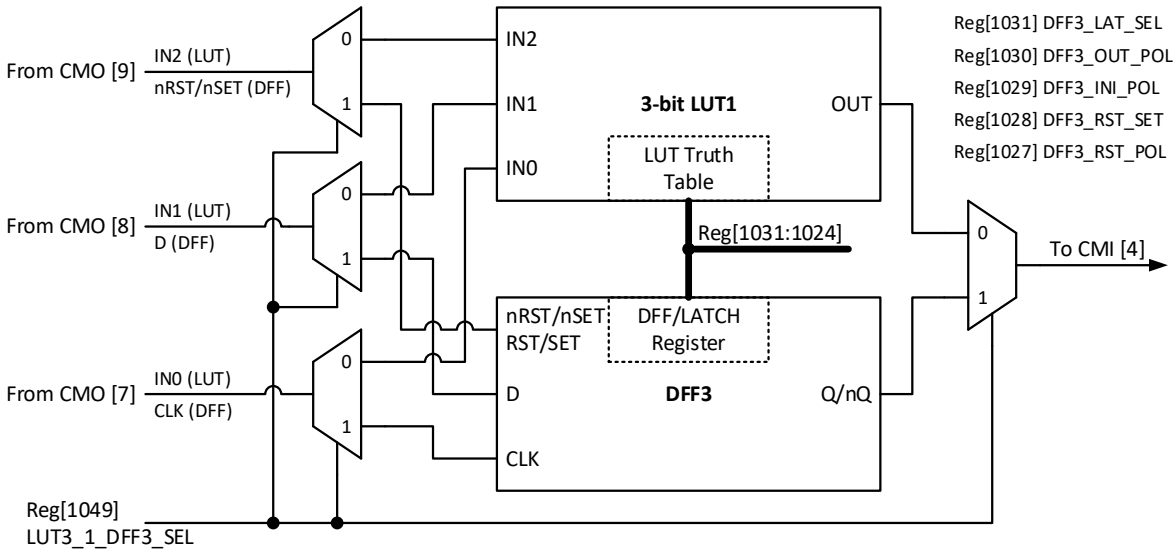


Figure 19. 3-bit LUT1 or DFF3

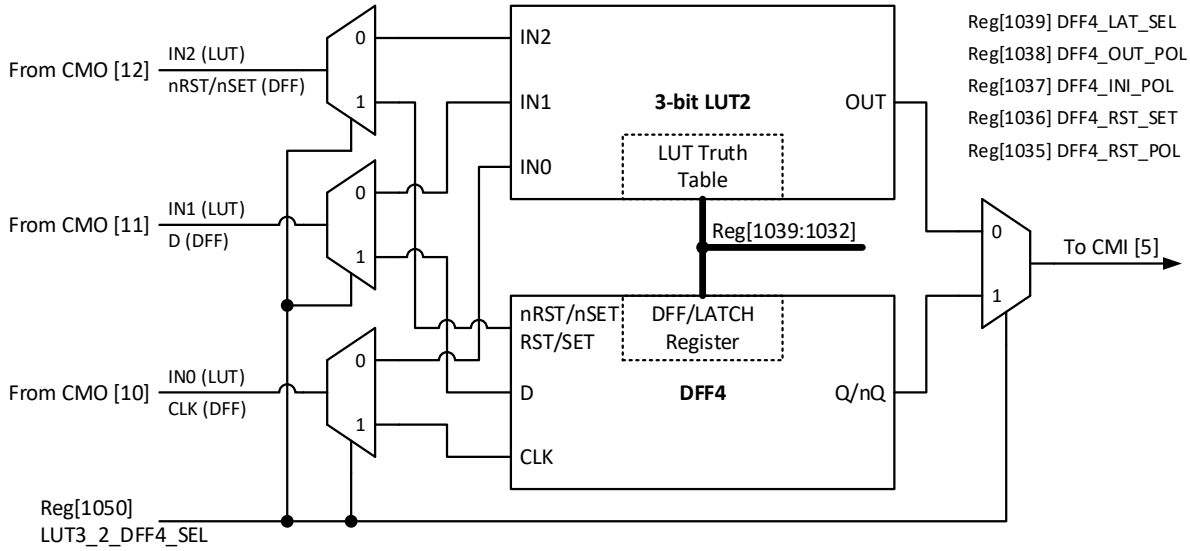


Figure 20. 3-bit LUT2 or DFF4

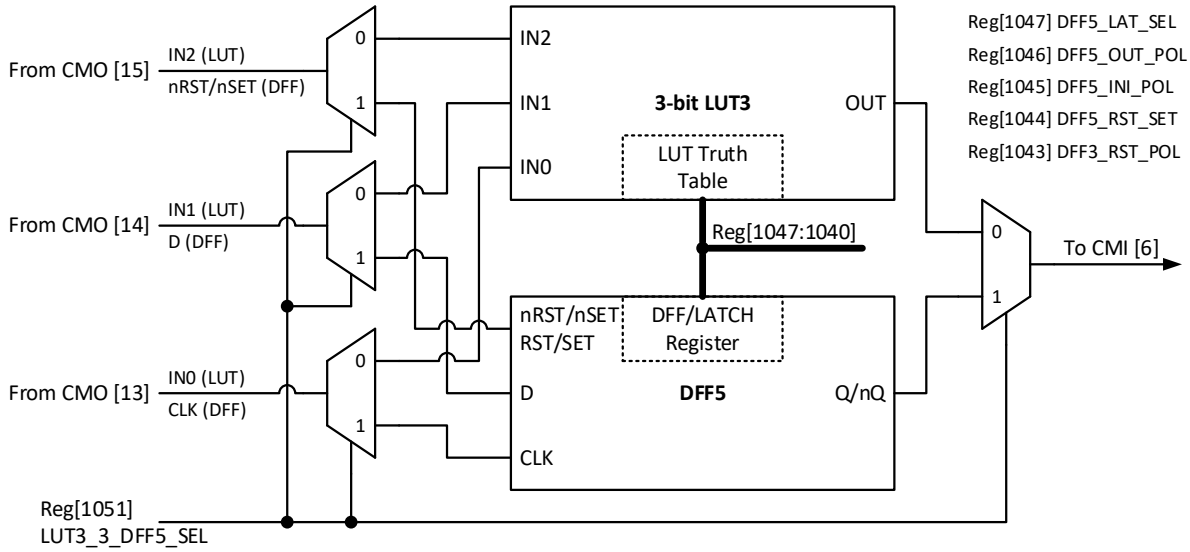


Figure 21. 3-bit LUT3 or DFF5

6.3 3-bit LUT or D Flip-Flop with Reset/Set or Shift Register Macrocells

There are four macrocells that can serve as 3-bit lookup tables (LUT), D flip-flop/latches (DFF/LATCH) or shift registers (SR). It is also possible to select the functionality (LUT, DFF/LATCH, or SR) of the macrocell and the logic polarity of the output (either active-high or active-low) by registers. When the macrocell is configured as a LUT, it takes three input signals from the connection matrix outputs (CMOs) and produces a single output, which goes back into the connection matrix input (CMI).

When DFF/LATCH function is selected, the three input signals from the connection matrix outputs are connected to data (D), clock (CLK) and reset/set (nRST/nSET) inputs of the DFF/LATCH, and the output goes back to the connection matrix input. It is possible to select the polarity of the reset/set input of the DFF/LATCH macrocell. The DFFx_RST_POL bit selects either active-high (RST/SET) or active-low (nRST/nSET) options. The DFFx_LAT_SEL registers select either DFF or LATCH function. The operations of the DFF and LATCH functions are described below:

- **DFF**: Q = D at a rising edge of CLK, otherwise Q remains its previous value.
- **LATCH**: Q = D when CLK is low, otherwise Q remains its previous value (D has no effect when CLK is high).

When the macrocell is configured as a SR, the three input signals from the connection matrix outputs are connected to the data (D), the clock (CLK) and the reset/set (nRST/nSET) inputs of the SR and its output is fed back to the connection matrix input. It is possible to select the polarity of the reset/set input of the SR macrocell by the DFFx_RST_POL bits. The input data (D) is written onto the MSB and the length of the SR (up to 8 bits per memory cell) is selected by the SRx_OUT_SEL[2:0] registers. If the length of the SR is one, it means a DFF/LATCH function is selected.

The data in the shift registers at ADDR 0x88, 0x8A, 0x8C, 0x8E can be read or written through I²C. Note that the data (D) and the clock (CLK) inputs should remain unchanged while the I²C controller is reading the data from the shift registers. Otherwise, the data in the shift register could be changed while the SR data are being read through I²C. Since the data are copied from the SR to the internal I²C buffer with the internal clock signal, there could be a situation that the setup time (t_{SETUP}) and the hold time (t_{HOLD}) will not be met for the internal clock signal. As a result, the data of the SR will be read incorrectly through I²C. When the SR clock is much slower than the I²C clock speed, a host processor can read the SR data multiple times to filter out the incorrect reading. It is also possible to change the DFF/SR value using I²C write command.

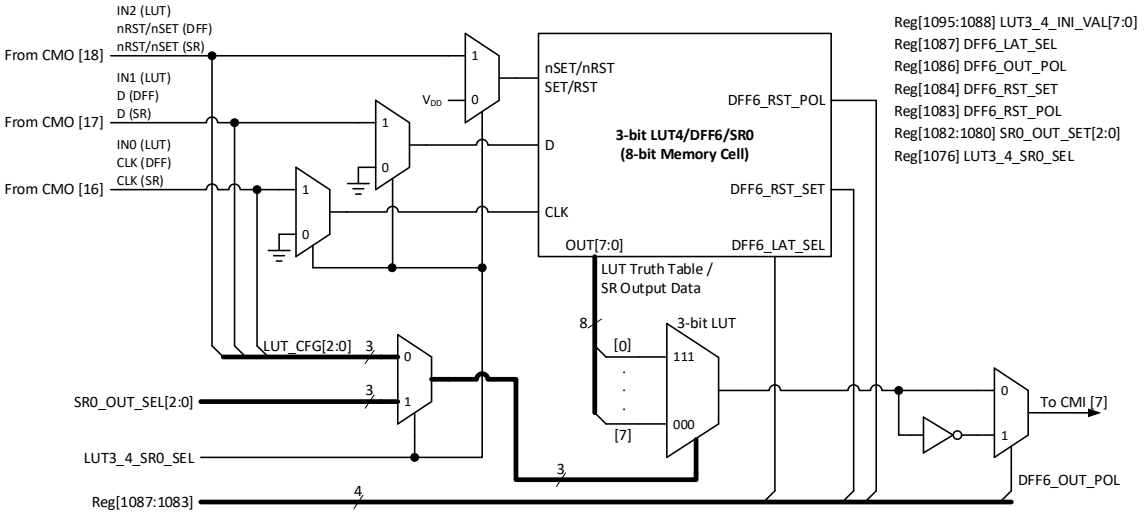


Figure 22. 3-bit LUT4, DFF6 or SR0

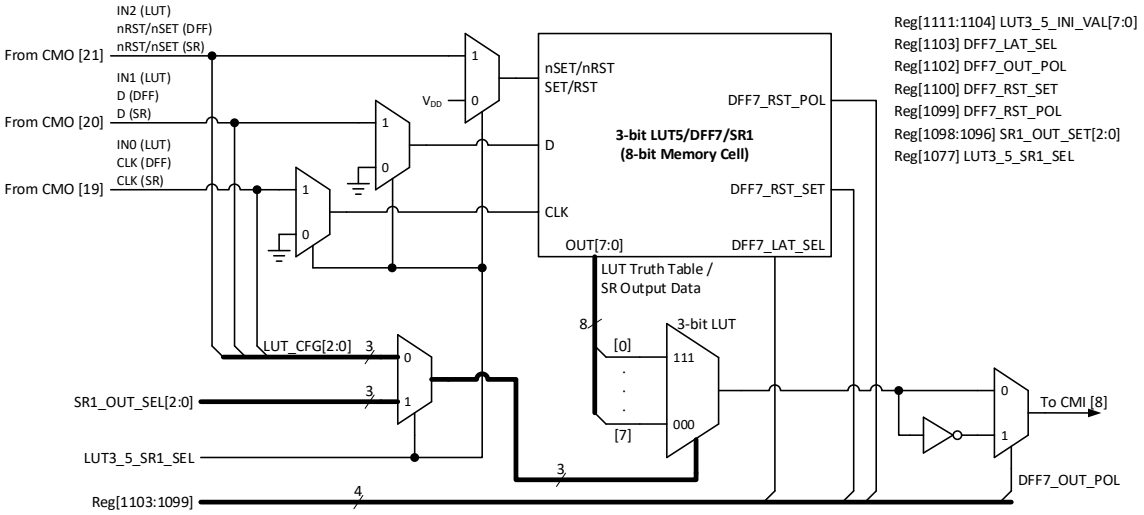


Figure 23. 3-bit LUT5, DFF7 or SR1

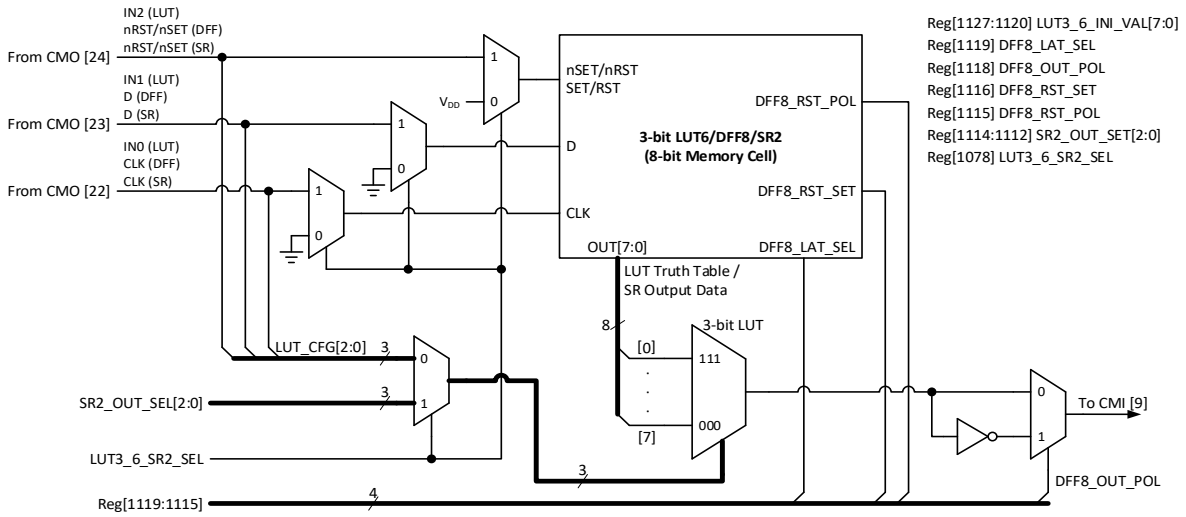


Figure 24. 3-bit LUT6, DFF8 or SR2

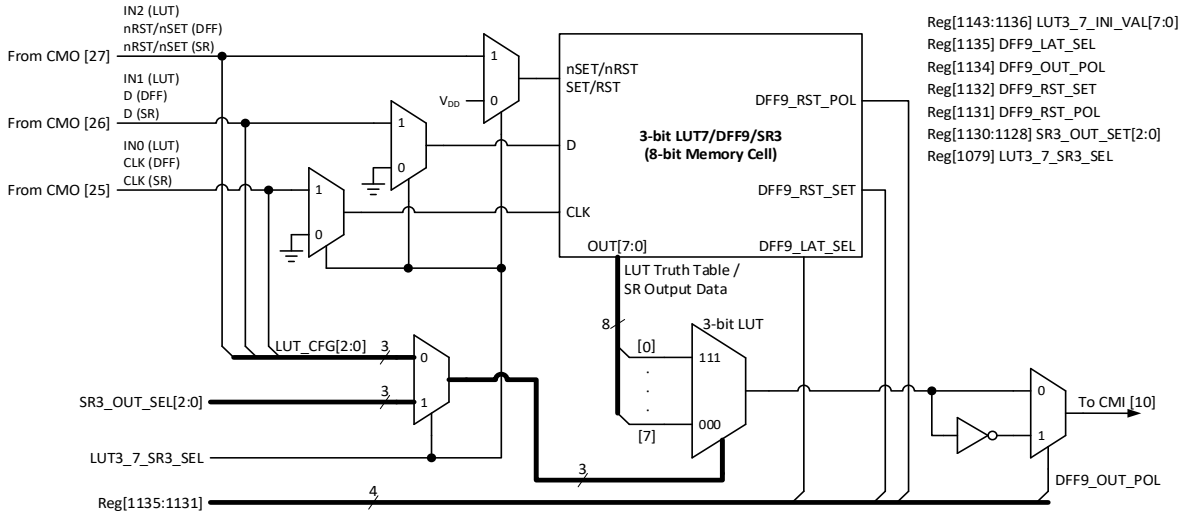
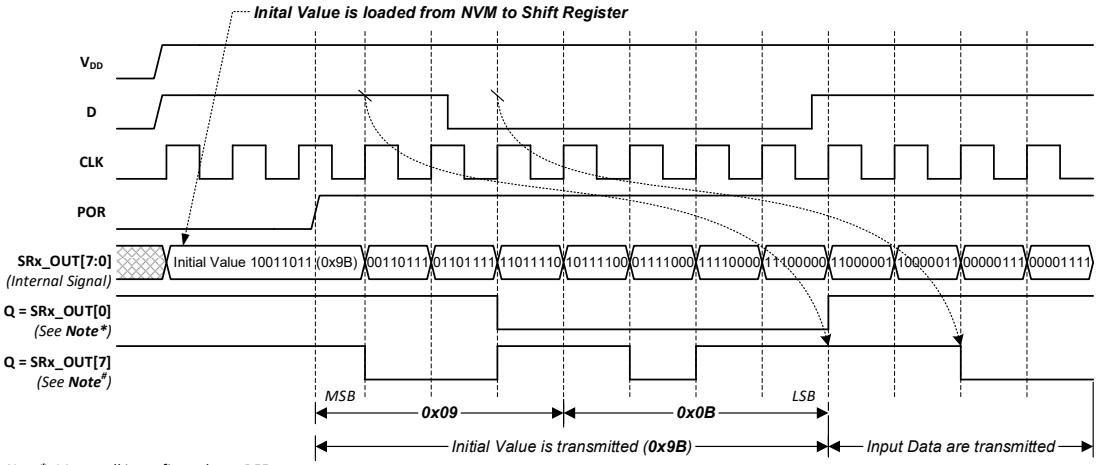
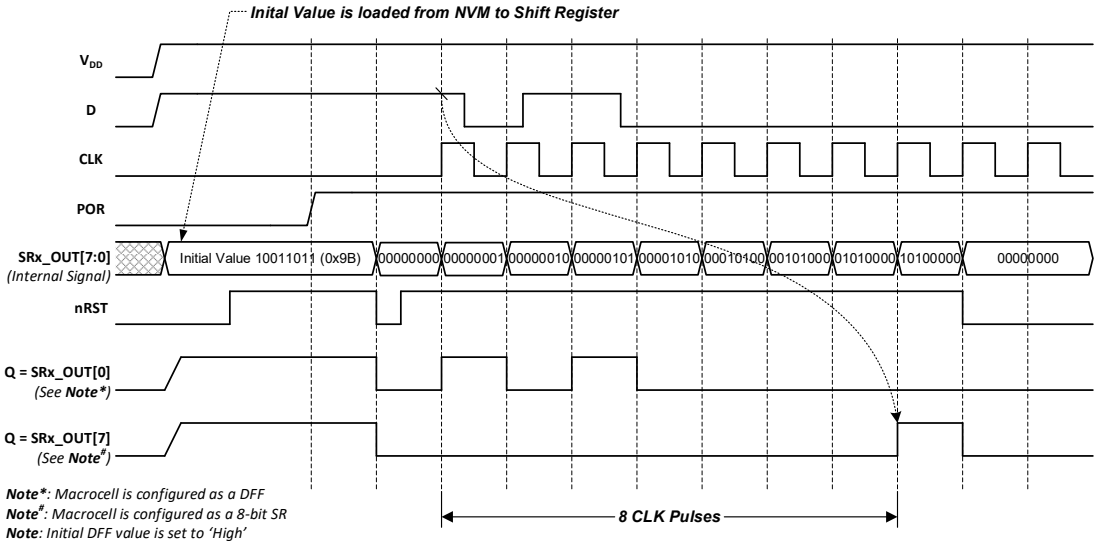


Figure 25. 3-bit LUT7, DFF9 or SR3



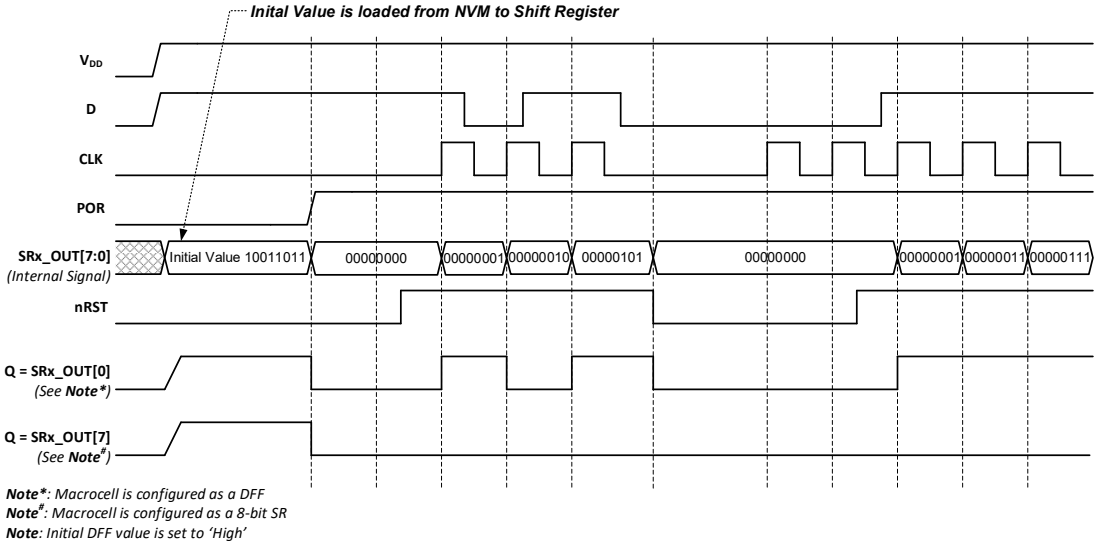
Note: Macrocell is configured as a DFF*
***Note**#: Macrocell is configured as a 8-bit Shift Register*

Figure 26. DFF6 – DFF9 or SR0 – SR3 Operation



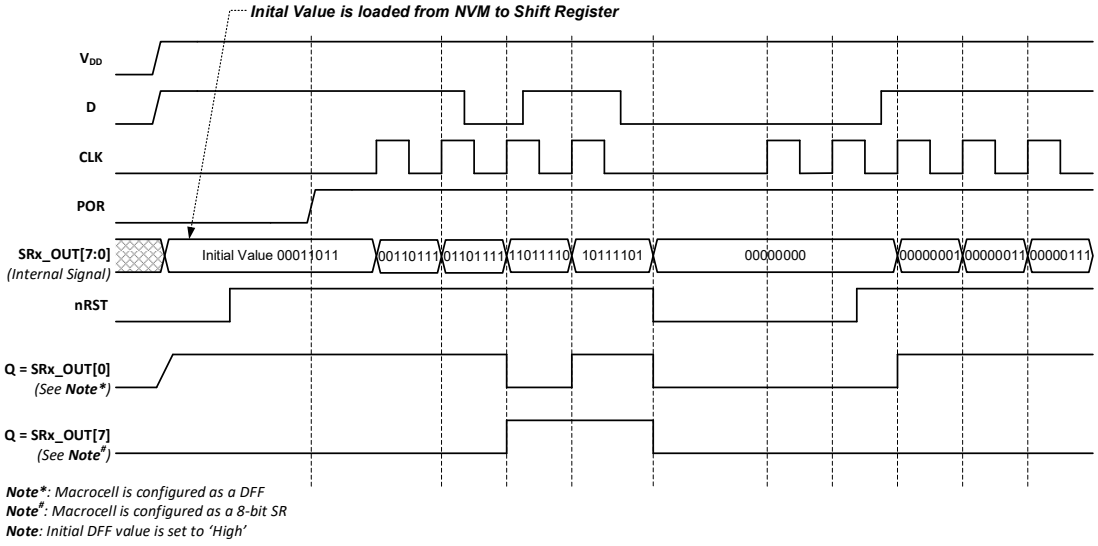
Note: Macrocell is configured as a DFF*
***Note**#: Macrocell is configured as a 8-bit SR*
***Note**: Initial DFF value is set to 'High'*

Figure 27. DFF6 – DFF9 or SR0 – SR3 Operation (nRST Option, Initial DFF Value = High, Case 1)



Note: Macrocell is configured as a DFF*
***Note**#: Macrocell is configured as a 8-bit SR*
***Note**: Initial DFF value is set to 'High'*

Figure 28. DFF6 – DFF9 or SR0 – SR3 Operation (nRST Option, Initial DFF Value = High, Case 2)



Note: Macrocell is configured as a DFF*
***Note**#: Macrocell is configured as a 8-bit SR*
***Note**: Initial DFF value is set to 'High'*

Figure 29. DFF6 – DFF9 or SR0 – SR3 Operation (nRST Option, Initial DFF Value = High, Case 3)

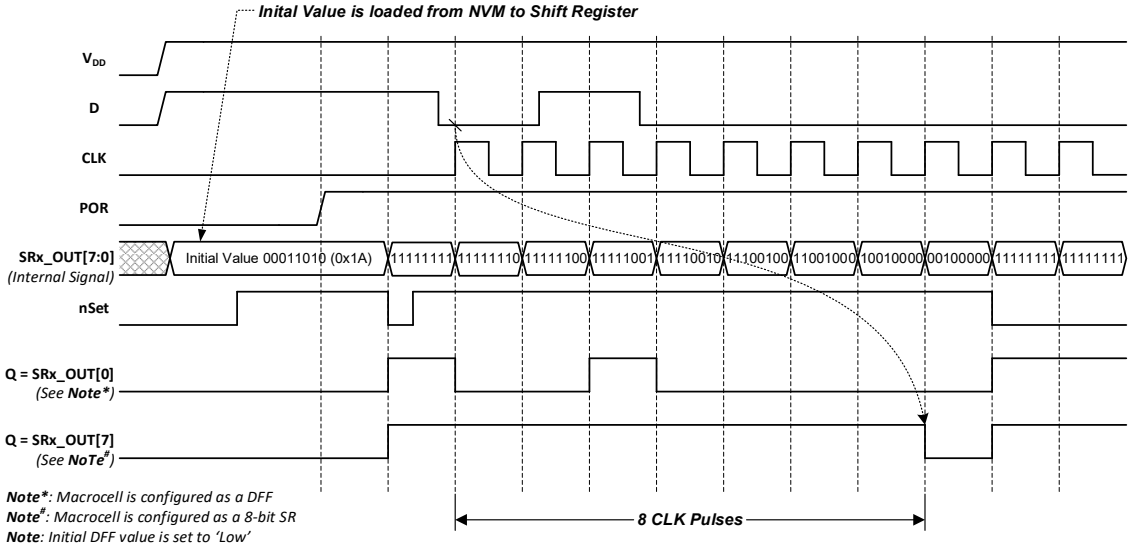


Figure 30. DFF6 – DFF9 or SR0 – SR3 Operation (nSET Option, Initial DFF Value = Low, Case 1)

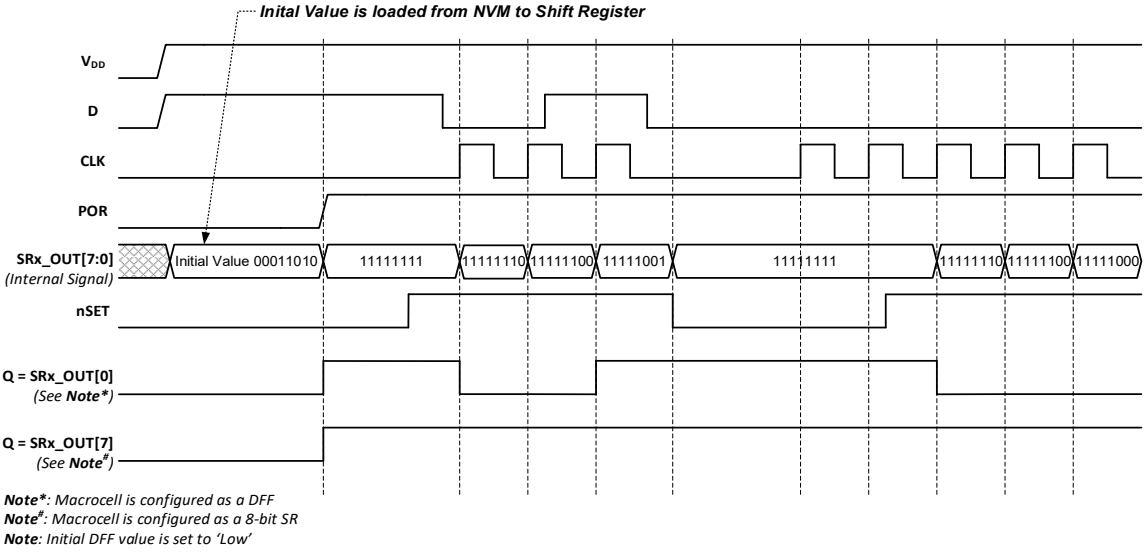


Figure 31. DFF6 – DFF9 or SR0 – SR3 Operation (nSET Option, Initial DFF Value = Low, Case 2)

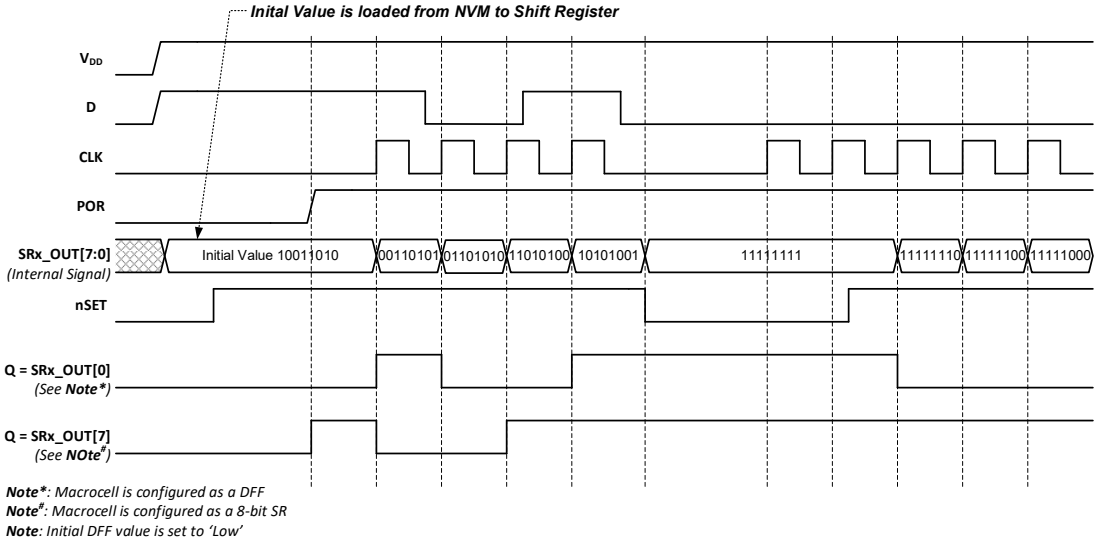


Figure 32. DFF6 – DFF9 or SR0 – SR3 Operation (nSET Option, Initial DFF Value = Low, Case 3)

6.3.1 3-bit LUT or D Flip-Flop Macrocells Used as 3-bit LUTs

When these macrocells are configured as LUT functions, 8-bit registers are used to define their output functions:

- 3-bit LUT0 output is defined by Reg[1023:1016]
- 3-bit LUT1 output is defined by Reg[1031:1024]
- 3-bit LUT2 output is defined by Reg[1039:1032]
- 3-bit LUT3 output is defined by Reg[1047:1040]
- 3-bit LUT4 output is defined by Reg[1095:1088]
- 3-bit LUT5 output is defined by Reg[1111:1104]
- 3-bit LUT6 output is defined by Reg[1127:1120]
- 3-bit LUT7 output is defined by Reg[1143:1136].

Table 8. 3-bit LUT0 to 3-bit LUT7 Truth Table

IN2	IN1	IN0	3-bit LUT0 OUT	3-bit LUT1 OUT	3-bit LUT2 OUT	3-bit LUT3 OUT	3-bit LUT4 OUT	3-bit LUT5 OUT	3-bit LUT6 OUT	3-bit LUT7 OUT
0	0	0	Reg[1016]	Reg[1024]	Reg[1032]	Reg[1040]	Reg[1088]	Reg[1104]	Reg[1120]	Reg[1136]
0	0	1	Reg[1017]	Reg[1025]	Reg[1033]	Reg[1041]	Reg[1089]	Reg[1105]	Reg[1121]	Reg[1137]
0	1	0	Reg[1018]	Reg[1026]	Reg[1034]	Reg[1042]	Reg[1090]	Reg[1106]	Reg[1122]	Reg[1138]
0	1	1	Reg[1019]	Reg[1027]	Reg[1035]	Reg[1043]	Reg[1091]	Reg[1107]	Reg[1123]	Reg[1139]
1	0	0	Reg[1020]	Reg[1028]	Reg[1036]	Reg[1044]	Reg[1092]	Reg[1108]	Reg[1124]	Reg[1140]
1	0	1	Reg[1021]	Reg[1029]	Reg[1037]	Reg[1045]	Reg[1093]	Reg[1109]	Reg[1125]	Reg[1141]
1	1	0	Reg[1022]	Reg[1030]	Reg[1038]	Reg[1046]	Reg[1094]	Reg[1110]	Reg[1126]	Reg[1142]
1	1	1	Reg[1023]	Reg[1031]	Reg[1039]	Reg[1047]	Reg[1095]	Reg[1111]	Reg[1127]	Reg[1143]

Table 9 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 9. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

6.4 4-bit LUT or D Flip-Flop with Reset/Set Macrocell

There is one macrocell that can serve as either a 4-bit LUT or a DFF with reset/set input. When it is used to implement a LUT function, the 4-bit LUT takes four input signals from the connection matrix outputs (CMOs) and produces a single output, which goes back to the connection matrix input (CMI). When it is used as a DFF function, the input signals from the connection matrix outputs are connected to data (D), clock (CLK), and

reset/set (nRST/nSET) inputs, and the output goes back to the connection matrix input. It is possible to select the polarity of the reset/set input of DFF/LATCH macrocell. The DFF10_RST_POL bit selects either active-high (RST/SET) or active-low (nRST/nSET) options. The DFF10_LAT_SEL bit selects either DFF or LATCH function. The operations of the DFF and LATCH functions are described below:

- **DFF**: Q = D at a rising edge of the CLK, otherwise Q remains its previous value.
- **LATCH**: Q = D when CLK is low, otherwise Q remains its previous value (D has no effect when CLK is high).

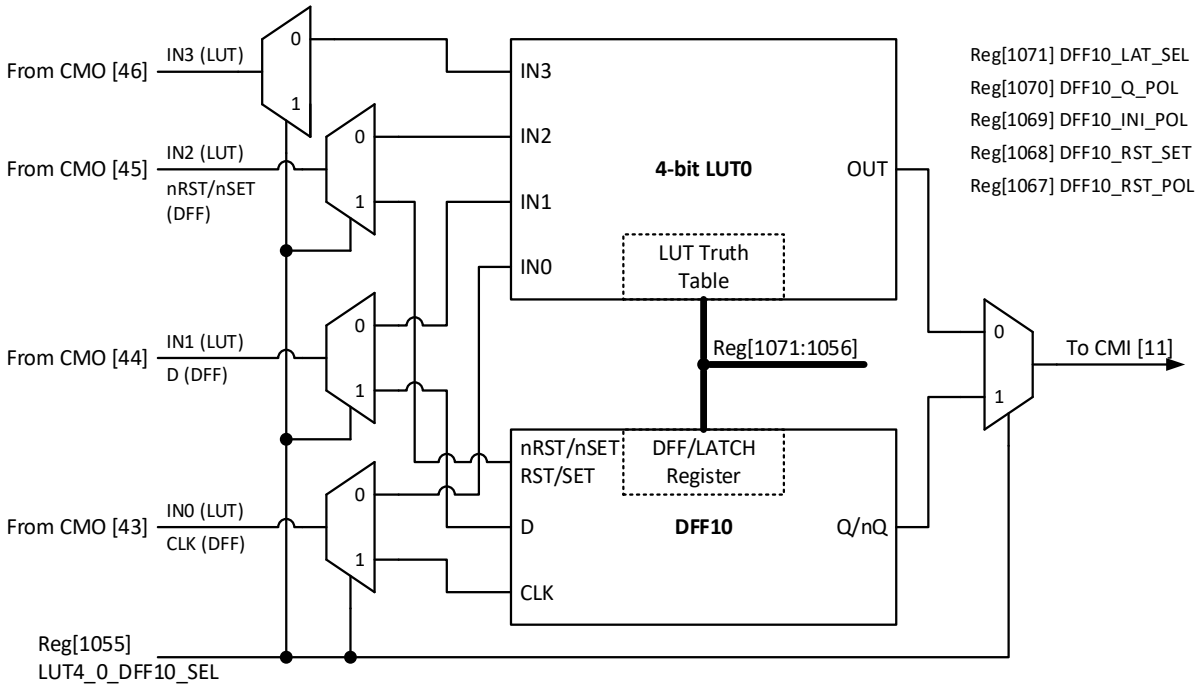


Figure 33. 4-bit LUT0 or DFF10

6.4.1 4-bit LUT Macrocell Used as 4-bit LUT

Table 10. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	4-bit LUT0 OUT
0	0	0	0	Reg[1056]
0	0	0	1	Reg[1057]
0	0	1	0	Reg[1058]
0	0	1	1	Reg[1059]
0	1	0	0	Reg[1060]
0	1	0	1	Reg[1061]
0	1	1	0	Reg[1062]
0	1	1	1	Reg[1063]
1	0	0	0	Reg[1064]
1	0	0	1	Reg[1065]
1	0	1	0	Reg[1066]
1	0	1	1	Reg[1067]
1	1	0	0	Reg[1068]
1	1	0	1	Reg[1069]
1	1	1	0	Reg[1070]
1	1	1	1	Reg[1071]

When this macrocell is configured as a LUT function, a 16-bit register is used to define its output function:

- 4-bit LUT0 output is defined by Reg[1071:1056].

Table 11. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7. Multi-Function Macrocells

The SLG47001-E/03-E has 5 multi-function macrocells that can serve more than one logic or timing function. Each multi-function macrocell can serve as a LUT, a DFF with flexible settings, or a counter/delay with multiple modes such as one-shot, frequency detection, edge detection, and others. Also, the macrocell can combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF (see Figure 34).

See the list below for the functions that can be implemented in these macrocells:

- Four macrocells that can serve as 3-bit LUTs/DFFs and as 8-bit CNT/DLY.
- One macrocell that can serve as 3-bit LUTs/DFFs and as 8-bit CNT/DLY/FSM.

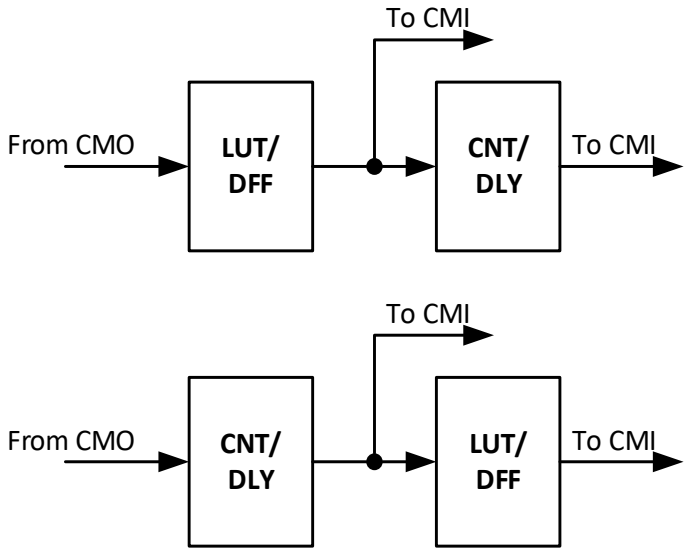


Figure 34. Possible Connections inside Multi-Function Macrocell

The IOs of the multi-function macrocells are configured from the connection matrix with specific logic functions being defined by the state of the NVM bits.

When the LUT function is selected, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 3-bit LUT or DFF/LATCH with 8-bit Counter/Delay Macrocells

There are five macrocells that can serve as 3-bit LUTs/DFFs and as 8-bit counter/delays. When the LUT function is selected, the 3-bit LUTs take three input signals from the connection matrix outputs (CMOs) and produce a single output, which goes back to the connection matrix input (CMI) or can be connected to the input of CNT/DLY. When DFF function is selected, the three input signals from the connection matrix outputs are connected to data (D), clock (CLK), and reset/set (nRST/nSET) inputs, and the output goes back to the connection matrix input or to the input of CNT/DLY.

For CNT/DLY function, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of the internal and the external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer counter/delay circuits. These macrocells can also operate in a one-shot mode, which generates an output pulse with the user-defined width. They can also operate in frequency detection or edge detection mode. The CNT/DLY macrocell has an initial value, which sets its initial condition after the device is powered up. It is possible to select initial low or initial high, as well as initial value defined by the DLY_IN signal. For example, in case initial low option is used, the rising edge delay will start operation. For timing diagrams, refer to section 7.2 CNT/DLY Timing Diagrams.

The CNT0/DLY0/FSM macrocell has an optional finite state machine (FSM) function. In this mode, one additional input (UP) is from the connection matrix output.

All CNT/DLY functions have a synchronization option which allows the DLY_IN/nRST and the UP signals to be synchronize to CLK using two DFF's (See Figure 42 and Figure 43). Enabling the synchronization option helps with proper resetting/setting of the CNT/DLY block to its initial value without error. Based on design requirements, the synchronization option can be disabled/enabled by setting the CNTx_MODE_SYNC bits.

7.1.1 3-bit LUT or 8-bit CNT/DLY Block Diagrams

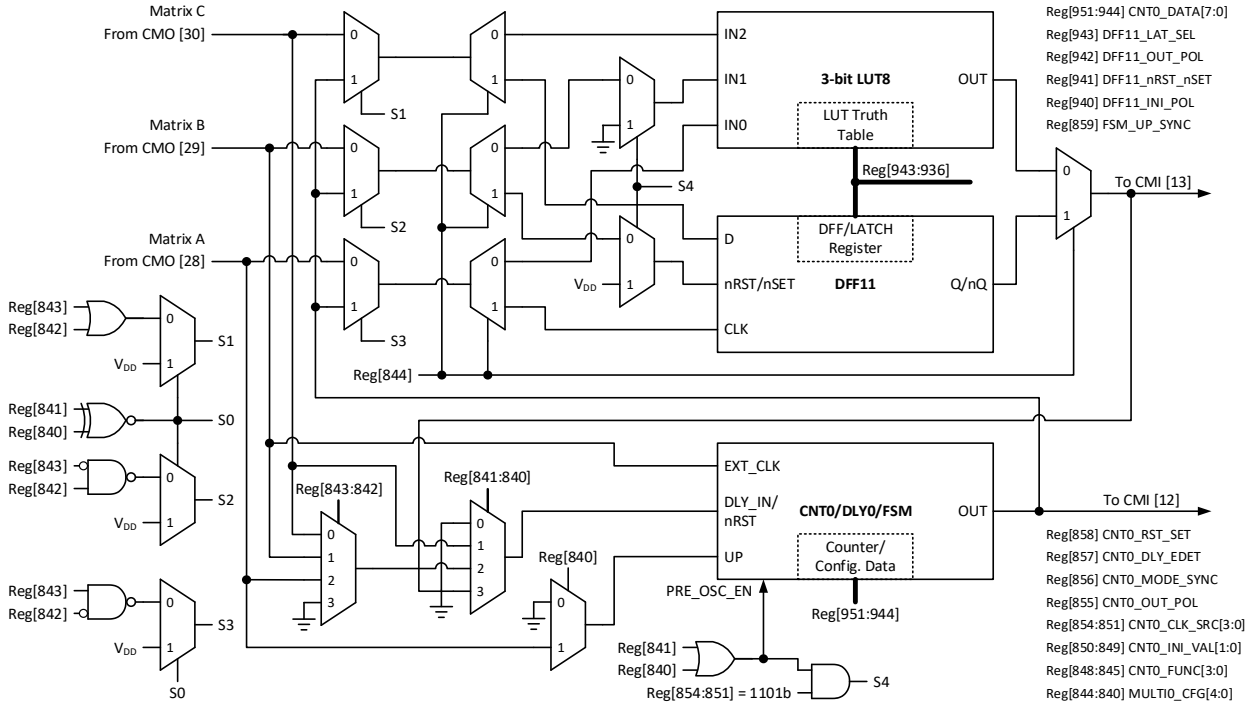


Figure 35. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF11, CNT0/DLY0/FSM)

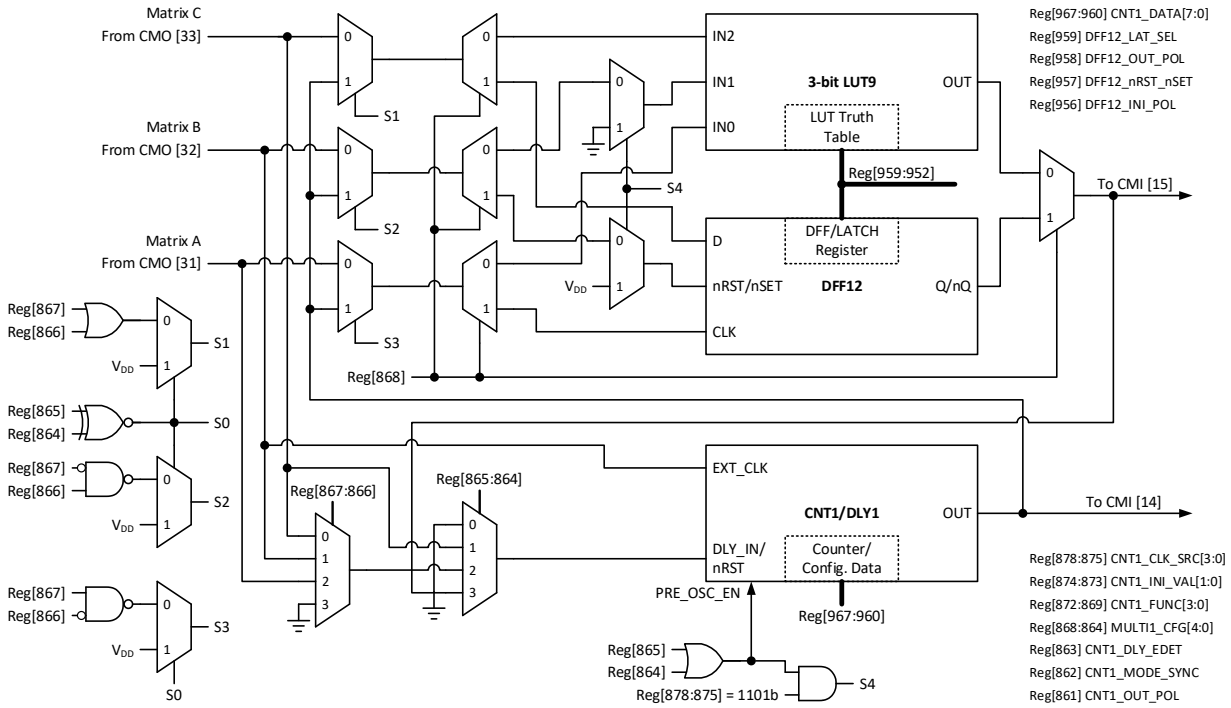


Figure 36. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF12, CNT1/DLY1)

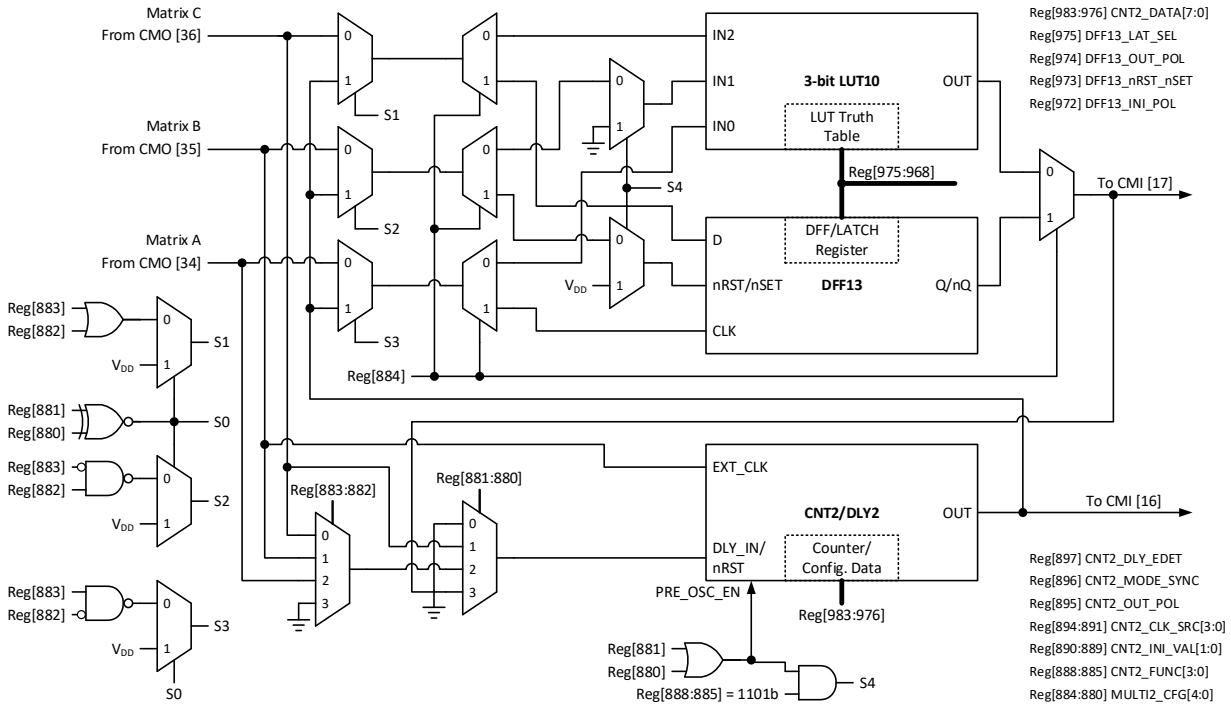


Figure 37. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF13, CNT2/DLY2)

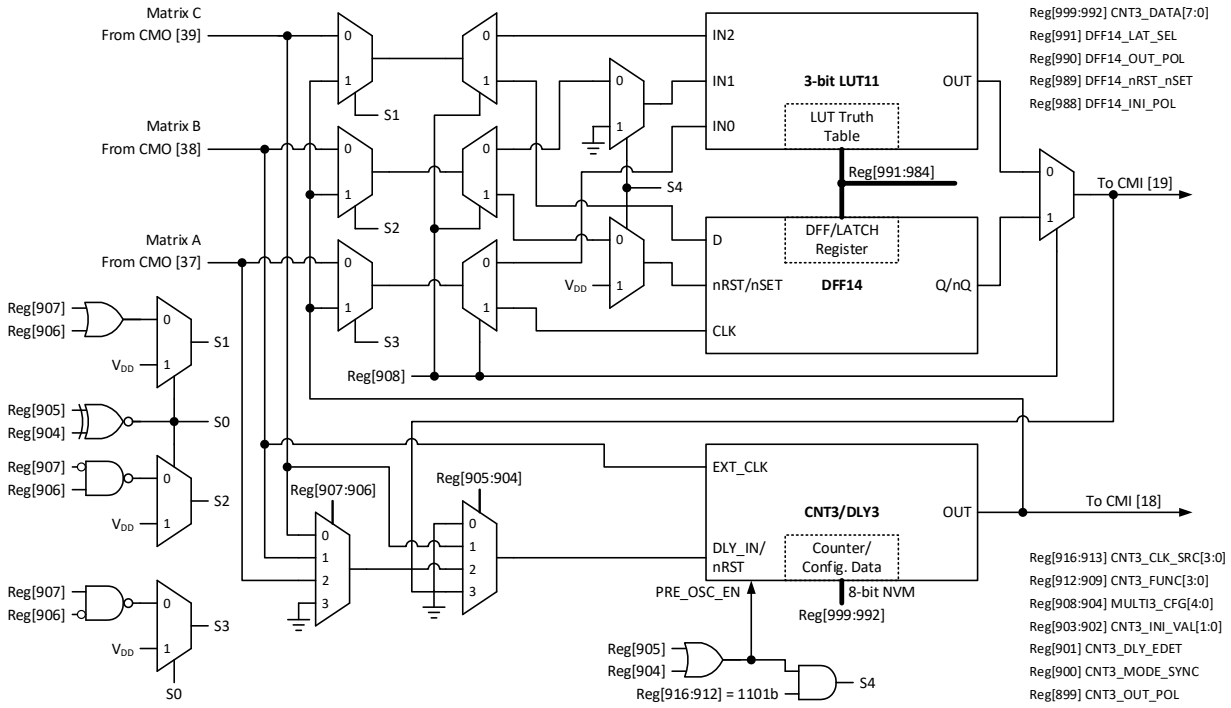


Figure 38. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF14, CNT3/DLY3)

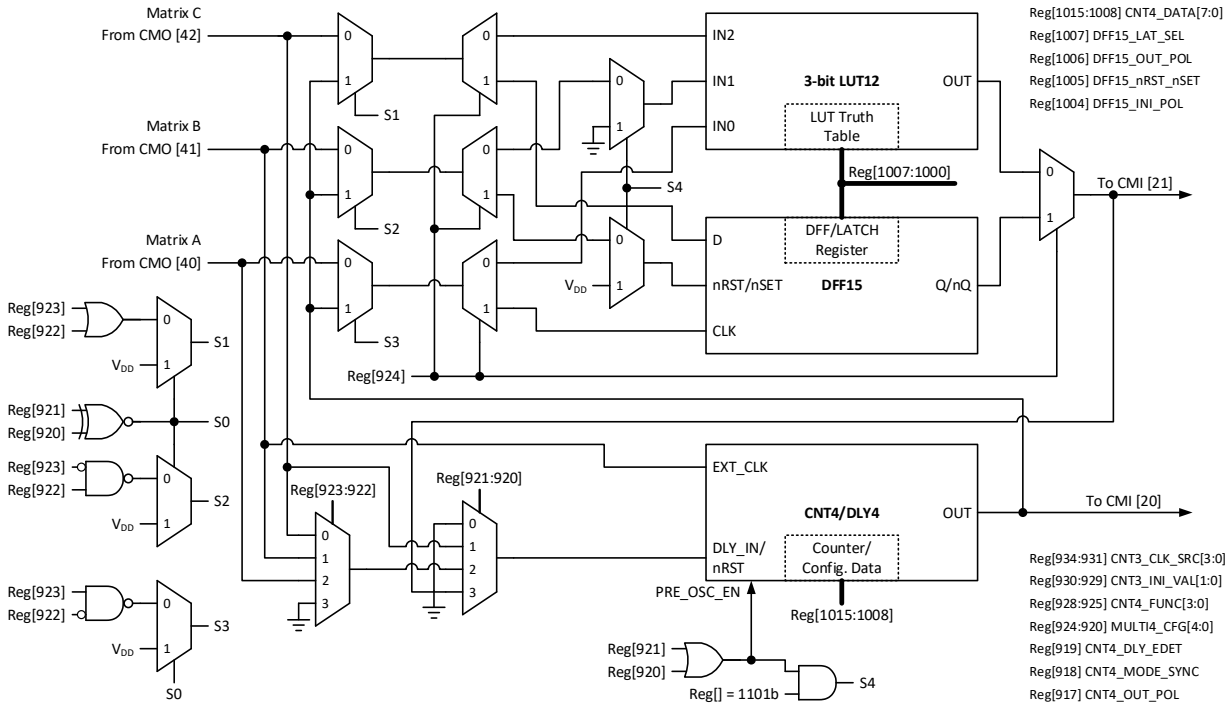


Figure 39. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF15, CNT4/DLY4)

As shown in Figure 35 thru Figure 39, it is possible to use LUT/DFF and CNT/DLY simultaneously. Note that LUT and DFF functions of a multi-function macrocell cannot be used at the same time. Table 12 and Table 13 show the selection options of the MULTIx_CFG[4:0] and the CNTx_FUNC[3:0] registers.

- **Case 1**: LUT/DFF in front of CNT/DLY.

  Three input signals from the connection matrix outputs are connected to the inputs of the previously selected LUT or DFF and produce a single output which goes to the input of CNT/DLY. In its turn, the output of CNT/DLY goes back to the connection matrix input.

- **Case 2**: CNT/DLY in front of LUT/DFF.

  Two input signals from the connection matrix outputs are connected to the input of CNT/DLY (IN and CLK). Its output signal can be connected to any input of the previously selected LUT or DFF, and after that the signal goes back to the connection matrix input.

- **Case 3**: Single LUT/DFF or CNT/DLY.

  Also, it is possible to use a standalone LUT/DFF or CNT/DLY function. In this case, all the inputs and the output of the macrocell are connected to the connection matrix.

Table 12. Multi-Function Macrocell Configuration Selection

MULTIx_CFG[4:0]	Function	Matrix C	Matrix B	Matrix A	Note
00000b	Single 3-bit LUT	IN2	IN1	IN0	DLY_IN = L
00001b	Single CNT/DLY	DLY_IN	EXT_CLK	UP [1]	DLY_OUT → LUT/DFF
00010b	CNT/DLY → LUT	DLY_IN	IN1	IN0	DLY_OUT → IN2
00011b	LUT → CNT/DLY	IN2	IN1	IN0	LUT_OUT → DLY_IN
00110b	CNT/DLY → LUT	IN2	DLY_IN	IN0	DLY_OUT → IN1
01010b		IN2	IN1	DLY_IN	DLY_OUT → IN0
10000b	Single DFF	D	nRST/nSET	CLK	DLY_IN = L
10010b	CNT/DLY → DFF	DLY_IN	nRST/nSET	CLK	DLY_OUT → D
10011b	DFF → CNT/DLY	D	nRST/nSET	CLK	DFF_OUT → DLY_IN
10110b	CNT/DLY → DFF	D	DLY_IN	CLK	DLY_OUT → nRST/nSET
11010b		D	nRST/nSET	DLY_IN	DLY_OUT → CLK

[1] "UP" is available only for MULTI0. "NC" for MULTI1 through MULTI4.

Table 13. Multi-Function Macrocell CNT/DLY Function Selection

CNTx_FUNC[3:0]	Function	CNTx_FUNC[3:0]	Function
0000b	Both Edge Delay	1000b	Rising Edge Frequency Detection
0001b	Falling Edge Delay	1001b	Both Edge Detection
0010b	Rising Edge Delay	1010b	Falling Edge Detection
0011b	Both Edge One-shot	1011b	Rising Edge Detection
0100b	Falling Edge One-shot	1100b	Both Edge Reset Counter
0101b	Rising Edge One-shot	1101b	Falling Edge Reset Counter
0110b	Both Edge Frequency Detection	1110b	Rising Edge Reset Counter
0111b	Falling Edge Frequency Detection	1111b	High-level Reset Counter

7.1.2 3-bit LUT or CNT/DLYs Used as 3-bit LUTs

Table 14. 3-bit LUT8 to 3-bit LUT12 Truth Table

IN2	IN1	IN0	3-bit LUT8 OUT	3-bit LUT9 OUT	3-bit LUT10 OUT	3-bit LUT11 OUT	3-bit LUT12 OUT
0	0	0	Reg[936]	Reg[952]	Reg[968]	Reg[984]	Reg[1000]
0	0	1	Reg[937]	Reg[953]	Reg[969]	Reg[985]	Reg[1001]
0	1	0	Reg[938]	Reg[954]	Reg[970]	Reg[986]	Reg[1002]
0	1	1	Reg[939]	Reg[955]	Reg[971]	Reg[987]	Reg[1003]
1	0	0	Reg[940]	Reg[956]	Reg[972]	Reg[988]	Reg[1004]
1	0	1	Reg[941]	Reg[957]	Reg[973]	Reg[989]	Reg[1005]
1	1	0	Reg[942]	Reg[958]	Reg[974]	Reg[990]	Reg[1006]
1	1	1	Reg[943]	Reg[959]	Reg[975]	Reg[991]	Reg[1007]

When these macrocells are configured as LUT functions, 8-bit registers are used to define their output functions:

- 3-bit LUT8 output is defined by Reg[943:936]
- 3-bit LUT9 output is defined by Reg[959:952]
- 3-bit LUT10 output is defined by Reg[975:968]
- 3-bit LUT11 output is defined by Reg[991:984]
- 3-bit LUT12 output is defined by Reg[1007:1000].

7.2 CNT/DLY Timing Diagrams

7.2.1 Delay Mode

In delay mode, the CNT/DLY macrocell shifts the input signal at the respective edge (rising, falling or both edge) for the delay time set by CNTx_DATA[7:0] registers. In case the input signal is shorter than the delay time, this macrocell works as a debounce filter.

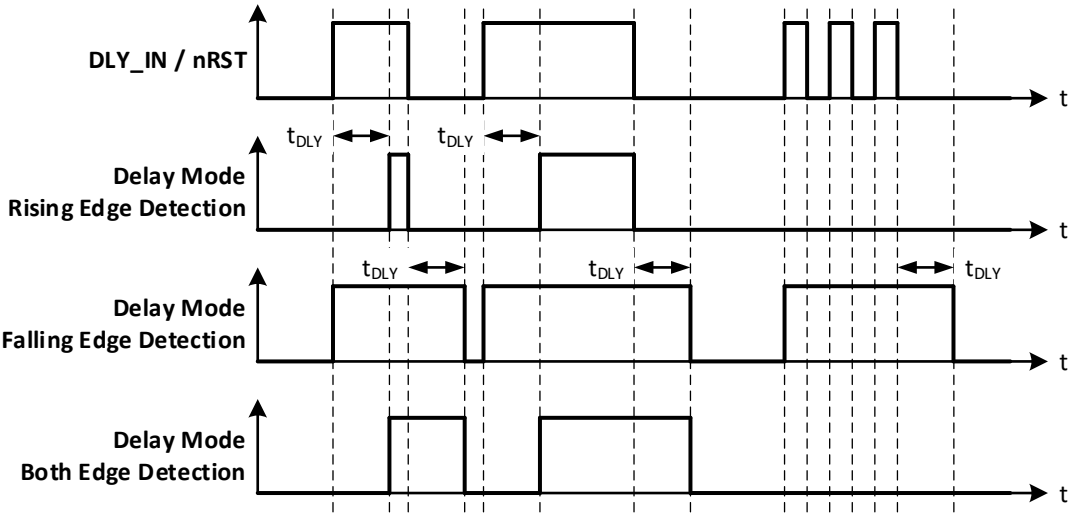


Figure 40. Delay Mode Timing Diagram

Example timing diagrams in delay mode with both edge detection are shown in Figure 41.

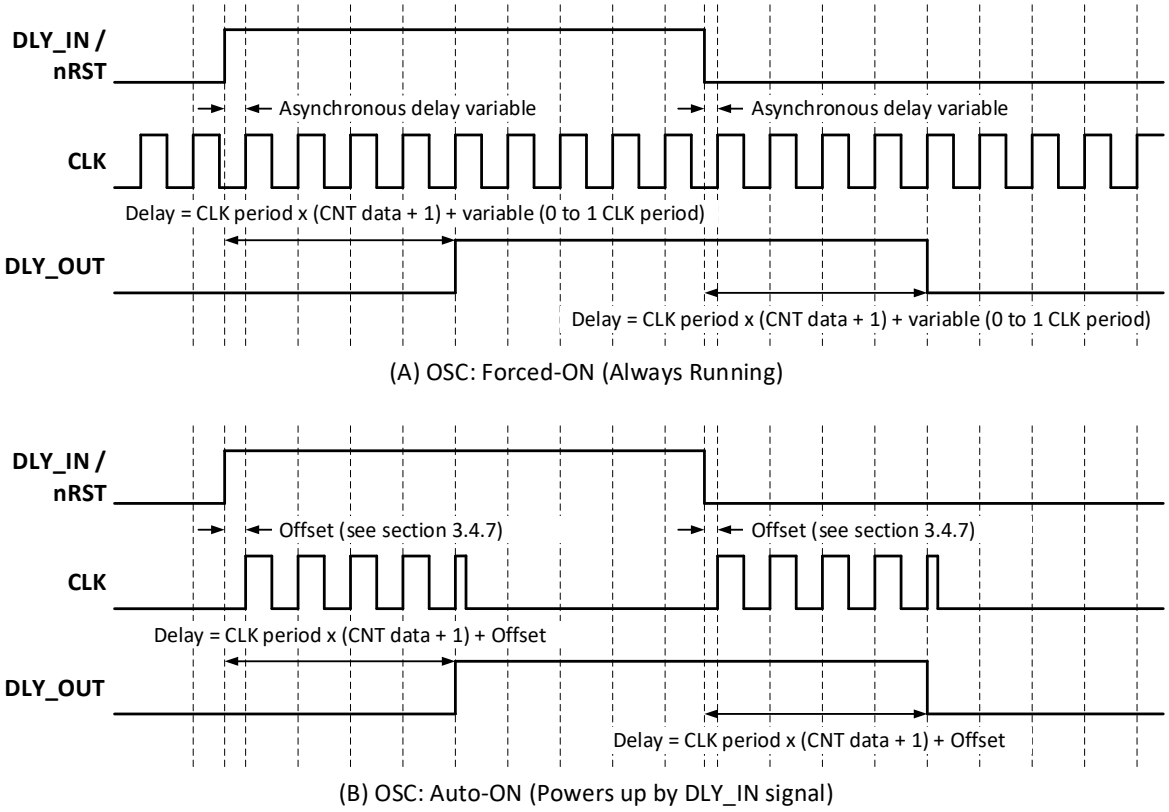


Figure 41. Delay Mode Timing Diagram (Both Edge, CNTx_DATA[7:0] = 3)

7.2.2 Counter Mode

Counter mode timing diagrams with rising edge detection for CNTx_DATA[7:0] = 3 are shown in Figure 42 (CNTx_MODE_SYNC = 0) and Figure 43 (CNTx_MODE_SYNC = 1).

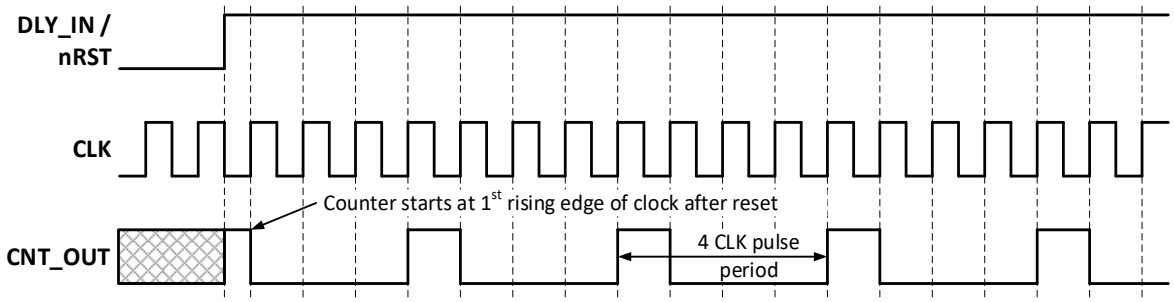


Figure 42. Counter Mode Timing Diagram (Rising Edge, No Synchronization)

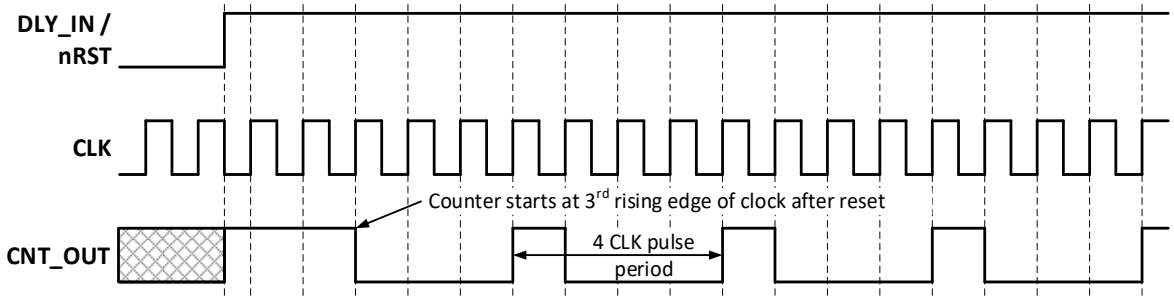


Figure 43. Counter Mode Timing Diagram (Rising Edge, Synchronized to CLK using Two DFFs)

7.2.3 One-Shot Mode

This macrocell generates a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by the CNTx_OUT_POL register bit. During the pulse width generation, any incoming edges will be ignored. The following diagram shows one-shot function with non-inverted output.

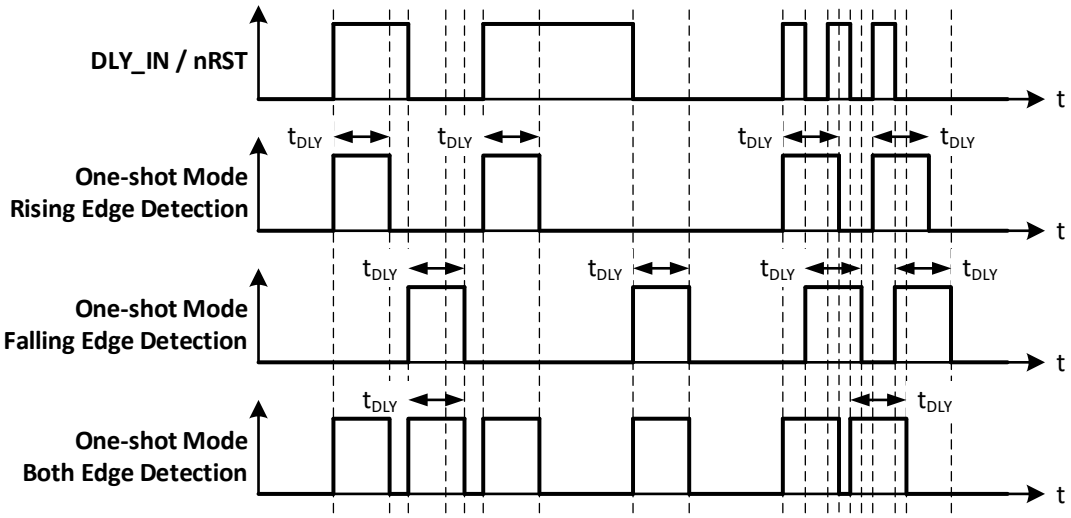


Figure 44. One-Shot Mode Timing Diagram

This macrocell generates a high-level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

7.2.4 Frequency Detection Mode

- **Rising Edge**: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge within the specified time.
- **Falling Edge**: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge does not come after the last falling edge within the specified time.
- **Both Edge**: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if the second edge has not come after the last rising/falling edge within the specified time.

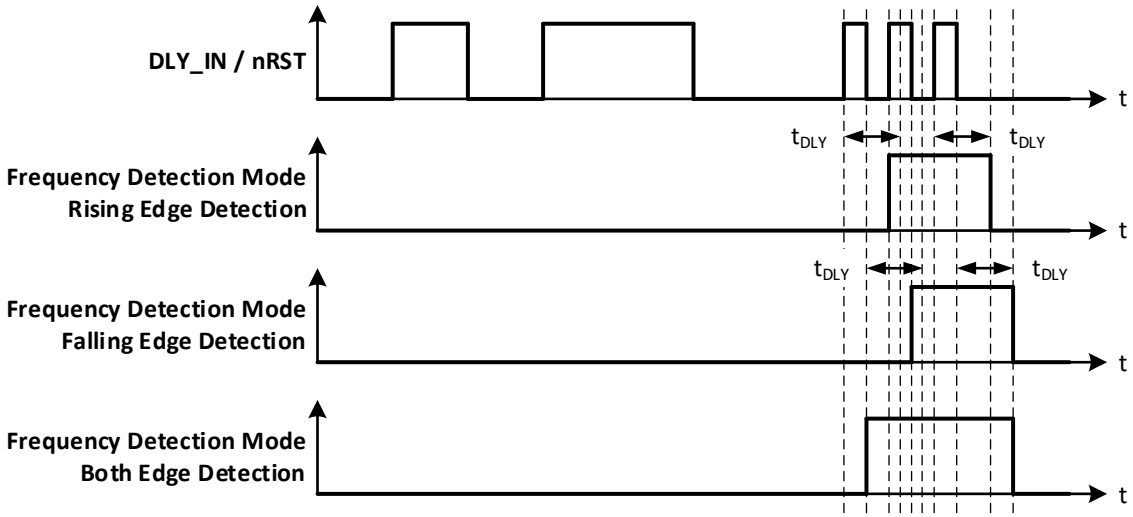


Figure 45. Frequency Detection Mode Timing Diagram

7.2.5 Edge Detection Mode

The macrocell generates high-level short pulse when detecting the respective edge (see section 3.4.4 Estimated Typical Delay of Each Macrocell).

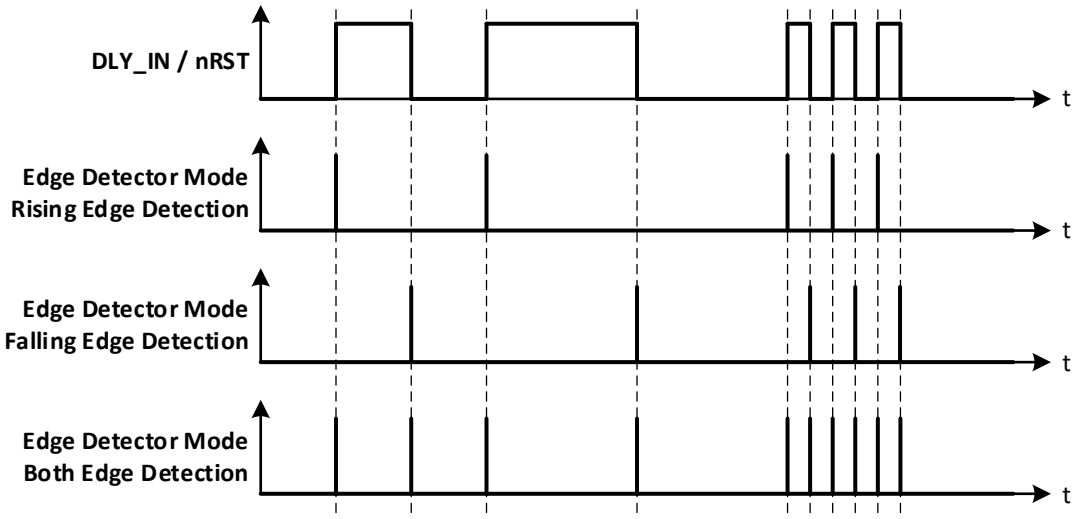


Figure 46. Edge Detection Mode Timing Diagram

7.2.6 Delayed Edge Detection Mode

In delayed edge detection mode, high level short pulses are generated on the macrocell output after the configured delay time if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 47.

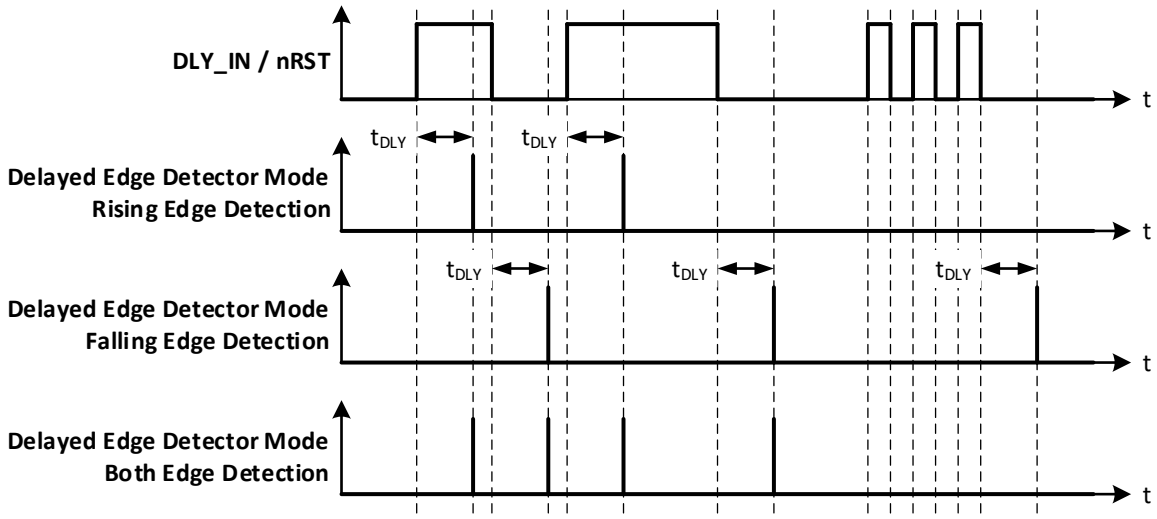


Figure 47. Delayed Edge Detection Mode Timing Diagram

7.2.7 Counter Value in Different Modes

As shown in Figure 48, the counter value is set with different values depending on CNT/DLY functions. In counter mode, the CNTx_DATA[7:0] register value is loaded to the counter at the first rising edge, while the counter value is shifted for two rising edges of the clock signal in delay, one-shot, and frequency detection modes.

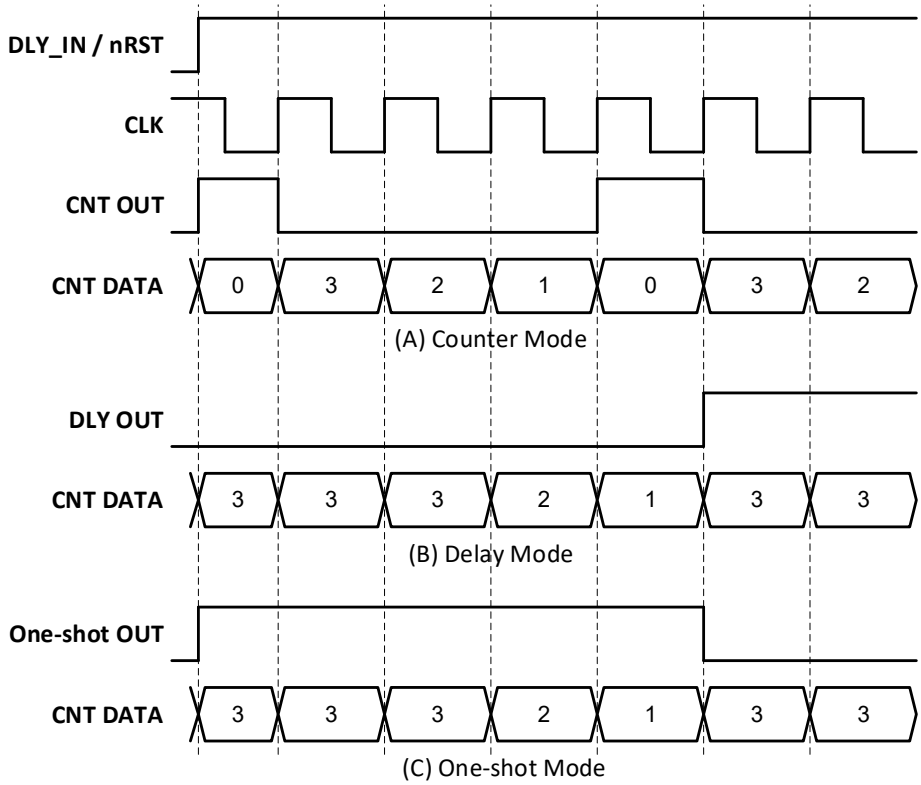


Figure 48. Counter Data Value in Different Modes (CNTx_DATA[7:0] = 3)

7.3 FSM Timing Diagrams

The behavior of FSM macrocell with low-level at Up input is the same as the behavior of other multi-function macrocells in corresponding modes (counter, delay, one-shot, frequency detection, and delayed edge detection).

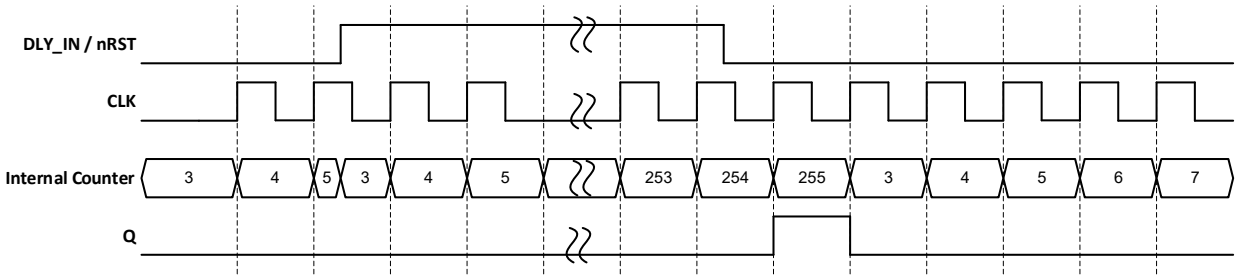


Figure 49. FSM Mode Timing Diagram (Rising Edge, OSC: Forced-ON, UP = 1, CNTx_DATA[7:0] = 3)

8. Programmable Delay/Edge Detector

The SLG47001-E/03-E has a programmable time delay logic cell that can generate a fixed time delay. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 50 and Figure 51 for further information.

Note that the input signal must be longer than the delay, otherwise it will be filtered out.

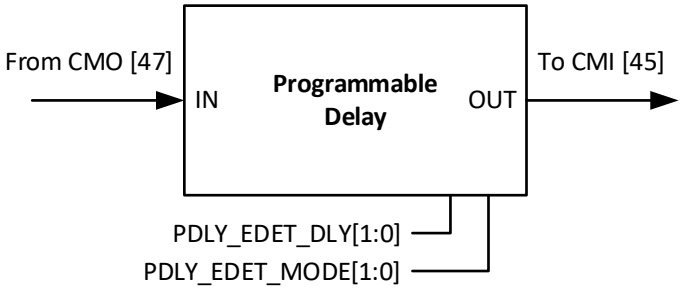


Figure 50. Programmable Delay

8.1 Programmable Delay Timing Diagram - Edge Detector Output

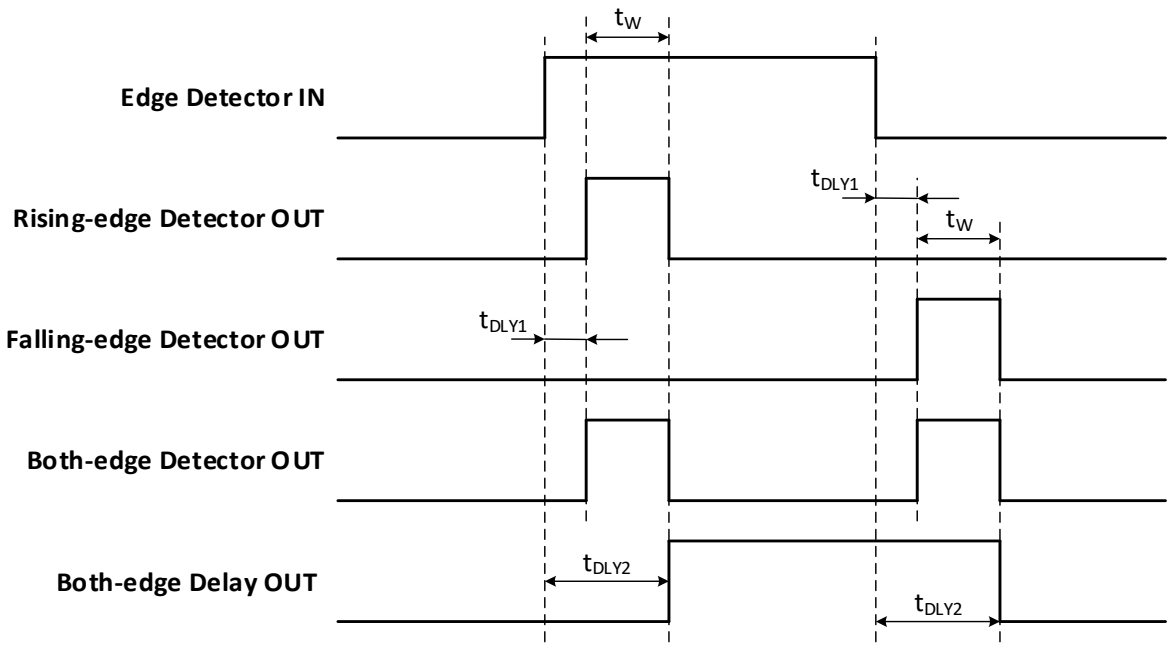


Figure 51. Edge Detector Output

For detailed specifications, refer to section 3.4.5 Typical Propagation Delay and Pulse Width.

9. Internal Voltage Reference

9.1 Internal V_{REF} General Description

The SLG47001-E/03-E has a voltage reference (V_{REF}) macrocell to provide fixed voltage references to the multi-channel analog comparator (MS-ACMP), the operational amplifiers (OpAmps), and the sink/source buffer. This macrocell has three reference voltage generators and one of them supports an option to select either a low-side or a high-side voltage reference. The low-side V_{REF} is referenced to GND, while the high-side V_{REF} has V_{DDA} as a common point. The structure of internal voltage references is shown in Figure 52.

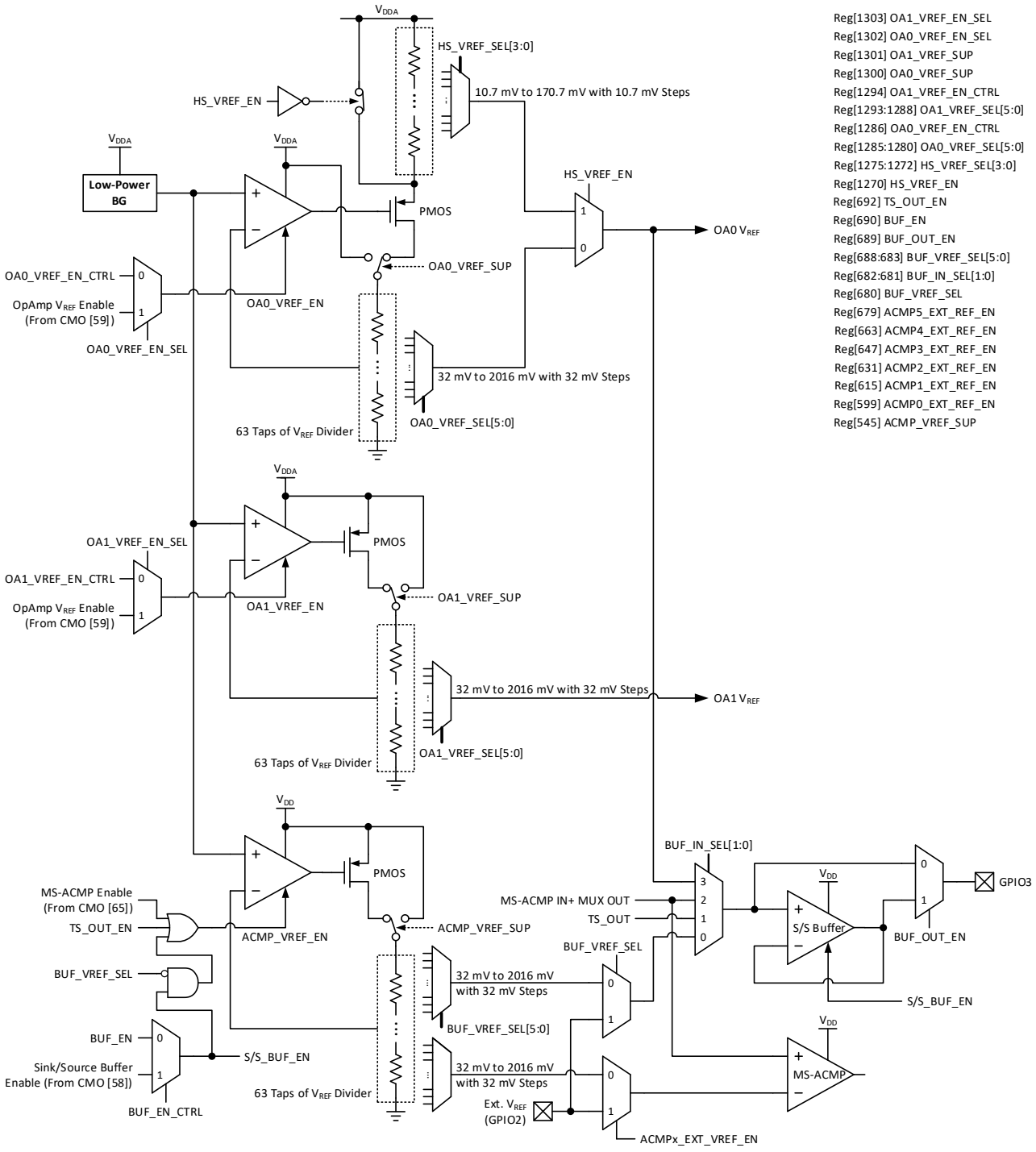


Figure 52. Internal V_{REF} Structure

The two operational amplifiers have dedicated low-side V_{REF} generators that provide 63 levels of reference voltages from 32 mV to 2016 mV with 32 mV steps. Each V_{REF} generator has an individual multiplexer (63-to-1 MUX) to select one of 63 V_{REF} voltages which is connected to the corresponding operational amplifier input. The supply voltages of the 63-tap divider circuits of the V_{REF} generators for the operational amplifiers are individually selected between V_{DDA} and 2016 mV by the OA0_VREF_SUP and the OA1_VREF_SUP registers respectively.

The high-side V_{REF} option is only available for OpAmp0 and this option is enabled by setting the HS_VREF_EN bit (Reg[1270]) to '1'. When HS_VREF_EN = 1, the low-side V_{REF} for OpAmp0 is automatically deactivated and the V_{DDA} voltage must be 2.5 V or higher for proper operation. The high-side V_{REF} voltage is selectable between 10.7 mV and 170.7 mV with 10.7 mV step size by the HS_VREF_SEL[3:0] register (Reg[1275:1272]).

There is another low-side voltage reference generator which is for the MS-ACMP and the sink/source buffer. The structure of this V_{REF} generator circuit is the same as the ones for the operational amplifiers except that it has two 63-to-1 multiplexers. The 63 levels of reference voltages are fed to the negative input of the MS-ACMP circuit though a 63-to-1 MUX which is controlled by the MS-ACMP sampling engine. The other MUX, which is controlled by the BUF_VREF_SEL[5:0] register, is used to source the reference voltage to GPIO3.

As shown in Figure 53, the BUF_IN_SEL[1:0] register selects the 4-to-1 MUX output to GPIO3 from four inputs including V_{REF} (either from the internal V_{REF} generator or GPIO2), the temperature sensor output (TS_OUT), the output of the MS-ACMP input MUX, and the V_{REF} for OpAmp0 (either low-side or high-side selected by the HS_VREF_EN bit). The selection between the internal V_{REF} and the external V_{REF} at GPIO2 is determined by the BUF_VREF_SEL bit. For a stronger driving capability to an external load on GPIO3, the sink/source buffer can be enabled by setting BUF_OUT_EN to '1'.

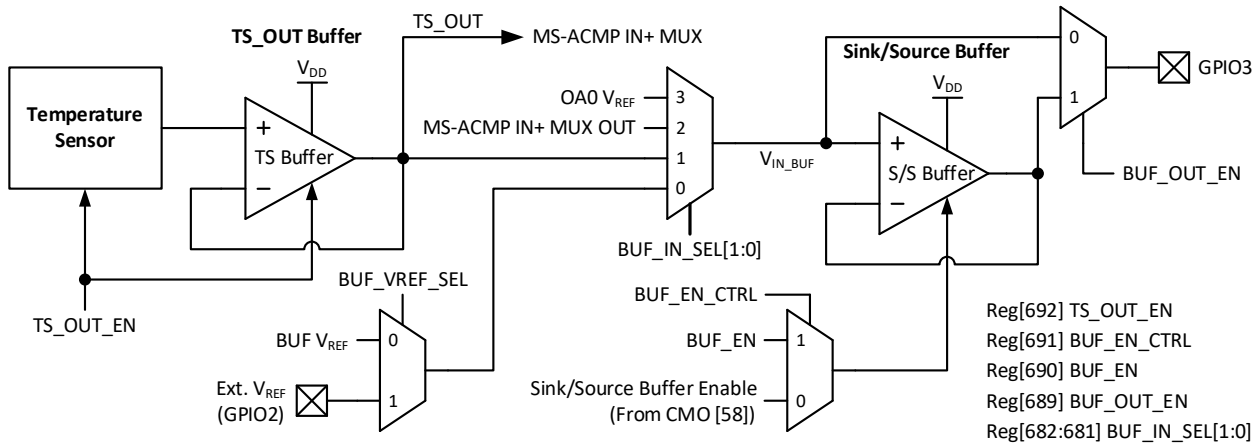


Figure 53. TS_OUT Buffer and Sink/Source Buffer Block Diagram

In production, the internal V_{REF} voltage at GPIO3 (which is driven by the sink/source buffer) is measured at room temperature and stored in the NVM. The VREF_ERROR[7:0] register at ADDR 0xA4 represents the voltage difference (error) between the target V_{REF} value (1.504 V) and the measured V_{REF} output voltage in 8-bit 2's complement format (0.25 mV per LSB). For example, if the measured V_{REF} value is 1.508 V, then the error will be 4 mV (= 1.508 V - 1.504 V) and the VREF_ERROR[7:0] value will be 4/0.25 = 16 = 00010000b.

The programmable options of the internal voltage reference are shown in Table 15.

Table 15. V_{REF} and Sink/Source Buffer Configuration Registers

Register Name	Access Type	Register Bit Description
ACMP_VREF_SUP	RW	MS-ACMP V_{REF} Supply Voltage Selection 0: 2016 mV 1: V_{DD}
BUF_VREF_SEL	RW	Sink/Source Buffer V_{REF} Input Selection 0: Internal V_{REF} 1: External V_{REF} (From GPIO2)

Register Name	Access Type	Register Bit Description
BUF_IN_SEL[1:0]	RW	Sink/Source Buffer Input Selection 00b: V_{REF} (Internal or External determined by Reg[680]) 01b: TS_OUT 10b: ACMP IN+ MUX Output 11b: OA0 V_{REF}
BUF_VREF_SEL[5:0]	RW	Sink/Source Buffer V_{REF} Voltage Selection 000000b: 32 mV 000001b: 64 mV 000010b: 96 mV ⋮ 111110b: 2016 mV 111111b: N/A
BUF_OUT_EN	RW	Source Buffer Output Enable Control 0: Disable (Unbuffered Output) 1: Enable (Buffered Output)
HS_VREF_EN	RW	OpAmp0 High-side V_{REF} Enable Control 0: Disable 1: Enable
HS_VREF_SEL[3:0]	RW	OpAmp0 High-side V_{REF} Voltage Selection 0000b: 10.7 mV / 1000b: 96 mV 0001b: 21.4 mV / 1001b: 106.7 mV 0010b: 32 mV / 1010b: 117.4 mV 0011b: 42.7 mV / 1011b: 128 mV 0100b: 53.4 mV / 1100b: 138.7 mV 0101b: 64 mV / 1101b: 149.4 mV 0110b: 74.7 mV / 1110b: 160 mV 0111b: 85.4 mV / 1111b: 170.7 mV
OA0_VREF_SEL[5:0]	RW	OpAmp0 Low-side V_{REF} Voltage Selection 000000b: 32 mV 000001b: 64 mV 000010b: 96 mV ⋮ 111110b: 2016 mV 111111b: N/A
OA0_VREF_EN_CTRL	RW	OpAmp0 Low-side V_{REF} Enable Control 0: Dynamic ON/OFF 1: Enable
OA1_VREF_SEL[5:0]	RW	OpAmp1 Low-side V_{REF} Voltage Selection 000000b: 32 mV 000001b: 64 mV 000010b: 96 mV ⋮ 111110b: 2016 mV 111111b: N/A
OA1_VREF_EN_CTRL	RW	OpAmp1 Low-side V_{REF} Enable Control 0: Dynamic ON/OFF 1: Enable

Register Name	Access Type	Register Bit Description
OA0_VREF_SUP	RW	OpAmp0 Low-side V_{REF} Supply Voltage Selection 0: 2016 mV 1: V_{DDA}
OA1_VREF_SUP	RW	OpAmp1 Low-side V_{REF} Supply Voltage Selection 0: 2016 mV 1: V_{DDA}
OA0_VREF_EN_SEL	RW	OpAmp0 V_{REF} Enable Selection 0: From Reg[1286] 1: From Connection Matrix Output [59]
OA1_VREF_EN_SEL	RW	OpAmp0 V_{REF} Enable Selection 0: From Reg[1294] 1: From Connection Matrix Output [59]

Table 16. Low-Side V_{REF} Voltage Selection Table

OA0_VREF_SEL[5:0] OA1_VREF_SEL[5:0] BUF_VREF_SEL[5:0]	V_{REF} [V]	OA0_VREF_SEL[5:0] OA1_VREF_SEL[5:0] BUF_VREF_SEL[5:0]	V_{REF} [V]
0 (000000b)	0.032	32 (100000b)	1.056
1 (000001b)	0.064	33 (100001b)	1.088
2 (000010b)	0.096	34 (100010b)	1.120
3 (000011b)	0.128	35 (100011b)	1.152
4 (000100b)	0.160	36 (100100b)	1.184
5 (000101b)	0.192	37 (100101b)	1.216
6 (000110b)	0.224	38 (100110b)	1.248
7 (000111b)	0.256	39 (100111b)	1.280
8 (001000b)	0.288	40 (101000b)	1.312
9 (001001b)	0.320	41 (101001b)	1.344
10 (001010b)	0.352	42 (101010b)	1.376
11 (001011b)	0.384	43 (101011b)	1.408
12 (001100b)	0.416	44 (101100b)	1.440
13 (001101b)	0.448	45 (101101b)	1.472
14 (001110b)	0.480	46 (101110b)	1.504
15 (001111b)	0.512	47 (101111b)	1.536
16 (010000b)	0.544	48 (110000b)	1.568
17 (010001b)	0.576	49 (110001b)	1.600
18 (010010b)	0.608	50 (110010b)	1.632

OA0_VREF_SEL[5:0] OA1_VREF_SEL[5:0] BUF_VREF_SEL[5:0]	V_{REF} [V]	OA0_VREF_SEL[5:0] OA1_VREF_SEL[5:0] BUF_VREF_SEL[5:0]	V_{REF} [V]
19 (010011b)	0.640	51 (110011b)	1.664
20 (010100b)	0.672	52 (110100b)	1.696
21 (010101b)	0.704	53 (110101b)	1.728
22 (010110b)	0.736	54 (110110b)	1.760
23 (010111b)	0.768	55 (110111b)	1.792
24 (011000b)	0.800	56 (111000b)	1.824
25 (011001b)	0.832	57 (111001b)	1.856
26 (011010b)	0.864	58 (111010b)	1.888
27 (011011b)	0.896	59 (111011b)	1.920
28 (011100b)	0.928	60 (111100b)	1.952
29 (011101b)	0.960	61 (111101b)	1.984
30 (011110b)	0.992	62 (111110b)	2.016
31 (011111b)	1.024	63 (111111b)	N/A

9.2 Typical Performance of V_{REF} Generator and Sink/Source Buffer

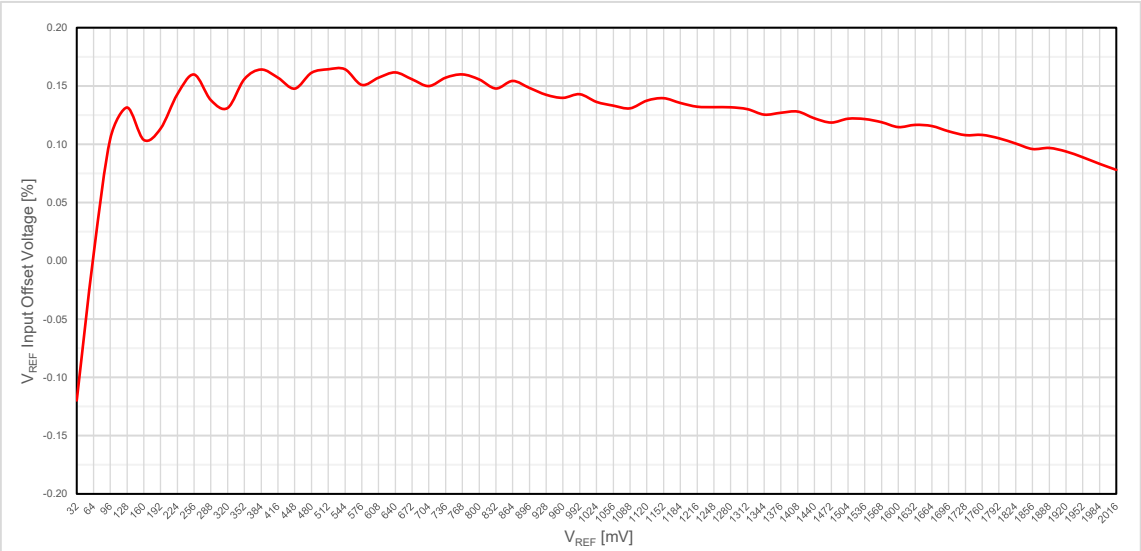


Figure 54. Typical V_{REF} Offset Voltage vs. V_{REF} at V_{DD} = 2.3 V to 5.5 V, T_A = +25 °C, Buffer Disabled

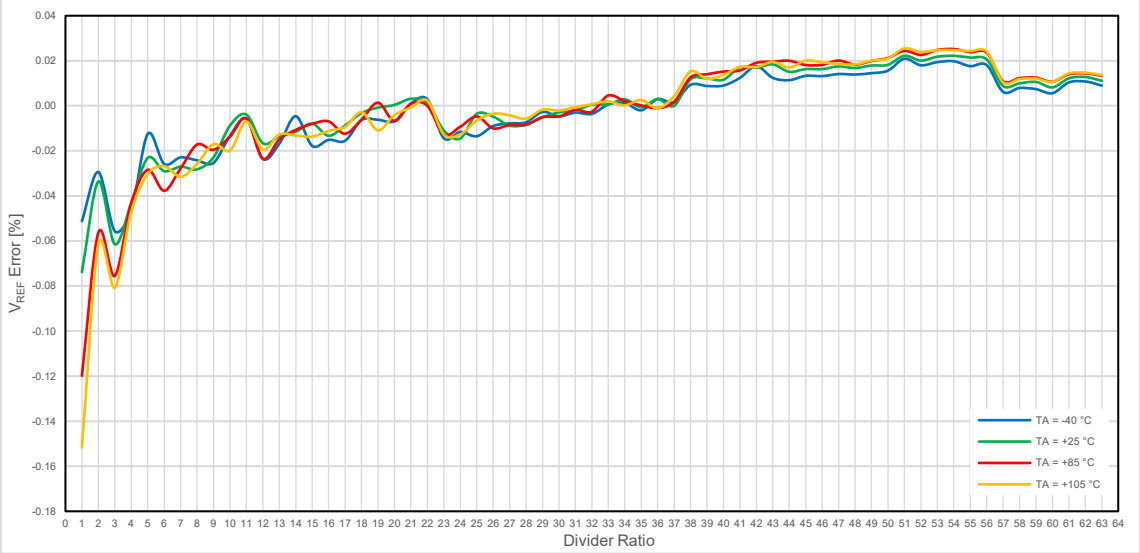


Figure 55. OpAmp V_{REF} Divider Accuracy at V_{DDA} = 3.3 V

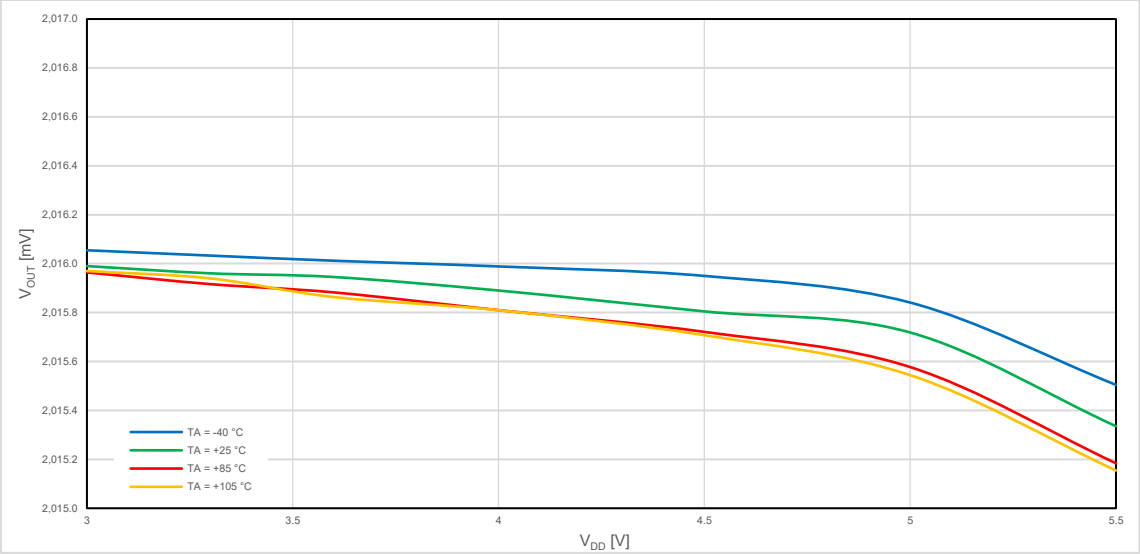


Figure 56. Typical Line Regulation in Source Mode at V_{REF} = 2016 mV, I_{LOAD} = 5 mA

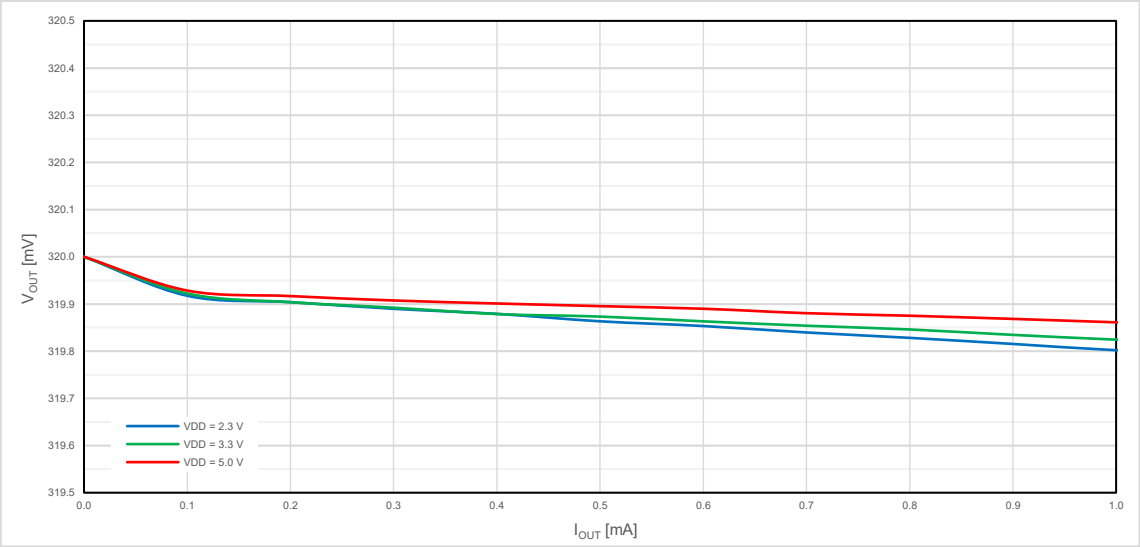


Figure 57. Typical Load Regulation in Source Mode at V_{REF} = 320 mV, T_A = -40 °C to +105 °C

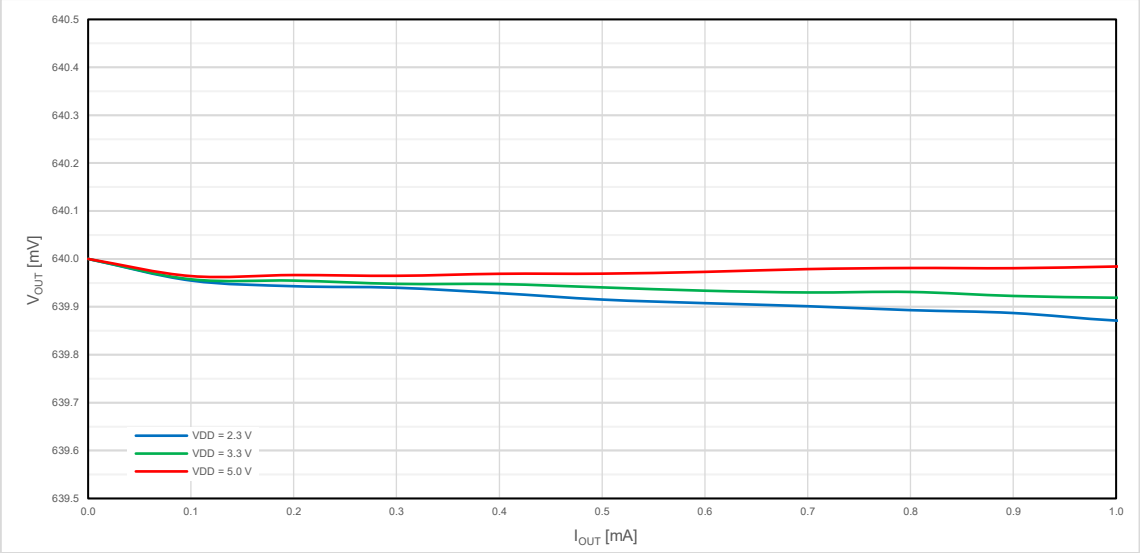


Figure 58. Typical Load Regulation in Source Mode at V_{REF} = 640 mV, T_A = -40 °C to +105 °C

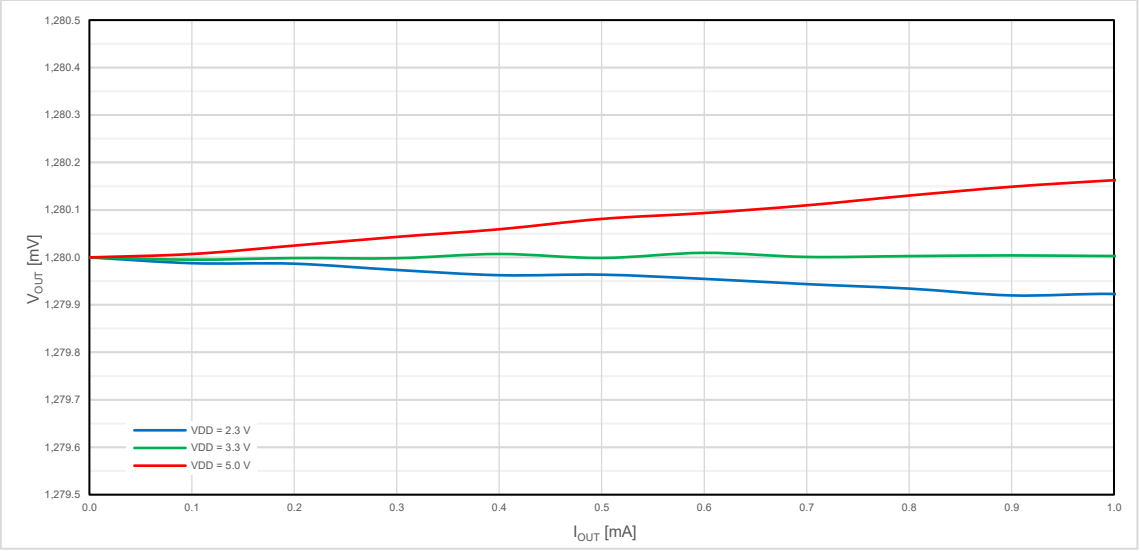


Figure 59. Typical Load Regulation in Source Mode at V_{REF} = 1280 mV, T_A = -40 °C to +105 °C

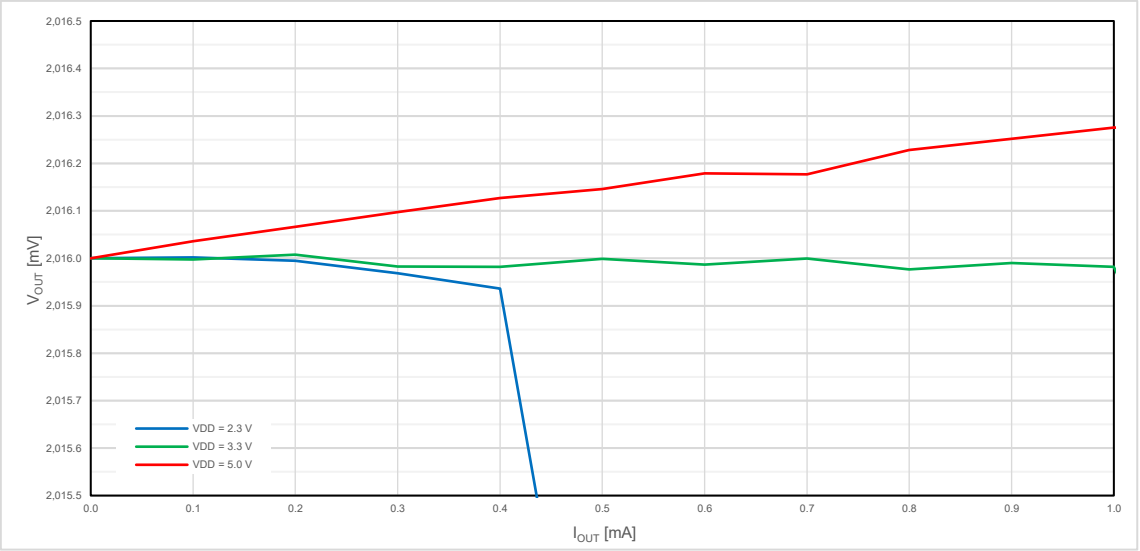


Figure 60. Typical Load Regulation in Source Mode at V_{REF} = 2016 mV, T_A = -40 °C to +105 °C

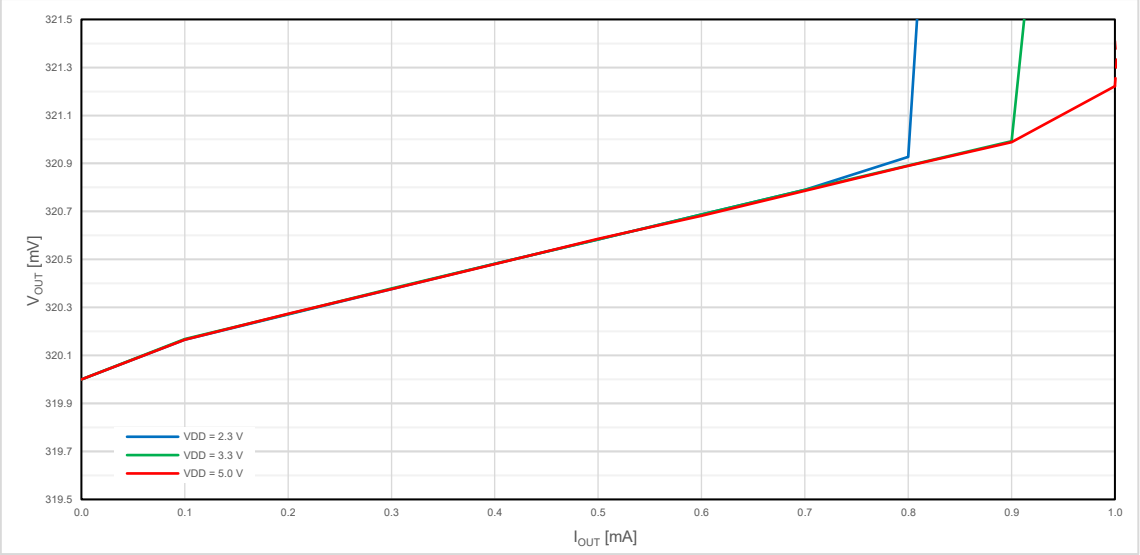


Figure 61. Typical Load Regulation in Sink Mode at V_{REF} = 320 mV, T_A = -40 °C to +105 °C

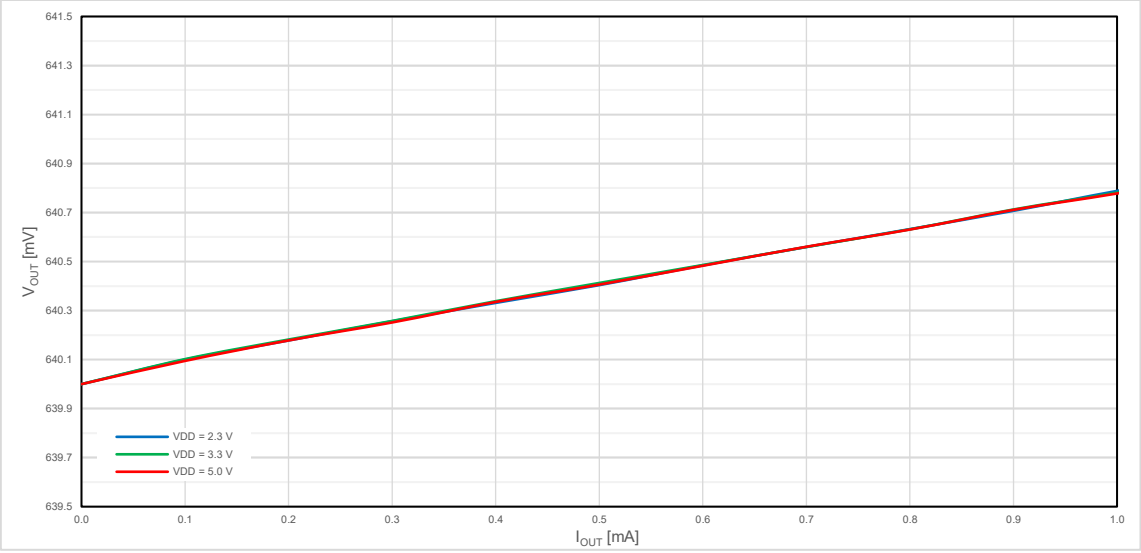


Figure 62. Typical Load Regulation in Sink Mode at V_{REF} = 640 mV, T_A = -40 °C to +105 °C

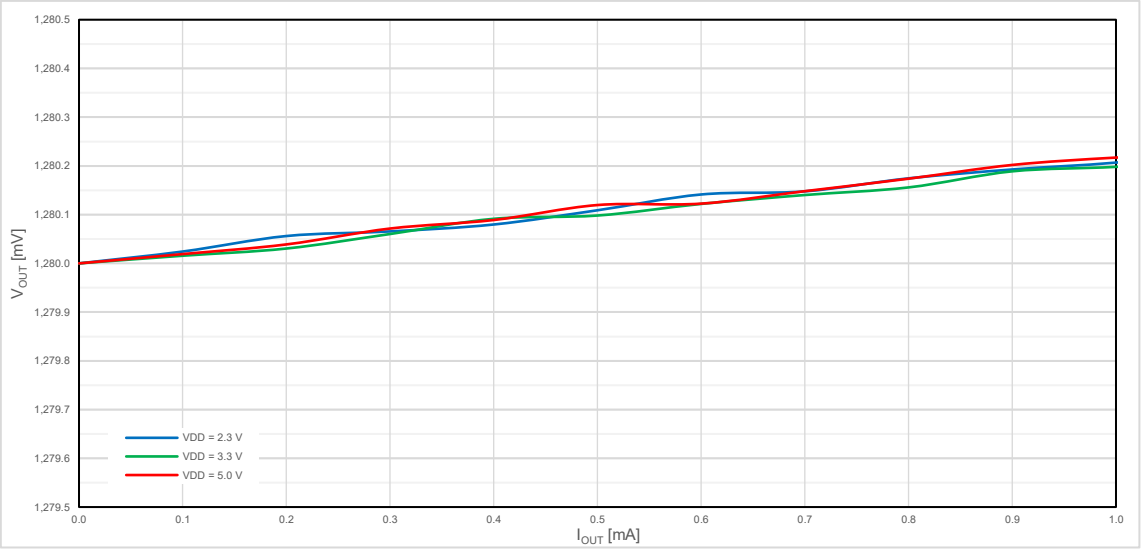


Figure 63. Typical Load Regulation in Sink Mode at V_{REF} = 1280 mV, T_A = -40 °C to +105 °C

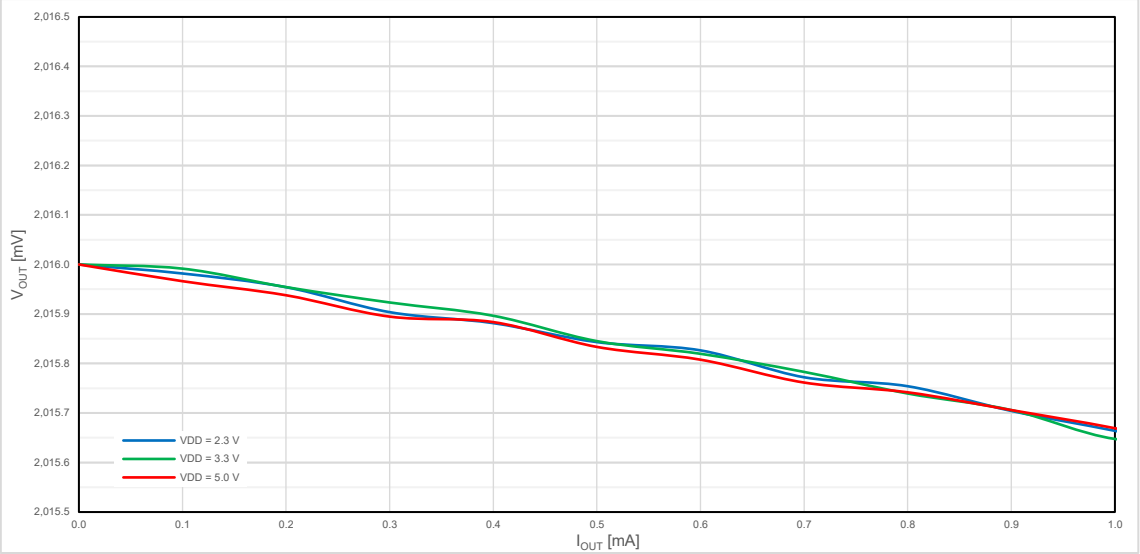


Figure 64. Typical Load Regulation in Sink Mode at V_{REF} = 2016 mV, T_A = -40 °C to +105 °C

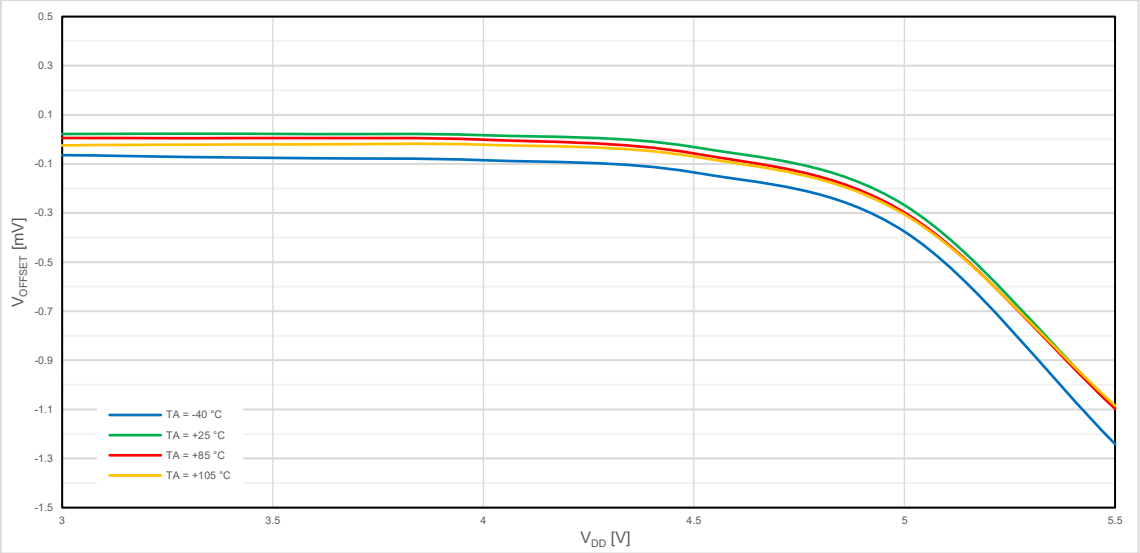


Figure 65. Sink/Source Buffer Offset vs. V_{DD}

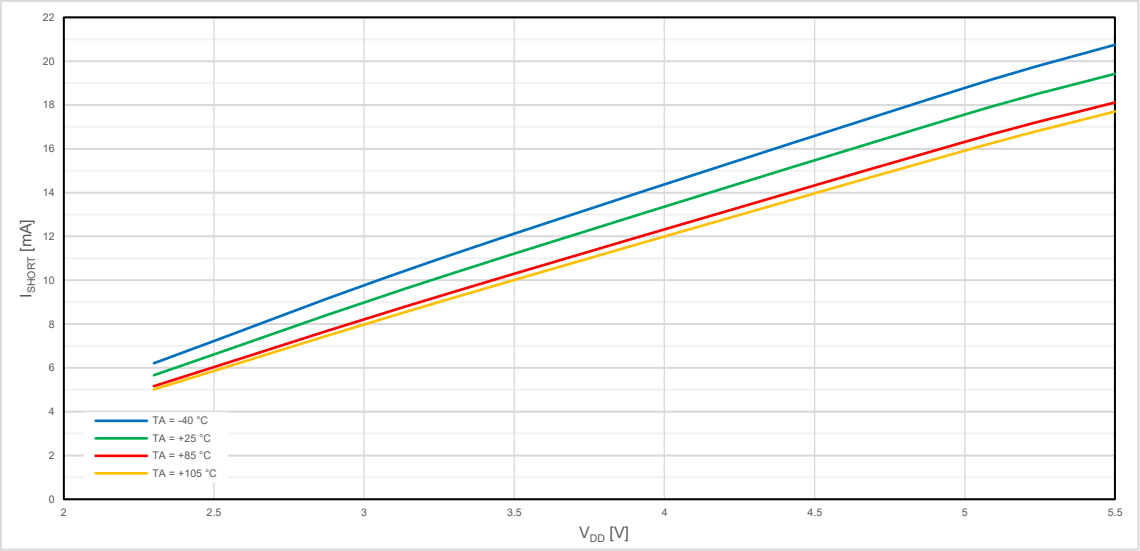


Figure 66. Sink/Source Buffer Short-Circuit Current vs. V_{DD}

10. Operational Amplifiers

10.1 OpAmp General Description

The SLG47001-E/03-E contains two operational amplifiers with rail-to-rail input and output (RRIO). The SLG47001-E/03-E uses a proprietary chopper-stabilized architecture as shown in Figure 67. The main amplifier is combined with a very high open-loop gain chopper-stabilized amplifier to achieve very low offset voltage and drift while consuming very low supply current. This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain chopper stabilized DC correction amplifier operating at 100 kHz. From DC to ~5 kHz, both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5 kHz crossover filter cuts off the low frequency amplifier path leaving the main amplifier active out to the 400 kHz gain-bandwidth product of the device. The key benefits of this architecture for precision applications are very high open loop gain, very low DC offset, and low 1/f noise. The noise is virtually flat across the frequency range from a few MHz out to 100 kHz, except for the narrow noise peak at the amplifier crossover frequency (5 kHz).

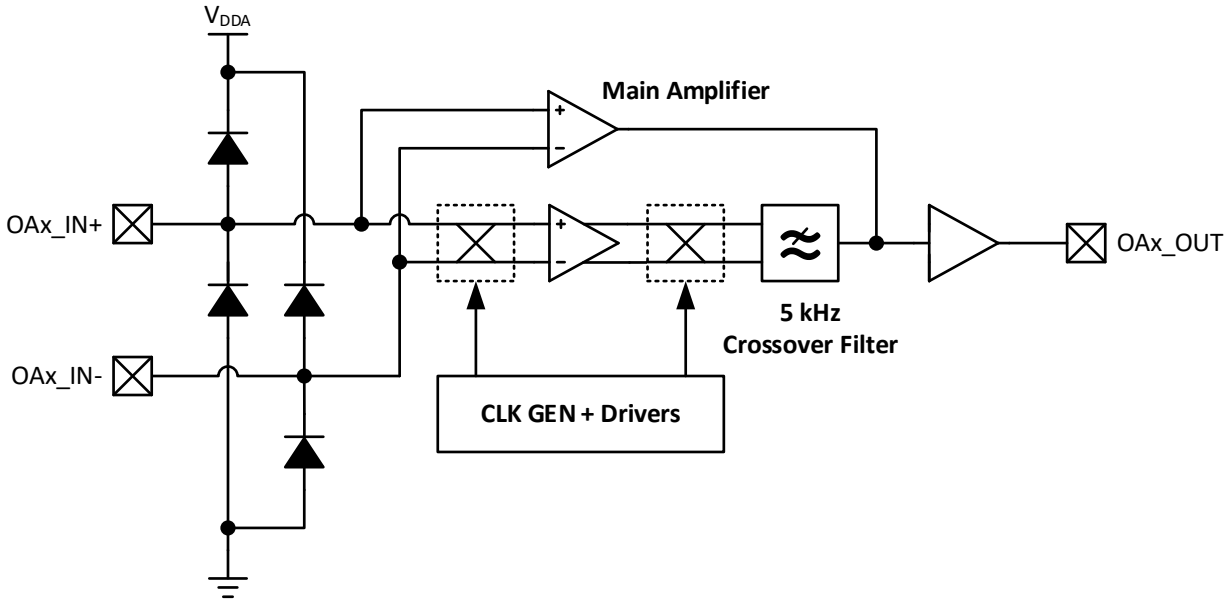


Figure 67. OpAmp Internal Structure

The ultra-low input offset voltage of the OpAmp can be degraded when large differential voltages are applied between its positive and negative inputs for very long time periods. For example, a 2 V differential voltage across the inputs over 168 hours can shift the input offset voltage by a few microvolts (µV). In case the OpAmp is subjected to large differential input voltages even when it is disabled, adding back-to-back diodes (see Figure 68) can ensure that the DC precision of the OpAmp is retained by preventing large differential voltages at the inputs. Such diode clamps are not needed if the OpAmps are always in close-loop operation where the differential voltage of the inputs is naturally kept small.

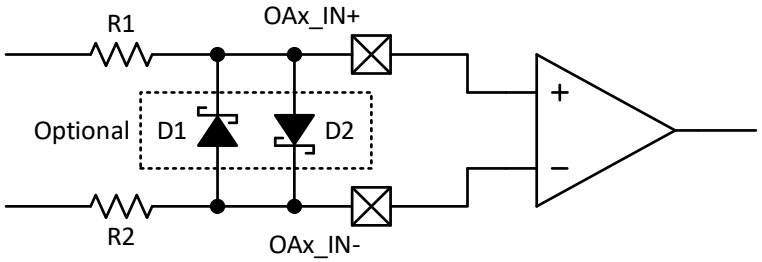


Figure 68. Differential Input Voltage Limiting Circuit using Diode Clamping

Table 17. OpAmp Configuration Registers

Register Name	Access Type	Register Bit Description
OA0_VREF_IN_EN	RW	OpAmp0 Low-side V_{REF} Input Enable Control 0: Disable 1: Enable (V_{REF} is connected to one of inputs of OpAmp0)
OA1_VREF_IN_EN	RW	OpAmp1 Low-side V_{REF} Input Enable Control 0: Disable 1: Enable (V_{REF} is connected to one of inputs of OpAmp1)
OA0_VREF_IN_SEL	RW	OpAmp0 V_{REF} Input Selection 0: V_{REF} Output to Negative Input of OpAmp0 1: V_{REF} Output to Positive Input of OpAmp0
OA1_VREF_IN_SEL	RW	OpAmp1 V_{REF} Input Selection 0: V_{REF} Output to Negative Input of OpAmp1 1: V_{REF} Output to Positive Input of OpAmp1
OA0_PD_CTRL	RW	OpAmp0 Pull-Down Enable Control 0: Enable (Typ. 1 kΩ Pull-Down) 1: Disable (Hi-Z)
OA1_PD_CTRL	RW	OpAmp1 Pull-Down Enable Control 0: Enable (Typ. 1 kΩ Pull-Down) 1: Disable (Hi-Z)

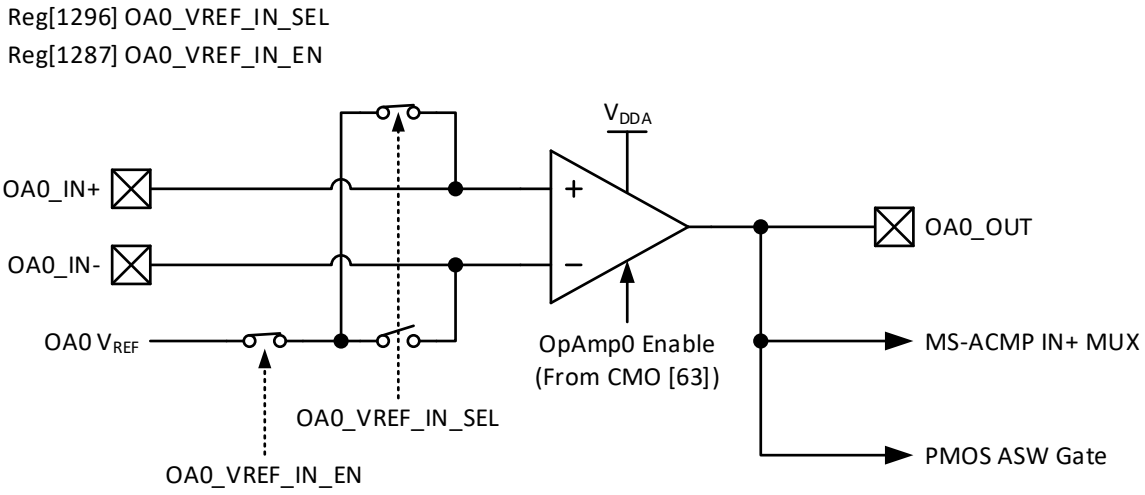


Figure 69. Operational Amplifier0 Circuit

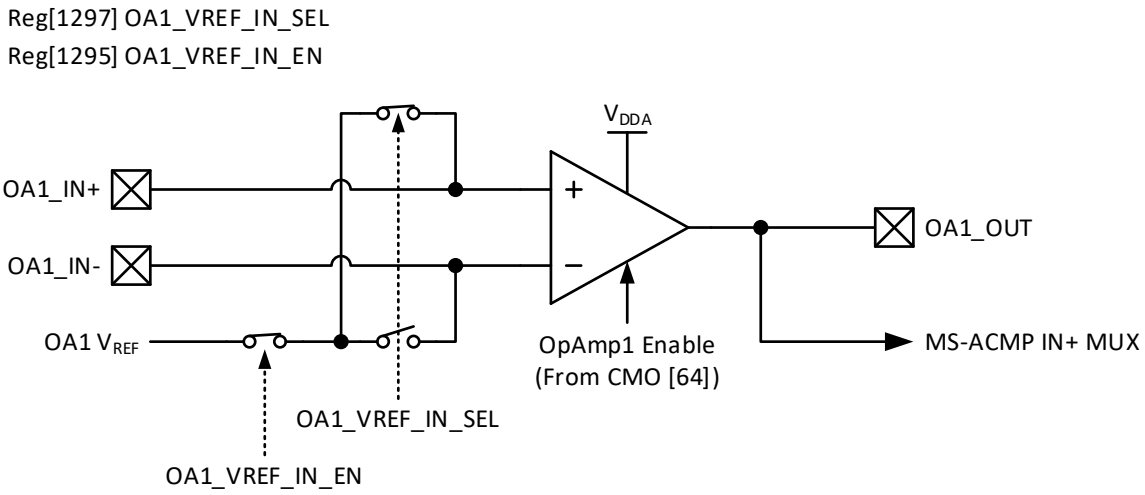


Figure 70. Operational Amplifier1 Circuit

As shown in Figure 69, only OpAmp0 has an additional function of driving the internal analog switch (OpAmp Switch Control Mode). The internal voltage reference (V_{REF}) can be connected to the inputs of the operational amplifiers by the OAx_VREF_IN_EN and the OAx_VREF_IN_SEL bits.

Each of the two OpAmp inputs has a hardware connection to the external pin and an optional connection to the internal voltage reference source, which makes it possible to generate a precise voltage or a current source. For more detailed description of the OpAmp V_{REF} sources (see section 9 Internal Voltage Reference).

10.2 Modes of Operation

To use OpAmp macrocells in the “Go Configure™ Software Hub”, the power-up signal (PWR_UP) must be set to logic high. By default, all OpAmp macrocells are turned off after the device starts up. During power-up, the outputs of OpAmp0 and OpAmp1 are initially determined by the OA0_PD_CTRL (Reg[1401]) and the OA1_PD_CTRL (Reg[1402]) respectively, and then becomes valid in 140 µs.

See the list below for the OpAmp operation modes:

- Operational Amplifier Mode
- OpAmp Switch Control Mode.

In both modes, the output of the OpAmp macrocell is determined by the OAx_PD_CTRL register (0: Typ. 1 kΩ Pull-Down, 1: Hi-Z) while the corresponding macrocell is turned off.

10.2.1 Operational Amplifier Mode

In this mode, the OpAmp operates as a conventional operational amplifier. Also, the outputs of the operational amplifiers (OA0_OUT and OA1_OUT) can be fed to the corresponding non-inverting inputs of the MS-ACMP (see section 12 Multi-Channel Sampling Analog Comparator).

10.2.2 OpAmp Switch Control Mode

In this mode, the OpAmp output is used to drive gate voltage for the PMOS of the analog switch. The OpAmp switch control mode is enabled by setting the ASW_MODE bit to ‘1’. When the OpAmp switch mode is disabled (ASW_MODE = 0), the output of OpAmp0 (OA0_OUT) is disconnected from the gate of the PMOS. Figure 71 (A) shows a typical implementation of the voltage source function. Optionally, this mode can be used to implement a constant current-source with load connected to ground as shown in Figure 71 (B) and (C).

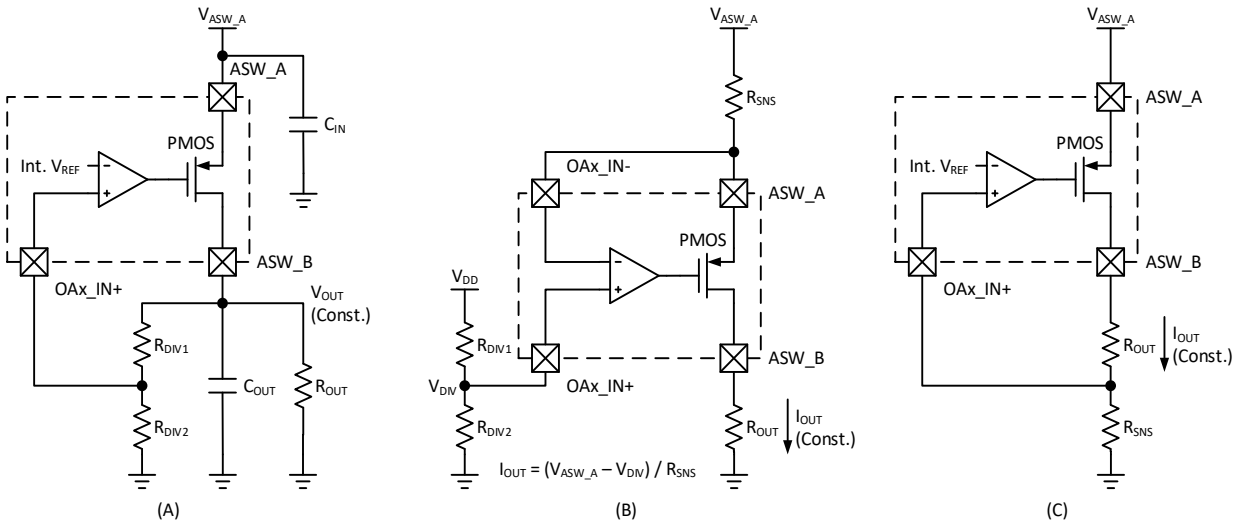


Figure 71. Typical Implementation of Voltage Regulator (A) and Current Sources (B and C)

10.3 Typical Performance of OpAmp

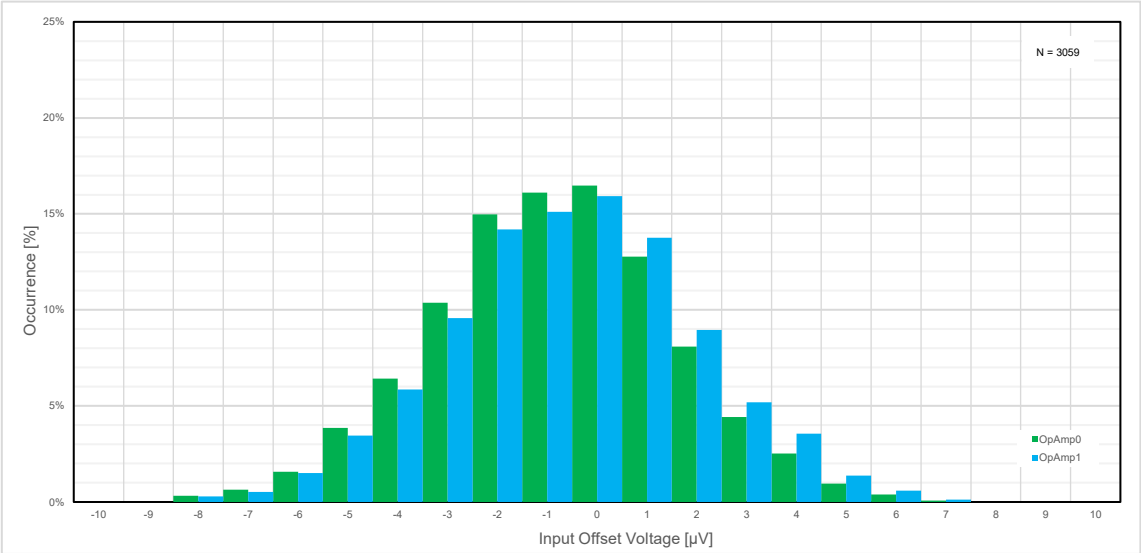


Figure 72. OpAmp Input Offset Voltage Distribution at V_{DDA} = 5 V, V_{CM} = V_{DDA}/2, T_A = +25 °C

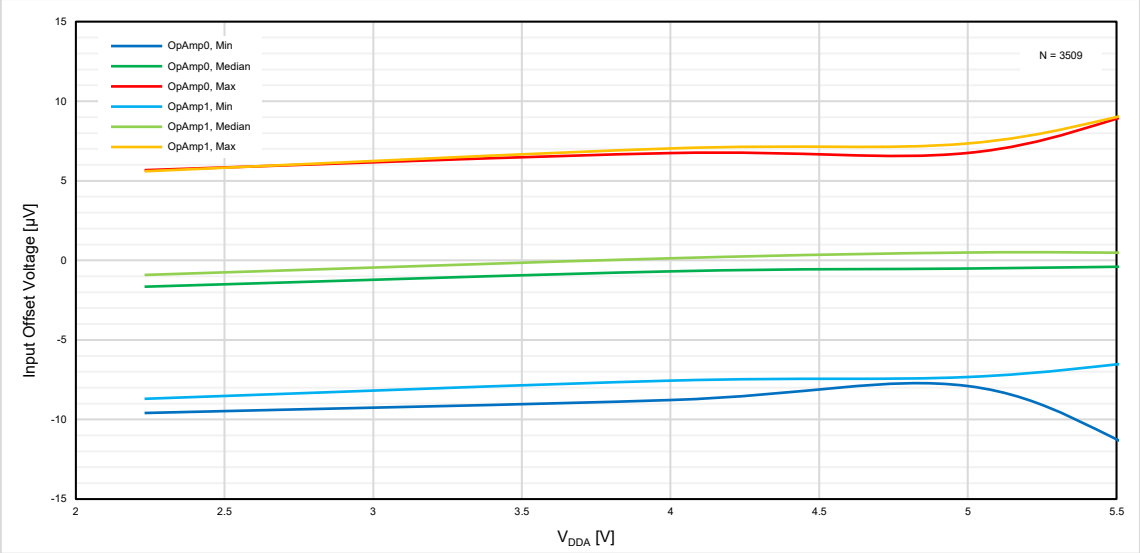


Figure 73. OpAmp Input Offset Voltage vs. V_{DDA} at T_A = +25 °C

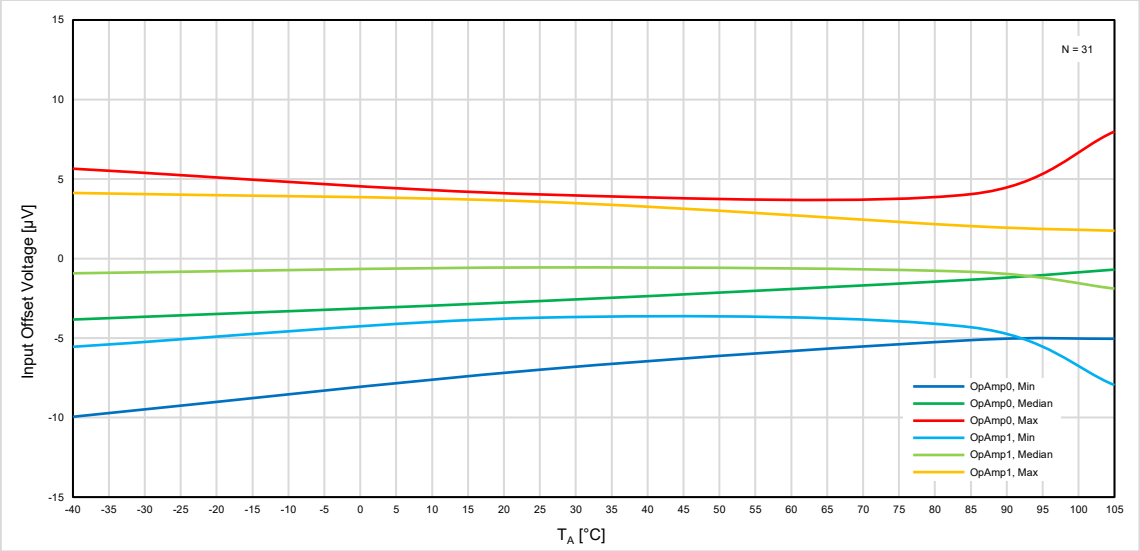


Figure 74. OpAmp Input Offset Voltage vs. T_A at V_{DDA} = 5 V, V_{CM} = V_{DDA}/2

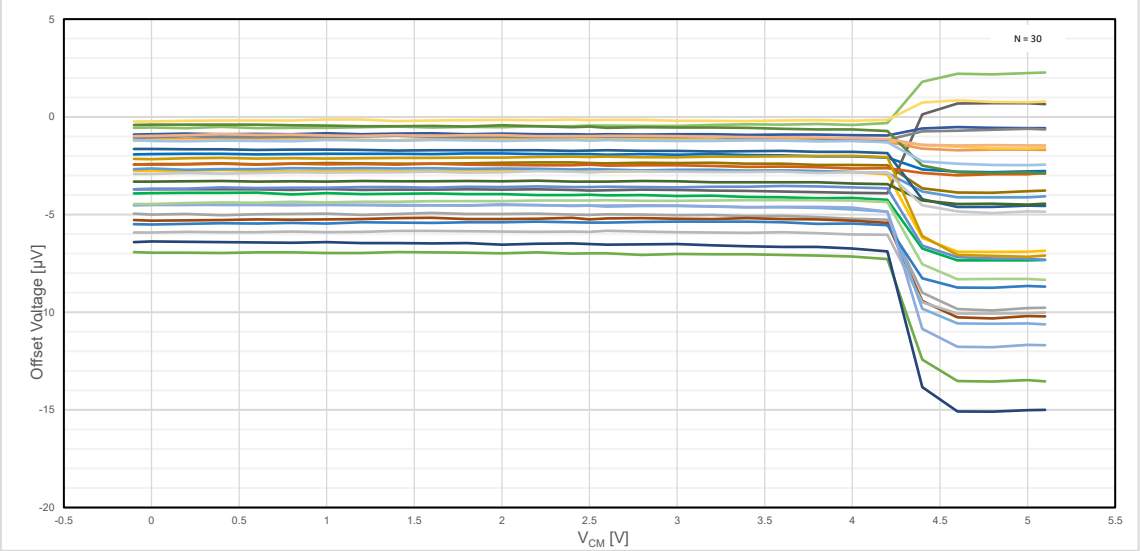


Figure 75. OpAmp Input Offset Voltage vs. V_{CM} at V_{DDA} = 5 V, T_A = +25 °C

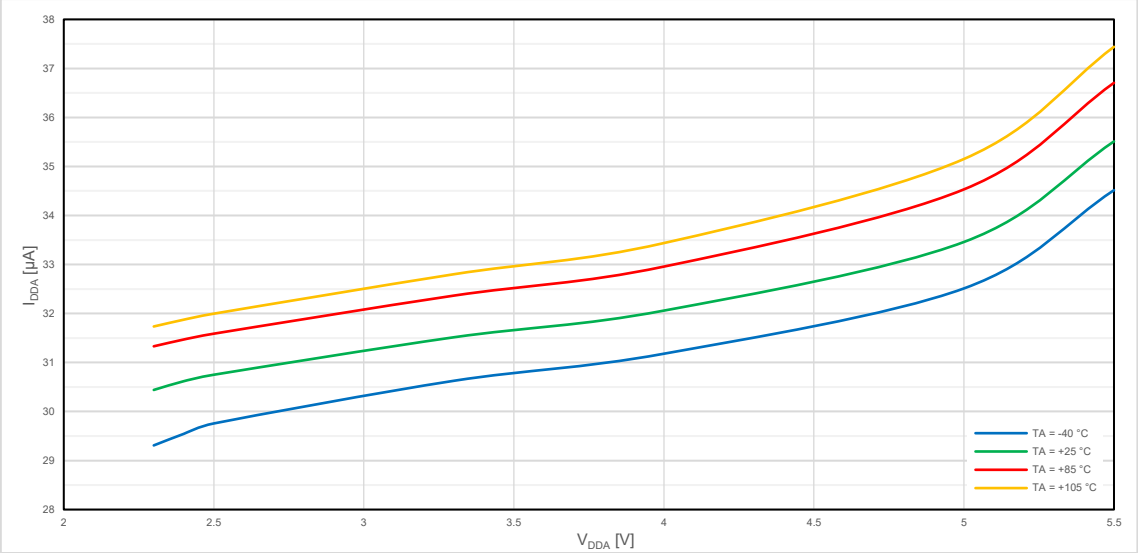


Figure 76. OpAmp Quiescent Current vs. V_{DDA}

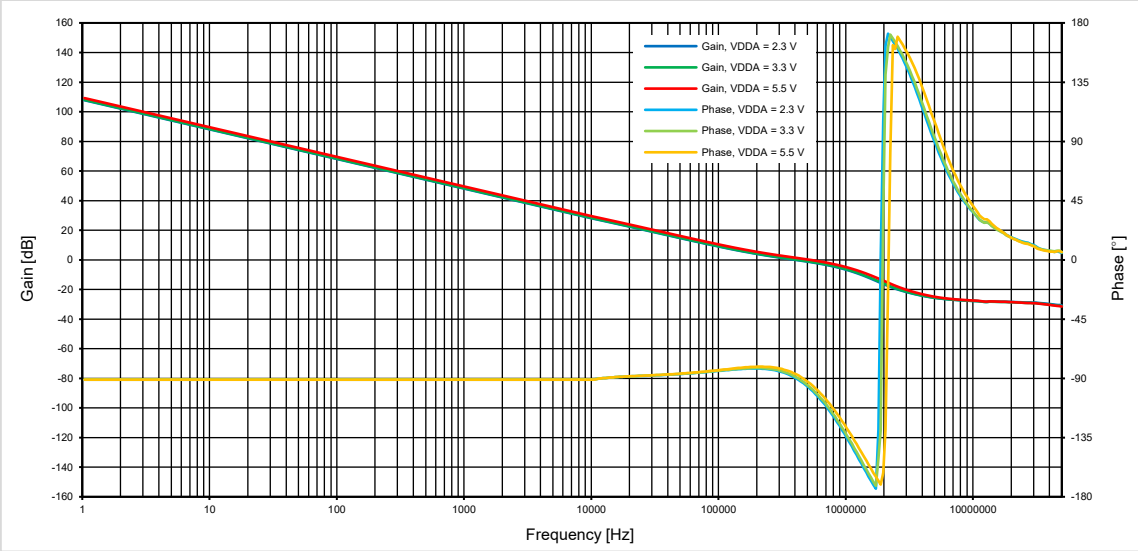


Figure 77. OpAmp0 Open-Loop Gain and Phase vs. Frequency at R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF

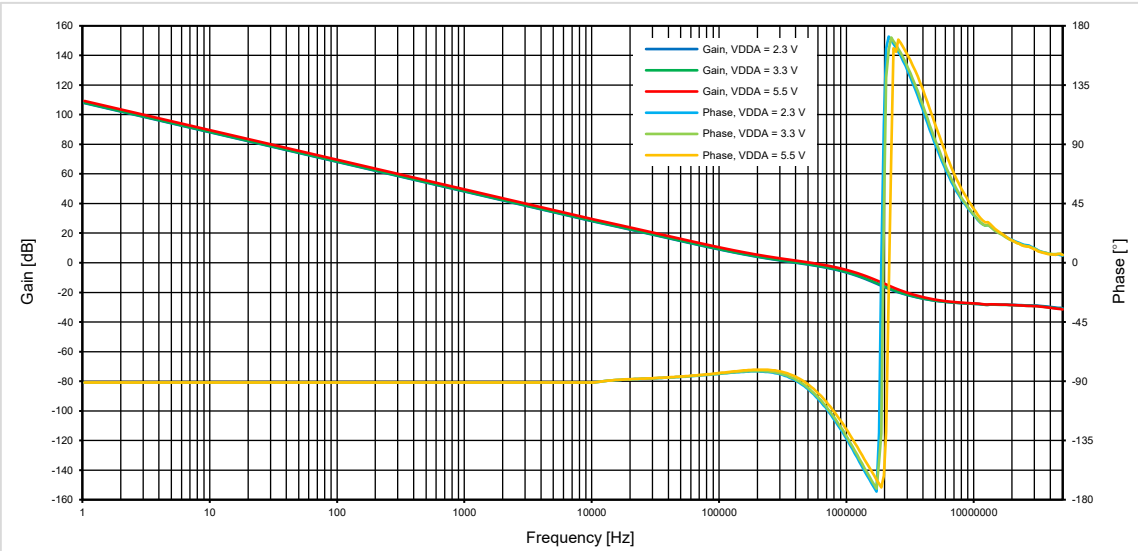


Figure 78. OpAmp1 Open-Loop Gain and Phase vs. Frequency at R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF

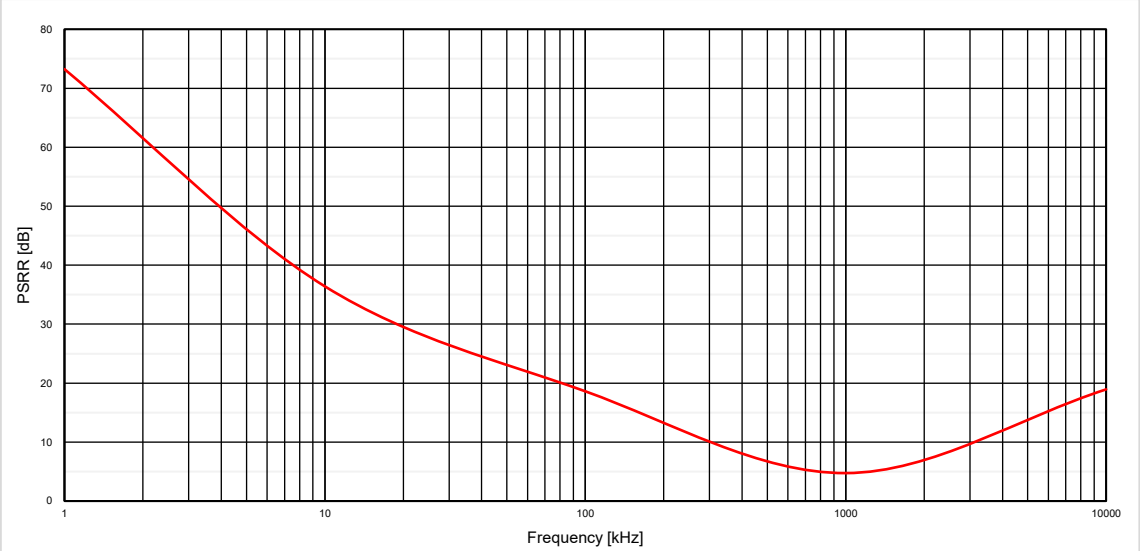


Figure 79. OpAmp PSRR vs. Frequency at V_{DDA} = 2.3 V to 5.5 V

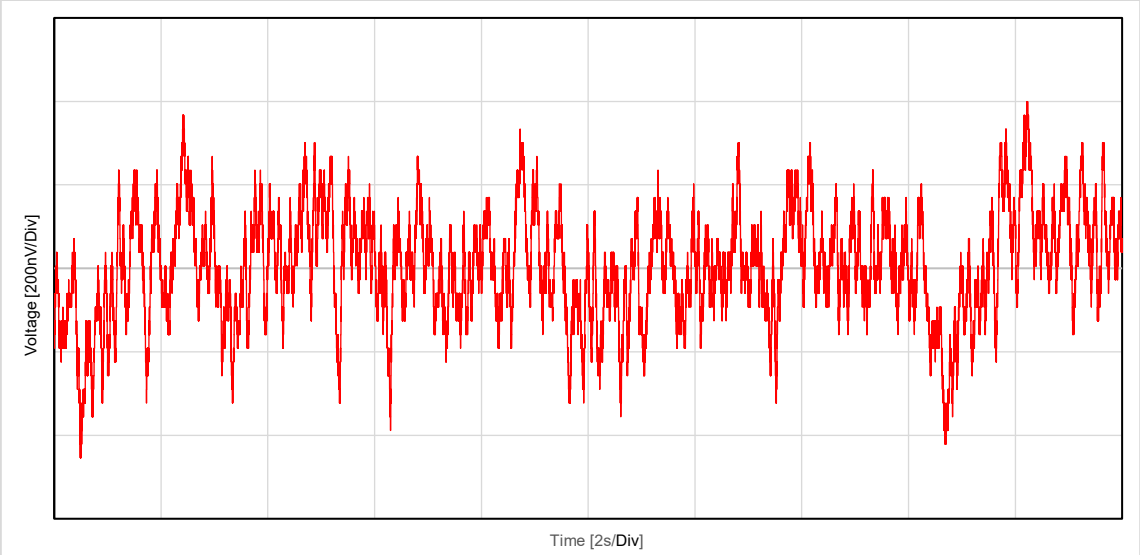


Figure 80. OpAmp 0.1 Hz to 10 Hz Noise at V_{DDA} = 5 V, V_{CM} = V_{DDA}/2, T_A = +25 °C

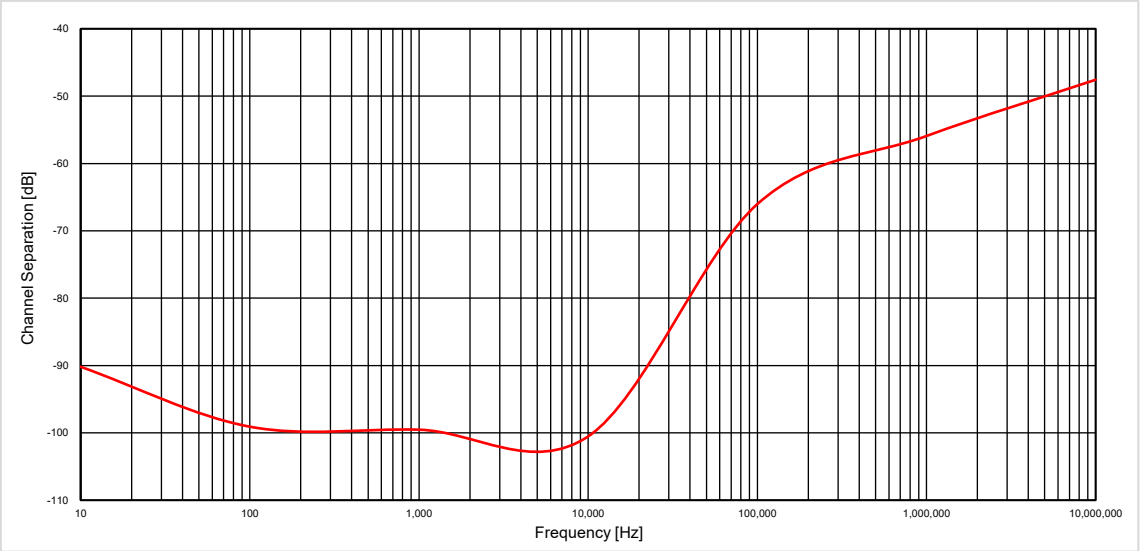


Figure 81. OpAmp Channel Separation vs. Frequency at T_A = +25 °C

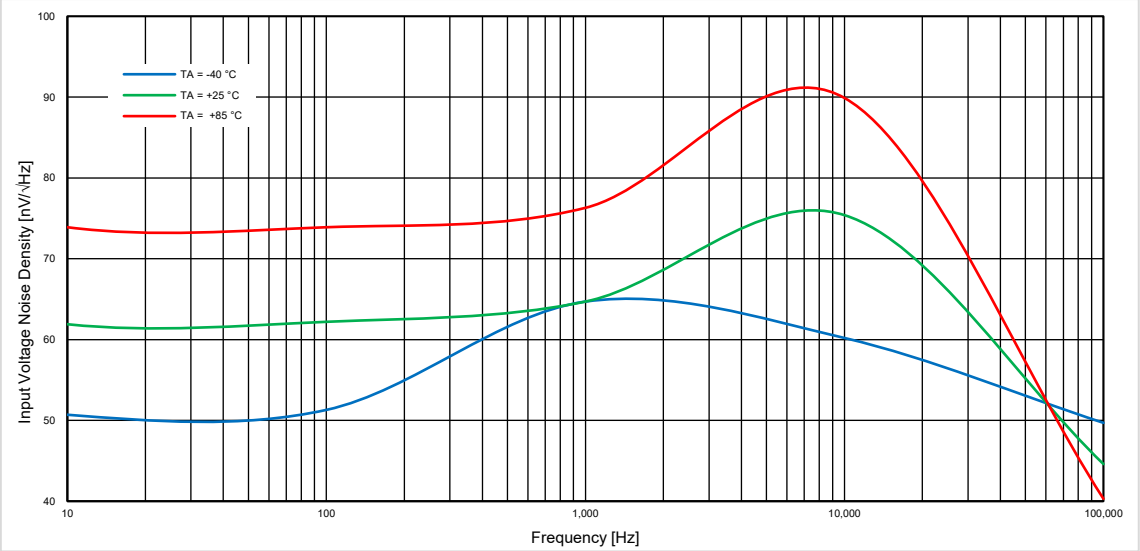


Figure 82. OpAmp Noise Voltage Density vs. Frequency

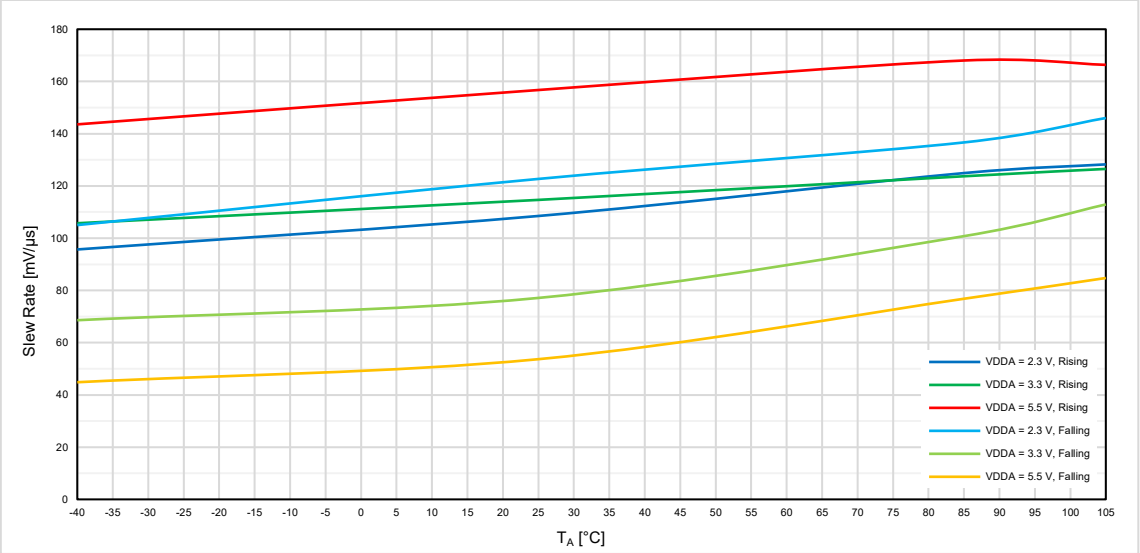


Figure 83. OpAmp Slew-Rate between 10 % and 90 % vs. T_A at G = 1, R_{LOAD} = 50 kΩ

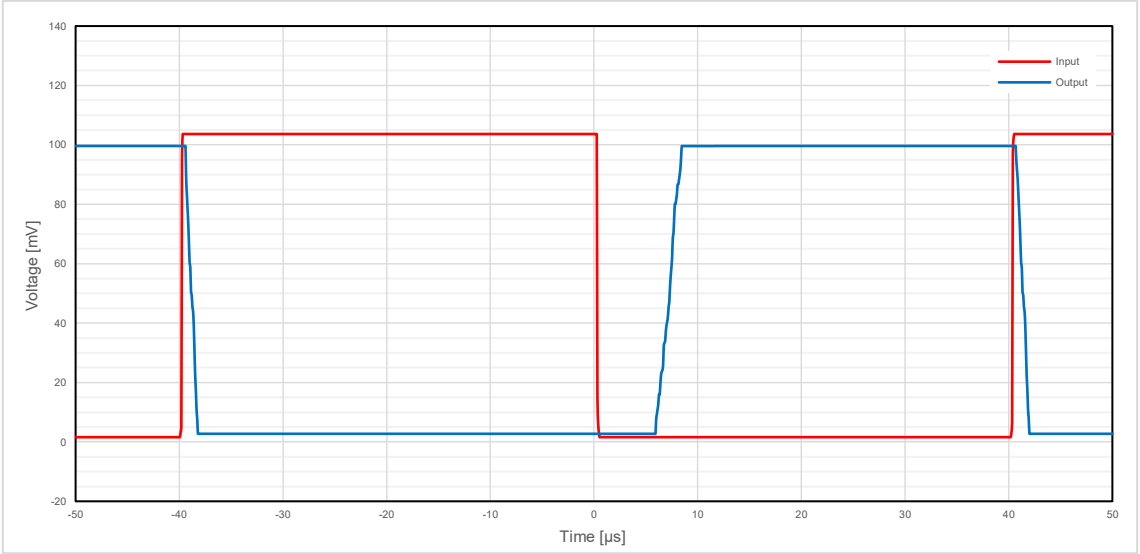


Figure 84. OpAmp Small Signal Inverting Step Response at G = -1, R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF

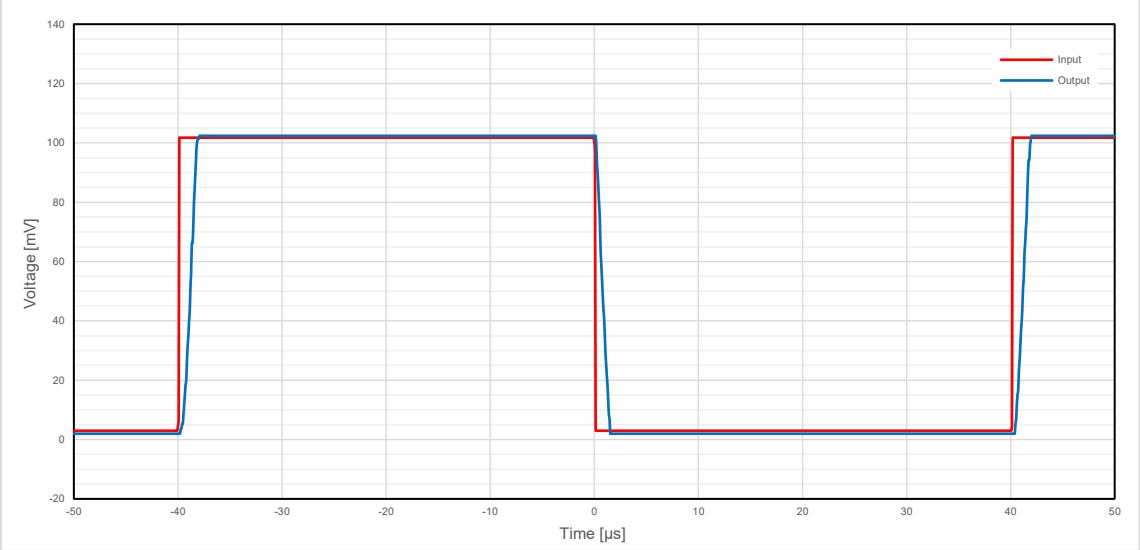


Figure 85. OpAmp Small Signal Non-Inverting Step Response at G = 1, R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF

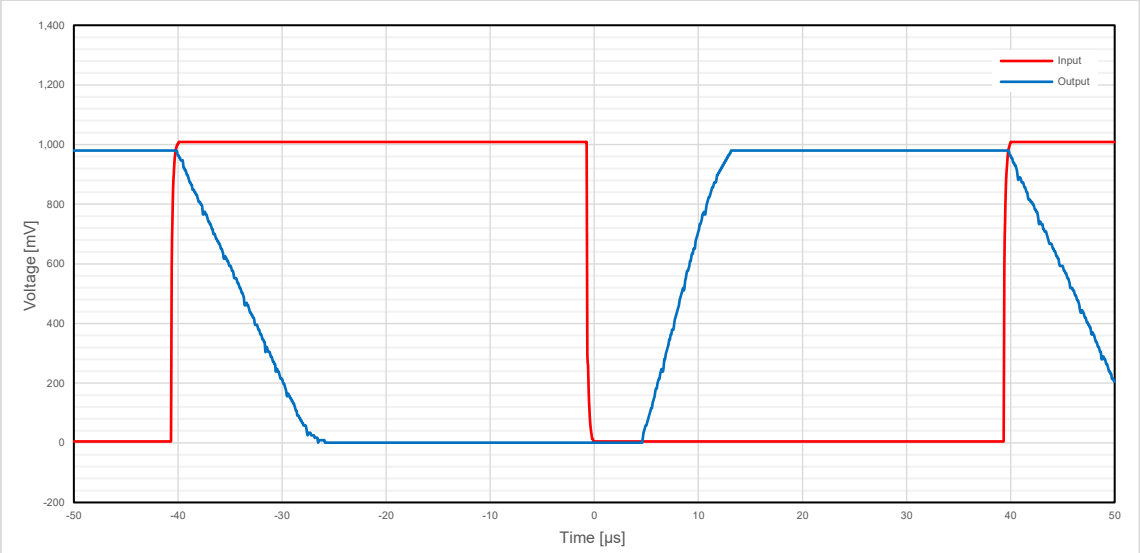


Figure 86. OpAmp Large Signal Inverting Step Response at G = -1, R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF

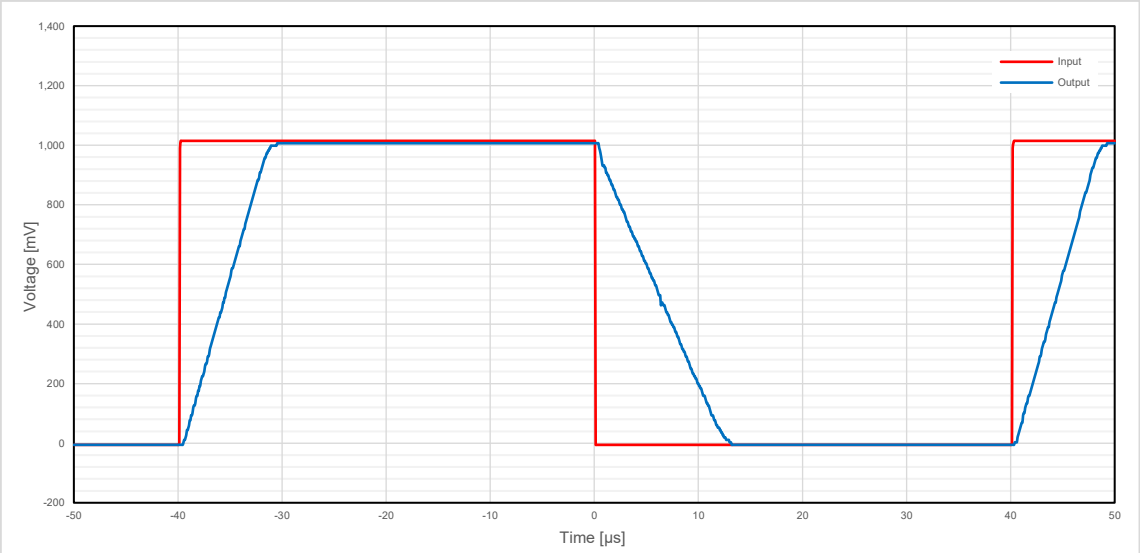


Figure 87. OpAmp Large Signal Non-Inverting Step Response at G = 1, R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF

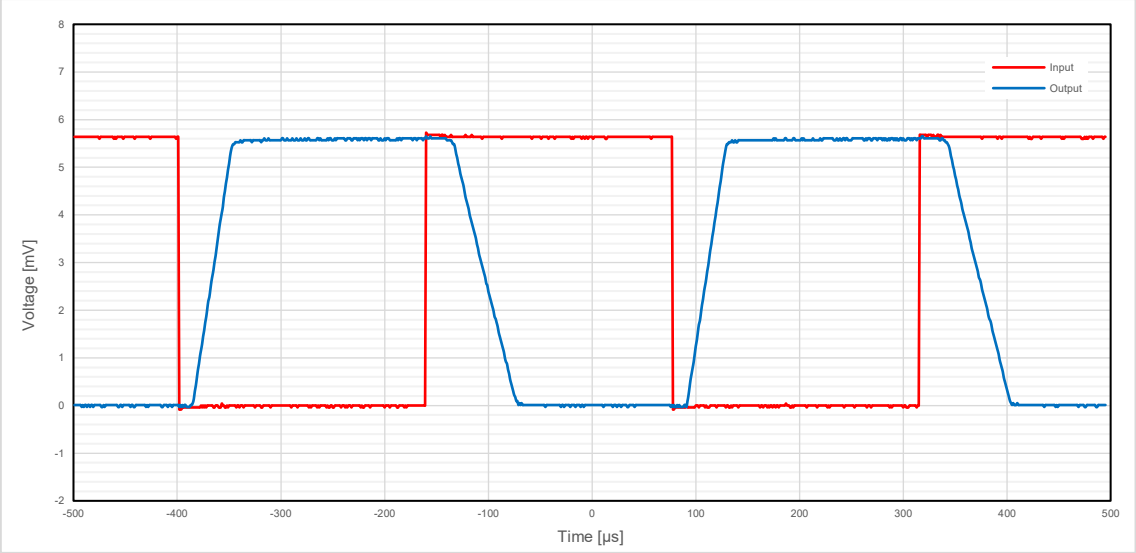


Figure 88. OpAmp Inverting Overload Recovery at G = -1, R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF

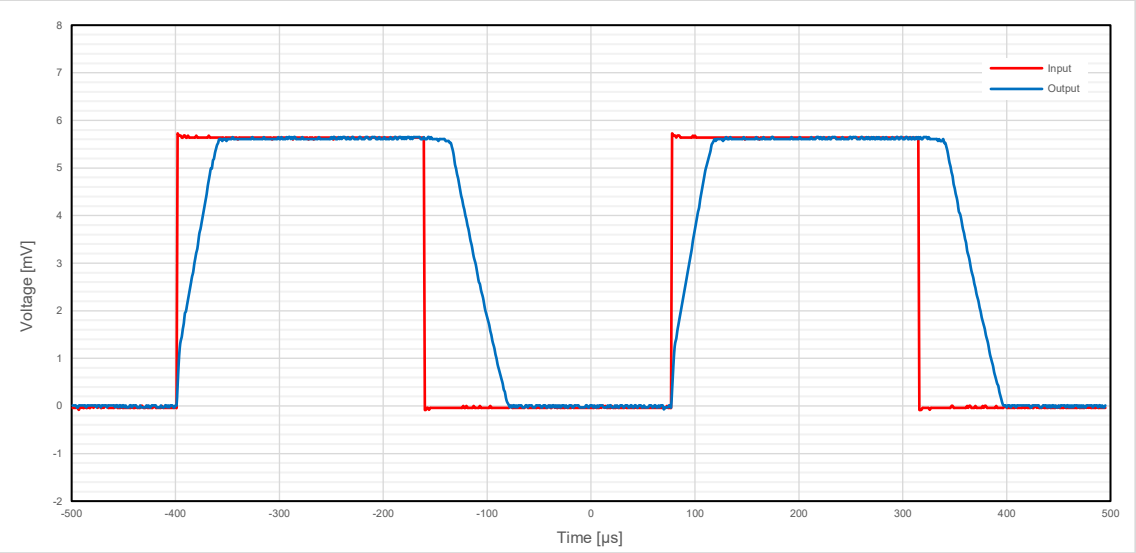


Figure 89. OpAmp Non-Inverting Overload Recovery at G = 1, R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF

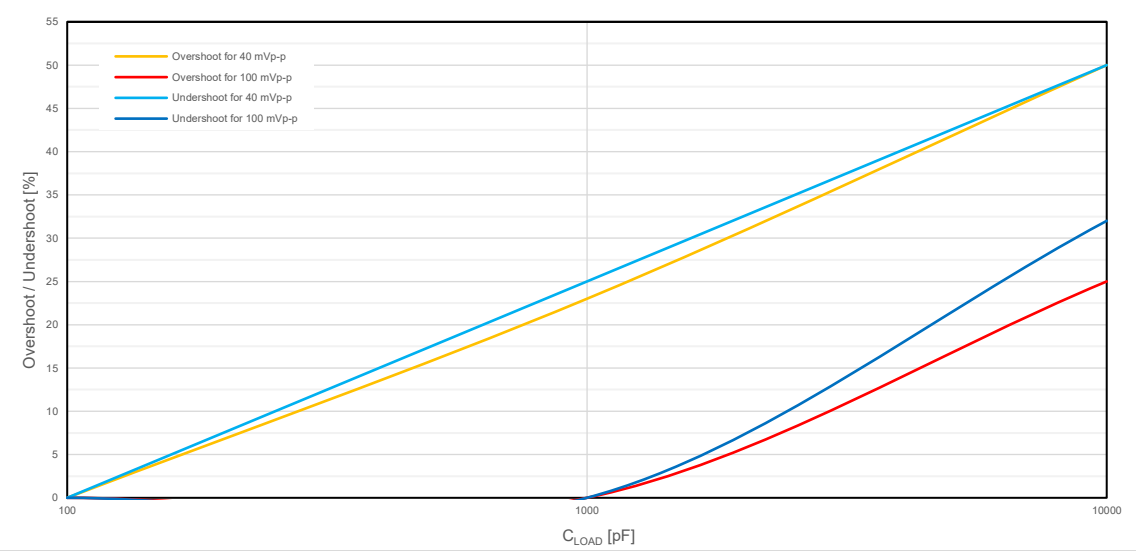


Figure 90. OpAmp Small Signal Overshoot vs. Capacitive Load at V_{DDA} = 3.3 V, G = 1

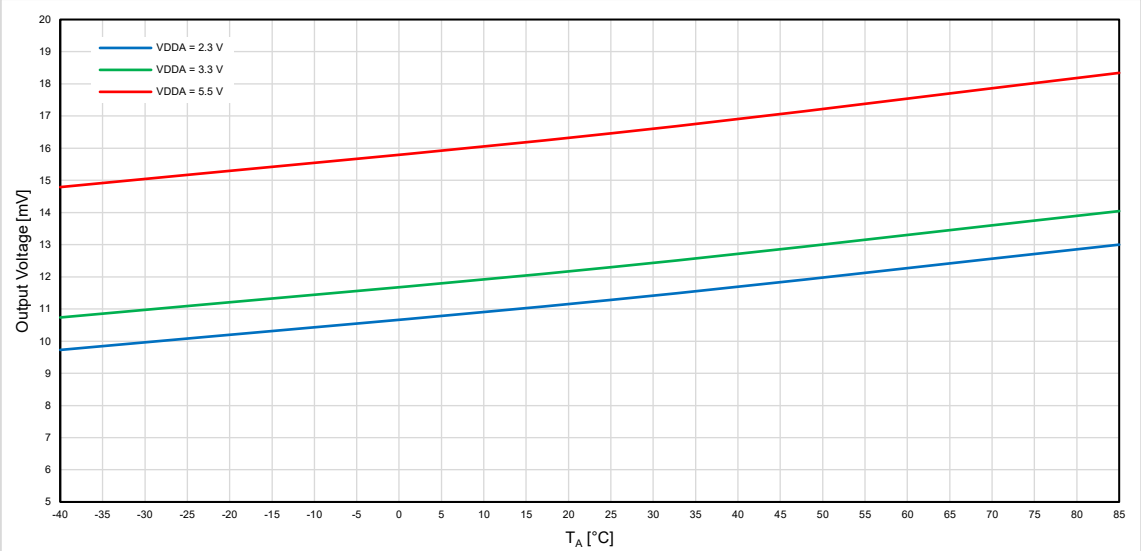


Figure 91. OpAmp Output Voltage Low (V_{OAx_OUT} – GND) vs. T_A at R_{LOAD} = 10 kΩ

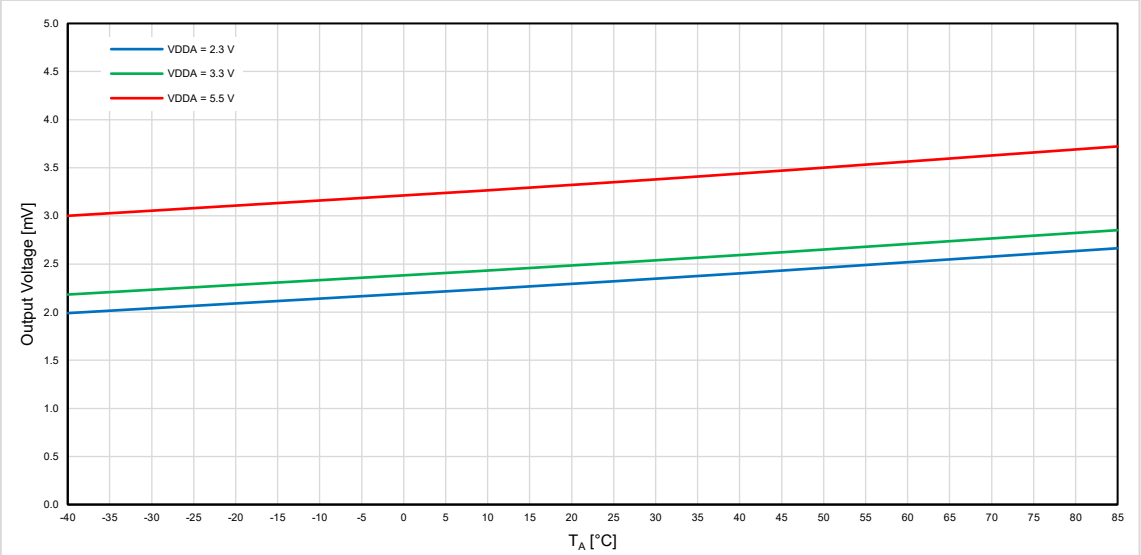


Figure 92. OpAmp Output Voltage Low (V_{OAx_OUT} – GND) vs. T_A at R_{LOAD} = 50 kΩ

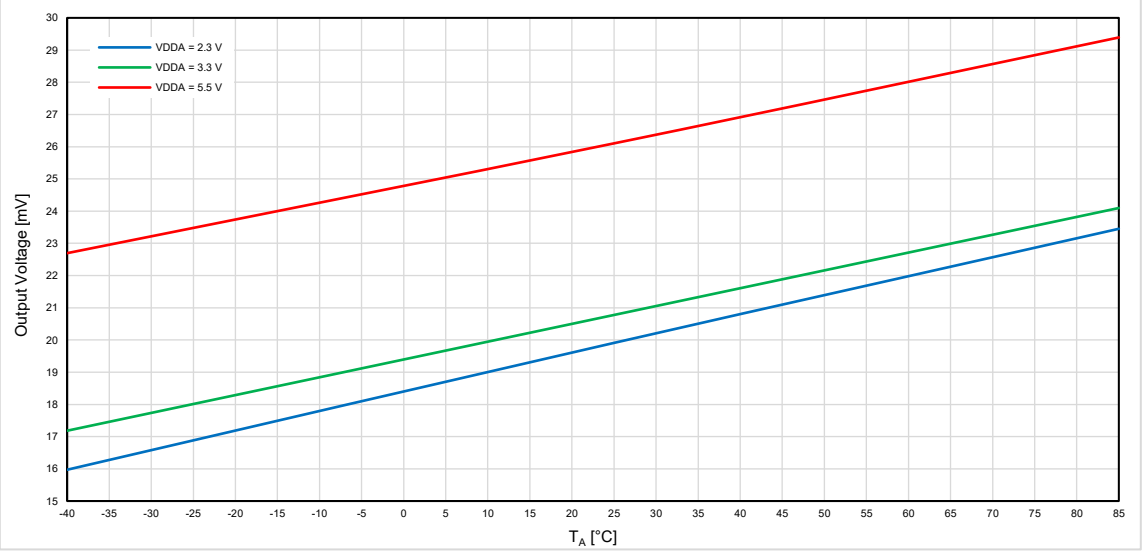


Figure 93. OpAmp Output Voltage High (V_{DDA} - V_{OAx_OUT}) vs. T_A at R_{LOAD} = 10 kΩ

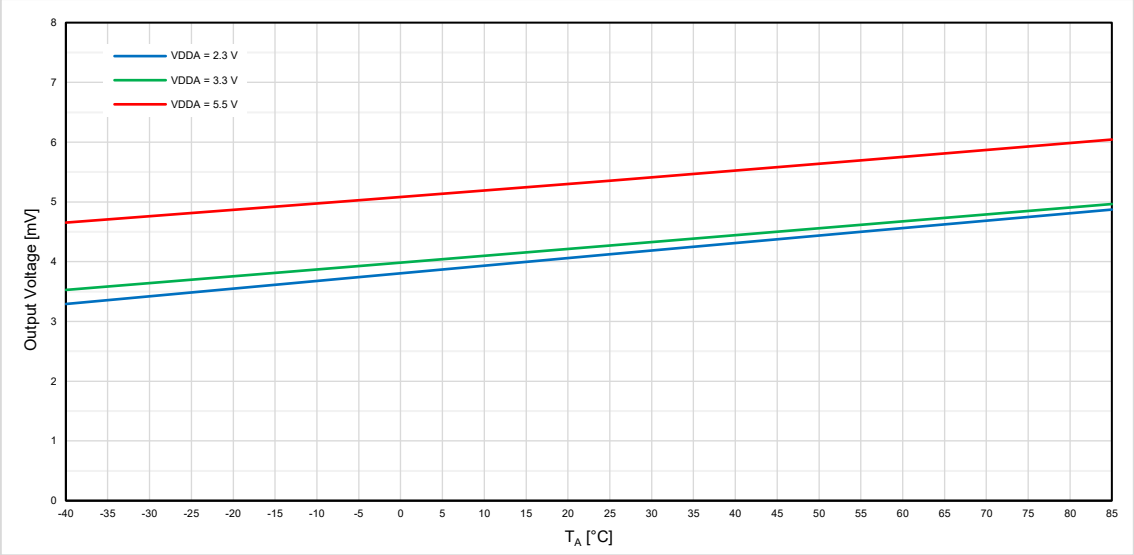


Figure 94. OpAmp Output Voltage High (V_{DDA} - V_{OAx_OUT}) vs. T_A at R_{LOAD} = 50 kΩ

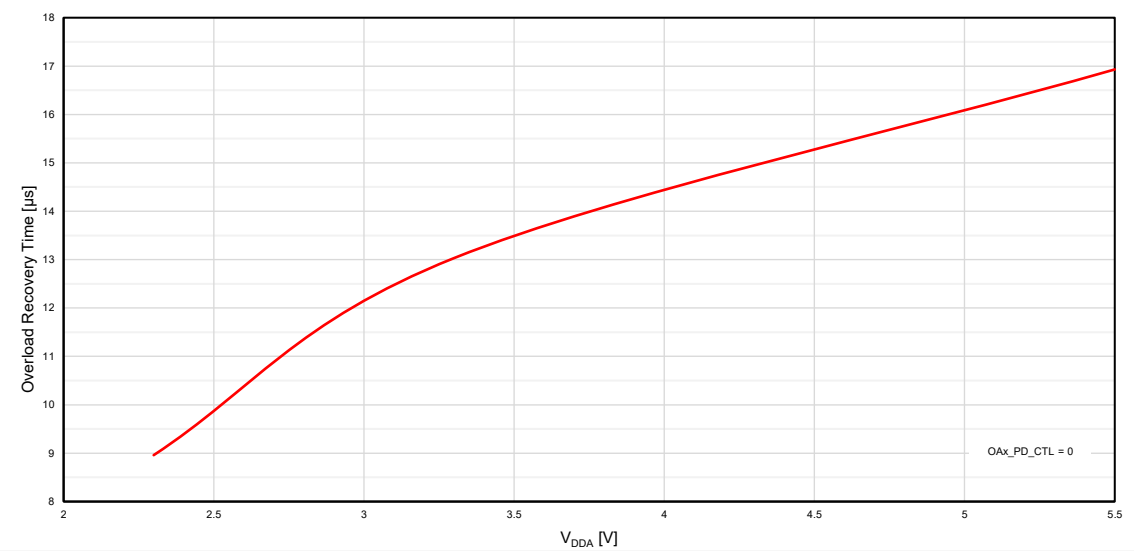


Figure 95. OpAmp Overload Recovery Time vs. V_{DDA} at G = 1, R_{LOAD} = 50 kΩ, Rising

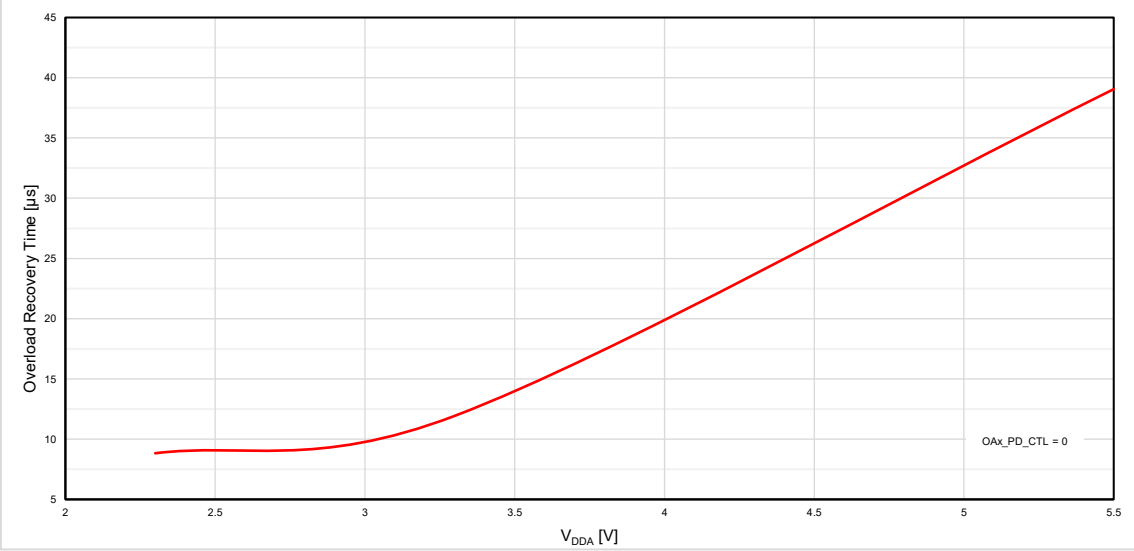


Figure 96. OpAmp Overload Recovery Time vs. V_{DDA} at G = 1, R_{LOAD} = 50 kΩ, Falling

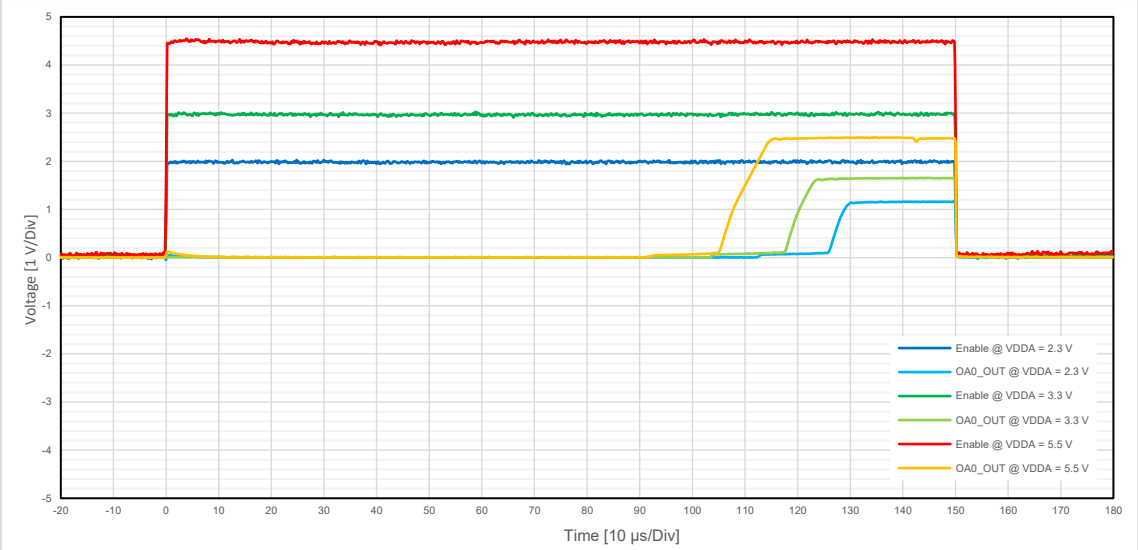


Figure 97. OpAmp Output Response to EN Signal at V_{OAx_IN} = V_{DDA}/2, G = 1, R_{LOAD} = 50 kΩ, C_{LOAD} = 20 pF

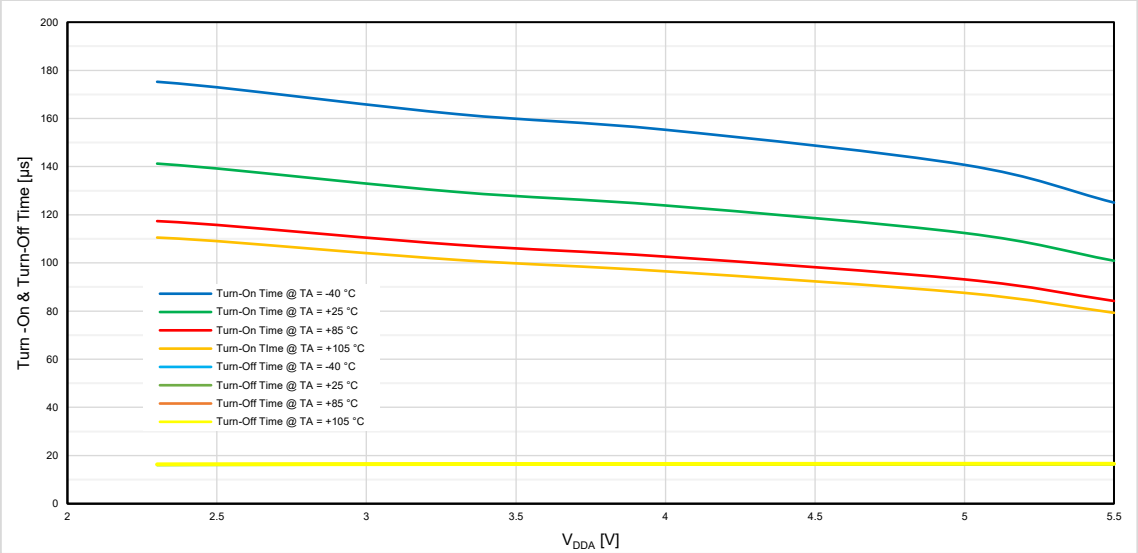


Figure 98. OpAmp Turn-On and Turn-Off Time vs. V_{DDA} at V_{OAx_IN} = V_{DDA}/2

11. Analog Switch

11.1 Analog Switch General Description

The SLG47001-E/03-E contains a single-pole/single-throw (SPST), normally off, analog switch (ASW). The analog switch conducts equally well in both directions when enabled. As shown in Figure 99, the analog switch consists of both n-type and p-type MOSFETs connected in parallel and those two MOSFETs can be driven together or separately depending on the ASW_NMOS_EN bit setting. Note that the NMOS and the PMOS of the analog switch have different resistances ($R_{DS(ON)\_PMOS}$ << $R_{DS(ON)\_NMOS}$).

The analog switch supports two operating modes, and it can be controlled by the following sources:

- **Analog Switch Mode (ASW_MODE = 0)**: The switch is controlled by the connection matrix output [62].
- **OpAmp Switch Control Mode (ASW_MODE = 1)**: The switch is controlled by OpAmp0 output.

In analog switch mode, the PMOS is controlled by the connection matrix output (default setting) and the NMOS can be enabled together with the PMOS when the ASW_NMOS_EN bit is set to '1'. In OpAmp switch control mode, only the PMOS is controlled by the OpAmp0 output.

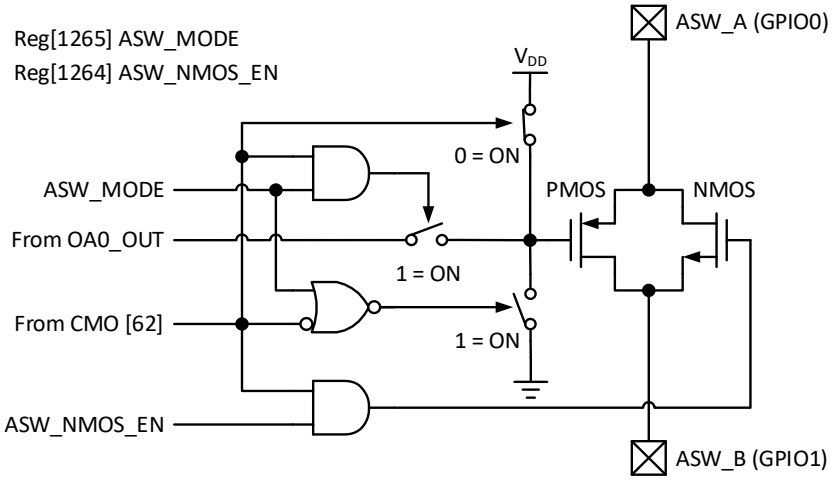


Figure 99. Analog Switch Structure

11.2 Typical Performance of Analog Switch

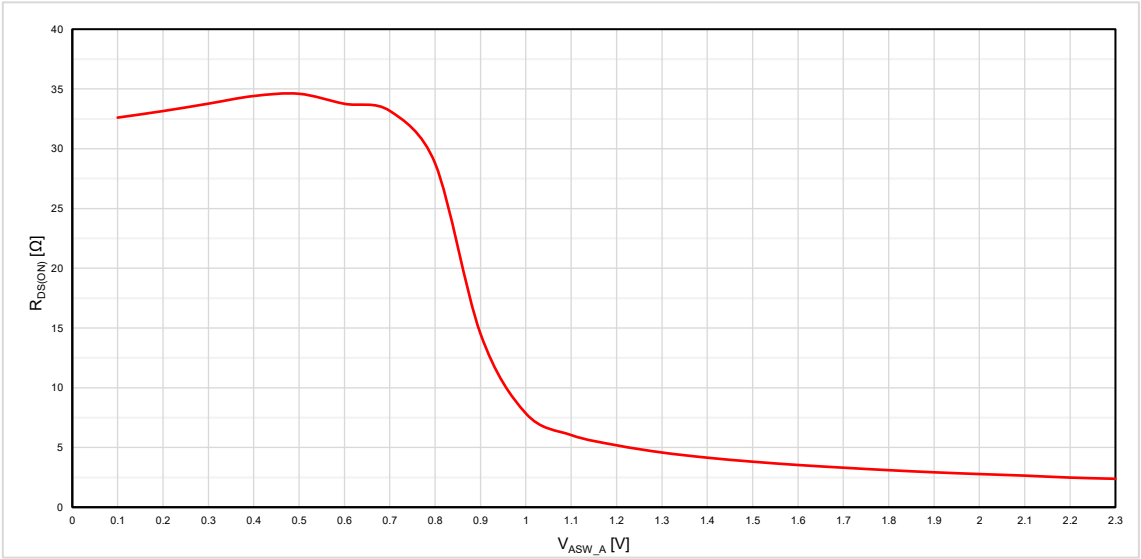


Figure 100. Typical ASW $R_{DS(ON)}$ vs. V_{ASW_A} (0 V to V_{DD}) at V_{DD} = 2.3 V, I_{LOAD} = 1 mA

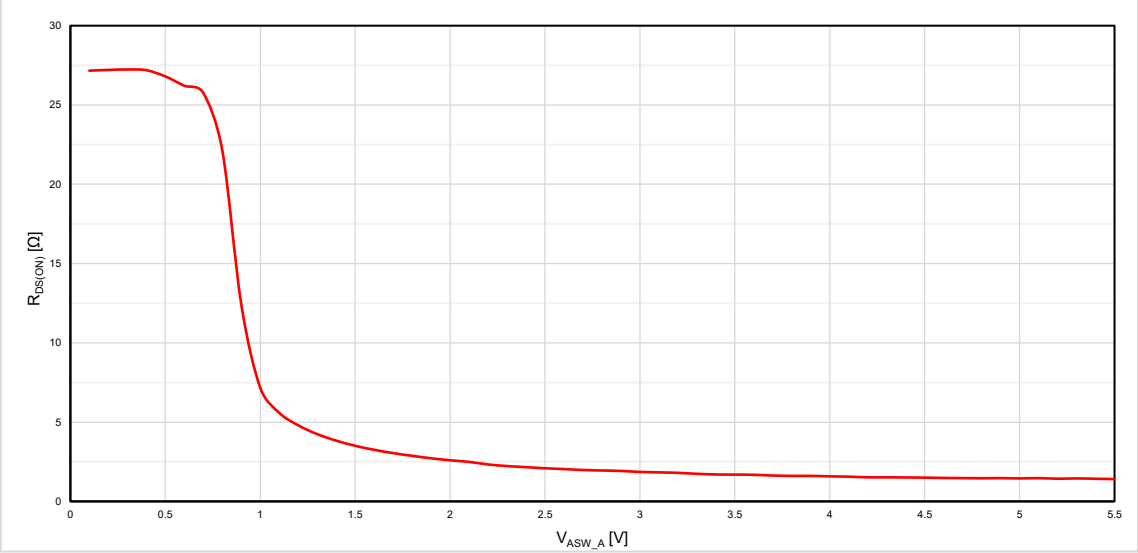


Figure 101. Typical ASW $R_{DS(ON)}$ vs. V_{ASW_A} (0 V to V_{DD}) at V_{DD} = 5.5 V, I_{LOAD} = 1 mA

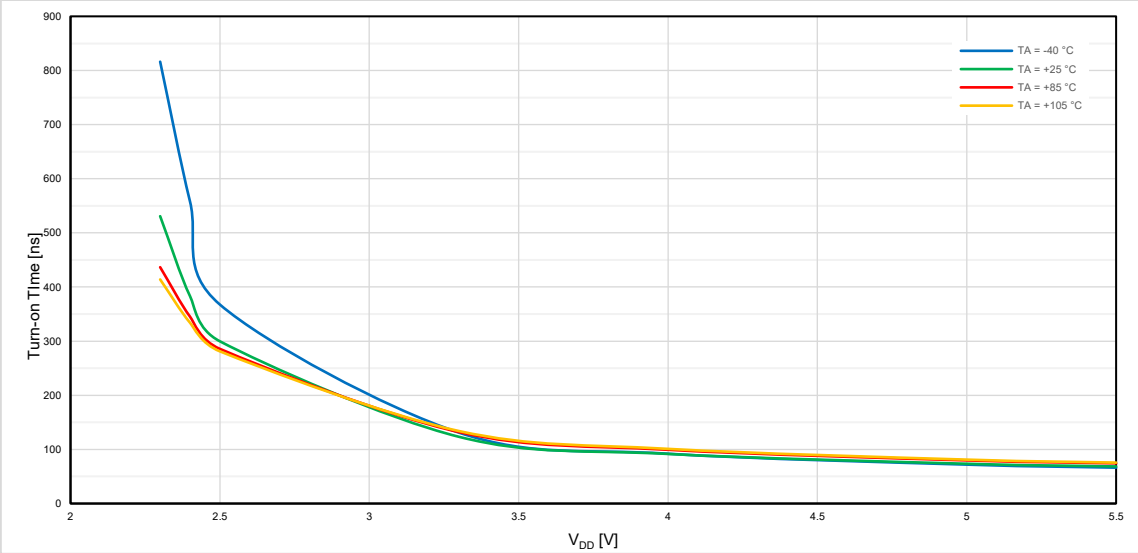


Figure 102. ASW Turn-On Time vs. V_{DD} at V_{ASW_A} = V_{DD}/2, R_{LOAD} = 100 Ω to GND

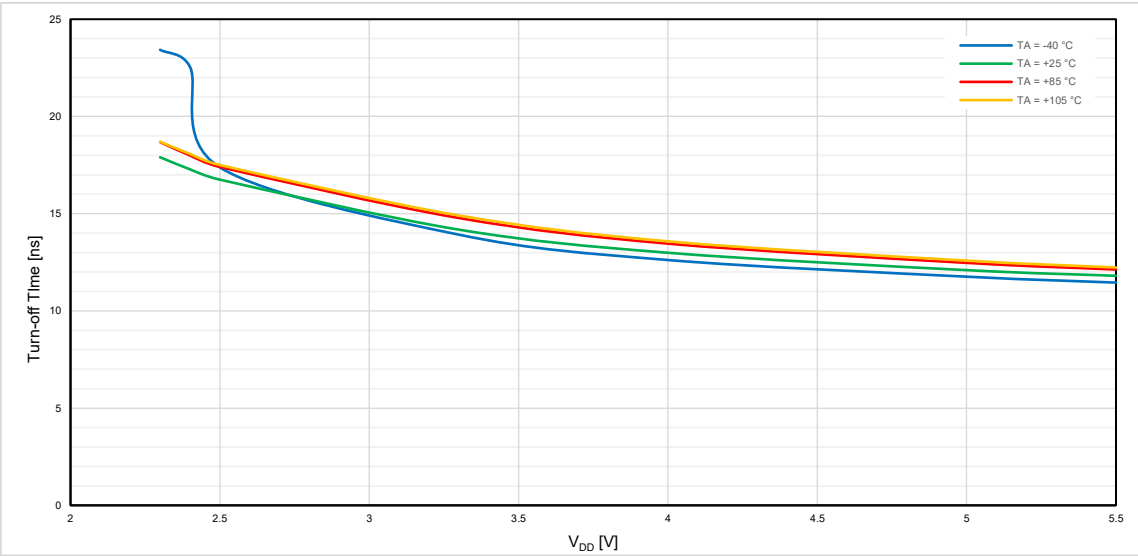


Figure 103. ASW Turn-Off Time vs. V_{DD} at V_{ASW_A} = V_{DD}/2, R_{LOAD} = 100 Ω to GND

12. Multi-Channel Sampling Analog Comparator

12.1 MS-ACMP General Description

The SLG47001-E/03-E has one multi-channel sampling analog comparator (MS-ACMP) that can make periodical samples of up to six input channels and latches the results at the six outputs. The input sources of the MS-ACMP can be GPIO0, GPIO1, GPIO2, GPIO3, OA0_OUT, OA1_OUT, RH1A, RH1B, TS_OUT or V_{DD} (GPIO8 and GPIO9 are also available in STQFN-24 package option). Users can select any number of channels to be sampled from one up to six (for example, Channel0, Channel1, and Channel2).

The channels are sampled in fixed order from Channel0 to Channel5. Each channel has an individual voltage reference with programmable low-to-high and high-to-low thresholds. The V_{REF} range is from 32 mV to 2016 mV with 32 mV steps and each channel has two separate registers (6-bit for the low-to-high V_{REF} threshold and another 6-bit for the high-to-low V_{REF} threshold selection). The non-inverting input of the MS-ACMP has a voltage divider (Gain of 1, 1/2, 1/3, and 1/4) that can configure the gain of each channel individually.

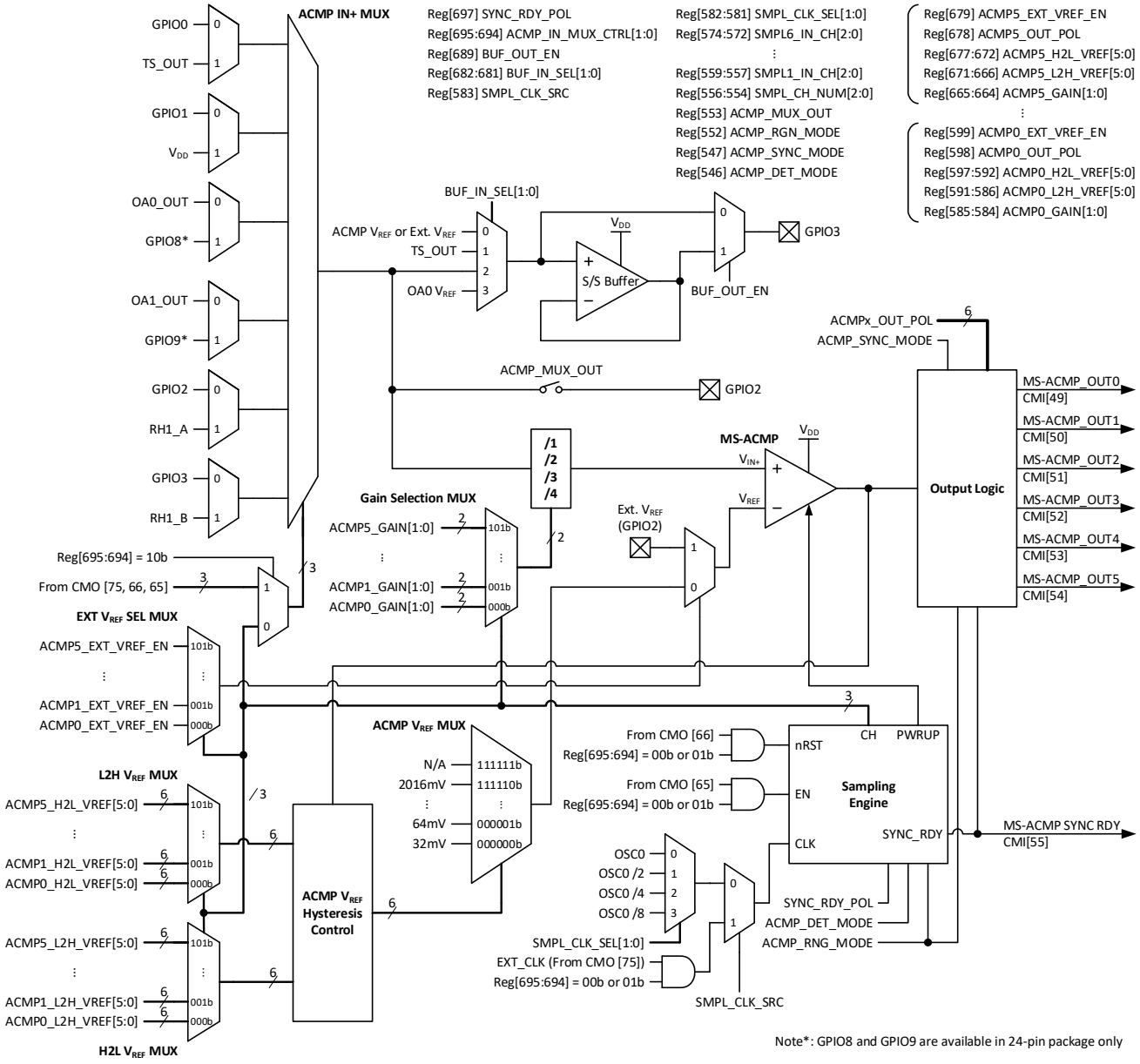


Figure 104. Multi-Channel Analog Comparator Block Diagram

The MS-ACMP uses the internal oscillator (OSC0) or an external clock (max. 10 kHz with 50 % duty cycle) to switch between channels, change V_{REF}, and latch the results. The clock from OSC0 can be divided by 2, 4, or 8 inside the MS-ACMP. If the 'Auto Power-on' setting of OSC0 is selected, a HIGH-level voltage (or a rising edge depending on the setting) on the EN input starts the internal oscillator (OSC0). Table 18 shows the recommended MS-ACMP clock frequencies when interfacing sensors with high output impedance.

Table 18. Recommended MS-ACMP Clock Frequencies

Parameter	Range 1	Range 2	Range 3	Range 4	Range 5	Unit
Sensor Output Resistance	< 1	1 to 2	2 to 4	4 to 6	> 6	MΩ
MS-ACMP Clock Frequency	≤ 10	≤ 5	≤ 2.5	≤ 1.25	≤ 0.5	kHz

The outputs of the MS-ACMP can be configured to be either asynchronous or synchronous. In asynchronous mode (ACMP_SYNC_MODE = 0), the results appear continuously after each channel is sampled. In synchronous mode (ACMP_SYNC_MODE = 1), the results at the output appear simultaneously after the last selected channel is sampled. The SYNC_RDY signal (to CMI [55]) generates a pulse when the sequence of selected channels is sampled.

The basic modes for the MS-ACMP are described below:

- **Range Mode (ACMP_RNG_MODE = 1) with Level-sensitive Detection (ACMP_DET_MODE = 0)**:

  In this mode, one analog input is compared with up to six thresholds (seven ranges) and the result latches every 'n' pulse(s) at the CLK input (where, n = number of channels) while the EN input (from CMO [65]) is high. When the EN signal goes low, the MS-ACMP finishes the sampling sequence and enters power-down mode.

  The SYNC_RDY output operates as 'Range6' output (TH0 < TH1 < TH2 < TH3 < TH4 < TH5). In this mode, the rate of the input signal change at the ACMP non-inverting input must be slow (less than 32 mV during 'Number of Channels' clocks of the MS-ACMP).
- **Range Mode (ACMP_RNG_MODE = 1) with Edge-sensitive Detection (ACMP_DET_MODE = 1)**:

  When a rising edge comes at the EN input, one analog input is compared with up to six thresholds (seven ranges) and the result latches every 'n' pulse(s) at the CLK input (where, n = number of channels). Then, the MS-ACMP enters power-down mode until the next rising edge comes at the EN input.

  The SYNC_RDY output operates as 'Range6' output (TH0 < TH1 < TH2 < TH3 < TH4 < TH5). In this mode, the rate of the input signal change at the ACMP non-inverting input must be slow (less than 32 mV during 'Number of Channels' clocks of the MS-ACMP).
- **Sampling Mode (ACMP_RNG_MODE = 0) with Level-sensitive Detection (ACMP_DET_MODE = 0)**:

  In this mode, the MS-ACMP switches between up to six sampled channels and latches the result every pulse at the CLK input while the EN input is high. When the EN signal goes low, the MS-ACMP finishes the sampling sequence and enters power-down mode.
- **Sampling Mode (ACMP_RNG_MODE = 0) with Edge-sensitive Detection (ACMP_DET_MODE = 1)**:

  When a rising edge comes at the EN input, the MS-ACMP samples up to six selected channels every rising edge at the CLK input and then enters power-down mode until the next rising edge comes at the EN input.

Table 19. MS-ACMP Configuration Registers

Register Name	Access Type	Register Bit Description
ACMP_DET_MODE	RW	MS-ACMP Signal Detection Mode Selection 0: Level-sensitive Mode 1: Edge-sensitive Mode
ACMP_SYNC_MODE	RW	MS-ACMP Output Synchronization Mode Selection 0: Asynchronous MS-ACMP Output 1: Synchronous MS-ACMP Output
ACMP_RNG_MODE	RW	MS-ACMP Range Mode Selection 0: Sampling Mode 1: Range Mode
ACMP_MUX_OUT	RW	MS-ACMP Analog MUX Unbuffered Output Control 0: Disable 1: Enable (Connected to GPIO2)
SMPL_CH_NUM[2:0]	RW	Number of Sampling Channels 000b: 1 Channel 001b: 2 Channels 010b: 3 Channels 011b: 4 Channels 100b: 5 Channels 101b: 6 Channels 110b - 111b: N/A
SMPL1_IN_CH[2:0]	RW	MS-ACMP Analog MUX Input Selection for 1st Sampling 000b: GPIO0 or TS_OUT determined by Reg[548] 001b: GPIO1 or V_{DD} determined by Reg[549] 010b: OA0_OUT or GPIO8 determined by Reg[699] 011b: OA1_OUT or GPIO9 determined by Reg[670] 100b: GPIO2 or RH1_A determined by Reg[550] 101b: GPIO3 or RH1_B determined by Reg[551]
SMPL2_IN_CH[2:0]	RW	MS-ACMP Analog MUX Input Selection for 2nd Sampling 000b: GPIO0 or TS_OUT determined by Reg[548] 001b: GPIO1 or V_{DD} determined by Reg[549] 010b: OA0_OUT or GPIO8 determined by Reg[699] 011b: OA1_OUT or GPIO9 determined by Reg[670] 100b: GPIO2 or RH1_A determined by Reg[550] 101b: GPIO3 or RH1_B determined by Reg[551]
SMPL3_IN_CH[2:0]	RW	MS-ACMP Analog MUX Input Selection for 3rd Sampling 000b: GPIO0 or TS_OUT determined by Reg[548] 001b: GPIO1 or V_{DD} determined by Reg[549] 010b: OA0_OUT or GPIO8 determined by Reg[699] 011b: OA1_OUT or GPIO9 determined by Reg[670] 100b: GPIO2 or RH1_A determined by Reg[550] 101b: GPIO3 or RH1_B determined by Reg[551]
SMPL4_IN_CH[2:0]	RW	MS-ACMP Analog MUX Input Selection for 4th Sampling 000b: GPIO0 or TS_OUT determined by Reg[548] 001b: GPIO1 or V^{DD} determined by Reg[549] 010b: OA0_OUT or GPIO8 determined by Reg[699] 011b: OA1_OUT or GPIO9 determined by Reg[670] 100b: GPIO2 or RH1_A determined by Reg[550] 101b: GPIO3 or RH1_B determined by Reg[551]

Register Name	Access Type	Register Bit Description
SMPL5_IN_CH[2:0]	RW	MS-ACMP Analog MUX Input Selection for 5th Sampling 000b: GPIO0 or TS_OUT determined by Reg[548] 001b: GPIO1 or V_{DD} determined by Reg[549] 010b: OA0_OUT or GPIO8 determined by Reg[699] 011b: OA1_OUT or GPIO9 determined by Reg[670] 100b: GPIO2 or RH1_A determined by Reg[550] 101b: GPIO3 or RH1_B determined by Reg[551]
SMPL6_IN_CH[2:0]	RW	MS-ACMP Analog MUX Input Selection for 6th Sampling 000b: GPIO0 or TS_OUT determined by Reg[548] 001b: GPIO1 or V_{DD} determined by Reg[549] 010b: OA0_OUT or GPIO8 determined by Reg[699] 011b: OA1_OUT or GPIO9 determined by Reg[670] 100b: GPIO2 or RH1_A determined by Reg[550] 101b: GPIO3 or RH1_B determined by Reg[551]
SMPL_CLK_SEL[1:0]	RW	Sampling Clock Selection 00b: CLK 01b: CLK /2 10b: CLK /4 11b: CLK /8
SMPL_CLK_SRC	RW	Sampling Clock Source Selection 0: OSC0 (LFOSC) 1: External CLK from Connection Matrix Output [75]
SYNC_RDY_POL	RW	SYNC_RDY Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP0_GAIN[1:0]	RW	ACMP0 Gain Divider Selection 00b: 1x 01b: 0.5x 10b: 0.33x 11b: 0.25x
ACMP0_L2H_VREF[5:0]	RW	ACMP0 Low-to-High V_{REF} Voltage Selection (See Table 20 for details)
ACMP0_H2L_VREF[5:0]	RW	ACMP0 High-to-Low V_{REF} Voltage Selection (See Table 20 for details)
ACMP0_OUT_POL	RW	ACMP0 Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP0_EXT_VREF_EN	RW	ACMP0 External V_{REF} Enable Control 0: Disable 1: Enable
ACMP1_GAIN[1:0]	RW	ACMP1 Gain Divider Selection 00b: 1x 01b: 0.5x 10b: 0.33x 11b: 0.25x
ACMP1_L2H_VREF[5:0]	RW	ACMP1 Low-to-High V_{REF} Voltage Selection (See Table 20 for details)

Register Name	Access Type	Register Bit Description
ACMP1_H2L_VREF[5:0]	RW	ACMP1 High-to-Low V_{REF} Voltage Selection (See Table 20 for details)
ACMP1_OUT_POL	RW	ACMP1 Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP1_EXT_VREF_EN	RW	ACMP1 External V_{REF} Enable Control 0: Disable 1: Enable
ACMP2_GAIN[1:0]	RW	ACMP2 Gain Divider Selection 00b: 1x 01b: 0.5x 10b: 0.33x 11b: 0.25x
ACMP2_L2H_VREF[5:0]	RW	ACMP2 Low-to-High V_{REF} Voltage Selection (See Table 20 for details)
ACMP2_H2L_VREF[5:0]	RW	ACMP2 High-to-Low V_{REF} Voltage Selection (See Table 20 for details)
ACMP2_OUT_POL	RW	ACMP2 Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP2_EXT_VREF_EN	RW	ACMP2 External V_{REF} Enable Control 0: Disable 1: Enable
ACMP3_GAIN[1:0]	RW	ACMP3 Gain Divider Selection 00b: 1x 01b: 0.5x 10b: 0.33x 11b: 0.25x
ACMP3_L2H_VREF[5:0]	RW	ACMP3 Low-to-High V_{REF} Voltage Selection (See Table 20 for details)
ACMP3_H2L_VREF[5:0]	RW	ACMP3 High-to-Low V_{REF} Voltage Selection (See Table 20 for details)
ACMP3_OUT_POL	RW	ACMP3 Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP3_EXT_VREF_EN	RW	ACMP3 External V_{REF} Enable Control 0: Disable 1: Enable
ACMP4_GAIN[1:0]	RW	ACMP4 Gain Divider Selection 00b: 1x 01b: 0.5x 10b: 0.33x 11b: 0.25x
ACMP4_L2H_VREF[5:0]	RW	ACMP4 Low-to-High V_{REF} Voltage Selection (See Table 20 for details)

Register Name	Access Type	Register Bit Description
ACMP4_H2L_VREF[5:0]	RW	ACMP4 High-to-Low V_{REF} Voltage Selection (See Table 20 for details)
ACMP4_OUT_POL	RW	ACMP4 Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP4_EXT_VREF_EN	RW	ACMP4 External V_{REF} Enable Control 0: Disable 1: Enable
ACMP5_GAIN[1:0]	RW	ACMP5 Gain Divider Selection 00b: 1x 01b: 0.5x 10b: 0.33x 11b: 0.25x
ACMP5_L2H_VREF[5:0]	RW	ACMP5 Low-to-High V_{REF} Voltage Selection (See Table 20 for details)
ACMP5_H2L_VREF[5:0]	RW	ACMP5 High-to-Low V_{REF} Voltage Selection (See Table 20 for details)
ACMP5_OUT_POL	RW	ACMP5 Output Polarity Selection 0: Non-inverted 1: Inverted
ACMP5_EXT_VREF_EN	RW	ACMP5 External V_{REF} Enable Control 0: Disable 1: Enable
ACMP_IN_MUX_CTRL[1:0]	RW	MS-ACMP Input MUX Control Setting 00b: MUX is controlled by the sampling engine (ACMP enabled) 01b: MUX is controlled by the sampling engine (ACMP disabled) 10b: MUX is controlled by the connection matrix output [75], [66], and [65] (ACMP and sampling engine disabled) CMO[75,66,65] = 000b: Select MUX CH0 CMO[75,66,65] = 001b: Select MUX CH1 CMO[75,66,65] = 010b: Select MUX CH2 CMO[75,66,65] = 011b: Select MUX CH3 CMO[75,66,65] = 100b: Select MUX CH4 CMO[75,66,65] = 101b: Select MUX CH5 CMO[75,66,65] = 110b – 111b: N/A 11b: N/A

Table 20. MS-ACMP Low-to-High and High-to-Low V_{REF} Voltage Selection Table

ACMPx_L2H_VREF[5:0] ACMPx_H2L_VREF[5:0]	V_{REF} [V]	ACMPx_L2H_VREF[5:0] ACMPx_H2L_VREF[5:0]	V_{REF} [V]
0 (000000b)	0.032	32 (100000b)	1.056
1 (000001b)	0.064	33 (100001b)	1.088
2 (000010b)	0.096	34 (100010b)	1.120

ACMPx_L2H_VREF[5:0] ACMPx_H2L_VREF[5:0]	V_{REF} [V]	ACMPx_L2H_VREF[5:0] ACMPx_H2L_VREF[5:0]	V_{REF} [V]
3 (000011b)	0.128	35 (100011b)	1.152
4 (000100b)	0.160	36 (100100b)	1.184
5 (000101b)	0.192	37 (100101b)	1.216
6 (000110b)	0.224	38 (100110b)	1.248
7 (000111b)	0.256	39 (100111b)	1.280
8 (001000b)	0.288	40 (101000b)	1.312
9 (001001b)	0.320	41 (101001b)	1.344
10 (001010b)	0.352	42 (101010b)	1.376
11 (001011b)	0.384	43 (101011b)	1.408
12 (001100b)	0.416	44 (101100b)	1.440
13 (001101b)	0.448	45 (101101b)	1.472
14 (001110b)	0.480	46 (101110b)	1.504
15 (001111b)	0.512	47 (101111b)	1.536
16 (010000b)	0.544	48 (110000b)	1.568
17 (010001b)	0.576	49 (110001b)	1.600
18 (010010b)	0.608	50 (110010b)	1.632
19 (010011b)	0.640	51 (110011b)	1.664
20 (010100b)	0.672	52 (110100b)	1.696
21 (010101b)	0.704	53 (110101b)	1.728
22 (010110b)	0.736	54 (110110b)	1.760
23 (010111b)	0.768	55 (110111b)	1.792
24 (011000b)	0.800	56 (111000b)	1.824
25 (011001b)	0.832	57 (111001b)	1.856
26 (011010b)	0.864	58 (111010b)	1.888
27 (011011b)	0.896	59 (111011b)	1.920
28 (011100b)	0.928	60 (111100b)	1.952
29 (011101b)	0.960	61 (111101b)	1.984
30 (011110b)	0.992	62 (111110b)	2.016
31 (011111b)	1.024	63 (111111b)	N/A

12.2 MS-ACMP Input Analog MUX

The MS-ACMP has a 6-to-1 analog multiplexer at its positive input and six 2-to-1 multiplexers are connected to six inputs of the 6-to-1 analog MUX. These multiplexers allow users to configure the positive input of the MS-ACMP from various sources such as GPIO0, GPIO1, GPIO2, GPIO3, OA0_OUT, OA1_OUT, RH1A, RH1B, TS_OUT or V_{DD}. Note that GPIO8 and GPIO9 are also available in STQFN-24 package option. The 6-to-1 MUX can be controlled by either the MS-ACMP sampling engine or the connection matrix (CMO [75, 66, 65]), determined by the ACMP_IN_MUX_CTRL[1:0] register (Reg[695:694]). When the analog MUX channels are switched by the external clock manually, the MS-ACMP can be turned off by setting ACMP_IN_MUX_CTRL[1:0] = 10b.

The output of the MS-ACMP input analog MUX can also be routed to GPIOs with or without a buffer. The analog MUX output is connected to the input MUX for the sink/source buffer output (GPIO3). When the ACMP_MUX_OUT bit (Reg[553]) is set to '1', the analog MUX output is connected to GPIO2 directly (unbuffered).

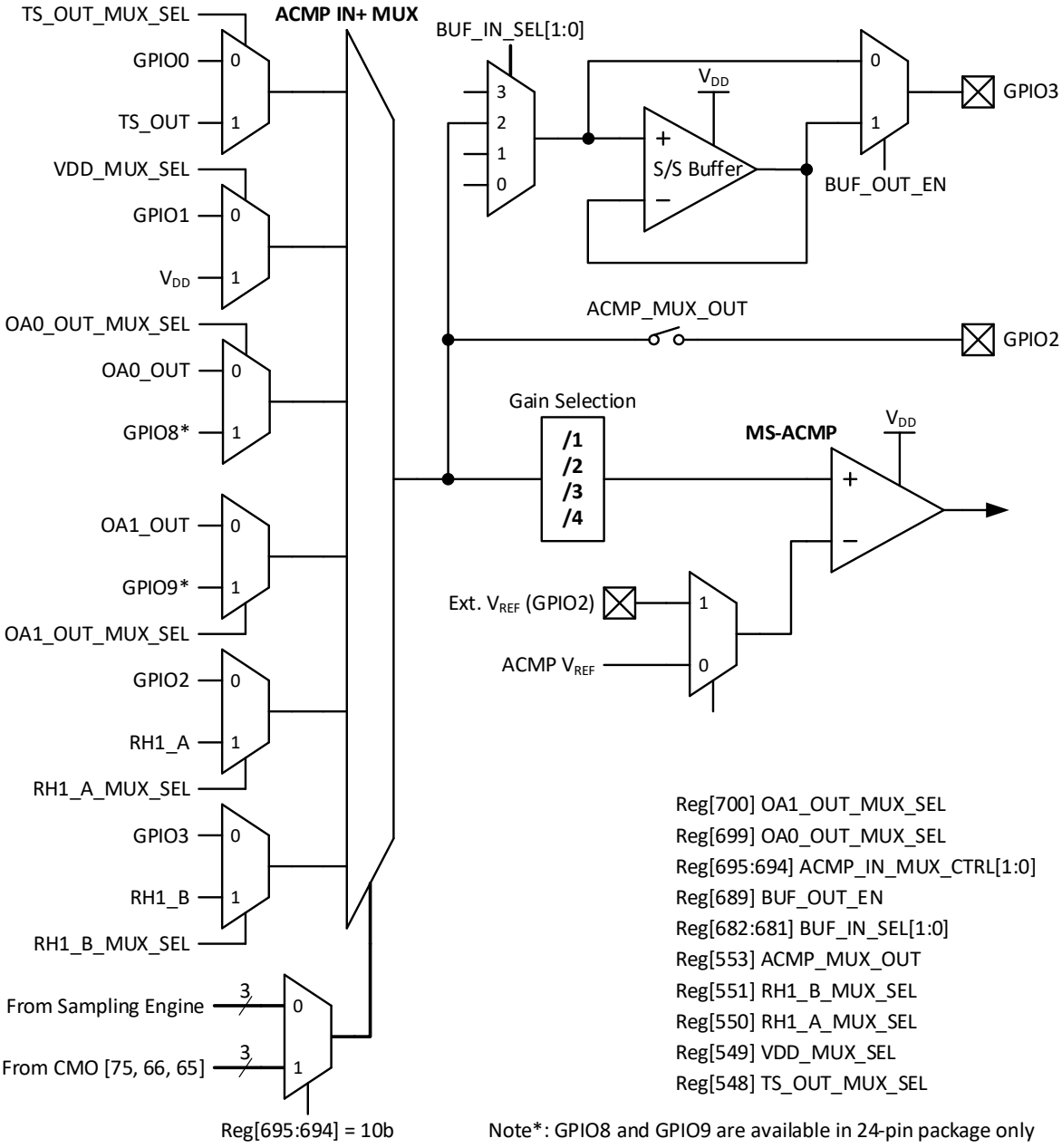


Figure 105. MS-ACMP Analog MUX Block Diagram

Table 21. MS-ACMP Input Analog MUX Configuration Registers

Register Name	Access Type	Register Bit Description
TS_OUT_MUX_SEL	RW	MS-ACMP Analog MUX TS_OUT Input Selection 0: GPIO0 1: TS_OUT
VDD_MUX_SEL	RW	MS-ACMP Analog MUX VDD Input Selection 0: GPIO1 1: V_{DD}
RH1_A_MUX_SEL	RW	MS-ACMP Analog MUX RH1_A Input Selection 0: GPIO2 1: RH1_A
RH1_B_MUX_SEL	RW	MS-ACMP Analog MUX RH1_B Input Selection 0: GPIO3 1: RH1_B
ACMP_MUX_OUT	RW	MS-ACMP Analog MUX Unbuffered Output Control 0: Disable 1: Enable (Connected to GPIO2)
ACMP_IN_MUX_CTRL[1:0]	RW	MS-ACMP Input MUX Control Setting 00b: MUX is controlled by the sampling engine (ACMP enabled) 01b: MUX is controlled by the sampling engine (ACMP disabled) 10b: MUX is controlled by the connection matrix output [75], [66], and [65] (ACMP and sampling engine disabled) CMO[75,66,65] = 000b: Select MUX CH0 CMO[75,66,65] = 001b: Select MUX CH1 CMO[75,66,65] = 010b: Select MUX CH2 CMO[75,66,65] = 011b: Select MUX CH3 CMO[75,66,65] = 100b: Select MUX CH4 CMO[75,66,65] = 101b: Select MUX CH5 CMO[75,66,65] = 110b – 111b: N/A 11b: N/A
OA0_OUT_MUX_SEL	RW	MS-ACMP Analog MUX OA0_OUT Input Selection 0: OA0 1: GPIO8
OA1_OUT_MUX_SEL	RW	MS-ACMP Analog MUX OA1_OUT Input Selection 0: OA1 1: GPIO9

12.3 MS-ACMP Timing Diagrams

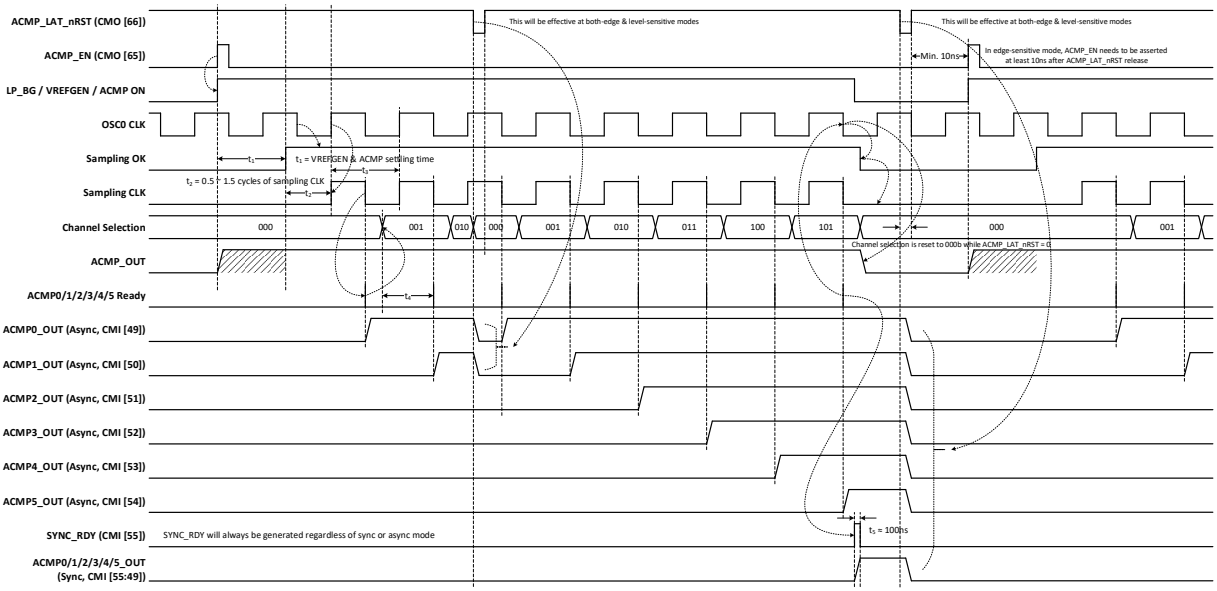


Figure 106. MS-ACMP Timing Diagram (Sampling, Edge-Sensitive, OSC0 and BG: Forced-ON)

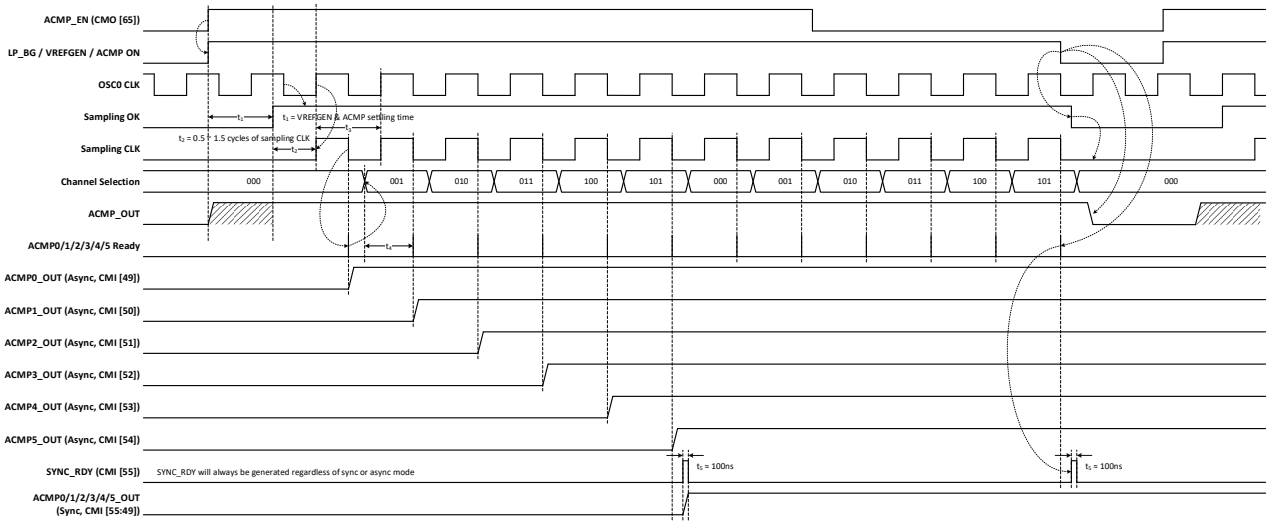


Figure 107. MS-ACMP Timing Diagram (Sampling, Level-Sensitive, OSC0 and BG: Forced-ON)

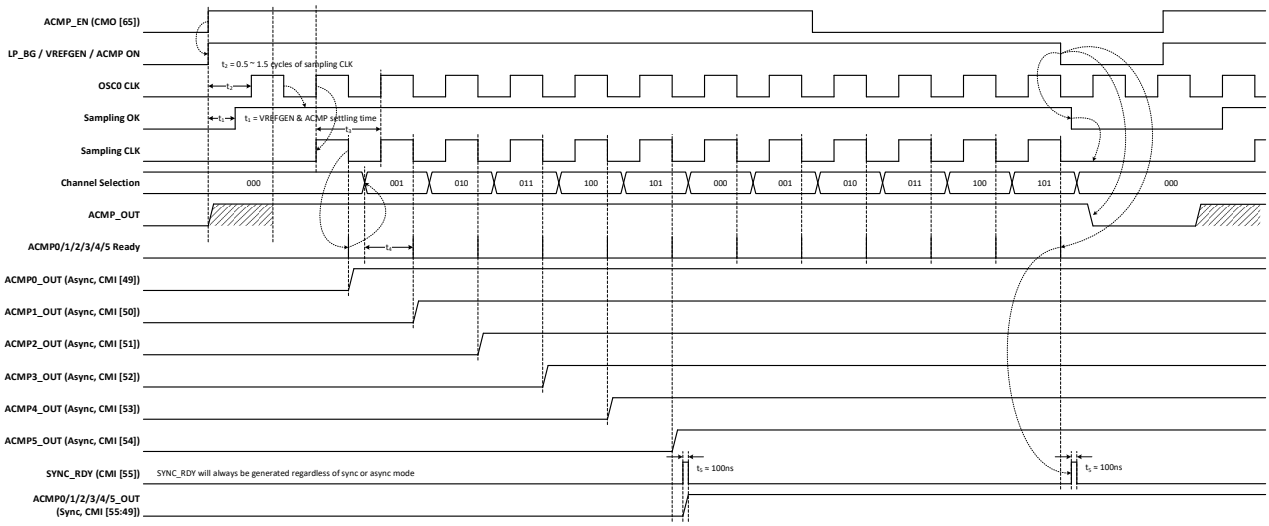


Figure 108. MS-ACMP Timing Diagram (Sampling, Level-Sensitive, OSC0: Auto-ON, BG: Forced-ON)

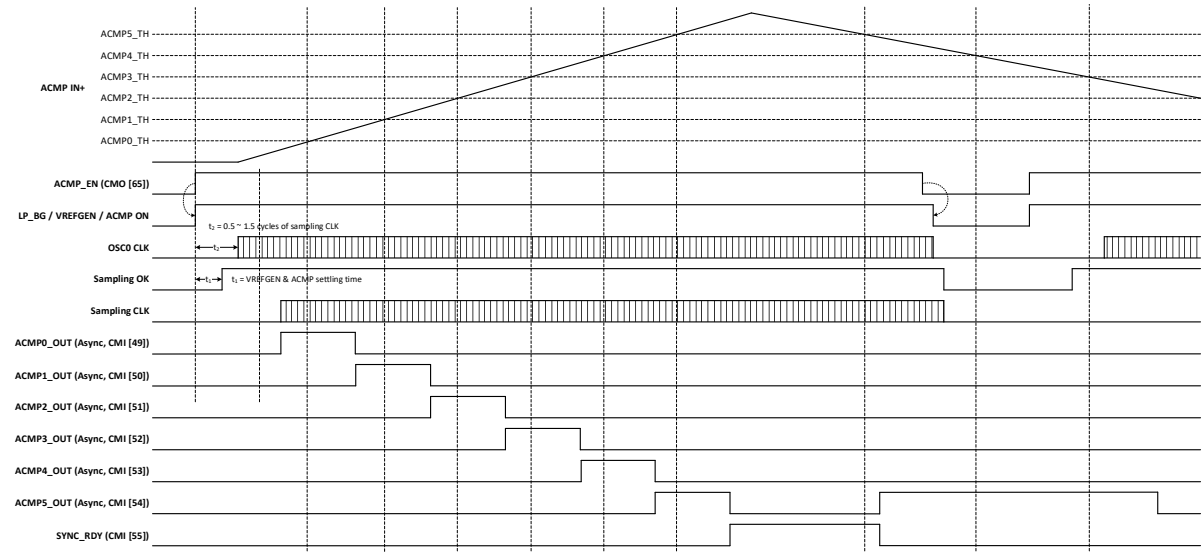


Figure 109. MS-ACMP Timing Diagram (Range, Level-Sensitive, OSC0: Auto-ON, BG: Forced-ON)

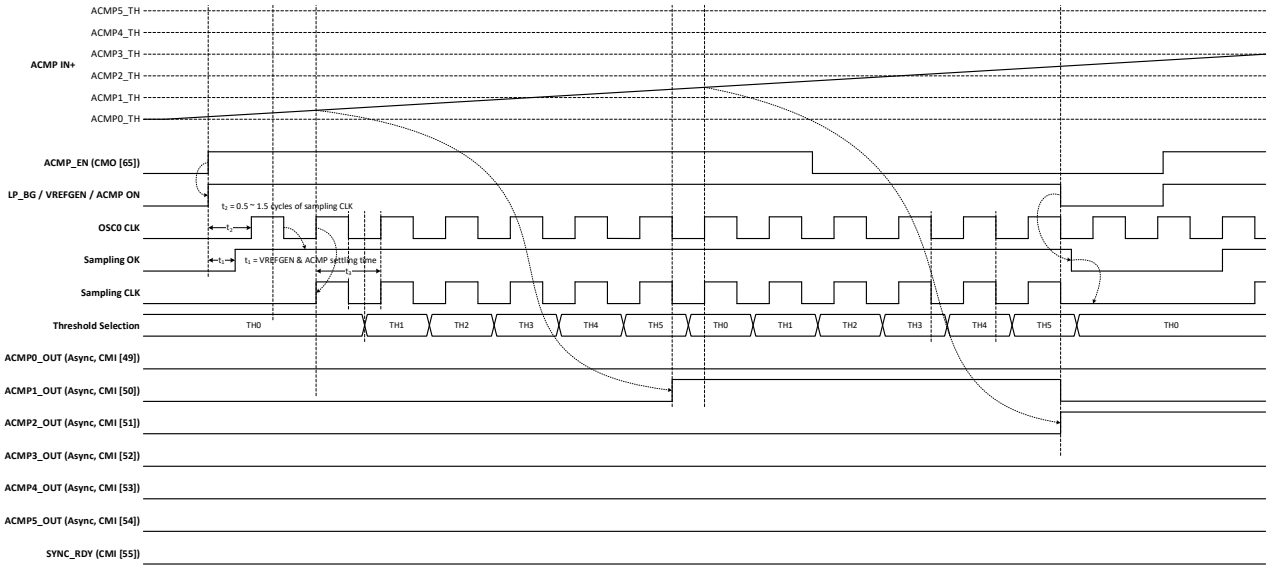


Figure 110. MS-ACMP Timing Diagram (Range, Level-Sensitive, OSC0: Auto-ON, BG: Forced-ON, Zoomed)

12.4 Typical Performance of MS-ACMP

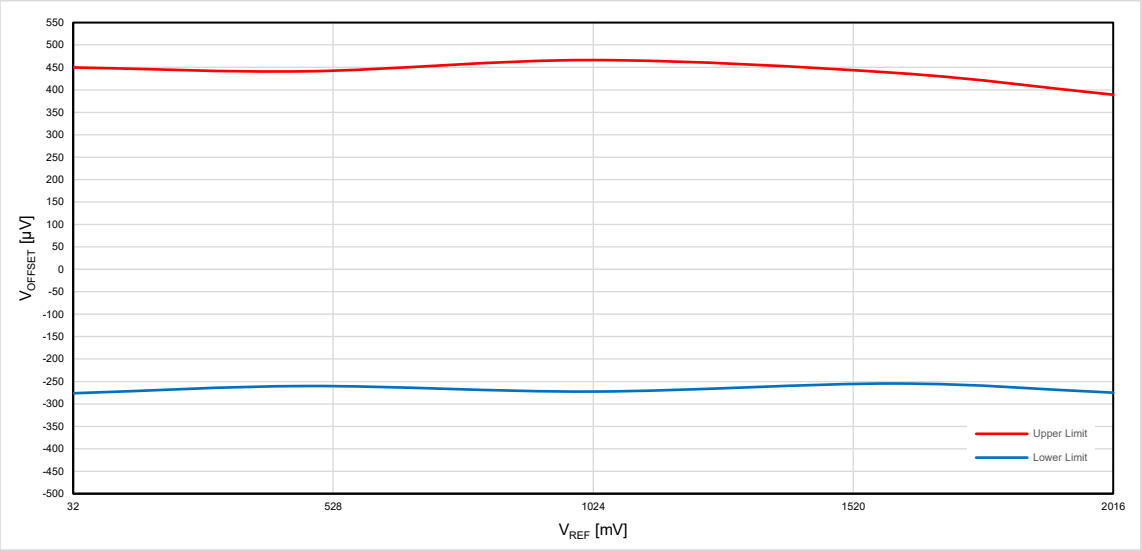


Figure 111. MS-ACMP Input Offset Voltage vs. V_{REF} at V_{DD} = 2.3 V to 5.5 V, Gain = 1, T_A = -40 °C to +105 °C

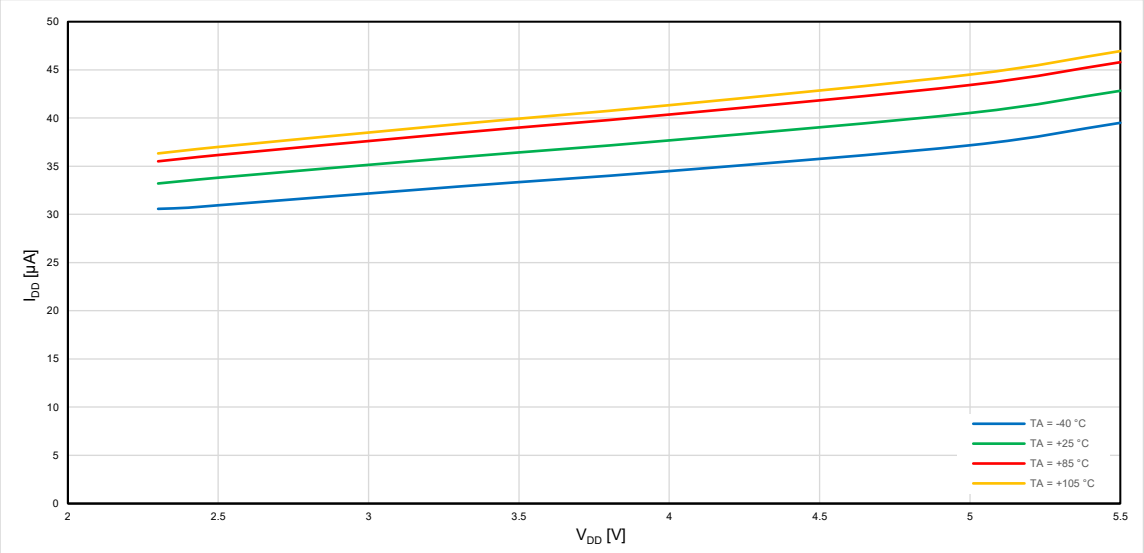


Figure 112. MS-ACMP Current Consumption vs. V_{DD} at f_{CLK} = 10 kHz

13. Analog Temperature Sensor

The SLG47001-E/03-E has an analog temperature sensor with an output voltage linearly proportional to the die temperature in Celsius (°C). The temperature sensor has a dynamic range of -40 °C to +130 °C. The accuracies of the temperature sensor output (TS_OUT) measured at GPIO3 bypassing the Sink/Source buffer (BUF_OUT_EN = 0) and the calculated junction temperature over V_{DD} are shown in section 3.4.15 Analog Temperature Sensor Specifications.

The TS_OUT can be selected as an input to the input MUX of the MS-ACMP. The equation below calculates the typical analog voltage (V_{TS_OUT}) fed to the input MUX of the MS-ACMP. Note that there will be about ±2 °C of unit-to-unit variation.

$$V_{TS\_OUT} = -4.8 \times T_J + 1825.2$$

where, V_{TS_OUT}: TS_OUT voltage in mV

T_J: Junction temperature in °C.

The hysteresis of the TS_OUT signal can be configured by enabling the hysteresis of the MS-ACMP.

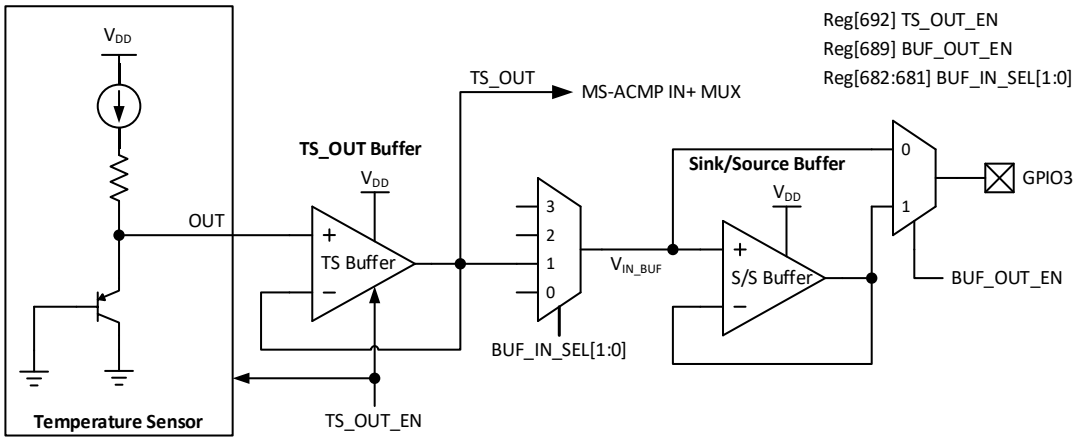


Figure 113. Analog Temperature Sensor Structure

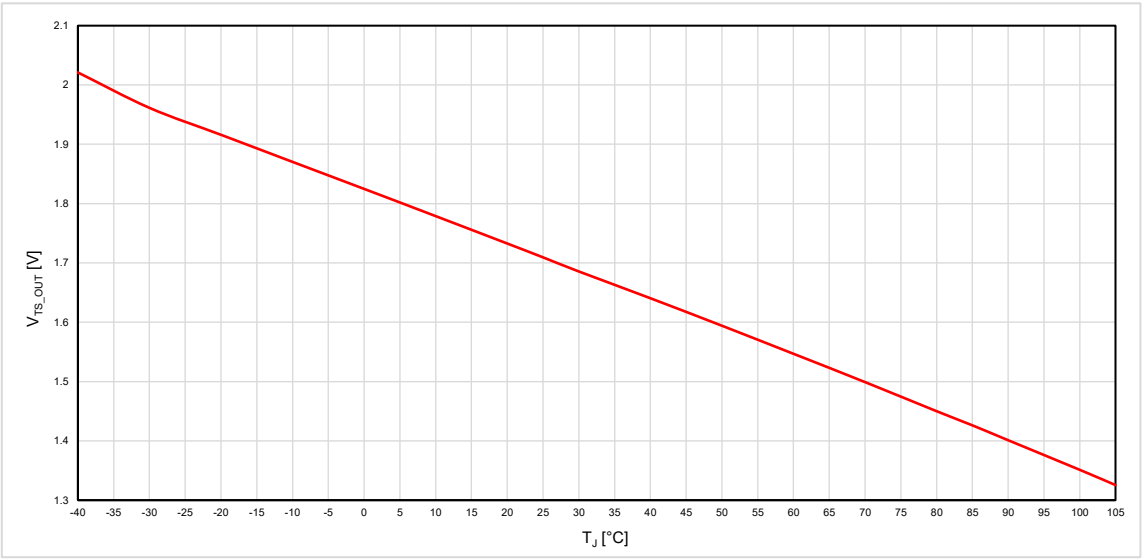


Figure 114. Junction Temperature vs. V_{TS_OUT} at V_{DD} = 2.3 V to 5.5 V

14. 100 kΩ Digital Rheostats

14.1 Digital Rheostats General Description

The SLG47001-E/03-E contains two 10-bit digital rheostats and the simplified structure of the digital rheostat macrocell is shown in Figure 115. The 10-bit counter value (1024 taps) corresponds to the rheostat resistance value between the RHx_A and the RHx_B terminals (‘Code 0’ and ‘Code 1023’ represents the minimum and the maximum rheostat resistance respectively). When the counter value increases, the resistance between the RHx_A and the RHx_B terminals monotonically increases. On the contrary, the resistance decreases when the counter value decreases. The voltage on any rheostat pins can be in the range from 0 V to V_{DDA}, and it can be changed dynamically during operation.

The initial values of the two rheostats can be programmed into the NVM (OTP). During the power-on event, the initial values stored in the NVM are loaded to the RH0_SET[9:0] and the RH1_SET[9:0] registers and those initial values are loaded to the rheostat counters as well. This value is used as the initial rheostat resistance as well as the starting point for count-down or count-up. The current rheostat counter values can be monitored by reading the RH0_READ[9:0] and the RH1_READ[9:0] registers. Before the digital rheostats are initialized during the power-on sequence, the rheostat resistance is Hi-Z (or highest resistance if it is not possible to disconnect the rheostats from the terminals).

During normal operations, the rheostat resistance can be changed on-the-fly in three ways:

- Changing the rheostat counter values by updating the RHx_SET[9:0] registers through I²C interface.
- Increasing/decreasing the rheostat counter values using the RHx_CLK and the UP/DOWNx signals.
- When the rheostats are driven by the EPG (in rheostat mode), the EPG data will be loaded onto the rheostat counters at the rising edge of the RELOADx signal.

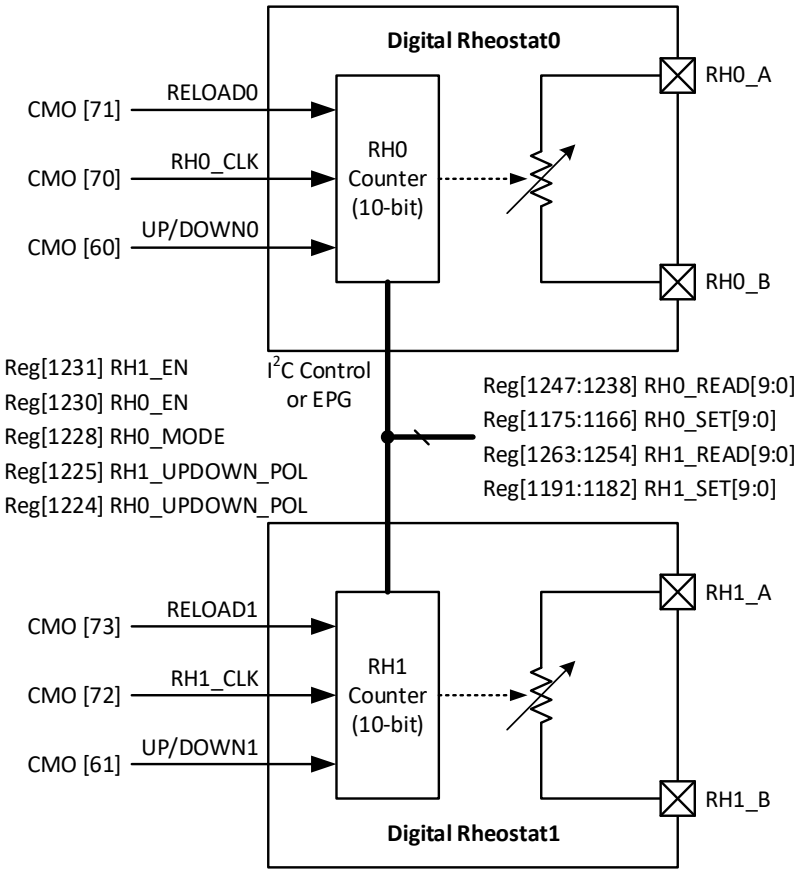


Figure 115. Simplified Digital Rheostat Structure

The digital rheostat can be clocked up to 25 MHz. However, in case precision transactions between the rheostat resistance change are required, a clock frequency less than 100 kHz should be applied. Also, the load capacitance on the rheostat terminals affects the settling time of the terminal voltages. Hence, a proper clock frequency needs to be used for different operating conditions.

Digital Rheostat Macrocell Signals:

- **UP/DOWNx**: The rheostat counter increases by one LSB at the rising edge of RHx_CLK when UP/DOWNx signal is high. When this signal is low, the counter value decreases by one LSB at the rising edge of RHx_CLK.
- **RHx_CLK**: The clock signal to the rheostat counter. The clock signal comes from the connection matrix output.
- **RELOADx**: At the rising edge of the RELOADx signal, the initial rheostat values stored in the NVM (OTP) will be loaded into the corresponding register (RHx_SET[9:0]) and the counter overwriting the existing settings. (Note that the RELOADx signal is used to load the EPG data onto the rheostat counters when the corresponding rheostats are driven by the EPG.)

There is an overflow protection feature that stops counting the rheostat counter from counting up when it hits the maximum value (0x3FF), and stops it from counting down when the minimum value (0x00) is reached. In case the counter values of RH0 and RH1 reach either 0x3FF or 0x00, the CMI [59] and the CMI [60] signals will go high respectively as an overflow flag.

Table 22. Digital Rheostat Configuration Registers

Register Name	Access Type	Register Bit Description
RH0_SET[9:0]	RW	Digital Rheostat0 Value Setting 00 0000 0000b: R_{RH_MIN} ~ 11 1111 1111b: R_{RH}
RH1_SET[9:0]	RW	Digital Rheostat1 Value Setting 00 0000 0000b: R_{RH_MIN} ~ 11 1111 1111b: R_{RH}
RH0_TOL_DATA[14:0]	RW	Digital Rheostat0 Tolerance Data Decimal value of 15-bit data represents the error from 100 kΩ at T_A = +25 °C
RH0_TOL_SIGN	RW	Digital Rheostat0 Sign of Tolerance Data 0: Positive 1: Negative
RH1_TOL_DATA[14:0]	RW	Digital Rheostat1 Tolerance Data Decimal value of 15-bit data represents the error from 100 kΩ at T_A = +25 °C
RH1_TOL_SIGN	RW	Digital Rheostat1 Sign of Tolerance Data 0: Positive 1: Negative
RH0_UPDOWN_POL	RW	Digital Rheostat0 UP/DOWN Polarity Selection 0: Default (UP/DOWN0 = 0 for DOWN, UP/DOWN0 = 1 for UP) 1: Inversed (UP/DOWN0 = 0 for UP, UP/DOWN0 = 1 for DOWN)
RH1_UPDOWN_POL	RW	Digital Rheostat1 UP/DOWN Polarity Selection 0: Default (UP/DOWN1 = 0 for DOWN, UP/DOWN1 = 1 for UP) 1: Inversed (UP/DOWN1 = 0 for UP, UP/DOWN1 = 1 for DOWN)

Register Name	Access Type	Register Bit Description
RH_MODE	RW	Rheostat Mode Selection 0: Two Individual Rheostats (RH0 and RH1) 1: POT Mode (RH0_SET [9:0] determines the POT value), rheostat1 is the inverted 10bits)
RH_DATA_MAP	RW	EPG (8-bit) to Rheostat (10-bit) Data Mapping Selection 0: From MSB (Two bits from LSB are filled with '00b') 1: From LSB (Two bits from MSB are filled with '00b')
RH0_EN	RW	Rheostat0 Enable Control 0: Disable 1: Enable
RH1_EN	RW	Rheostat1 Enable Control 0: Disable 1: Enable
RH0_READ[9:0]	RO	Digital Rheostat0 Readback Data (Read-only) 00 0000 0000b: R_{RH_MIN} ~ 11 1111 1111b: R_{RH}
RH1_READ[9:0]	RO	Digital Rheostat1 Readback Data (Read-only) 00 0000 0000b: R_{RH_MIN} ~ 11 1111 1111b: R_{RH}

14.2 Potentiometer Mode

When the RH_MODE bit (Reg[1228]) is set to '1', the two rheostats work as one 3-pin potentiometer. In this mode, the RH0 resistance is set by the RH0_SET[9:0] register and the RH1_SET[9:0] becomes the inverted value of the RH0_SET[9:0] register. In potentiometer mode, the RH0_B pin and the RH1_A pin must be connected externally as shown in Figure 116.

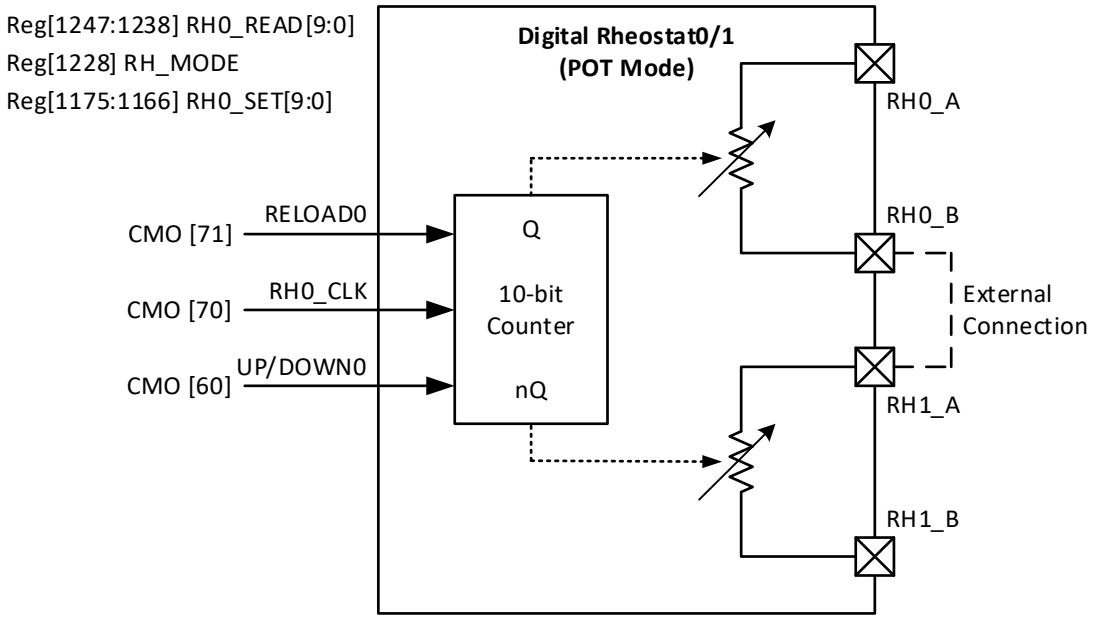


Figure 116. Two Rheostats in Potentiometer Mode

14.3 Calculating Actual Rheostat Resistance

In applications where the knowledge of the absolute rheostat resistance is critical, it can be calculated using the rheostat tolerance data stored in the NVM. This two-byte tolerance data for each rheostat are stored at ADDR 0x95 thru 0x98. The structure of rheostat tolerance data is shown in Figure 117.

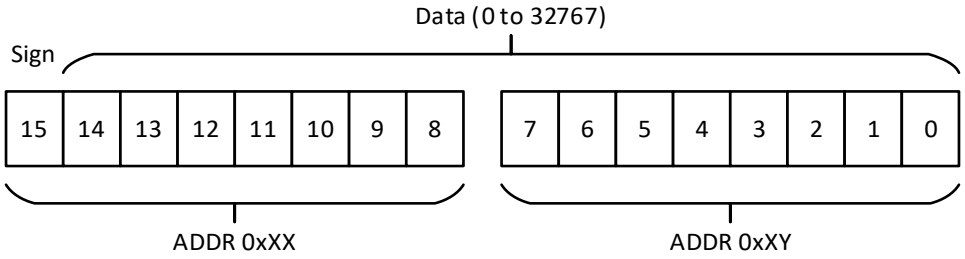


Figure 117. Rheostat Tolerance Data Structure

Bit15 represents the sign (0 = positive, 1 = negative) of the tolerance data and the remaining 15 bits (Bit14 – Bit0) converted in decimal system corresponds to the absolute difference between the target value (100 kΩ) and the actual maximum rheostat resistance measured at T_A = +25 °C.

The actual rheostat resistance value at the given code and the maximum rheostat resistance can be calculated by the following formulae.

$$R_{CODE} = (R_{RH} – R_{RH\_MIN}) \times (CODE/1023) + R_{RH\_MIN}$$

$$R_{RH} = 100 \times 10^3 + (SIGN_{RH\_TOL} \times R_{RH\_TOL})$$

where, R_{CODE}: Rheostat resistance for the given code

R_{RH}: Total rheostat resistance

R_{RH_MIN}: Minimum rheostat resistance

CODE: Rheostat position ranging from 0x000 to 0x3FF

$SIGN_{RH\_TOL}$: Sign of rheostat tolerance data defined by the MSB (Bit15)

R_{RH_TOL}: 15-bit rheostat tolerance data value (Bit14 – Bit0).

For example, the value of rheostat tolerance data written in the NVM is 0x2B67. It corresponds to +11111 in decimal system. Hence, the maximum R_{Pot} value is 100000 + 11111 = 111111 Ω.

14.3.1 Changing Rheostat Value Directly through I²C

The rheostat value can be set directly through I²C serial interface as the data in the digital rheostat registers (10-bit) can be read and written through I²C interface if not protected. As shown in Figure 118, the host processor (I²C controller) uses a user-defined trim algorithm to change the rheostat value through I²C interface.

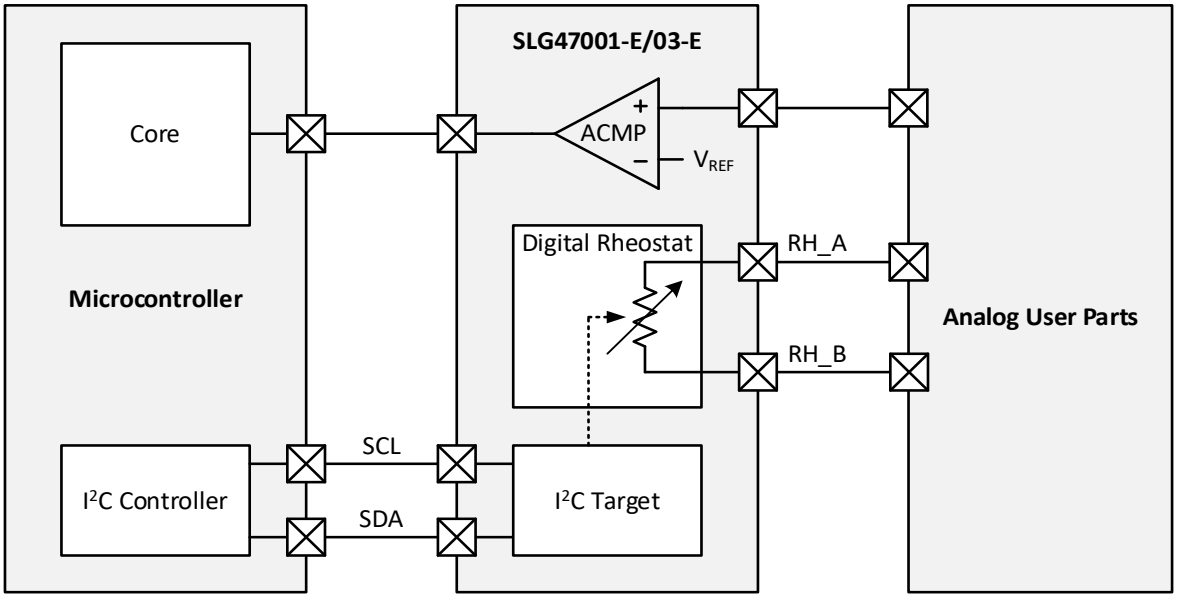


Figure 118. Hardware Configuration Example

The host processor can use its internal resources such as an ADC to read system data, find the error, and adjust the digital rheostat value. Also, it is possible to change the digital rheostat value for different conditions. For example, the I²C controller block can change the digital rheostat value based on a temperature change to reduce the system error due to the temperature.

14.4 Typical Performance of Digital Rheostat

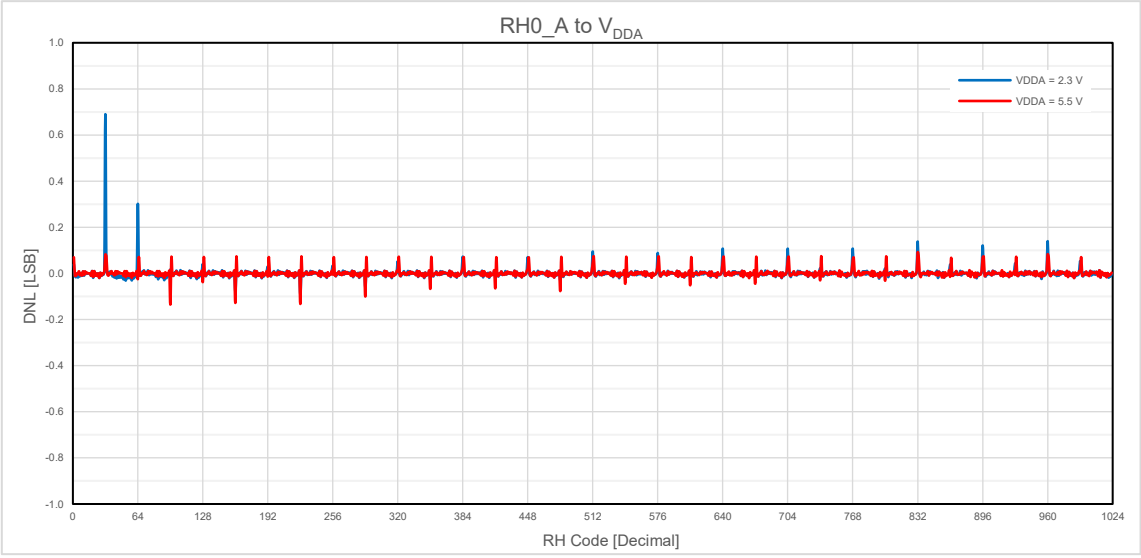


Figure 119. DNL vs. Digital Code in Rheostat Mode (V_{RHx_A} - V_{RHx_B} = 1 V) at T_A = +25 °C

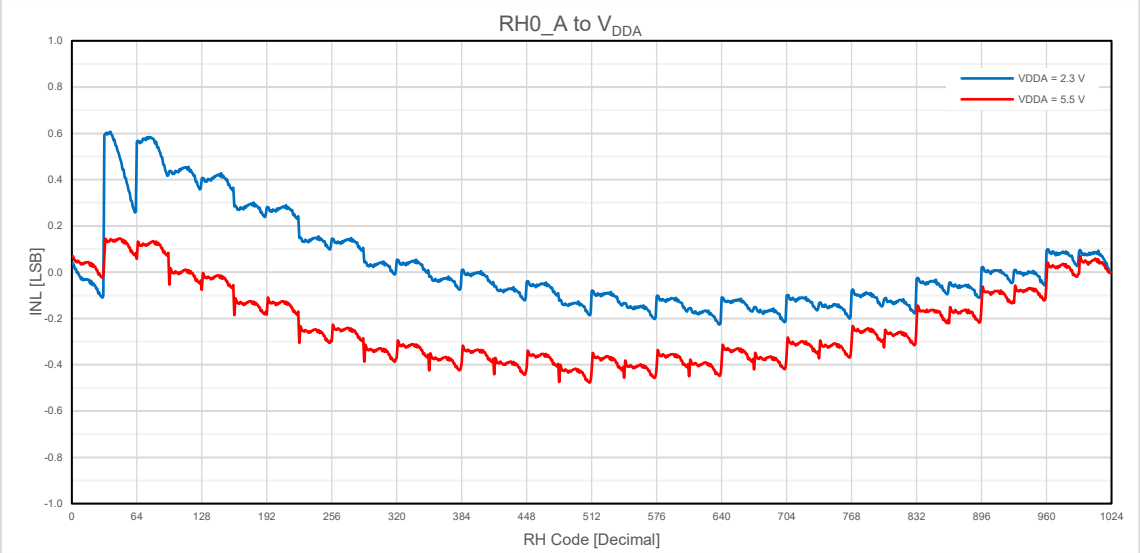


Figure 120. INL vs. Digital Code in Rheostat Mode (V_{RHx_A} - V_{RHx_B} = 1 V) at T_A = +25 °C

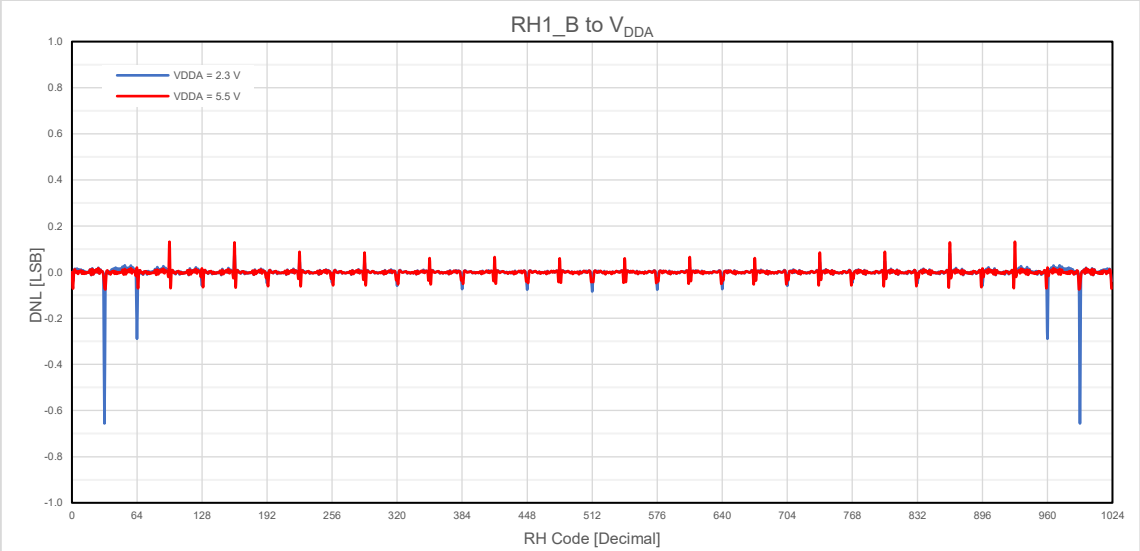


Figure 121. DNL vs. Digital Code in Potentiometer Mode (V_{RHx_A} - V_{RHx_B} = 1 V) at T_A = +25 °C

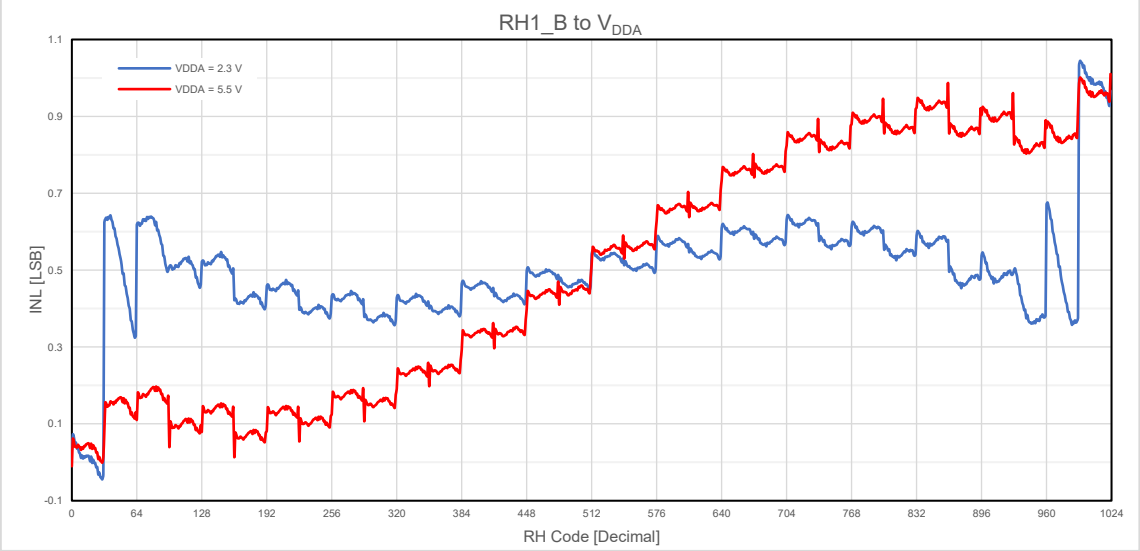


Figure 122. INL vs. Digital Code in Potentiometer Mode (V_{RHx_A} - V_{RHx_B} = 1 V) at T_A = +25 °C

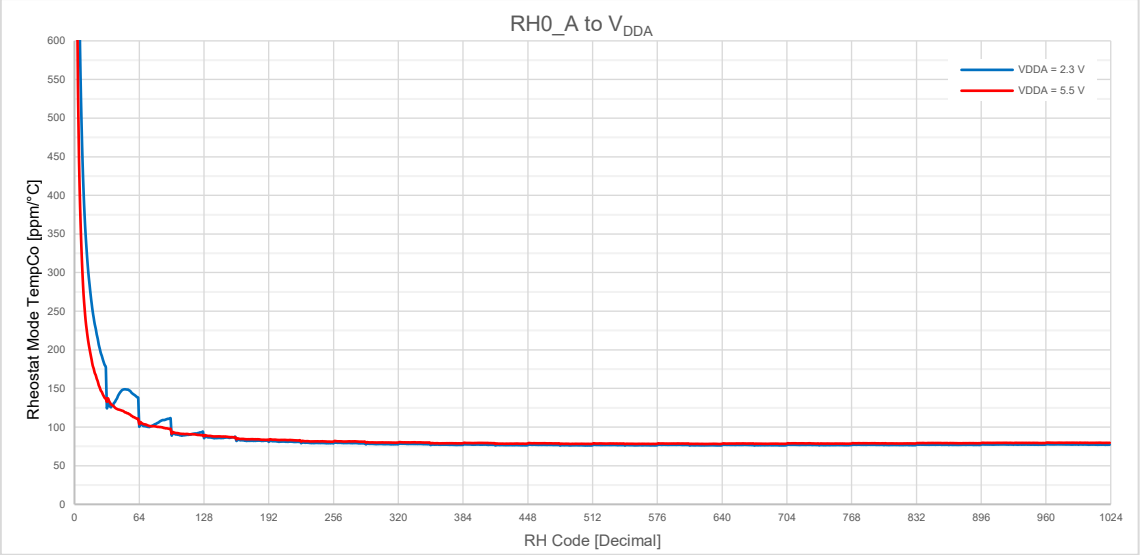


Figure 123. Temperature Coefficient ($\Delta R_{AB}/R_{AB})/\Delta T_A$ in Rheostat Mode

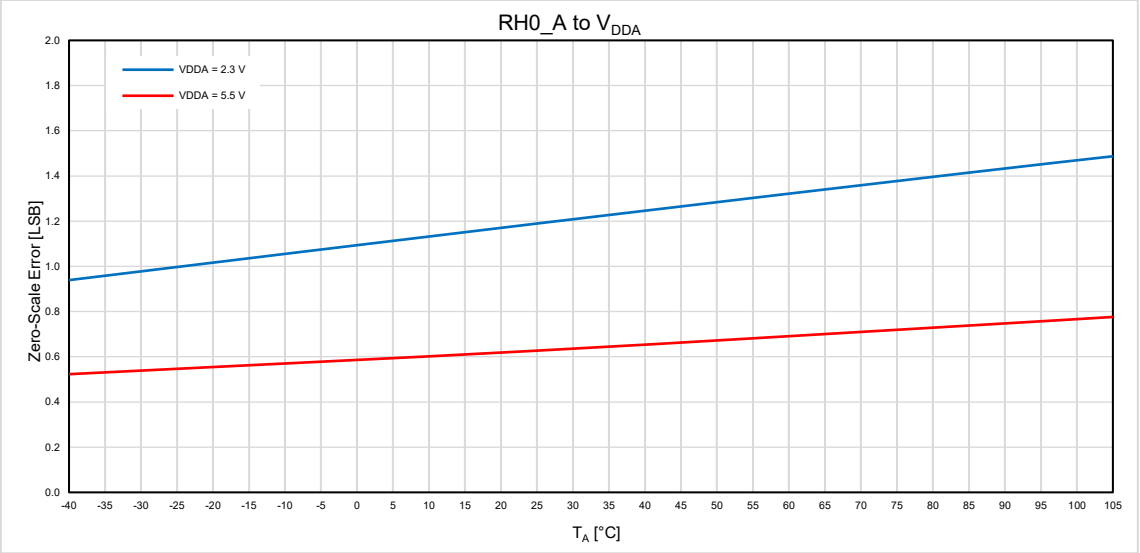


Figure 124. Rheostat Zero Scale Error vs. Temperature (V_{RHx_A} - V_{RHx_B} = 1 V)

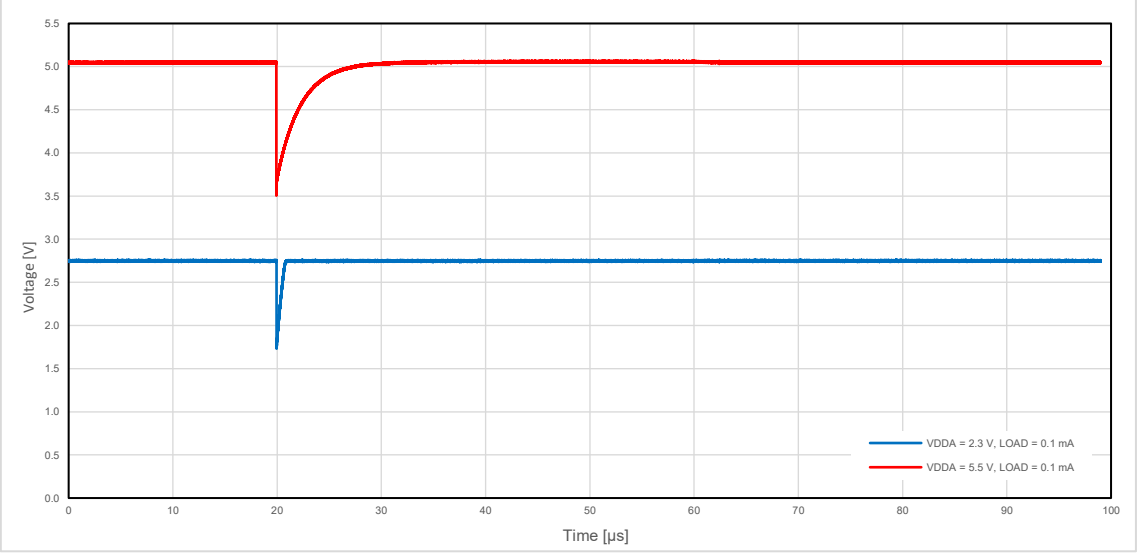


Figure 125. Rheostat Worst-Case (Code = 511 to 512) Transition Glitch

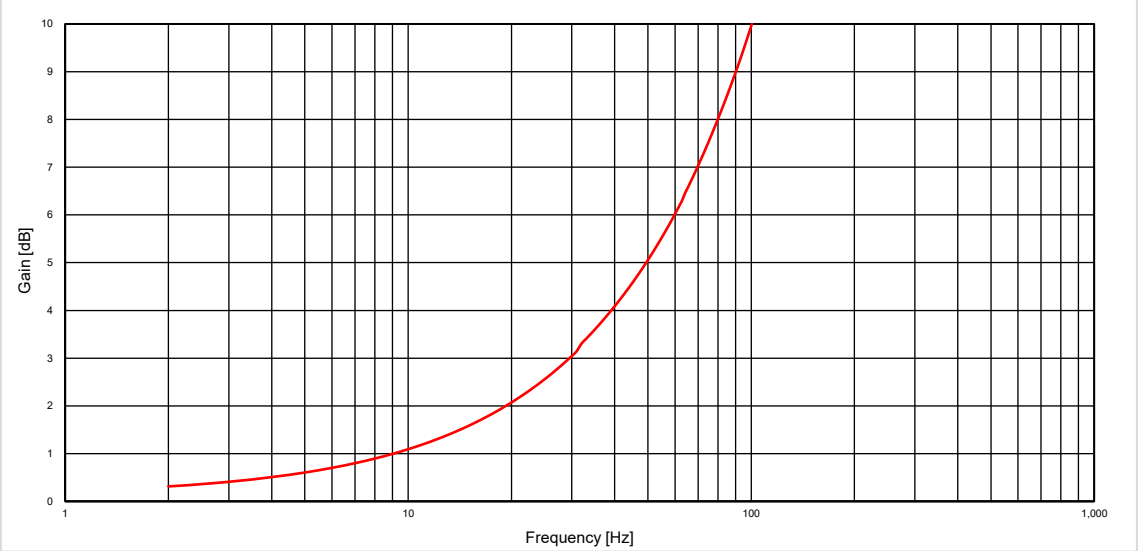


Figure 126. Rheostat Gain vs. Frequency (Code = 512) at V_{DDA} = 5.0 V, T_A = +25 °C

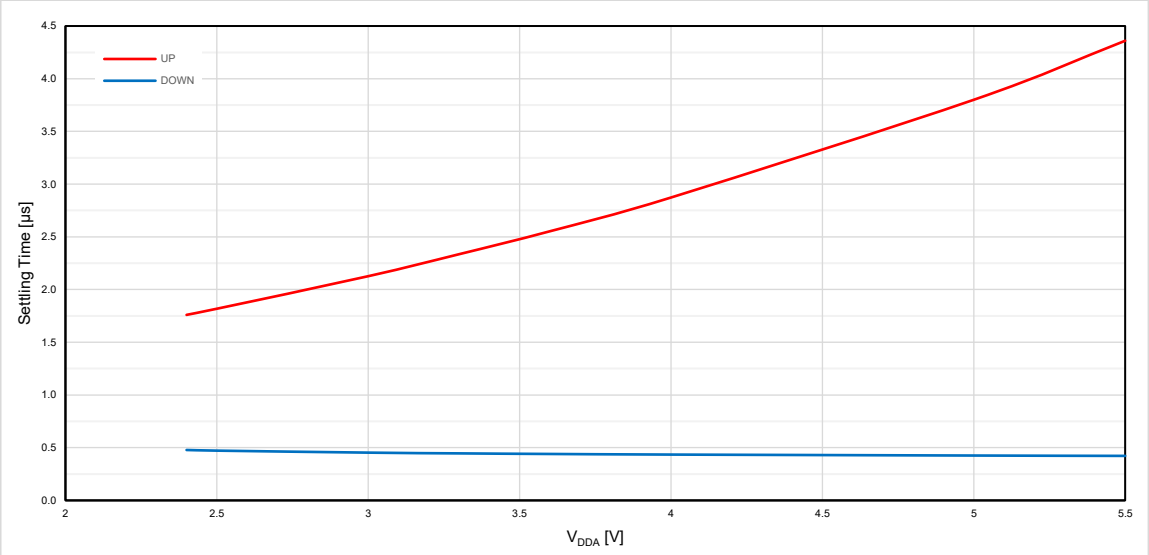


Figure 127. Rheostat Settling Time vs. V_{DD} at I_{LOAD} = 1 mA, T_A = +25 °C

15. Extended Pattern Generator

15.1 EPG General Description

The SLG47001-E/03-E has one 8-bit width converter logic macrocell designed to provide data from the part of the NVM to the connection matrix. The macrocell takes 8-bit data from part of the NVM parallel output. The initial value of the extended pattern generator (EPG) output is defined by the register value at ADDR 0xBA. This initial value appears at the output of the EPG macrocell after power-up or reset (EPG nRST signal from CMO [69]).

When the internal pointer reaches the last address of the 59 bytes of the EPG programming range (ADDR 0xC2 through 0xFE) in the NVM, users can select the behavior of the internal counter by the EPG_OVF_MODE bit (Reg[703]):

- If EPG_OVF_MODE = 0, the internal counter will overflow and reset to 0xC2.
- If EPG_OVF_MODE = 1, the internal counter will stop when reaching the last byte of the NVM (0xFC).

When the EPG nRST input is pulled low, the NVM pointer sets to the beginning of the EPG programming range (0xC2) and the initial value from ADDR 0xBA is loaded to the outputs.

The EPG supports four conversion modes and the maximum clock frequency allowed for each EPG mode is shown in Table 23.

- 8 → 8 Mode (8-bit parallel output)
- 8 → 4 Mode (8-bit word to two 4-bit words)
- 8 → 2 Mode (8-bit word to four 2-bit words)
- 8 → 1 Mode (8-bit word to serial bit stream).

Table 23. Maximum EPG CLK Frequency

EPG Mode	Maximum CLK Frequency
8 → 8	1 MHz
8 → 4	2 MHz
8 → 2	4 MHz
8 → 1	8 MHz

The EPG can also drive both digital rheostats in rheostat mode. See details in section 15.3 EPG in Rheostat Mode.

Table 24. EPG Configuration Registers

Register Name	Access Type	Register Bit Description
EPG_MODE[1:0]	RW	EPG Conversion Mode Selection 00b: 8 → 8 Mode (8-bit Parallel Output) 01b: 8 → 4 Mode (8-bit Word to Two 4-bit Words) 10b: 8 → 2 Mode (8-bit Word to Four 2-bit Words) 11b: 8 → 1 Mode (8-bit Word to Serial Bit Stream)
EPG_OVF_MODE	RW	EPG Counter Overflow Mode Selection 0: EPG Counter Pointer Reset to 0xC2 1: EPG Counter Pointer Remain at 0xFC

Register Name	Access Type	Register Bit Description
RH_DATA_MAP	RW	Rheostat 8-bit Data Mapping Selection 0: From MSB 1: From LSB
EPG_RH0_EN	RW	EPG Rheostat0 Path Enable Control 0: Disable 1: Enable
EPG_RH1_EN	RW	EPG Rheostat1 Path Enable Control 0: Disable 1: Enable
EPG_INI_VAL[7:0]	RW	EPG Initial Value at POR and EPG nRST

15.2 EPG Conversion Modes

15.2.1 8 → 8 Conversion Mode

In 8 → 8 mode, EPG converts data from the NVM to 8 parallel outputs, as shown in Figure 128 and Figure 129.

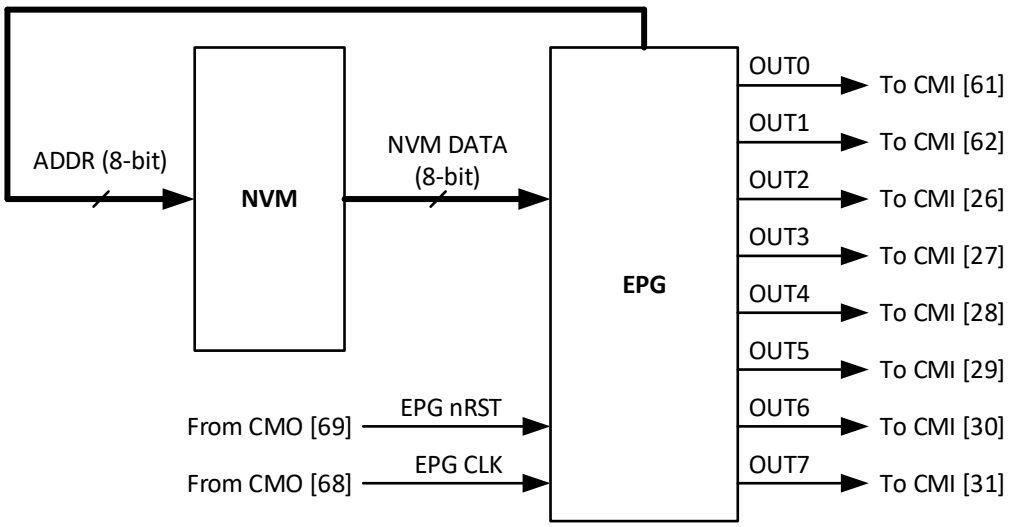


Figure 128. EPG in 8 → 8 Mode Functional Diagram

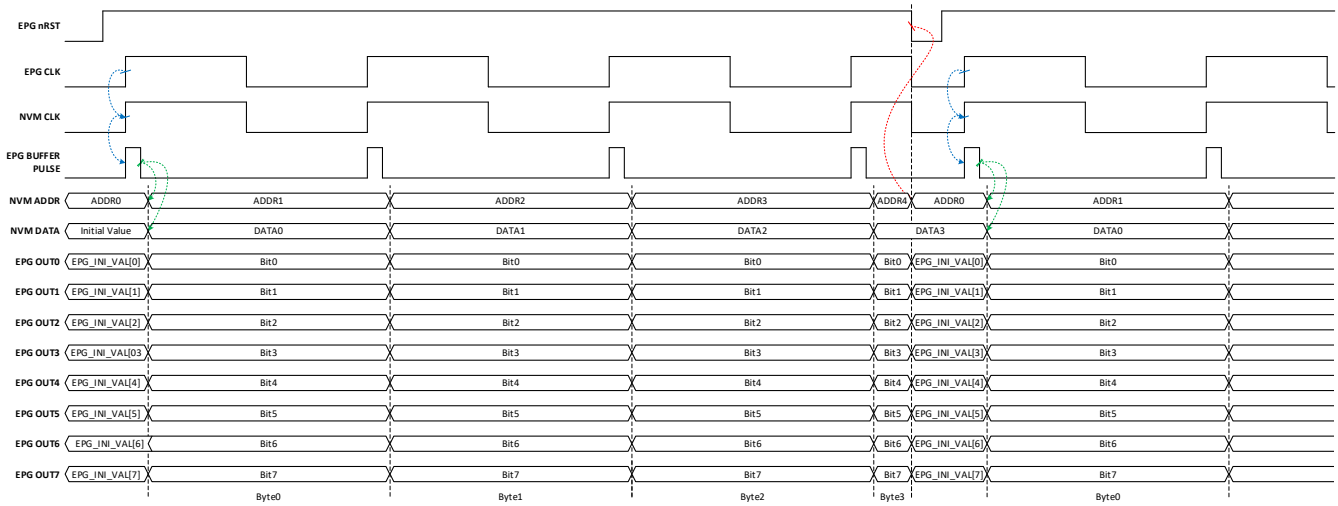


Figure 129. EPG in 8 → 8 Mode Output Waveforms

15.2.2 8 → 4 Conversion Mode

In 8 → 4 mode, EPG converts 8-bit word from the NVM to two 4-bit words in 4 parallel outputs. See Figure 130 and Figure 131.

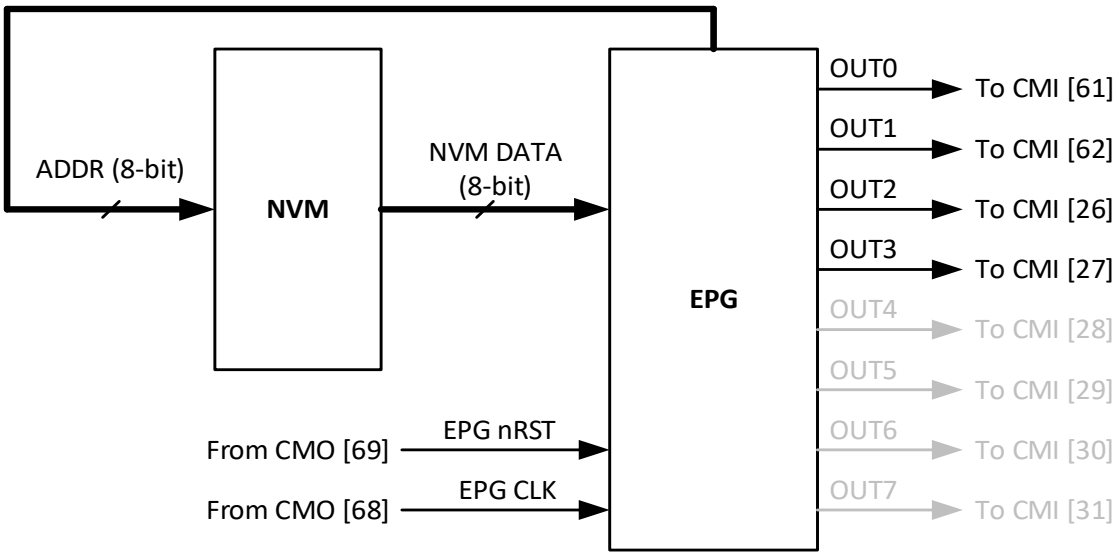


Figure 130. EPG in 8 → 4 Mode Functional Diagram

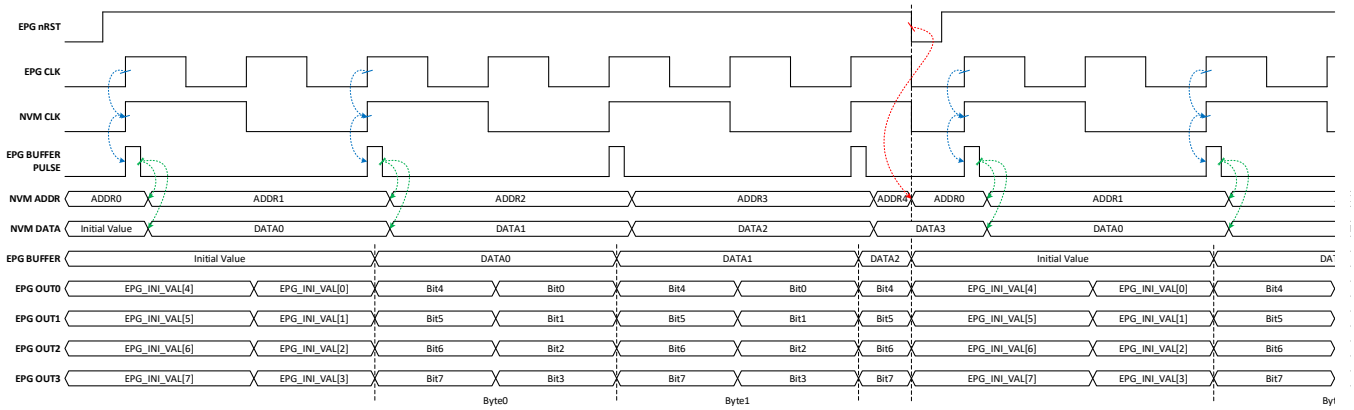


Figure 131. EPG in 8 → 4 Mode Output Waveforms

15.2.3 8 → 2 Conversion Mode

In 8 → 2 mode, EPG converts 8-bit word from the NVM to four 2-bit words in 2 parallel outputs. See Figure 132 and Figure 133.

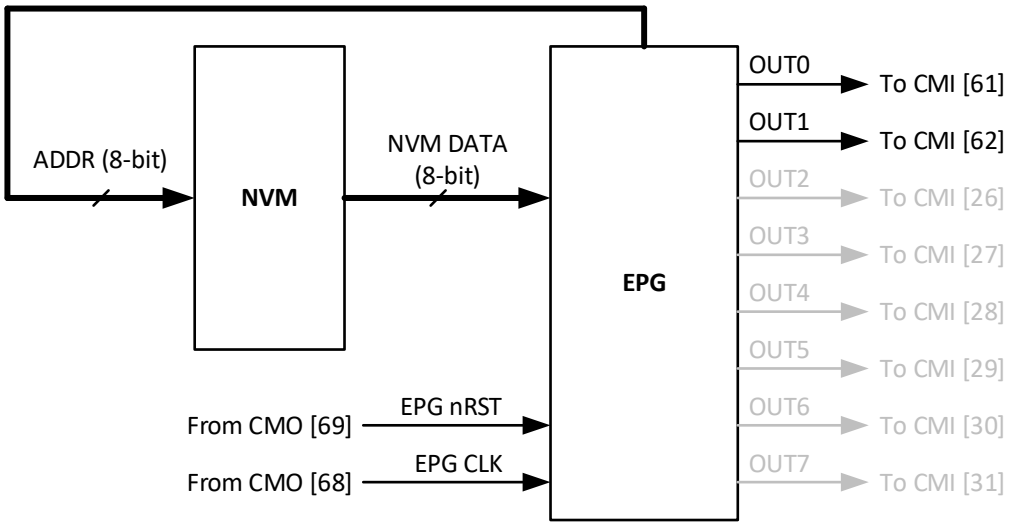


Figure 132. EPG in 8 → 2 Mode Functional Diagram

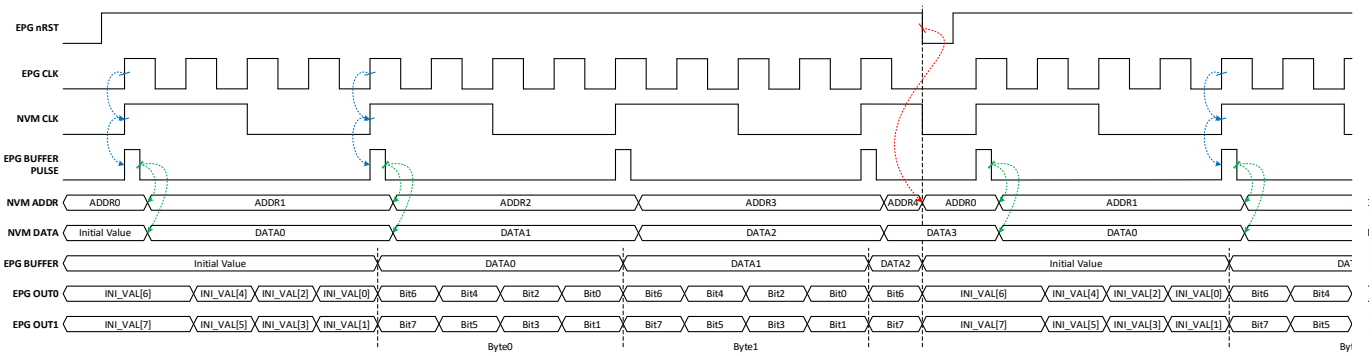


Figure 133. EPG in 8 → 2 Mode Output Waveforms

15.2.4 8 → 1 Conversion Mode

In 8 → 1 mode, EPG converts 8-bit word from the NVM to a serial bit stream output. See Figure 134 and Figure 135.

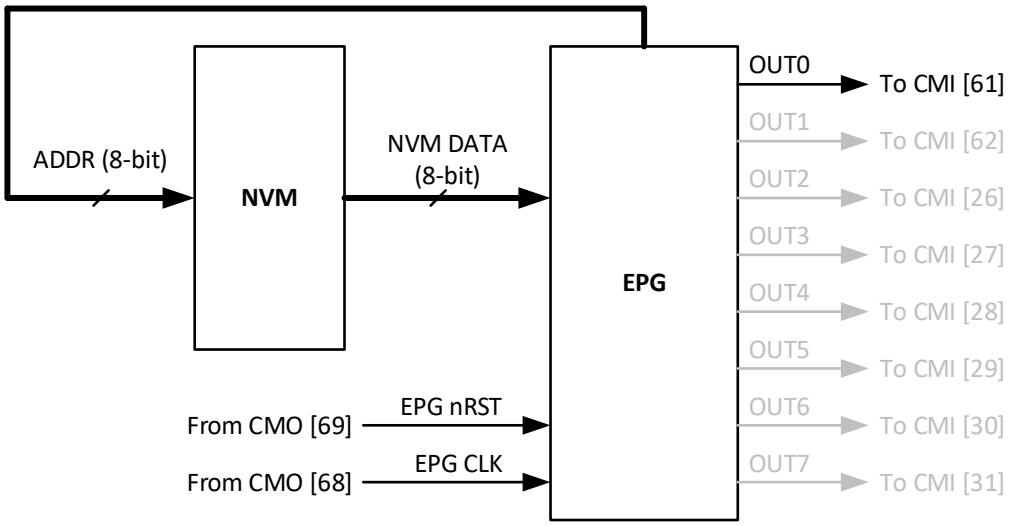


Figure 134. EPG in 8 → 1 Mode Functional Diagram

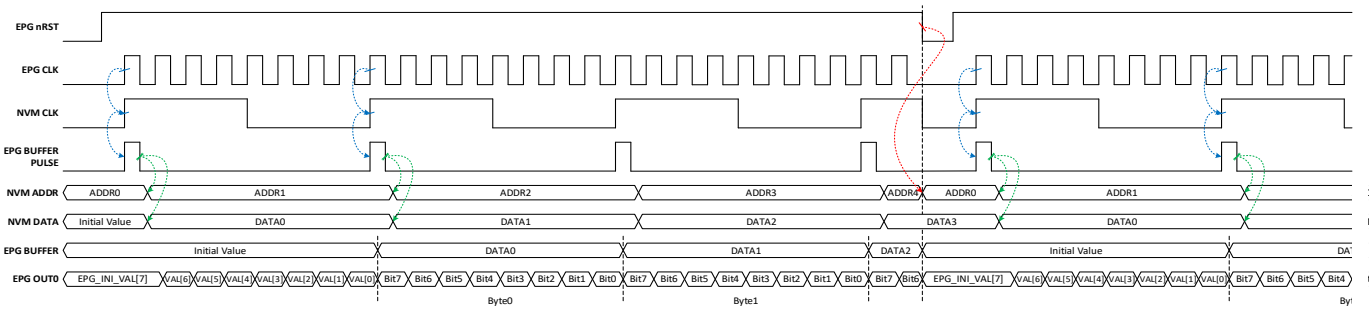


Figure 135. EPG in 8 → 1 Mode Output Waveforms

15.3 EPG in Rheostat Mode

As shown in Figure 136, the digital rheostats can be driven by the EPG when the EPG_RH0_EN (Reg[1226]) and/or the EPG_RH1_EN (Reg[1227]) registers are set to '1'. In rheostat mode, the 8-bit data from the EPG will be loaded into the activated rheostat counters at the rising edge of the corresponding RELOAD signal. The RH_DATA_MAP bit (Reg[1229]) determines how the 8-bit of EPG data will be mapped to the 10-bit rheostat counters. When RH_DATA_MAP = 0 (Default), the EPG data will be mapped from the MSB of the rheostat counter data and the 'Bit1' and 'Bit0' will be filled with '00b'. In case precise rheostat resistance control is needed, the EPG data can be mapped from the LSB by setting RH_DATA_MAP = 1 and the 'Bit9' and 'Bit8' will be filled with '00b' accordingly. Even in rheostat mode, the rheostat counter data can be increased or decreased using the UP/DOWN and the CLK inputs of each rheostat.

During the power-on event, the initial values stored in the NVM will be loaded onto the RH0_SET[9:0] and the RH1_SET[9:0] registers and the rheostat counter values are updated with the initial values. Once the EPG_RHx_EN bit is set to '1', the corresponding rheostat will be controlled by the EPG data, however the rheostat counter data can be overwritten by writing a new 10-bit data onto the RH0_SET[9:0] and the RH1_SET[9:0] registers. Note that the rheostat counter values will be updated at the 'STOP' condition of the I^2C write command.

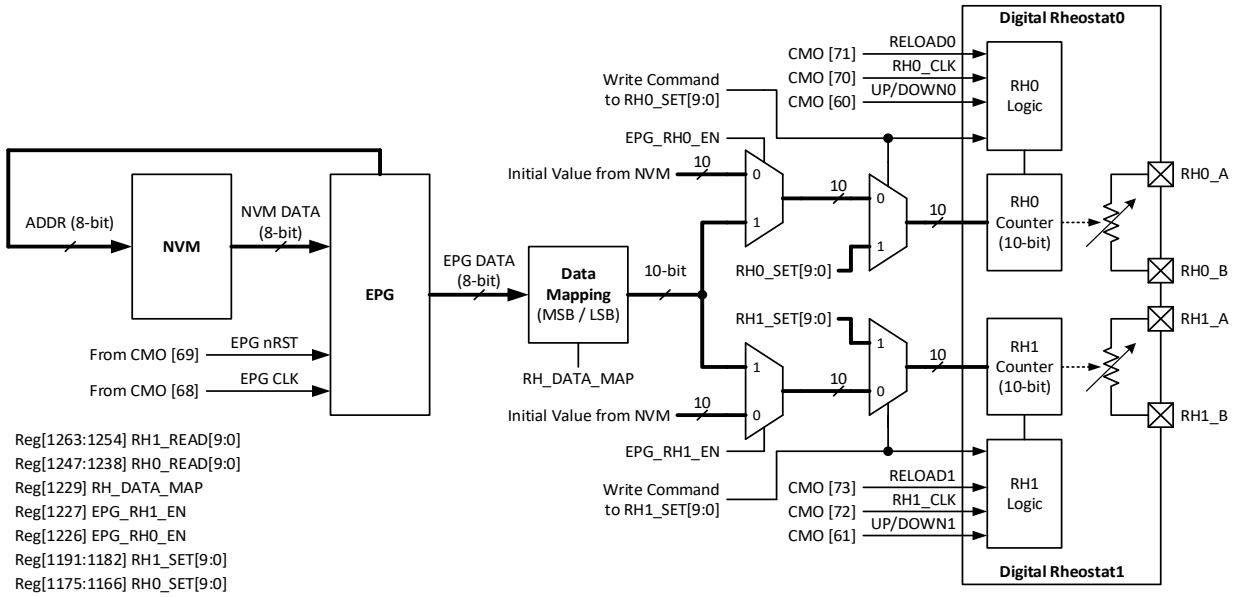


Figure 136. EPG in Rheostat Mode Functional Diagram

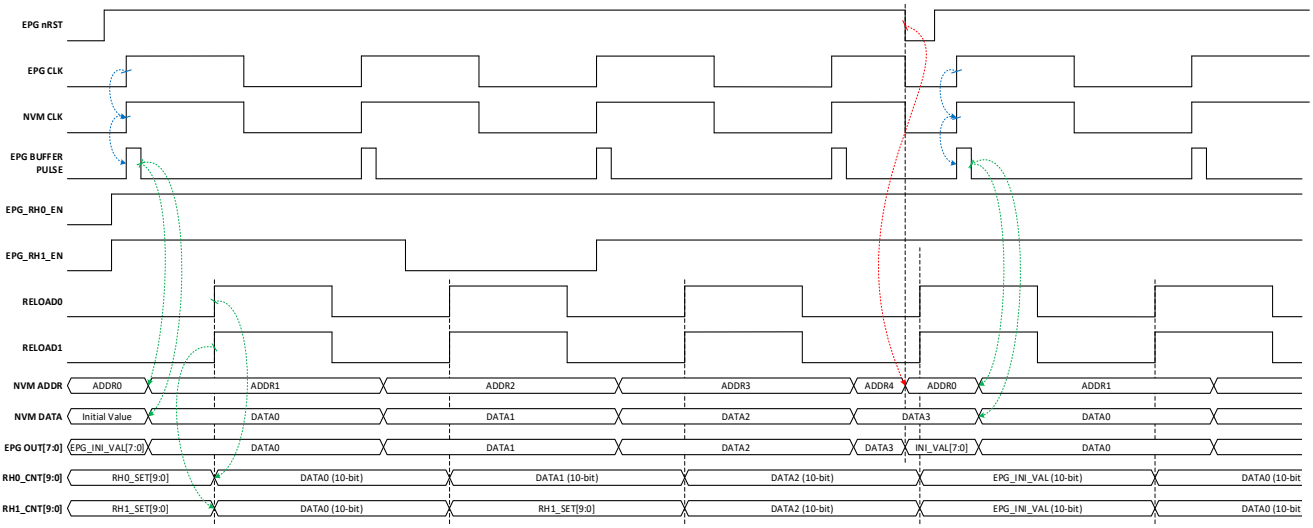


Figure 137. EPG in Rheostat Mode Output Waveforms with EPG_RHx_EN

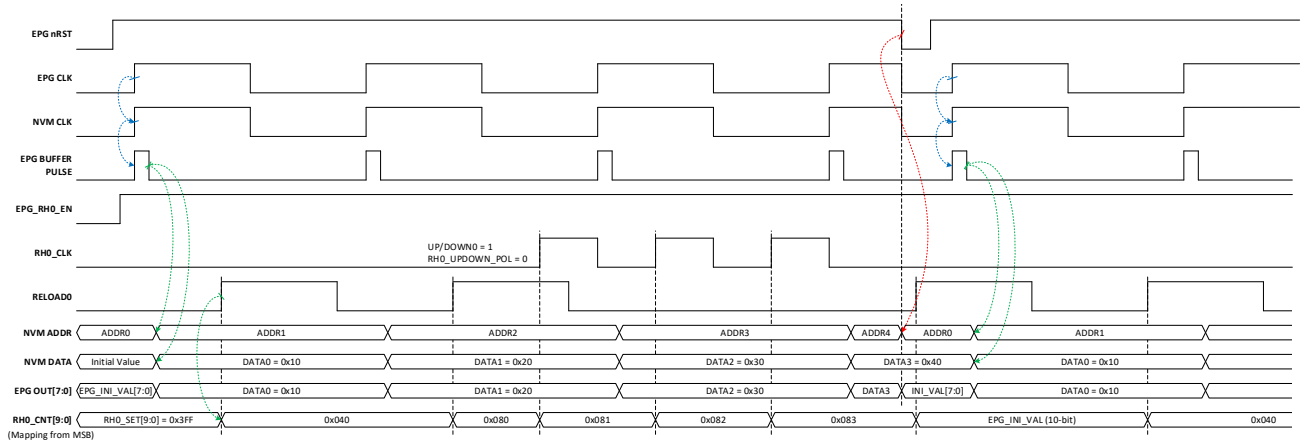


Figure 138. EPG in Rheostat Mode Output Waveforms with RH0_CLK, RELOAD0

16. Clocking

16.1 Clocking General Description

The SLG47001-E/03-E has two internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz or 10 kHz optional selection)
- Oscillator1 (25 MHz).

Oscillator0 can operate in one of two modes (2.048 kHz or 10 kHz) selected by the OSC0_FREQ bit (Reg[717]). There are two clock divider stages for each oscillator that allow for flexibility for providing clock signals to the connection matrix inputs as well as various other macrocells. The OSC0_PRE_DIV[1:0] register (Reg[719:718]) selects the pre-divider (first stage) options (/1, /2, /4 and /8) for OSC0. The pre-divider (first stage) options (/1, /2, /4, /8, /12, /24, and /48) for OSC1 is selected by the OSC1_PRE_DIV[2:0] register (Reg[710:708]). The input of the second stage divider is connected to the output of the pre-divider, and it has eight frequency divider options (/1, /2, /3, /4, /8, /12, /24 and /64) determined by the OSC0_OUT1_DIV[2:0], the OSC0_OUT2_DIV[2:0], and the OSC1_OUT_DIV[2:0] registers. The second stage divider outputs are connected to CMI [46], CMI [47], and CMI [48] respectively. These three outputs are individually enabled by the OSC0_OUT1_EN (Reg[723]), the OSC0_OUT2_EN (Reg[727]), and the OSC1_OUT_EN (Reg[707]) registers. See Figure 139, Figure 140 and Figure 141 for more details on the SLG47001-E/03-E clocking scheme.

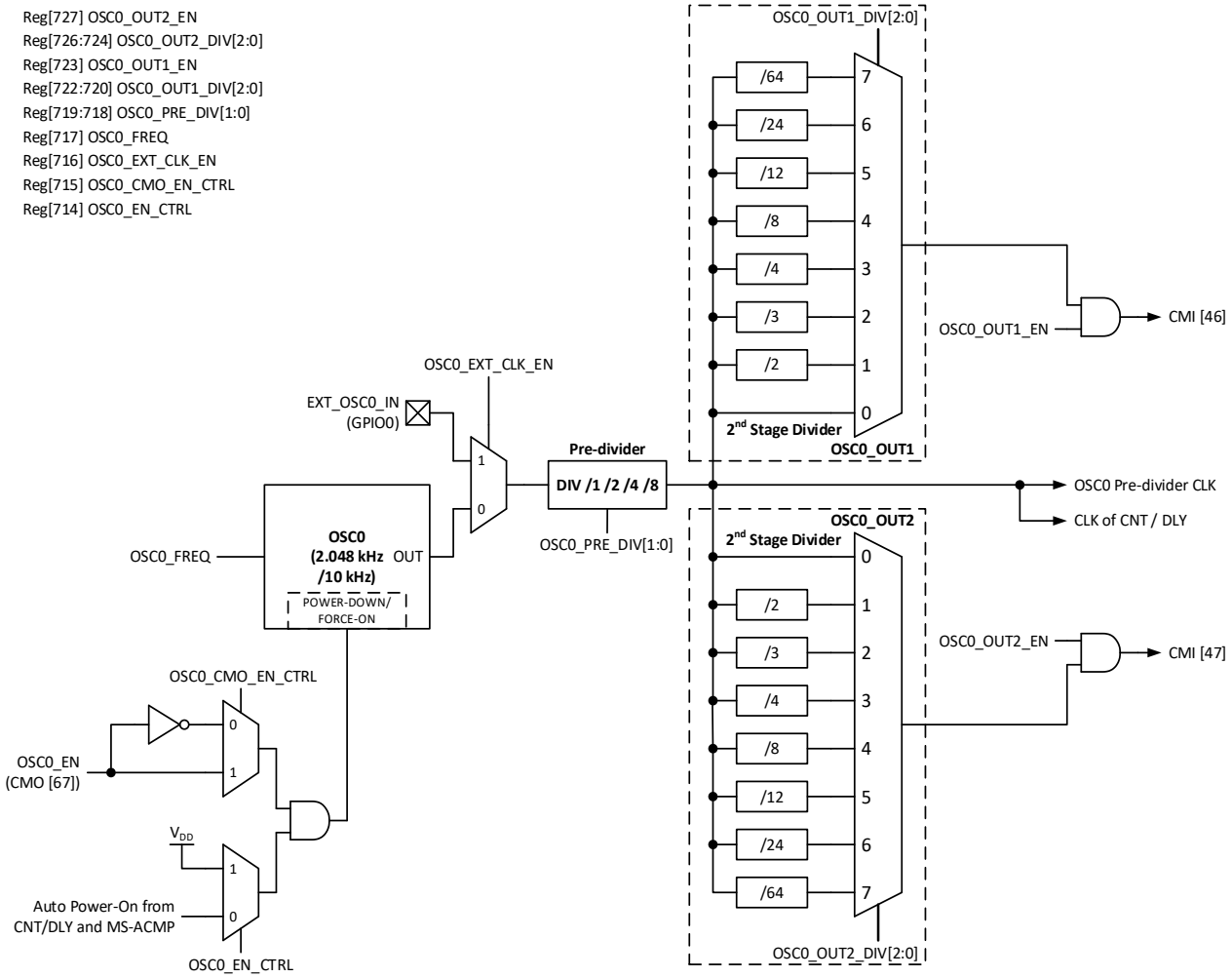


Figure 139. Oscillator0 (2.048 kHz or 10 kHz) Block Diagram

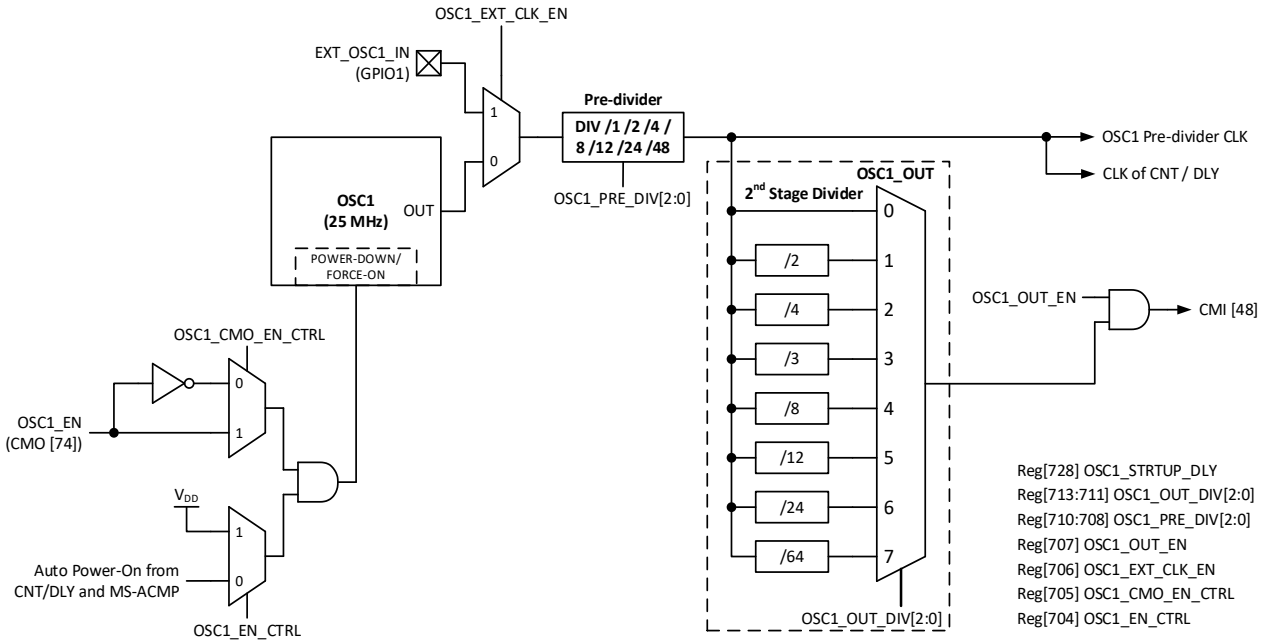


Figure 140. Oscillator1 (25 MHz) Block Diagram

The OSC0_CMO_EN_CTRL bit (Reg[715]) selects either forced disable or forced enable of OSC0 when CMO [67] = 1. In the same way, the OSC1_CMO_EN_CTRL bit (Reg[705]) selects either forced disable or forced enable of OSC1 when CMO [74] = 1. In case the OSC enable signals from the connection matrix outputs (CMO [67] and CMO [74]) are low ('0'), the OSC0_CMO_EN_CTRL and the OSC1_CMO_EN_CTRL bits are ignored (does not affect OSC enable logic). The OSC enable signals from CMOs have higher priority than the OSCx_EN_CTRL registers. When both the OSC enable signal from CMO and the OSCx_EN_CTRL are low ('0'), the OSC enable logic is determined by the OSC enable request from the CNT/DLY macrocells (for OSC0 and OSC1) and the MS-ACMP (OSC0 only). The operating modes of the oscillators are shown in Table 25.

The first rising edge of the oscillator should appear within one period. The oscillator frequency should settle down within no more than 10 periods of the high-speed oscillator.

The OSC1 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by the OSC1_STRTUP_DLY bit (Reg[728]). This function is recommended to be used when analog blocks are used along with the oscillator.

Table 25. Oscillator Operating Modes

POR	OSC Trim EN	Ext. CLK EN	OSC EN Signal from CMO	OSCx_CMO_EN_ CTRL Register	OSCx_EN_CTRL Register	OSC EN Request from CNT/DLY (OSC0 and OSC1) and MS-ACMP (OSC0 only)	OSC Operating Mode
0	X	X	X	X	X	X	OFF
1	0	1	X	X	X	X	OSC is OFF, Logic is ON
1	0	0	1	0	X	X	OFF
1	0	0	1	1	X	X	ON
1	0	0	0	X	1	X	ON
1	0	0	0	X	0	1	ON

POR	OSC Trim EN	Ext. CLK EN	OSC EN Signal from CMO	OSCx_CMO_EN_CTRL Register	OSCx_EN_CTRL Register	OSC EN Request from CNT/DLY (OSC0 and OSC1) and MS-ACMP (OSC0 only)	OSC Operating Mode
1	0	0	0	X	0	0	OFF
1	1	X	X	X	X	X	ON
[1] 'X' denotes 'don't care' condition.							

Table 26. OSC Configuration Registers

Register Name	Access Type	Register Bit Description
OSC0_EN_CTRL	RW	OSC0 (LFOSC) Enable Control 0: Auto Power-ON by Delay Cells 1: Always ON
OSC0_CMO_EN_CTRL	RW	OSC0 (LFOSC) CMO Enable Control Selection 0: OSC0 is forced disabled when CMO [67] = 1 1: OSC0 is forced enabled when CMO [67] = 1
OSC0_EXT_CLK_EN	RW	External Clock Source Enable Control 0: Disable (Internal LFOSC) 1: External CLK from GPIO0
OSC0_FREQ	RW	OSC0 (LFOSC) Frequency Selection 0: 2.048 kHz 1: 10 kHz
OSC0_PRE_DIV[1:0]	RW	OSC0 (LFOSC) Pre-divider Selection 00b: /1 01b: /2 10b: /4 11b: /8
OSC0_OUT1_DIV[2:0]	RW	OSC0 (LFOSC) 1st Output Second Stage Divider Selection 000b: /1 001b: /2 010b: /3 011b: /4 100b: /8 101b: /12 110b: /24 111b: /64
OSC0_OUT1_EN	RW	OSC0 (LFOSC) 1st Output (To CMI [46]) Enable Control 0: Disable 1: Enable
OSC0_OUT2_DIV[2:0]	RW	OSC0 (LFOSC) 2nd Output Second Stage Divider Selection 000b: /1 001b: /2 010b: /3 011b: /4 100b: /8 101b: /12 110b: /24 111b: /64

Register Name	Access Type	Register Bit Description
OSC0_OUT2_EN	RW	OSC0 (LFOSC) 2nd Output (To CMI [47]) Enable Control 0: Disable 1: Enable
OSC1_EN_CTRL	RW	OSC1 (RingOSC) Enable Control 0: Auto Power-ON by Delay Cells 1: Always ON
OSC1_CMO_EN_CTRL	RW	OSC1 (RingOSC) CMO Enable Control Selection 0: OSC1 is forced disabled when CMO [74] = 1 1: OSC1 is forced enabled when CMO [74] = 1
OSC1_EXT_CLK_EN	RW	External Clock Source Enable Control 0: Disable (Internal RingOSC) 1: External CLK from GPIO1
OSC1_OUT_EN	RW	OSC1 (RingOSC) Output (To CMI [48]) Enable Control 0: Disable 1: Enable
OSC1_PRE_DIV[2:0]	RW	OSC1 (RingOSC) Pre-divider Selection 000b: /1 001b: /2 010b: /4 011b: /8 100b: /12 101b: /24 110b: /48 111b: N/A
OSC1_OUT_DIV[2:0]	RW	OSC1 (RingOSC) Output Second Stage Divider Selection 000b: /1 001b: /2 010b: /4 011b: /3 100b: /8 101b: /12 110b: /24 111b: /64
OSC1_STRTUP_DLY	RW	OSC1 Startup Delay for 100 ns 0: Disable 1: Enable

16.2 CNT/DLY Clock Scheme

The CNT/DLY of each multi-function macrocell has its own additional clock dividers connected to the pre-dividers of the oscillators. The available dividers options are:

- OSC0 /1, OSC0 /8, OSC0 /12, OSC0 /24, OSC0 /64, OSC0 /512, OSC0 /4096.
- OSC1 /1, OSC1 /4, OSC1 /8, OSC1 /64, OSC1 /512.

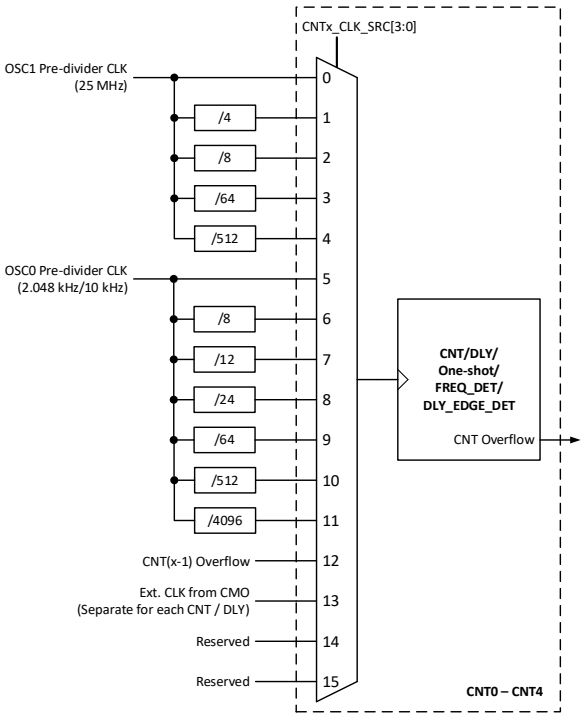


Figure 141. CNT/DLY Clock Scheme

16.3 External Clocking

The SLG47001-E/03-E supports several ways to use an external, higher accuracy clock as a reference source for the internal operations.

16.3.1 GPIO Source for Oscillator0 (2.048 kHz/10 kHz)

When the OSC0_EXT_CLK_EN bit is set to '1', an external clock signal on GPIO0 will be routed in place of the internal oscillator derived from the 2.048 kHz (or 10 kHz) clock source (see Figure 139). The low and the high limits of the external clock frequency are 0 Hz and 10 MHz.

16.3.2 GPIO Source for Oscillator1 (25 MHz)

When the OSC1_EXT_CLK_EN bit is set to '1', an external clocking signal on GPIO1 will be routed in place of the internal oscillator derived from 25 MHz clock source (see Figure 140). The external frequency ranges for different V_{DD} voltages are shown below:

- **V_{DD} = 2.3 V**: 0 Hz to 20 MHz
- **V_{DD} = 3.3 V**: 0 Hz to 30 MHz
- **V_{DD} = 5.0 V**: 0 Hz to 50 MHz.

16.4 Oscillators Power-On Delay

When 'Auto Power-ON' is selected (OSCx_EN_CTRL = 0), the enable signal of the oscillator appears when any macrocell that uses the corresponding oscillator is powered on (see Figure 142). The values of 'Power-on Delay' are shown in section 3.4.8 Oscillator Power-On Delay.

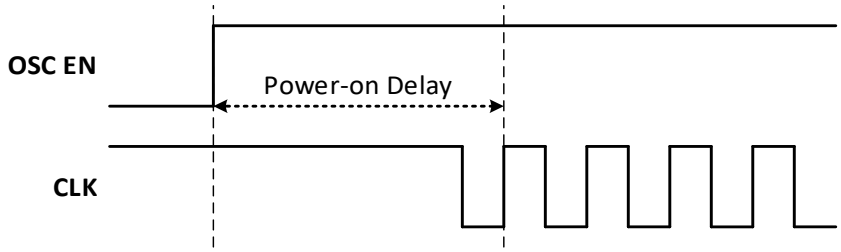


Figure 142. Oscillator Startup Diagram

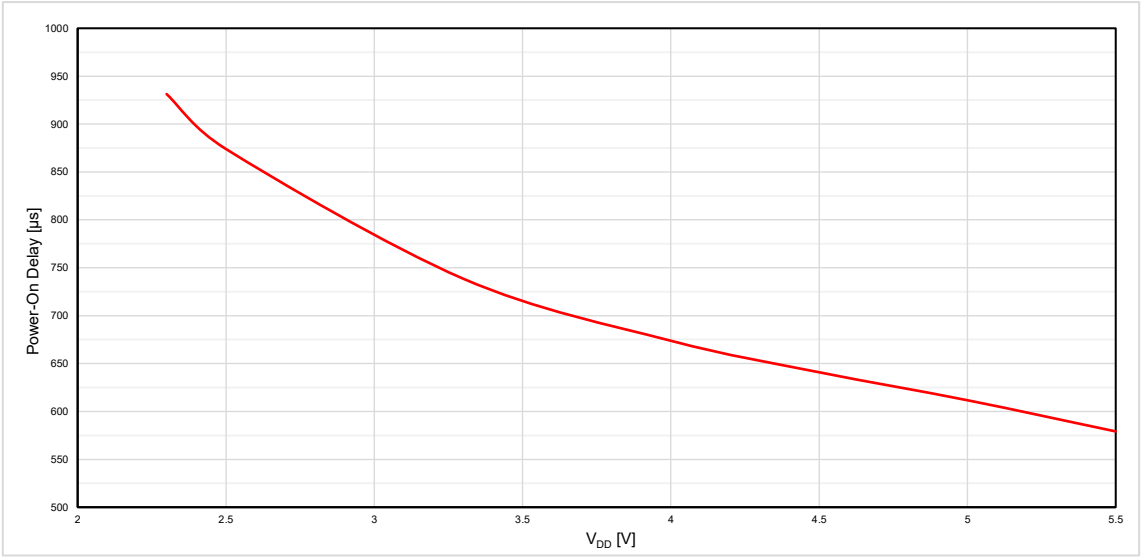


Figure 143. OSC0 (2.048 kHz) Maximum Power-On Delay vs. V_{DD} at T_A = +25 °C

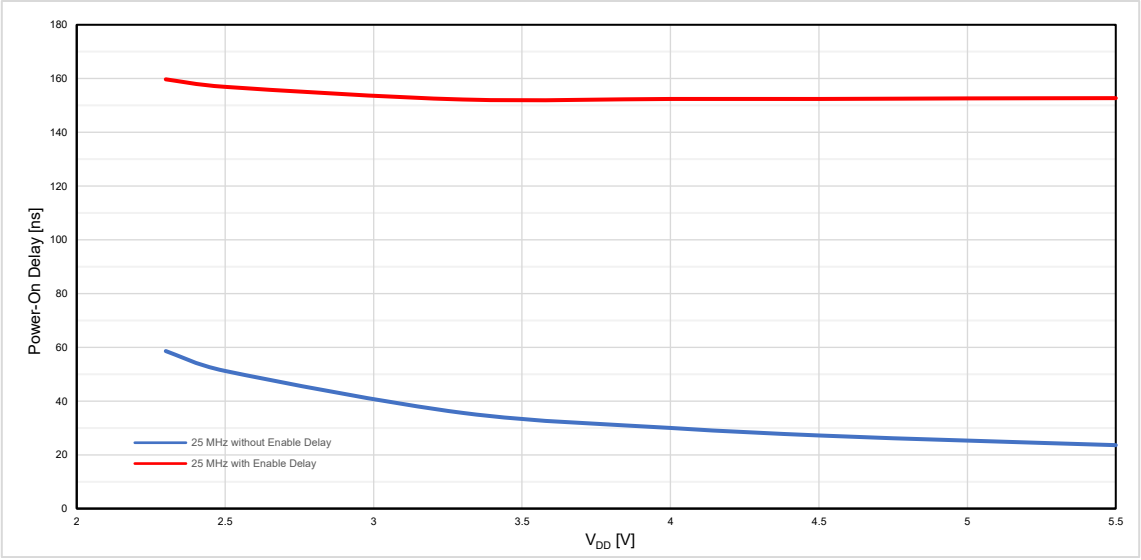


Figure 144. OSC1 (25 MHz) Maximum Power-On Delay vs. V_{DD} at T_A = +25 °C

16.5 Oscillators Accuracy

The measurement conditions are:

- Bandgap is enabled (BG_OFF_CTRL = 0).
- Oscillators are forced on (OSCx_EN_CTRL = 1).
- Oscillator outputs are enabled (OSC0_OUTx_EN = 1, OSC1_OUT_EN = 1).

For more information, see section 3.4.7 Oscillator Frequency.

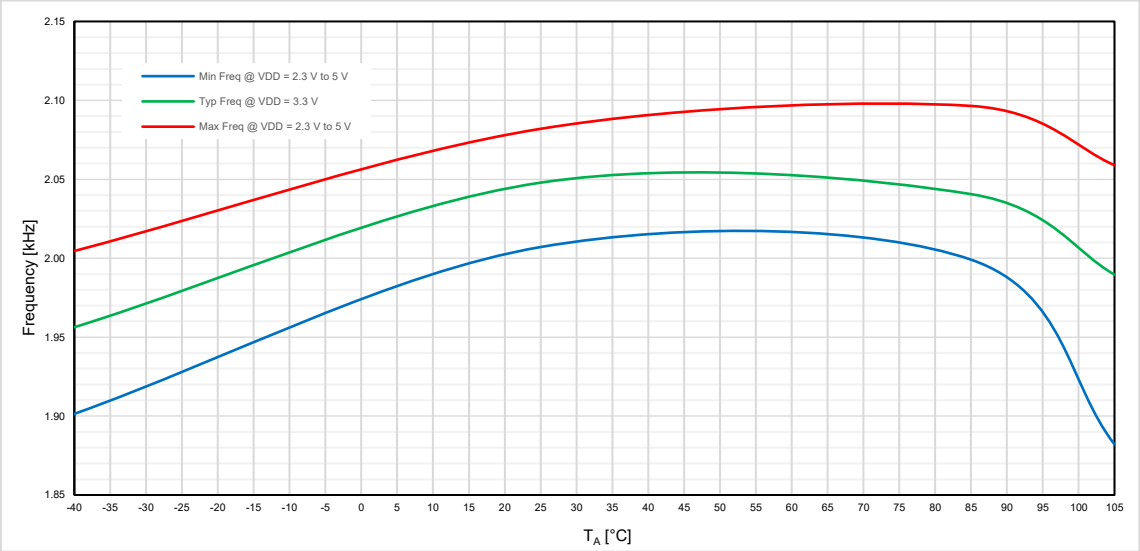


Figure 145. OSC0 (2.048 kHz) Frequency vs. T_A

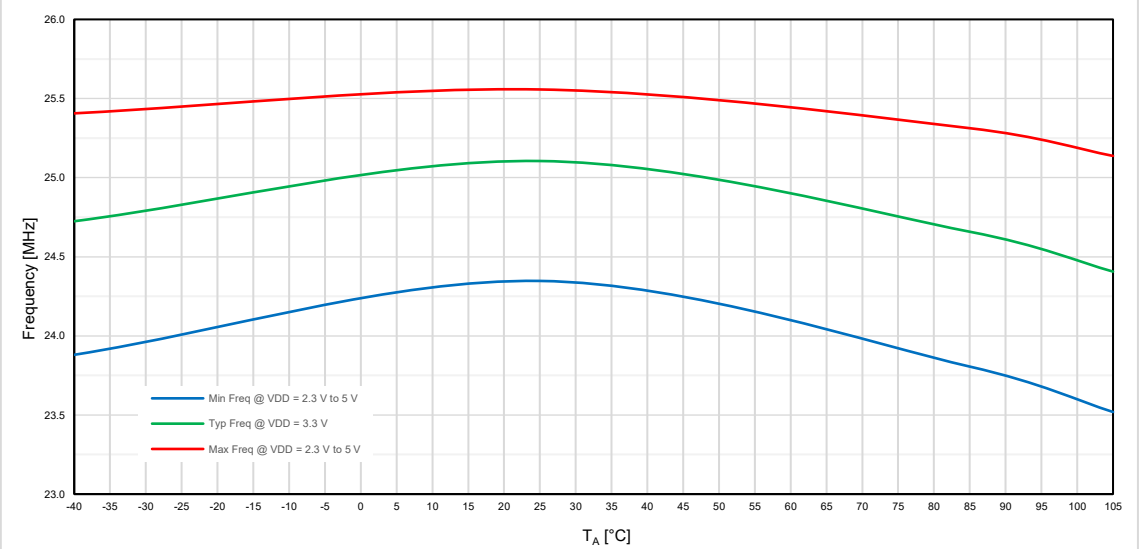


Figure 146. OSC1 (25 MHz) Frequency vs. T_A

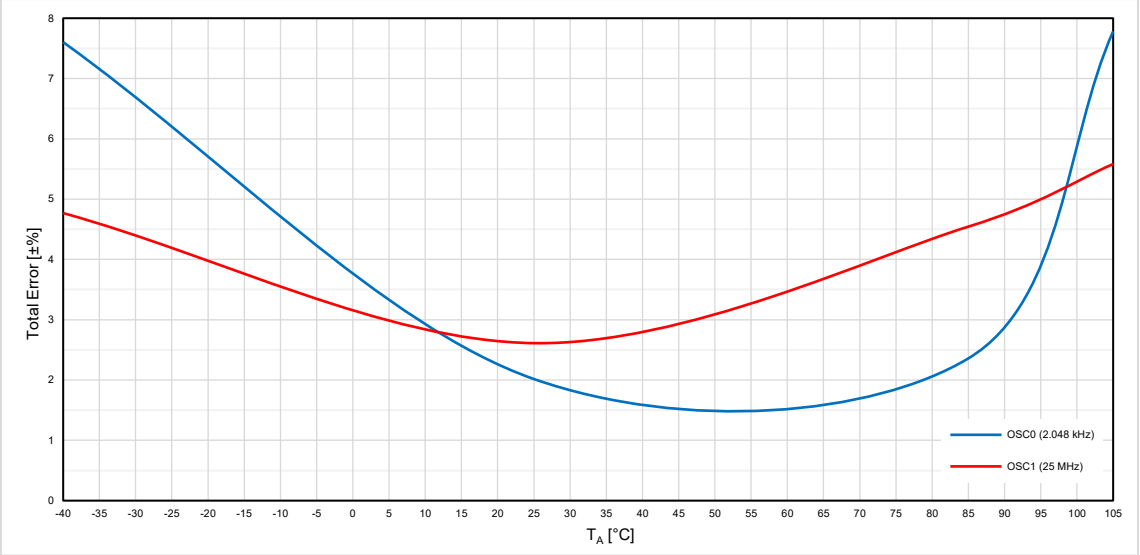


Figure 147. Oscillators Total Error vs. T_A at V_{DD} = 2.3 V to 5.5 V

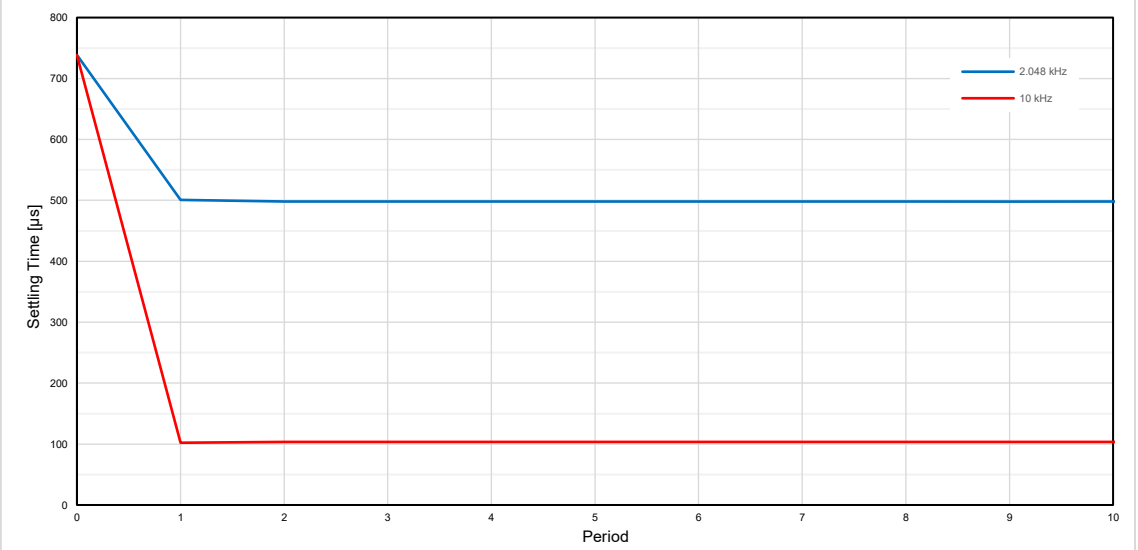


Figure 148. OSC0 (2.048 kHz, 10 kHz) Settling Time at V_{DD} = 3.3 V T_A = +25 °C

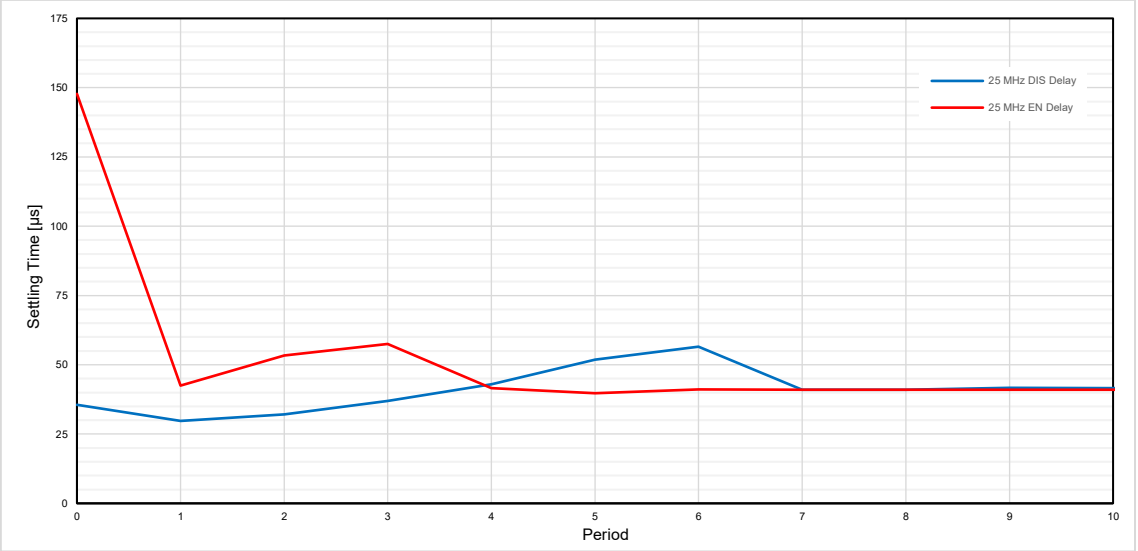


Figure 149. OSC1 (25 MHz) Settling Time at V_{DD} = 3.3 V T_A = +25 °C

17. Power-on Reset

The SLG47001-E/03-E has a Power-on Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and while the V_{DD} voltage is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

17.1 POR General Operation

The SLG47001-E/03-E is guaranteed to be powered down and non-operational when the V_{DD} voltage is lower than the power-off threshold (V_{TH_POFF}). While the device is in power-down state, all the input pins are in high-impedance state. In any case, the voltage applied to all the pins (except for SCL/GPIO4, SDA/GPIO5, and GPI0 pins) must not exceed the allowed maximum voltage (ABSMAX ratings) specified in section 3.1 Absolute Maximum Ratings. For example, if the V_{DD} voltage is 1.0 V during power-down, applying a voltage higher than 1.5 V to any other pin must be avoided because it may lead to unexpected behaviors or damage to the device.

To initiate the POR sequence, the V_{DD} voltage needs to exceed the power-on threshold (V_{TH_PON}) which is lower than the recommended operating voltage range for the V_{DD} and the V_{DDA} pins. This means that the POR sequence will start before the V_{DD} voltage reaches its operating voltage range. Once the POR sequence has initiated, the SLG47001-E/03-E will need a certain time to go through all the steps in the POR sequence.

While the POR sequence is taking place, all the pins are in Hi-Z state. At the last step in the POR sequence, the states of IO pins are released from Hi-Z. The pin configuration at this point of time is defined by the design programmed into the device. Once the POR sequence is complete, the device will be completely operational.

As a part of POR sequence, the SLG47001-E/03-E compares the CRC (Cyclic Redundancy Check) remainders between the calculated values and the NVM data which are programmed in production. If the calculated CRC remainders do not match with the CRC remainder register values, the SLG47001-E/03-E becomes inactive until the next power (V_{DD}) cycling.

To power down the device, the V_{DD} voltage needs to be pulled below the power-off threshold. For the power-off (V_{TH_POFF}) and the power-on threshold (V_{TH_PON}) thresholds in details, see section 3.4.1 Logic IO Specifications.

17.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 150.

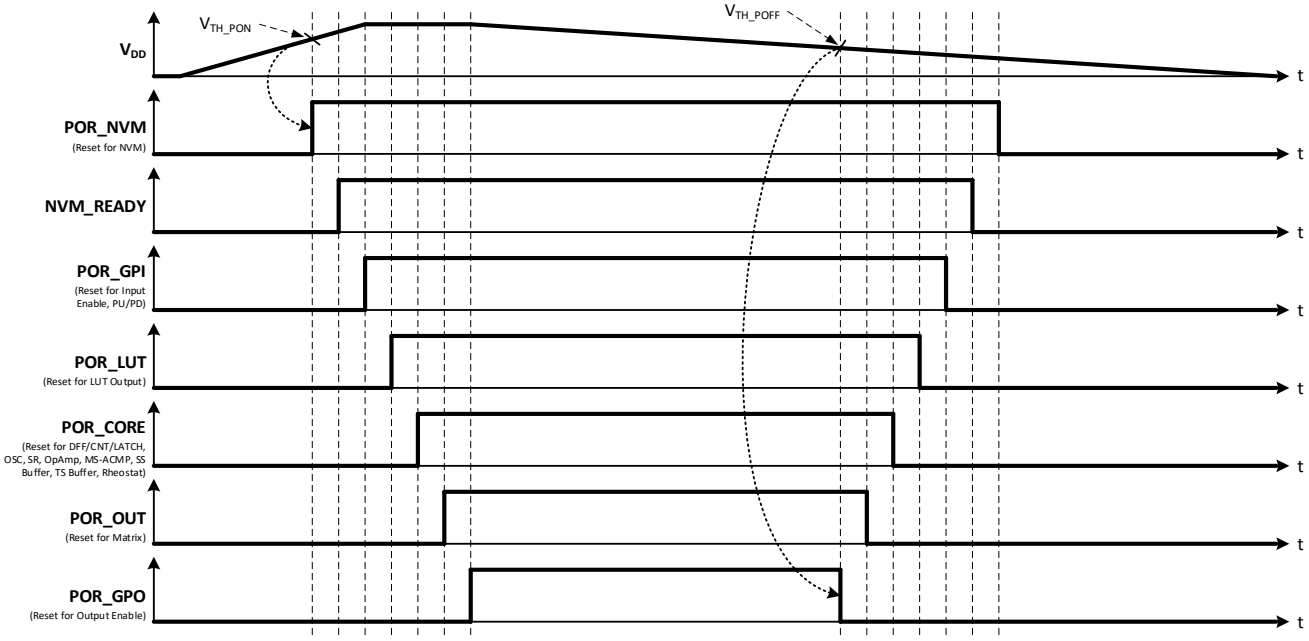


Figure 150. POR Power-Up and Power-Down Sequences

As shown in Figure 150, once the V_{DD} voltage exceeds the POR (Power-on Reset) threshold, the on-die NVM controller gets reset first. Next, the device reads the data from the NVM and transfers this information to CMOS latches that configure each macrocell and the connection matrix. At the third stage, the input pins get reset and enabled. At this moment, the resistances of digital rheostats are set to their default values. Then, the LUTs are reset and become active. After that, the delay cells, RC OSC, DFFs, and latches are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from low to high. At the last step of the device initialization, the output pins transition from high impedance state to active.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many operating conditions, such as: the V_{DD} voltage and its slew-rate, temperature, and process variations.

17.3 Macrocells Output States During POR Sequence

Figure 151 describes the output states of all macrocells in the SLG47001-E/03-E during the POR sequence.

Before the device has been reset, the outputs of all macrocells are set to logic-low, except for the output pins which are in Hi-Z state. Until the NVM is ready, the outputs of all macrocells are unpredictable, except for the output pins. At the next step, some macrocells start initialization:

- Output states of the input pins become low.
- Resistances of the digital rheostats are set to their default values.
- LUT outputs become low.

Only the programmable delay macrocell which is configured as an edge detector becomes active at this time. After that, input pins are enabled. Next, only LUTs are configured. Soon after all other macrocells are initialized. Once all macrocells are initialized, the internal POR matrix signal switches from low to high. At the last step, the output pins become active, and their output states are determined by the input signals.

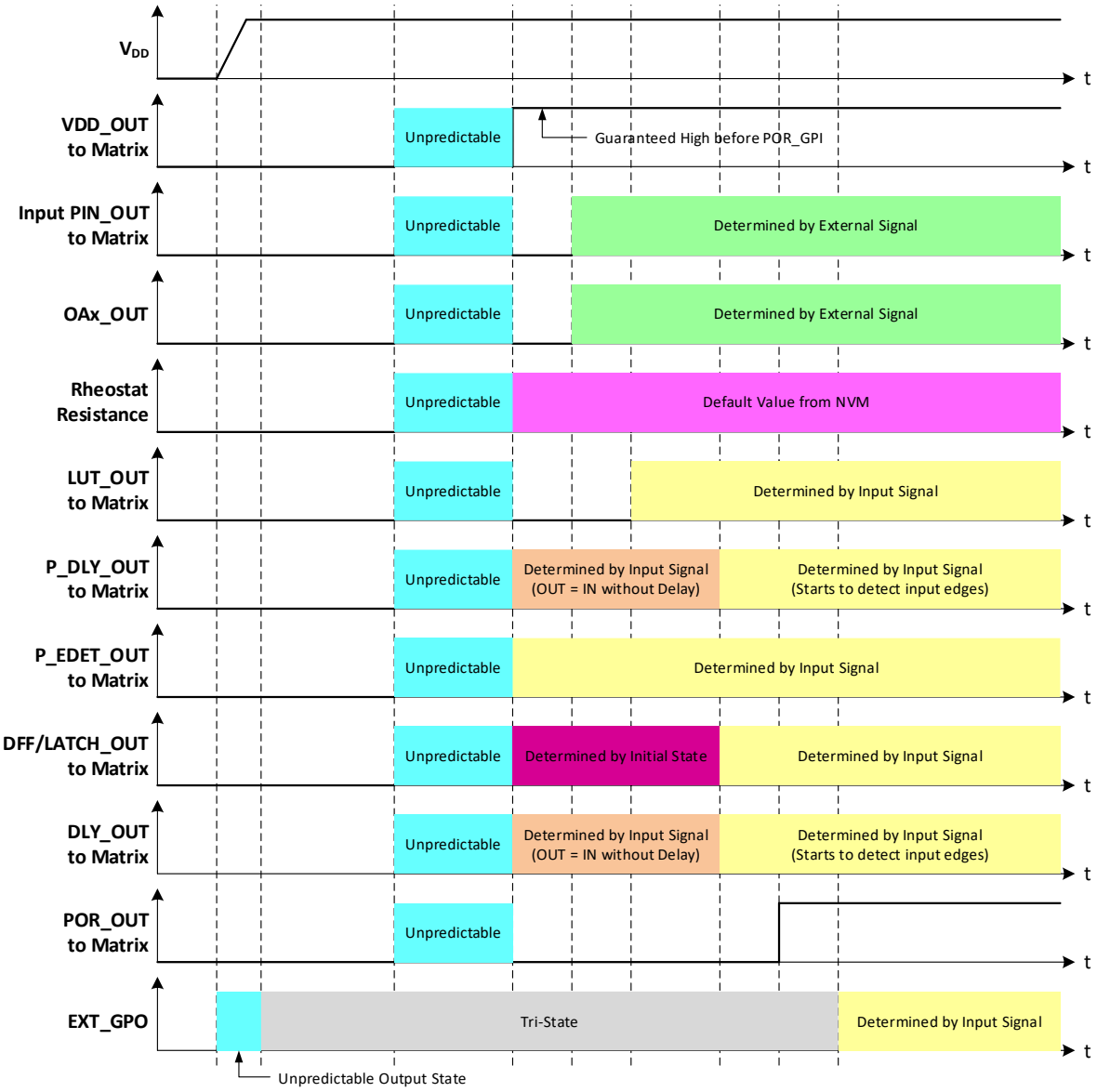


Figure 151. Macrocell States during POR Sequence

17.3.1 Initialization

All the macrocells have LOW-level of initial states by default. After the indicated power-up time from the condition that the V_{DD} voltage exceeds the power-on threshold (V_{TH_PON}), all macrocells in the SLG47001-E/03-E are powered on, while they are forced in reset state. At this stage, all outputs are in Hi-Z state and the device starts loading the initial data from the NVM. After that, the reset signal is released for the macrocells to start initializing according to the following sequence:

1. Input Pins, PU/PD Resistors, Operational Amplifiers, MS-ACMP, Digital Rheostats.
2. LUTs.
3. DFFs, Oscillators, Delays/Counters, Shift Registers.
4. Matrix.
5. Output Pins.

The low-to-high transition of the POR signal indicates that the power-up sequence is complete.

17.3.2 Power-Down

When the V_{DD} voltage drops below the power-off threshold (V_{TH_POFF}), the macrocells in the SLG47001-E/03-E are powered off during power-down sequency which is the opposite of POR sequence (see Figure 150). In case the V_{DD} voltage ramp-down is slow, the outputs can possibly switch states during power-down sequence.

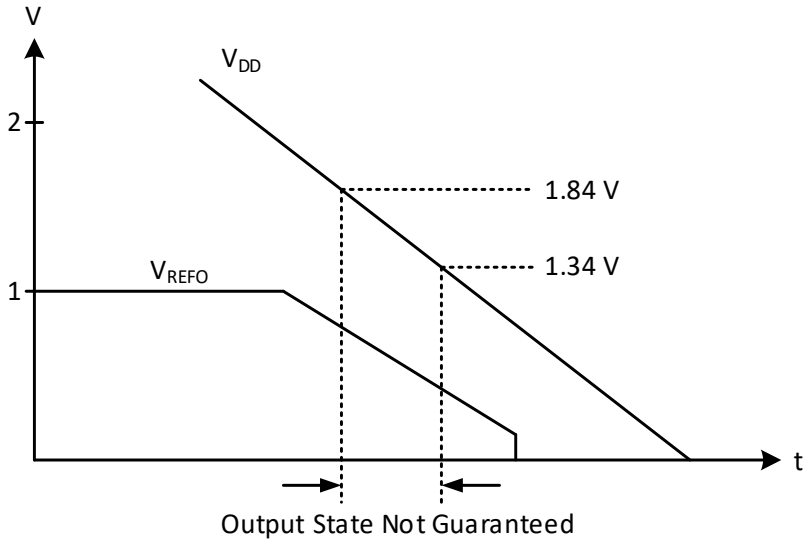


Figure 152. V_{REF} Output Voltage during Power-Down

18. I²C Serial Communications Macrocell

In the standard use-cases for GreenPAK devices, the configuration choices made by the user are stored as bit settings in the non-volatile memory (NVM). At startup, this information is transferred to the volatile RAM registers that configure the macrocells. Other RAM registers in the device are used for establishing connections within the connection matrix to route signals in the most appropriate manner for the application.

The I²C serial communications macrocell in this device allows an I²C controller (for example, a host processor) to read and write data directly from/to the RAM registers through a serial interface, allowing the re-configuration of macrocells, and changes to signal chains within the device. The I²C controller is also able to read and write other registers that are not associated with the NVM. For example, the input lines to the connection matrix can be read as digital register bits. These are the signal outputs of each macrocell in the device, giving the I²C controller the capability to read the current value of any macrocell.

The PROT_MODE_EN (Reg[1411]) and the PROT_MODE_SEL[2:0] (Reg[1415:1413]) registers allow the use to control the I²C read/write access protection mode. See section 18.4 Device Configuration Data Protection for more details.

Table 27. I²C Configuration Registers

Register Name	Access Type	Register Bit Description
I2C_SOFT_RST	RW	I²C Reset Bit with Reloading NVM to Data Register (Soft Reset) 0: Keep Existing Condition 1: Reset Execution
I2C_WRITE_LATCH	RW	IO Latching during I²C Write 0: Disable 1: Enable
PROT_MODE_EN	RW	Register Protect Mode Enable Control 0: Disable 1: Enable
PROT_MODE_SEL[2:0]	RW	Register Protection Mode Selection 000b: All Read/Write Unlocked (Mode 0) 001b: Read Partially Locked (Mode 1) 010b: Read2 Partially Locked (Mode 2) 011b: Read2/Write Partially Locked (Mode 3) 100b: All Read Locked (Mode 4) 101b: All Write Locked (Mode 5) 110b: All Read/Write Locked (Mode 6) 111b: N/A
I2C_WRITE_MASK[7:0]	RW	I²C Write Mask Setting 0: Overwrite 1: Mask
I2C_SLA[3:0]	RW	I²C Target Address Setting
I2C_SLA0_SEL	RW	I²C Target Address Bit0 Selection 0: From Reg[1464] 1: From GPI0
I2C_SLA1_SEL	RW	I²C Target Address Bit1 Selection 0: From Reg[1465] 1: From GPIO2

18.1 I²C Serial Communications Device Addressing

Each command to the I²C serial communications macrocell begins with a 'START' condition. The basic command structure of the I²C protocol is shown in Figure 153. After the 'START' condition (S), the I²C controller (master) sends 7-bit target (slave) address followed by the R/W bit. The SLG47001-E/03-E allows multiple target addresses by programming the first four bits ('Control Code') of the 7-bit target address. Each bit in the 'Control Code' can be sourced independently from the I2C_SLA[3:0] (Reg[1467:1464]) register. When the I2C_SLA0_SEL (Reg[1468]) and the I2C_SLA1_SEL (Reg[1469]) registers are set to '1', Bit0 and Bit1 of the 'Control Code' are defined by the logic levels of GPI0 and GPIO2 pins respectively. This gives flexibility in addressing with multiple devices on the same I²C bus. The R/W bit selects whether a read (R/W = 1) or a write (R/W = 0) command is requested. The R/W bit will be followed by an 'Acknowledge' bit (ACK), which is sent by the target device to indicate successful communication of the first byte of data.

In the I²C-bus specification and the user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for special functions, such as 'General Call Address'. If the user decides to set the 'Control Code' to either '1111b' or '0000b' in a system with other target devices, consult the I²C-bus specification and the user manual to understand the addressing and implementation of these special functions.

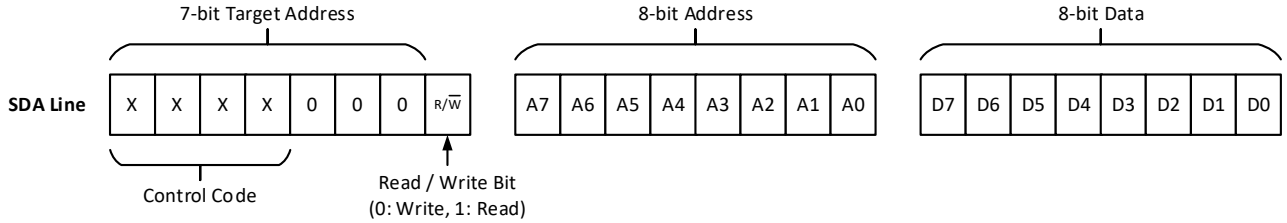


Figure 153. I²C Basic Command Structure

18.2 I²C Serial General Timing

The general timing characteristics for the I²C serial communications macrocell are shown in Figure 154 and the timing specifications can be found in section 3.4.2 I2C Specifications.

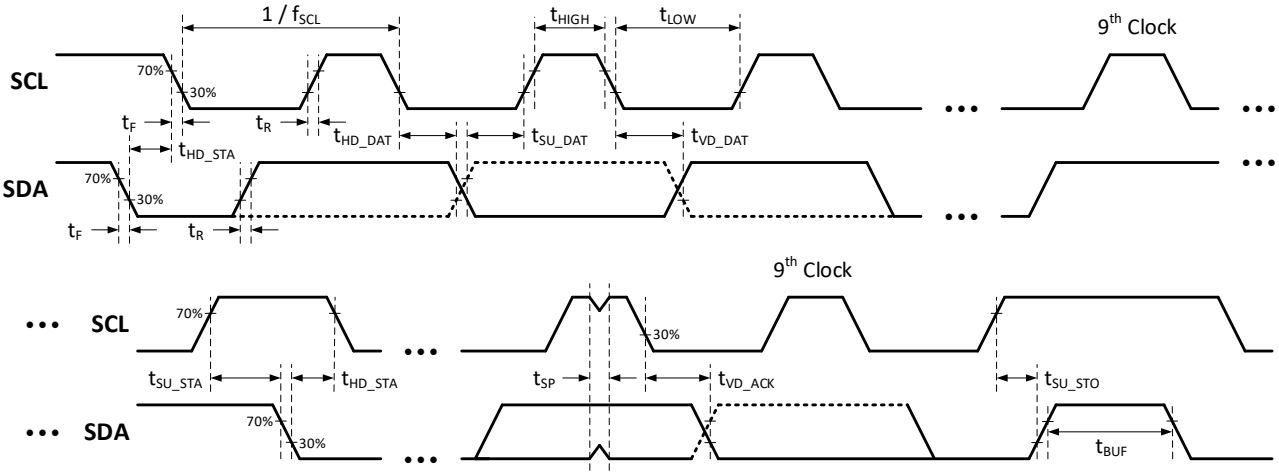


Figure 154. I²C General Timing Characteristics

18.3 I²C Serial Communications Commands

18.3.1 Byte Write Command

Following a 'START' condition from the I²C controller, the 7-bit target address and the R/W bit (set to '0' for write command) are placed onto the I²C bus by the I²C controller. After the SLG47001-E/03-E sends an 'Acknowledge' bit (ACK), the I²C controller transmits the 'Word Address' (A7 through A0). After the I²C controller receives another 'ACK' bit from the SLG47001-E/03-E, it will transmit the 'Data' byte to be written into the

addressed memory location. The SLG47001-E/03-E provides an 'ACK' bit again, and then the I²C controller generates a 'STOP' condition. The internal write cycle for the data will take place at the time that the SLG47001-E/03-E generates the 'ACK' bit.

It is possible to latch all IOs during I²C write command by setting the I2C_WRITE_LATCH bit (Reg[1409]) to '1'. When the I²C write latch is enabled, the IOs will remain in their states until the write command is completed.

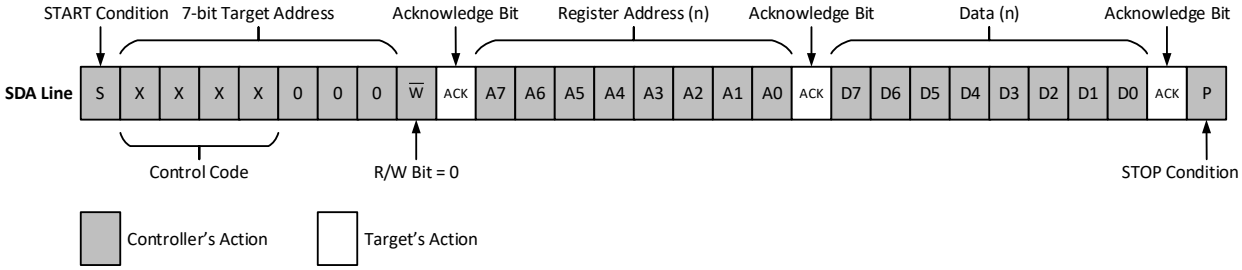


Figure 155. Byte Write Command (R/W = 0)

18.3.2 Sequential Write Command

The 'Sequential Write Command' is the same as the 'Byte Write Command' until the first byte of data is transmitted. After that, the I²C controller continues to transmit data bytes to the SLG47001-E/03-E instead of generating a 'STOP' condition. Each subsequent data byte will increment the internal address pointer and will be written into the next higher byte in the command addressing. The internal write cycle will take place at the time that the SLG47001-E/03-E generates the 'ACK' bit. Same as the 'Byte Write Command'.

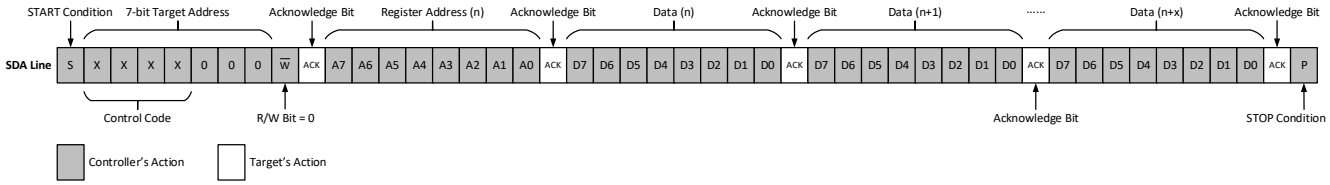


Figure 156. Sequential Write Command

18.3.3 Current Address Read Command

The 'Current Address Read Command' allows the I²C controller to read the data from the register that the current address pointer indicates. The address pointer is incremented at the 9th clock of the previous command. For example, if a 'Sequential Read Command' reads data up to address 'n', the address pointer gets increased to 'n+1' at the 9th clock right before the 'STOP' condition. Subsequently, the 'Current Address Read Command' that follows the 'Sequential Read Command' will start reading data at 'n+1'. The 'Current Address Read Command' contains the 7-bit target address sent by the I²C controller, with the R/W bit = '1'. The SLG47001-E/03-E will issue an 'ACK' bit and then transmit eight data bits for the requested byte. The I²C controller will not issue an 'ACK' bit and follow immediately with a 'STOP' condition.

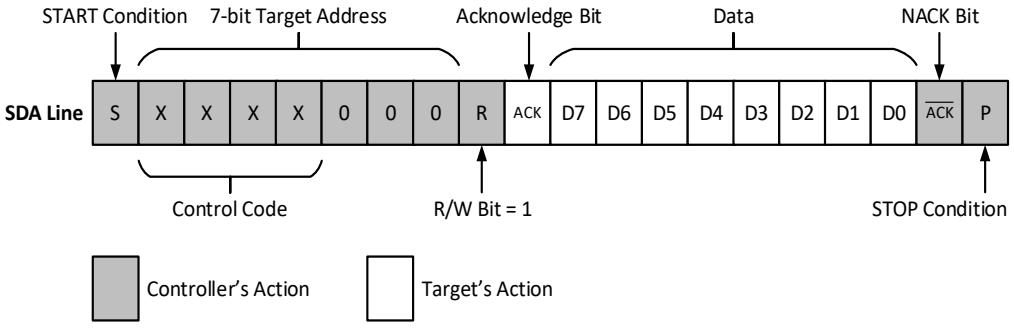


Figure 157. Current Address Read Command (R/W = 1)

18.3.4 Random Read Command

The ‘Random Read Command’ starts with a ‘START’ condition followed by the 7-bit target address and R/W = 0 (indicating a write command). After the SLG47001-E/03-E generates an ‘ACK’ bit, the I²C controller sends ‘Word Address’ to set the internal address pointer. After another ‘ACK’ bit from the SLG47001-E/03-E, the I²C controller generates a ‘Repeated START’ (Sr) condition without ‘STOP’ condition, that keeps the internal address pointer unchanged, in preparation for the next command. After initiating the ‘Repeated START’ condition, the I²C controller sends the same 7-bit target address with the R/W bit set to ‘1’. After the SLG47001-E/03-E issues an ‘ACK’ bit, it transmits the data byte from the register indicated by the internal address pointer. When the transmission of the data is completed, the I²C controller issues a ‘Not Acknowledge’ (NACK) bit before generating a ‘STOP’ condition.

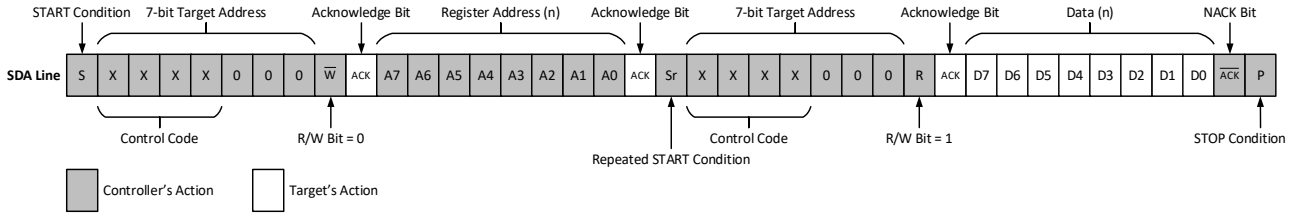


Figure 158. Random Read Command

18.3.5 Sequential Read Command

The ‘Sequential Read Command’ is initiated in the same way as the ‘Random Read Command’, except that the I²C controller issues an ‘ACK’ bit once the SLG47001-E/03-E transmits the first data byte. The controller can continue reading sequential bytes of data and terminate the sequential reading with a ‘NACK’ bit followed by a ‘STOP’ condition.

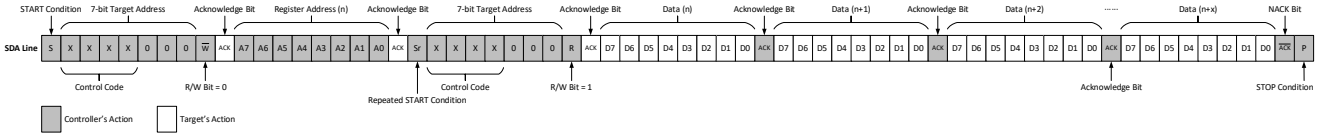


Figure 159. Sequential Read Command

18.3.6 I²C Serial Reset Command

It is possible for the I²C controller to reset the device to the initial power-up conditions, including configuration of all macrocells, and all interconnects by the connection matrix. This is initiated by setting the I2C_SOFT_RST bit (Reg[1408]) to ‘1’, which causes the device to re-enable the Power-on Reset (POR) sequence, including the reloading of all register data from the NVM. During the POR sequence, the outputs of the device will be in tri-state (Hi-Z). After the reset has taken place, the I2C_SOFT_RST bit will be set to ‘0’ automatically. Figure 160 illustrates the sequence of events for this reset function.

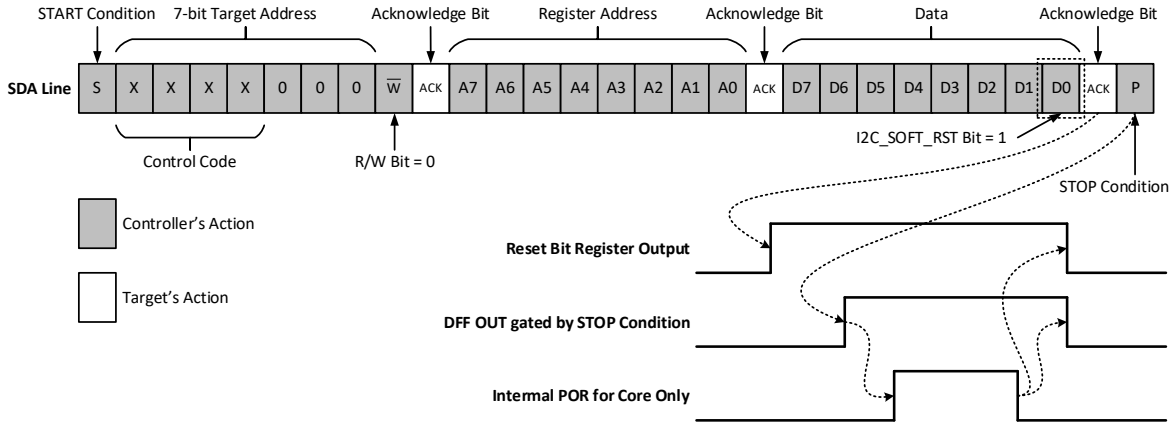


Figure 160. Reset Command Timing

18.3.7 I²C Additional Options

When the IO latching during I²C writing feature is enabled (I2C_WRITE_LATCH = 1), the output values of all pins are latched until I²C writing is done. This feature protects the output states from being changed due to configuration process during I²C write in case multiple register bytes are updated. The inputs and the macrocells retain their status during I²C writing. If the SCL/GPIO4 and the SDA/GPIO5 pins are configured for other functions, all access through I²C will be disabled.

Note that any write commands that come to the device through I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

18.3.8 I²C Byte Write Bit Masking

The I²C macrocell inside the SLG47001-E/03-E supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user needs to configure the I2C_WRITE_MASK[7:0] register (ADDR 0xB1) with the desired bit mask pattern by a 'Byte Write' command (see section 18.3.1 Byte Write Command for details). This sets a bit mask pattern for the target memory location that will take effect on the next 'Byte Write' command to this register byte. If the mask bit is set to '1', the corresponding bit in the target register will not change. If the mask bit is set to '0', the corresponding bit in the target register will be changed to the new value. After a valid 'Byte Write' command, the I2C_WRITE_MASK[7:0] register will be reset (set to 0x00). In case the next command received by the device is not a 'Byte Write' command, the bit masking function will be aborted and the I2C_WRITE_MASK[7:0] register will be reset with no effect. Figure 161 shows an example of this function.

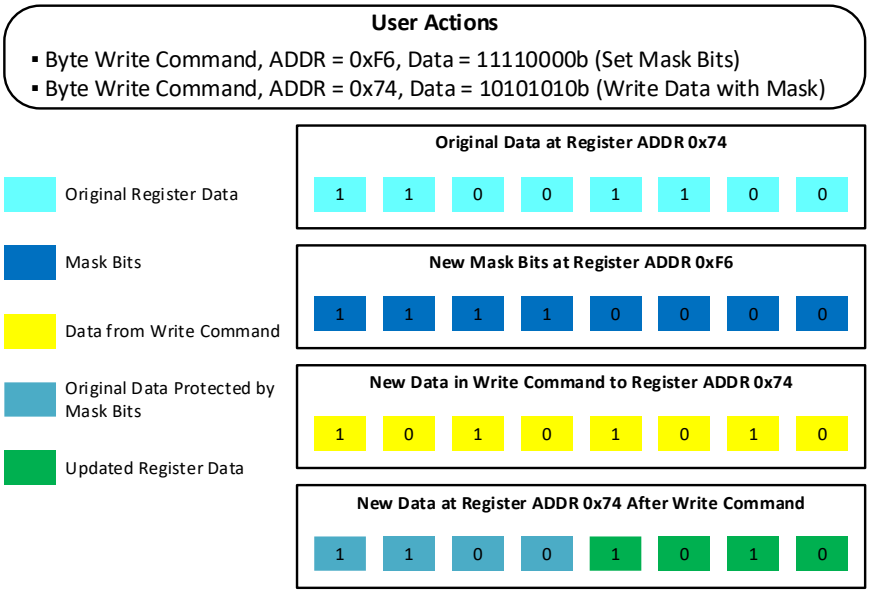


Figure 161. Example of I²C Byte Write Bit Masking

18.4 Device Configuration Data Protection

The SLG47001-E/03-E has a protection feature that allows a part or the entire memory to be protected from being read and/or written. To enable the protection scheme, the PROT_MODE_EN bit needs to be set to '1'. The protection options are defined by the PROT_MODE_SEL[2:0] registers. The user can select one of the seven schemes below (see Table 28 for details):

- 000b: All Read/Write Unlocked (Mode 0)
- 001b: Read Partially Locked (Mode 1)
- 010b: Read Partially Locked (Mode 2)

- 011b: Read/Write Partially Locked (Mode 3)
- 100b: All Read Locked (Mode 4)
- 101b: All Write Locked (Mode 5)
- 110b: All Read/Write Locked (Mode 6).

Table 28. Read/Write Protection Options

Configurations	Protection Modes							Register Address
	All Read/Write Unlocked (Mode 0)	Read Partially Locked (Mode 1)	Read Partially Locked (Mode 2)	Read/Write Partially Locked (Mode 3)	All Read Locked (Mode 4)	All Write Locked (Mode 5)	All Read/Write Locked (Mode 6)	
Macrocells Inputs Configuration (Connection Matrix Outputs)	RW	WO	WO	-	WO	RO	-	0x00 – 0x3B
Macrocells Output Values (Connection Matrix Inputs)	RO	RO	RO	RO	-	RO	-	0x3C, 0x3D, 0x3E Bit5-0, 0x40 – 0x43
Connection Matrix Virtual Inputs (Shared with GPIs and EPG OUTs)	RW	RW	RW	RW	RW	RW	RW	0x3E Bit7-6, 0x3F
Configuration Bits for All Macrocells (MS-ACMP, EPG, OSC, IO, Multi-Function and Combination Function, Prog. Delay, ASW, OpAmp, and others)	RW	RW	WO	-	WO	RO	-	0x44 - 0xA2, 0xBA, 0xBB
Rheostat Counter Input (D)	RW	RW	RW	RW	WO	RO	-	0x91 – 0x94
Rheostat Tolerance Data	RO	RO	RO	RO	RO	RO	RO	0x95 – 0x98
Rheostat Counter Output (Q)	RO	RO	RO	RO	RO	RO	RO	0x9A – 0x9D
V_{REF} Error Data	RO	RO	RO	RO	RO	RO	RO	0xA4
I^2C Soft Reset Bit	RW	RW	RW	RW	RW	RO	RO	0xB0 Bit0
Output Latching during I^2C Write	RW	RW	RW	RW	RW	RO	RO	0xB0 Bit1
Protection Mode Enable	RO	RO	RO	RO	RO	RO	RO	0xB0 Bit3
Protection Mode Selection	RW	RO	RO	RO	RO	RO	RO	0xB0 Bit7-5
I^2C Byte Write Masking Bit	RW	RW	RW	RW	WO	RO	-	0xB1
Pin Target Address Select	RO	RO	RO	RO	RO	RO	RO	0xB4, 0xB2
I^2C Control Code	RO	RO	RO	RO	RO	RO	RO	0xB6
I^2C Disable/Enable	RO	RO	RO	RO	RO	RO	RO	0xB7 Bit3-0
Programming Disable	RO	RO	RO	RO	RO	RO	RO	0xB7 Bit5-4
Code Compare Enable	RO	RO	RO	RO	RO	RO	RO	0xB8 Bit0

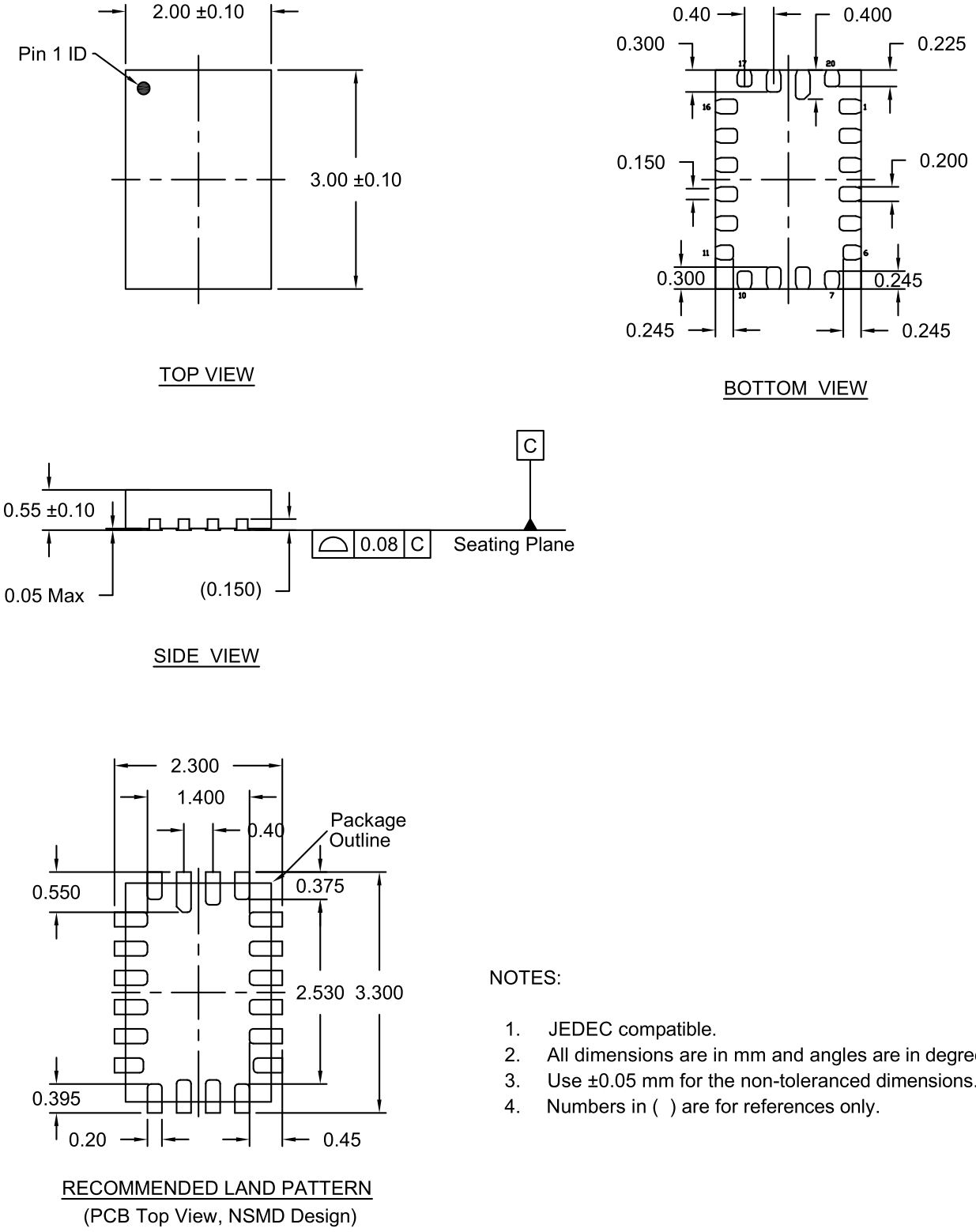
RW	Allow Read and Write Data
WO	Allow Write Data Only
RO	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as the current values of the counters, the connection matrix, and the connection matrix virtual inputs. The I^2C write will not have any impact on the data if they come from macrocell outputs, except the connection matrix virtual inputs. The silicon identification service bits allow for identifying silicon family, its revision, and others.

19. Package Information

19.1 Package Outline Drawings

19.1.1 STQFN-20 (2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) FCD

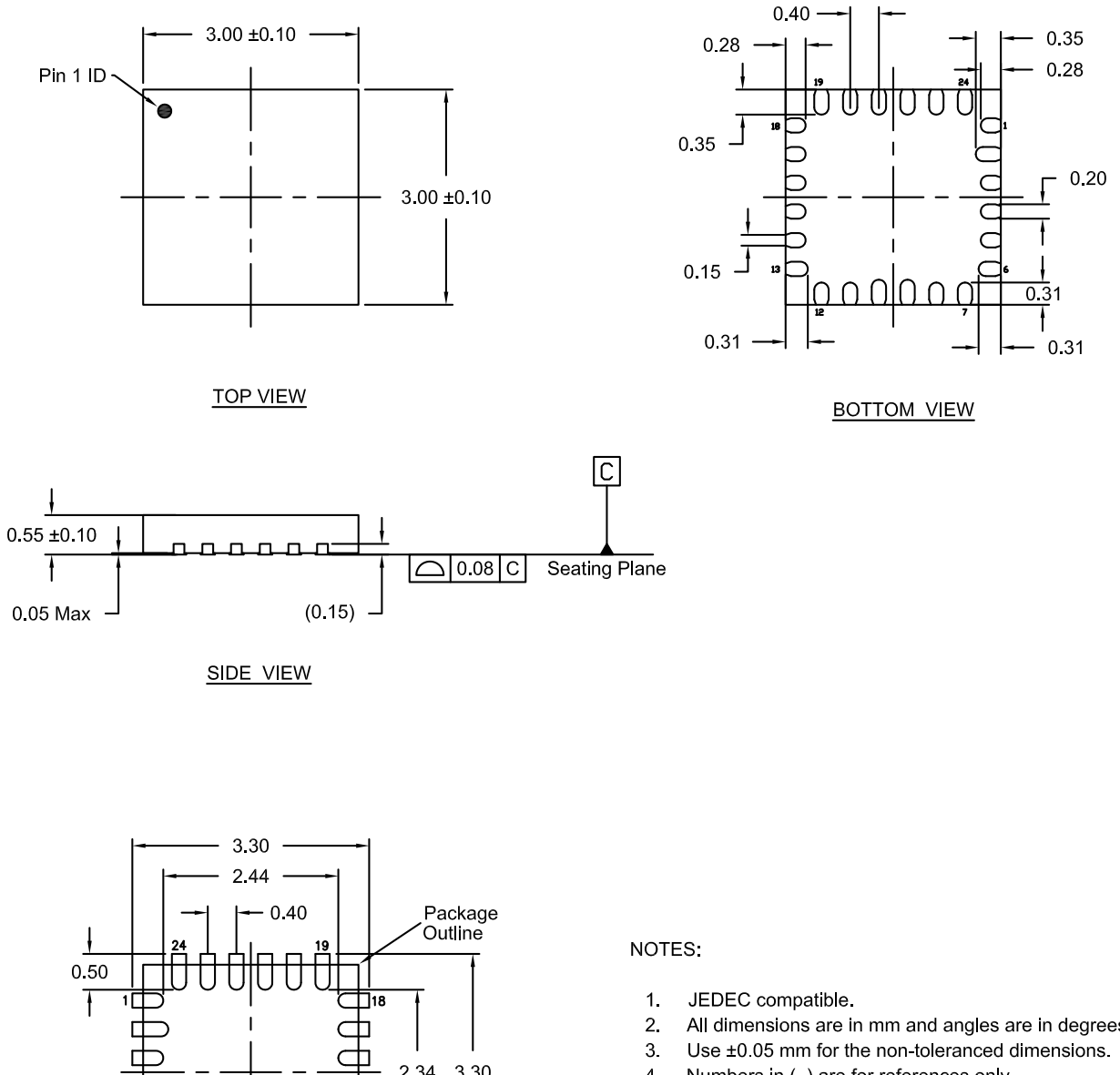


NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Figure 162. STQFN-20 Package Outline Drawing

19.1.2 STQFN-24 (3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) WB



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Figure 163. STQFN-24 Package Outline Drawing

19.2 Package Top Marking

19.2.1 STQFN-20 (2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) FCD

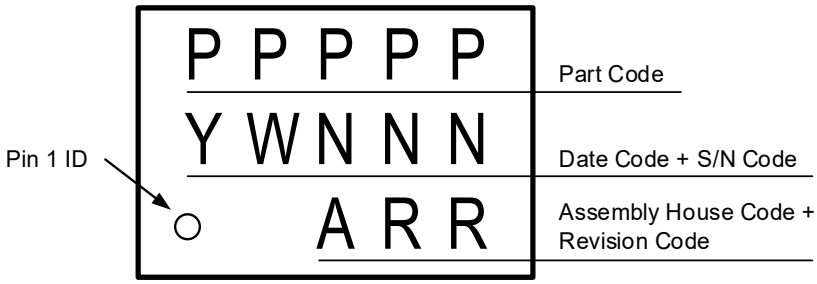


Figure 164. STQFN-20 Package Top Marking

19.2.2 STQFN-24 (3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) WB

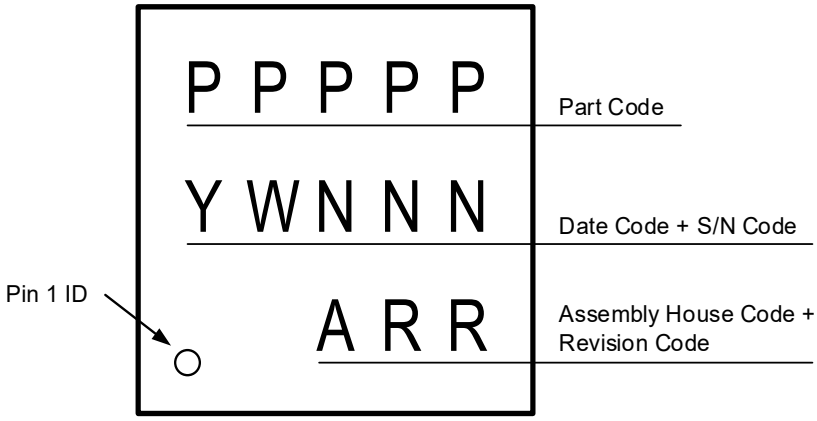


Figure 165. STQFN-24 Package Top Marking

19.3 Junction-to-Ambient Thermal Resistance (θ_{JA})

Table 29. Junction-to-Ambient Thermal Resistance

Package Option	Thermal Resistance (θ_{JA})
STQFN-20 (SLG47001-E)	45.8 °C/W
STQFN-24 (SLG47003-E)	79.7 °C/W

19.4 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 30.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The STQFN-24 and STQFN-20 packages are qualified for MSL 1.

Table 30. MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 Hours	30 °C/60 % RH
MSL 3	168 Hours	30 °C/60 % RH
MSL 2A	4 Weeks	30 °C/60 % RH
MSL 2	1 Year	30 °C/60 % RH
MSL 1	Unlimited	30 °C/85 % RH

19.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

20. PCB Layout Guidelines

The SLG47001-E/03-E has two supply input pins (V_{DD} and V_{DDA}) and one ground pin (GND) as analog and digital ground signals are internally connected. Separating the analog supply voltage (V_{DDA}) from the digital supply (V_{DD}) helps to minimize cross-coupling of noise generated by the digital part of the device.

- **Analog (V_{DDA}) Domain**: Operational Amplifiers, V_{REF} of OpAmp, digital rheostats, and low-power bandgap.
- **Digital (V_{DD}) Domain**: MS-ACMP (Chopper ACMP), V_{REF} of MS-ACMP, TS_OUT buffer, sink/source buffer, analog switch, OSC0 (2 kHz/10 kHz), OSC1 (25 MHz), I^2C macrocell, the NVM logic, multi-function macrocells, and combination-function macrocells.

It is strongly recommended to connect unused digital input pins to GND.

The following suggestions allow to minimize the impacts of the digital domain noise onto the analog domain:

- Decrease the slew-rate of digital input signals if possible.
- Use proper grounding scheme with bypass capacitors on V_{DDA} and V_{DD} pins.
- Assign GPIO0 – GPIO9 for digital signals first, then use other pins in case more digital IOs are needed.

20.1 STQFN-20 (2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) FC Package

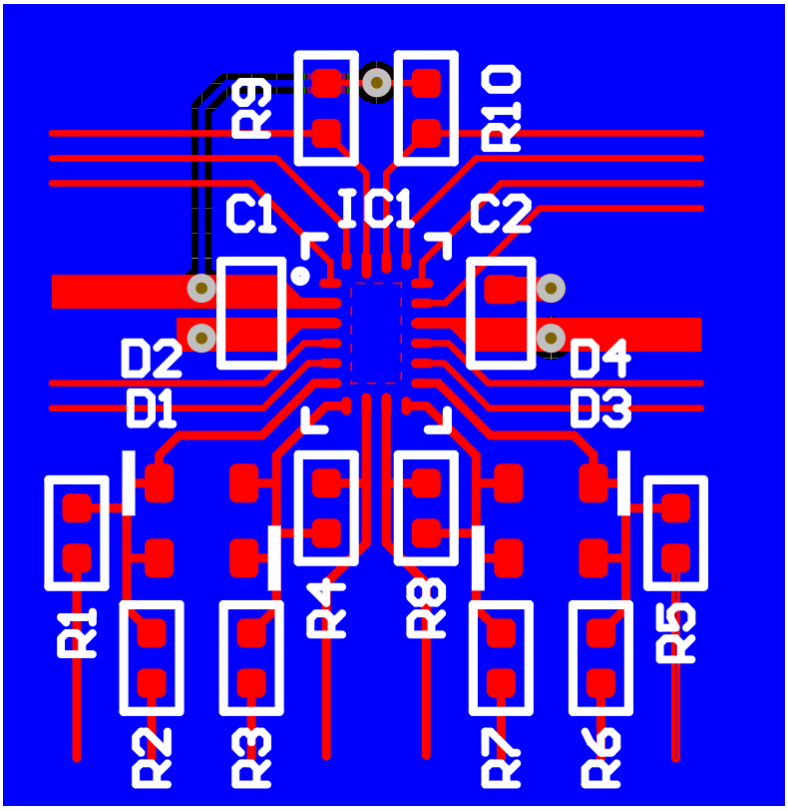


Figure 166. STQFN-20 PCB Layout Example

Note that D1 through D4 (differential input voltage limiting diodes) are optional.

20.2 STQFN-24 (3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) WB Package

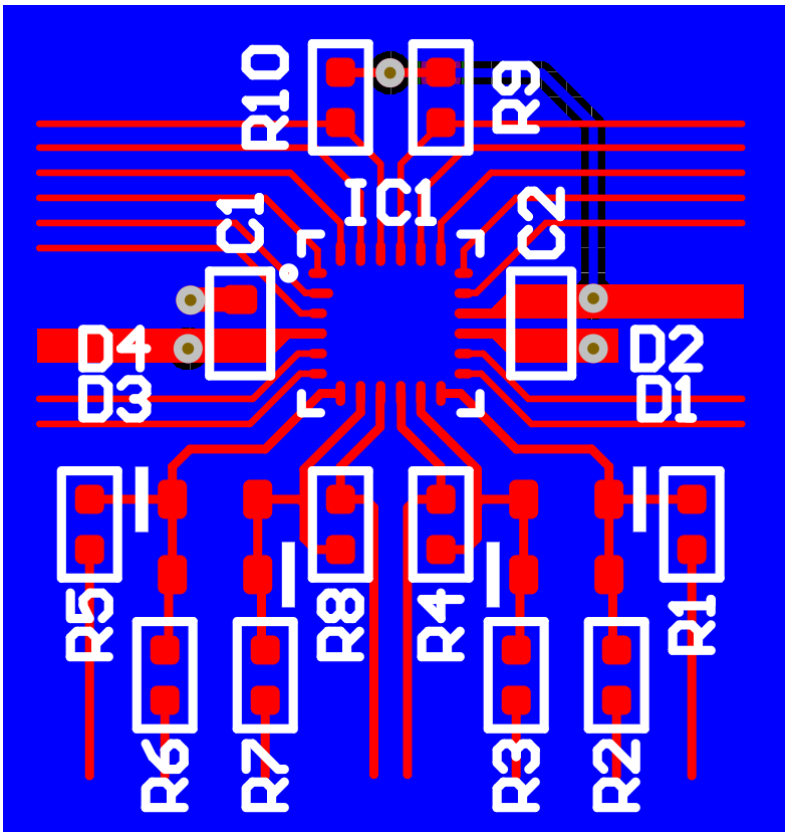


Figure 167. STQFN-24 PCB Layout Example

Note that D1 through D4 (differential input voltage limiting diodes) are optional.

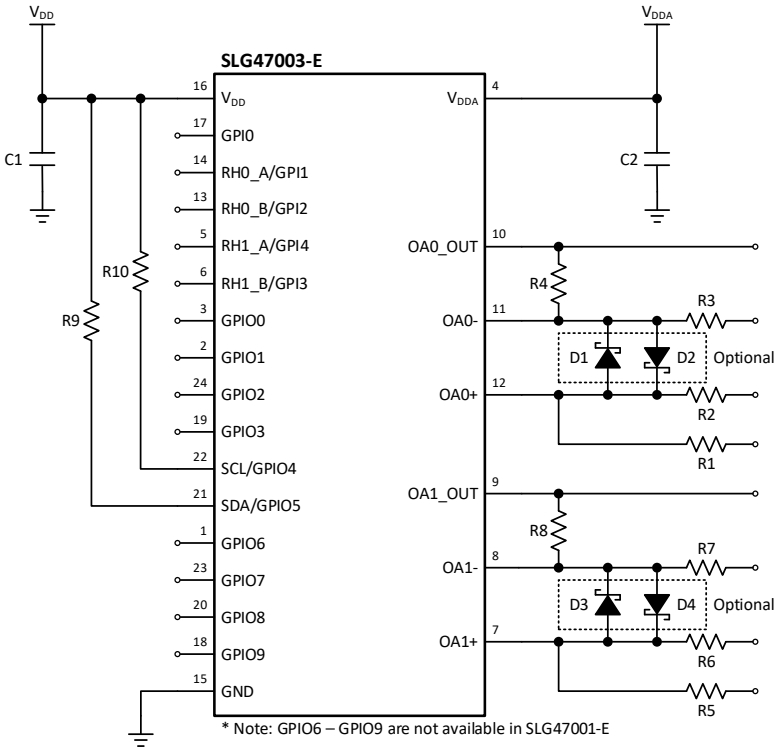


Figure 168. STQFN-24 PCB Layout Example Schematic

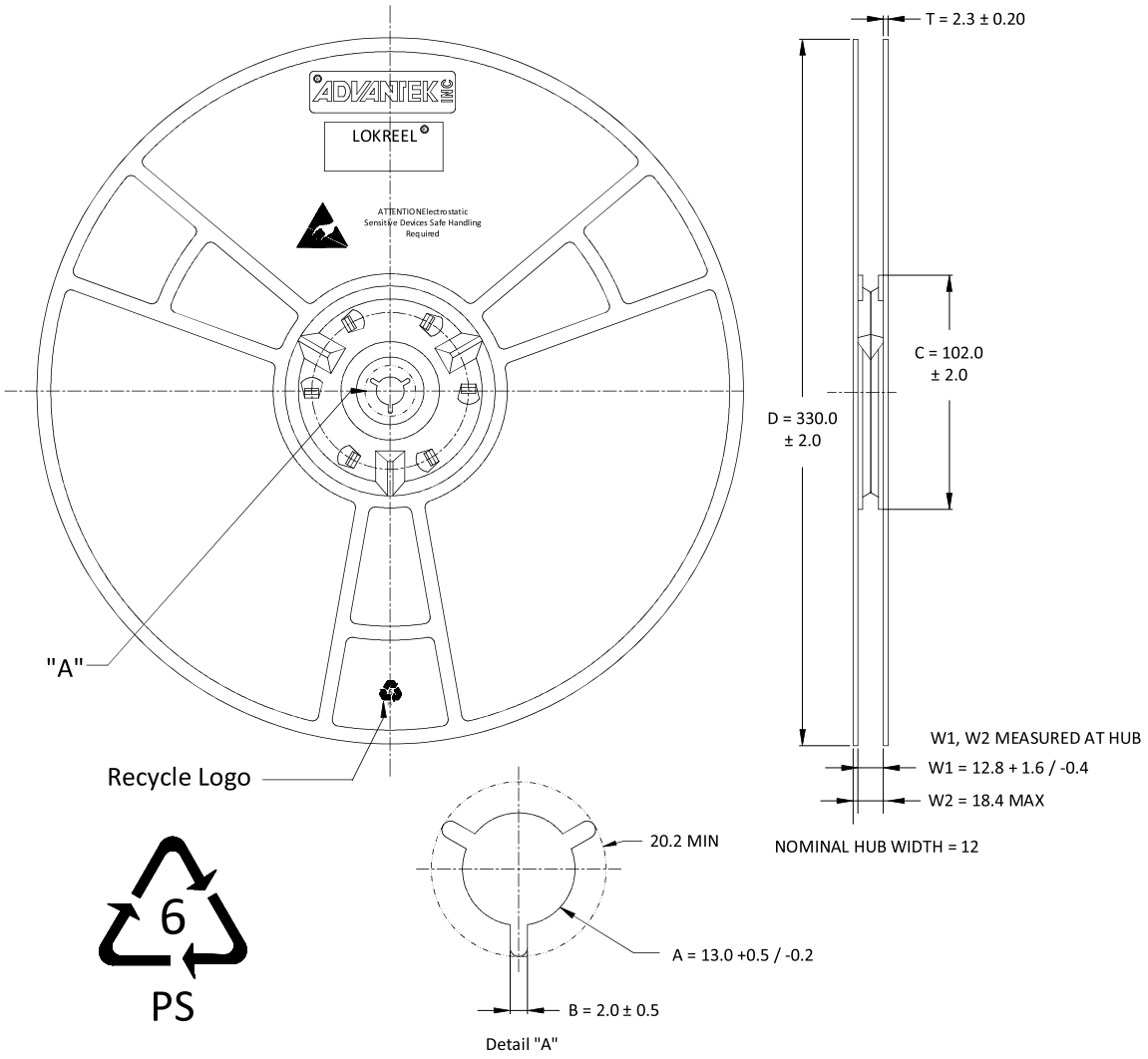
21. Ordering Information

Orderable Part Number	Package Description	Carrier Type	Temperature Range
SLG47001-EV	STQFN-20, 2 mm x 3 mm	Tape and Reel	-40 °C to +105 °C
SLG47003-EV	STQFN-24, 3 mm x 3 mm	Tape and Reel	

The ordering number consists of the part number followed by a suffix indicating the packing options. For details and availability, please consult Renesas Electronics Corporation customer support portal or your local sales representative.

21.1 Tape and Reel Specifications

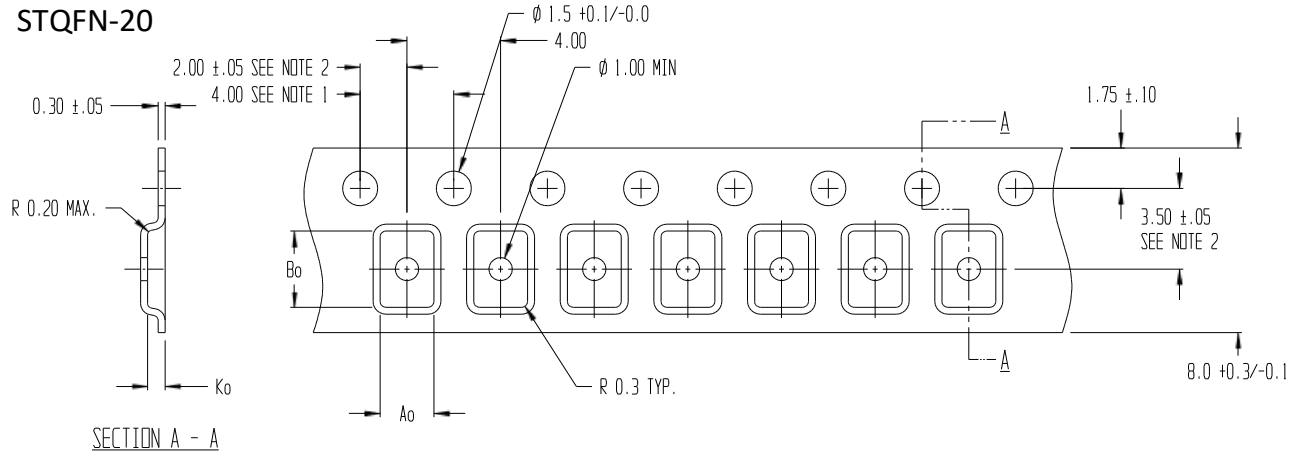
Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader [min]		Trailer [min]		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN-20	20	2.0 x 3.0 x 0.55	3,000	3,000	178/60	100	400	100	400	8.0	4.0
STQFN-24	24	3.0 x 3.0 x 0.55	5,000	5,000	330/102	42	336	42	336	12.0	8.0



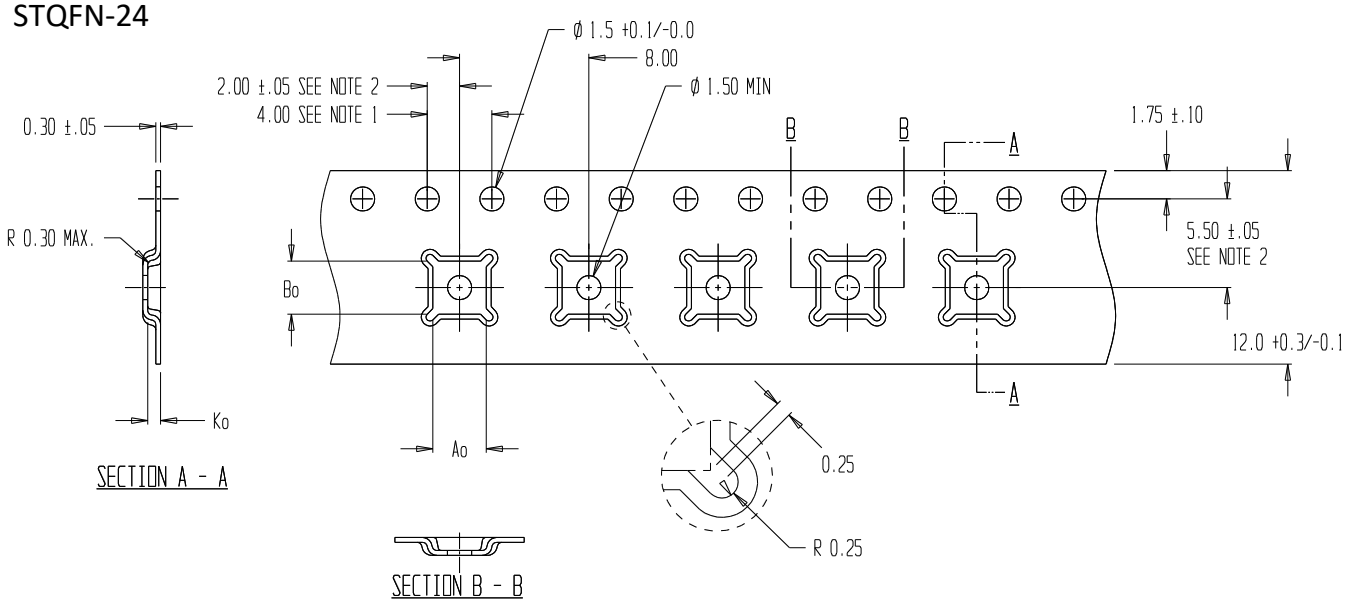
21.2 Carrier Tape Drawing and Dimensions

Package Type	PocketB™ Length [mm]	PocketB™ Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN-20	2.2 ± 0.1	3.2 ± 0.1	0.92 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	1.55 ± 0.05	1.75 ± 0.1	3.5 ± 0.05	8.0 +0.3 / -0.05
STQFN-24	3.3 ± 0.1	3.3 ± 0.1	0.75 ± 0.05	4.0 ± 0.1	4.0 ± 0.1	1.5 +0.1 / -0.0	1.75 ± 0.1	5.5 ± 0.05	12.15 ± 0.1

STQFN-20



STQFN-24



Glossary

A

ACK	Acknowledge Bit
ACMP	Analog Comparator
ASW	Analog Switch

B

BG	Bandgap

C

CF	Combination Function
CLK	Clock
CMI	Connection Matrix Input
CMO	Connection Matrix Output
CNT	Counter

D

DFF	D Flip-flop
DLY	Delay

E

EN	Enable
EPG	Extended Pattern Generator
ESD	Electro-static Discharge
EXT	External

F

Fm+	Fast-mode Plus
FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LP_BG	Low-power Bandgap
LPF	Low-pass Filter
LSB	Least Significant Bit
LUT	Look-up Table

M

MF	Multi-Function
MSB	Most Significant Bit
MUX	Multiplexer

N

nRST	Reset Signal (Active Low)
nSET	Set Signal (Active Low)
NVM	Non-volatile Memory

O

OA/OpAmp	Operational Amplifier
OCP	Over-current Protection
OD	Open-drain
OE	Output Enable
OSC	Oscillator
OTP	One-time Programmable
OUT	Output
OVF	Overflow

P

PD	Power-down
P_DLY	Programmable Delay
P_EDET	Programmable Edge Detector
POR	Power-on Reset
PP	Push-Pull
PU	Pull-Up
PWR	Power

R

RO	Read-only
RST	Reset
RW	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address (Target Address)
SMT	Schmitt Trigger
SR	Shift Register

T

TH	Threshold
TSD	Thermal Shutdown
TS	Temperature Sensor

U

UVLO	Under-voltage Lockout

V

V_{REF}	Voltage Reference

W

WO	Write-only
WOSMT	Without Schmitt Trigger

Revision History

Revision	Date	Description
1.02	Jul 22, 2025	Updated part numbering format. Fixed a typo in document number revision.
1.01	Jun 24, 2025	Fixed a typo (.gpx → *.aap) in section 1.2. Fixed typos (ms → µs) in Figure 84 – Figure 87. Redrew Figure 119 – Figure 123 with correct data. Fixed typos (2.4 V → 2.3 V) in legends of Figure 124. Fixed a typo (µs → ns) in Figure 144. Fixed typos (2.5 V → 2.3 V) in legends of Figure 145 and Figure 146. Updated Figure 153 and Figure 155 – Figure 160 with controller's and target's actions.
1.00	Apr 28, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
SLG47001-EV	20	STQFN	QU0020AA/PSC-5003-01
SLG47003-EV	24	STQFN	QU0024AA/PSC-5001-01

A.2 Symbol Pin Information

A.2.1 20-STQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	GPI0	Input	-
2	V_{DD}	Power	-
3	GND	Power	-
4	RH0_A	I/O	GPI1
5	RH0_B	I/O	GPI2
6	OA0+	Input	-
7	OA0-	Input	-
8	OA0_OUT	Output	-
9	OA1_OUT	Output	-
10	OA1-	Input	-
11	OA1+	Input	-
12	RH1_B	I/O	GPI3
13	RH1_A	I/O	GPI4
14	V_{DDA}	Power	-
15	GPIO0	I/O	-
16	GPIO1	I/O	-
17	GPIO2	I/O	-
18	SCL	Input	GPIO4
19	SDA	I/O	GPIO5
20	GPIO3	I/O	-

A.2.2 24-STQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	GPIO6	I/O	-
2	GPIO1	I/O	-
3	GPIO0	I/O	-
4	V_{DDA}	Power	-
5	RH1_A	I/O	GPI4
6	RH1_B	I/O	GPI3
7	OA1+	Input	-
8	OA1-	Input	-
9	OA1_OUT	Output	-
10	OA0_OUT	Output	-
11	OA0-	Input	-
12	OA0+	Input	-
13	RH0_B	I/O	GPI2
14	RH0_A	I/O	GPI1
15	GND	Power	-
16	V_{DD}	Power	-
17	GPI0	Input	-
18	GPIO9	I/O	-
19	GPIO3	I/O	-
20	GPIO8	I/O	-
21	SDA	I/O	GPIO5
22	SCL	Input	GPIO4
23	GPIO7	I/O	-
24	GPIO2	I/O	-

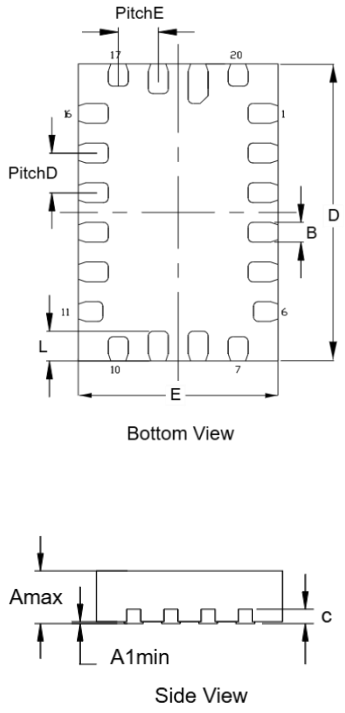
A.3 Symbol Parameters

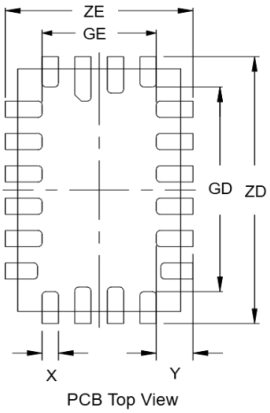
Orderable Part Number	Qualification	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Number of OpAmp	Number of Analog Switch	Number of Digital Rheostat	Number of ACMP/ DCMP	Number of V_{REF}	Number of GPIO	Number of CF	Number of MF	Number of Oscillator	Interface	RoHS
SLG47001-EV	Industrial	-40 °C	+105 °C	2.30 V	5.50 V	2	1	2	6	3	6	11	5	2	I^2C	Compliant
SLG47003-EV	Industrial	-40 °C	+105 °C	2.30 V	5.50 V	2	1	2	6	3	10	11	5	2	I^2C	Compliant

A.4 Footprint Design Information

A.4.1 20-STQFN

IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	PSC-5003-01	20

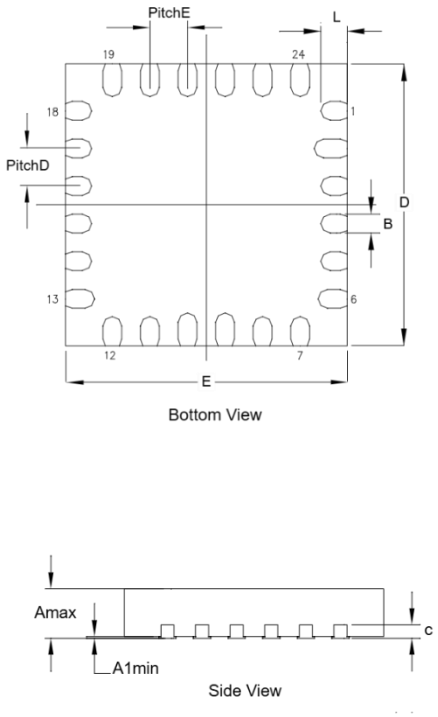
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.90	
Maximum body span (vertical side)	Dmax	3.10	
Minimum body span (horizontal side)	Emin	1.90	
Maximum body span (horizontal side)	Emax	2.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.25 [1]	
Maximum Lead Length	Lmax	0.35 [1]	
Number of pins (vertical side)	PinCountD	6	
Number of pins (horizontal side)	PinCountE	4	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side(center).	Pin1	S2	
Maximum Height	Amax	0.65	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.10	
Maximum Lead Thickness	cmax	0.20	

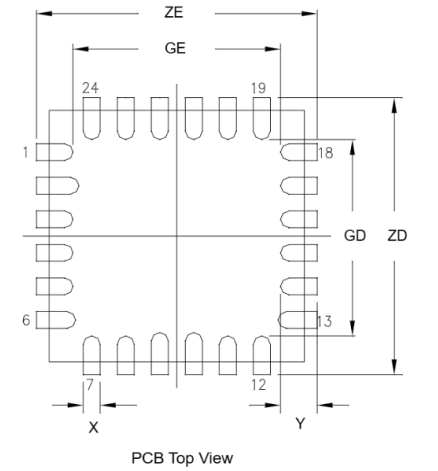
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	2.30	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	3.30	
Distance between left pad heel to right pad heel (horizontal side)	GE	1.40	
Distance between top pad heel to bottom pad heel (vertical side)	GD	2.53	
Pad Width	X	0.20	
Pad Length	Y	0.45 [1]	

[1] This package has more than one custom lead length.

A.4.2 24-STQFN

IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	PSC-5001-01	24

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.90	
Maximum body span (vertical side)	Dmax	3.10	
Minimum body span (horizontal side)	Emin	2.90	
Maximum body span (horizontal side)	Emax	3.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.23 [1]	
Maximum Lead Length	Lmax	0.33 [1]	
Number of pins (vertical side)	PinCountD	6	
Number of pins (horizontal side)	PinCountE	6	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side(center).	Pin1	S2	
Maximum Height	Amax	0.65	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.10	
Maximum Lead Thickness	cmax	0.20	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	3.30	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	3.30	
Distance between left pad heel to right pad heel (horizontal side)	GE	2.44	
Distance between top pad heel to bottom pad heel (vertical side)	GD	2.34	
Pad Width	X	0.20	
Pad Length	Y	0.43 [1]	

[1] This package has more than one custom lead length.