SLG47104

GreenPAK Programmable Mixed-Signal Matrix with High Voltage Features

Description

The SLG47104 provides a small, low power component for commonly used Mixed-Signal and Bridge functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, the High Voltage Pins, and the macrocells of the SLG47104.

Configurable PWM macrocell in combination with Special High Voltage outputs will be useful for a motor drive or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load.

Features

- Two Power Supply Inputs:
  - 2.5 V (±8 %) to 5.0 V (±10 %) V_{DD}
  - 3.3 V (±9 %) to 12.0 V (±10 %) V_{DD2}
- Two High Voltage High Current Drive GPOs
  - Full Bridge Driver Option
  - Dual/Single Half Bridge Driver Option
  - Slew Rate Modes:
    - Motor Driver Mode
    - Pre-Driver (MOSFET Driver) Mode
  - SLEEP Function
  - Low $R_{DS(ON)}$ High Side + Low Side resistance = 0.4 Ω
  - 2 A Peak, 1.5 A RMS per Full Bridge (at V_{DD2} = 5 V, T = +25 °C) (Note 1)
  - 2 A Peak, 1.5 A RMS per Half Bridge GPO (at V_{DD2} = 5 V, T = +25 °C) (Note 1)
  - Integrated Protections:
    - Over Current Protection (OCP)
    - Short Circuit Protection
    - Under-Voltage Lockout (UVLO)
    - Thermal Shutdown (TSD)
  - SENSE Input that is connected to the Current Comparator for Current Control
  - Fault Signal Indicator for Full Bridge:
    - OCP
    - UVLO
    - TSD
- One Current Sense Comparators with Dynamical V_{REF} Mode
- One High-Speed General Purpose ACMP
  - Modes: UVLO, OCP, TSD, Voltage Monitor, Current Monitor
- One Voltage Reference (V_{REF}) Output
- Three Multi-Function Macrocells
  - Two Selectable DFF/LATCH/3-bit LUTs + 8-bit Delay/ Counters
  - One Selectable DFF/LATCH/4-bit LUT + 16-bit Delay/ Counter
- Nine Combination Function Macrocells
  - Two Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Three Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable D FF/LATCH or 3-bit LUT or PWM Chopper
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUT
- PWM Macrocell
  - Flexible 8-bit/7-bit PWM Mode with the Duty Cycle Control
  - 16 Preset Duty Cycle Registers Switching Mode for PWM Sine or Other Waveforms (Note 2)
- Serial Communications
  - I^2C Protocol Interface
- Additional Logic Function – One Deglitch Filter with Edge Detectors
- Two Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 25 MHz Oscillator
- POR
- One Time Programmable Memory
- Operating Temperature Range: -40 °C to +85 °C
- RoHS Compliant/Halogen-Free
- 20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

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Applications

- Smart Locks
- Personal Computers and Servers
- Consumer Electronics
- Motor Drivers
- Toys
- HV MOSFET Drivers
- Video Security Cameras
- LED Matrix Dimmers

Note 1: Power dissipation and thermal limits must be observed. See section 3.3 Recommended Operating Conditions.

Note 2: For all PWM features see section 12 Pulse Width Modulator Macrocell.

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1. Block Diagram

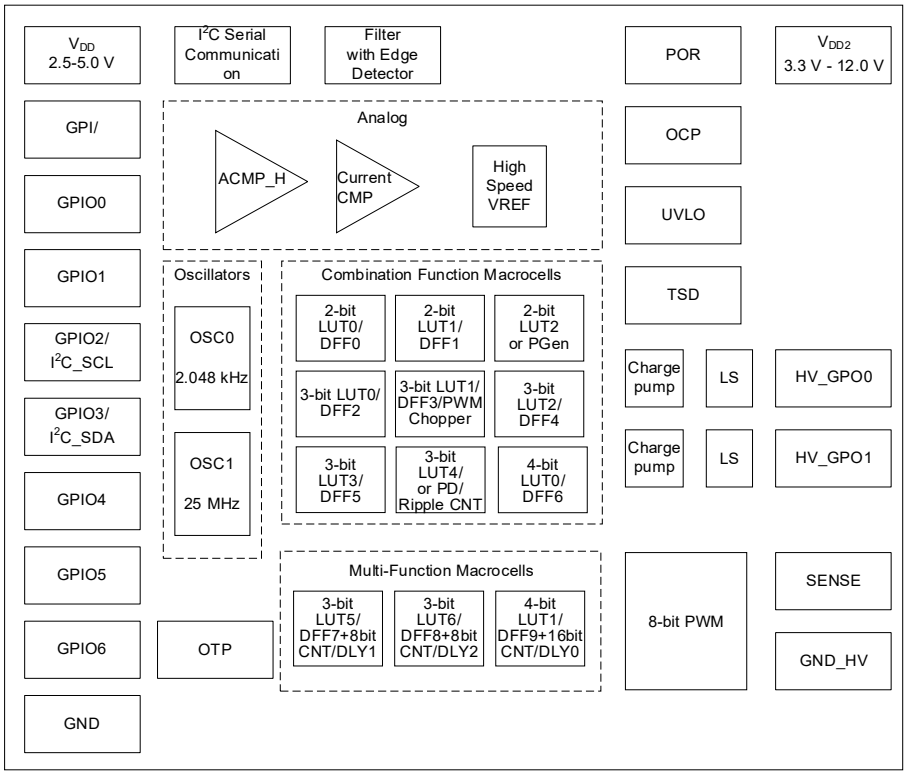


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

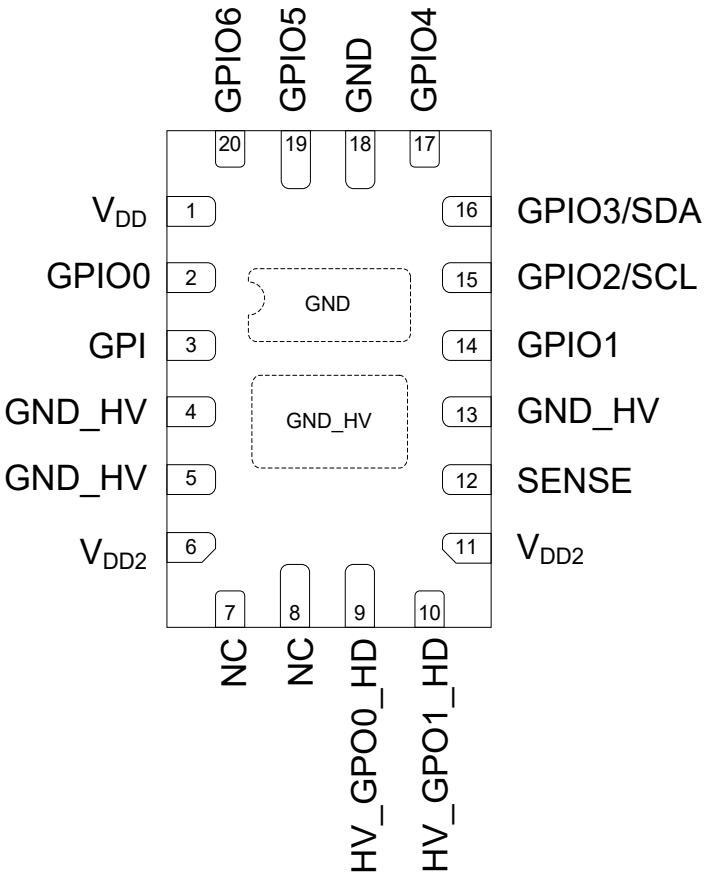


Figure 2. Pin Assignments – STQFN-20 – Top View

2.2 Pin Descriptions

Table 1. Pin Assignments and Description

Pin Number	Pin Name	Pin Function
1	V_{DD}	Power Supply 2.5 V – 5.0 V
2	GPIO0	Matrix OE GPIO, V_{REF} OUT
3	GPI	GPI, EXT_Vref, SLA_0
4	GND_HV	Analog Ground
5	GND_HV	Analog Ground
6	V_{DD2}	High Voltage Power Supply 3.3 V - 12.0 V (Note)
7	NC	Not connected
8	NC	Not connected
9	HV_GPO0_HD	HV_GPO_HD
10	HV_GPO1_HD	HV_GPO_HD
11	V_{DD2}	High Voltage Power Supply 3.3 V - 12.0 V (Note)
12	SENSE	Winding Sense, relate to HV_GPO0_HD and to HV_GPO1_HD
13	GND_HV	Analog Ground
14	GPIO1	Matrix OE GPIO, SLA_1, EXT_CLK for OSC0 or Current Sense CMP EXT_Vref
15	SCL/GPIO2	SCL, GPIO
16	SDA/GPIO3	SDA, GPIO
17	GPIO4	Matrix OE GPIO, SLA_2, EXT_CLK for OSC1
18	GND	General Ground
19	GPIO5	Matrix OE GPIO, ACMP_H
20	GPIO6	Matrix OE GPIO, SLA_3

Table 2. Pin Type Definitions

Pin Type	Description
V_{DD}	Power Supply
GPIO	General Purpose Input/Output
GPI	General Purpose Input
HV_GPO_HD	High Voltage General Purpose Output High Current Drive
SCL	I^2C Serial Clock Input
SDA	I^2C Serial Data Input/Output
GND	General Ground
GND_HV	Analog Ground
SENSE	Current Sense Pin
V_{DD2}	High Voltage Power Supply
NC	Not connected

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Parameter		Description	Conditions	Min	Max	Unit
Supply voltage on V_{DD} relative to GND				-0.3	7.0	V
Supply voltage on V_{DD2} relative to GND			(Note)	-0.3	18	V
DC Input Voltage				GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum V_{DD} Average or DC Current		(Through V_{DD} or GND pin) for V_{DD} group		--	120	mA
Maximum V_{DD2} or Sense Average or DC Current		(Through each V_{DD2}, SENSE pins)		--	2000	mA
Maximum Average or DC Current (V_{DD} power supply)	Push-Pull 1x	Through V_{DD} Group pins	T_J = -40 °C to +85 °C	--	11	mA
	Push-Pull 2x			--	16	
	OD 1x			--	11	
	OD 2x			--	21	
Maximum Average or DC Current (V_{DD} power supply)	Push-Pull 1x	Through V_{DD} Group pins	T_J = -40 °C to +85 °C	--	3.8	mA
	Push-Pull 2x			--	7.6	
	OD 1x			--	3.8	
	OD 2x			--	7.6	
Maximum Average or DC Current (V_{DD2} power supply)	Push-Pull/ Half Bridge	Through V_{DD2} High Current Group pins		--	1500	mA
Maximum pulsed current sink/sourced per HV HD pin		Pulse width ≤ 0.5 ms; duty cycle ≤ 2 %		-	Internally limited by OCP	mA
Current at Input Pin		Through V_{DD} Group pin		-0.1	1.0	mA
Input Leakage Current (Absolute Value)				--	1000	nA
Storage Temperature				-65	150	°C
Junction Temperature				--	150	°C
Moisture Sensitivity Level				1		

3.2 ESD Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	4000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage (V_{DD})		2.3	3.3	5.5	V
High Supply Voltage (V_{DD2})		3.0	12.0	13.2	V
Operating Ambient Temperature (T_A)		-40	+25	+85	°C
Operating Junction Temperature (T_J)		-40	--	+150	°C
Capacitor Value at V_{DD}		--	0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	--	V_{DD} [1]	V
[1] V_{DD} for GPI, GPIO4, GPIO5, GPIO6					

3.4 Thermal Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	4L JEDEC PCB	--	--	65	°C/W
		4L JEDEC PCB with a thermal vias that connects thermal pad through all layers of the PCB	--	--	46	°C/W
Junction-to-case (top) Thermal Resistance	$\theta_{JC(top)}$		--	23.50	--	°C/W
Junction-to-board Thermal Resistance	θ_{JB}		--	25.51	--	°C/W
Junction-to-case (top) Characterization Parameter	$\Psi_{JC(top)}$		--	6.80	--	°C/W
Junction-to-board Characterization Parameter	Ψ_{JB}		--	24.44	--	°C/W

3.5 Electrical Specifications

3.5.1 Logic IO Specifications

V_{DD} = 2.3 V to 5.5 V, T = -40 °C to +85 °C, typical values are at T = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-Level Input Voltage for V_{DD} group [3]	V_{IH}	Logic Input [1]	0.7xV_{DD}	--	V_{DD} + 0.3	V
		Logic Input with Schmitt Trigger	0.8xV_{DD}	--	V_{DD} + 0.3	V
		Low-level Logic Input [1]	1.25	--	V_{DD} + 0.3	V
LOW-Level Input Voltage for V_{DD} group [3]	V_{IL}	Logic Input [1]	GND - 0.3	--	0.3xV_{DD}	V
		Logic Input with Schmitt Trigger	GND - 0.3	--	0.2xV_{DD}	V
		Low-level Logic Input [1]	GND - 0.3	--	0.5	V
Maximal Voltage Applied to any pin in High Impedance State	V_O	For V_{DD} group	--	--	V_{DD} + 0.3	V
	V_{O2}	For V_{DD2} group	--	--	V_{DD} + 0.3	V
HIGH-Level Output Voltage for V_{DD} Group T_J = -40 °C to +85 °C	V_{OH}	Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OH} = 1 mA	2.07	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OH} = 3 mA	2.54	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, I_{OH} = 5 mA	3.95	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OH} = 1 mA	2.13	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OH} = 3 mA	2.69	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 5 V ± 10%, I_{OH} = 5 mA	4.11	--	--	V
HIGH-Level Output Voltage for V_{DD} Group T_J = -40 °C to +150 °C		Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OH} = 1 mA	2.05	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OH} = 3 mA	2.49	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, I_{OH} = 5 mA	3.90	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OH} = 1 mA	2.12	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OH} = 3 mA	2.67	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 5 V ± 10%, I_{OH} = 5 mA	4.09	--	--	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Voltage for V_{DD} Group T_J = -40 °C to +85 °C	V_{OL}	Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.08	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.18	V
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, I_{OL} = 5 mA	--	--	0.21	V
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.04	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.09	V
		Push-Pull, 2x Drive, V_{DD} = 5 V ± 10%, I_{OL} = 5 mA	--	--	0.11	V
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.030	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.068	V
		NMOS OD, 1x Drive, V_{DD} = 5 V ±10 %, I_{OL} = 5 mA	--	--	0.083	V
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.014	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.035	V
		NMOS OD, 2x Drive, V_{DD} = 5 V ± 10%, I_{OL} = 5 mA	--	--	0.083	V
LOW-Level Output Voltage for V_{DD} Group T_J = -40 °C to +150 °C	V_{OL}	Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.09	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.21	V
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, I_{OL} = 5 mA	--	--	0.26	V
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.04	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.11	V
		Push-Pull, 2x Drive, V_{DD} = 5 V ± 10%, I_{OL} = 5 mA	--	--	0.13	V
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.035	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.082	V
		NMOS OD, 1x Drive, V_{DD} = 5 V ±10 %, I_{OL} = 5 mA	--	--	0.100	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Voltage for V_{DD} Group T_J = -40 °C to +150 °C	V_{OL}	NMOS OD, 2x Drive, V_{DD} = 2.5 V ±8 %, I_{OL} = 1 mA	--	--	0.017	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ±10 %, I_{OL} = 3 mA	--	--	0.042	V
		NMOS OD, 2x Drive, V_{DD} = 5 V ± 10%, I_{OL} = 5 mA	--	--	0.052	V
HIGH-Level Output Voltage for V_{DD2} High Current Group	V_{OH2}	Push-Pull, V_{DD2} = 5 V ± 10 %, I_{OH2} = 10 mA	4.496	--	--	V
		Push-Pull, V_{DD2} = 9 V ± 10 %, I_{OH2} = 10 mA	8.097	--	--	V
		Push-Pull, V_{DD2} = 12 V ± 10 %, I_{OH2} = 10 mA	10.797	--	--	V
LOW-Level Output Voltage for V_{DD2} High Current Group	V_{OLH2}	Push-Pull, V_{DD2} = 5 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 9 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 12 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
HIGH-Level Output Pulse Current [2] Voltage for V_{DD} Group, T_J = -40 °C to +85 °C	I_{OH}	Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OH} = V_{DD} - 0.2	1.43	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OH} = 2.4 V	4.80	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, V_{OH} = 2.4 V	18.60	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OH} = V_{DD} - 0.2	2.87	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OH} = 2.4 V	9.56	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5 V ±10 %, V_{OH} = 2.4 V	36.83	--	--	mA
HIGH-Level Output Pulse Current [2] Voltage for V_{DD} Group, T_J = -40 °C to +150 °C		Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OH} = V_{DD} - 0.2	1.27	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OH} = 2.4 V	4.35	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, V_{OH} = 2.4 V	16.70	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OH} = V_{DD} - 0.2	2.52	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OH} = 2.4 V	8.57	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5 V ±10 %, V_{OH} = 2.4 V	32.99	--	--	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Pulse Current [2] Voltage for V_{DD} Group, T_J = -40 °C to +85 °C	I_{OL}	Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	1.92	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	6.18	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	8.98	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	3.82	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	12.25	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	17.67	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	4.71	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	15.16	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	21.84	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	9.24	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	29.51	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	41.90	--	--	mA
LOW-Level Output Pulse Current [2] Voltage for V_{DD} Group, T_J = -40 °C to +150 °C	I_{OL}	Push-Pull, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	1.63	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	5.23	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	7.52	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	3.22	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	10.34	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	14.78	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	3.99	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	12.77	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	18.26	--	--	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Pulse Current [2] Voltage for V_{DD} Group, T_J = -40 °C to +150 °C	I_{OL}	NMOS OD, 2x Drive, V_{DD} = 2.5 V ±8 %, V_{OL} = 0.15 V	7.83	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ±10 %, V_{OL} = 0.4 V	24.94	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5 V ±10 %, V_{OL} = 0.4 V	35.03	--	--	mA
All macrocells are in SLEEP mode including charge pumps	I_{sleep}	For V_{DD2} <= 5.0V UVLO disabled	--	--	219	nA
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip, T_J = -40 °C to +150 °C	1.80	1.98	2.16	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip, T_J = -40 °C to +150 °C	1.33	1.55	1.83	V
Pull-up or Pull-down Resistance T_J = -40 °C to +85 °C	R_{PULL}	1 M for Pull-up: V_{IN} = GND, for Pull-down: V_{IN} = DV_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND, for Pull-down: V_{IN} = DV_{DD}	--	100	--	kΩ
		10 k for Pull-up: V_{IN} = GND, for Pull-down: V_{IN} = DV_{DD}	--	10	--	kΩ
Pull-up or Pull-down Resistance T_J = -40 °C to +150 °C		1 M for Pull-up: V_{IN} = GND, for Pull-down: V_{IN} = DV_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND, for Pull-down: V_{IN} = DV_{DD}	--	100	--	kΩ
		10 k for Pull-up: V_{IN} = GND, for Pull-down: V_{IN} = DV_{DD}	--	10	--	kΩ
Input Capacitance	C_{IN}		--	2.5	--	pF

[1] No hysteresis.

[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

[3] ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}. See sections 6.6 ESD Protection to 6.9 Matrix OE IO Structure (for VDD Group).

3.5.2 I²C Specifications

V_{DD} = 2.3 V to 5.5 V, T = -40 °C to +150 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
IO Stage							
LOW-level Input Voltage	V_{IL}	Schmitt Trigger Input	-0.5	0.3xV_{DD}	-	0.3xV_{DD}	V
		Low-voltage Logic Input	-0.5	0.5	N/A	N/A	
HIGH-level Input Voltage	V_{IH}	Schmitt Trigger Input	0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
		Low-voltage Logic Input	1.2	5.5	N/A	N/A	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05xV_{DD}	--	0.05xV_{DD}	--	V

Parameter	Symbol	Conditions	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
LOW-Level Output Voltage 1	V_{OL1}	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
LOW-Level Output Voltage 2	V_{OL2}	(Open-Drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
LOW-Level Output Current	I_{OL}	V_{OL} = 0.4 V	3	--	20	--	mA
		V_{OL} = 0.6 V	6	--	--	--	
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ [1]	t_{OF}		14x (V_{DD}/5.5 V)	250	14x (V_{DD}/5.5 V)	120	ns
Pulse Width of Spikes that must be suppressed by the Input Filter	t_{SP}		0	50	0	50	ns
Input Current each IO Pin	I_i	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µA
Capacitance for each IO Pin	C_i		--	10	--	10	pF
Timings (see Figure 132 for Diagram)							
SCL Clock Frequency	f_{SCL}		--	400	--	1000	kHz
SCL Clock, LOW Period	t_{LOW}		1300	--	500	--	ns
SCL Clock, HIGH Period	t_{HIGH}		600	--	260	--	ns
Input Filter Spike Suppression (SCL, SDA)	t_I		--	50	--	50	ns
Data Valid Time	t_{VD_DAT}		--	900	--	450	ns
Data Valid Acknowledge Time	t_{VD_ACK}		--	900	--	450	ns
Bus Free Time between Stop and Start	t_{BUF}		1300	--	500	--	ns
Start Hold Time	t_{HD_STA}		600	--	260	--	ns
Start Set-up Time	t_{SU_STA}		600	--	260	--	ns
Data Hold Time [1]	t_{HD_DAT}		0	--	0	--	ns
		Low-voltage Logic Input Mode	327	--	N/A	N/A	
Data Set-up Time[1]	t_{SU_DAT}		100	--	50	--	ns
		Low-voltage Logic Input Mode	443	--	N/A	N/A	
SCL, SDA Rise Time	t_R		--	300	--	120	ns
SCL, SDA Fall Time	t_F		--	300	--	120	ns
Set-up Time for Repeated START Condition	t_{SU_STA}		600	--	260	--	ns
Data OUT Hold Time	t_{DH}		50	--	50	--	ns

[1] Does not meet standard I^2C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min).

[2] For Fast-mode Plus SDA pin must be configured as 3.2x Open-Drain

[3] Please follow official I^2C spec UM10204.

[4] When SCL Input is in Low-Level Logic mode max frequency is 400 kHz.

3.5.3 Macrocells Current Consumption

Typical current estimated for each macrocell at T = +25 °C.

Parameter	Symbol	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Current	I_{DD}	Chip Quiescent (Pdet + OTP st-by)	0.038	0.040	0.047	µA
		Chip Quiescent and LPBG (LPBG + Pdet + OTP st-by + I^2C en + leakages), UVLO disabled	0.57	0.59	0.63	µA
		Chip Quiescent and LPBG (LPBG + Pdet + OTP st-by + I^2C en + leakages), UVLO enabled	20.98	21.14	21.53	µA
		V_{REF} (LPBG + Vref_mux + Vref_OUT_BUF)	21.6	21.7	22.1	µA
		OSC1 25 MHz, Pre-divider = 1	62.37	79.3	126.74	µA
		OSC1 25 MHz, Pre-divider = 2	47.41	59.3	94.93	µA
		OSC1 25 MHz, Pre-divider = 4	40.14	49.4	79.02	µA
		OSC1 25 MHz, Pre-divider = 8	36.28	44.2	70.81	µA
		OSC1 25 MHz, Pre-divider = 12	35.21	42.8	68.41	µA
		OSC0 2.048 kHz, Pre-divider = 1	0.35	0.35	0.37	µA
		OSC0 2.048 kHz, Pre-divider = 4	0.34	0.35	0.37	µA
		OSC0 2.048 kHz, Pre-divider = 8	0.34	0.35	0.37	µA
		IO with 1x push-pull + 4 pF (2.048 kHz)	0.13	0.16	0.22	µA
		ACMP_H (includes internal V_{REF})	36.1	36.5	37.8	µA
		ACMP_H (includes external V_{REF})	21.5	22.0	23.2	µA
		Any Half Bridge, V_{DD2} = 5 V	164.7	193.7	270.2	µA
		Full Bridge + one CCMP (any V_{REF}, any Gain), V_{DD2} = 5 V	361.3	394.1	480.7	µA
Current (through V_{DD2})	I_{DD2}	Any Half Bridge, V_{DD2} = 5 V	164.3	162.0	160.6	µA
		Full Bridge + one CCMP (any V_{REF}, any Gain), V_{DD2} = 5 V	327.7	319.4	313.6	µA
		Under-voltage Lockout Enabled, V_{DD2} = 5 V	4.17	4.17	4.17	µA

3.5.4 HV Output Electrical Specifications

Typical values are at T = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Rise time HV OUT in Driver Mode	t_R	V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to +150 °C	80	116	200	ns
Rise time HV OUT in Pre-Driver Mode		V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to +150 °C	10	13	22	ns
Fall time HV OUT in Driver Mode	t_F	V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to +85 °C	80	115	200	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to +150 °C	80	115	225	ns
Fall time HV OUT in Pre-Driver Mode		V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to +85 °C	8	11	23	ns
		V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to +150°C	8	11	25	ns
Dead band time of HV_GPOx_HD in Driver Mode (For Full Bridge and Half Bridge HV OUT modes)	t_{DEAD}	V_{DD2} = 3 V, T_J = -40 °C to +150 °C	--	337	--	ns
		V_{DD2} = 5 V, T_J = -40 °C to +150 °C	--	75	--	ns
		V_{DD2} = 13.2 V, T_J = -40 °C to +150 °C	--	91	--	ns
Dead band time of HV_GPOx_HD in Pre-driver Mode (For Full Bridge and Half Bridge HV OUT modes)		V_{DD2} = 3 V, T_J = -40 °C to +150 °C	--	55	--	ns
		V_{DD2} = 5 V, T_J = -40 °C to +150 °C	--	23	--	ns
		V_{DD2} = 13.2 V, T_J = -40 °C to +150 °C	--	22	--	ns
Dead band time, gener- ated by PWM block	PWM_t_{DEAD}	Configured in PWM block	0; 1·T_{clk}; 2·T_{clk}; 3·T_{clk};			Clk time
HS FET on resistance (SENSE, GND_HV and GND Pins are connected together)	$R_{DS(ON)}$	V_{DD2} = 13.2 V, I_O = 500 mA, T_J = +25 ºC	--	171	--	mΩ
		V_{DD2} = 13.2 V, I_O = 500 mA, T_J = +150 ºC	--	--	295	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = +25 ºC	--	171	--	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = +150 ºC	--	--	295	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = +25 ºC	--	177	--	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = +150 ºC	--	--	305	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = +25 ºC	--	256	--	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = +150 ºC	--	--	426	mΩ
LS FET on resistance (SENSE, GND_HV and GND Pins are connected together)		V_{DD2} = 13.2 V, I_O = 500 mA, T_J = +25 ºC	--	182	--	mΩ
		V_{DD2} = 13.2 V, I_O = 500 mA, T_J = +150 ºC	--	--	332	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = +25 ºC	--	182	--	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = +150 ºC	--	--	331	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = +25 ºC	--	185	--	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = +150 ºC	--	--	338	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = +25 ºC	--	232	--	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = +150 ºC	--	--	414	mΩ
Off-state leakage current	I_{OFF}	GPO0_HD, GPO1_HD, V_{DD2} = 5.0 V, T_J = -40 °C to +85 °C, Sleep Mode	--	--	0.2	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		GPO0_HD, GPO1_HD, V_{DD2} = 5.0 V, T_J = -40 °C to +150 °C, Sleep Mode	--	--	1.5	µA
Single HV Driver Current Consumption (including support circuits), without output load	I_{DD2}	V_{DD2} = 5.0 V, T_J = -40 °C to +150 °C, Static (PWM is off), including the charge pump OSC	--	--	250	µA
		V_{DD2} = 5.0 V, T_J = -40 °C to +150 °C, Switching (PWM = 250 kHz)	--	344	625	µA
All HV Drivers On Current Consumption (including support circuits), without output load		V_{DD2} = 5.0 V, T_J = -40 °C to +150 °C, Static (PWM is off), including the charge pump OSC	100	--	313	µA
Charge Pump consump- tion current (from V_{DD1} Pin or V_{DD2} Pin)		V_{DD2} = 5.0 V, T_J = -40 °C to +150 °C, PWM is off, including the charge pump OSC	--	--	200	µA
Wake-up time	t_{WAKE}	HV SLEEP OUT high to output transition, BG is always on, Another pins SLEEP - disable	--	82.3	134	µs

3.5.5 Protection Circuits Electrical Specifications

Typical values are at T = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overcurrent protection threshold	I_{OCP}	Per any HS or LS FET	--	2.18	--	A
OCP deglitch time [1]	t_{OCP1}	V_{DD} = 5 V, V_{DD2} = 5 V, T = +25 ºC, Deglitch = Enable, High Side	--	2.497	--	µs
		V_{DD} = 5 V, V_{DD2} = 5 V, T = +25 ºC, Deglitch = Enable, Low Side	--	1.232	--	µs
OCP retry time [2]	t_{OCP2}	Delay = 492 µs	--	491	--	µs
		Delay = 656 µs	--	655	--	µs
		Delay = 824 µs	--	818	--	µs
		Delay = 988 µs	--	982	--	µs
		Delay = 1152 µs	--	1146	--	µs
		Delay = 1316 µs	--	1309	--	µs
		Delay = 1480 µs	--	1473	--	µs
		Delay = 1640 µs	--	1637	--	µs
Recover from Under-voltage lockout	V_{UVLO} [3]	At rising edge of V_{DD2}	--	--	2.90	V
Under-voltage lockout		At falling edge of V_{DD2}	--	--	2.77	V
Thermal shutdown temperature	T_{TSD}	Junction temperature T_J	135	141	159	°C
Thermal shutdown hysteresis	T_{HYST}		--	16	--	°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit

[1] OCP deglitch time option can be enabled by register [875]. The High Side FETs doesn't have OCP deglitch time if the current through the FET is higher than I_{OCP} level during enable time. This is done to avoid huge currents during retry when the short is persist on the output.

[2] OCP retry time can be selected separately for each HV OUT: HV GPO0 – registers [796:794], HV GPO1 – registers [804:802]. For more information check the section 7.3.3 Over-Current Protection (OCP).

[3] UVLO function can be enabled for V_{DD2} by registers [864:865]. For more information see section 7.3.5 Under-Voltage Lockout (UVLO).

3.5.6 Timing Specifications

Typical startup estimated for chip at T = +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chip Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	1	2	ms

Typical delay estimated for each macrocell at T = +25 °C.

Parameter	Symbol	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Delay	tpd	Digital Input to PP 1x	25	25	16	18	12	13	ns
		Digital Input with Schmitt Trigger to PP 1x	25	26	17	19	14	14	ns
		Low Voltage Digital Input to PP 1x	25	247	17	157	13	83	ns
		Digital Input to PP 2x	22	24	15	17	11	13	ns
		Digital Input to NMOS 1x	--	23	--	17	--	13	ns
		Digital Input to NMOS 2x	--	23	--	16	--	12	ns
		1x3-State Hi-Z to 0	--	23	--	17	--	12	ns
		1x3-State Hi-Z to 1	24	--	17	--	12	--	ns
		2x3-State Hi-Z to 0	--	23	--	16	--	11	ns
		2x3-State Hi-Z to 1	23	--	16	--	12	--	ns
		OE Hi-Z to 0	--	23	--	17	--	12	ns
		OE Hi-Z to 1	24	--	17	--	12	--	ns
		DFF	22	24	15	17	10	11	ns
		LATCH	24	25	15	17	10	11	ns
		CTN/DLY	72	71	51	50	35	34	ns
		2-bit LUT	17	17	11	12	8	8	ns
		3-bit LUT	19	19	13	13	8	9	ns
		4-bit LUT	20	19	13	12	9	9	ns
		Pipe Delay nRESET OUT Q, nQ	24	24	17	17	12	12	ns
		Pipe Delay OUT0 Q, nQ	24	26	18	15	10	11	ns
		PGEN CLK	18	18	12	13	8	9	ns
Delay	tpd	PGEN nRESET Zto0	--	20	--	14	--	10	ns
		PGEN nRESET Zto1	21	--	13	--	9	--	ns

Parameter	Symbol	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Width	tw	Edge detect	256	255	180	179	125	125	ns
Delay	tpd	Edge detect	18	19	12	12	8	8	ns
		Edge detect Delayed	275	274	190	191	132	133	ns
		Filter nQ	180	209	118	137	75	82	ns
		Filter nQ First spark	--	191	--	123	--	73	ns
		Filter Q	209	180	136	119	81	75	ns
		Filter Q First spark	191	--	123	--	73	--	ns
		Inverter Filter nQ First spark	--	165	--	107	--	68	ns
		Inverter Filter Q First spark	164	--	107	--	68	--	ns
		Ripple CNT CLK UP Q1	25	23	17	16	11	11	ns
		Ripple CNT CLK UP Q2	29	22	29	16	13	11	ns
		Ripple CNT CLK UP Q3	33	22	23	16	15	11	ns
		Ripple CNT CLK DOWN Q1	25	24	17	17	11	11	ns
		Ripple CNT CLK DOWN Q2	25	29	17	20	11	13	ns
		Ripple CNT CLK DOWN Q3	25	36	16	25	11	16	ns
		Ripple CNT nSET UP Q1	25	41	16	29	11	19	ns
		Ripple CNT nSET UP Q2	23	42	15	29	11	19	ns
		Ripple CNT nSET UP Q3	22	46	14	31	10	21	ns
		Ripple CNT nSET DOWN Q1	25	41	16	28	11	19	ns
		Ripple CNT nSET DOWN Q2	23	40	15	27	10	18	ns
		Ripple CNT nSET DOWN Q3	22	40	14	27	10	18	ns
		PWM CHOPPER BLANK	--	37	--	25	--	17	ns
		PWM OUT- nQ1	--	25	--	17	--	11	ns
		PWM OUT- Q1	24	--	16	--	11	--	ns
		PWM OUT+ nQ1	21	--	14	--	9	--	ns
		PWM OUT+ Q1	--	22	--	15	--	10	ns

Typical Filter Rejection Pulse Width at T = +25 °C.

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 180	< 118	< 71	ns

LP_BG Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, typical values are at T = +25 °C, unless otherwise specified.

Parameter	Min	Typ	Max	Unit
LP_BG Start-Up Time	--	--	2.5	ms
LP_BG I_{cc}	--	555	--	nA

3.5.7 Counter/Delay Specifications

Typical Counter/Delay Offset at T = +25 °C.

Parameter	OSC Freq	OSC Power-on	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	25 MHz	auto	134	127	125	ns
Power-On time	2.048 kHz	auto	496	443	398	µs
Frequency settling time	25 MHz	auto	850	1100	1200	ns
Frequency settling time	2.048 kHz	auto	900	950	900	µs
Variable (CLK period)	25 MHz	forced	39-42	39-42	39-42	ns
Variable (CLK period)	2.048 kHz	forced	476-495	476-495	476-495	µs
Typical Propagation Delay (non-delayed edge)	25 MHz	either	39	26	17	ns

3.5.8 Oscillator Specifications

OSC0 Frequency Limits, V_{DD} = 2.3 V to 5.5 V.

OSC	Junction Temperature Range											
	+25 °C			-40 °C to +85 °C			-40 °C to +125 °C			-40 °C to +150 °C		
	Min Value	Max Value	Error, %	Min Value	Max Value	Error, %	Min Value	Max Value	Error, %	Min Value	Max Value	Error, %
2.048 kHz OSC0	2.015 kHz	2.071 kHz	+1.12	1.901 kHz	2.137 kHz	+4.35	1.901 kHz	2.137 kHz	+4.35	1.720 kHz	2.137 kHz	+4.35
			-1.61			-7.17			-7.17			-16.01

OSC1 Frequency Limits, V_{DD} = 2.3 V to 5.5 V.

OSC	Junction Temperature Range								
	+25 °C			-40 °C to +85 °C			-40 °C to +150 °C		
	Min Value	Max Value	Error, %	Min Value	Max Value	Error, %	Min Value	Max Value	Error, %
25 MHz OSC1	24.610 MHz	25.300 MHz	+1.20	24.084 MHz	25.944 MHz	+3.78	23.560 MHz	25.944 MHz	+3.78
			-1.56			-3.66			-5.76

Oscillators power-on delay at T = +25 °C, OSC power setting: "Auto Power-On".

Power Supply Range (V_{DD}), V	OSC0 2.048 kHz		OSC1 25 MHz		OSC1 25 MHz Start with Delay	
	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns
2.30	521	660	50	59	138	148
2.50	496	622	44	50	134	143
3.30	443	539	29	34	127	137
5.00	398	469	18	32	125	137
5.50	385	452	17	31	125	137

3.5.9 Current Sense Comparator Specifications

T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, typical values are at T = +25 °C, unless otherwise noted.

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Current limit input range	$R_{CurrCMP}$	Per Full Bridge SENSE Pin (LS FET only)	I_{FET}*R_{SENSE}	50	--	500	mV
Current Sense accuracy	I_{accur}	T_J = 25 °C	120 mV input	-3.1	--	+3.9	%
			504 mV input	-0.9	--	+1.0	%
		T_J = -40 °C to +85 °C	120 mV input	-4.5	--	+4.7	%
			504 mV input	-1.2	--	+1.2	%
Current Sense accuracy	I_{accur}	T_J = -40 °C to +150 °C	120 mV input	-4.5	--	+5.6	%
			504 mV input	-1.2	--	+1.4	%
		T_J = +25 °C	60 mV input	-5.1	--	+7.7	%
			252 mV input	-1.6	--	+1.8	%
		T_J = -40 °C to +85 °C	60 mV input	-7.5	--	+8.8	%
			252 mV input	-2.0	--	+2.1	%
		T_J = -40 °C to +150 °C	60 mV input	-7.5	--	+10.4	%
			252 mV input	-2.2	--	+2.5	%
Current Sense CMP Startup Time	t_{start}	Current Sense CMP Power-on delay	T_J = -40 °C to +85 °C	--	6.7	12.1	µs
Propagation Delay, Response Time	PROP		Low to High, T_J = -40 °C to +85 °C, V_{REF} = 1024 mV, Overdrive = 100 mV	--	0.5	0.9	µs
			Low to High, T_J = -40 °C to +85 °C, V_{REF} = 1024 mV, Overdrive = 10 mV	--	0.9	2.5	µs
			Low to High, T_J = -40 °C to +85 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.5	1.0	µs
			Low to High, T_J = -40 °C to +85 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 10 mV	--	1	3.7	µs
			High to Low, T_J = -40 °C to +85 °C, V_{REF} = 1024 mV, Overdrive = 100 mV	--	0.6	0.9	µs
			High to Low, T_J = -40 °C to +85 °C, V_{REF} = 1024 mV, Overdrive = 10 mV	--	1.8	5.6	µs

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
			High to Low, T_J = -40 °C to +85 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.6	1.0	µs
			High to Low, T_J = -40 °C to +85 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 10 mV	--	1.8	7.0	µs
Propagation Delay, Response Time	PROP		Low to High, T_J = -40 °C to +150 °C, V_{REF} = 1024 mV, Overdrive = 100 mV	--	0.5	0.9	µs
			Low to High, T_J = -40 °C to +150 °C, V_{REF} = 1024 mV, Overdrive = 10 mV	--	1.0	2.6	µs
			Low to High, T_J = -40 °C to +150 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.6	1.0	µs
			Low to High, T_J = -40 °C to +150 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 10 mV	--	1.0	3.7	µs
			High to Low, T_J = -40 °C to +150 °C, V_{REF} = 1024 mV, Overdrive = 100 mV	--	0.6	1.0	µs
			High to Low, T_J = -40 °C to +150 °C, V_{REF} = 1024 mV, Overdrive = 10 mV	--	1.9	5.6	µs
			High to Low, T_J = -40 °C to +150 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.6	1.1	µs
			High to Low, T_J = -40 °C to +150 °C, V_{REF} = 480 mV to 2016 mV, Overdrive = 10 mV	--	1.9	7.9	µs

3.5.10 ACMP Specifications

T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, typical values are at T = +25 °C, unless otherwise noted.

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
ACMP Input Voltage Range	V_{ACMP}	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
ACMP Input Offset [2]	V_{offset}	ACMPH Vhys = 0 mV, Gain = 1, V_{REF} = 32 mV to 2016 mV	T_J = -40 °C to +85 °C	-8	--	6.5	mV
			T_J = -40 °C to +150 °C	-9.8	--	7.2	mV
ACMP Startup Time	t_{start}	ACMPH Power-On delay, Minimal required wake time for the "Wake and SLEEP function	T_J = -40 °C to +85 °C	--	--	32	µs
			T_J = -40 °C to +150 °C	--	--	32.7	µs
ACMPH Built-in Hysteresis [1] [2]	V_{HYS}	V_{HYS} = 32 mV	T_J = -40 °C to +85 °C	30	--	35	mV
		V_{HYS} = 64 mV		62	--	66	mV
		V_{HYS} = 192 mV		187	--	197	mV
		V_{HYS} = 32 mV	T_J = -40 °C to +150 °C	29	--	36	mV
		V_{HYS} = 64 mV		61	--	67	mV
		V_{HYS} = 192 mV		186	--	198	mV
Series Input Resistance	R_{sin}	Gain = 1x		--	10	--	GΩ
		Gain = 0.5x		1.7	--	2.4	MΩ
		Gain = 0.33x		1.7	--	2.4	MΩ
		Gain = 0.25x		1.7	--	2.4	MΩ
Propagation Delay, Response Time	PROP	ACMPH, V_{REF} = 1.024 V, Gain = 1, Overdrive = 100 mV	Low to High, T_J = -40 °C to +85 °C	--	0.51	1.51	µs
			High to Low, T_J = -40 °C to +85 °C	--	0.51	0.79	µs
		ACMPH, V_{REF} = 0.032 V to 2.016 V, Gain = 1, Overdrive = 100 mV	Low to High, T_J = -40 °C to +85 °C	--	0.53	1.51	µs
			High to Low, T_J = -40 °C to +85 °C	--	0.52	1.11	µs
		ACMPH, V_{REF} = 1.024 V, Gain = 1, Overdrive = 100 mV	Low to High, T_J = -40 °C to +150 °C	--	0.51	1.51	µs
			High to Low, T_J = -40 °C to +150 °C	--	0.51	0.80	µs
		ACMPH, V_{REF} = 0.032 V to 2.016 V, Gain = 1, Overdrive = 100 mV	Low to High, T_J = -40 °C to +150 °C	--	0.53	1.51	µs
			High to Low, T_J = -40 °C to +150 °C	--	0.52	1.18	µs
Gain Error (including threshold and internal V_{REF} error)	G	G = 1	T_J = -40 °C to +85 °C	1	1	1	
		G = 0.5		0.487	0.500	0.519	
		G = 0.33		0.320	0.334	0.346	
		G = 0.25		0.244	0.250	0.260	
		G = 1	T_J = -40 °C to +150 °C	1	1	1	
		G = 0.5		0.485	0.500	0.519	
		G = 0.33		0.320	0.334	0.346	
		G = 0.25		0.244	0.250	0.260	

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Internal V_{REF} accuracy	$V_{REFaccuracy}$	V_{REF} ≥ 1.216 V	T_J = +25 °C	-0.50	--	+0.50	%
			T_J = -40 °C to +150 °C	-1.64	--	+1.64	%
V_{REF} output buffer offset (when connected to the output Pin)	V_{REFbuf_offset}	V_{REF} = 32 mV to 2016 mV	T_J = +25 °C	-17.1	--	9.6	mV
			T_J = -40 °C to +150 °C	-18.0	--	11.1	mV
V_{REF} Output Buffer Capacitance Loading	C_{VREF}	Resistance Load in Condition cell	1 MΩ	--	--	5	pF
			560 kΩ	--	--	10	pF
			100 kΩ	--	--	40	pF
			10 kΩ	--	--	80	pF
			2 kΩ	--	--	120	pF
			1 kΩ, V_{REF}: 32 mV to 1024 mV	--	--	150	pF

[1] V_{IL} = Vin - V_{HYS}, V_{IH} = Vin.

[2] ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}. See sections 6.6 ESD Protection to 6.9 Matrix OE IO Structure (for VDD Group).

4. User Programmability

The SLG47104 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.hvp file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

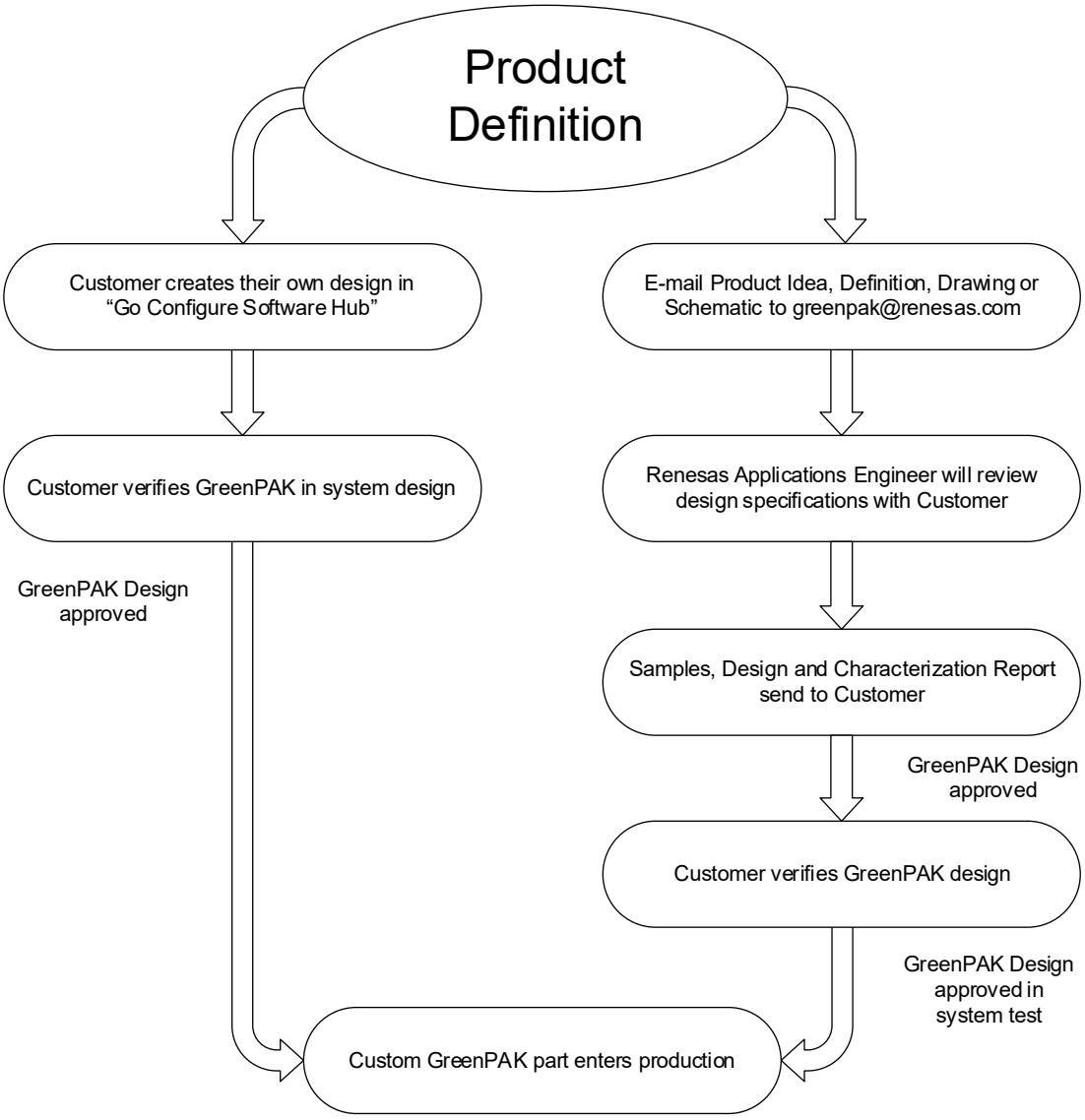


Figure 3. Steps to Create a Custom GreenPAK Device

5. System Overview

5.1 GPIO Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- NMOS Open-drain Outputs
- Push-pull Outputs
- Analog IO
- 10 kΩ/100 kΩ/1 MΩ Pull-up/Pull-down resistors
- GPIO with OE can be configured as bidirectional IO or three-state output.

5.2 High Voltage Output Pins

- High voltage digital output in Push-pull, Open-drain configurations or Full Bridge logic
- Build-in Overcurrent and Short Circuit protection
- Configurable Dead Band Time
- Sleep mode to save energy

5.3 Connection Matrix

- Digital matrix for circuit connections based on user design.

5.4 Current Sense Comparator

- SENSE pin that is connected to a positive input of Sense Comparator for Advanced Current Control
- Selectable V_{REF}: 6-bit selection
- Static or Dynamic V_{REF} selection
- Configurable Gain: 4x or 8x.

5.5 General Purpose Analog Comparator

- Wide V_{REF} Selector: 32 mV to 2016 mV, with 32 mV step
- Selectable hysteresis: 2-bit selection
- Configurable Gain (resistor divider) 1x, 0.5x, 0.33x, 0.25x
- Different input sources: PINs, V_{DD}.

5.6 Voltage Reference

- Used for references on Analog Comparators
- Can be driven to external pin.

5.7 Nine Combination Function Macrocells

- Two Selectable DFF/LATCH or 2-bit LUTs
- One Selectable Programmable Pattern Generator or 2-bit LUT
- Three Selectable DFF/LATCH with Set/Reset input or 3-bit LUTs
- One Selectable DFF/LATCH with Set/Reset input or 3-bit LUTs or PWM Chopper
- One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
- One Selectable DFF/LATCH with Set/Reset input or 4-bit LUT.

5.8 Three Multi-Function Macrocells

- Two Selectable DFF/LATCH/3-bit LUTs + 8-bit Delay/Counters
- One Selectable DFF/LATCH/4-bit LUT + 16-bit Delay/Counter.

5.9 PWM Macrocells

- Flexible 8-bit or 7-bit PWM mode with the Duty Cycle control
- True 0 % and 100 % Duty Cycle
- Regular or 16 Preset Registers mode
- Autostop mode
- Phase correct mode
- Selectable separate Dead Band Time
- Glitch Safety.

5.10 Serial Communication

- I^2C Interface.

5.11 Additional Logic Function

- One Deglitch filter macrocell
- Includes Edge Detection function.

5.12 Two Oscillators

- 2.048 kHz
- 25 MHz.

5.13 DUAL V_{DD}

- General Power Supply V_{DD} in range 2.5 V to 5.0 V
- Second Power Supply V_{DD2} in range 3.3 V to 12.0 V (Note)
- Two GPIOs groups: V_{DD} GPIOs Group, V_{DD2} GPOs Group.

Note: Both V_{DD2} pins must be connected to V_{DD2} source.

6. Input/Output Pins

6.1 GPIO Pins

The SLG47104 has a total of 7 GPIO, 1 GPI, and 2 HV GPO Pins, which can function as either a user-defined Input or Output, as well as serving as a special function (such as outputting the voltage reference).

6.2 GPI Pin

GPI serves as General Purpose Input Pin of V_{DD} Group.

6.3 HV GPO Pins

HV GPO0, HV GPO1 serve as High Voltage General Purpose Output Pins of V_{DD2} Group.

6.4 Pull-Up/Down Resistors

All IO Pins of V_{DD} Group have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either Pull-up or Pull-downs.

6.5 Fast Pull-Up/Down during Power-Up

During power-up, IO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to the normal setting value. This function is enabled by register [754].

6.6 ESD Protection

Every pin has the ESD protection circuit built-in, see Figure 4, Figure 5, Figure 6. In addition to the ESD diodes, when configured as inputs, all pins have a series resistor which decreases the exceeding input current to a safe level. For the value of the resistors refer to Table 3. It should be noted, this additional input resistance will affect the input thresholds (V_{IH} and V_{IL}) when using pull-up/pull-down resistors.

Table 3. ESD Resistors Value

Pin	Value, Ohm
GPIO0	200
GPI	200
GPIO1	1060
GPIO2	200
GPIO3	200
GPIO4	1060
GPIO5	1060
GPIO6	1060

6.7 GPI IO Structure (for V_{DD} Group)

6.7.1 GPI IO Structure

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode, lv_en = 1
11: Analog IO mode

Note 1: Can be varied over PVT, for reference only.
Note 2: Should be taken into consideration when using pull-up/pull-down resistors. May affect V_{IH} and V_{IL}.

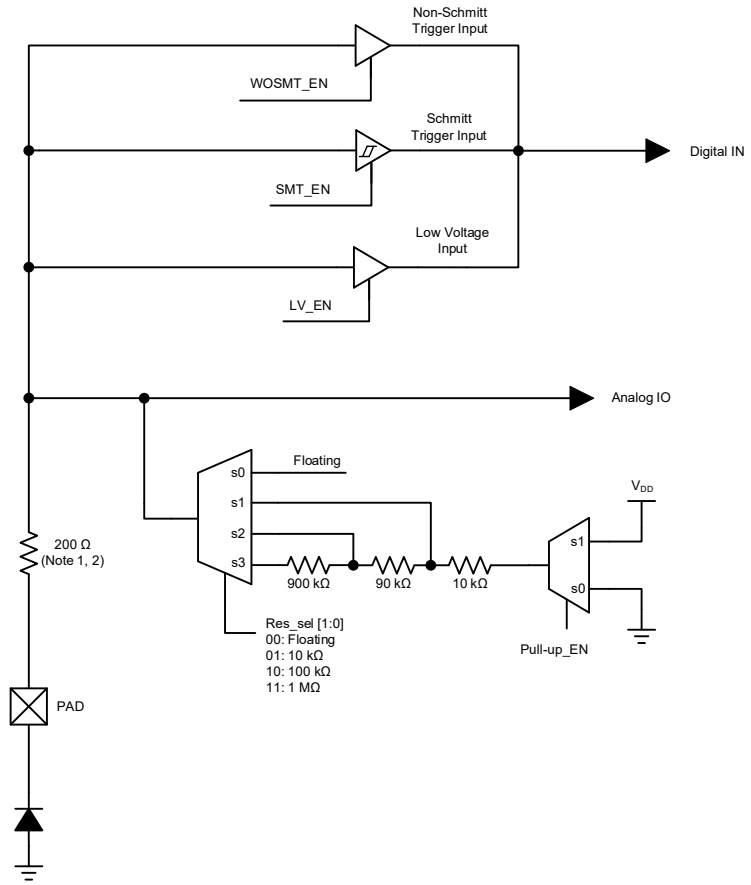


Figure 4. GPI Structure Diagram

6.8 I²C Mode IO Structure (for V_{DD} Group)

6.8.1 I²C Mode IO Structure (for SCL/GPIO2 and SDA/GPIO3, Register OE)

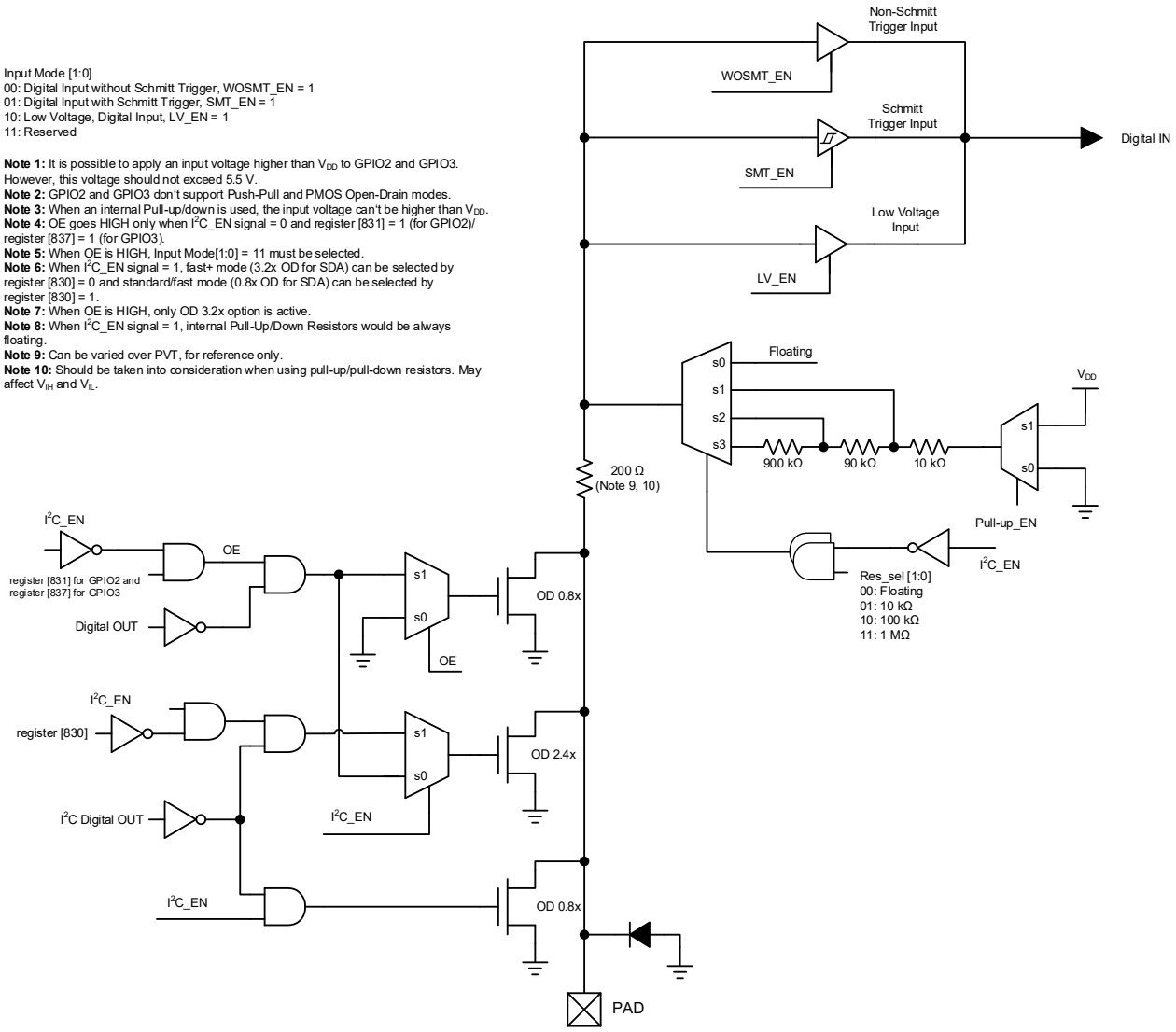


Figure 5. GPIO with I²C Mode Structure Diagram

Table 4. GPIO2 Mode Selection

Register [2032]	Register [831]	Register [830]	GPIO2 Mode
0	x	x	I²C SCL
1	0	x	GPI, depends on registers [826:825]
1	1	x	GPO, 3.4x OD only

Table 5. GPIO3 Mode Selection

Register [2032]	Register [837]	Register [830]	GPIO3 Mode
0	x	0	I²C SDA, fast+
0	x	1	I²C SDA, standard/fast
1	0	x	GPI, depends on registers [833:832]
1	1	x	GPO, 3.4x OD only

6.9 Matrix OE IO Structure (for V_{DD} Group)

6.9.1 Matrix OE IO Structure (for GPIOs 0, 1, 4, 5, 6)

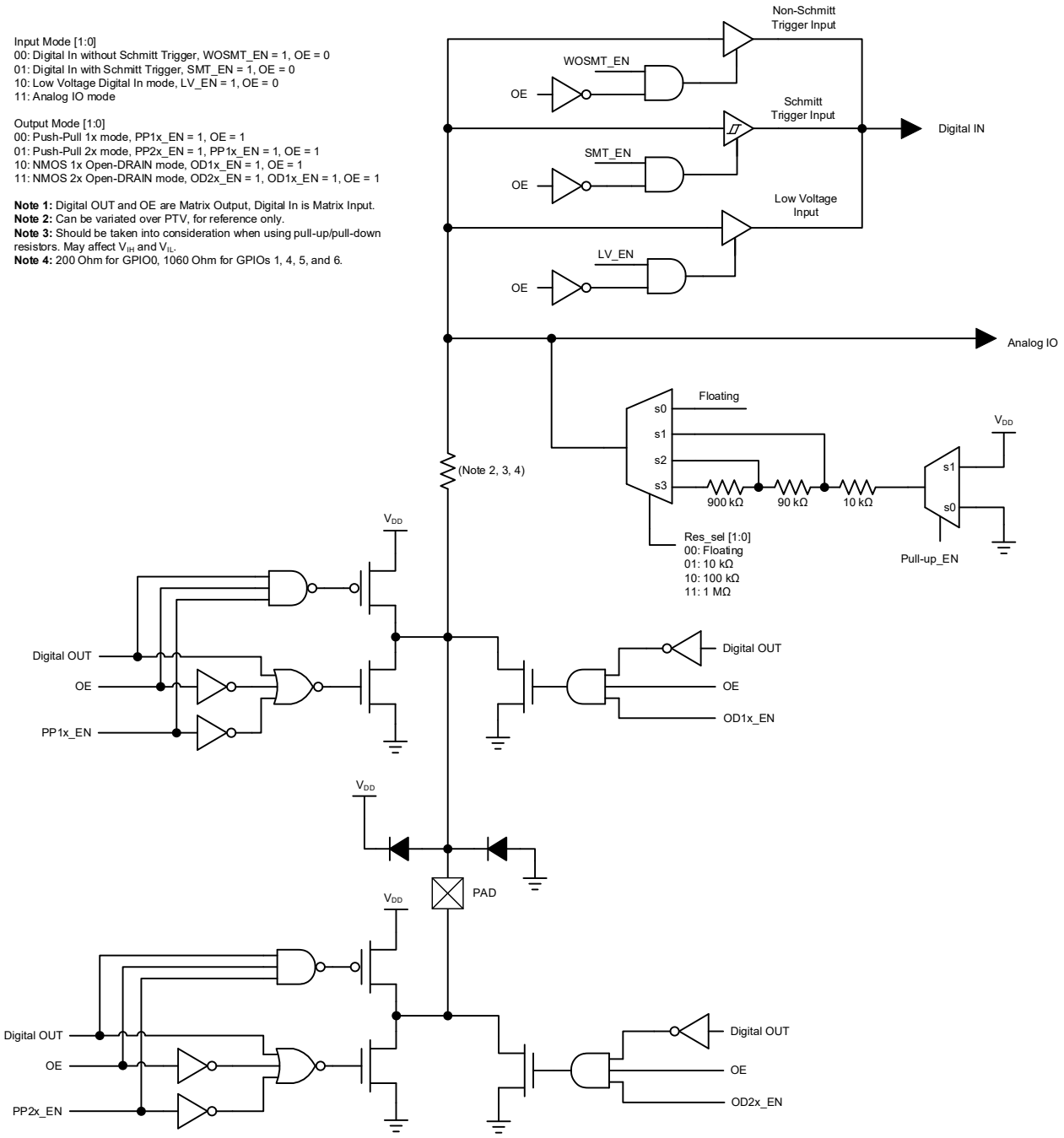


Figure 6. GPIO Matrix OE IO Structure Diagram

6.10 GPO Matrix OE Structure (for V_{DD2} Group)

Using SLEEP mode to minimize supply current should be sufficient under normal operation.

Outputs HV GPO0, HV GPO1 have individual HV_SLEEP Input signal. If Sleep Input is active, Charge Pumps are disabled, and Full Bridge FETs are set to Hi-Z state.

6.10.1 GPO with Matrix OE Structure (for HV GPOs 0 and 1)

Output Mode registers [793:792] for HV_GPO_0, registers [801:800] for HV_GPO_1:
00: Hi-Z mode (High Impedance)
01: NMOS 1x LOW SIDE Open-DRAIN mode (Open-DRAIN LOW side On)
10: NMOS 1x HIGH SIDE Open-DRAIN mode (Open-DRAIN HIGH side On)
11: Push-Pull 1x mode (Open-DRAIN HIGH and LOW sides On)

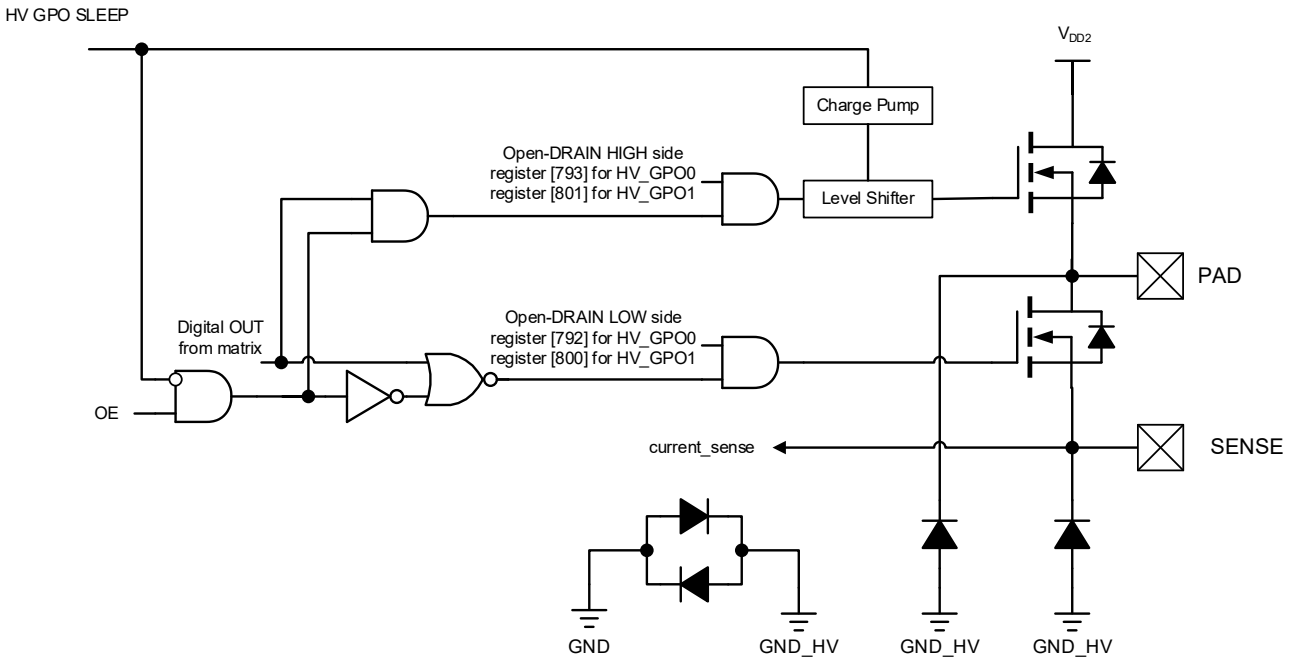


Figure 7. HV GPO Matrix OE IO Structure Diagram (for HV GPOs 0 and 1)

6.11 IO Typical Performance

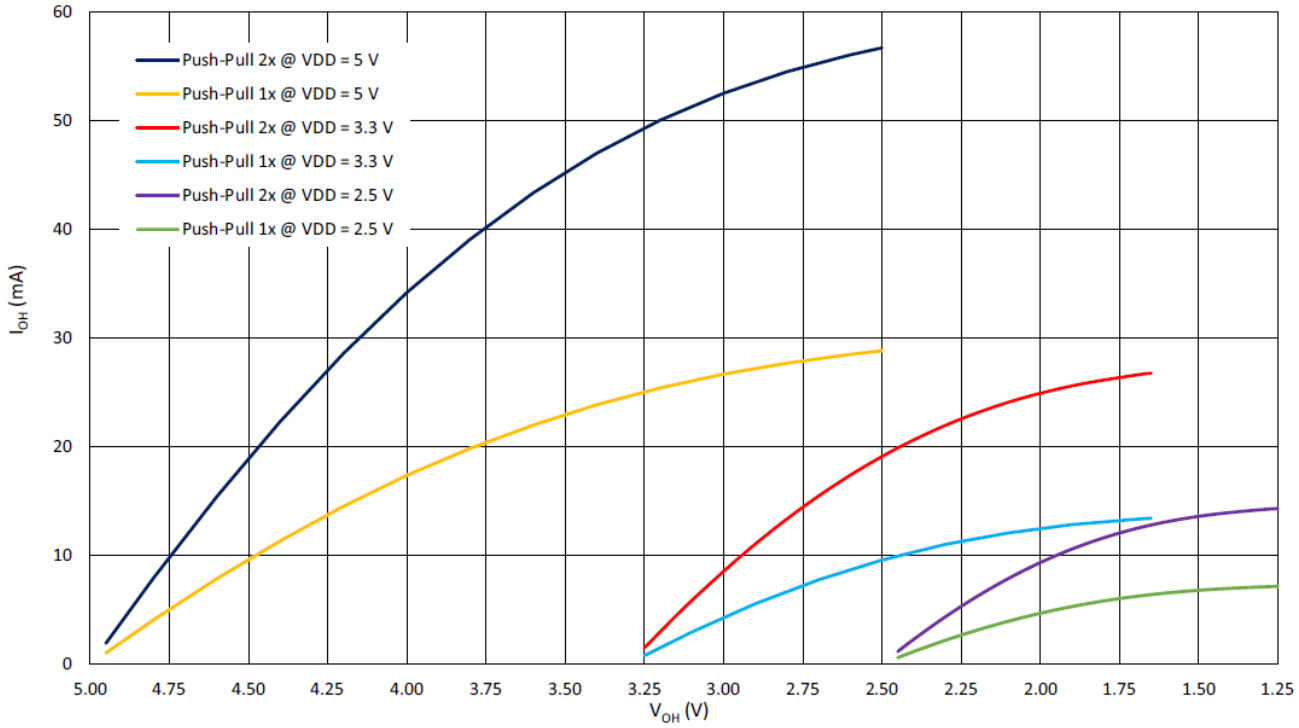


Figure 8. Typical High Level Output Current vs. High Level Output Voltage at T = +25 °C

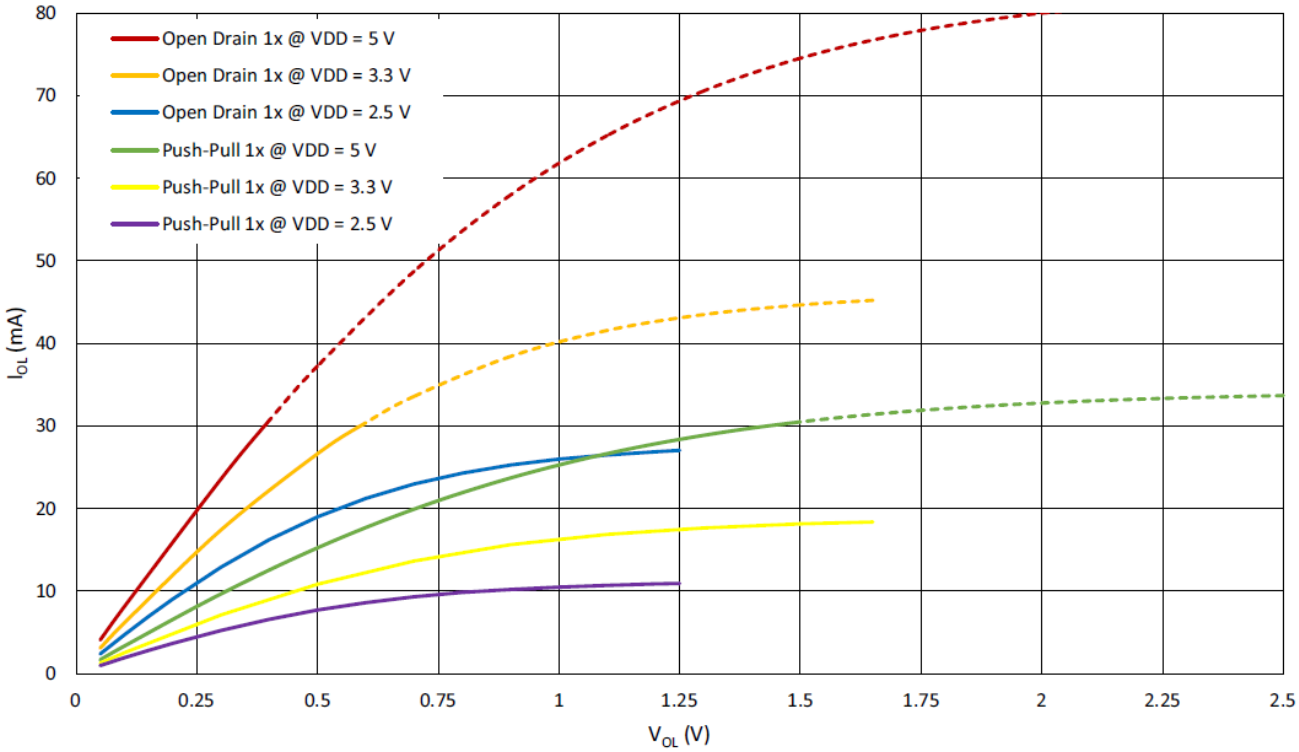


Figure 9. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = +25 °C, Full Range

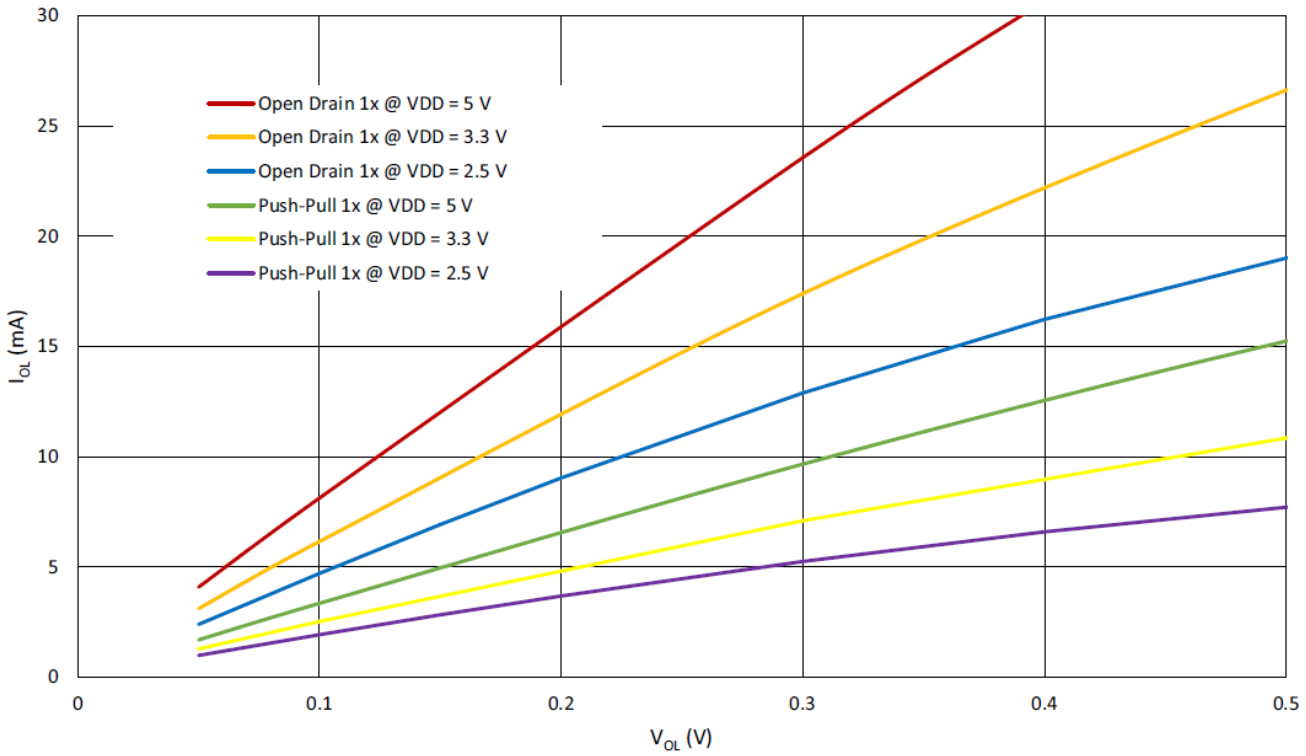


Figure 10. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = +25 °C

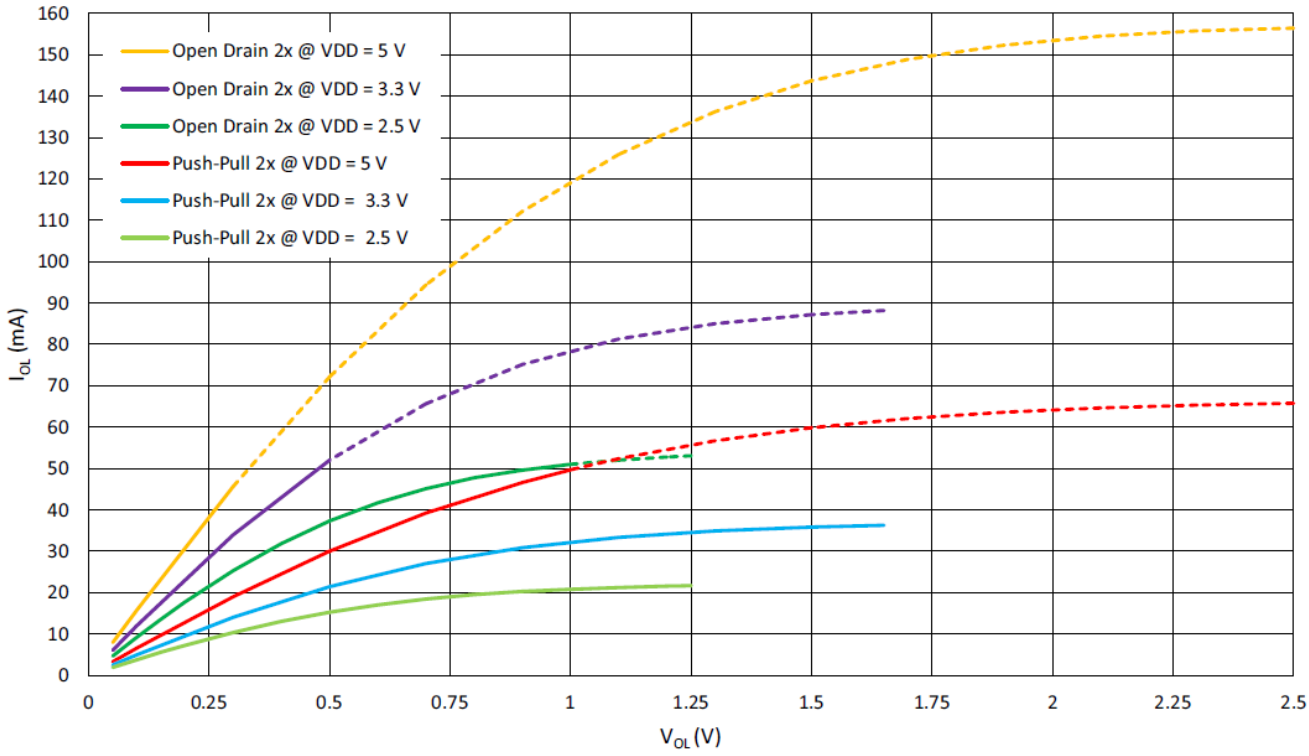


Figure 11. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = +25 °C, Full Range

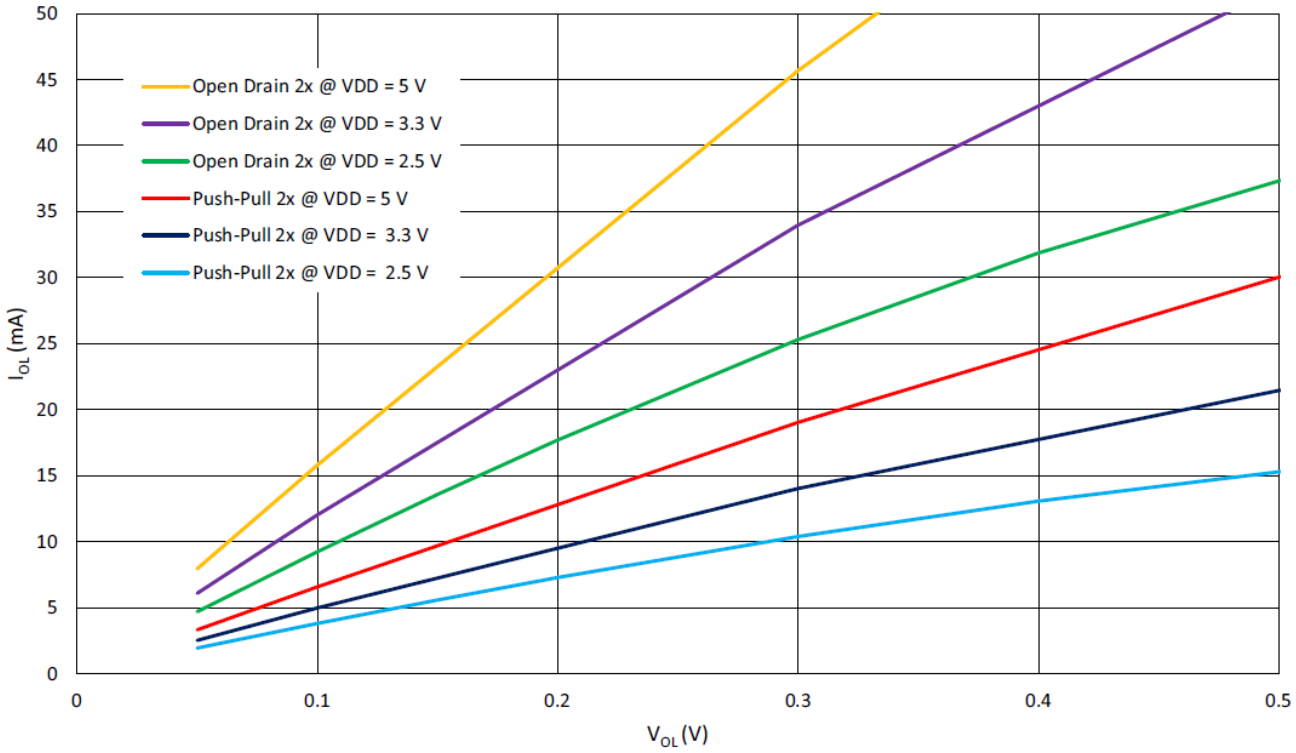


Figure 12. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = +25 °C

7. High Voltage Output Modes

The device integrates two High Drive Half bridges, PWM voltage regulation method, current regulation circuitry, and protection circuits, including dead band circuit.

HV GPOs work as power pins, so if two bridges open simultaneously for any reason, for example, timing desynchronization, it will result in cross-conduction (shoot-through) between the two bridges and damage the chip. To avoid this, t_{DEAD} is entered between switching on upper and lower power transistors. During output state transition from LOW to HIGH, the lower NMOS turns off and only after t_{DEAD} the upper NMOS turns on. While t_{DEAD} the pin is in Hi-Z state. The same process is applied when transiting from HIGH to LOW. t_{DEAD} is different for DRIVER and PREDRIVER modes.

The user can select Modes of HV Outputs:

- Full Bridge Mode
- Half Bridge Mode.

Additionally, user can select Slew Rate Modes:

- Slow Slew Rate Motor Driver Mode
- Fast Slew Rate Pre-Driver Mode.

PWM Voltage regulation is useful for designs where there is a need to maintain constant motor speed with changeable power supply level. When the High V_{DD2} is decreasing (battery discharging), it's possible to increase PWM duty cycle, and when the High V_{DD2} is increasing (battery charging) it's possible to decrease PWM duty cycle. It's possible to turn off the PWM and HV GPO for battery saving when the motor is idle, and others.

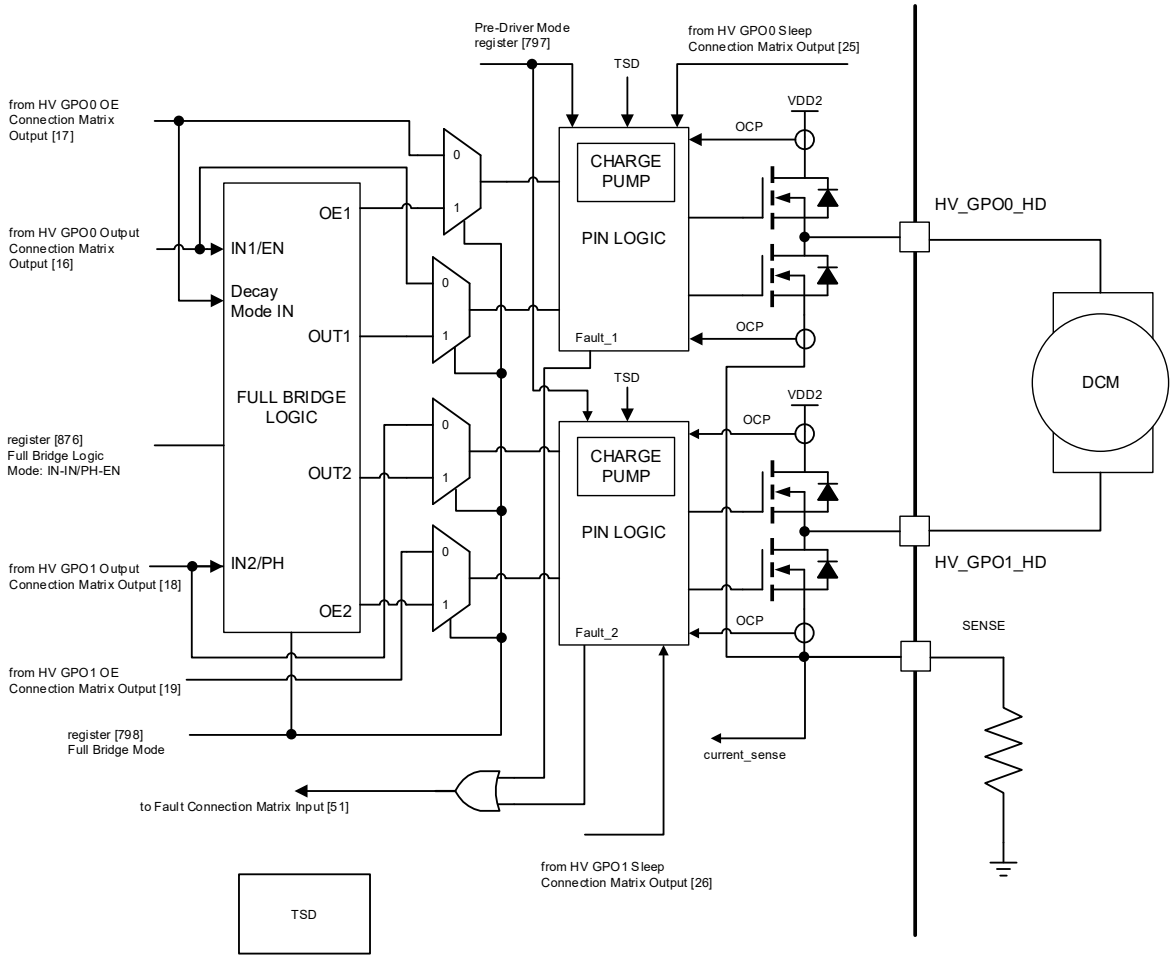


Figure 13. HV OUT Block Diagram

7.1 HV Outputs Modes

7.1.1 Full Bridge Mode

Full Bridge mode for HV_GPO0/HV_GPO1 is selected by setting register [798] to 1. In Full Bridge mode, HV GPO0 functions in couple with HV GPO1. This mode is useful for driving DC motors with the ability to change the motors rotation direction as shown in Figure 14.

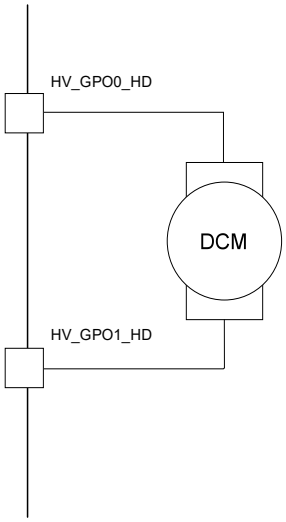


Figure 14. Full Bridge Mode Operation

OE inputs of high voltage pins aren't used in Full-Bridge mode except HV GPO0 OE input in PH-EN sub-mode, where this input is used to select Decay Mode for Full Bridge.

Note 1: Both Sleep inputs in this mode are active separately.

Other inputs and outputs of HV_GPO0/HV_GPO1 operate depending on Control Sel register [876] as shown in Table 6 and Table 7.

Table 6. HV OUT CTRL Full Bridge Logic for IN-IN Mode

Sleep_x	IN0	IN1	HV_GPO0_HD (Pin 9)	HV_GPO1_HD (Pin 10)	Function
1	X	X	Hi-Z	Hi-Z	Off (Coast)
0	0	0	Hi-Z	Hi-Z	Coast
0	0	1	L	H	Reverse
0	1	0	H	L	Forward
0	1	1	L	L	Brake

Table 7. HV OUT CTRL Full Bridge Logic for PH-EN Mode

Sleep_x	Decay	EN	PN	HV_GPO0_HD (Pin 9)	HV_GPO1_HD (Pin 10)	Function
1	X	X	X	Hi-Z	Hi-Z	Off (Coast)
0	0 (Fast Decay)	0	X	Hi-Z	Hi-Z	Coast
0	1 (Slow Decay)	0	X	L	L	Brake
0	X	1	0	H	L	Forward
0	X	1	1	L	H	Reverse

HV GPO0 and HV GPO1 are tri-state Pins, which cannot be pulled up/down internally.

The HV GPOs can be used to control the motor speed with the help of PWM technique. Fast decay mode causes a rapid reduction in inductive current and allows the motor to coast toward zero velocity. Slow decay mode leads to a slower reduction in inductive current but produces rapid deceleration.

For IN-IN mode, to drive DC motor in fast-decay mode, the PWM signal should be applied to one of IN0 or IN1 inputs, while the other is held in the logic LOW state. To use slow-decay mode, one of IN0 or IN1 inputs should be sourced by PWM signal, while the opposite pin is held in the logic HIGH state.

Table 8. PWM Control of Motor Speed (IN-IN Mode)

Function	IN0	IN1
Forward PWM, fast decay	PWM	0
Forward PWM, slow decay	1	PWM
Reverse PWM, fast decay	0	PWM
Reverse PWM, slow decay	PWM	1

PH-EN mode is convenient for Full Bridge control by internal PWM macrocell, because PWM signal is connected to EN input only. In this case there is no need to use an additional MUXs. Rotation direction is changed by PH input.

Table 9. PWM Control of Motor Speed (PH-EN Mode)

Function	EN	PH	Decay
Forward PWM, fast decay	PWM	0	0
Reverse PWM, fast decay	PWM	1	0
Forward PWM, slow decay	PWM	0	1
Reverse PWM, slow decay	PWM	1	1

Figure 15 shows the current paths in a different drive and decay modes.

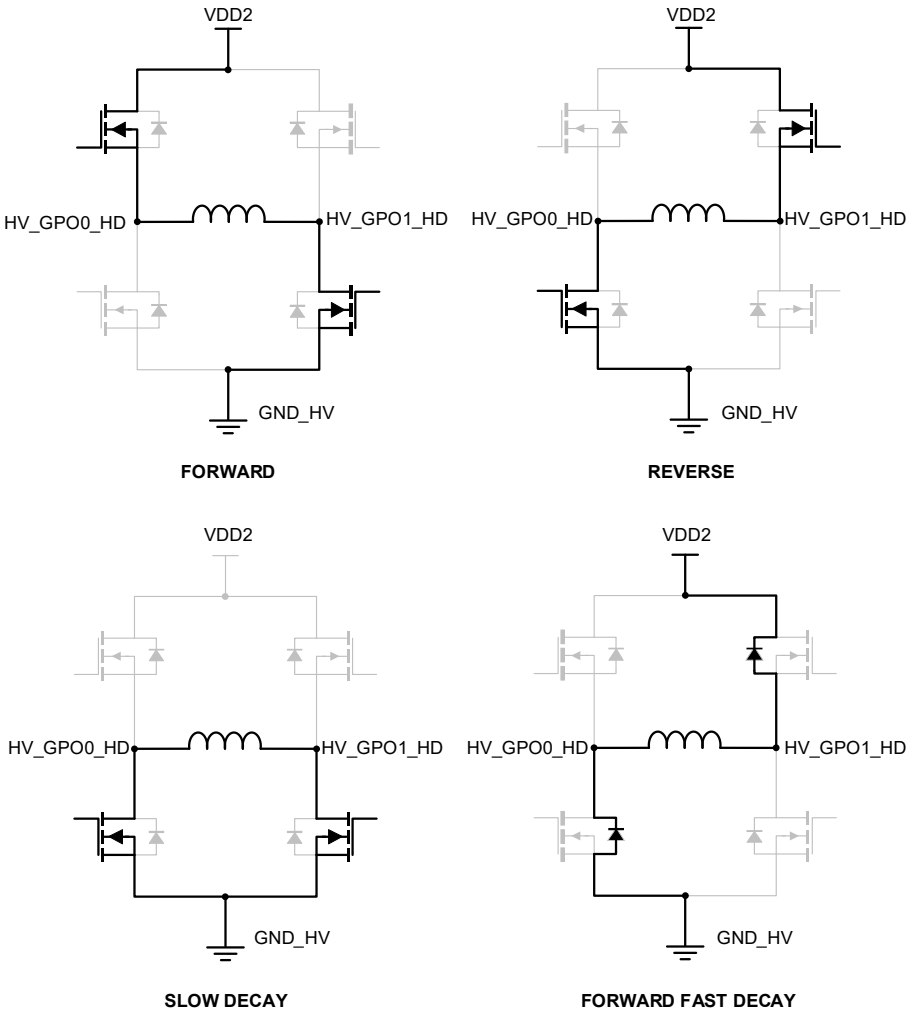


Figure 15. Drive and Decay Modes

7.1.2 Half Bridge Mode

Half Bridge Mode for HV_GPO0/HV_GPO1 is selected by setting register [798] to 0. This mode is the default mode for HV GPO pins. In this mode, there is a possibility to drive up to two motors spinning in one direction.

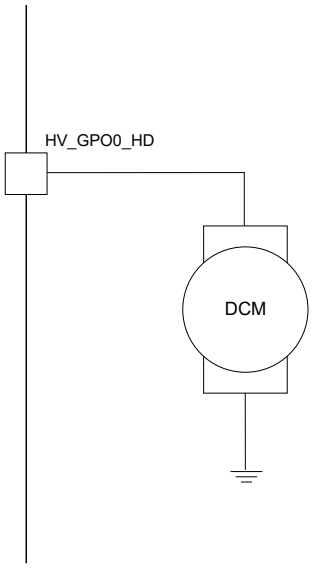


Figure 16. Half Bridge Mode Operation

In Half Bridge mode HV GPO will work as shown in Table 10 and Table 11.

Table 10. HV_GPO0_HD Half Bridge Logic

Function	Sleep0	OE0	IN0	HV_GPO0_HD (Pin 9)
Off	1	X	X	Hi-Z
Off (Coast)	0	0	X	Hi-Z
Brake	0	1	0	L
Forward	0	1	1	H

Table 11. HV_GPO1_HD Half Bridge Logic

Function	Sleep1	OE1	IN1	HV_GPO1_HD (Pin 10)
Off	1	X	X	Hi-Z
Off (Coast)	0	0	X	Hi-Z
Brake	0	1	0	L
Forward	0	1	1	H

Note: Both Sleep inputs in this mode are active separately.

7.2 Fast Slew Rate Pre-Driver Mode

This mode for HV_GPO0/HV_GPO1 is activated by setting register [797] to 1. The difference of this mode is that the rise time t_R and fall time t_F of High Drive HV GPO MOSFETs are much smaller than in regular mode. This allows using SLG47104 as a driver for external transistors.

When this mode is active, user can configure HV GPO to work in Full Bridge or Half Bridge Modes, as well as in regular mode (Pre-Driver Mode is disabled, registers [797] = 0).

7.3 Protection Circuits

7.3.1 General FAULT Signals

The SLG47104 has three fault signals to the Connection Matrix (FAULT, OCP FAULT and THERMAL FAULT). FAULT is the general signal which consist of three available FAULT signals for V_{DD2}.

FAULT:

- Over-current Protection OCP
- Thermal Shutdown
- Under-voltage Lockout.

For more information of FAULT signals see sections 7.3.3 Over-Current Protection (OCP), 7.3.4 Thermal Shutdown (TSD) and Thermal Considerations, and 7.3.5 Under-Voltage Lockout (UVLO).

7.3.2 Advanced Current Control

A current control circuit is provided to regulate the system in the event of an overcurrent condition, for example, an abnormal mechanical load of DC motor. This circuit can be used for implementing constant current closed loop systems or for current limitation.

The current is sensed by external sense resistor connected to SENSE pin. Current comparator is used to convert these currents to logic level. Using a current comparator with PWM block, output current can be dynamically changed. For example, for dynamic DC motor current limiting.

7.3.3 Over-Current Protection (OCP)

Each of FETs has an analog current limit circuit for turning off FETs when the current exceeds the threshold. When the overcurrent (I_{OCP}) persists for longer than the t_{OCP1} time, the FETs in the Half Bridge are disabled, and FAULT signal to matrix driven high. t_{OCP1} time is optional. It can be enabled by register [875] for HV GPO0/1. When this option is disabled, OCP circuit reacts immediately without deglitch time. The FETs will be disabled along t_{OCP2} time when the current decreases to a normal value. t_{OCP2} could be changed by setting the registers (HV GPO0 – registers [796:794], HV GPO1 – registers [804:802]). Overcurrent conditions are detected for both high- and low-side FETs. There is personal matrix input [61] for OCP_FAULT.

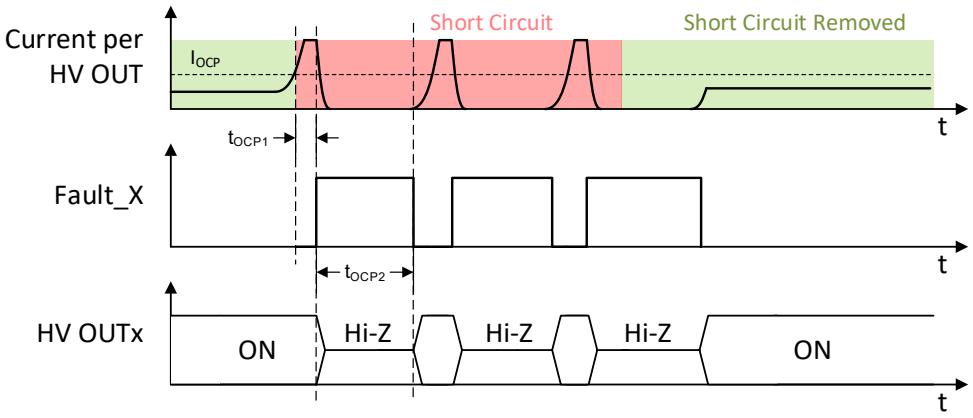


Figure 17. Overcurrent Protection Operation

7.3.4 Thermal Shutdown (TSD) and Thermal Considerations

If the die temperature exceeds safe limits TSD, all output FETs in each Full/Half Bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes. Note that TSD is active only during HV GPOs are wake. When all HV GPOs are in Power-down, TSD function is inactive. The SLG47104 has a special package optimized for better heat dissipation. All HV output pins and central plates should be thermally connected to copper traces or pads on the PCB for better heat dissipation. It is recommended to use thermal vias under the Ground and V_{DD} plates for the better thermal characteristic. TSD_FAULT signal is connected to Matrix Input [62]. TSD_FAULT signal is also present in FAULT signal.

7.3.5 Under-Voltage Lockout (UVLO)

When the voltage on the pin V_{DD2} is less than the V_{UVLO}, then the HV_GPOx outputs are disabled, Fault output is driven HIGH. When the voltage rises to the minimal V_{DD2} voltage, then the Fault output is driven LOW and work is restored.

UVLO can be enabled for V_{DD2} by registers [864:865] = 11.

7.4 High Voltage Outputs Typical Performance

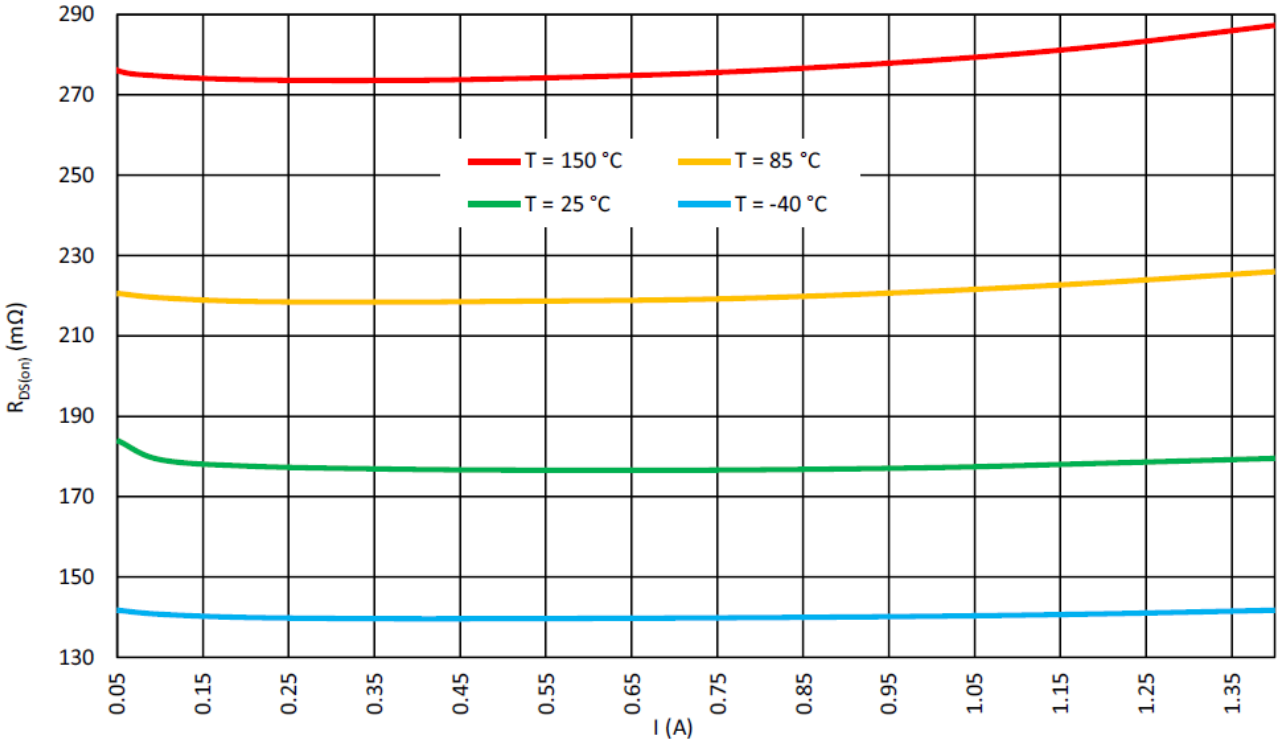


Figure 18. Full Bridge Typical Drain-Source High Side On-Resistance vs. Load Current at V_{DD} = 5.5 V, V_{DD2} = 5 V

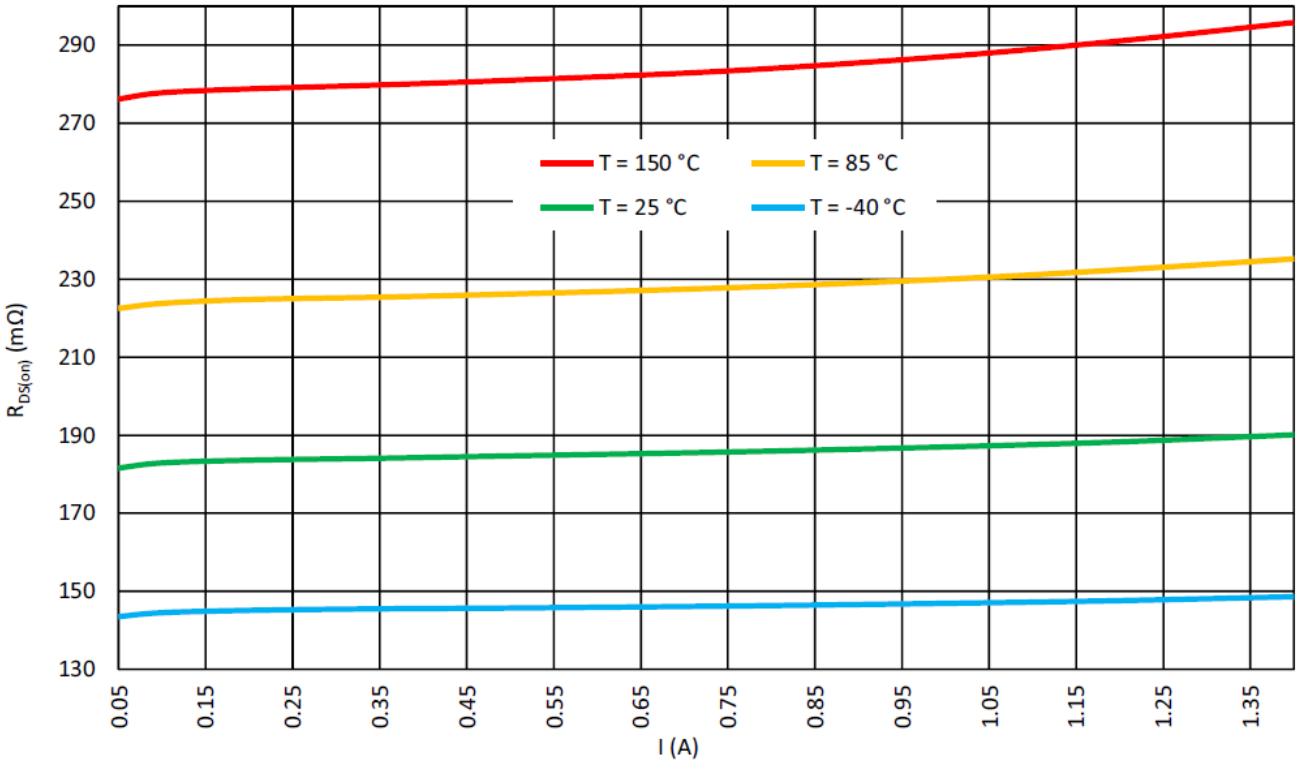


Figure 19. Full Bridge Typical Drain-Source Low Side On-Resistance vs. Load Current at V_{DD} = 5.5 V, V_{DD2} = 5 V

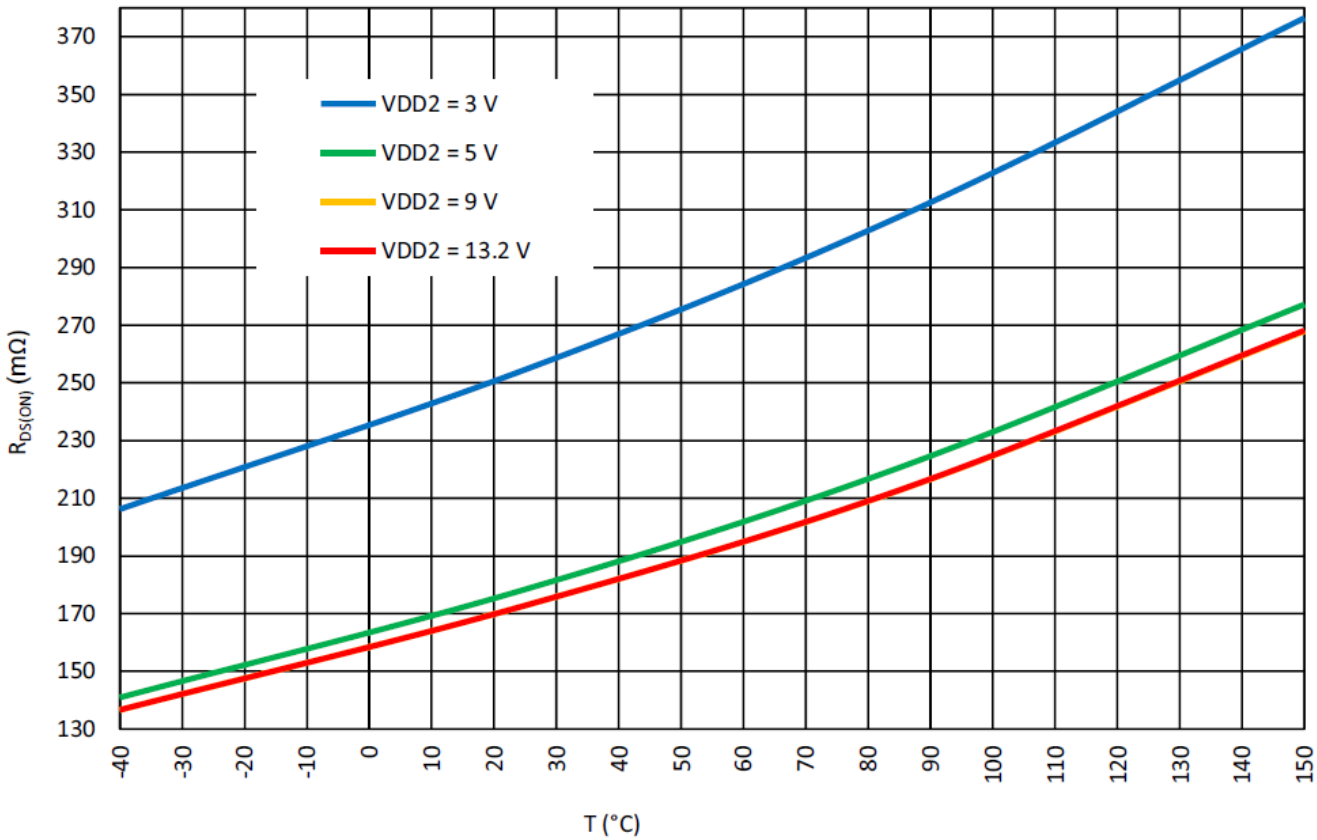


Figure 20. Full Bridge Typical Drain-Source High Side On-Resistance vs. Temperature at I_{LOAD} = 0.5 A, V_{DD} = 2.3 V

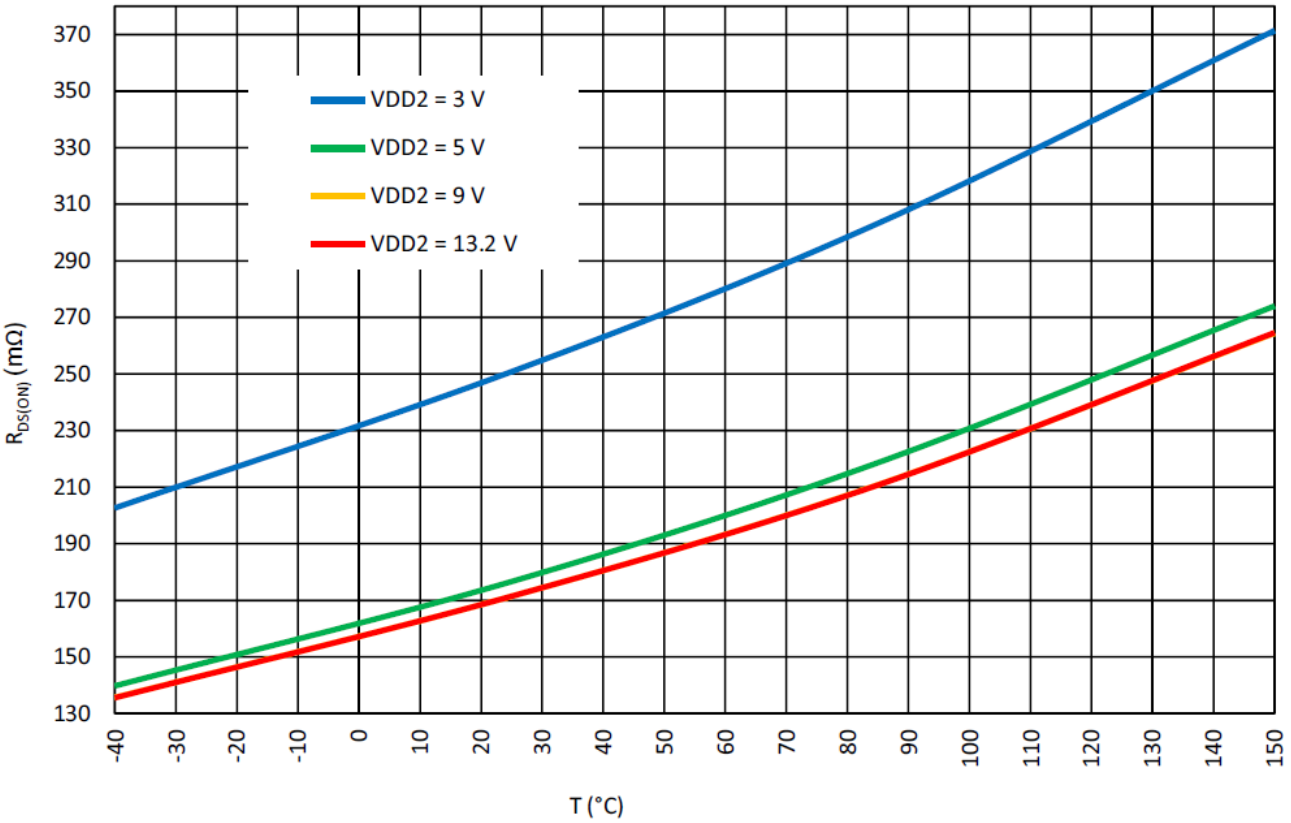


Figure 21. Full Bridge Typical Drain-Source High Side On-Resistance vs. Temperature at I_{LOAD} = 0.5 A, V_{DD} = 5.5 V

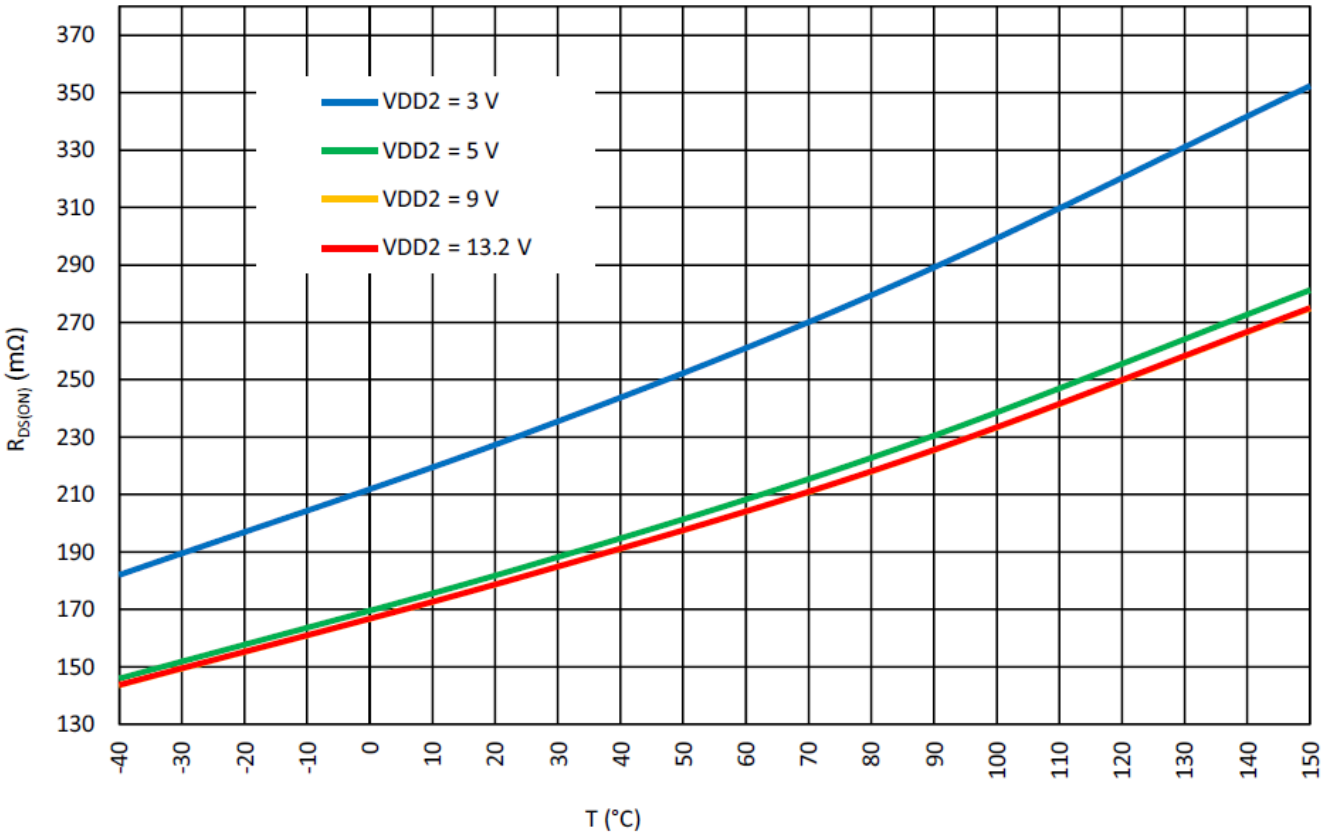


Figure 22. Full Bridge Typical Drain-Source Low Side On-Resistance vs. Temperature at I_{LOAD} = 0.5 A, V_{DD} = 2.3 V

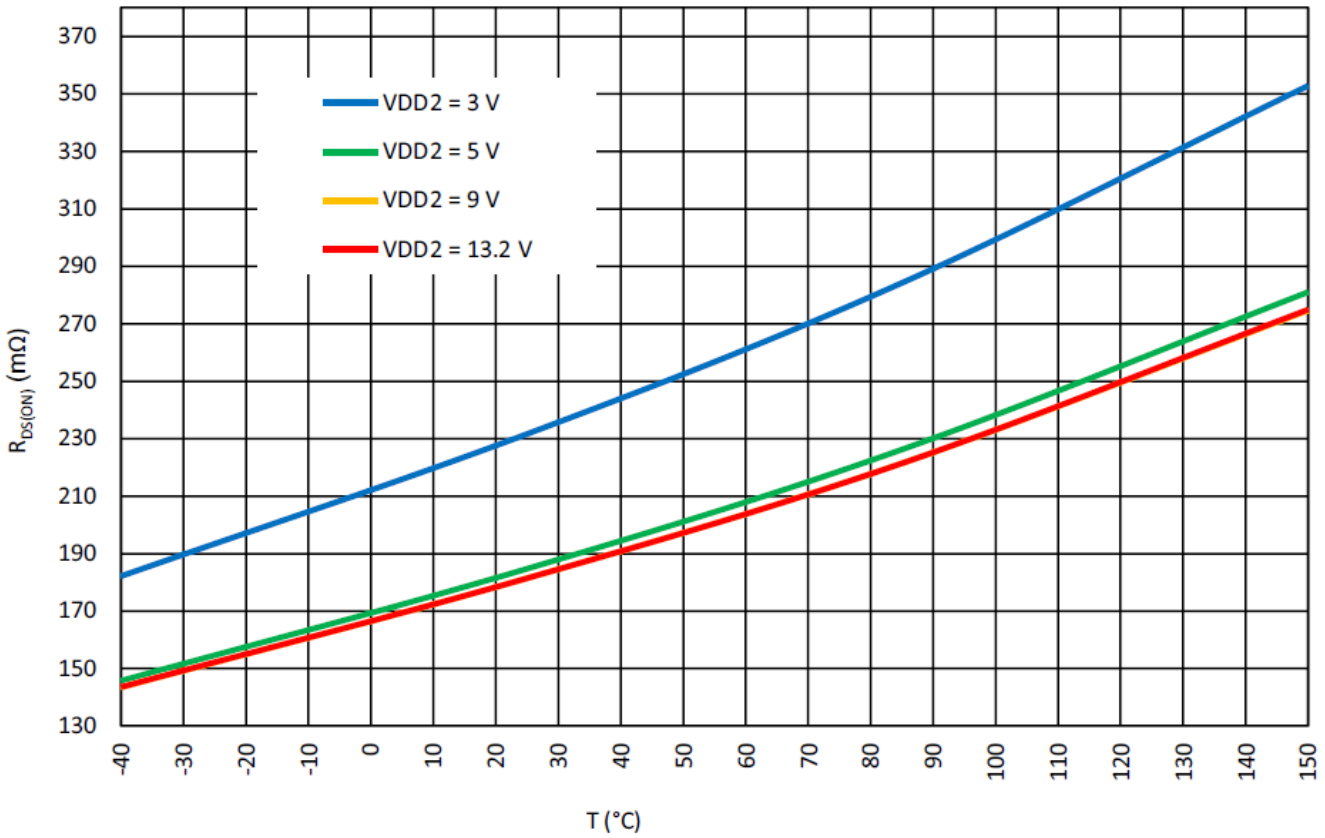


Figure 23. Full Bridge Typical Drain-Source Low Side On-Resistance vs. Temperature at I_{LOAD} = 0.5 A, V_{DD} = 5.5 V

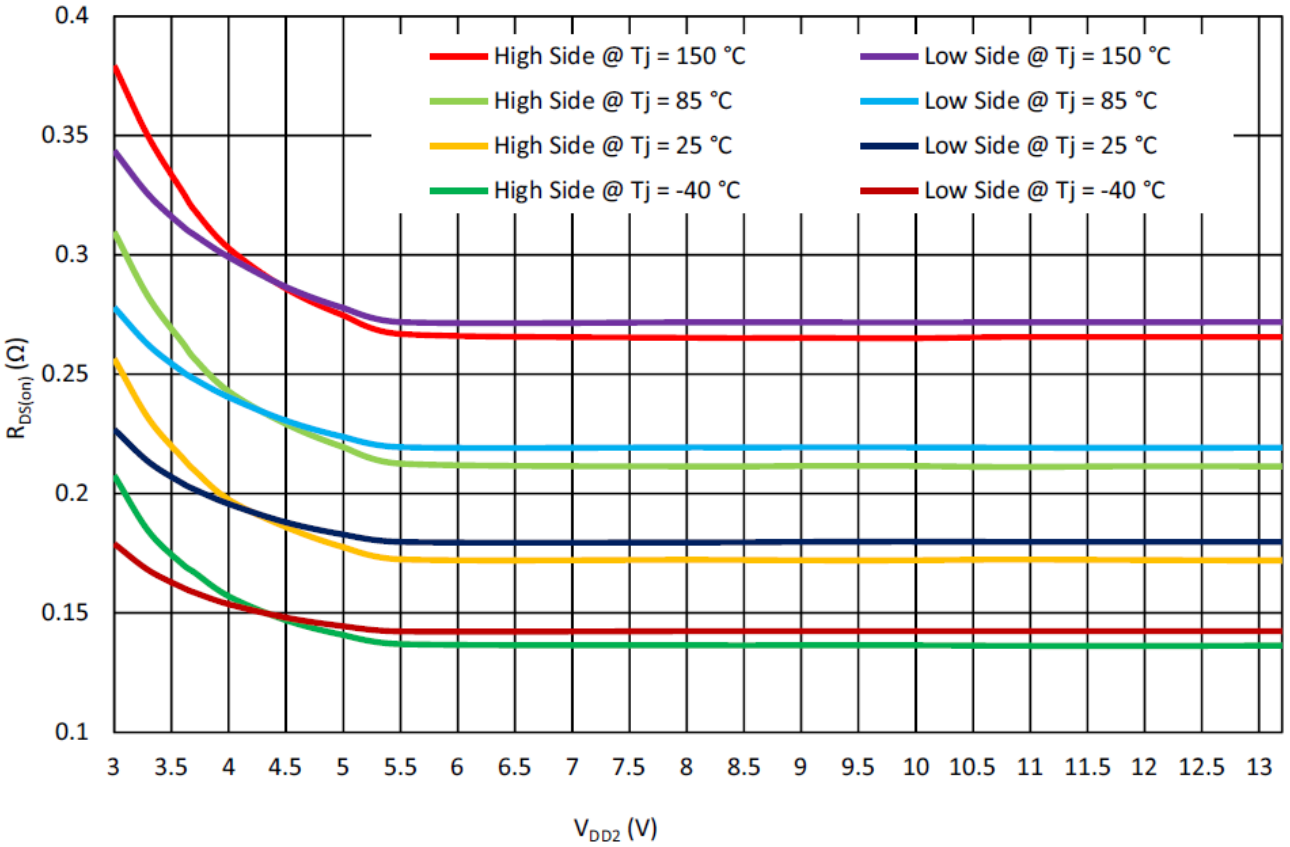


Figure 24. Full Bridge Typical Drain-Source On-Resistance vs. V_{DD2} at V_{DD} = 5.5 V, I_{LOAD} = 0.1 A

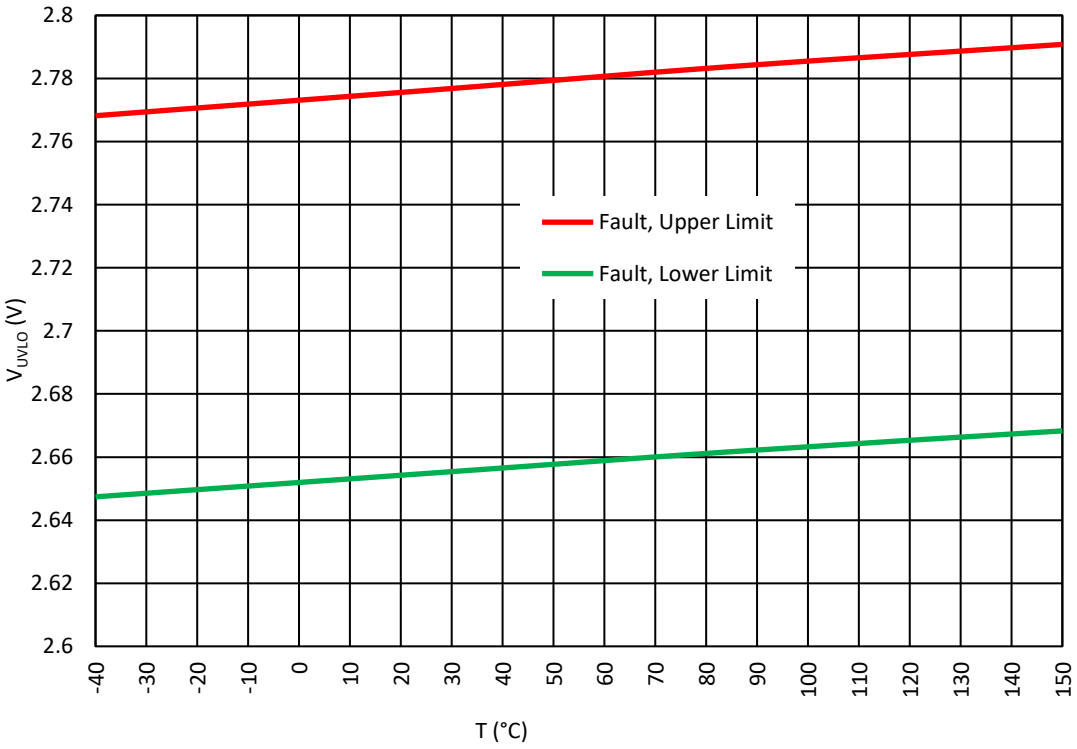


Figure 25. Half Bridge Under-voltage Lockout Value vs. Temperature at V_{DD} = 3.3 V

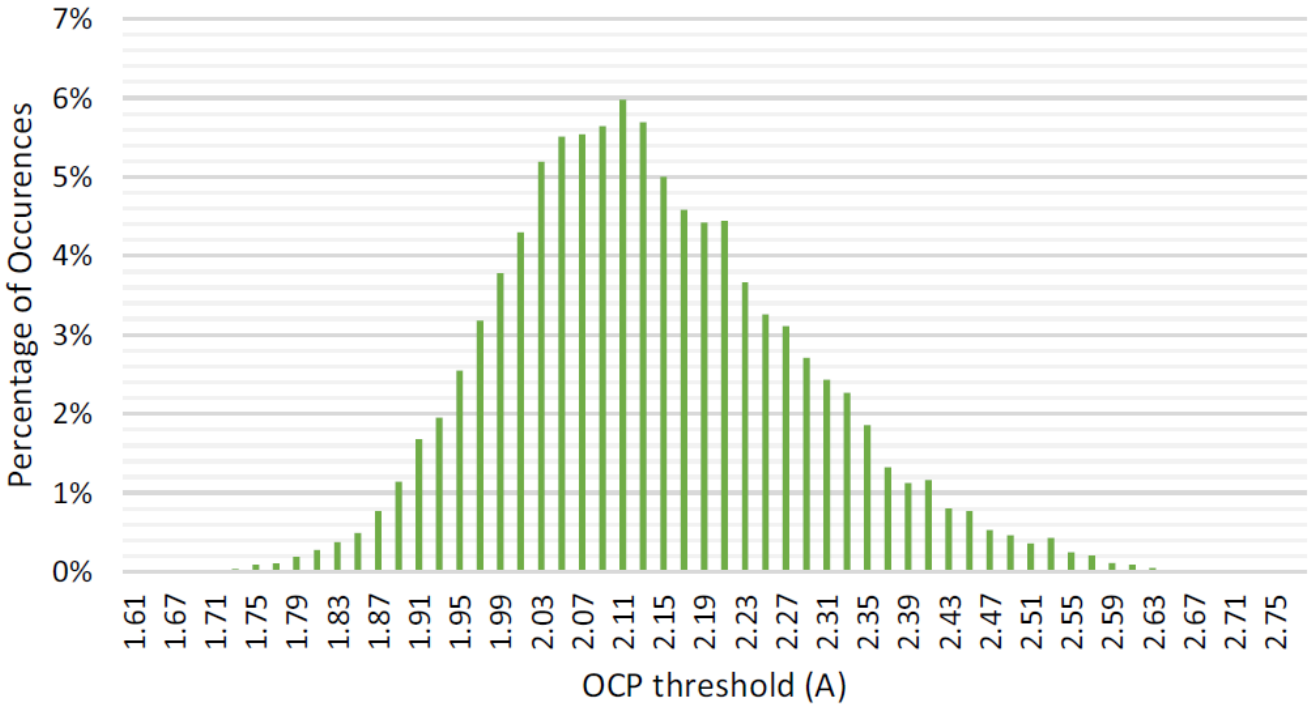


Figure 26. Full Bridge High Side OCP Threshold Distribution at V_{DD} = 2.3 V to 5.5 V, V_{DD2} = 3 V to 13.2 V, T_J = -40 °C to +150 °C

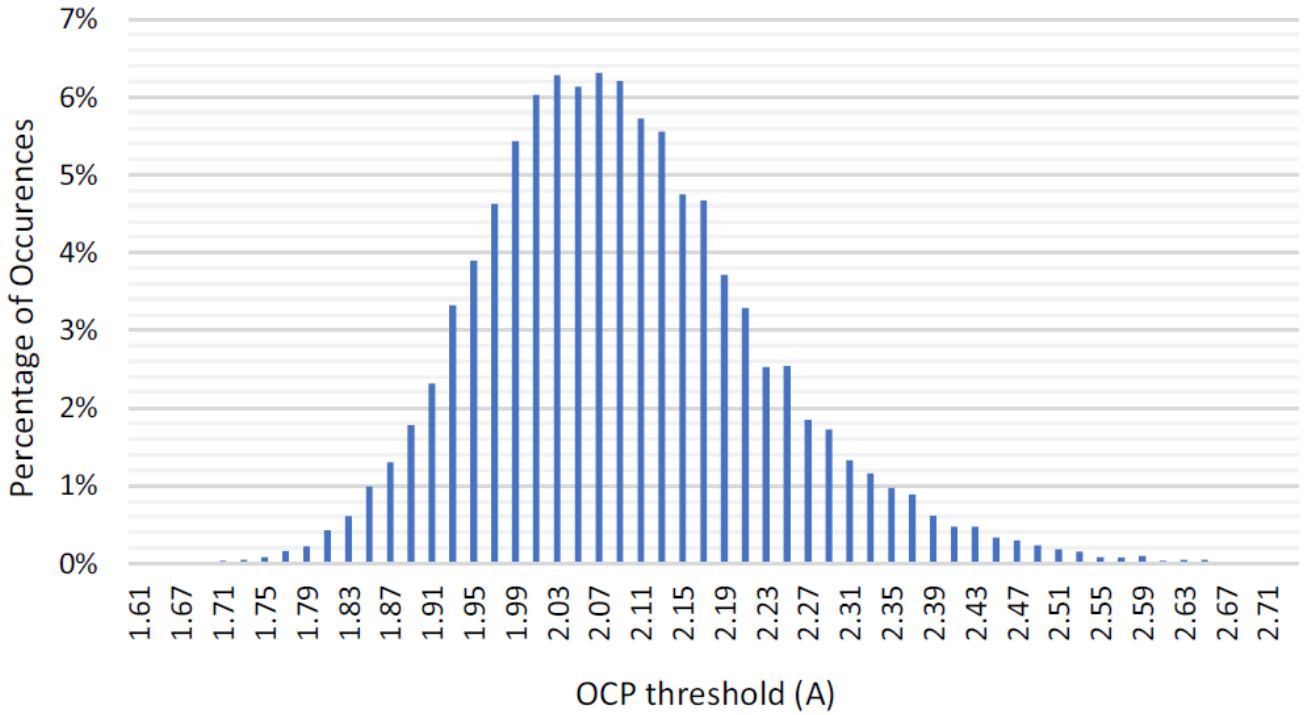


Figure 27. Full Bridge Low Side OCP Threshold Distribution at V_{DD} = 2.3 V to 5.5 V, V_{DD2} = 3 V to 13.2 V, T_J = -40 °C to +150 °C

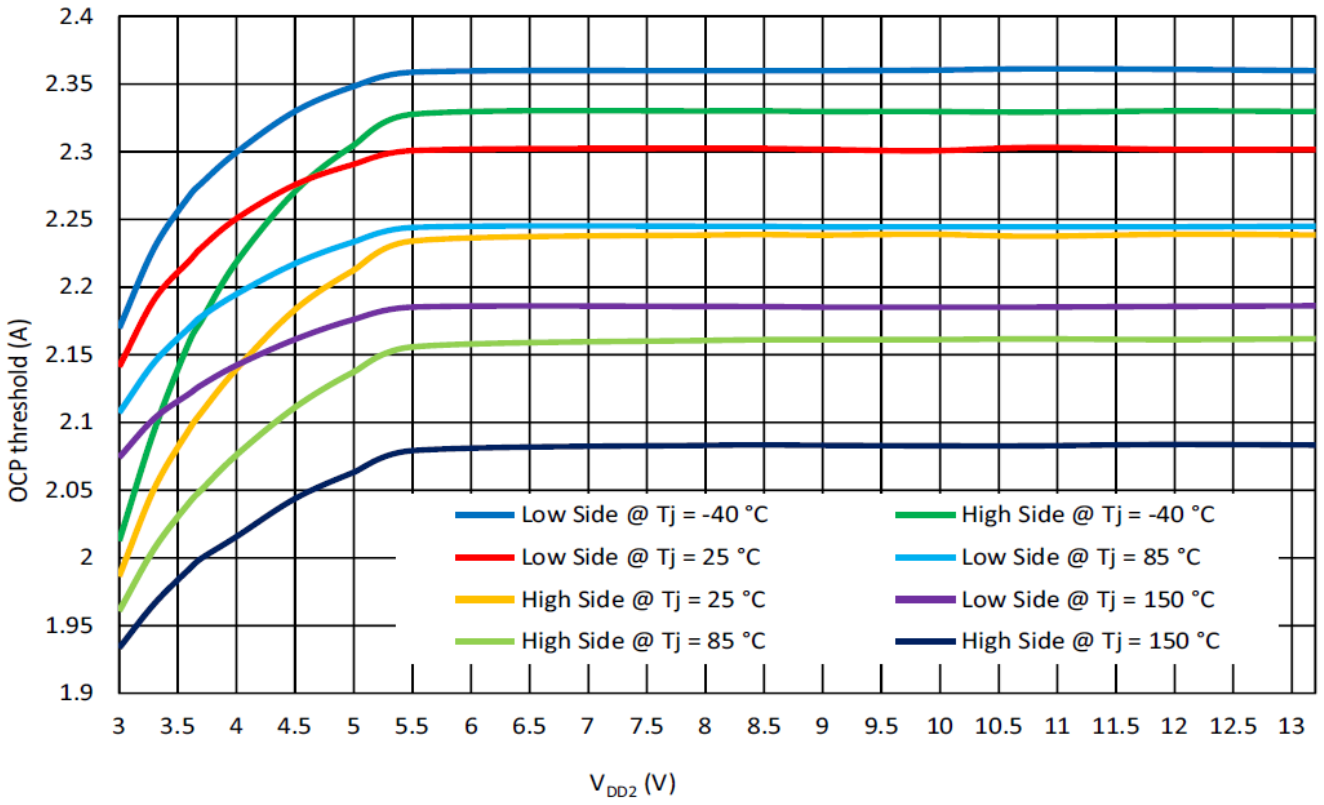


Figure 28. Full Bridge OCP Threshold vs. V_{DD2} at V_{DD} = 5.5 V

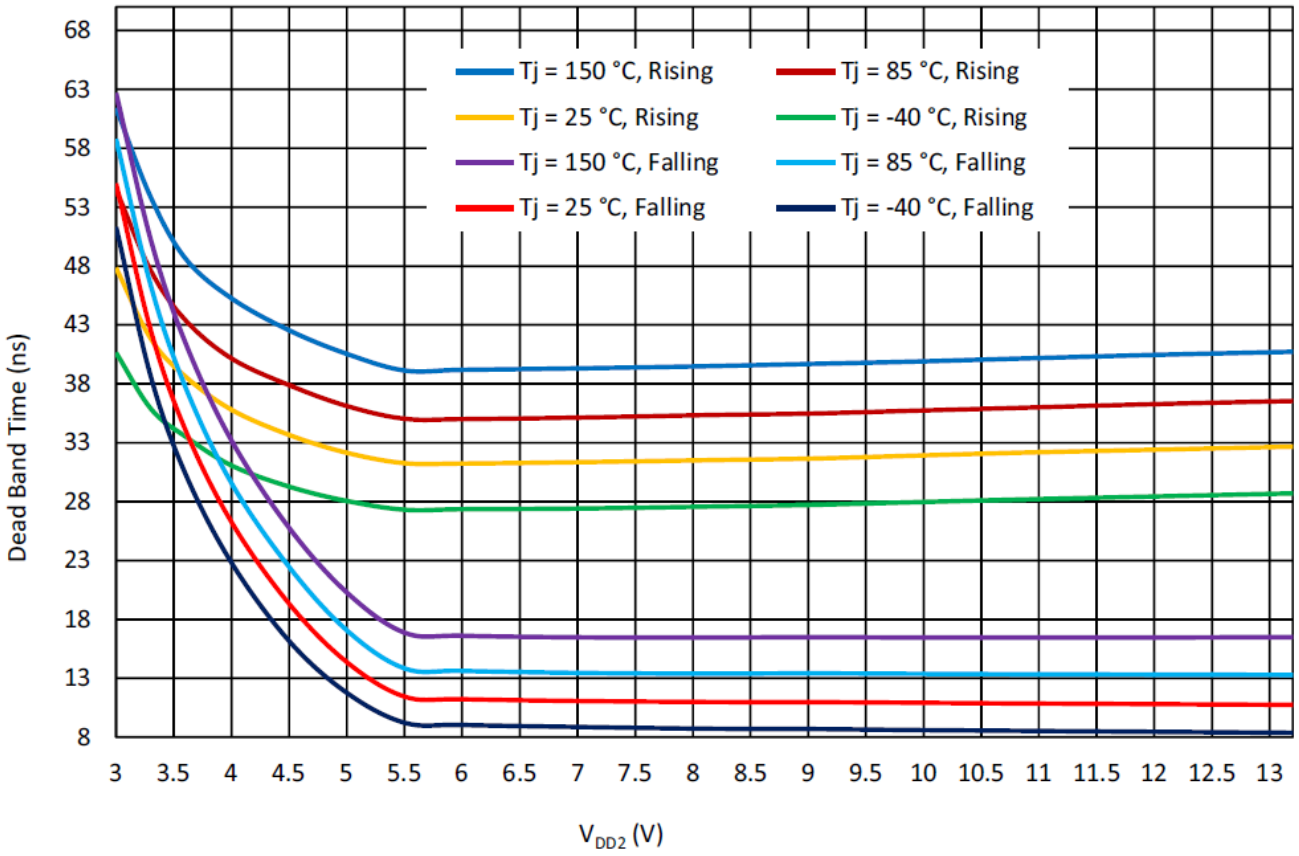


Figure 29. Half Bridge Dead Band Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, f = 50 kHz for Pre-Driver Mode

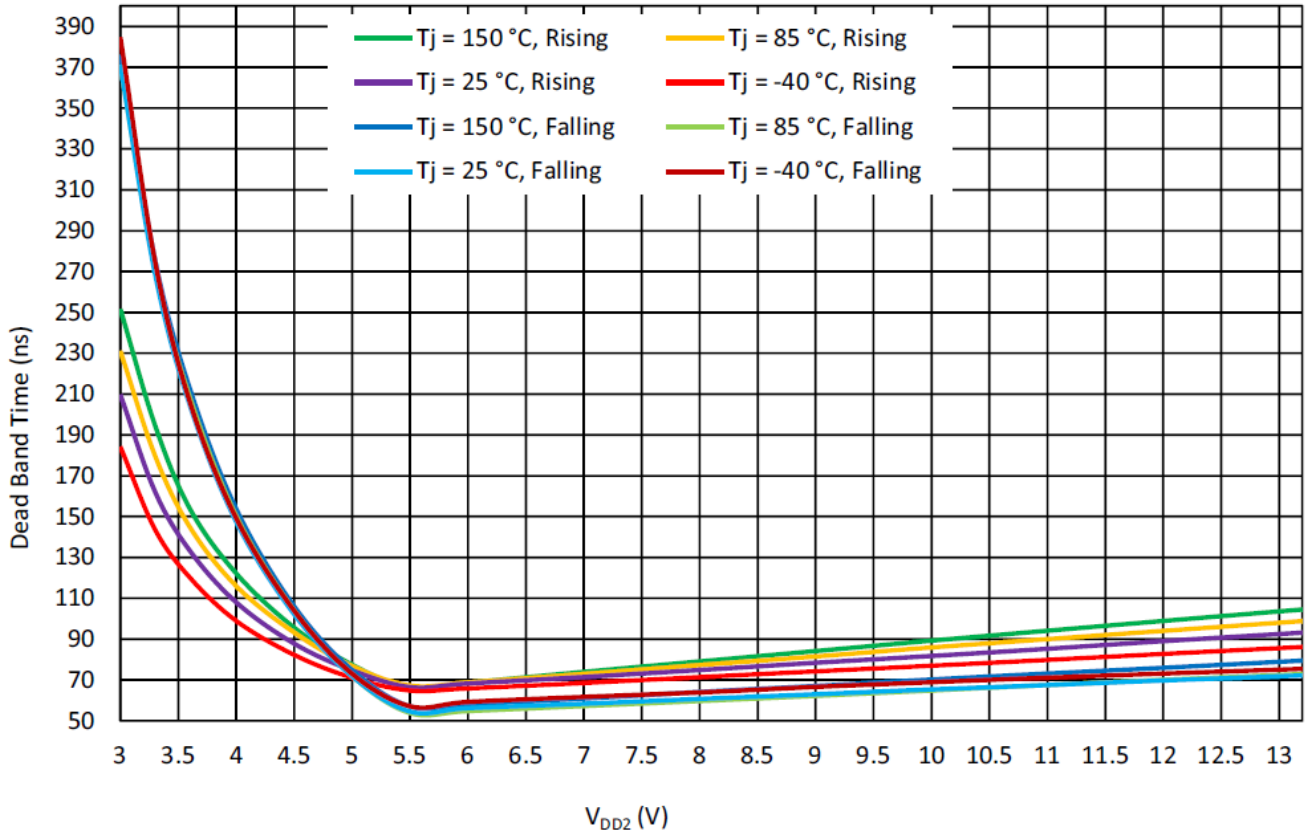


Figure 30. Half Bridge Dead Band Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, f = 50 kHz for Regular Mode

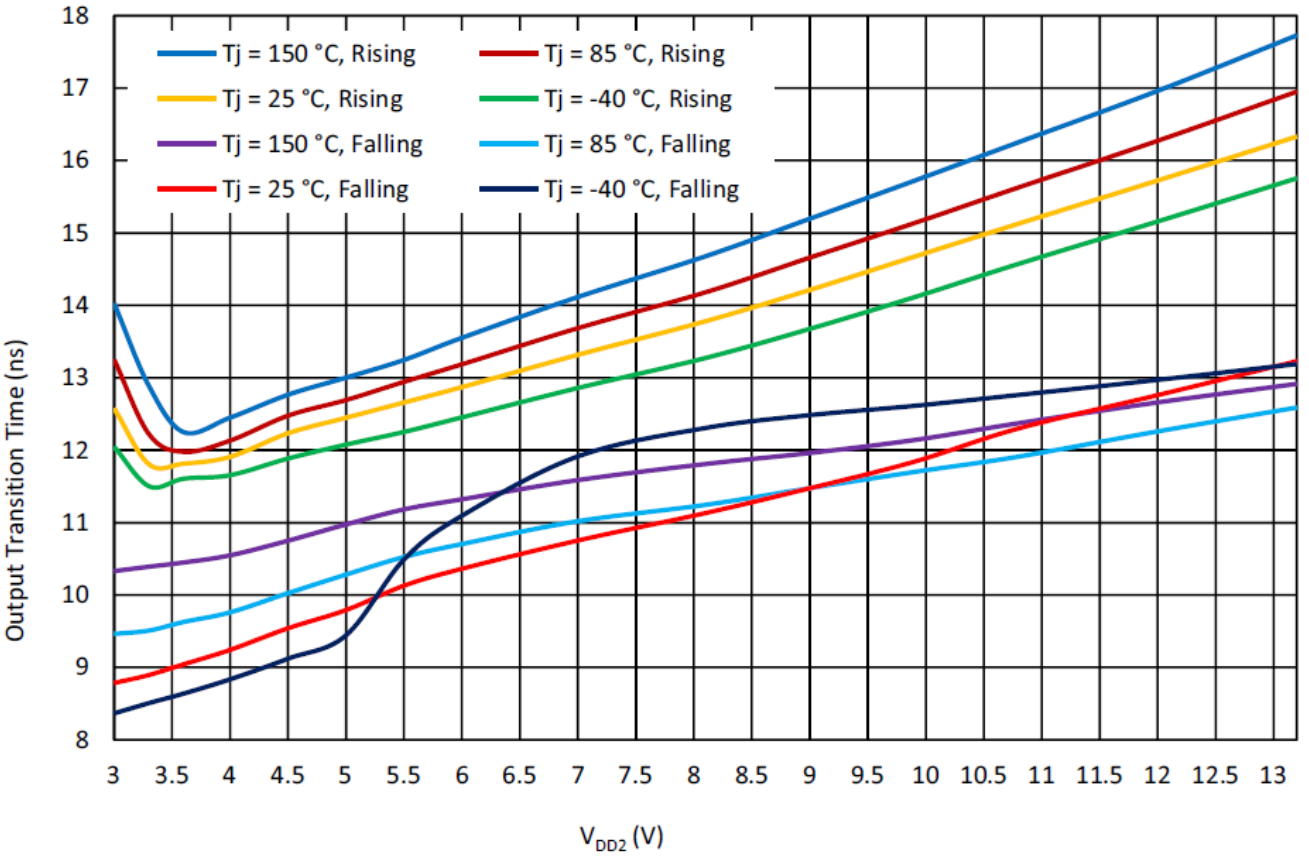


Figure 31. Half Bridge Output Transition Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, f = 50 kHz for Pre-Driver Mode

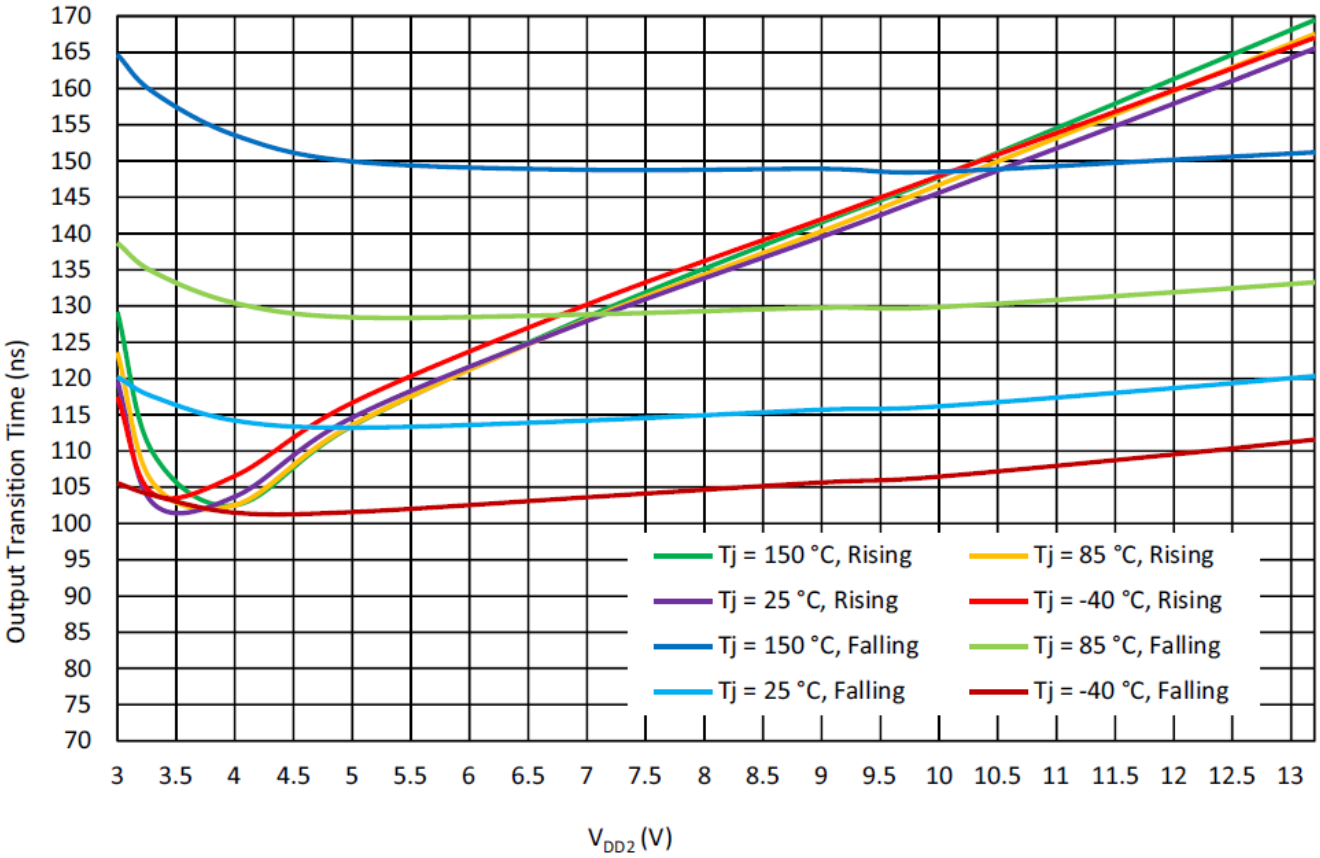


Figure 32. Half Bridge Output Transition Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, f = 50 kHz for Regular Mode

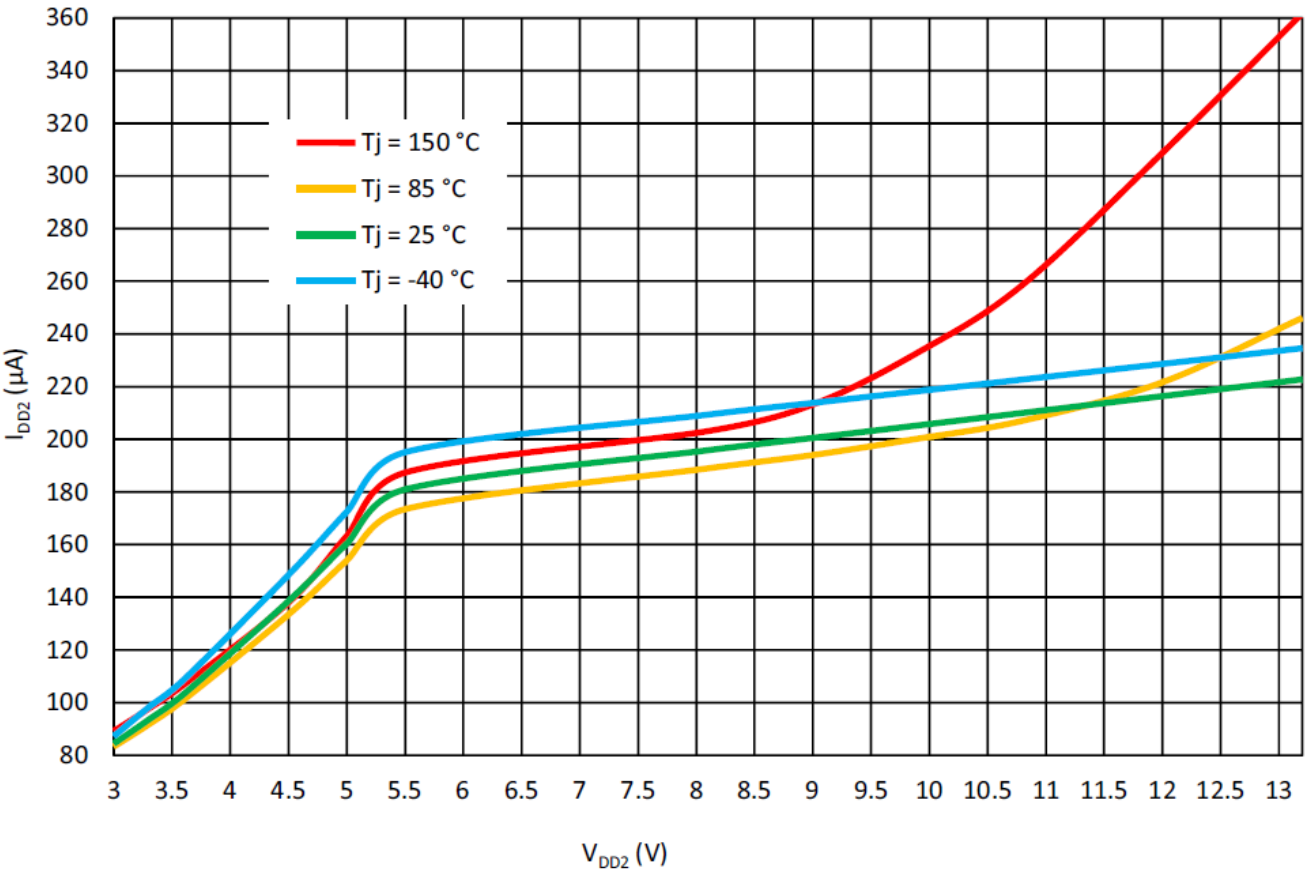


Figure 33. One Half Bridge I_{DD2} vs. V_{DD2} at V_{DD} = 5.5 V

8. Current Sense Comparator

There are one Current Sense Comparator macrocell in the SLG47104.

The Current CMP macrocell has a positive input signal that is connected to SENSE pin through Selectable Gain block. The options for Selectable Gain are 4x or 8x.

The Current CMP macrocell has a negative input signal that can be connected to static or dynamic variable V_{REF}. The static V_{REF} value is selected via registers. The dynamically changed V_{REF} values are selected with the help of the PWM block. In this case, 6-bit V_{REF} is selected by 6 Low Significant bits of Synchro Buffer, which is a part of the PWM block (detailed in section 12 Pulse Width Modulator Macrocell). For example, the Current Sense Comparator V_{REF} can be changed "on the flight" from 16-bytes Register File, which is connected to the Synchro Buffer by PWM block settings, and where user-defined V_{REF} values are stored. The V_{REF} values are switched Up or Down depending on the level of PWM macrocell Up/ Down input, each pulse on DUTY_CYCLE_CLK input.

Note 1: The PWM block can be active when 16-bytes Register File is used by Current Sense Comparator.

Note 2: The V_{REF} can be changed in a range from 32 mV to 2016 mV with 32 mV step.

During power-up, the Current Sense Comparator output will remain LOW, and then become valid 12.5 µs (max) after power-up signal goes high.

8.1 Current Sense Comparator Block Diagram

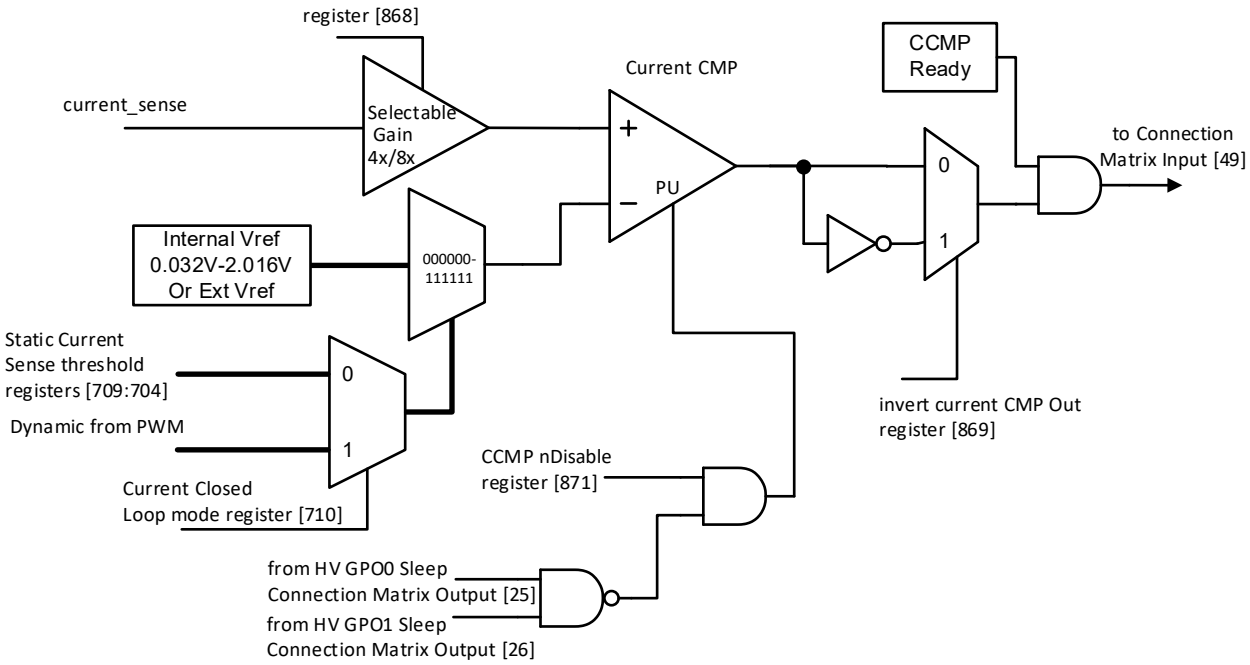


Figure 34. Current Sense Comparator Block Diagram

8.2 Current Regulation

To use the Current Regulation, it is necessary to connect sense-resistor between SENSE pin and ground. The resistor value is calculated by the formula:

$$I = \frac{V_{REF}}{R_{SENSE} \text{ x } Gain}$$

Where:

- I- Load Current (through controlled winding or resistive load) for selected V_{REF}
- V_{REF} - reference voltage of Current Sense Comparator, constant value, external source, or selectable value from Register File
- R_{SENSE} - resistance of the sense resistor
- Gain - selectable gain (4x or 8x, selectable by the register).

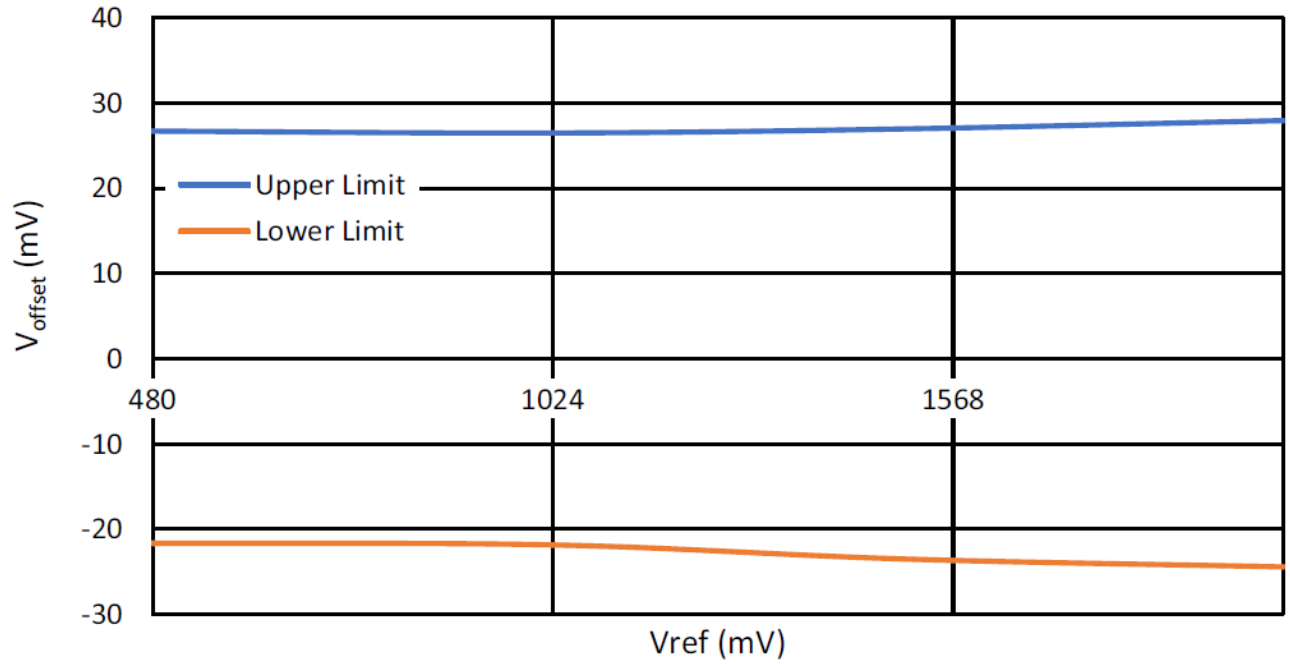
The reference voltage can be set statically or dynamically. For static reference voltage setting it is required to calculate R_{SENSE} for selected reference voltage and desired motor current.

For dynamic reference voltage setting it is required to calculate R_{SENSE} for the maximal user-defined reference voltage and maximal current via motor winding.

16 values in the Reg File can be used to determine the shape of motor current, for example, sine current.

DUTY_CYCLE_CLK input of PWM macrocell is used to switch to the next V_{REF} value, and UP/DOWN input of PWM macrocell selects the direction of V_{REF} change (next or previous V_{REF} value). For more detailed description of Reg File see section 12 Pulse Width Modulator Macrocell.

8.3 Current Sense Comparator Typical Performance



T = -40 °C to +150 °C, V_{DD} = 2.3 V to 5.5 V, Gain = 4

Figure 35. Input Offset Voltage Error vs. V_{REF} for CCMP (including Amplifier Offset and ACMP Offset)

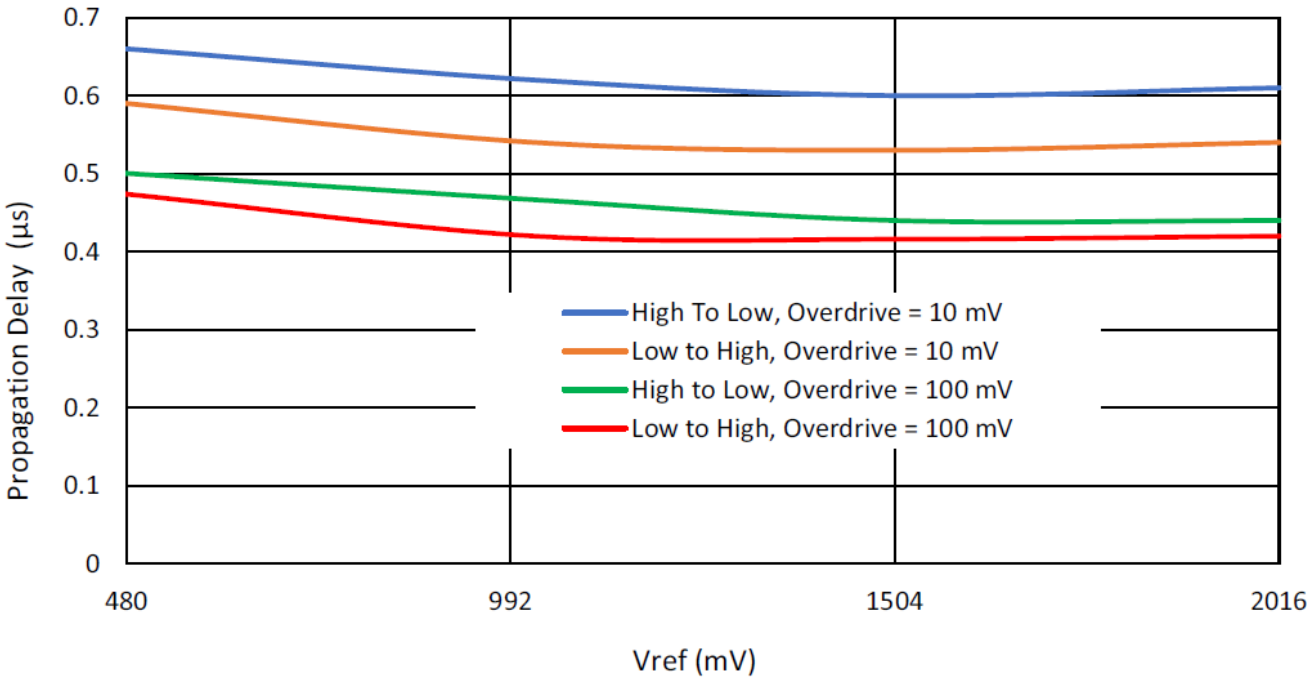


Figure 36. Typical Propagation Delay vs. V_{REF} for CCMP at T = +25 °C, at V_{DD} = 2.3 V to 5.5 V, Gain = 4

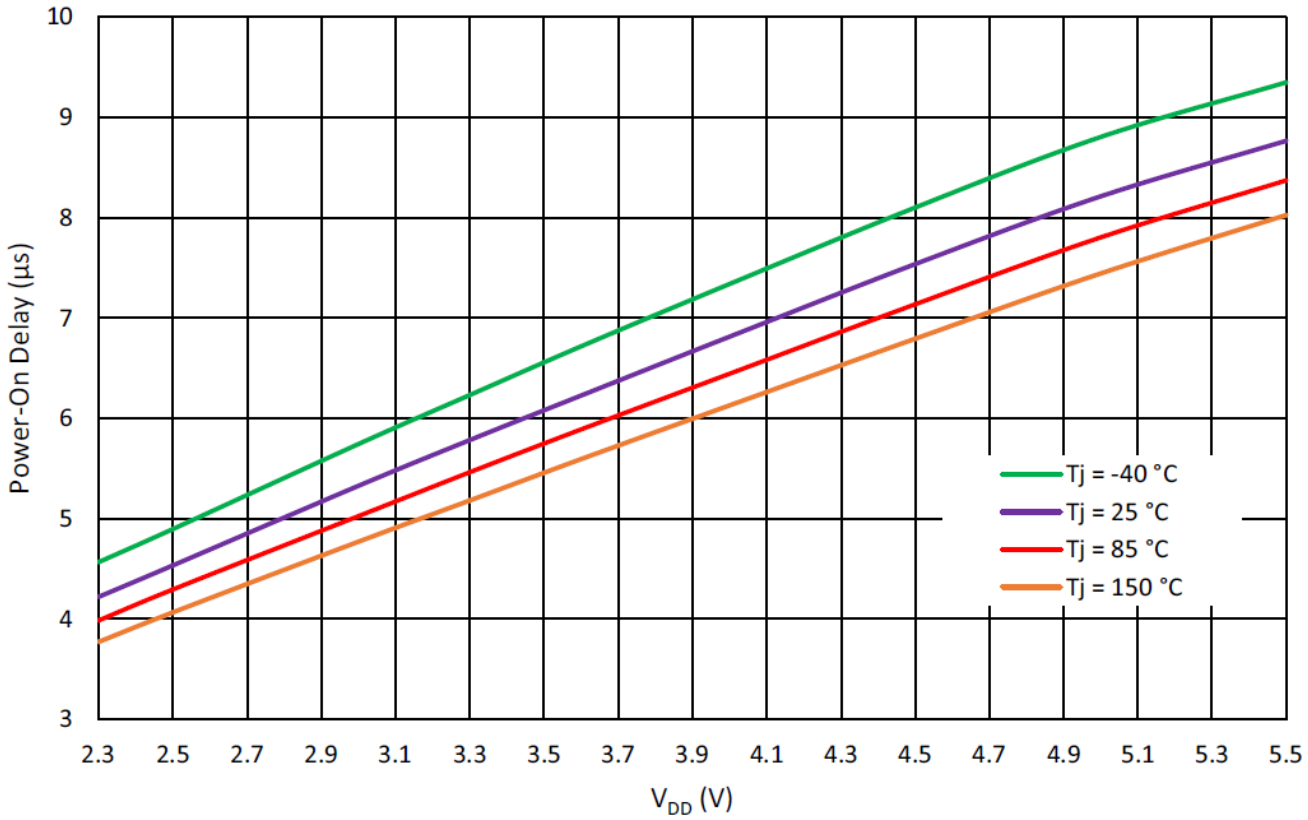


Figure 37. CCMP Power-On Delay vs. V_{DD} (BG is Forced On)

9. Connection Matrix

The Connection Matrix in the SLG47104 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one time programmable (OTP) NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG47104 has a specific digital bit code assigned to it, that is either set to active “High”, or inactive “Low”, based on the design that is created. Once the 2048 register bits within the SLG47104 are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 94 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

Matrix Input Signal Functions	№
GND	0
LUT2_0/DFF0 output	1
LUT2_1/DFF1 output	2
Reserved	3
⋮	⋮
TSD_FAULT	62
V_{DD}	63

Matrix Inputs / Matrix Outputs	№	0	1	2	------	93
	Registers	Reg [5:0]	Reg [11:6]	Reg [17:12]	------	Reg [563:558]
	Functions	GPIO0 Digital Output	GPIO0 Digital Output OE	GPIO1 Digital Output	------	BG Power-down from the matrix

Figure 38. Connection Matrix

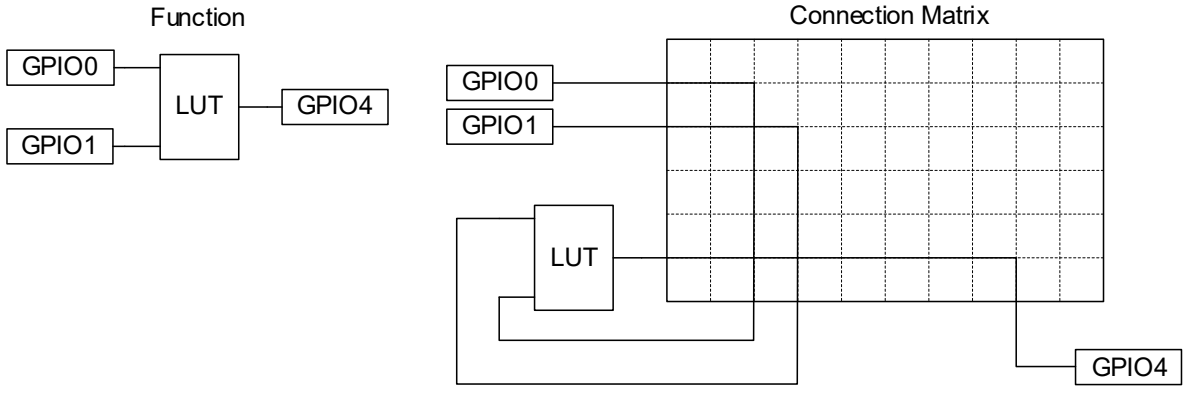


Figure 39. Connection Matrix Example

9.1 Matrix Input Table

Table 12. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	2-bit LUT0/DFF0 output	0	0	0	0	0	1
2	2-bit LUT1/DFF1 output	0	0	0	0	1	0
3	Reserved	0	0	0	0	1	1
4	2-bit LUT2/PGen output	0	0	0	1	0	0
5	3-bit LUT0/DFF2 output	0	0	0	1	0	1
6	3-bit LUT1/DFF3/Chopper output	0	0	0	1	1	0
7	Reserved	0	0	0	1	1	1
8	Reserved	0	0	1	0	0	0
9	3-bit LUT2/DFF4 output	0	0	1	0	0	1
10	3-bit LUT3/DFF5 output	0	0	1	0	1	0
11	4-bit LUT0/DFF6 output	0	0	1	0	1	1
12	3-bit LUT4/PD/RIPP CNT output0	0	0	1	1	0	0
13	3-bit LUT4/PD/RIPP CNT output1	0	0	1	1	0	1
14	3-bit LUT4/PD/RIPP CNT output2	0	0	1	1	1	0
15	Reserved	0	0	1	1	1	1
16	MULTFUNC_8BIT_1: DLY_CNT_OUT	0	1	0	0	0	0
17	MULTFUNC_8BIT_2: DLY_CNT_OUT	0	1	0	0	0	1
18	Reserved	0	1	0	0	1	0
19	Reserved	0	1	0	0	1	1
20	MULTFUNC_8BIT_1: LUT3_DFF_OUT	0	1	0	1	0	0
21	MULTFUNC_8BIT_2: LUT3_DFF_OUT	0	1	0	1	0	1
22	Reserved	0	1	0	1	1	0
23	Reserved	0	1	0	1	1	1
24	MULTFUNC_16BIT_0: DLY_CNT_OUT	0	1	1	0	0	0
25	MULTFUNC_16BIT_0: LUT4_DFF_OUT	0	1	1	0	0	1
26	GPIO0 Digital Input	0	1	1	0	1	0
27	GPI Digital Input	0	1	1	0	1	1
28	GPIO1 Digital Input	0	1	1	1	0	0
29	GPIO4 Digital Input	0	1	1	1	0	1
30	GPIO5 Digital Input	0	1	1	1	1	0
31	GPIO6 Digital Input	0	1	1	1	1	1
32	GPIO2 digital input or I^2C_virtual_0 Input	1	0	0	0	0	0

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
33	GPIO3 digital input or I²C_virtual_1 Input	1	0	0	0	0	1
34	I²C_virtual_2 Input	1	0	0	0	1	0
35	I²C_virtual_3 Input	1	0	0	0	1	1
36	I²C_virtual_4 Input	1	0	0	1	0	0
37	I²C_virtual_5 Input	1	0	0	1	0	1
38	I²C_virtual_6 Input	1	0	0	1	1	0
39	I²C_virtual_7 Input	1	0	0	1	1	1
40	Reserved	1	0	1	0	0	0
41	Reserved	1	0	1	0	0	1
42	PWM_OUT+	1	0	1	0	1	0
43	PWM_OUT-	1	0	1	0	1	1
44	Reserved	1	0	1	1	0	0
45	Reserved	1	0	1	1	0	1
46	ACMPH_OUT	1	0	1	1	1	0
47	Reserved	1	0	1	1	1	1
48	Reserved	1	1	0	0	0	0
49	CurrentSenseComp_OUT	1	1	0	0	0	1
50	Reserved	1	1	0	0	1	0
51	FAULT	1	1	0	0	1	1
52	EDET_FILTER_OUT	1	1	0	1	0	0
53	Oscillator1 (25 MHz) output	1	1	0	1	0	1
54	Flex-Divider output	1	1	0	1	1	0
55	Oscillator0 (2.048 kHz) output 0	1	1	0	1	1	1
56	Oscillator0 (2.048 kHz) output 1	1	1	1	0	0	0
57	POR OUT	1	1	1	0	0	1
58	Reserved	1	1	1	0	1	0
59	PWM_PERIOD	1	1	1	0	1	1
60	Reserved	1	1	1	1	0	0
61	OCP_FAULT	1	1	1	1	0	1
62	TSD_FAULT	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

9.2 Matrix Output Table

Table 13. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	GPIO0 Digital Output	0
[11:6]	GPIO0 Digital Output OE	1
[17:12]	GPIO1 Digital Output	2
[23:18]	GPIO1 Digital Output OE	3
[29:24]	GPIO2 Digital Output	4
[35:30]	GPIO3 Digital Output	5
[41:36]	GPIO4 Digital Output	6
[47:42]	GPIO4 Digital Output OE	7
[53:48]	GPIO5 Digital Output	8
[59:54]	GPIO5 Digital Output OE	9
[65:60]	GPIO6 Digital Output	10
[71:66]	GPIO6 Digital Output OE	11
[77:72]	Reserved	12
[83:78]	Reserved	13
[89:84]	Reserved	14
[95:90]	Reserved	15
[101:96]	HV GPO0 Digital Output	16
[107:102]	HV GPO0 Digital Output OE	17
[113:108]	HV GPO1 Digital Output	18
[119:114]	HV GPO1 Digital Output OE	19
[125:120]	Reserved	20
[131:126]	Reserved	21
[137:132]	Reserved	22
[143:138]	Reserved	23
[149:144]	Reserved	24
[155:150]	HV GPO0 SLEEP	25
[161:156]	HV GPO1 SLEEP	26
[167:162]	IN0 of 2-bit LUT0 or Clock Input of DFF0	27
[173:168]	IN1 of 2-bit LUT0 or Data Input of DFF0	28
[179:174]	IN0 of 2-bit LUT2 or Clock Input of PGen	29
[185:180]	IN1 of 2-bit LUT2 or nRST of PGen	30
[191:186]	IN0 of 2-bit LUT1 or Clock Input of DFF1	31
[197:192]	IN1 of 2-bit LUT1 or Data Input of DFF1	32
[203:198]	Reserved	33

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[209:204]	Reserved	34
[215:210]	IN0 of 3-bit LUT0 or Clock Input of DFF2	35
[221:216]	IN1 of 3-bit LUT0 or Data Input of DFF2	36
[227:222]	IN2 of 3-bit LUT0 or nRST(nSET) of DFF2	37
[233:228]	IN0 of 3-bit LUT1 or Clock Input of DFF3	38
[239:234]	IN1 of 3-bit LUT1 or Data Input of DFF3	39
[245:240]	IN2 of 3-bit LUT1 or nRST(nSET) of DFF3	40
[251:246]	Reserved	41
[257:252]	Reserved	42
[263:258]	Reserved	43
[269:264]	Reserved	44
[275:270]	Reserved	45
[281:276]	Reserved	46
[287:282]	IN0 of 3-bit LUT2 or Clock Input of DFF4	47
[293:288]	IN1 of 3-bit LUT2 or Data Input of DFF4	48
[299:294]	IN2 of 3-bit LUT2 or nRST(nSET) of DFF4	49
[305:300]	IN0 of 3-bit LUT3 or Clock Input of DFF5	50
[311:306]	IN1 of 3-bit LUT3 or Data Input of DFF5	51
[317:312]	IN2 of 3-bit LUT3 or nRST(nSET) of DFF5	52
[323:318]	IN0 of 3-bit LUT4 or Input of Pipe Delay or UP Signal of RIPP CNT	53
[329:324]	IN1 of 3-bit LUT4 or nRST of Pipe Delay or nSET of RIPP CNT	54
[335:330]	IN2 of 3-bit LUT4 or Clock of Pipe/RIPP_CNT	55
[341:336]	IN0 of 4-bit LUT0 or Clock Input of DFF6	56
[347:342]	IN1 of 4-bit LUT0 or Data Input of DFF6	57
[353:348]	IN2 of 4-bit LUT0 or nRST(nSET) of DFF6	58
[359:354]	IN3 of 4-bit LUT0	59
[365:360]	MULTFUNC_8BIT_1: IN0 of 3-bit LUT5 or Clock Input of DFF7, Delay1 Input (or Counter1 nRST Input)	60
[371:366]	MULTFUNC_8BIT_1: IN1 of 3-bit LUT5 or nRST (nSET) of DFF7, Delay1 Input (or Counter1 nRST Input) or Delay/Counter1 External Clock Source	61
[377:372]	MULTFUNC_8BIT_1: IN2 of 3-bit LUT5 or Data Input of DFF7, Delay1 Input (or Counter1 nRST Input)	62
[383:378]	MULTFUNC_8BIT_2: IN0 of 3-bit LUT6 or Clock Input of DFF8, Delay2 Input (or Counte2 nRST Input)	63
[389:384]	MULTFUNC_8BIT_2: IN1 of 3-bit LUT6 or nRST (nSET) of DFF8, Delay2 Input (or Counter2 nRST Input) or Delay/Counter2 External Clock Source	64
[395:390]	MULTFUNC_8BIT_2: IN2 of 3-bit LUT6 or Data Input of DFF8, Delay2 Input (or Counter2 nRST Input)	65

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[401:396]	Reserved	66
[407:402]	Reserved	67
[413:408]	Reserved	68
[419:414]	Reserved	69
[425:420]	Reserved	70
[431:426]	Reserved	71
[437:432]	MULTFUNC_16BIT_0: IN0 of 4-bit LUT1 or Clock Input of DFF9; Delay0 Input (or Counter0 RST/SET Input)	72
[443:438]	MULTFUNC_16BIT_0: IN1 of 4-bit LUT1 or nRST of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source	73
[449:444]	MULTFUNC_16BIT_0: IN2 of 4-bit LUT1 or nSET of DFF9 or KEEP Input of FSM0 or External Clock Input of Delay0 (or Counter0)	74
[455:450]	MULTFUNC_16BIT_0: IN3 of 4-bit LUT1 or Data Input of DFF9; Delay0 Input (or Counter0 nRST Input) or UP Input of FSM0	75
[461:456]	Reserved	76
[467:462]	Reserved	77
[473:468]	Reserved	78
[479:474]	Reserved	79
[485:480]	Reserved	80
[491:486]	PWM_UP/DOWN	81
[497:492]	PWM_KEEP/STOP	82
[503:498]	PWM_DUTY_CYCLE_CNT	83
[509:504]	PWM_EXT_CLK	84
[515:510]	PWM_RESET/SET	85
[521:516]	pd of ACMPH from the matrix	86
[527:522]	Reserved	87
[533:528]	Filter/Edge detect input	88
[539:534]	Reserved	89
[545:540]	OSC0 ENABLE from matrix	90
[551:546]	OSC1 ENABLE from matrix	91
[557:552]	VREF PD from matrix	92
[563:558]	BG Power-down from the matrix	93

9.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x4C (76).

An I²C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup) or the values from a previous write command (if that has happened).

Table 14. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Address (d)
32	I²C_virtual_0 Input	[608]
33	I²C_virtual_1 Input	[609]
34	I²C_virtual_2 Input	[610]
35	I²C_virtual_3 Input	[611]
36	I²C_virtual_4 Input	[612]
37	I²C_virtual_5 Input	[613]
38	I²C_virtual_6 Input	[614]
39	I²C_virtual_7 Input	[615]

9.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time it is possible to read the state of each of the macrocell outputs as a register value via I²C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I²C addresses for reading these register values are registers [639:576]. Write commands to the same register values will be ignored (with the exception of the Virtual Input register bits at registers [615:608]).

10. Combination Function Macrocells

The SLG47104 has nine combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Two macrocells that can serve as either 2-bit LUT or as D Flip-Flop.
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen).
- Three macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input.
- One macrocell that can serve as either 3-bit LUTs, as D Flip-Flops with Set/Reset Input or as PWM Chopper.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter.
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input.

Inputs/Outputs for the combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

10.1 2-bit LUT or D Flip-Flop Macrocells

There are two macrocells that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2- bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
- LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

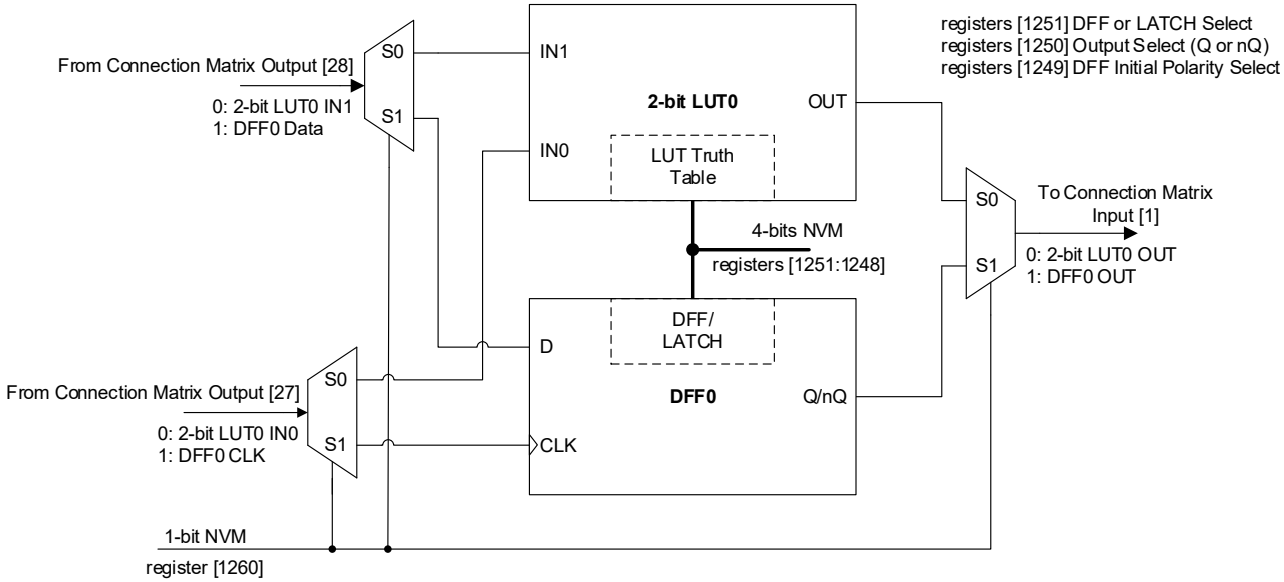


Figure 40. 2-bit LUT0 or DFF0

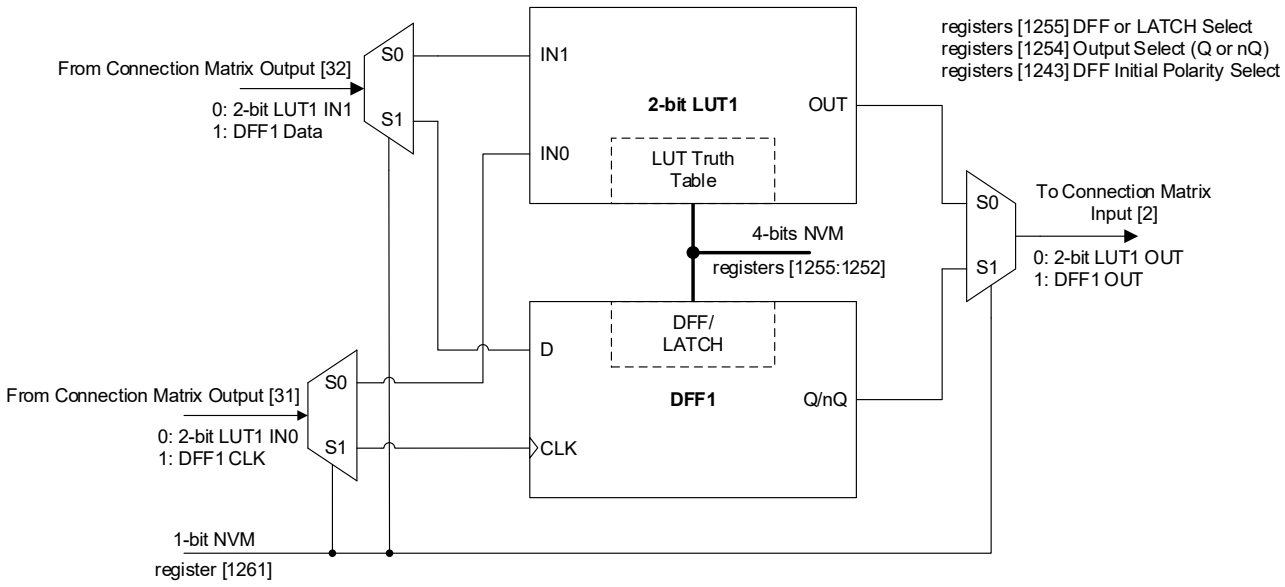


Figure 41. 2-bit LUT1 or DFF1

10.1.1 2-bit LUT or D Flip-Flop Macrocell Used as 2-bit LUT

Table 15. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1248]	LSB
0	1	register [1249]	
1	0	register [1250]	
1	1	register [1251]	MSB

Table 16. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1252]	LSB
0	1	register [1253]	
1	0	register [1254]	
1	1	register [1255]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT0 is defined by registers [1251:1248]
- 2-bit LUT1 is defined by registers [1255:1252]

Table 17 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 17. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0

Function	MSB			LSB
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

10.1.2 Initial Polarity Operations

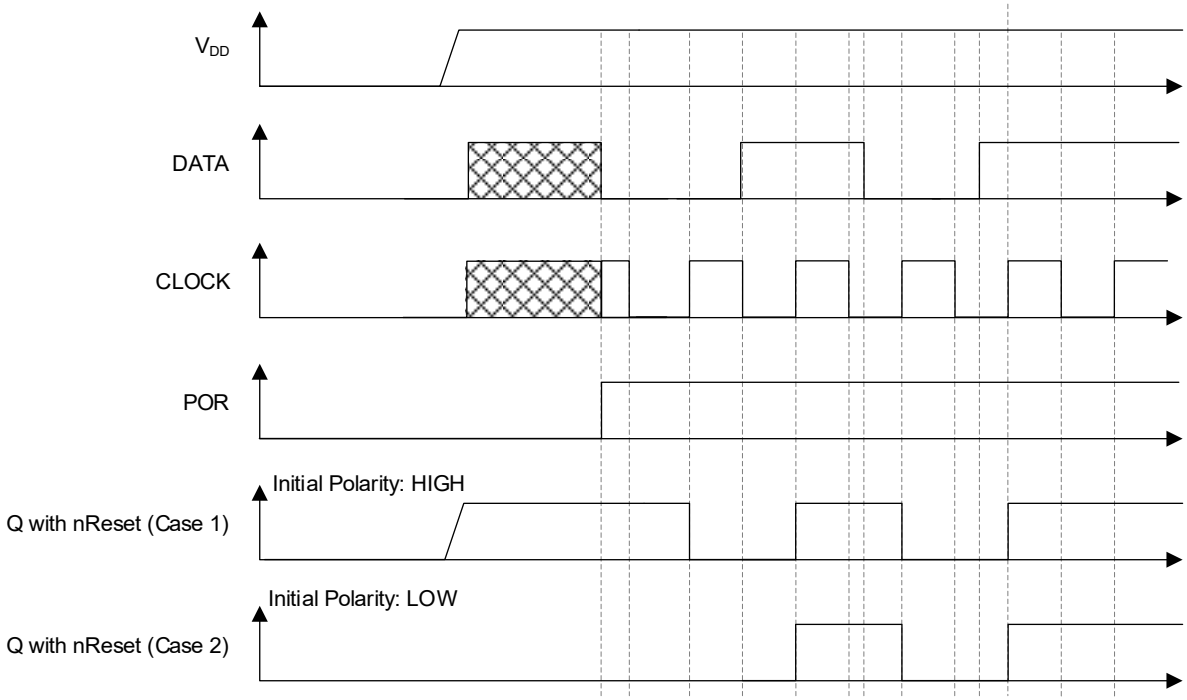


Figure 42. DFF Polarity Operations

10.2 2-bit LUT or Programmable Pattern Generator

The SLG47104 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high-level reset (RST) and a low-level reset (nRST) options available, which are selected by register [1193]. When operating as a Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

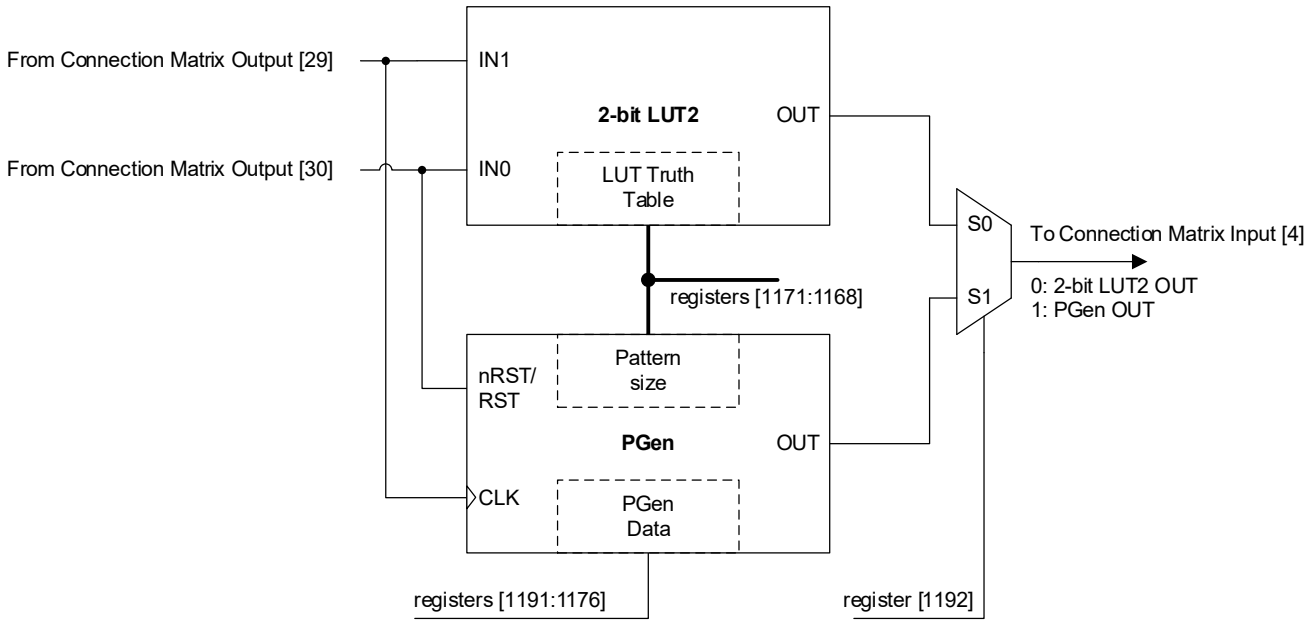


Figure 43. 2-bit LUT2 or PGen

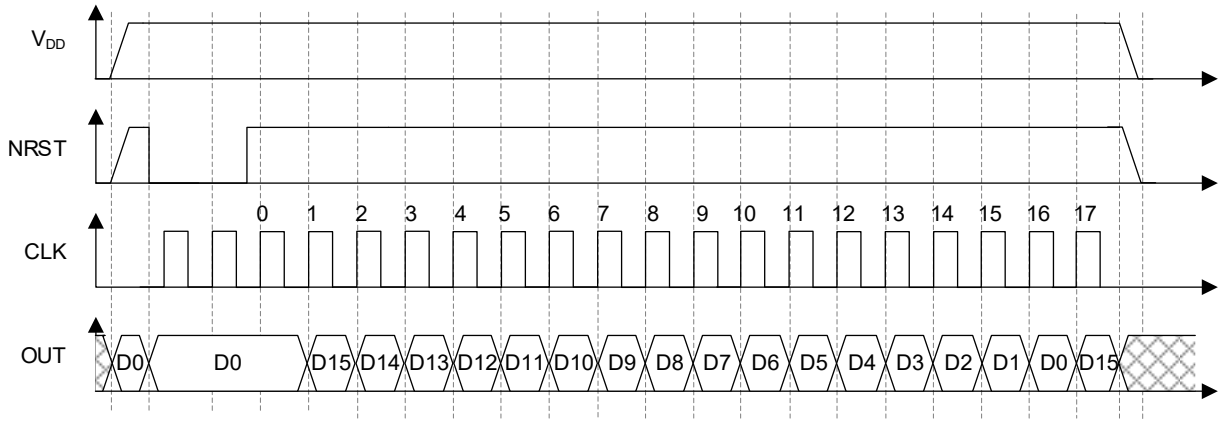


Figure 44. PGen Timing Diagram

10.2.1 2-bit LUT or PGen Macrocell Used as 2-bit LUT

Table 18. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1168]	LSB
0	1	register [1169]	
1	0	register [1170]	
1	1	register [1171]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT2 is defined by registers [1171:1168].

Table 19 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 19. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0

Function	MSB			LSB
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

10.3 3-bit LUT or D Flip-Flop with Set/Reset Macrocells

There are three macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by register (3-bit LUT0 – register [1226], 3-bit LUT2 – register [1163], 3-bit LUT3 – register [1243]).

DFF2 functionality is different from the other DFFs. DFF2 operation will flow the functional description below:

- If register [1228] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1228] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

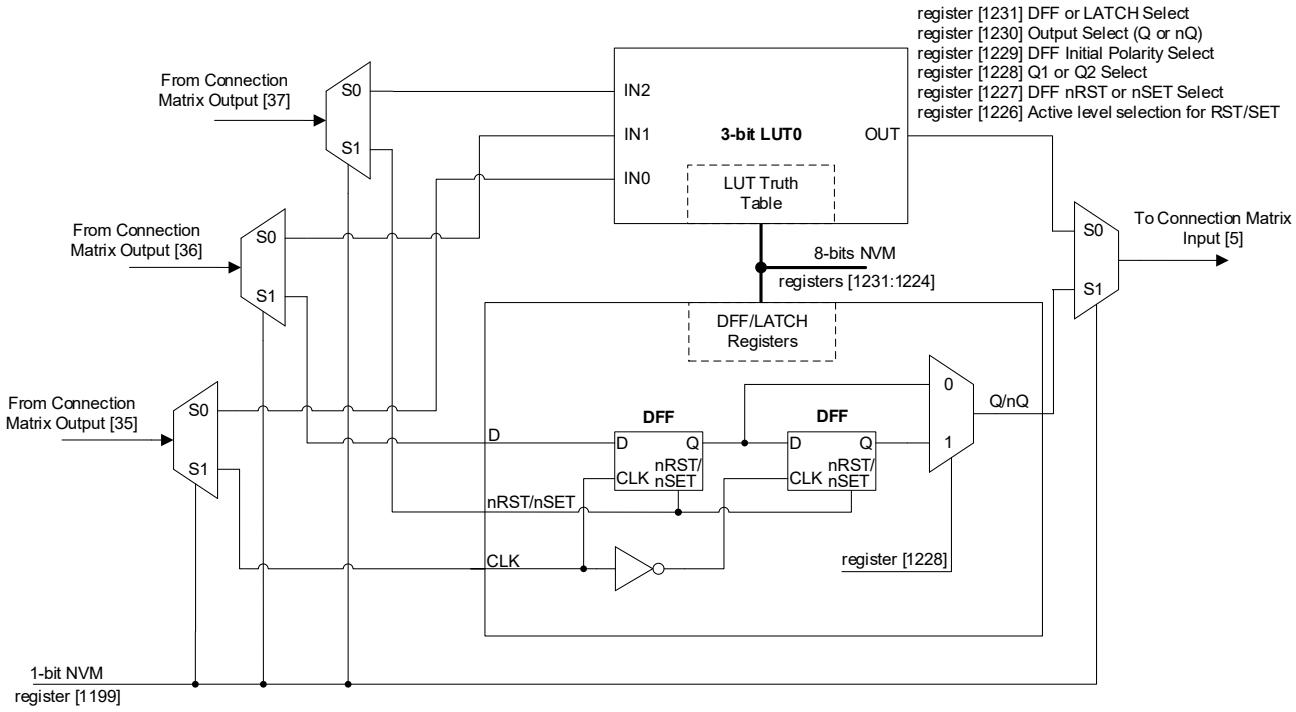


Figure 45. 3-bit LUT0 or DFF2

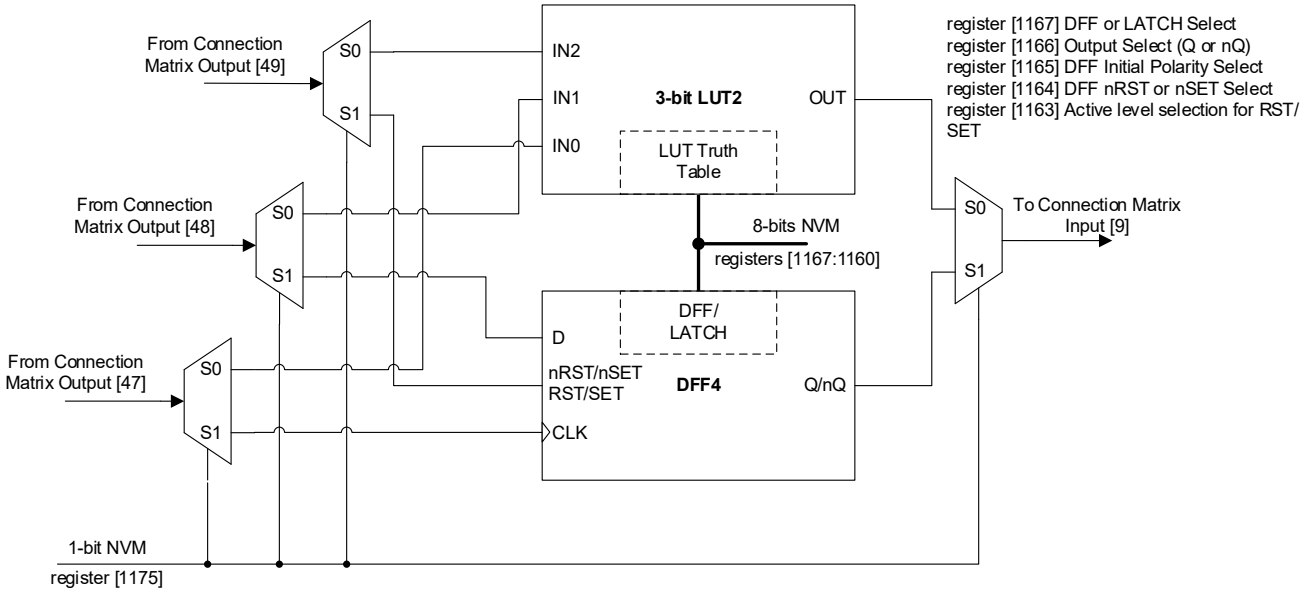


Figure 46. 3-bit LUT2 or DFF4

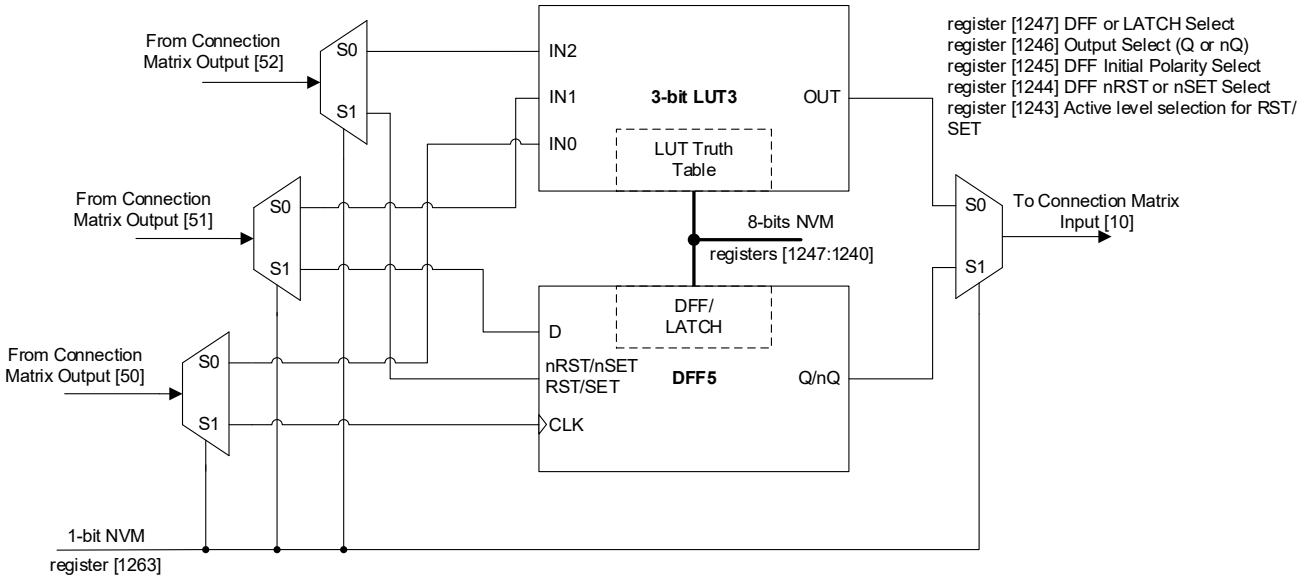


Figure 47. 3-bit LUT3 or DFF5

10.3.1 3-bit LUT or D Flip-Flop Macrocells Used as 3-bit LUTs

Table 20. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Table 21. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1160]	LSB
0	0	1	register [1161]	
0	1	0	register [1162]	
0	1	1	register [1163]	
1	0	0	register [1164]	
1	0	1	register [1165]	
1	1	0	register [1166]	
1	1	1	register [1167]	MSB

Table 22. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1240]	LSB
0	0	1	register [1241]	
0	1	0	register [1242]	
0	1	1	register [1243]	
1	0	0	register [1244]	
1	0	1	register [1245]	
1	1	0	register [1246]	
1	1	1	register [1247]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT0 is defined by registers [1231:1224]
- 3-bit LUT2 is defined by registers [1167:1160]
- 3-bit LUT3 is defined by registers [1247:1240].

Table 23 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 23. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.3.2 Initial Polarity Operations

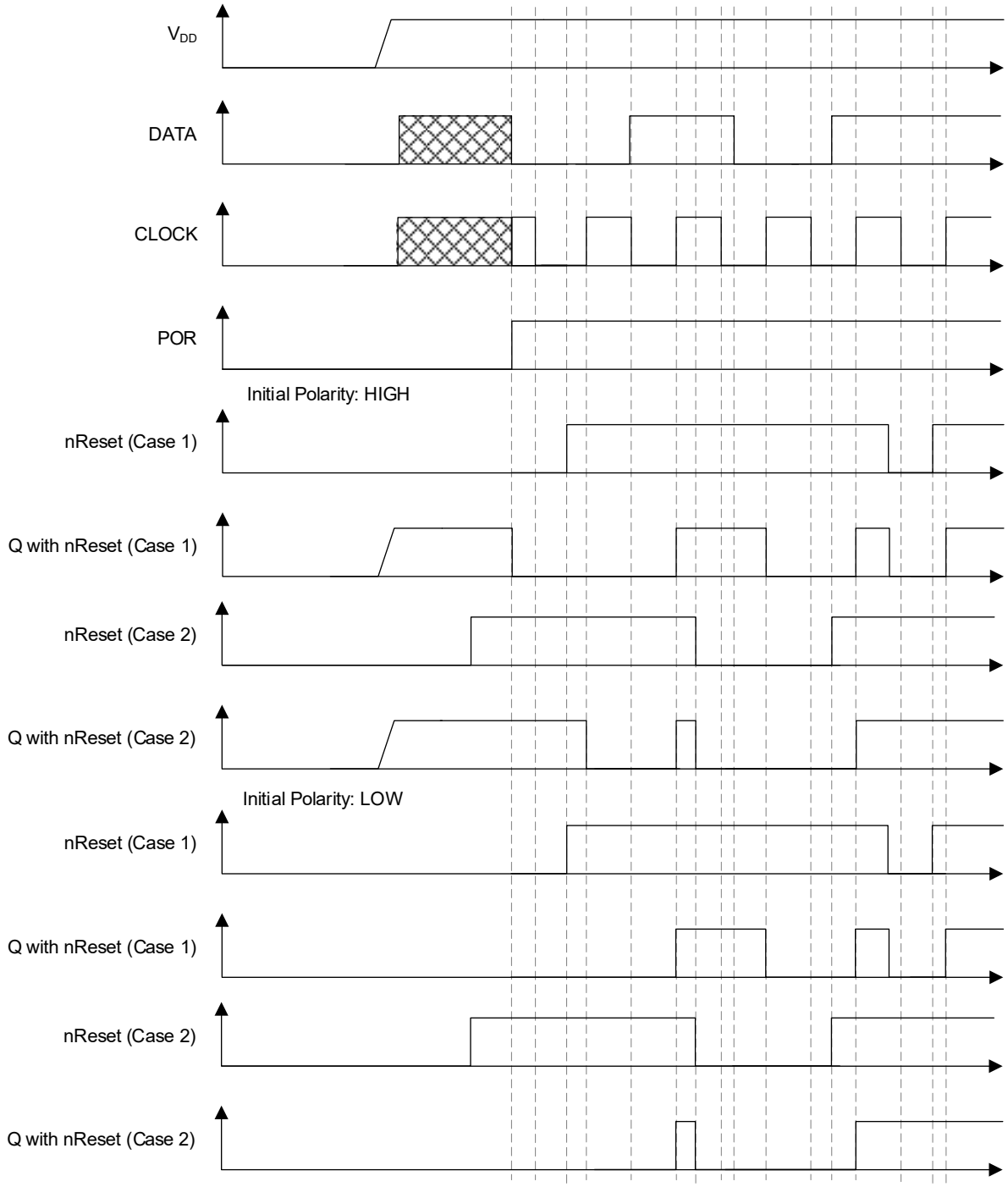


Figure 48. DFF Polarity Operations with nReset

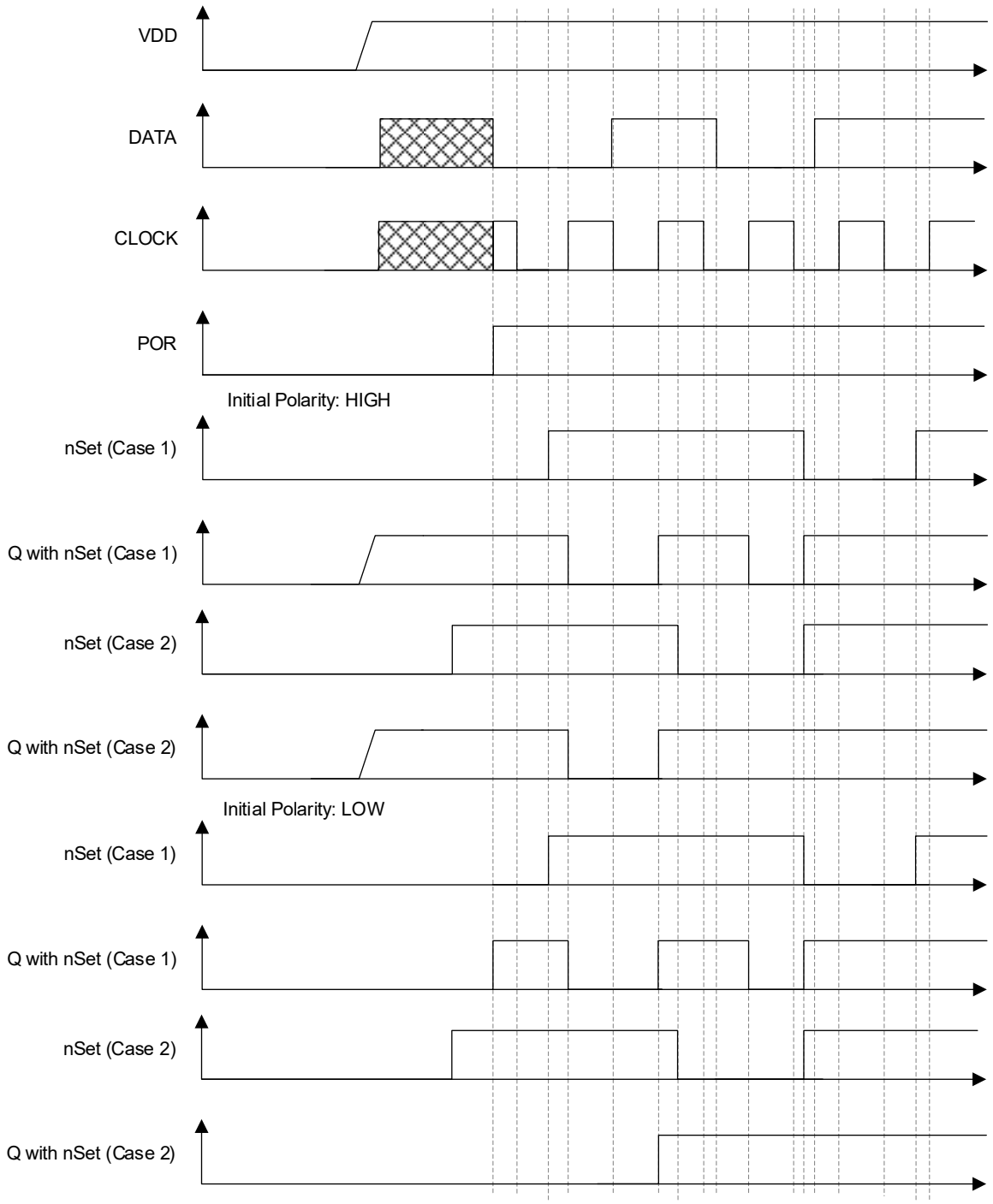


Figure 49. DFF Polarity Operations with nSet

10.4 3-bit LUT or D Flip-Flop with Set/Reset Macrocell or PWM Chopper

There is one macrocell that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs, or as PWM Chopper. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high-level reset/set (RST/SET) and active low-level reset/set (nRST/nSET) options available, which are selected by register [1139]. When used to implement PWM Chopper function, the three input signals from the connection

matrix go to the PWM input (PWM) and Blanking Time input (Blanking Time), and Chopper input (Chop) for the PWM Chopper, with the output (OUT) going back to the connection matrix.

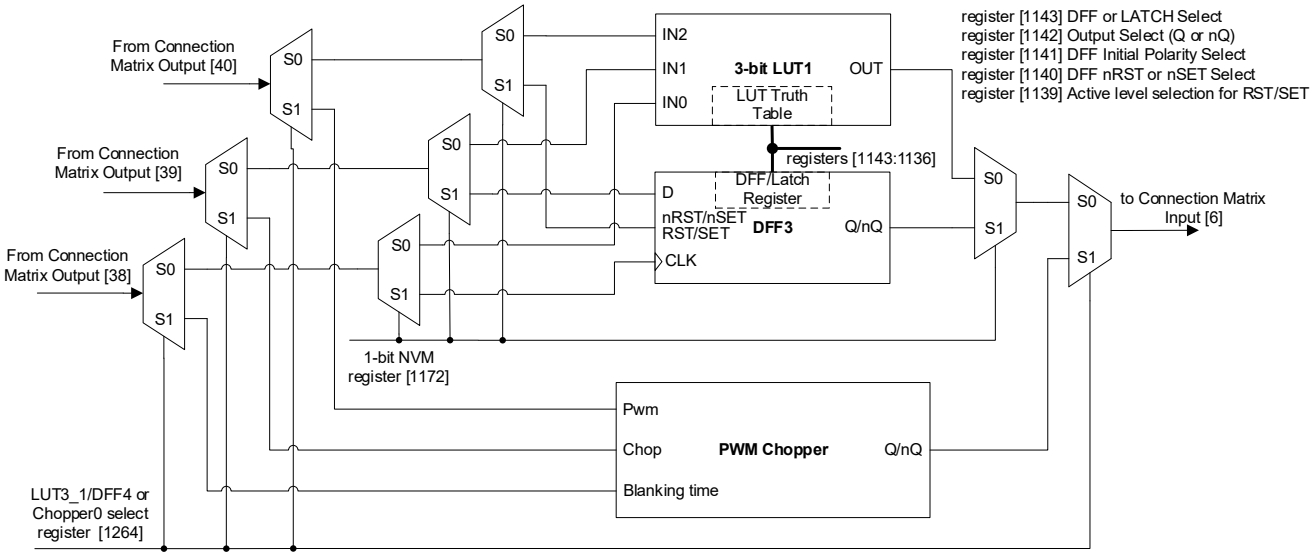


Figure 50. 3-bit LUT1 or DFF3

10.4.1 3-bit LUT or D Flip-Flop or PWM Chopper Macrocells Used as 3-bit LUTs

Table 24. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1136]	LSB
0	0	1	register [1137]	
0	1	0	register [1138]	
0	1	1	register [1139]	
1	0	0	register [1140]	
1	0	1	register [1141]	
1	1	0	register [1142]	
1	1	1	register [1143]	MSB

This macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT1 is defined by registers [1143:1136].

Table 25 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 25. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.4.2 PWM Chopper

PWM Chopper function can be used to chop PWM Duty Cycle by Current Comparator signal.

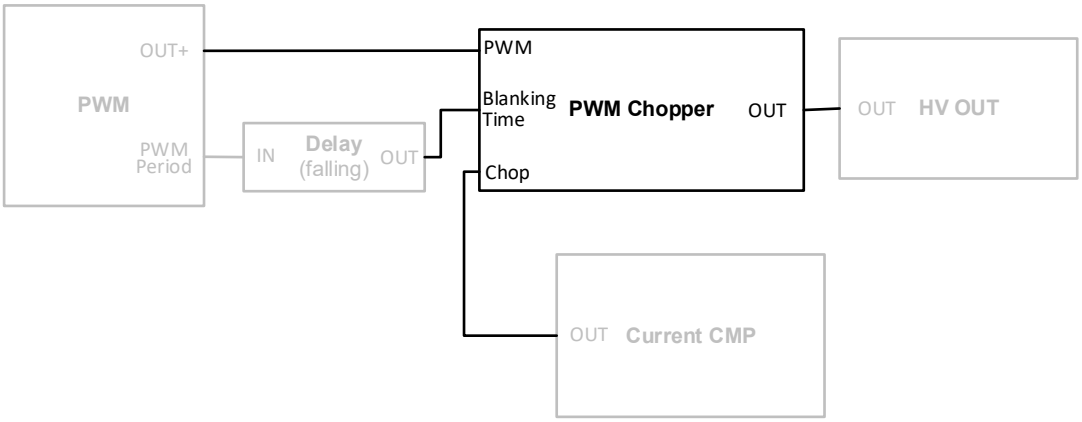


Figure 51. PWM Chopper Circuit Example

In PWM Chopper mode all internal components of 3-bit LUT or D Flip-Flop, or PWM Chopper Macrocell are connected as shown in Figure 52.

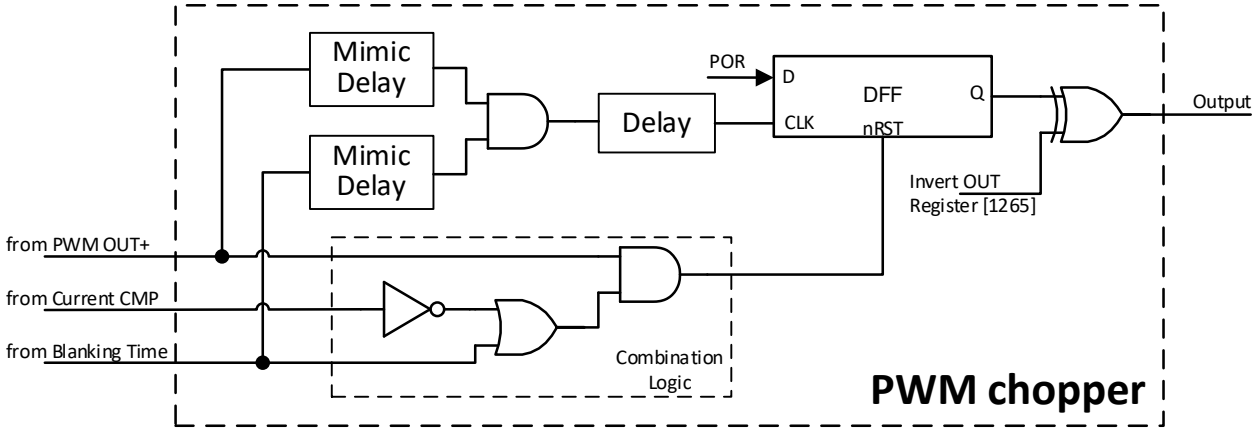


Figure 52. PWM Chopper Interconnection

This configuration allows ignoring Current Comparator signal during Blanking time during the motor start period. Any active signal from Current CMP after Blanking time causes PWM Duty Cycle chopping to currently Period end. The following figures demonstrate PWM Chopper operation.

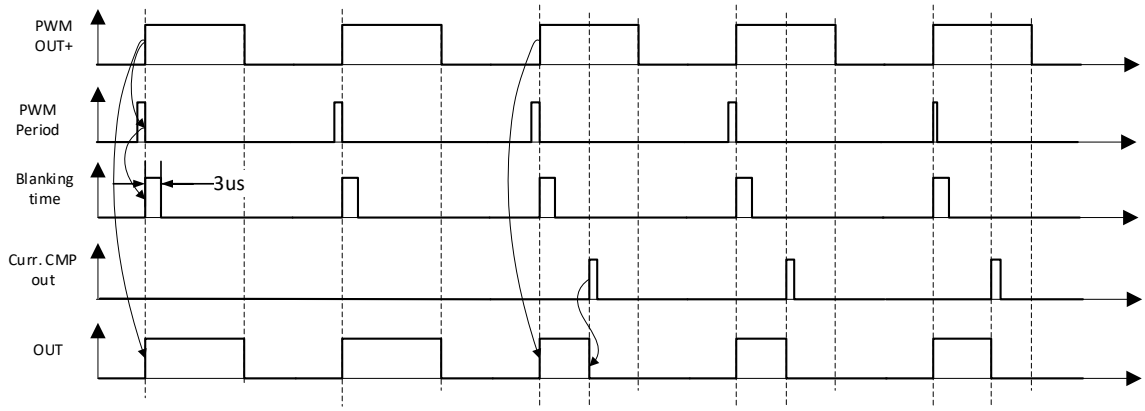


Figure 53. PWM Chopper. Overcurrent Timing Diagram

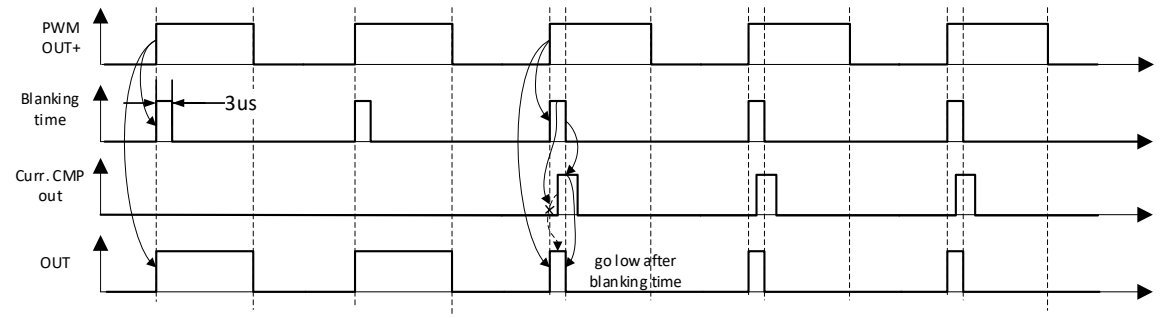


Figure 54. PWM Chopper. Overcurrent Start During Blanking Time

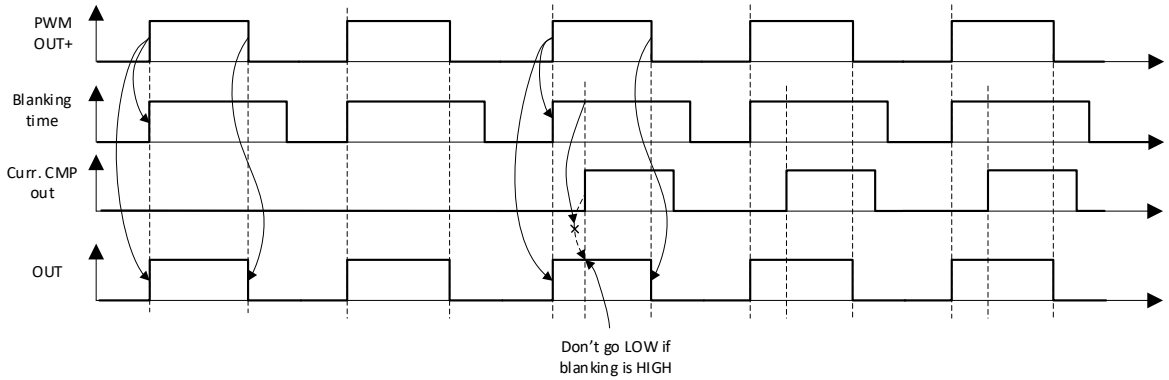


Figure 55. PWM Chopper. PWM Duty Cycle is Less than Blanking Time

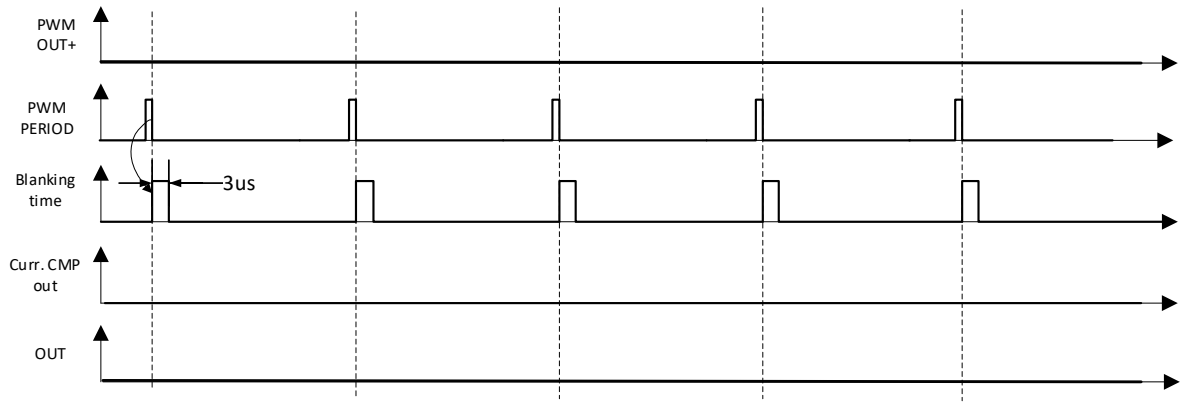


Figure 56. PWM Chopper. 0% Duty Cycle

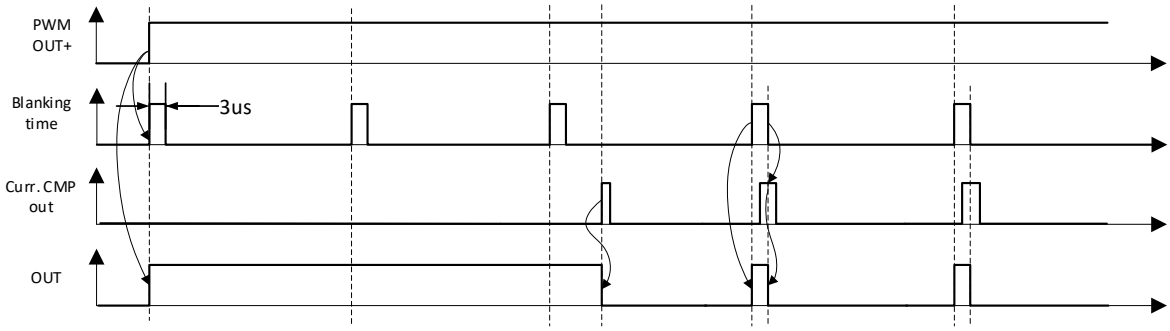


Figure 57. PWM Chopper. Overcurrent when 100 % Duty Cycle

10.4.3 Initial Polarity Operations

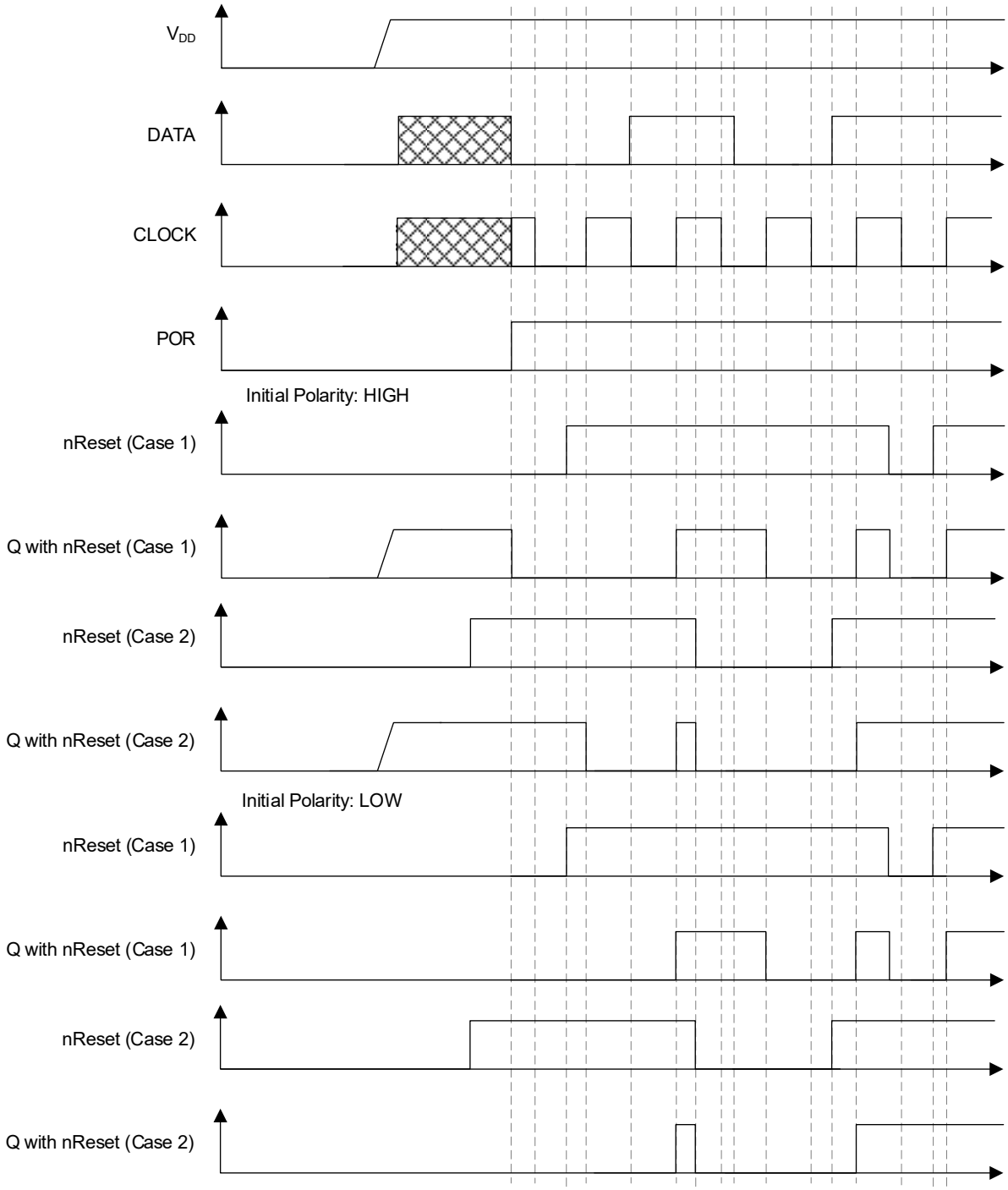


Figure 58. DFF Polarity Operations with nReset

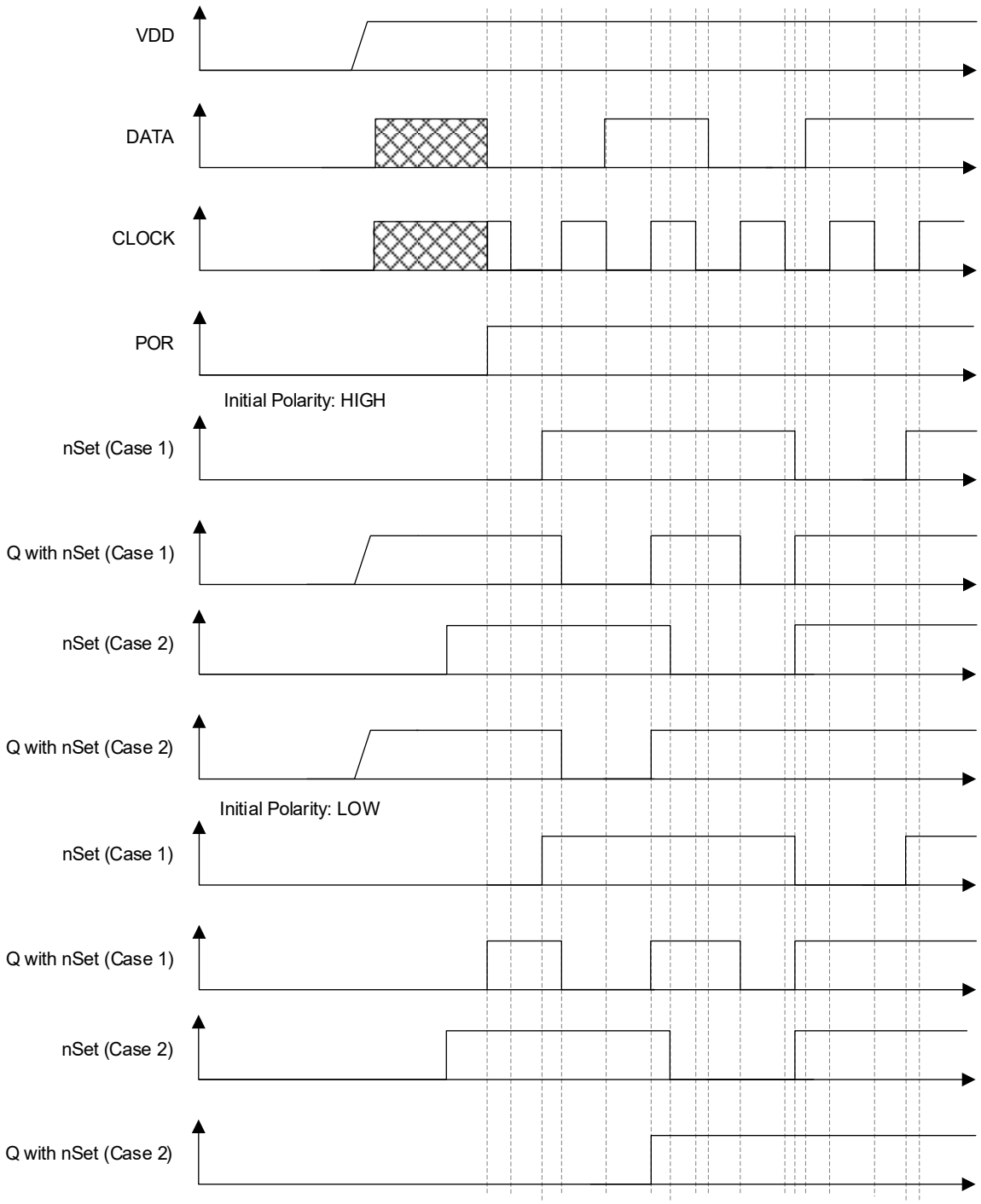


Figure 59. DFF Polarity Operations with nSet

10.5 3-bit LUT or Pipe Delay/Ripple Counter Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 - 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that

is controlled by registers [1203:1200] for OUT0 and registers [1207:1204] for OUT1. The 4- input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG47104 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG47104). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1197]).

In the Ripple Counter mode, there are 3 options for setting which use 7 bits. There are 3 bits to set nSET value (SV) in the range from 0 to 7. This value will be set into the Ripple Counter outputs when nSET input goes LOW. End value (EV) will use 3 bits for setting output code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The Functionality mode option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by the register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, the count starts from SV up to EV, and others.

In the FULL range configuration, the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. The current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, the count goes up starting from SV. The current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 61.

Every step is executed by the rising edge on CLK input.

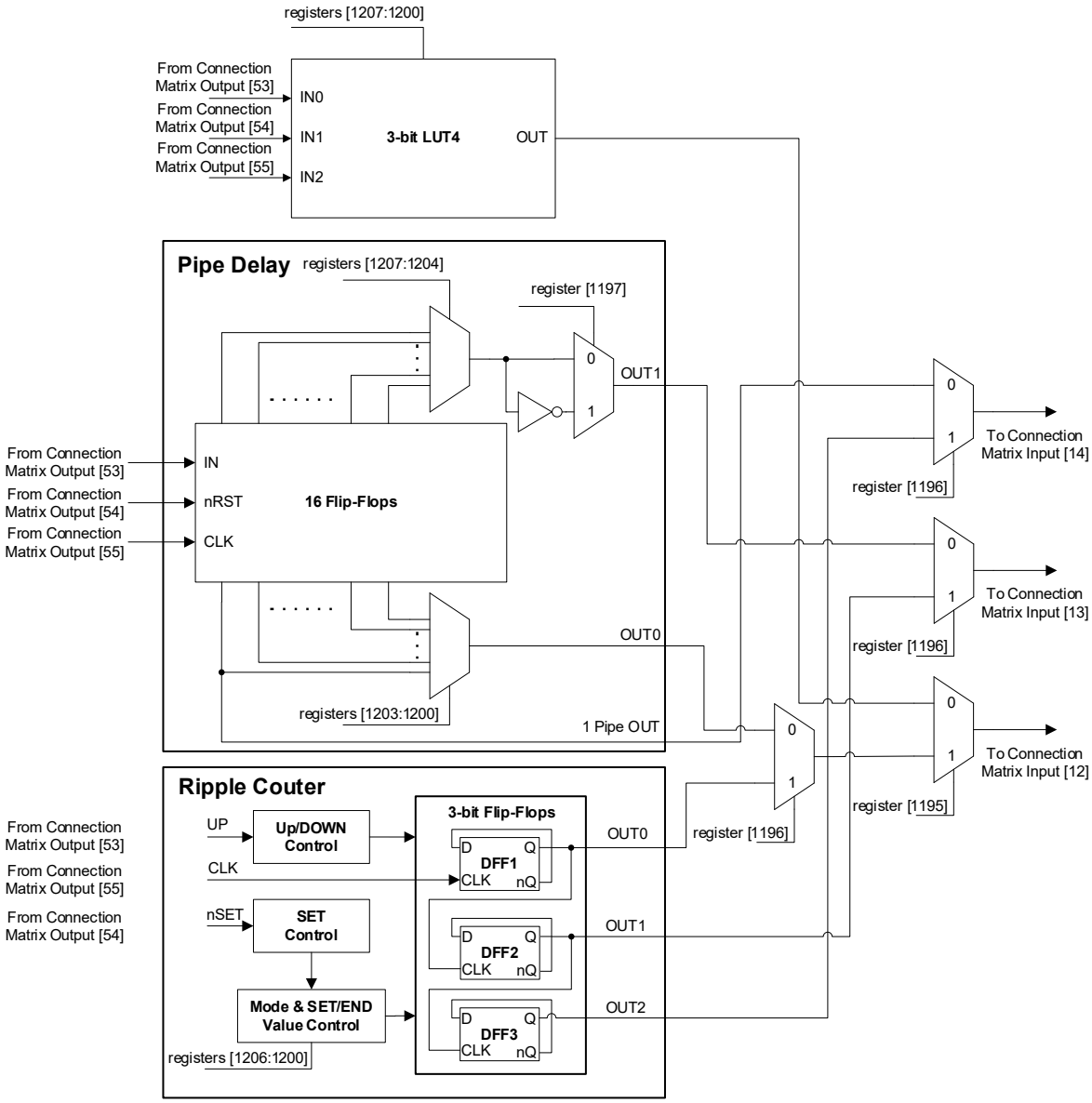


Figure 60. 3-bit LUT4/Pipe Delay/Ripple Counter

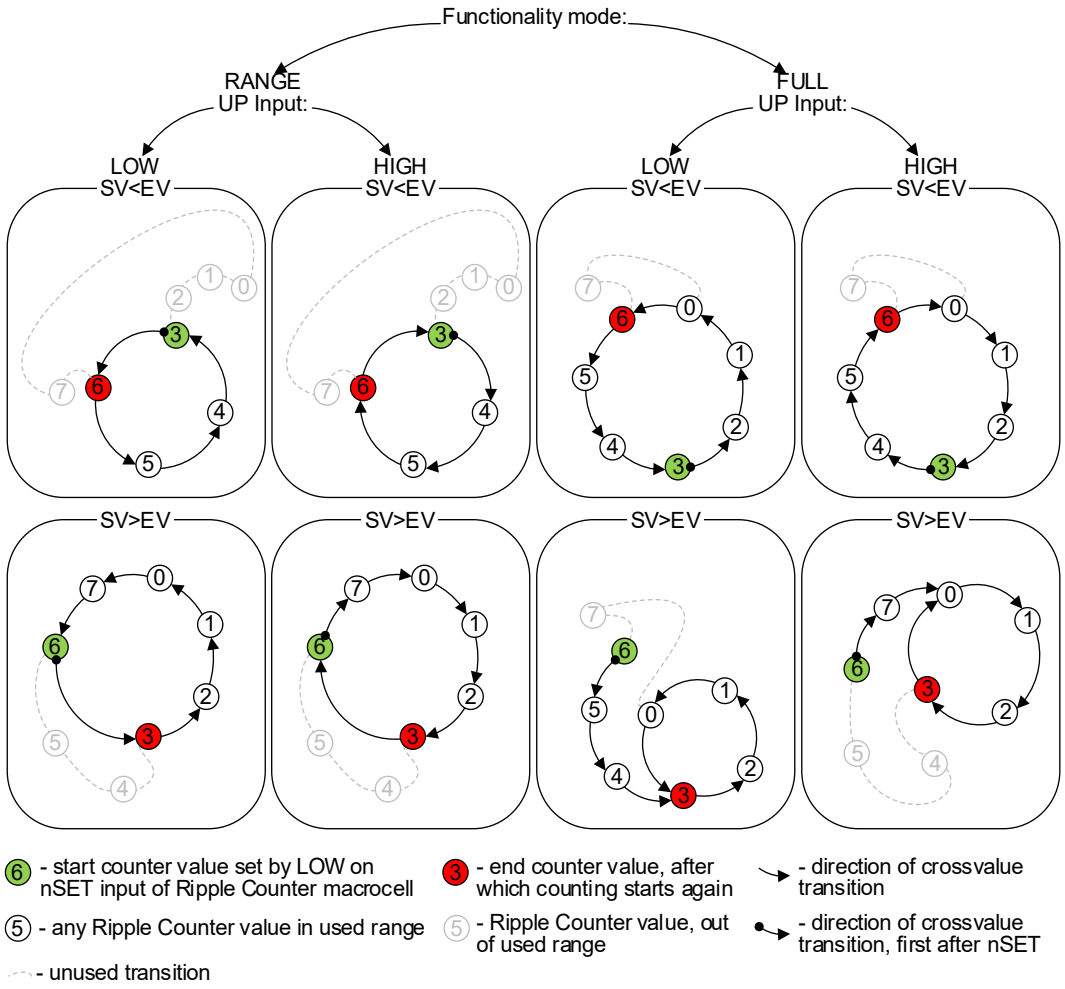


Figure 61. Example of Ripple Counter Functionality

10.5.1 3-bit LUT or Pipe Delay Macrocells Used as 3-bit LUT

Table 26. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1200]	LSB
0	0	1	register [1201]	
0	1	0	register [1202]	
0	1	1	register [1203]	
1	0	0	register [1204]	
1	0	1	register [1205]	
1	1	0	register [1206]	
1	1	1	register [1207]	MSB

Macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT4 is defined by registers [1207:1200].

10.6 4-bit LUT or D Flip-Flop Macrocell

There is one macrocell that can serve as either 4-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 4-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
- LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output when CLK is High).

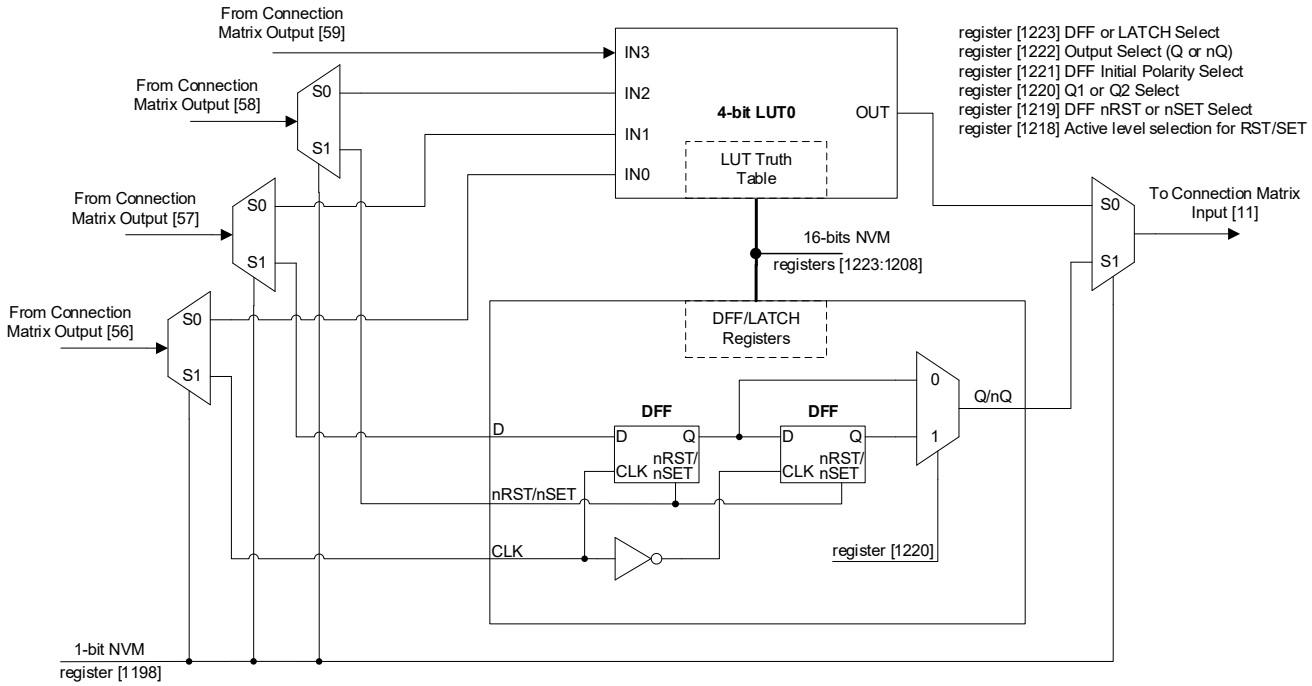


Figure 62. 4-bit LUT0 or DFF6

10.6.1 4-bit LUT Macrocell Used as 4-bit LUT

Table 27. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1208]	LSB
0	0	0	1	register [1209]	
0	0	1	0	register [1210]	
0	0	1	1	register [1211]	
0	1	0	0	register [1212]	
0	1	0	1	register [1213]	
0	1	1	0	register [1214]	
0	1	1	1	register [1215]	
1	0	0	0	register [1216]	
1	0	0	1	register [1217]	
1	0	1	0	register [1218]	

IN3	IN2	IN1	IN0	OUT	
1	0	1	1	register [1219]	
1	1	0	0	register [1220]	
1	1	0	1	register [1221]	
1	1	1	0	register [1222]	
1	1	1	1	register [1223]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-bit LUT0 is defined by registers [1223:1208].

Table 28. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

11. Multi-Function Macrocells

The SLG47104 has three Multi-Function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 63.

See the list below for the functions that can be implemented in these macrocells:

- Three macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-bit Counter/Delays.

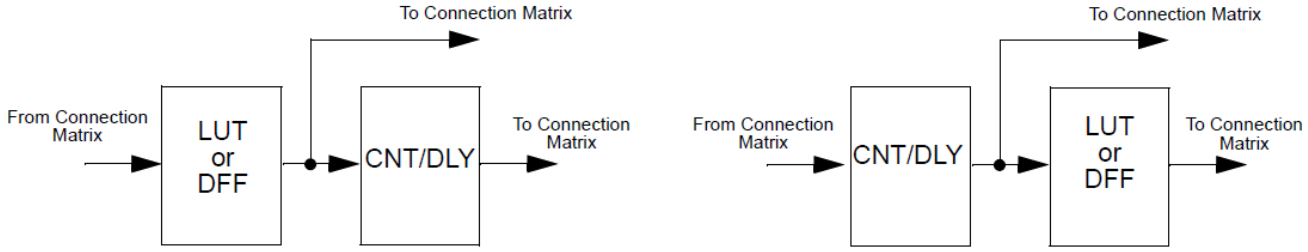


Figure 63. Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the three Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

11.1 3-bit LUT or DFF/LATCH with 8-bit Counter/Delay Macrocells

There are two macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which defines its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as the initial value defined by a Delay In signal.

For example, in case the initial LOW option is used, the rising edge delay will start operation. For timing diagrams refer to section 11.3 CNT/DLY/FSM Timing Diagrams

Only CNT0 current count value can be read via I^2C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 19.5.4 for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 and After two DFF is bypass – counters initialize with counter data after POR.

11.1.1 3-bit LUT or 8-bit CNT/DLY Block Diagrams

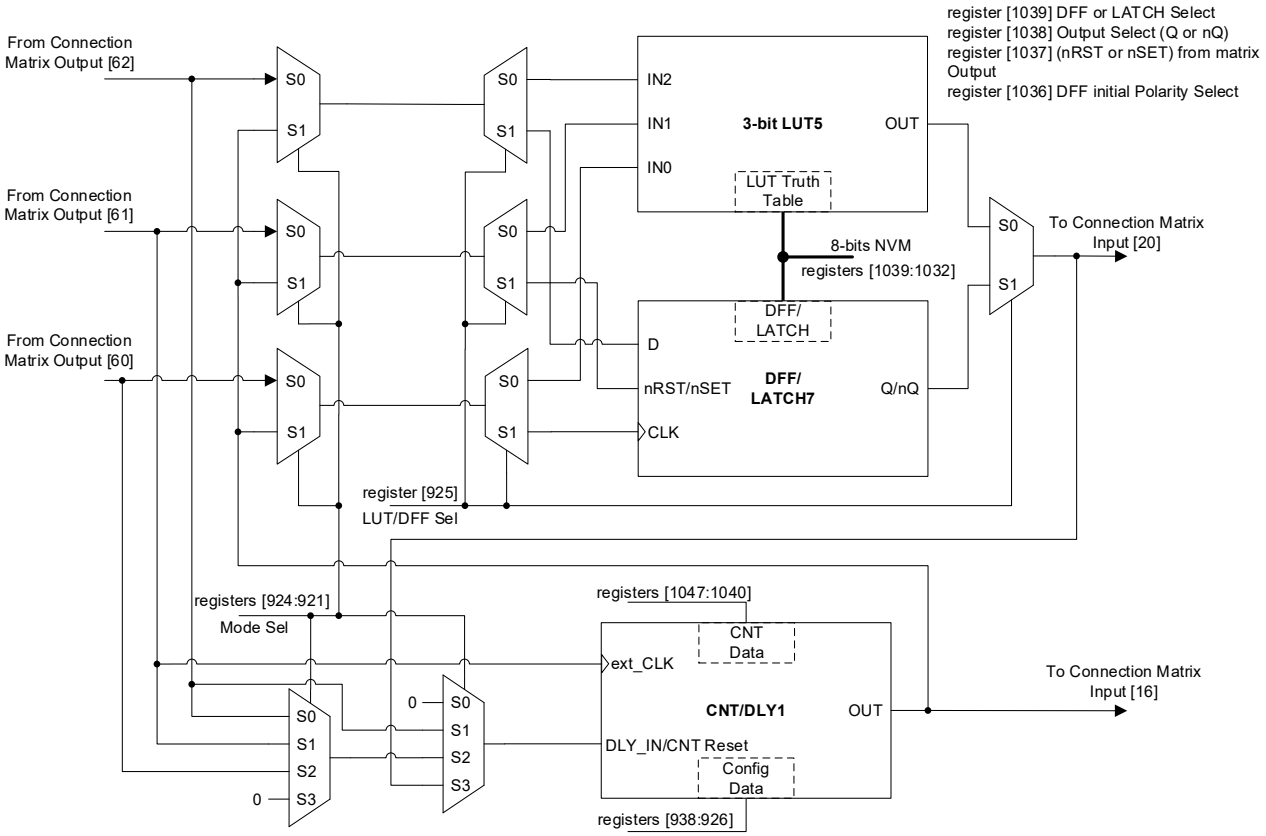


Figure 64. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT5/DFF7, CNT/DLY1)

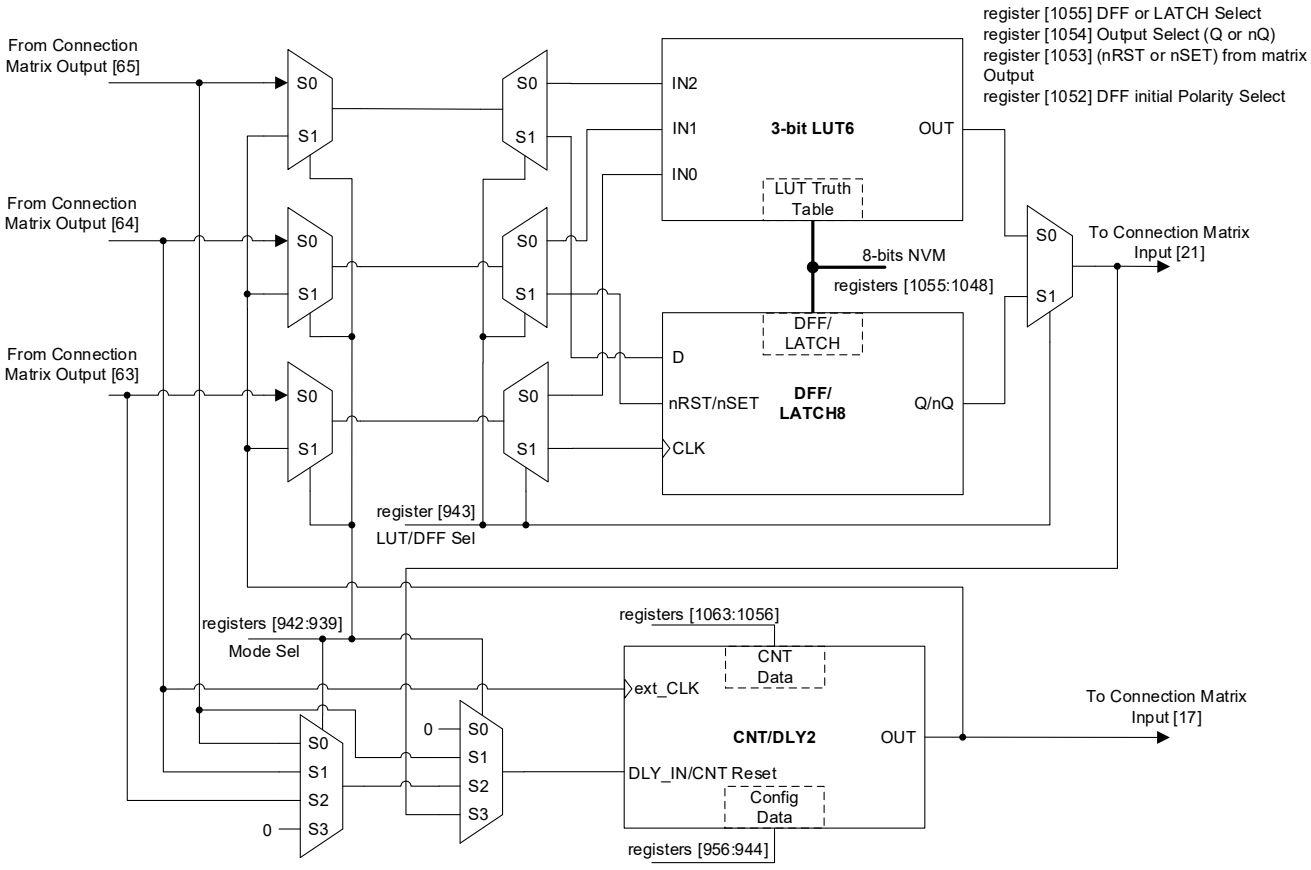


Figure 65. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT6/DFF8, CNT/DLY2)

There is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

11.1.2 3-bit LUT or CNT/DLYs Used as 3-bit LUTs

Table 29. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1032]	LSB
0	0	1	register [1033]	
0	1	0	register [1034]	
0	1	1	register [1035]	
1	0	0	register [1036]	
1	0	1	register [1037]	
1	1	0	register [1038]	
1	1	1	register [1039]	MSB

Table 30. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1048]	LSB
0	0	1	register [1049]	
0	1	0	register [1050]	
0	1	1	register [1051]	
1	0	0	register [1052]	
1	0	1	register [1053]	
1	1	0	register [1054]	
1	1	1	register [1055]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT5 is defined by registers [1039:1032]
- 3-bit LUT6 is defined by registers [1055:1048].

11.2 4-bit LUT or DFF/LATCH with 16-bit Counter/Delay Macrocell

There is one macrocell that can serve as either 4-bit LUT or as 16-bit Counter/Delay. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-bit Counter/Delay function, two of four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See section 19 I2C Serial Communications Macrocell for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

11.2.1 4-bit LUT or DFF/LATCH with 16-bit CNT/DLY Block Diagram

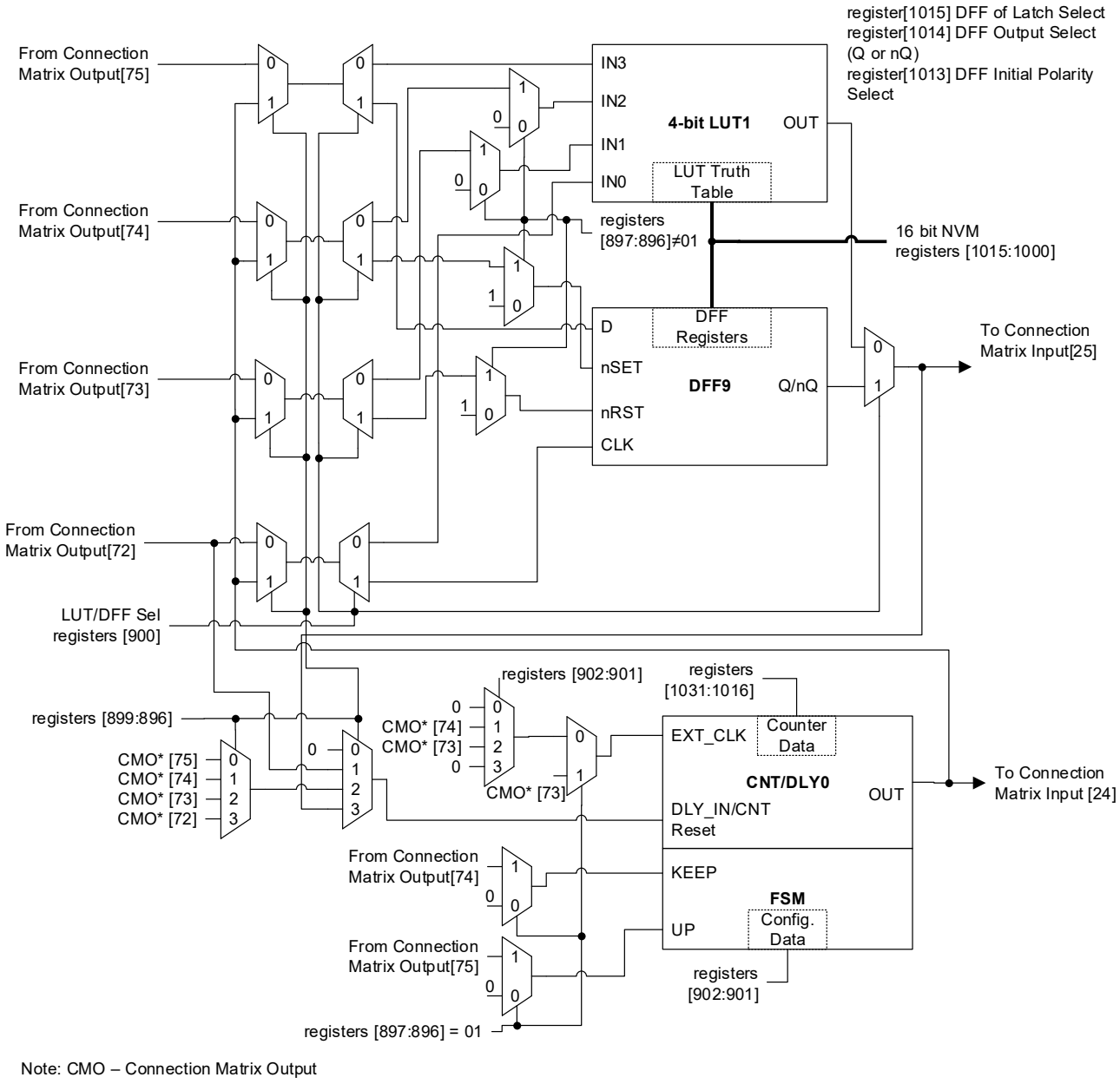


Figure 66. 16-bit Multi-Function Macrocell Block Diagram (4-bit LUT1/DFF9, CNT/DLY/FSM0)

11.2.2 4-bit LUT or 16-bit Counter/Delay Macrocells Used as 4-bit LUTs

Table 31. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1000]	LSB
0	0	0	1	register [1001]	
0	0	1	0	register [1002]	
0	0	1	1	register [1003]	
0	1	0	0	register [1004]	

IN3	IN2	IN1	IN0	OUT	
0	1	0	1	register [1005]	
0	1	1	0	register [1006]	
0	1	1	1	register [1007]	
1	0	0	0	register [1008]	
1	0	0	1	register [1009]	
1	0	1	0	register [1010]	
1	0	1	1	register [1011]	
1	1	0	0	register [1012]	
1	1	0	1	register [1013]	
1	1	1	0	register [1014]	
1	1	1	1	register [1015]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

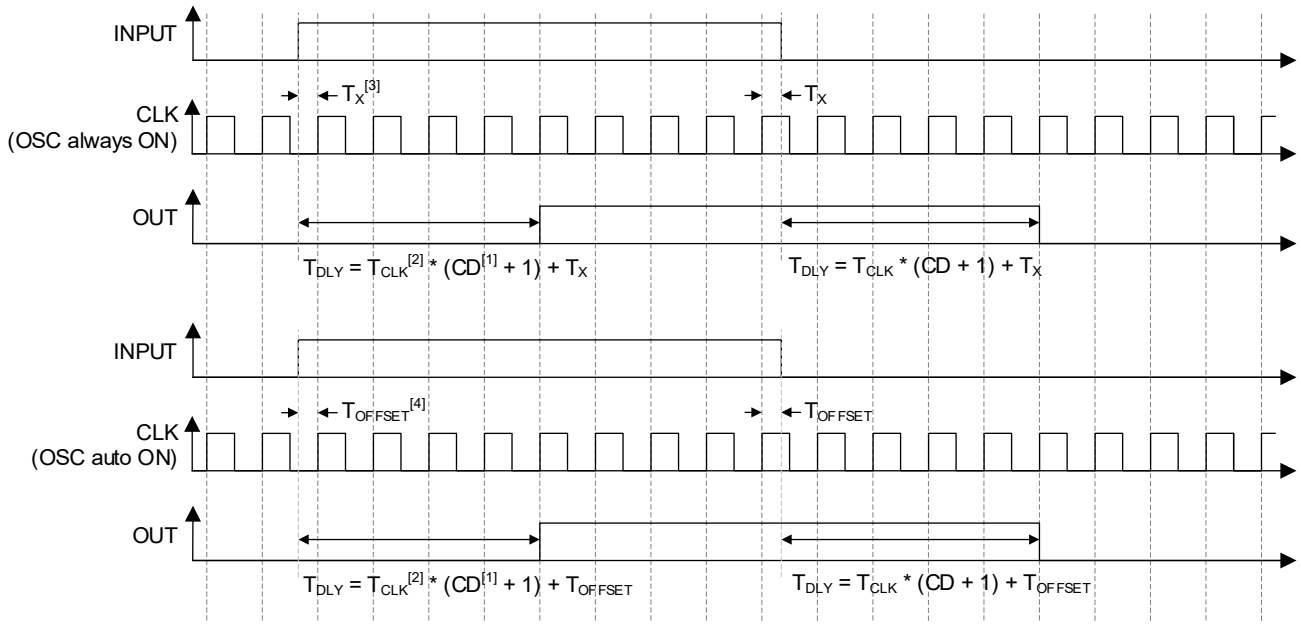
- 4-bit LUT1 is defined by registers [1015:1000].

Table 32. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

11.3 CNT/DLY/FSM Timing Diagrams

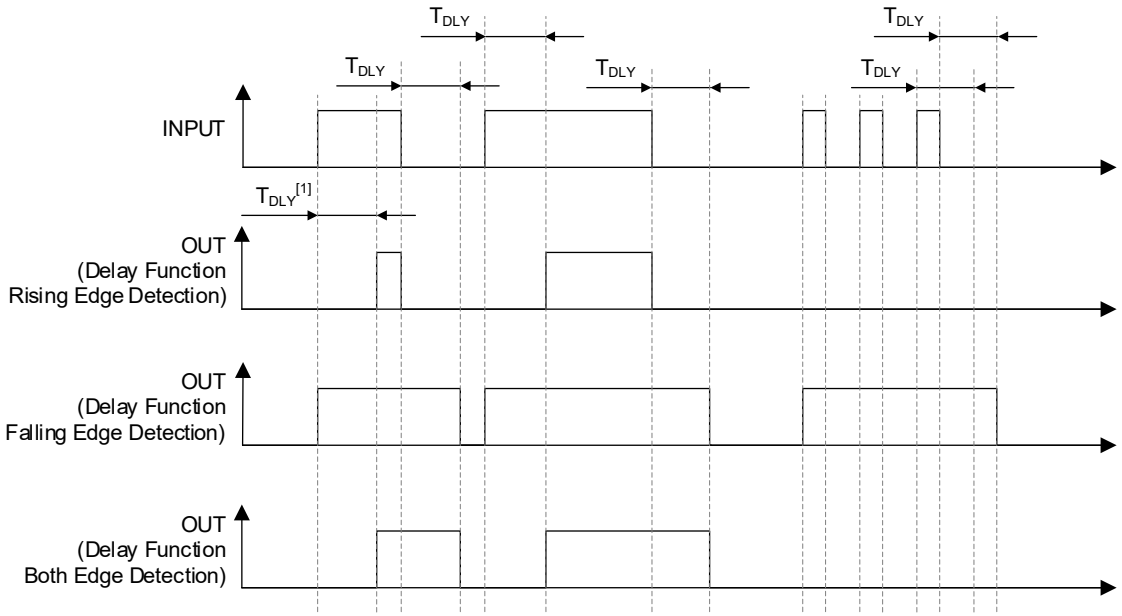
11.3.1 Delay Mode CNT/DLY0 to CNT/DLY2



[1]CD is a TIMER Counter Data value.
[2]T_{CLK} is a CLK period time.
[3]T_X is an asynchronous delay variable. It can take a value from 0 to 1 T_{CLK}.
[4]T_{OFFSET} is a time between delay start and first CLK after OSC start, see Specifications section.

Figure 67. Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.



[1]T_{DLY} is a delay time defined by Counter Data registers.

Figure 68. Delay Mode Timing Diagram for Different Edge Select Modes

11.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY2

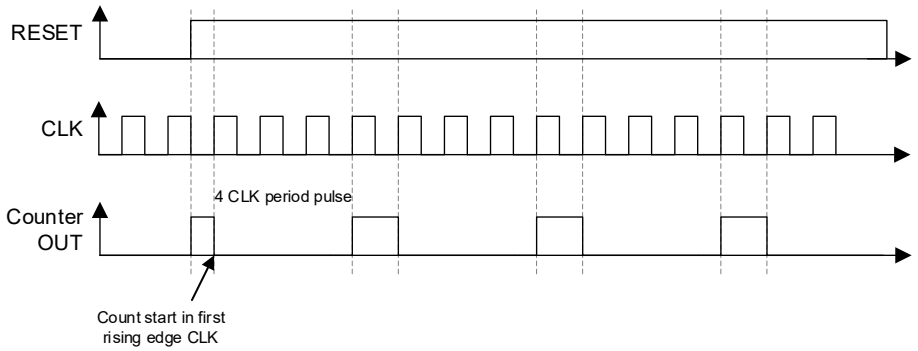


Figure 69. Counter Mode Timing Diagram without Two DFFs Synced Up

Note: This mode may cause counter data to be loaded wrong, if reset releases at the same time when the clock appears. As a solution, please use the mode with two DFFs synced up.

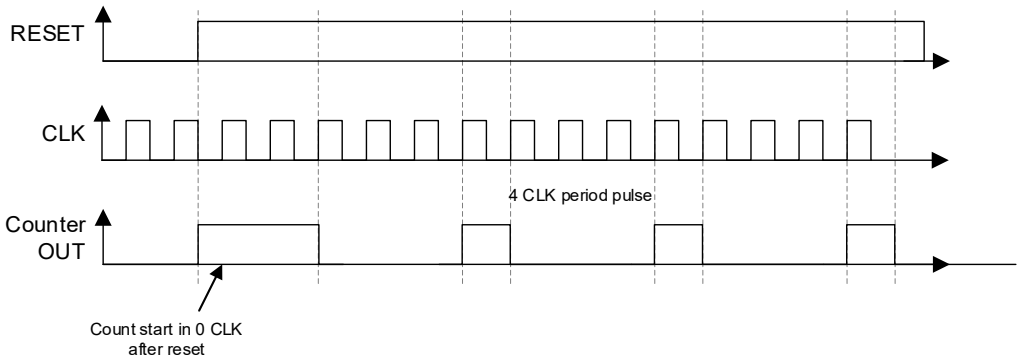
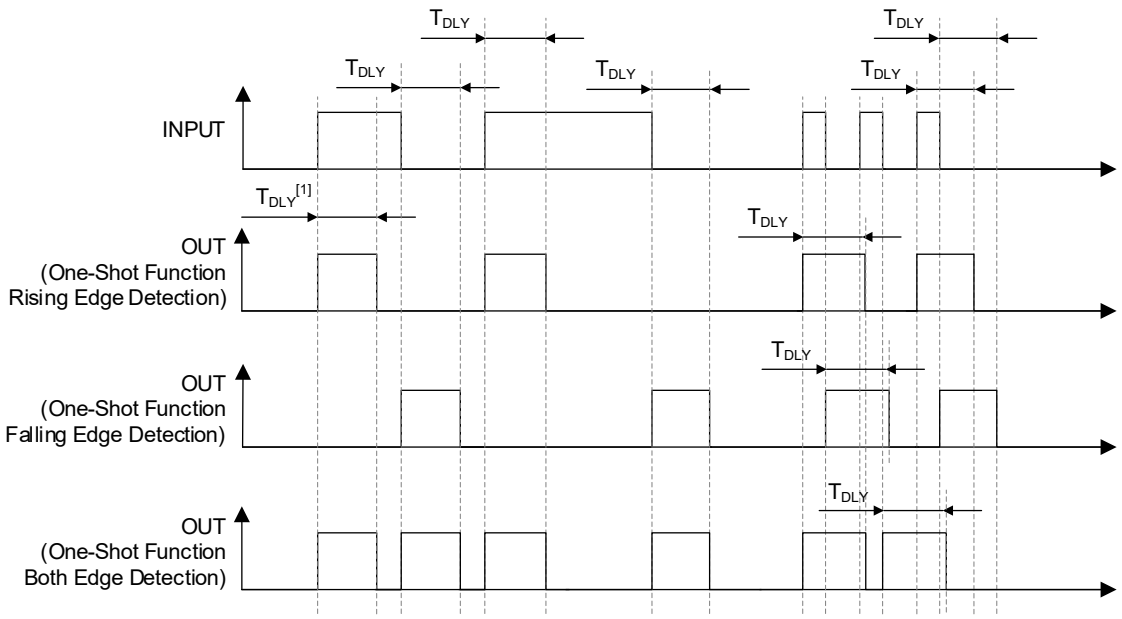


Figure 70. Counter Mode Timing Diagram with Two DFFs Synced Up

11.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY2

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties.

The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.



[1]T_{DLY} is a delay time defined by Counter Data registers.

Figure 71. One-Shot Function Timing Diagram

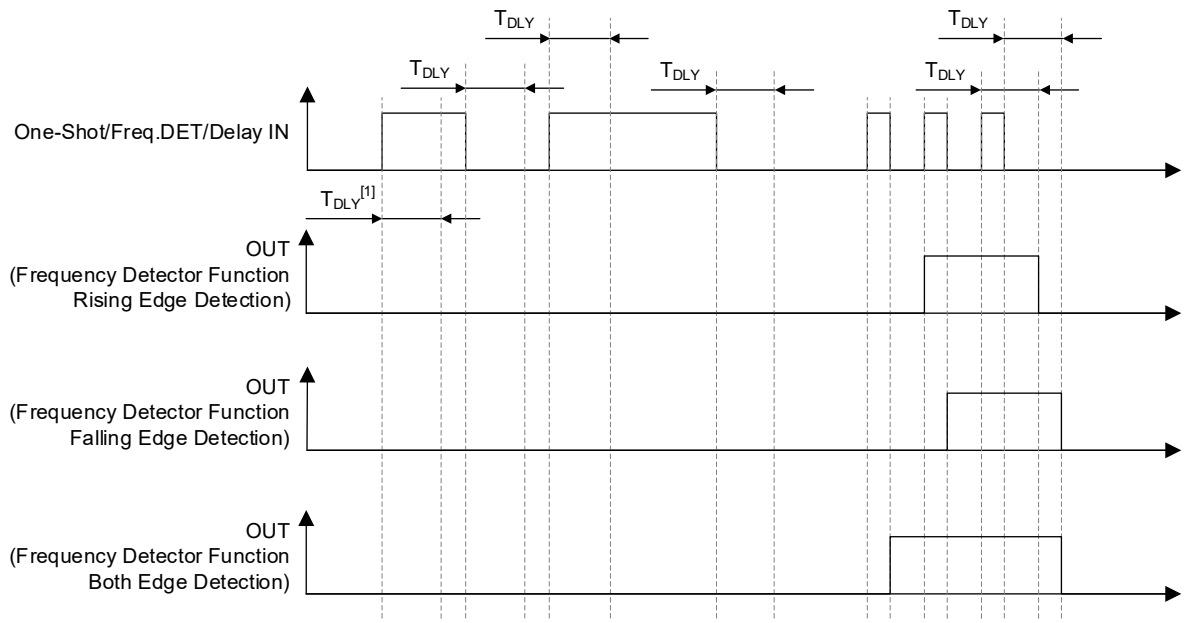
This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

11.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY2

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.



[1]T_{DLY} is a delay time defined by Counter Data registers.

Figure 72. Frequency Detection Mode Timing Diagram

11.3.5 Edge Detection Mode CNT/DLY0 to CNT/DLY2

The macrocell generates high level short pulse when detecting the respective edge.

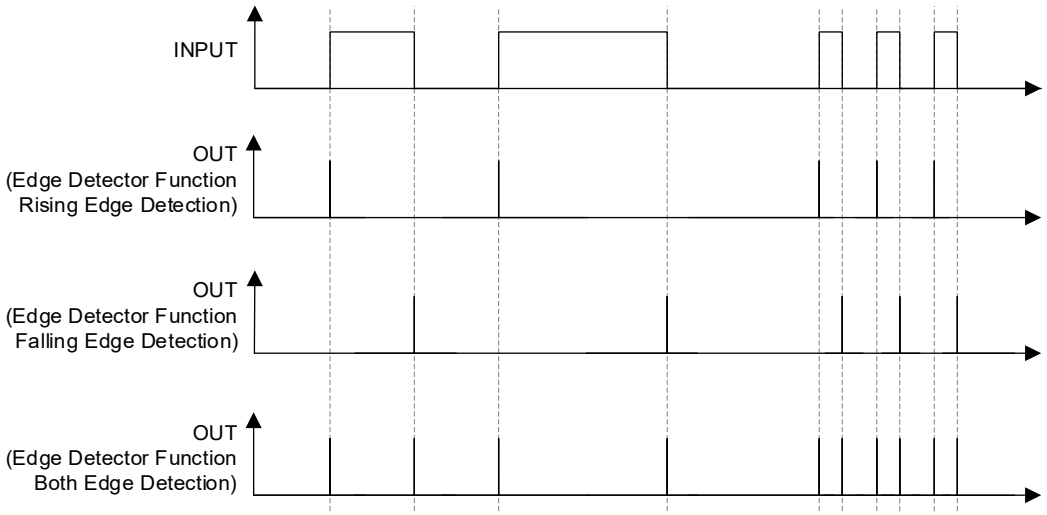
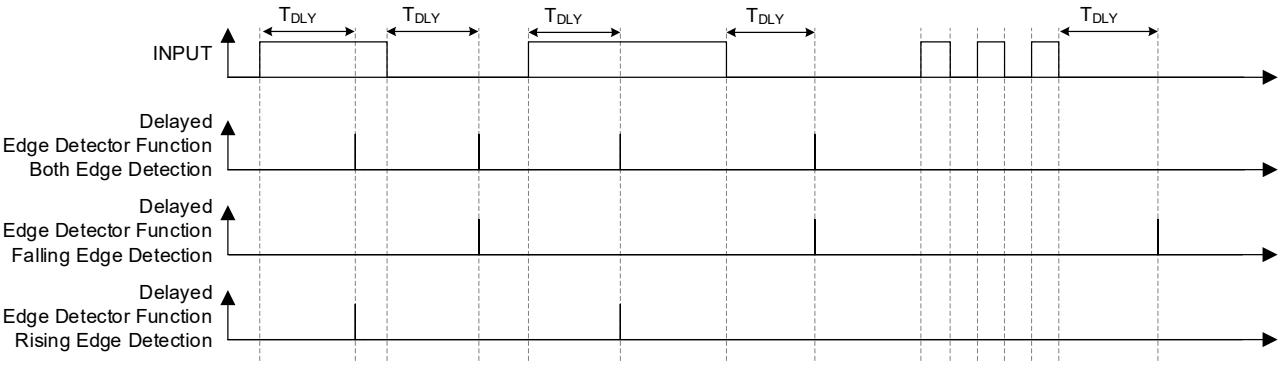


Figure 73. Edge Detection Mode Timing Diagram

11.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY2

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 74.



T_{DLY} is a delay time defined by Counter Data registers.

Figure 74. Delayed Edge Detection Mode Timing Diagram

11.3.7 CNT/FSM Mode CNT/DLY0

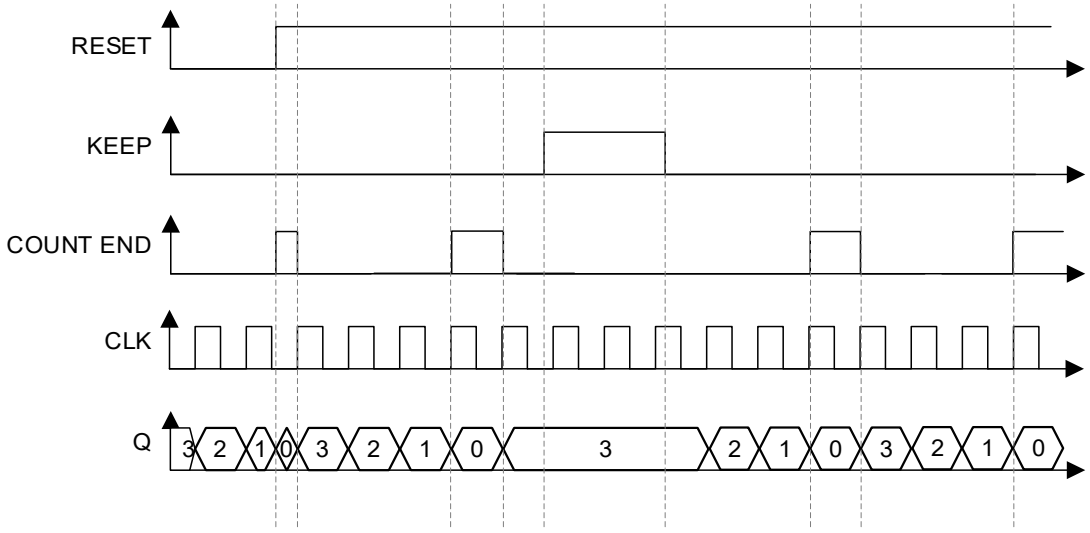
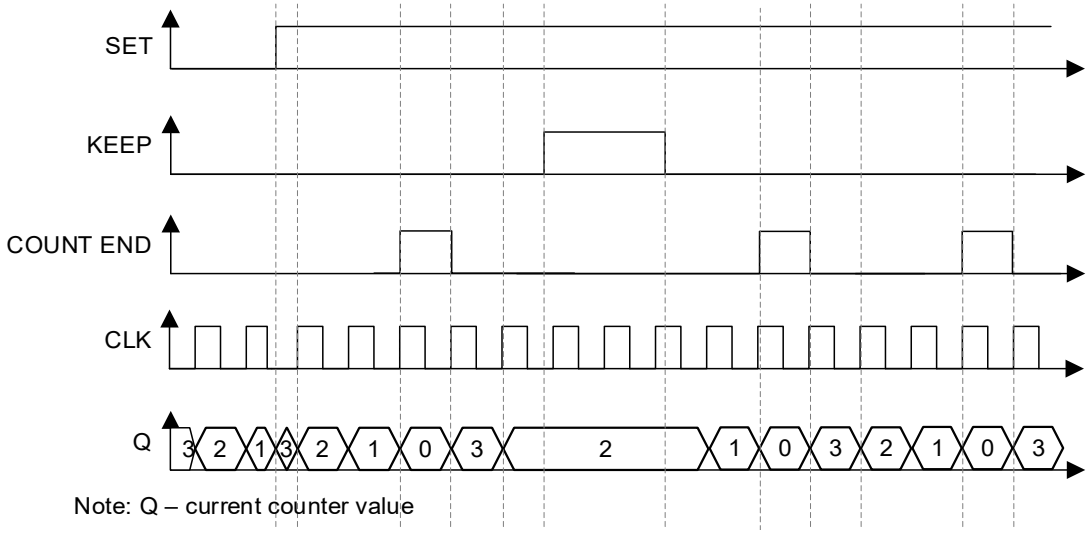


Figure 75. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3



Note: Q – current counter value

Figure 76. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

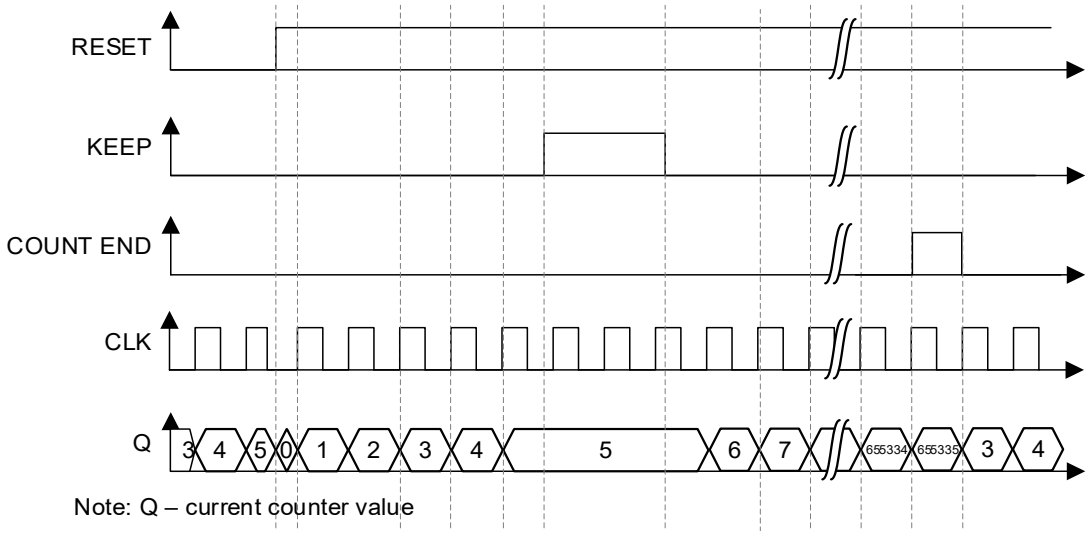


Figure 77. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

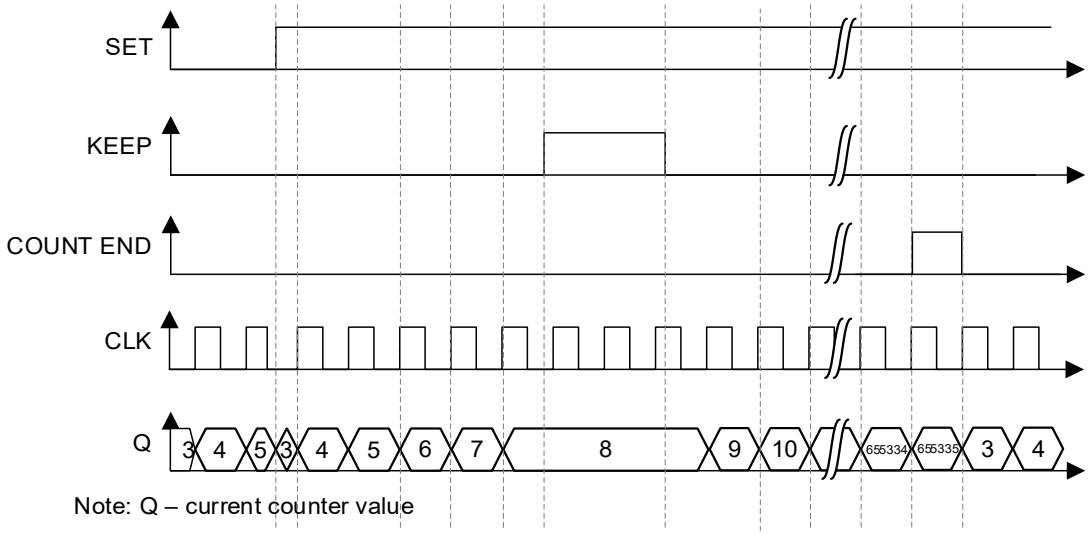


Figure 78. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator Is Forced On, UP = 1) for Counter Data = 3

11.3.8 The Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. Compared to Counter mode, in Delay/One-Shot/Frequency Detect modes the counter value is shifted for two rising edges of the clock signal.

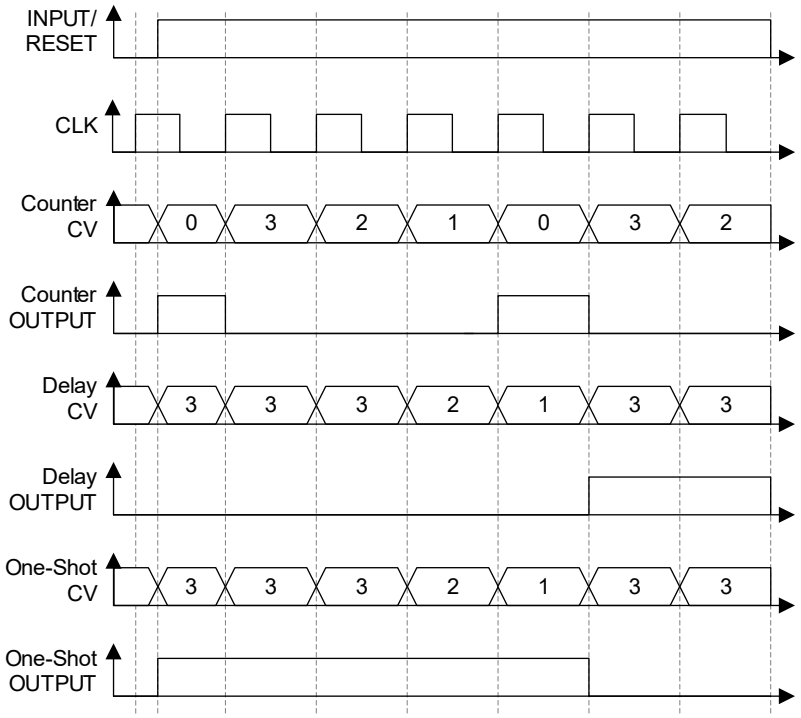


Figure 79. Counter Value, Counter Data = 3

11.4 Wake and Sleep Controller

SLG47104 has a Wake and Sleep function for General Purpose ACMP. The macrocell CNT/DLY0 can be reconfigured for this purpose by setting register [918] = 1 and registers [904:903] = 11. The WS serves for power saving, it allows to switch on and off selected General Purpose ACMP on a selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in the wake and sleep timing in case it dynamically powers on/off.

Note 2: Wake time should be long enough to make sure ACMP and V_{REF} have enough time to get a sample before going to sleep.

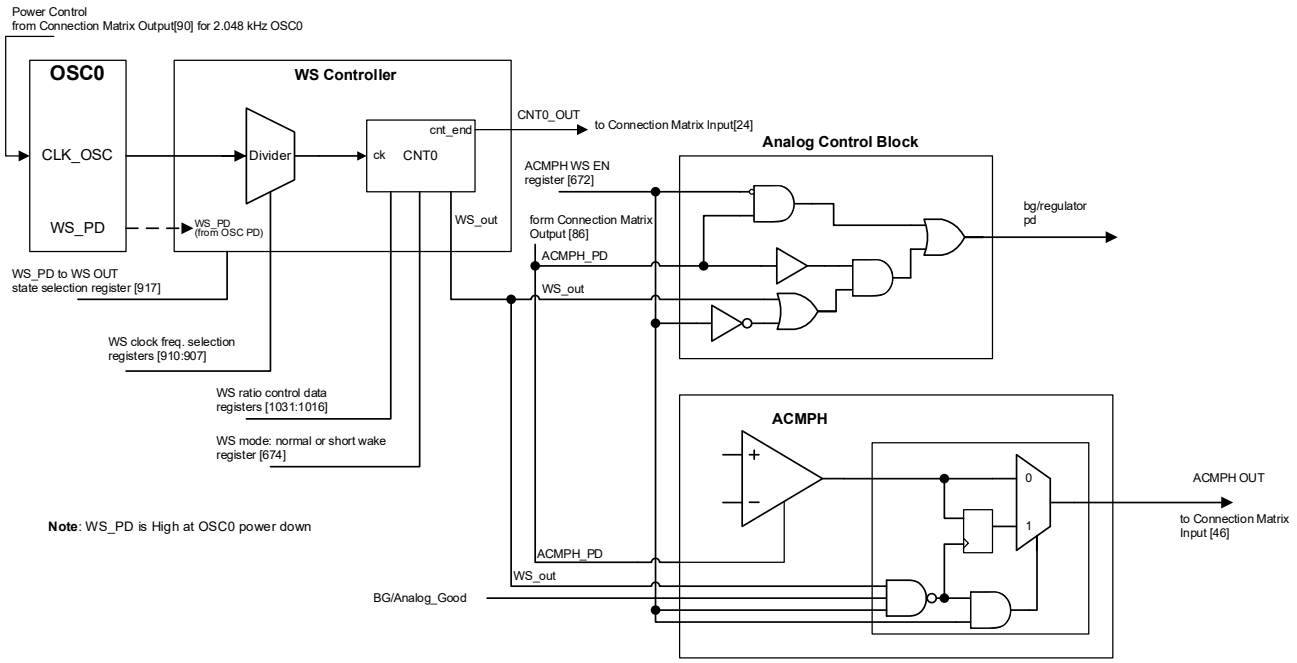
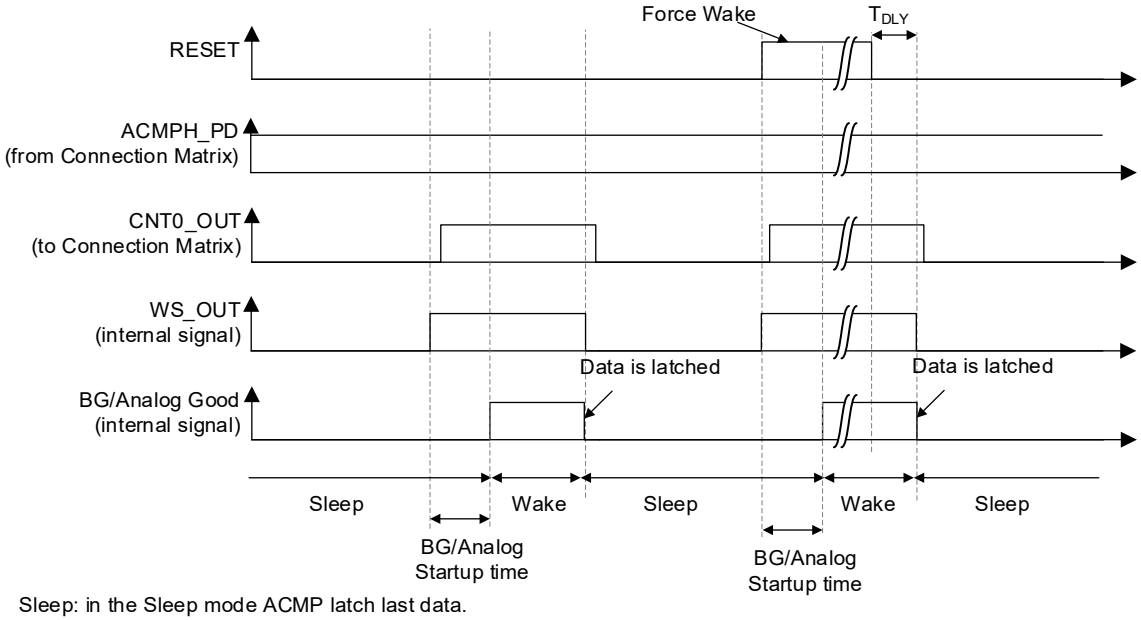
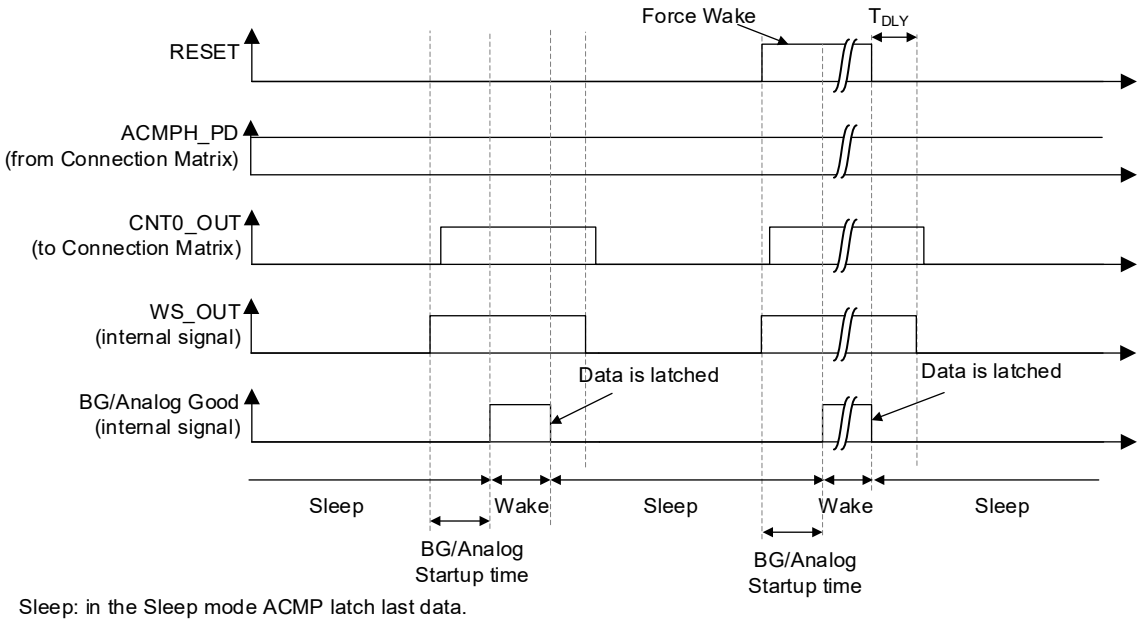


Figure 80. Wake/Sleep Controller



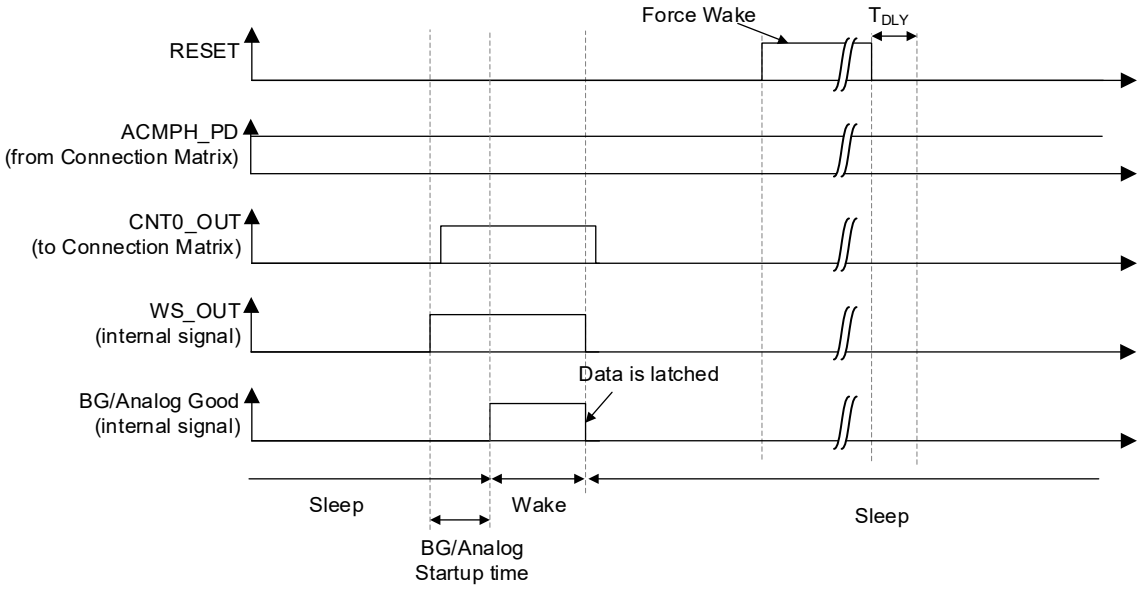
Sleep: in the Sleep mode ACMP latch last data.
Wake: a normal operation of ACMP. ACMP follow input.
T_{DLY}: time between falling edge at RESET input and 1st rising edge of WS clock.
CNT0_OUT is a delayed WS_OUT signal for 1us to make sure the data is correct during latch.

Figure 81. Wake/Sleep Timing Diagram, Normal Wake Mode, Couznter Reset is Used



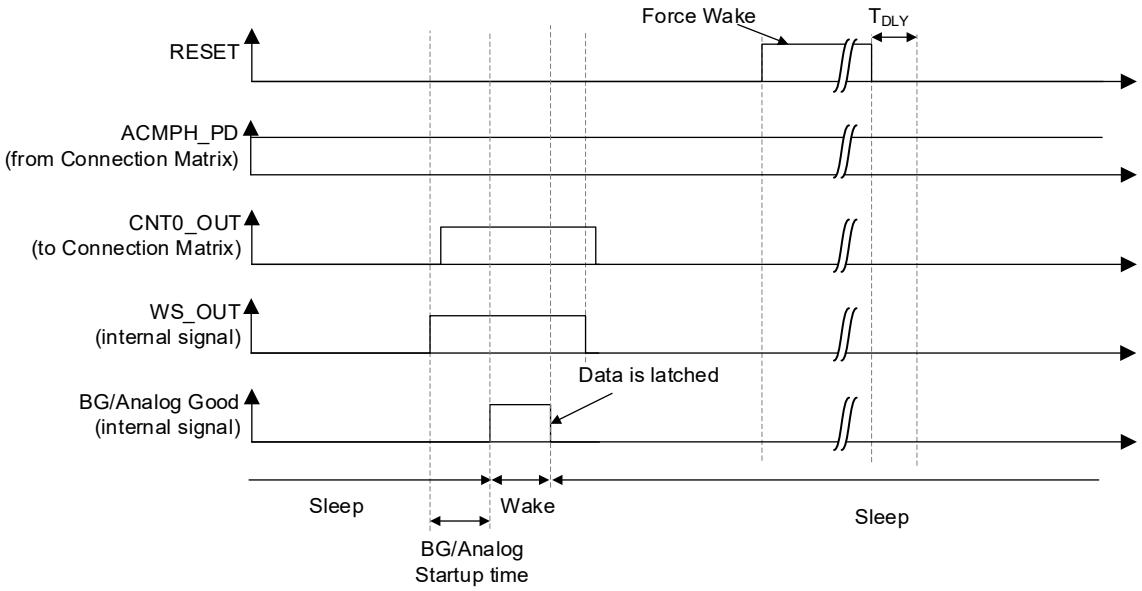
Sleep: in the Sleep mode ACMP latch last data.
Wake: a normal operation of ACMP. ACMP follow input.
T_{DLY}: time between falling edge at RESET input and 1st rising edge of WS clock.
CNT0_OUT is a delayed WS_OUT signal for 1us to make sure the data is correct during latch.

Figure 82. Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Sleep: in the Sleep mode ACMP latch last data.
Wake: a normal operation of ACMP. ACMP follow input.
T_{DLY}: time between falling edge at RESET input and 1st rising edge of WS clock.
CNT0_OUT is a delayed WS_OUT signal for 1us to make sure the data is correct during latch.

Figure 83. Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Sleep: in the Sleep mode ACMP latch last data.
Wake: a normal operation of ACMP. ACMP follow input.
T_{DLY}: time between falling edge at RESET input and 1st rising edge of WS clock.
CNT0_OUT is a delayed WS_OUT signal for 1us to make sure the data is correct during latch.

Figure 84. Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog startup time will take maximal 2 ms. Therefore, 8 periods of the Oscillator0 are recommended for the wake time, when BG is configured to Auto Power mode. If low power BG is always on, Oscillator0 period is longer than required wake time. The short wake mode can be used to reduce the current consumption. The short wake mode is edge triggered when the wake signal is latched by a rising edge and released the Power-On signal after the ACMP output data is latched. This allows to have a valid ACMP data for any type of wake signal and have the optimized current consumption.

To use any ACMP under WS controller, the following settings must be done:

- ACMP Power-Up Input from matrix = 1
- CNT/DLY0 must be set to Wake and Sleep Controller function
- Register WS → enable
- CNT/DLY0 set/reset input = 0.

As the OSC, any oscillator with any pre-divider can be used. The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMP remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.

  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)

  The user can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMP. When Reset signal goes out, the WS counter will go Low and turn off the ACMP until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMP. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMP while counter is counting up to the end.

Note: The OSC0 matrix power down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode

  High level Set/Reset - switches mode Set/Reset when level is High

Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPH on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMP on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required com- paring time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMP on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 1.

12. Pulse Width Modulator Macrocell

The SLG47104 has one Pulse Width Modulator (PWM) block. Inputs/Outputs for the macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

PWM macrocell features:

- 8-bit (7-bit) PWM Resolution
- I²C/Matrix/Auto dynamically changeable Duty Cycle
- Changeable Period by changing PWM clock source
- Flexible OSC-integrated divider for PWM period selection
- I²C Duty cycle read/write
- Synchronous change of all PWM blocks by sequential I²C write command
- Configurable dead band option for OUT+ and OUT-
- 16 Preset Duty Cycle Registers Switching Mode (for PWM sine or other waveforms)
- Autostop at 0 % and 100 % of PWM duty cycle value
- Synchro OFF Mode (wait for PWM period end before stop block)
- Inv/non-Inv macrocell Output options
- From 0 %, 0.4 % to 99.6 %,100 % Duty cycle for 8-bit resolution.

12.1 8-bit/7-bit PWM Configurations

When configured as PWM, this macrocell has an 8-bit resolution. It is also possible to select 7-bit PWM resolution if the higher PWM frequency is needed.

The PWM block consists of two 8-bit counters. First one, named PWM Period CNT, is used to create PWM period and the second one, named PWM Duty Cycle CNT, is used to set PWM Duty Cycle and to make dynamic changes in PWM functionality.

There is an ability to change the Duty Cycle from 0 % to 100 %. The PWM duty cycle step is 0.4 % for 8-bit resolution and 0.8 % for 7-bit resolution mode. This step is constant in the whole range. Both 0 % and 100 % are included.

12.2 PWM Inputs

- Duty Cycle CNT Up/Down is the signal for defining the direction of duty cycle change.
  - If Duty Cycle CNT Up/Down = 1, the duty cycle increases from current value up to 255.
  - If Duty Cycle CNT Up/Down = 0, the duty cycle decreases from current value down to 0.
- Duty Cycle CNT Keep/Stop.
  - When Keep function is selected (register [1479] = 0) HIGH logic level on this input disables the change of Duty Cycle CNT (clock for Duty Cycle CNT is blocked). However, PWM block still generates PWM output with a constant duty cycle.
  - When Stop function is selected (register [1479] = 1) HIGH logic level on this input disables the change of both Duty Cycle CNT and PWM Period CNT. Consequently, if Stop signal is active (logic HIGH) the output of PWM block remains constant.

    Note that if no other macrocells except PWM block use the internal OSC, the logic HIGH on Stop input disables the work of internal OSC that is used as a clock source for PWM Period CNT. For this case, logic LOW on this input enables OSC again.
- Duty Cycle CNT CLK is the clock signal for incrementing/decrementing duty cycle value. Keep in mind that the actual duty cycle value will be updated during the next PWM period.
- Power-down (PD) is an active high-level signal for updating Duty Cycle to default user-defined value. Keep in mind, that user can change the default Duty Cycle value via I²C. The PD signal will apply right away when Sync Off (register [1475] = 1) and after PWM period is completed when Sync On (register [1475] = 0 (Note)). HIGH logic level on PD input disables the change of all PWM internal counters and stops the internal oscillator

(if internal OSC is not used by other macrocells) (see section 12.10 SYNC On/Off Setting for Power-Down Signal). This function is individual for each PWM block.

Note that for async mode a minimal time duration for HIGH level at PD input is 100 ns, which guarantee PWM response. A pulse shorter than 100 ns might be ignored. An input pulse will be extended internally to this minimal required time to power down the PWM block.

- Ext PWM Period CNT CLK is clock input for PWM Period CNT. The clock at this input defines PWM signal frequency. PWM Period CNT CLK comes from the internal predefined clock or from the matrix for the high flexibility of PWM frequency.

Note: First PWM period will be 2-3 clocks longer after PD signal is released.

12.3 PWM Outputs

- OUT+: PWM positive output
- OUT-: PWM negative output
- PWM_PERIOD: PWM start period pulse (the duration of the high level is equal to one period of the PERIOD CNT CLK).

12.4 I²C/Matrix/Auto Dynamically Changeable Duty Cycle and Period

Duty Cycle in PWM macrocell can be changed in two ways:

1. PWM Duty Cycle CNT block has two parameters: Counter Data and Current Counter Value. The Current Counter Value defines PWM Duty Cycle. Counter Data of PWM Duty Cycle CNT can be changed by I²C commands with a reload into Current Counter Value. In this case, I²C Controller can change PWM Duty Cycle by I²C. Therefore, Counter Data of PWM Duty Cycle CNT must support change via I²C.
2. Matrix changeable Duty Cycle. In this case "Duty Cycle CNT CLK" and "Duty Cycle CNT Up/Down" inputs are used. Rising edge at "Duty Cycle CNT CLK" changes Current Counter Value corresponding to "Duty Cycle CNT Up/Down" input state: if "Duty Cycle CNT Up/Down" is LOW then Current Counter Value decreases and vice versa.

PWM period (frequency) can be changed only by changing PWM Period CNT Clock source. There are several different clock options available for user selection. Therefore, for PWM frequency flexibility an OSC-integrated CNT divider can be used.

12.5 I²C PWM Duty Cycle Read/Write

The I²C Controller should be able to reliably read and write duty cycle value into PWM block. Synchro Buffer is used for correct I²C reading of actual PWM duty cycle. The I²C command has some time duration. Synchro Buffer captures actual PWM duty cycle for read command and I²C Controller can read this data without errors.

The I²C Controller can change PWM duty cycle via I²C write command. The newly written PWM duty cycle value will be loaded (but not applied) to the PWM block as the default value. The load will happen when I²C "stop" command is issued. To apply a default value to PWM block user must set the "I²C Trigger" bit to 1 via I²C interface. Note, that this value will be applied after the current PWM period.

If the user wants to change both PWM blocks simultaneously, I²C sequential write command must be used.

Note: Avoid the change of PD signal during I²C read, since it causes the buffer value to update.

12.6 Flexible OSC-Integrated Divider

The OSC-integrated divider is built into 25 MHz OSC to configure the PWM period. This divider can be used for other chip resources. There is 8-bit Counter with the source from OSC pre-divider and output to the matrix or directly to CNT/DLY block as one possible selection. In many cases, for all PWM macrocells, the same clock frequency is used. It is possible to use this Flexible OSC divider for fine frequency tuning of PWM cells.

The counter in flexible divider can be enabled/disabled by the register bit [741] only. When the counter in flexible divider is enabled, it will start to count down from the counter data till 0. That is why the frequency division is

counter data + 1. Minimum frequency after Flexible OSC-integrated Divider is at least twice smaller than input Flexible OSC-integrated Divider frequency. Counter will not count with 0b00000000 counter data. There is a separate register bit selection to enable the flexible divider output to the connection matrix.

Counter flexible divider resets with POR or RESET signal.

12.7 Inverted Output Option

By default, PWM output begins from HIGH logic level and after reaching duty cycle value, output changes to LOW logic level. Optionally the user can invert outputs of PWM block.

The PWM macrocell Outputs has an inverter option enabled by registers. It is necessary for simple driving of different LED types (common Anode/common Cathode), and others. Each OUT+ and OUT- outputs has one separate register to select its inverted/non-inverted output option.

12.8 Changeable Dead Band Option for OUT+ and OUT-

Dead band parameter is needed to drive external power FETs. The dead band helps to avoid short through for high power FETs. Dead band parameter is configurable for driving different external transistor. It is possible to select no dead band time or dead band equal to one, two or three PWM Period clock cycles.

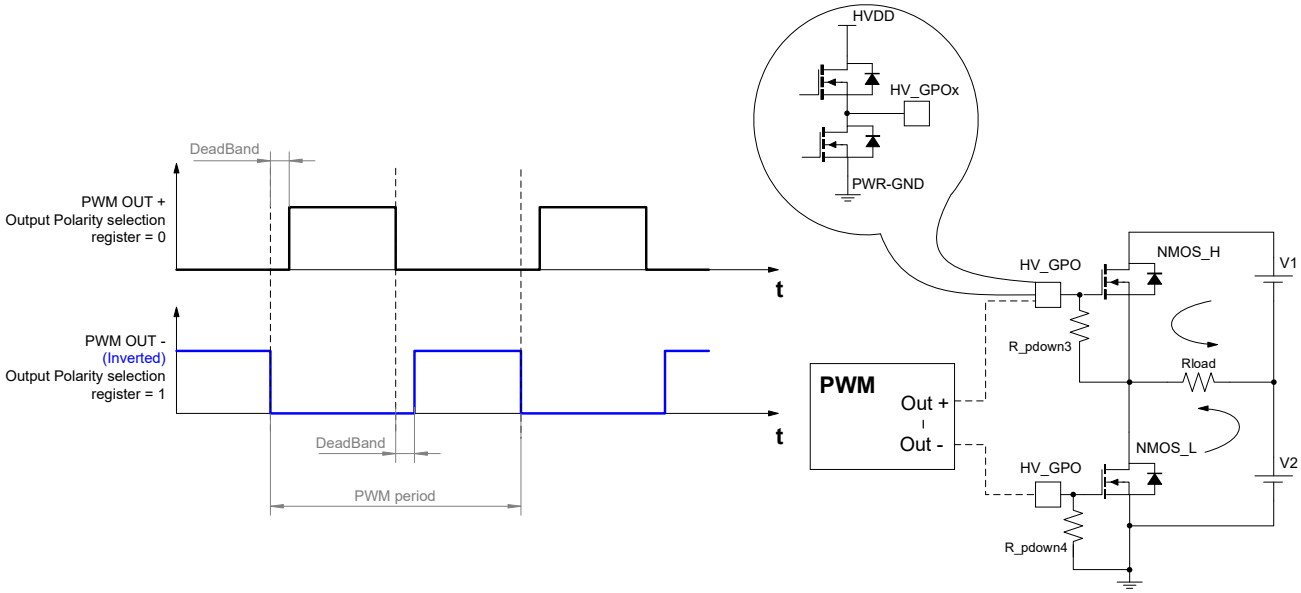


Figure 85. PWM Output Waveforms and Test Circuit Example for Driving NMOS FETs

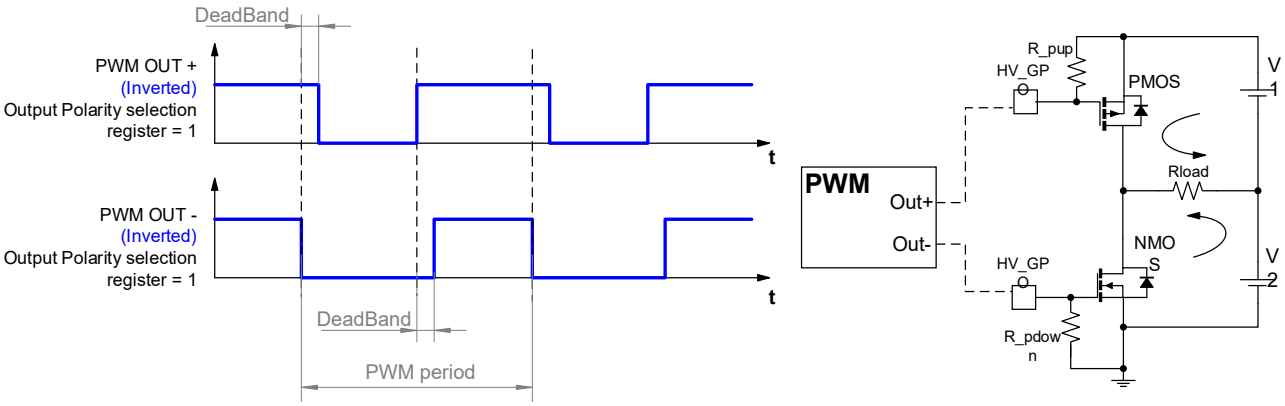


Figure 86. PWM Output Waveforms and Test Circuit Example for Driving NMOS and PMOS FETs

Note that external FETs must have Pull-up/Pull-down resistors between Gate and Source terminals to avoid unpredictable behavior of FETs when output pins of SLG47104 are in Hi-Z state (Sleep Mode).

The waveforms for Phase Correct PWM Mode are shown in Figure 87. Note that in Phase Correct PWM mode dead band delay is applied after phase correction, Figure 93.

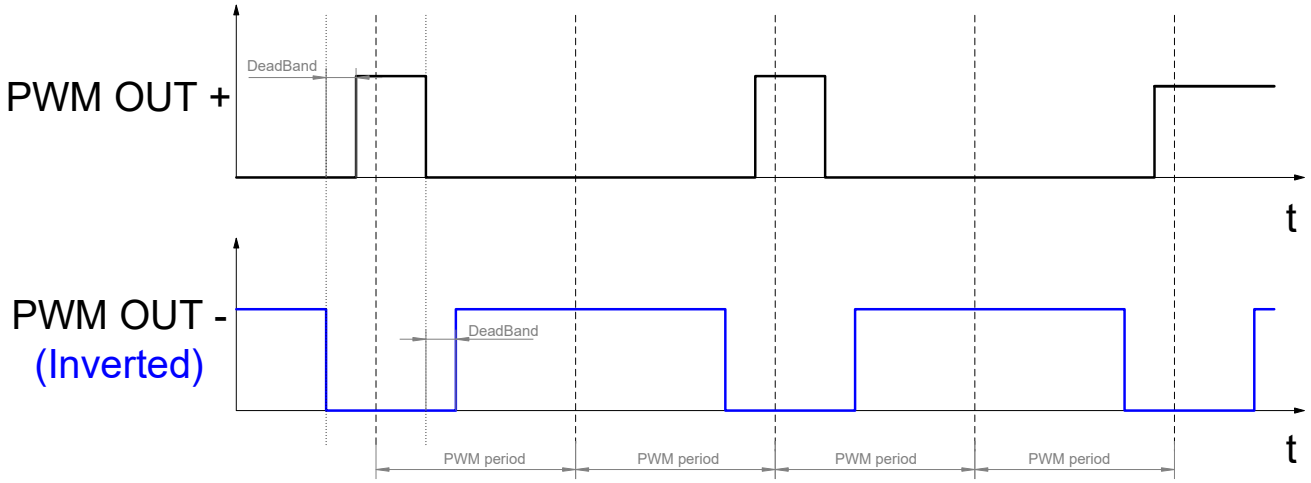


Figure 87. PWM Output Waveforms for Phase Correct PWM Mode

12.9 Initial PWM Value

Initial PWM duty cycle value is selected by Counter Data of PWM Duty Cycle CNT for regular mode. If Preset Registers Mode is selected, the initial value of PWM Duty Cycle CNT (Counter Data) is the preset registers address. Please refer to section 12.11 Regular/Preset Registers Mode.

12.10 SYNC On/Off Setting for Power-Down Signal

"SYNC On/Off" registers define the behavior of Power-down signal. This is the individual setting for each PWM macrocell. If this option is disabled (register [1475]), the PWM output goes low right away by active Power-down, Figure 88. If this option is enabled, the PWM block will finish the current PWM period and then will go low, Figure 91.

SYNC On/Off has no effect on duty cycle change via I^2C. In the case of duty cycle change via I^2C interface, new duty cycle value will be applied to PWM macrocell only after finishing the current PWM period.

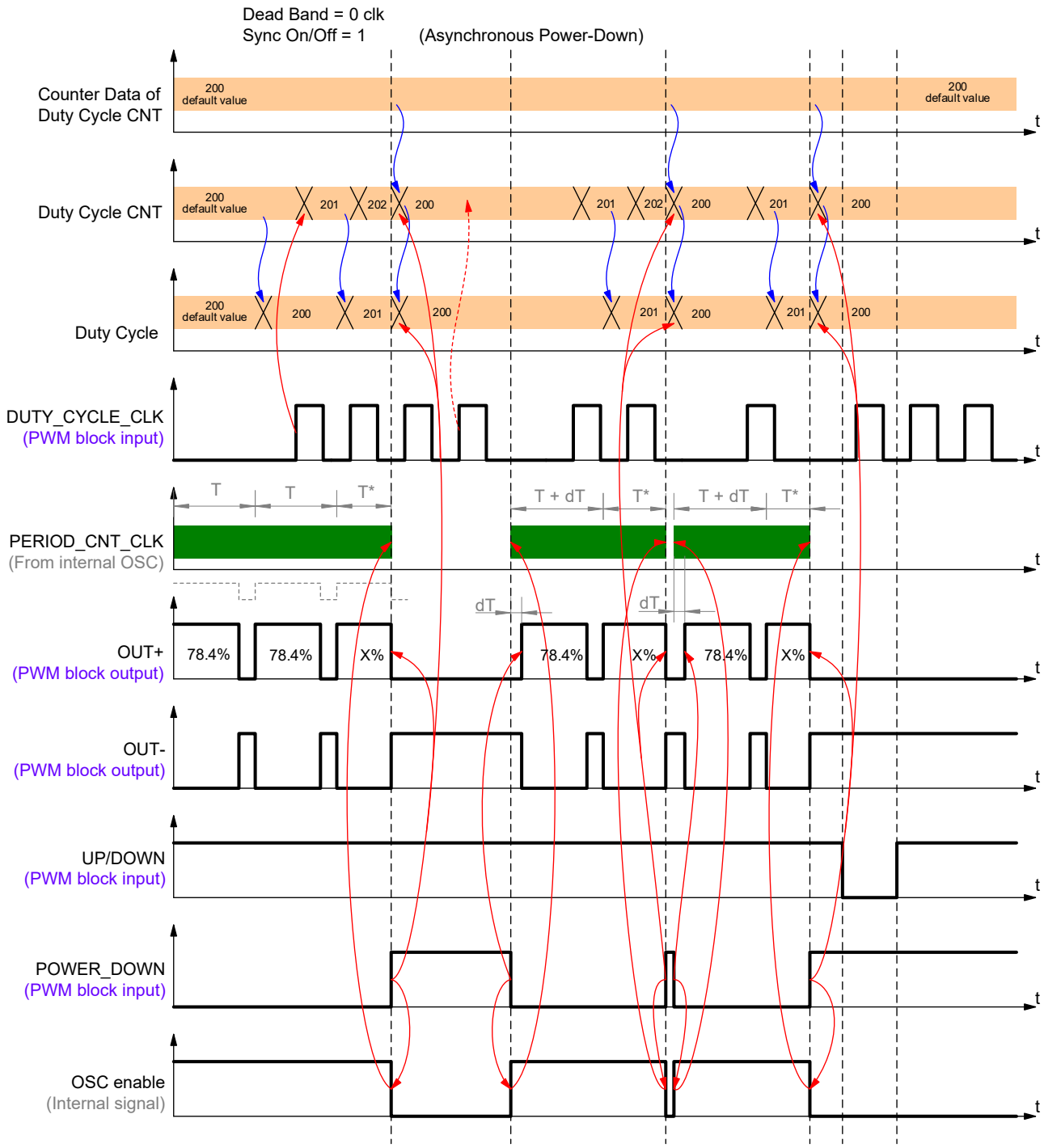


Figure 88. Power-Down with SYNC On/Off = 1 and Dead Band = 0 CLK

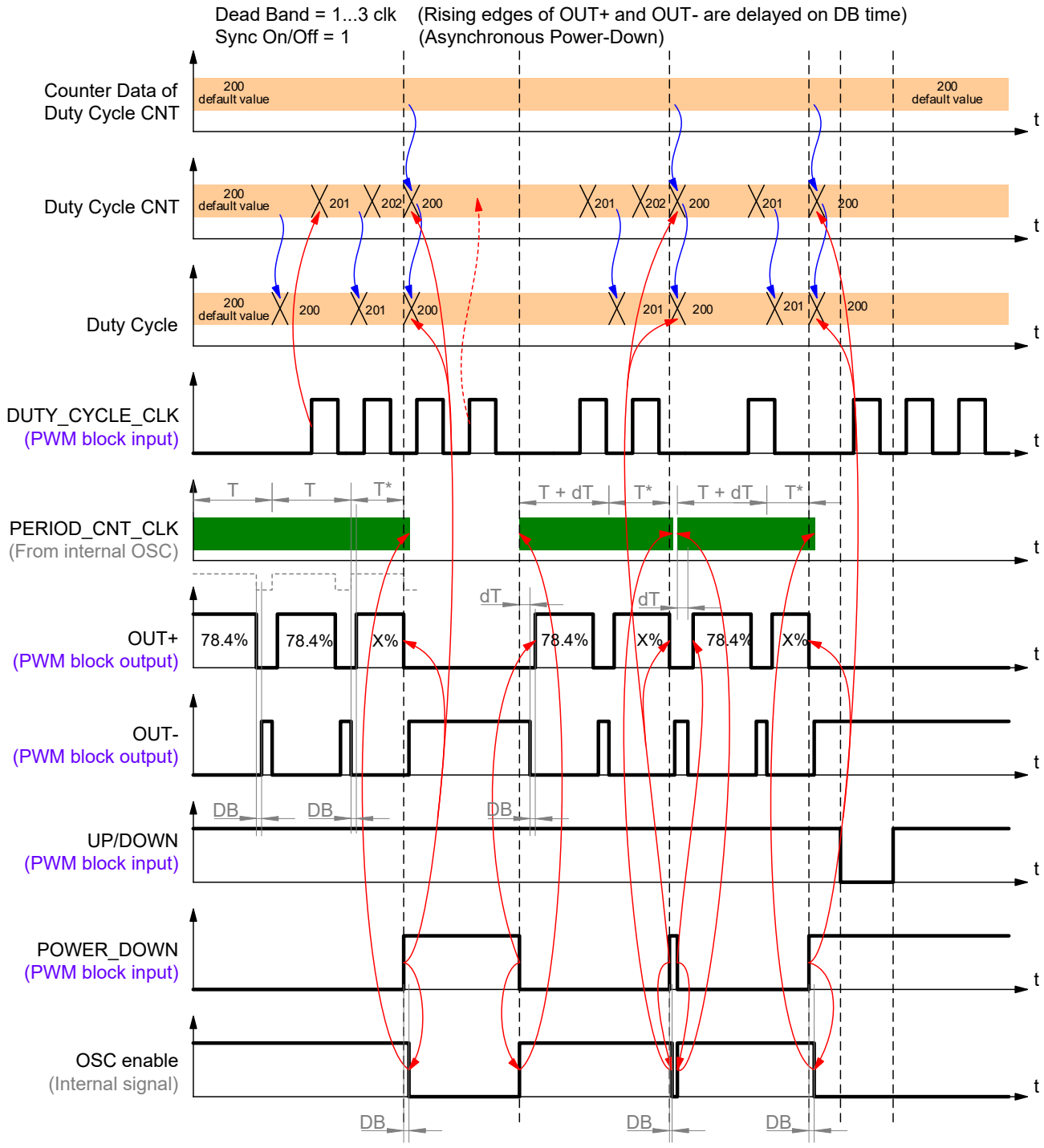


Figure 89. Power-Down with SYNC On/Off = 1 and Dead Band = 1 to 3 CLK

In Figure 88 to Figure 91:

- dT = 2-3 CLK and it is the additional number of clock pulses, that make first PWM period longer, after releasing PD signal.
- DB - user selected Dead Band time between OUT+ and OUT-.
- T* means the short period of x % duty cycle (T* < 255 PERIOD_CNT_CLK), that is finished at the moment of PD signal com- ing.

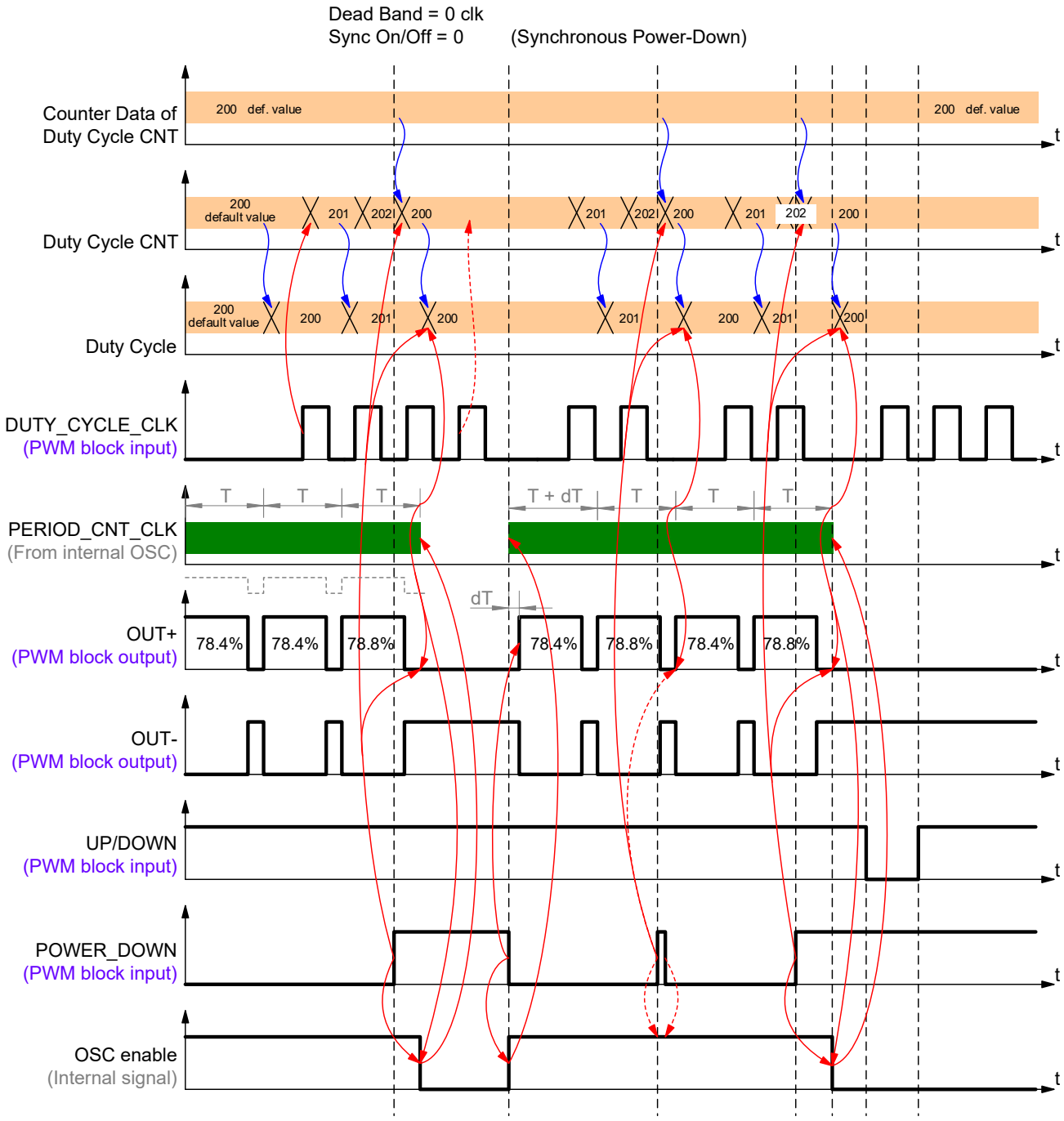


Figure 90. Power-Down with SYNC On/Off = 0 and Dead Band = 0 CLK

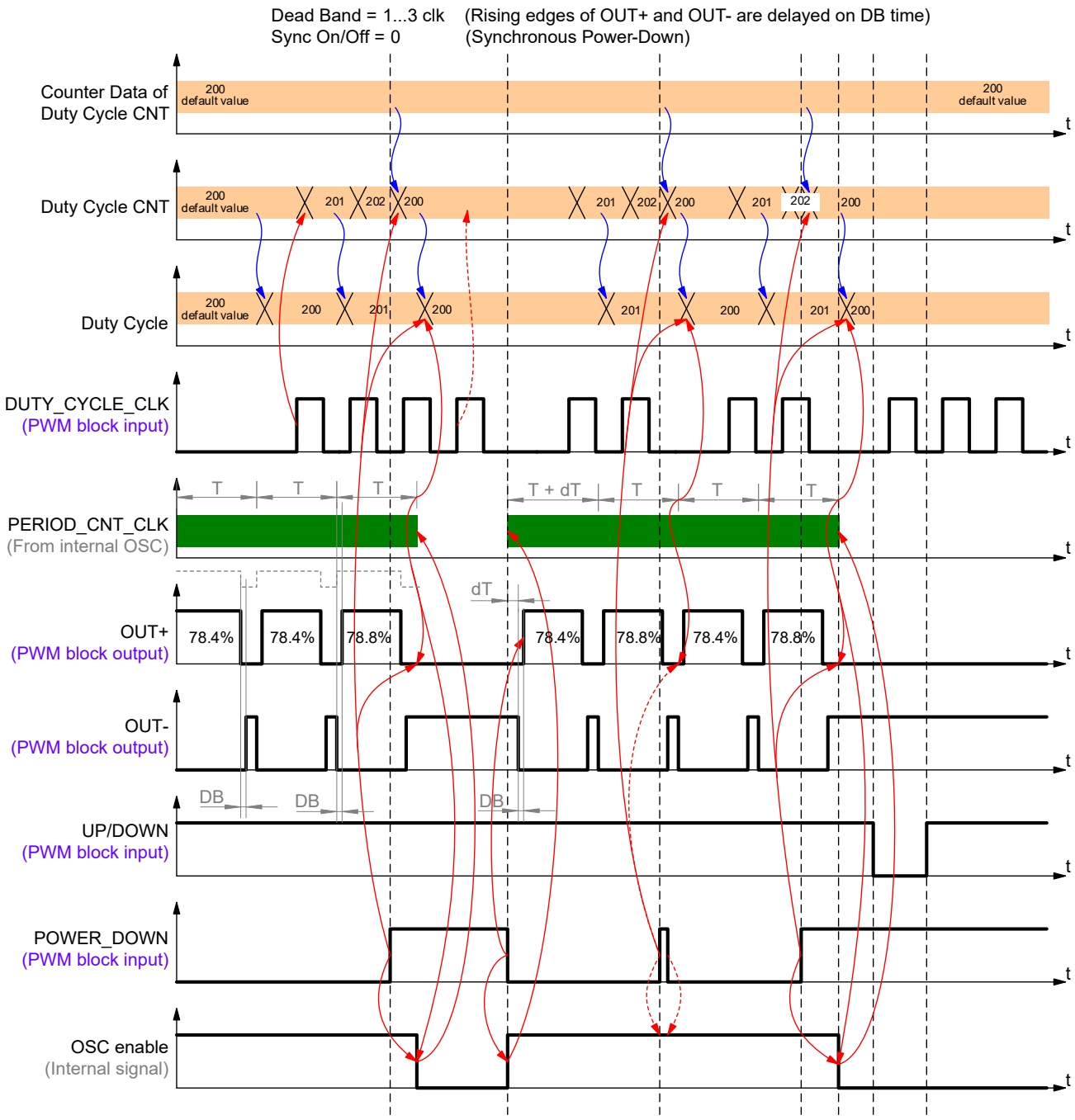


Figure 91. Power-Down with SYNC On/Off = 0 and Dead Band = 1 to 3 CLK

12.11 Regular/Preset Registers Mode

In Regular Mode the value of duty cycle is changed every rising edge on Duty Cycle CNT CLK input. In Preset Registers Mode the duty cycle is changed according to 16 predefined values, named Reg File, every rising edge on Duty Cycle CNT CLK input.

Selectable Preset registers are reserved to determine 16 different PWM Duty Cycle values. In Preset Registers mode the "Up/ Down" input and "Duty Cycle CNT CLK input" change the address of Preset Register, that will be applied to PWM block at the rising edge on "Duty Cycle CNT CLK input".

One 16-byte Preset Register is shared between two PWM macrocells.

Each PWM block can select Reg File as Duty Cycle source. When the Reg File is selected as a source, there are three options: use all 16 bytes, use less significant 8 bytes, or use most significant 8 bytes. In this case,

4-bits (when using 16-Bytes Reg File) or 3-bits (when using any of 8 bytes Reg File) LSB Current Value of PWM Duty Cycle CNT is used to select data address inside the Reg File. The counter data of the Duty Cycle CNT will define the initial starting point in the Reg file. So, each PWM block has its own initial position in the Reg File.

Table 33. Regular/Preset Mode Registers

Register Name	Mode of Operation	Register Definition
PWMx: Duty Cycle source	Regular Mode	00: from PWM Duty Cycle CNT
	Preset Registers Mode	01: 8-byte MSB of RegFile
		10: 8-byte LSB of RegFile
		11: 16-byte RegFile

For more detailed description see Table 35.

12.12 PWM Continuous/Autostop Mode

“Continuous/Autostop mode” register enables Autostop mode. This mode can be used with both Preset Registers or Regular Mode.

If PWM block works in Continuous Mode (register [1476] = 0), PWM Duty Cycle CNT will overflow when it reaches boundaries. For example, for PWM Duty Cycle Counter counts up: $254^{th} \rightarrow 255^{th} \rightarrow 0^{th} \rightarrow 1^{st}$, and for PWM Duty Cycle Counter counts down: $1^{st} \rightarrow 0^{th} \rightarrow 255^{th} \rightarrow 254^{th}$ …

Or in Preset Registers Mode, when Continuous Mode is selected (register [1476] = 0): counting up $14^{th} \rightarrow 15^{th} \rightarrow 0^{th} \rightarrow 1^{st}$, and counting down $1^{st} \rightarrow 0^{th} \rightarrow 15^{th} \rightarrow 14^{th}$ …

If Autostop mode is active (register [1476] = 1), PWM duty cycle counter will stop when it reaches boundaries. The conditions of Autostop are the next:

- PWM Duty Cycle reaches the value 0 in Regular Mode or Least Significant Byte of Preset registers in Preset Registers Mode, and Up/Down is LOW logic level (counting Down).
- PWM Duty Cycle reaches the value 255 (127 in 7-bit submode) in Regular Mode or Most Significant Byte of Preset registers in Preset Registers Mode and Up/Down is HIGH logic level (counting Up).

12.13 Internal Oscillator Auto Disable Mode

There is an OSC Auto Disable/Enable control, in which internal OSC is enabled only when it is required for PWM block. This Auto Disable Mode will operate only if user selects internal oscillator as a clock source for PWM Period Clock Counter ("PWM Period Clock Source selection" registers have a value from b0000 to b1001).

If the user selected PWM Period CNT overflow event as a clock source for Duty Cycle Counter (registers [1485:1484] = 01, or registers [1485:1484] =10, or registers [1485:1484] = 11), then no clocks will be on Duty Cycle Counter Clock input when PWM enters to Autostop State (see Table 34).

The conditions, in which internal OSC will be automatically disabled, are shown in Table 34.

Table 34. Conditions for Disabling/Enabling an Internal Oscillator

No	Disable Condition	Delay before OSC in Disabled	Enable Condition
1	PD signal goes HIGH	Disable OSC immediately if SYNC On/Off register [1475] = 1	PD signal goes LOW
		Disable OSC after current duty cycle period if SYNC On/Off register [1475] = 0	
2	Stop signal goes HIGH	Disable OSC immediately	Stop signal goes LOW

No	Disable Condition	Delay before OSC in Disabled	Enable Condition
3	Up/Down is logic HIGH (counting up) and actual PWM value is 255 (127 for 7-bit submode), "PWM boundary OSC automatically disable" (register [1477] = 1]) "Continuous/Autostop mode"(register [1476] = 1) (Figure 92)	Disable OSC after one full PWM period	Up/Down signal changes its level to logic LOW (count down) (Figure 92)
4	Up/Down is logic LOW (counting down) and actual PWM value is 0, "PWM boundary OSC automatically disable" (register [1477] = 1) and "Continuous/Autostop mode"(register [1476] = 1)	Disable OSC after one full PWM period	Up/Down signal changes its level to logic HIGH (count up)

Note 1: If PWM boundary OSC automatically disable register [1477] = 1 and PWM works with Preset Registers (registers [1483:1482] = 01 or registers [1483:1482] = 10, or registers [1483:1482] = 11), internal OSC will stop if Preset Registers Index = 15 (7 when LSByte mode of Preset Registers is used) the Preset Register Index remains unchanged until Up/Down signal changes. The same behavior has zero Preset Register Index (8 when MSByte mode of Preset Registers is used). When this index will be reached and OSC Auto Disable Mode is active the Preset Register Index remains unchanged until Up/Down signal changes.

Note 2: Other macrocells that use OSC, can start it or keep it enabled even if OSC Auto Disable Mode is active and condition for disabling OSC occurs.

Note 3: If dead band is different from 0, then OSC will be disabled for Dead Band Time later.

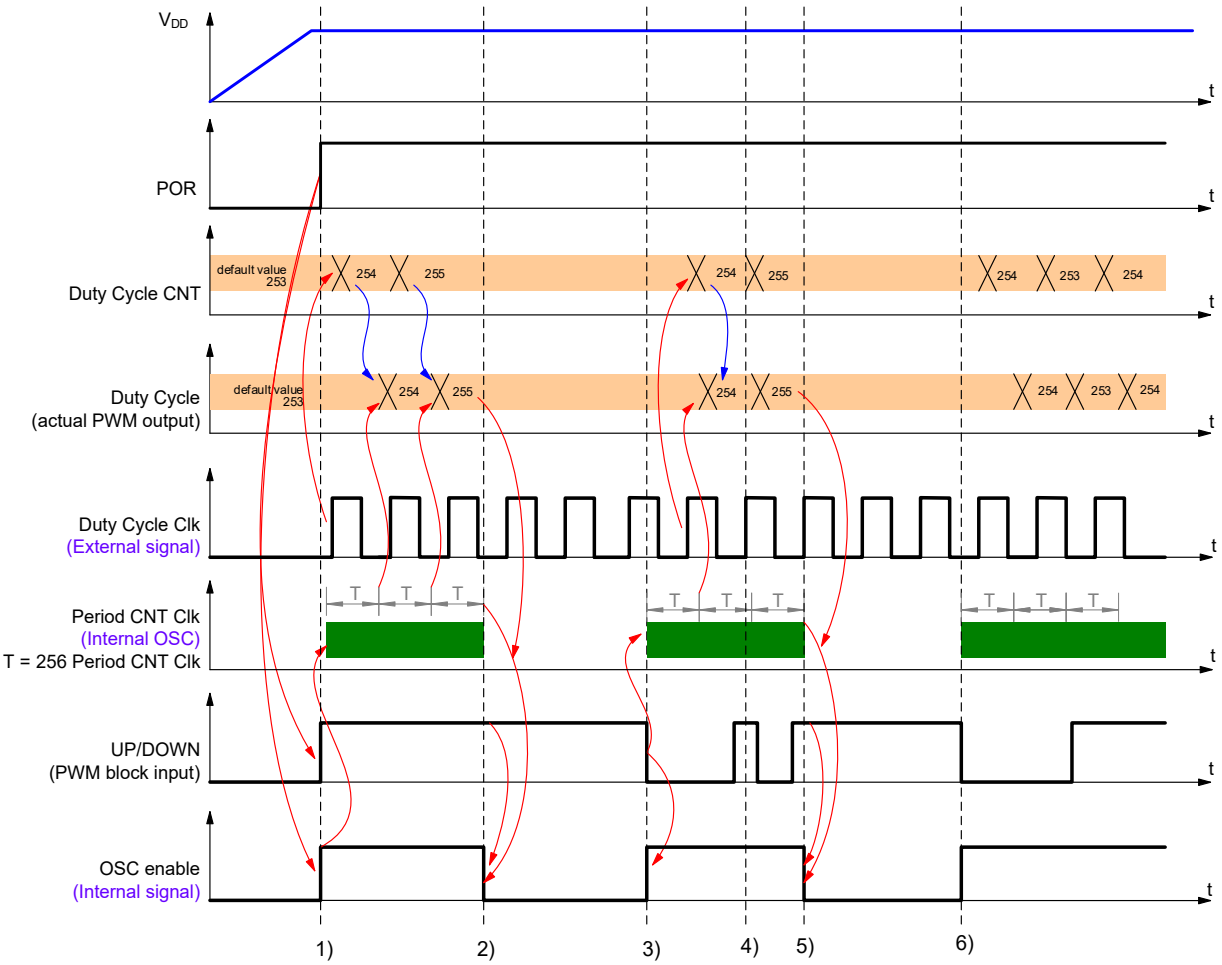


Figure 92. Example of PWM Auto Oscillator Control

In the example in Figure 92, Duty Cycle CLK is external to PWM block signal, Period CNT CLK is a signal from internal OSC. "PWM boundary OSC automatically disable" register [1477] = 1. Autostop Mode is active too ("Continuous/Autostop mode" register [1476] = 1). The key events of Autostop are the next:

- Event 1) after chip start-up, OSC is enabled. The clock from internal OSC is used to generate PWM period. Duty Cycle CNT counts up since Up/Down input of PWM macrocell is logic HIGH. Note that first OSC pulse is delayed when OSC becomes enabled (see section 3.5.8 Oscillator Specifications).
- Event 2) the value of Duty Cycle CNT is updated every rising edge at Duty Cycle CLK input. This value becomes valid at the beginning of every PWM period.
- When the Duty Cycle value of 100 % is reached and Up/Down input is logic HIGH, PWM macrocell disables internal OSC after one full PWM period.
- Event 3) internal OSC starts working because Up/Down signal becomes LOW and Duty Cycle = 100 %. This is the scenario for starting OSC after it was automatically disabled.
- Event 4) the Up/Down signal changes the direction of Duty Cycle counting because at the moment of signals rising edge on Duty Cycle CLK input, the level of Up/Down input is logic HIGH.
- Event 5) OSC is disabled because the value of Duty Cycle is 100 % and at the beginning of the next PWM period the Up/ Down input is logic HIGH.
- Event 6) Since Up/Down goes low and Duty Cycle is equal to 100 %, this is the scenario for starting up the OSC.

12.14 Phase Correct PWM Mode

In normal mode, PWM output is HIGH, then LOW for each PWM period. When Phase correct PWM (also called Center Align) register is active (register [1478] = 1), the PWM output is HIGH, then LOW for the first period, then LOW again and HIGH for the second period. So, there are less edges (or less output switches) for the Phase correct PWM mode.

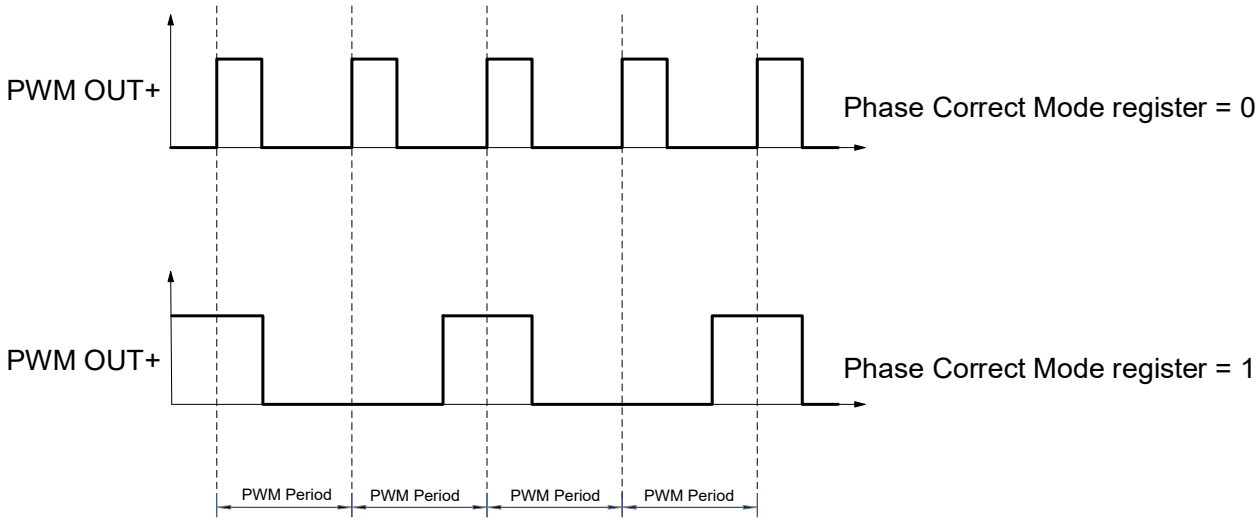


Figure 93. Phase Correct PWM Mode

12.15 PWM Period Output

PWM_PERIOD output indicates the start of the new PWM period at PWM_OUT+. This output doesn't depend on the PWM duty cycle. The duration of the high level is equal to one period of the PERIOD_CNT_CLK.

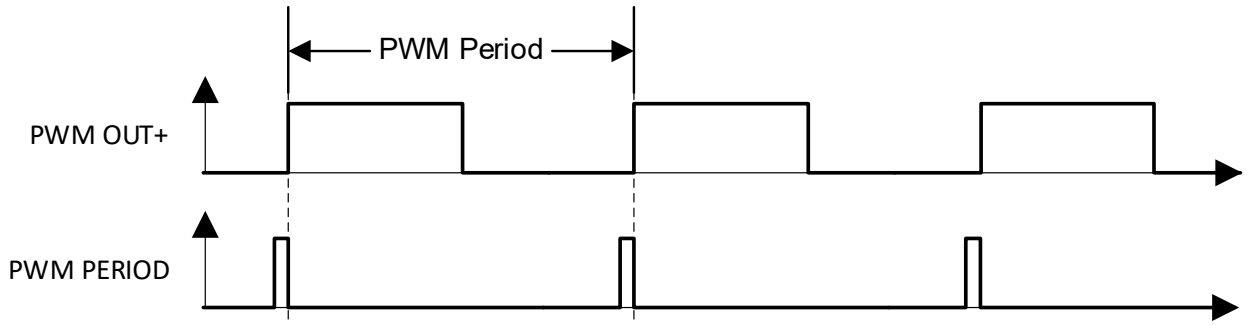


Figure 94. PWM Period Waveform

12.16 PWM Block Diagram

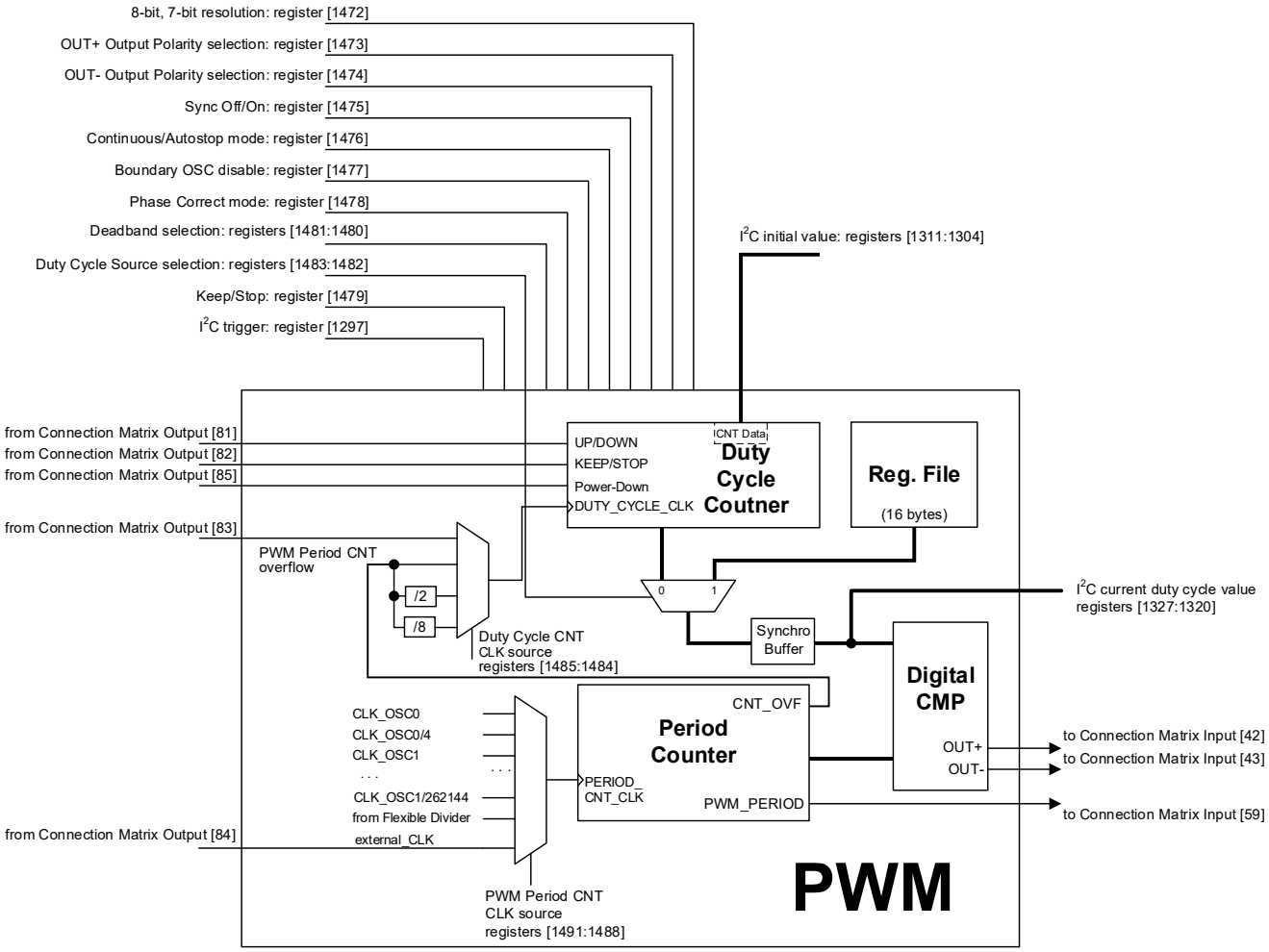


Figure 95. PWM Functional Diagram

12.17 PWM Register Settings

Table 35. PWM Register Settings

Signal Function	Register Bit Address	Register Definition
PWM: 8-bit or 7-bit resolution	1 bit [1472] register	0: 8-bit PWM 1: 7-bit PWM
PWM: OUT+ polarity selection	1 bit [1473] register	0: Non-Inverted Output 1: Inverted Output
PWM: OUT- polarity selection	1 bit [1474] register	0: Non-Inverted Output 1: Inverted Output
PWM: SYNC On/Off	1 bit [1475] register	0: Synchronous Power-Down 1: Asynchronous Power-Down
PWM: Continuous/Autostop mode	1 bit [1476] register	0: Continuous mode 1: PWM Duty Cycle Counter Autostop at 0 % or 100 %
PWM: Boundary OSC disable	1 bit [1477] register	0: OSC is always enabled at boundaries 1: Automatically Disable OSC
PWM: Phase Correct mode	1 bit [1478] register	0: Disable 1: Enable
PWM: Deadband selection	2 bits [1481:1480] registers	00: No Deadband 01: 1 PWM clock cycles 10: 2 PWM clock cycles 11: 3 PWM clock cycles
PWM: Keep/Stop selection	1 bit [1479] register	0: Keep 1: Stop
PWM: I^2C trigger	1 bit [1297] register	0: Do not update duty cycle value 1: Update duty cycle value
PWM: Duty Cycle source	2 bits [1483:1482] registers	00: from PWM Duty Cycle CNT (Regular Mode) 01: 8-byte MSB of RegFile (Preset Registers Mode) 10: 8-byte LSB of RegFile (Preset Registers Mode) 11: 16-byte RegFile (Preset Registers Mode)
PWM Period Counter Clock Source selection	4 bits [1491:1488] registers	0000: CLK_OSC0 0001: CLK_OSC0/4 0010: CLK_OSC1 0011: CLK_OSC1/8 0100: CLK_OSC1/64 0101: CLK_OSC1/512 0110: CLK_OSC1/4096 0111: CLK_OSC1/32768 1000: CLK_OSC1/262144 1001: From Flexible Divider 1010: Reserved 1011: Matrix OUT [79] (external clock)
PWM: Duty Cycle Counter Clock Source selection	2 bits [1485:1484] registers	00: Matrix output 01: PWM Period CNT overflow 10: every 2nd pulse of PWM Period CNT overflow 11: every 8th pulse of PWM Period CNT overflow
PWM: Preset 16-byte Registers byte [0...15]	16 bytes [1455:1328] registers	Preset 16 bytes Duty Cycle values

Signal Function	Register Bit Address	Register Definition
PWM: Initial value	8 bits [1311:1304] registers	Initial PWM Duty Cycle value
PWM: Current duty cycle value	8 bits [1327:1320] registers	Current PWM duty cycle value for I²C read

"Keep/Stop" register defines which function will be performed by "Duty Cycle CNT Keep/Stop" input. Keep/Stop signal is active HIGH level.

"PWM Period Clock Source selection" registers define clock source for "PWM Period CNT CLK" input: from the matrix, from OSCx and OSCx dividers, from the flexible OSC-integrated divider. Also, there is an option to select counter overflow condition as a source for PWM Period Clock.

"PWM: Duty Cycle Source selection" defines the clock source for changing the duty cycle. It can be:

- Clock source from the connection matrix.
- Clock pulse that is generated after the end of PWM cycle period (PWM Period Counter overflow). This pulse is generated every 255 (for 8-bit option) or 127 (for 7-bit option) PWM Period Clocks.
- Clock pulse that is generated once per 2 PWM period, or every 510 (for 8-bit option) or 254 (for 7-bit option) PWM Period Clocks.
- Clock pulse that is generated once per 8 PWM period, or every 2040 (for 8-bit option) or 1016 (for 7-bit option) PWM Period Clocks.

"I²C Trigger" register allows to update duty cycle value via I²C command:

- When I²C_Trigger = 0, PWM duty cycle isn't updated.
- When I²C_Trigger = 1, PWM duty cycle is updated from register at I²C stop pulse after the current PWM period is completed. The I²C_Trigger bit will be automatically cleared after the I²C stop pulse.

"SYNC On/Off" registers define the Power-down signal behavior on PWM block. This is the individual setting for each PWM macrocell. If this option is disabled (register [1475] = 1), then PWM output is changed right away by active Power-down. If this option is enabled (register [1475] = 0), the PWM block will finish the current PWM period and then will react to Power-down signal.

"Continuous/Autostop mode" register enables Autostop mode. This mode can be used with both Preset Registers or Regular Mode. If PWM block works in Continuous Mode (register [1476] = 0), PWM Duty Cycle CNT will overflow when it reaches boundaries. For example, for PWM Duty Cycle Counter counts up: $254^{th} \rightarrow 255^{th} \rightarrow 0^{th} \rightarrow 1^{st}$, and for PWM Duty Cycle Counter counts down: $1^{st} \rightarrow 0^{th} \rightarrow 255^{th} \rightarrow 254^{th}$ … If Autostop mode is active (register [1476] = 1), PWM duty cycle counter will stop when it reaches boundaries. Please refer to section 12.12 PWM Continuous/Autostop Mode.

"PWMx boundary OSC disable" is the function, that allows disabling internal oscillator when there is no need for PWM to be clocked (boundary is reached in Autostop Mode only). This feature is useful for energy saving, but the user can optionally disable it and keeps the oscillator always enabled.

"Phase Correct mode". In normal mode, PWM output is HIGH, then LOW for each PWM period. When Phase correct PWM (also called Center Align) register is active (register [1478] = 1), then PWM output is HIGH, then LOW for the first period, then LOW again, and HIGH for the second period. So, there are less edges (or less output switches) for the Phase correct PWM mode.

"Duty Cycle source" (registers [1483:1482]) defines the Regular Mode of operation (registers [1483:1482] = 00) or Preset Registers Mode (registers [1483:1482] = 01, registers [1483:1482] = 10, registers [1483:1482] = 11). In Regular Mode, the value of duty cycle is changed every rising edge on Duty Cycle CNT CLK input. In Preset Registers Mode the duty cycle is changed according to values, saved in 8-byte MSB of RegFile (registers [1483:1482] = 01), 8-byte LSB of RegFile (registers [1483:1482] = 10) or 16-byte of RegFile (registers [1483:1482] = 11). The address of RegFile value, that is applied to PWM block, is changed every rising edge on Duty Cycle CNT CLK input.

"OUT+ polarity selection" registers enable/disable inverted option for Output+ of PWM macrocell. "OUT- polarity selection" registers enable/disable inverted option for Output- of PWM macrocell.

"Deadband selection" registers [1480:1481] chose dead band time between OUT+ and OUT- signals. It is 0, 1, 2, or 3 clock period of PWM Period CNT CLK signal.

"8-bit/7-bit PWM resolution". It is possible to select 7-bit instead of default 8-bit resolution for the PWM to increase the PWM speed. If the 7-bit resolution is selected, the maximum value of the duty cycle counter is 127.

13. Analog Comparator

There is one Rail-to-Rail General Purpose Analog Comparator (ACMP) macrocell in the SLG47104. For the ACMP cell to be used in a GreenPAK design, the power-up signal (ACMPH_nPD) need to be active. By connecting to signal coming from the Connection Matrix, it is possible to have ACMP be on continuously, off continuously, or switched on periodically, based on a digital signal coming from the Connection Matrix. When ACMP is powered down, the output is low (the output remains its state while sleeping).

The General-Purpose Rail-to-Rail Analog Comparator is optimized for high-speed operation (ACMPH).

The ACMP cell has a positive input signal that can be provided by a variety of external sources and can also have a selectable gain stage before connection to the analog comparator. The ACMP cell has a negative input signal that is either created from an internal V_{REF} or provided by a way of the external sources.

Power-Up = 1 – ACMP is powered up.

Power-Up = 0 – ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then becomes valid after power up signal goes high for ACMPH (see parameter t_{start} in section 3.5.10 ACMP Specifications). Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 2 MΩ resistors. Internally generated IN- voltage range is: 0.032 - 2.016 V, while external IN- voltage range is 0 - V_{DD}.

The ACMP cell also has a hysteresis selection, to offer hysteresis of (0, 32, 64, 192) mV. The hysteresis option is available when using an internal V_{REF} only.

The ESD resistors should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}. See sections 6.6 ESD Protection to 6.9 Matrix OE IO Structure (for VDD Group).

ACMPH IN+ options are GPIO5, V_{DD}.

13.1 ACMPH Block Diagram

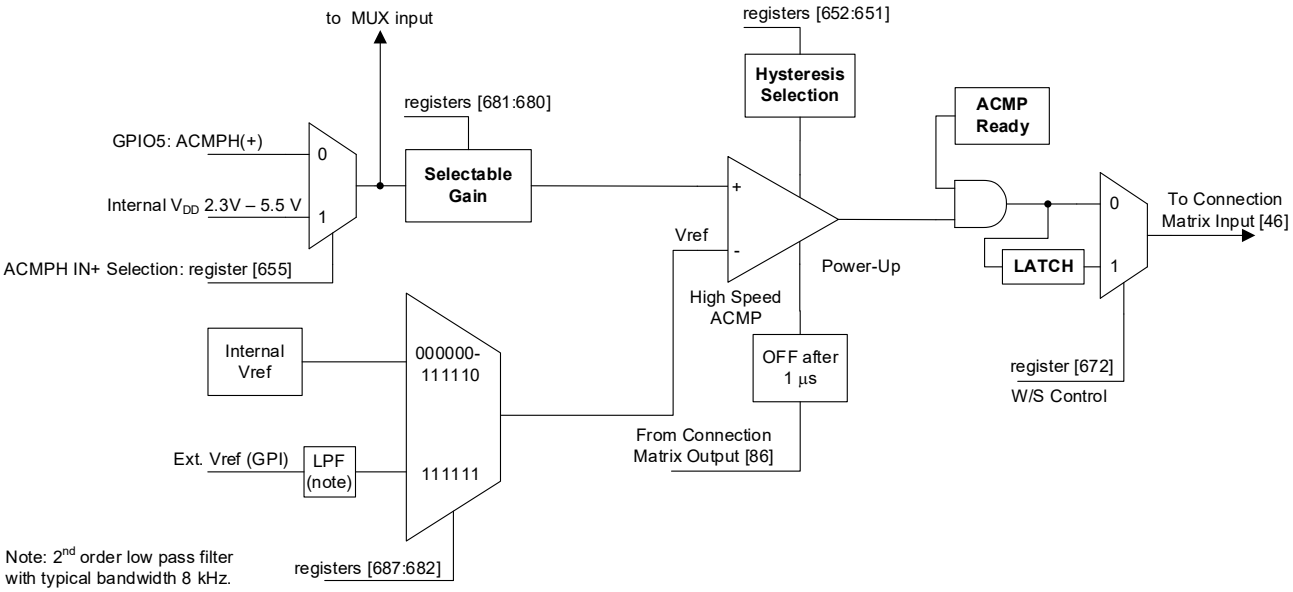


Figure 96. ACMPH Block Diagram

13.2 ACMP Typical Performance

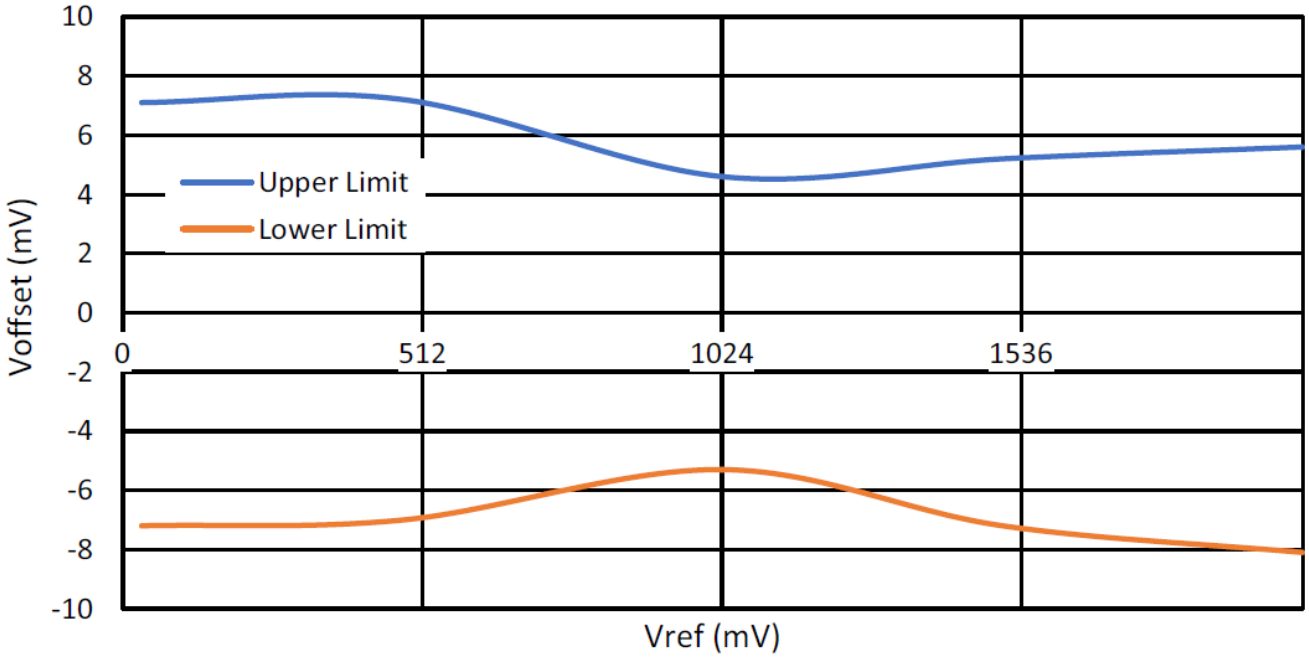


Figure 97. ACMPH Input Offset Voltage vs. V_{REF} at V_{DD} = 2.3 V to 5.5 V, T = -40 °C to +85 °C

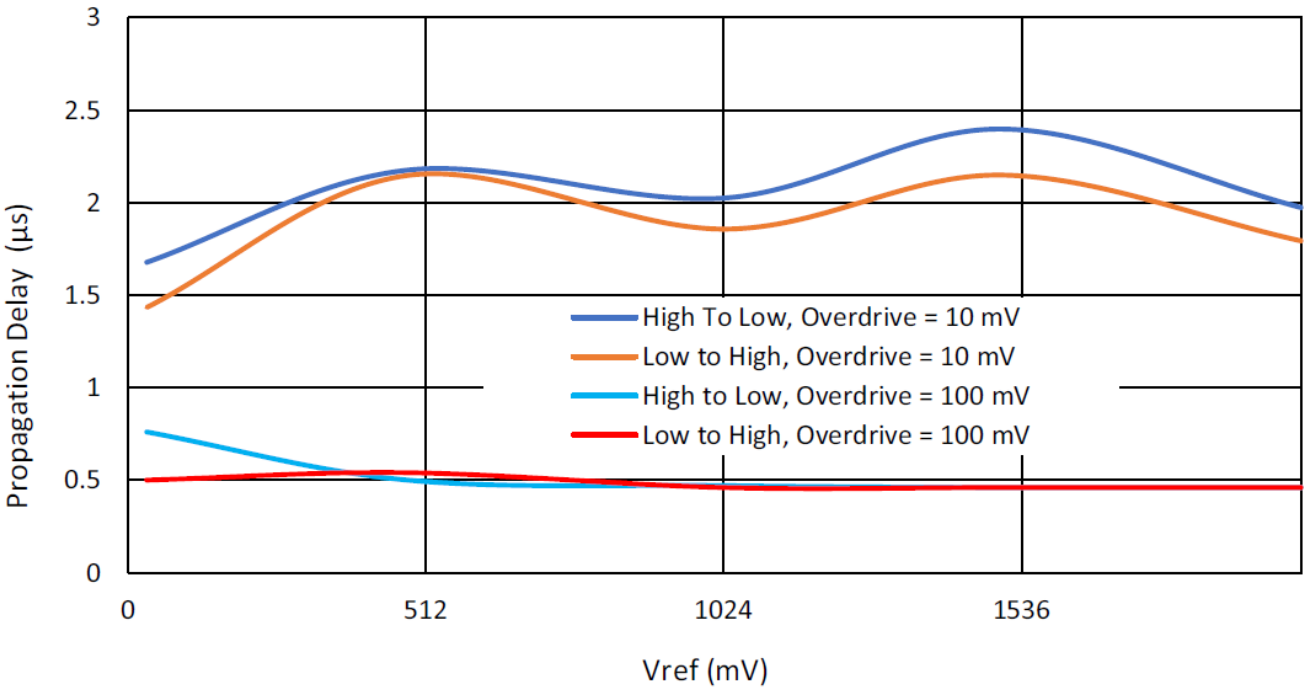


Figure 98. Propagation Delay vs. V_{REF} for ACMPH at T = +25 °C, at V_{DD} = 2.3 V to 5.5 V, Gain = 1, Hysteresis = 0

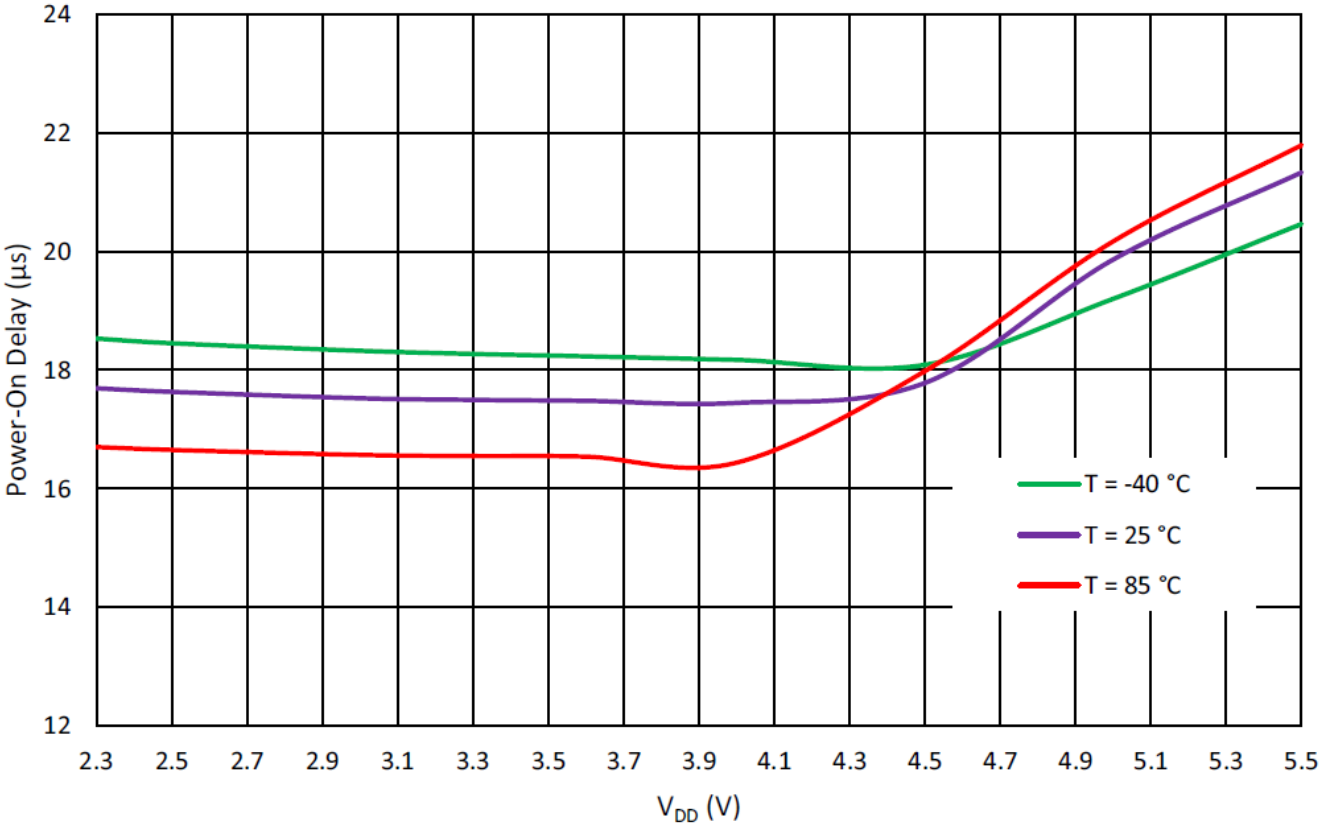


Figure 99. ACMPH Power-On Delay vs. V_{DD}

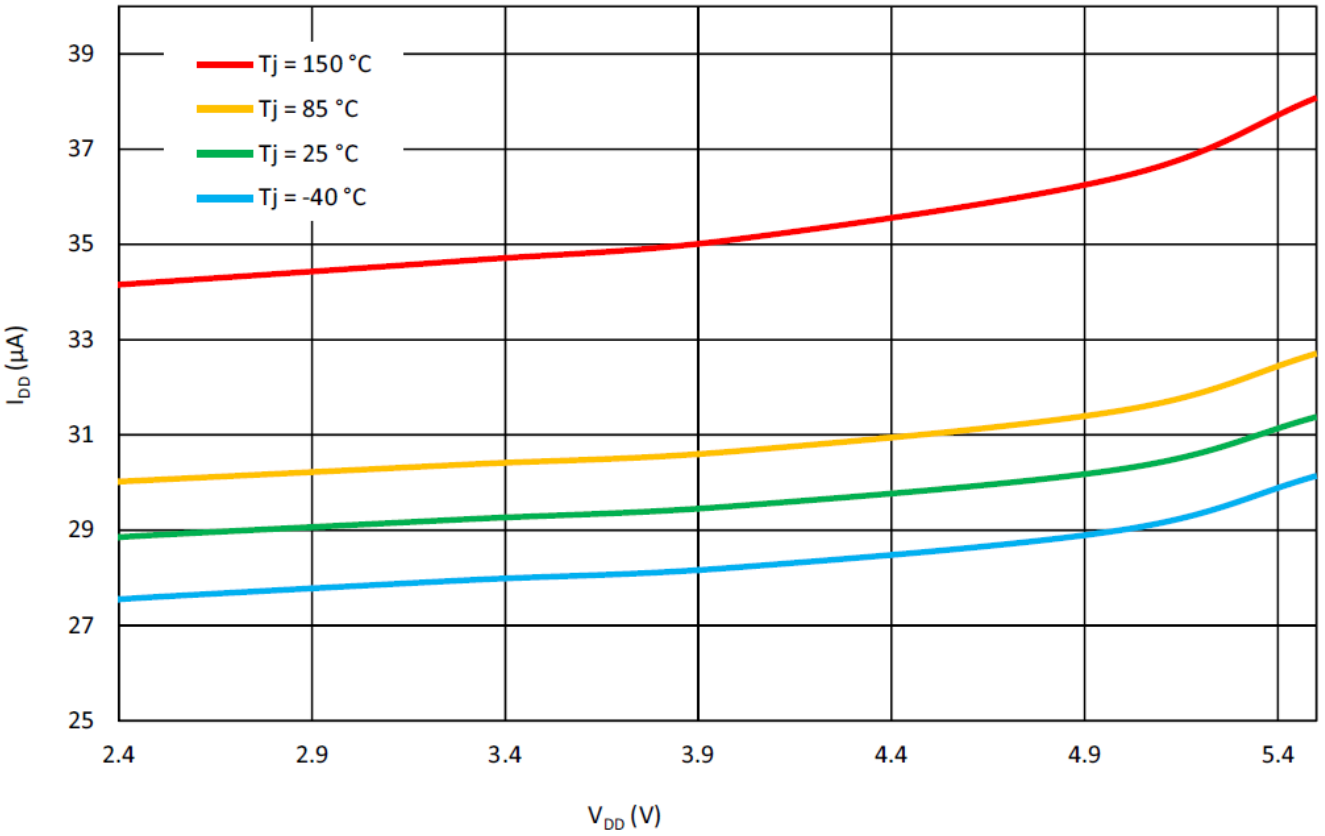


Figure 100. ACMPH Current Consumption vs. V_{DD} at V_{REF} = 32 mV

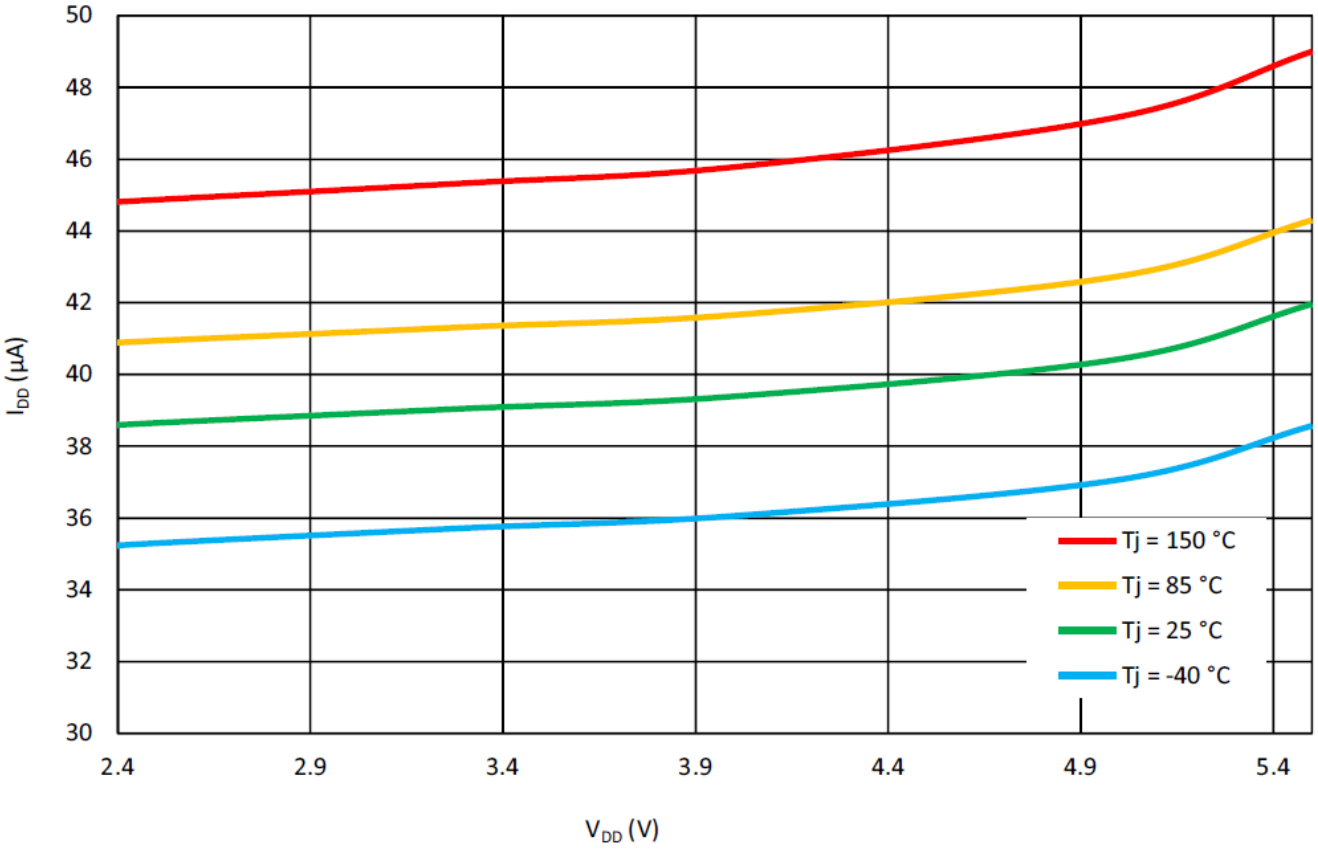


Figure 101. ACMPH Current Consumption vs. V_{DD} at V_{REF} = 1024 mV

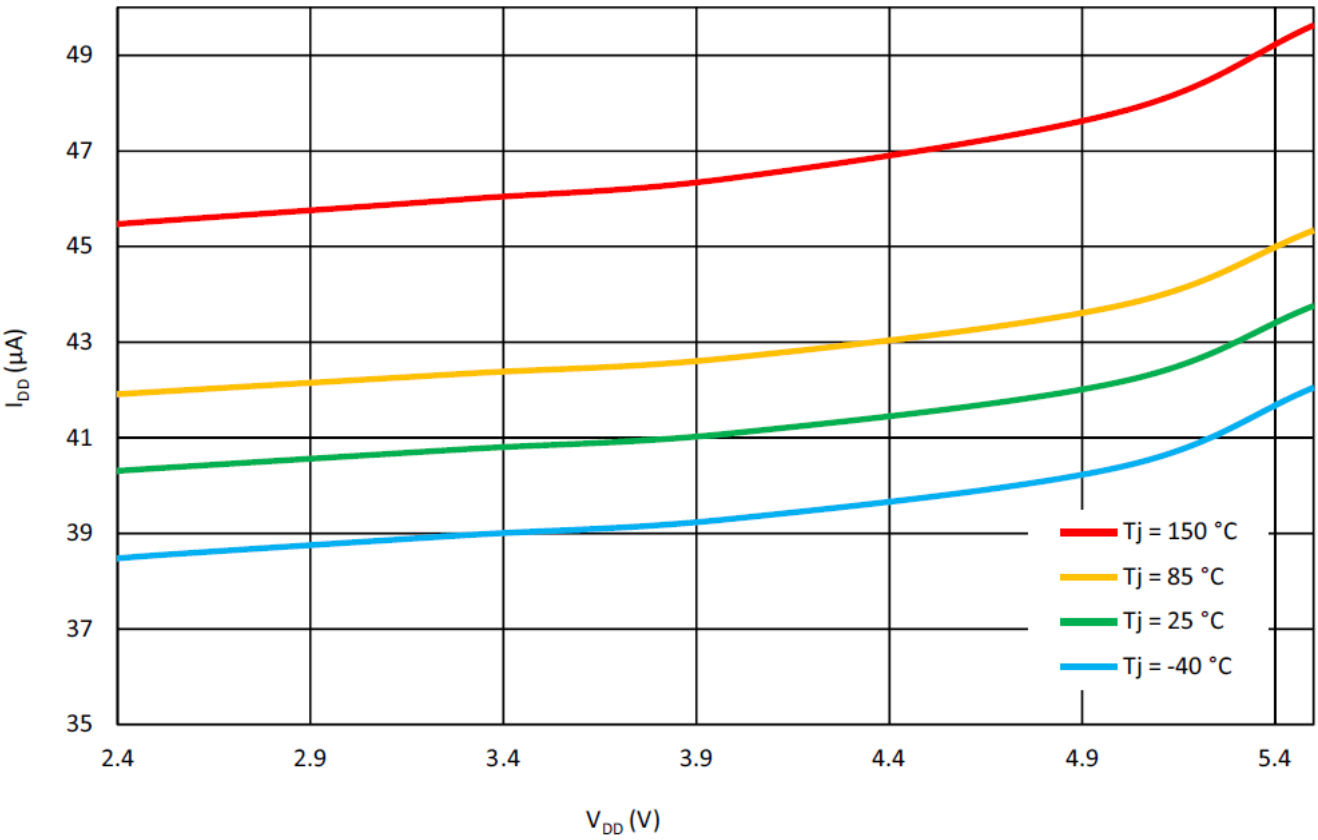


Figure 102. ACMPH Current Consumption vs. V_{DD} at V_{REF} = 2016 mV

14. Additional Logic Function. Deglitch Filter

The SLG47104 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay.

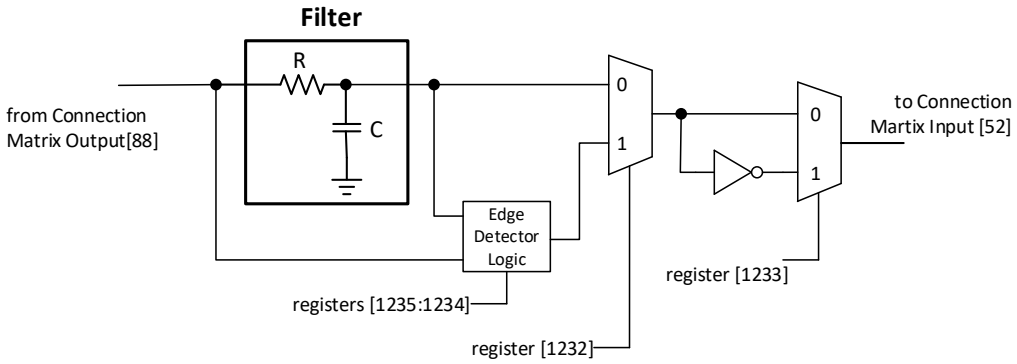


Figure 103. Deglitch Filter/Edge Detector

15. Voltage Reference

15.1 Voltage Reference Overview

The SLG47104 has a Voltage Reference (V_{REF}) macrocell to provide references to the analog comparator. This macrocell can supply a user selection of fixed voltage references. The macrocell also has the option to output reference voltages on GPIO0. See Table 36 for the available selections for the analog comparator.

Also, see Figure 104, which shows the reference output structure.

15.2 V_{REF} Selection Table

Table 36. V_{REF} Selection Table

SEL	SEL[5:0]	V_{REF}	SEL	SEL[5:0]	V_{REF}
0	000000	0.032	32	100000	1.056
1	000001	0.064	33	100001	1.088
2	000010	0.096	34	100010	1.12
3	000011	0.128	35	100011	1.152
4	000100	0.16	36	100100	1.184
5	000101	0.192	37	100101	1.216
6	000110	0.224	38	100110	1.248
7	000111	0.256	39	100111	1.28
8	001000	0.288	40	101000	1.312
9	001001	0.32	41	101001	1.344
10	001010	0.352	42	101010	1.376
11	001011	0.384	43	101011	1.408
12	001100	0.416	44	101100	1.44
13	001101	0.448	45	101101	1.472
14	001110	0.48	46	101110	1.504
15	001111	0.512	47	101111	1.536
16	010000	0.544	48	110000	1.568
17	010001	0.576	49	110001	1.6
18	010010	0.608	50	110010	1.632
19	010011	0.64	51	110011	1.664
20	010100	0.672	52	110100	1.696
21	010101	0.704	53	110101	1.728
22	010110	0.736	54	110110	1.76
23	010111	0.768	55	110111	1.792
24	011000	0.8	56	111000	1.824
25	011001	0.832	57	111001	1.856
26	011010	0.864	58	111010	1.888
27	011011	0.896	59	111011	1.92

SEL	SEL[5:0]	V_{REF}	SEL	SEL[5:0]	V_{REF}
28	011100	0.928	60	111100	1.952
29	011101	0.96	61	111101	1.984
30	011110	0.992	62	111110	2.016
31	011111	1.024	63	111111	External

15.3 Mode Selection

Conditions	M[2]	M[1]	M[0]	Mode
GPIO0 is not configured as Analog IO (registers [756:755] ≠ 11) OR GPIO0 OE is HIGH	0	0	0	Analog Power-down
	0	0	1	Analog Power-down
	0	1	0	Reserved
	0	1	1	Reserved
	1	0	0	Analog Power-down
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Analog Power-down
GPIO0 is configured as Analog IO (registers [756:755] = 11) AND GPIO0 OE is LOW	0	0	0	Analog Power-down
	0	0	1	Vref_OUT to GPIO0 only
	0	1	0	Reserved
	0	1	1	Reserved
	1	0	0	Reserved
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Vref_OUT to GPIO0 bypass analog buffer

Note: Voltage Reference can be outputted to GPIO0 according to M[2:0] state when this GPIO is configured as Analog IO (registers [756:755] = 11) AND GPIO0 OE is LOW.

15.4 V_{REF} Block Diagram

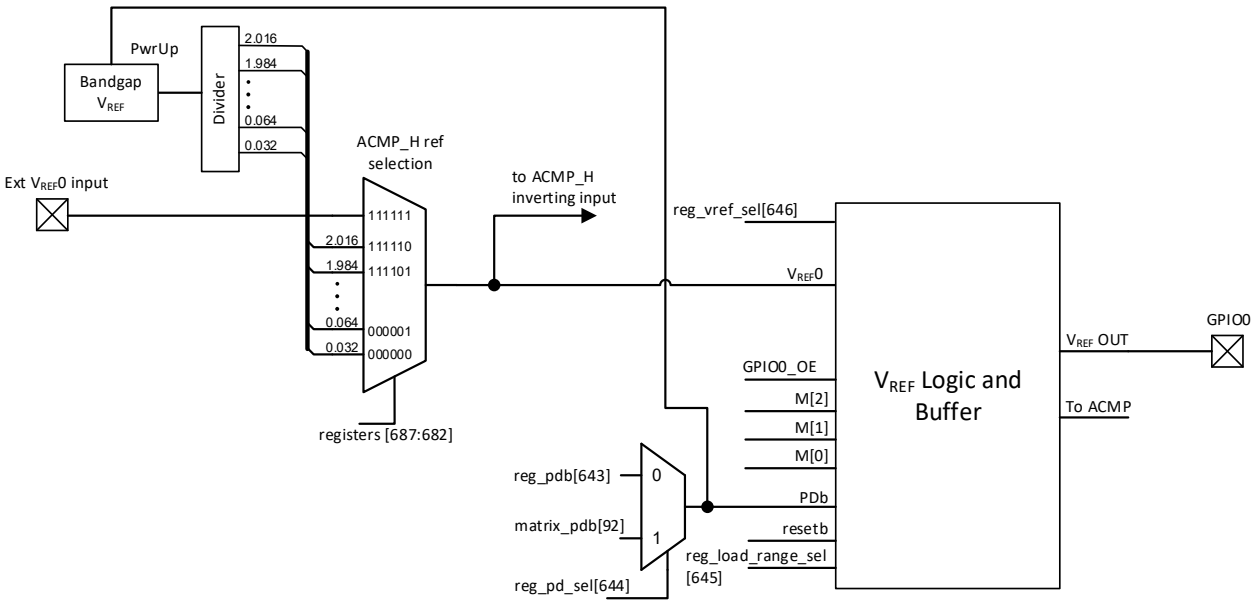


Figure 104. Voltage Reference Block Diagram

Note 1: reg_load_range_sel register should be set to 1 for better stability when the load resistance at GPIO0 is more than 100 kΩ. This option affects consumption current.

15.5 V_{REF} Load Regulation

Note: It is not recommended to use V_{REF} connected to external pin without buffer.

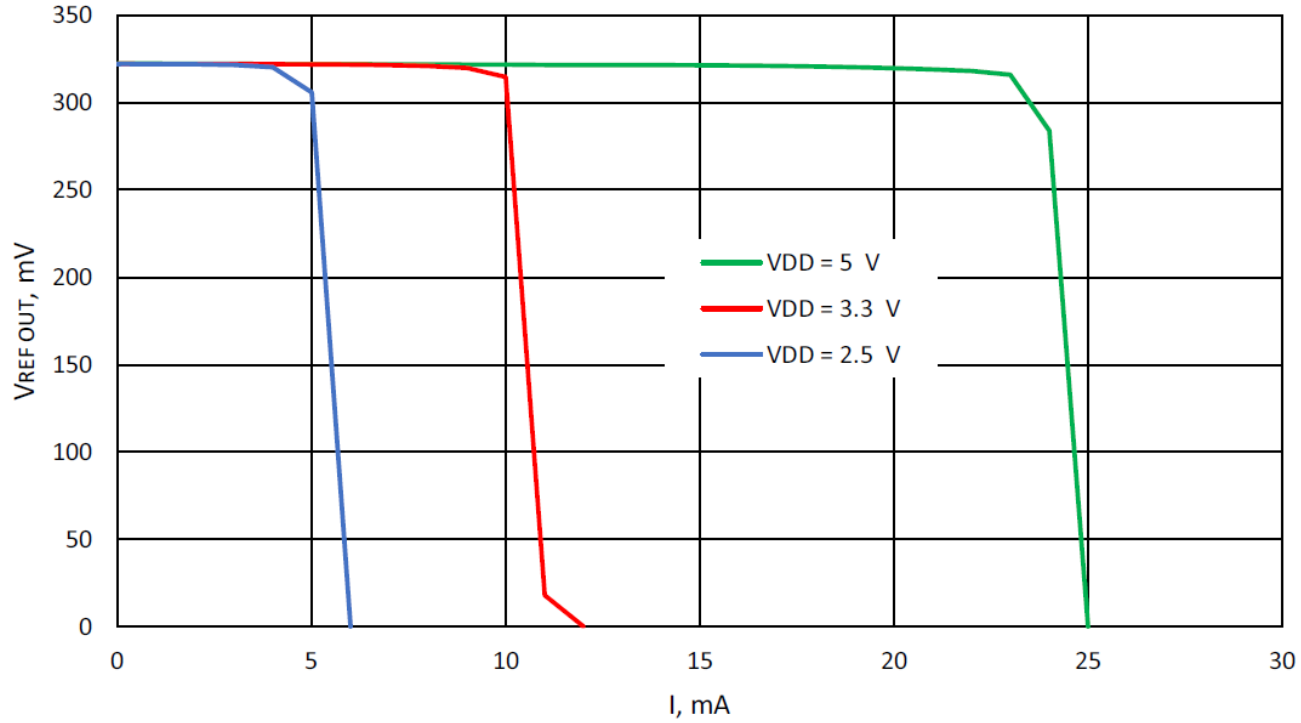


Figure 105. Typical Load Regulation, V_{REF} = 320 mV, T = -40 °C to +85 °C, Buffer – Enabled

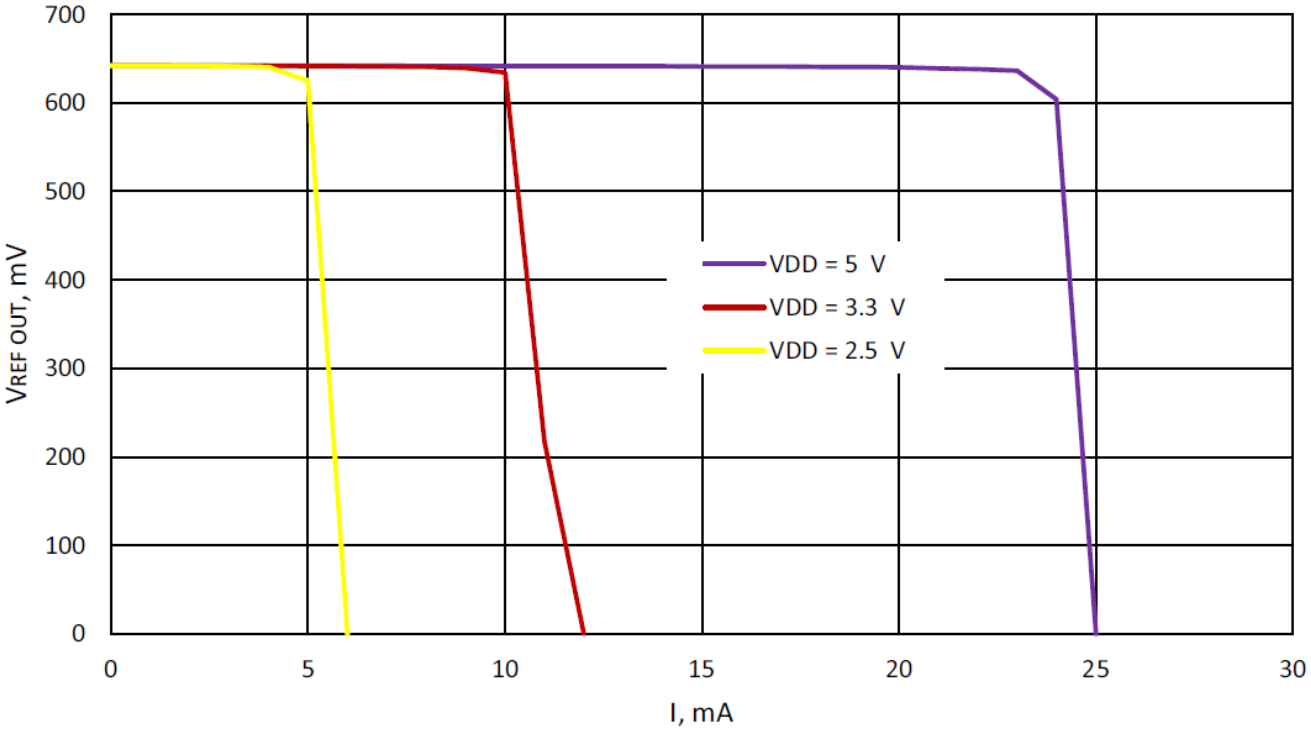


Figure 106. Typical Load Regulation, V_{REF} = 640 mV, T = -40 °C to +85 °C, Buffer – Enabled

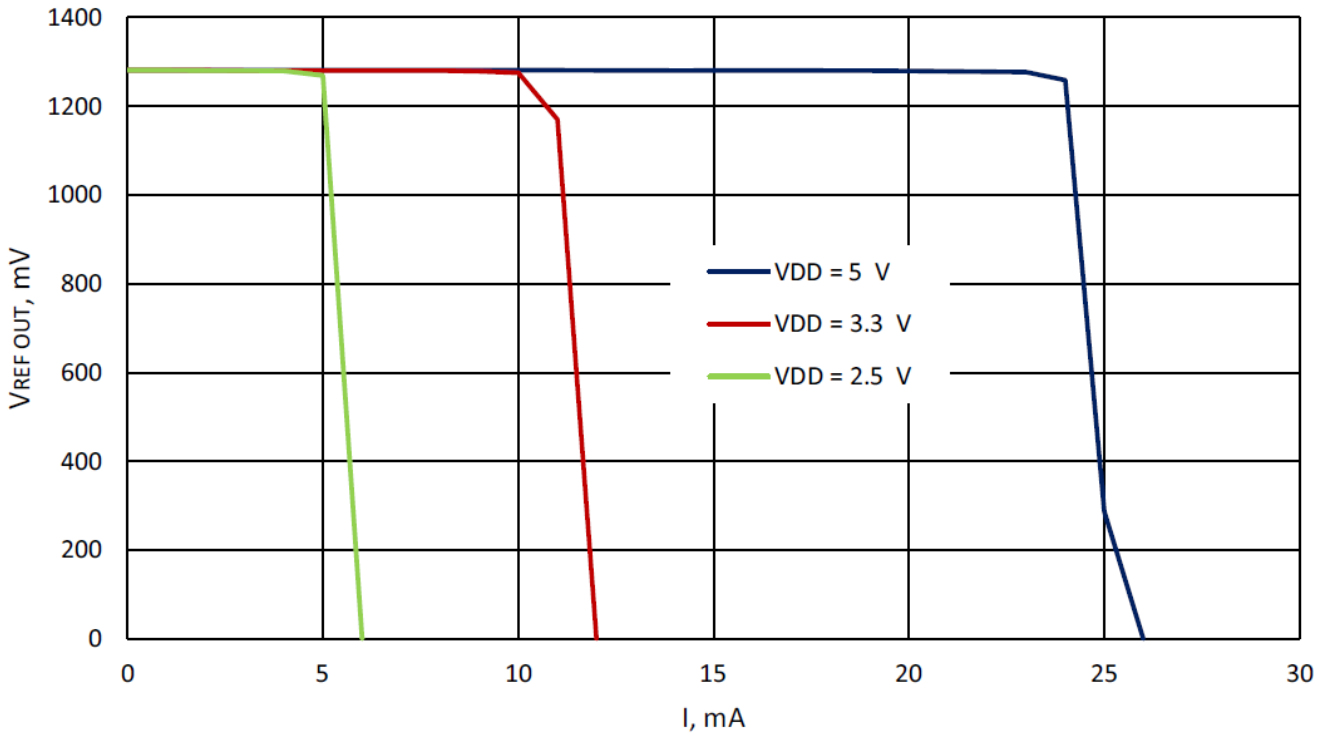


Figure 107. Typical Load Regulation, V_{REF} = 1280 mV, T = -40 °C to +85 °C, Buffer – Enabled

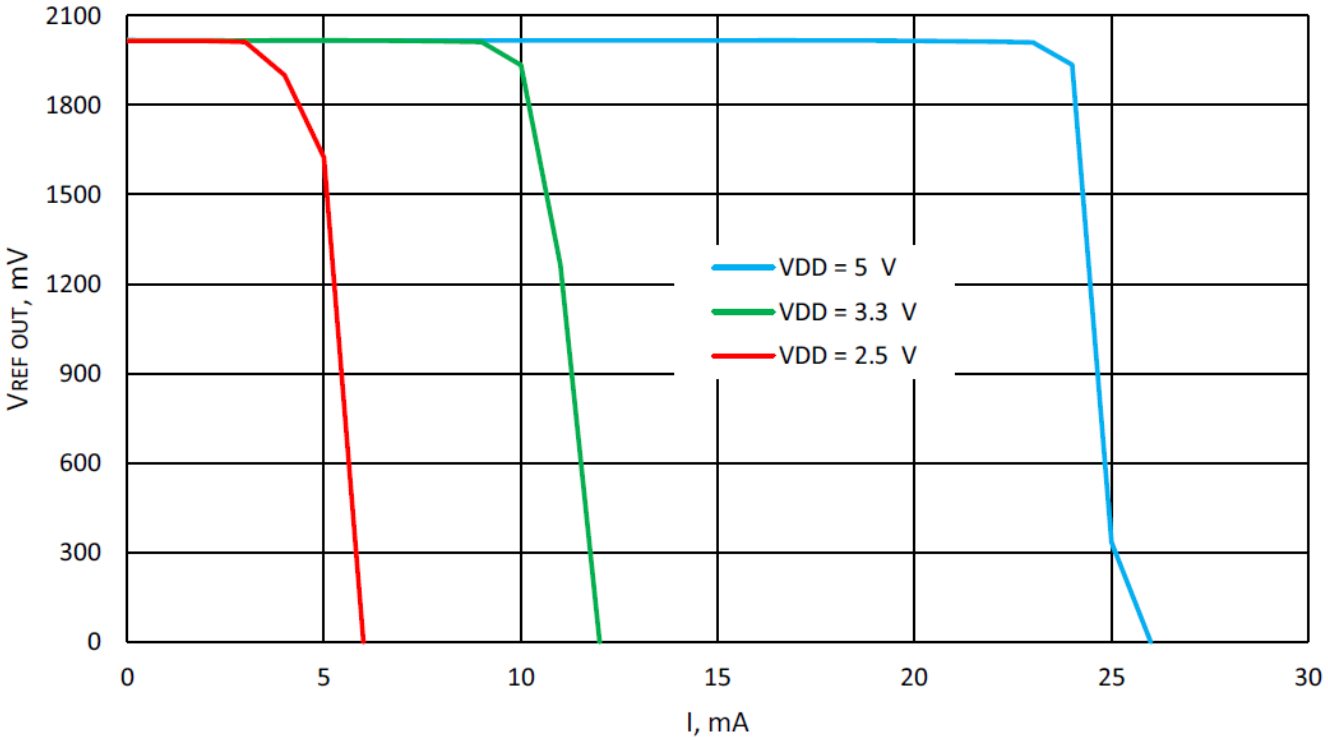


Figure 108. Typical Load Regulation, V_{REF} = 2016 mV, T = -40 °C to +85 °C, Buffer – Enabled

16. Clocking

16.1 OSC General Description

The SLG47104 has two internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (25 MHz).

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to the connection matrix, as well as various other macrocells. The Pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8, and /12 in Oscillator1(25 MHz) to divide down frequency from the fundamental. The second stage divider has an input of frequency from the Pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24, or /64 on Connection Matrix Input lines [53], [54], [55], and [56]. Please see Figure 109 for more details on the SLG47104 clock scheme.

Oscillator1 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [722]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power- down/Force-On (Connection Matrix Output [90], [91]) signal has the highest priority. The OSC operates according to the following table:

Table 37. Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

[1] The OSC will run only when any macrocell that uses OSC is powered on.

16.2 Oscillator0 (2.048 kHz)

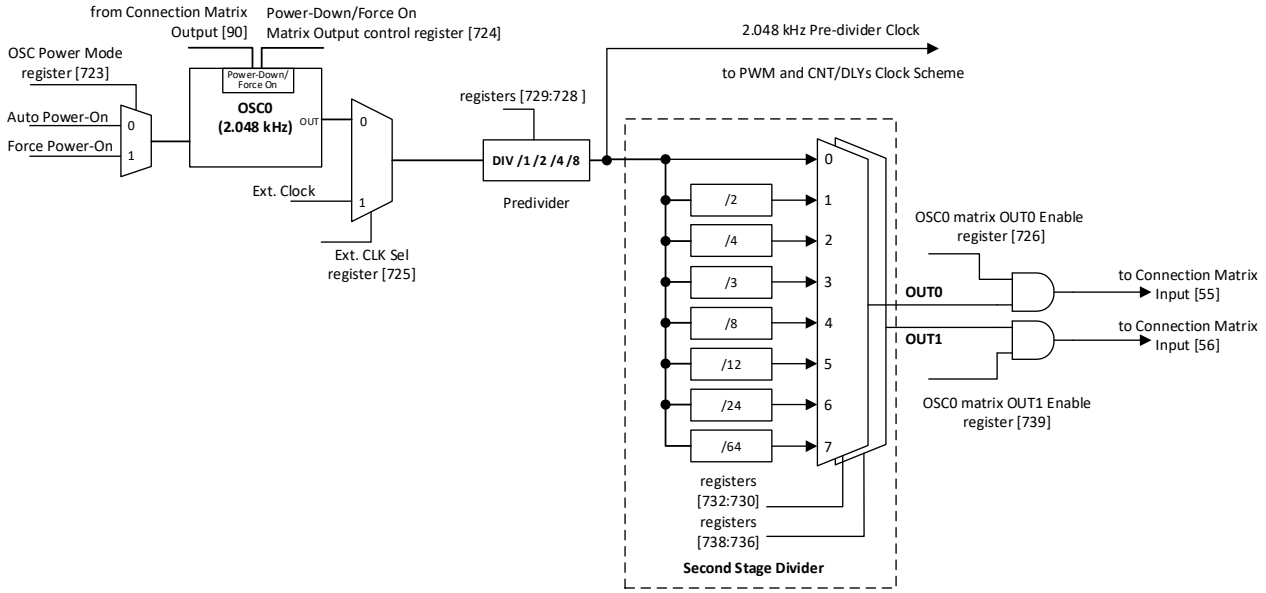


Figure 109. Oscillator0 Block Diagram

16.3 Oscillator1 (25 MHz)

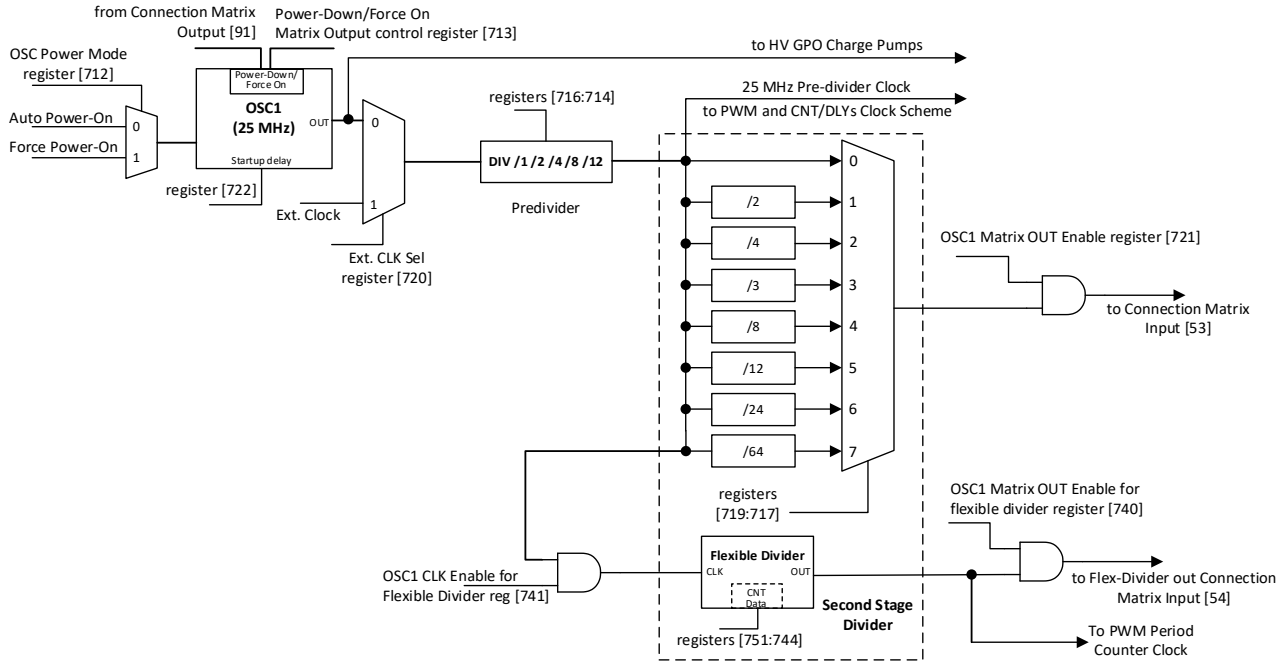


Figure 110. Oscillator1 Block Diagram

The OSC-integrated divider is built into 25 MHz OSC for saving chip resources. Actually, this divider is created especially for PWM, but it can be used for other chip resources thanks to its output to the matrix. There is 8-bit Counter with the source from OSC pre-divider and output to the matrix. In many cases for the PWM macrocell, the same frequency is a need. In these cases, it is possible to use this PWM divider for fine frequency tuning of PWM cell by I^2C or from NVM.

16.4 CNT/DLY Clock Scheme

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/4.

It is possible also to connect input from CNT(x-1) overflow or from Connection Matrix OUT.

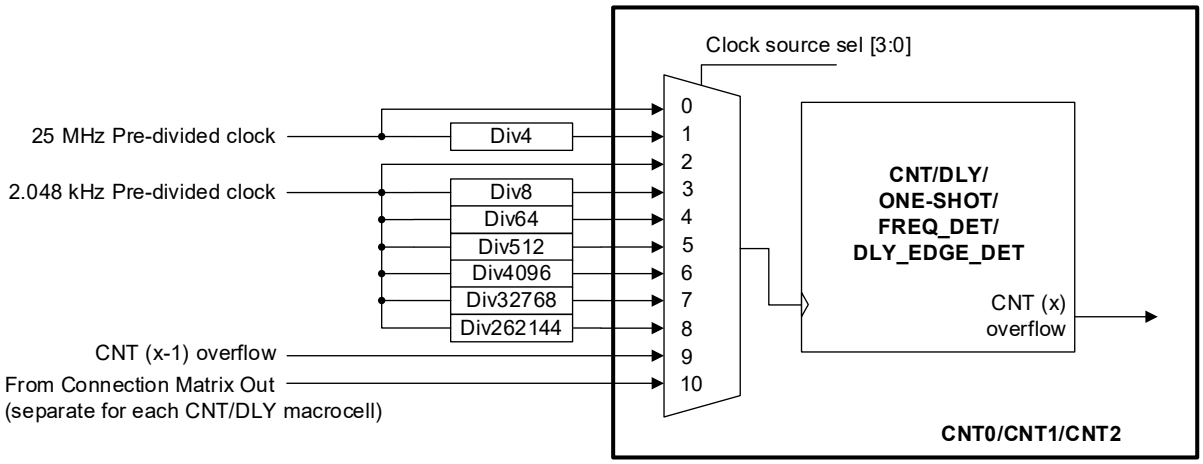


Figure 111. Clock Scheme

16.5 PWM Clock Scheme

The PWM macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC1/1, OSC1/8, OSC1/64, OSC1/512, OSC1/4096, OSC1/32768, OSC1/262144
- OSC0/1, OSC0/4.

It is possible also to connect input from Flexible Divider (OSC1 clock divider) or from Connection Matrix OUT.

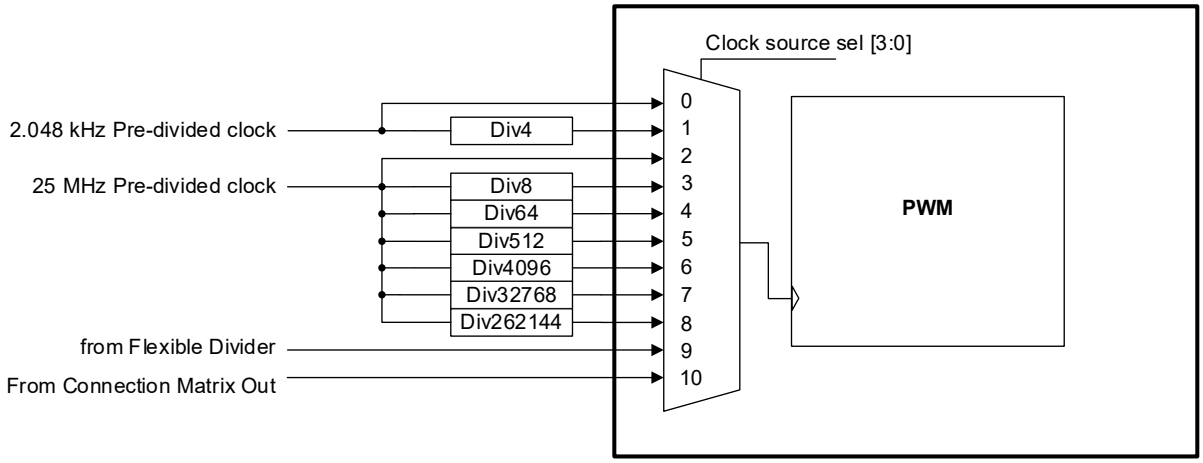


Figure 112. PWM Clock Scheme

16.6 External Clocking

The SLG47104 supports several ways to use an external, higher accuracy clock as a reference source for internal operations. Note that the Low Voltage Digital Input pin type can only support up to 1 MHz.

16.6.1 GPIO1 Source for Oscillator0 (2.048 kHz)

When register [725] is set to 1, an external clocking signal on GPIO1 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 109. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

16.6.2 GPIO4 Source for Oscillator 1 (25 MHz)

When register [720] is set to 1, an external clocking signal on GPIO4 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 110. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.3 V, 30 MHz at V_{DD} = 3.3 V, 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC1, the oscillator's output signal will be inverted with respect to the GPIO4 input signal.

16.7 Oscillators Power-On Delay

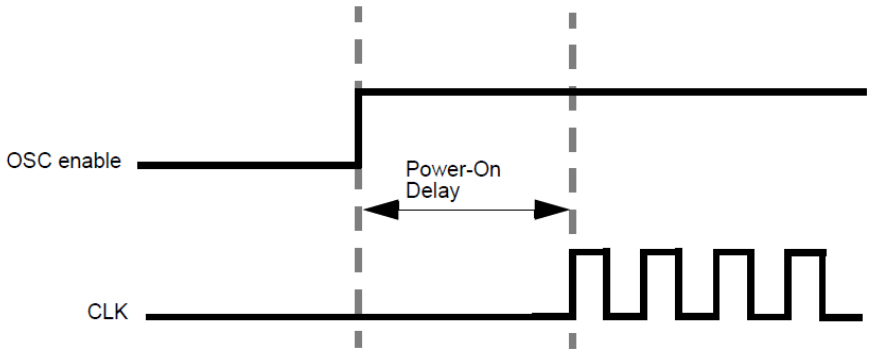


Figure 113. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.

Note 2: “OSC enable” signal appears when any macrocell that uses OSC is powered on.

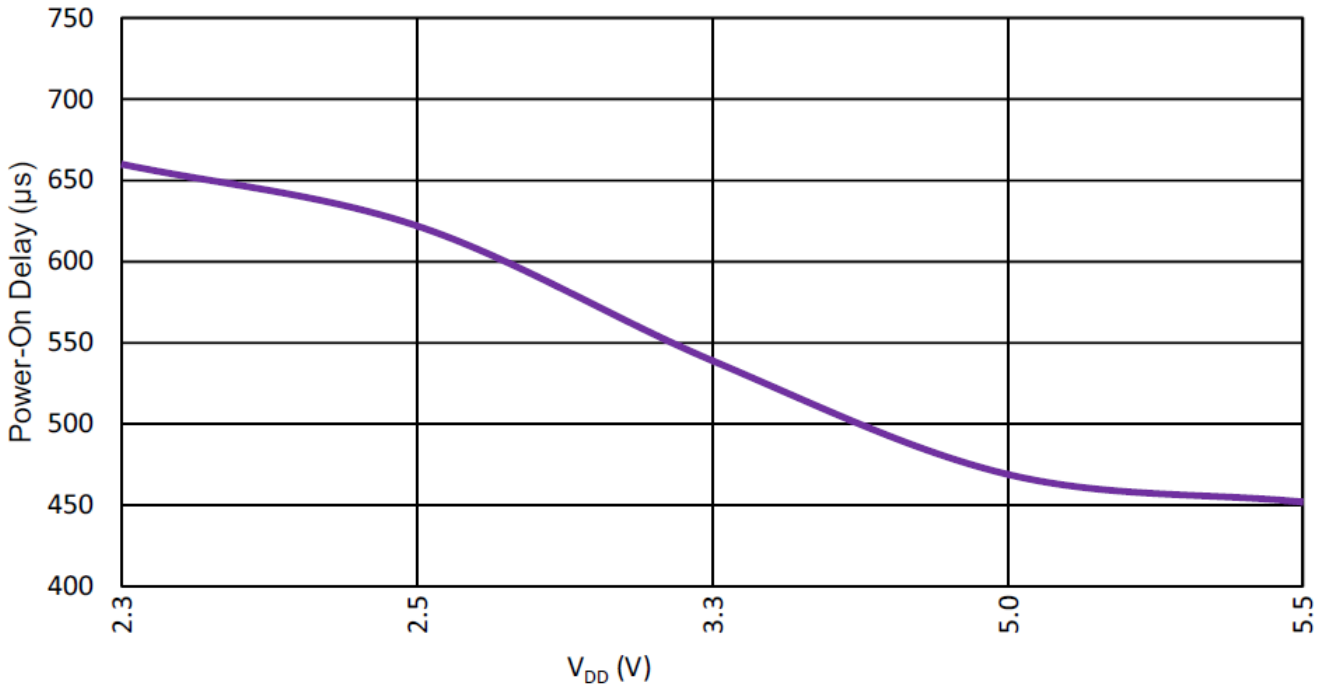


Figure 114. Oscillator0 Maximum Power-On Delay vs. V_{DD} at T = +25 °C, OSC0 = 2.048 kHz

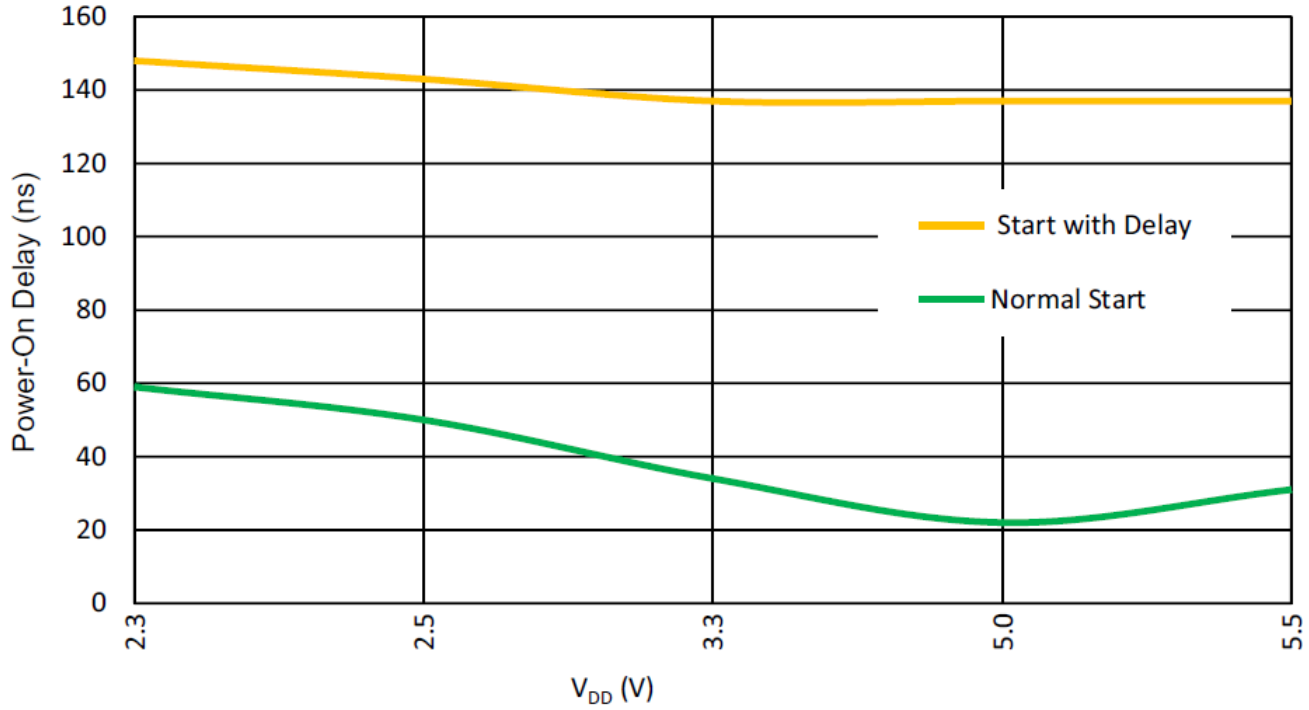


Figure 115. Oscillator1 Maximum Power-On Delay vs. V_{DD} at T = +25 °C, OSC1 = 25 MHz

16.8 Oscillators Accuracy

Note 1: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

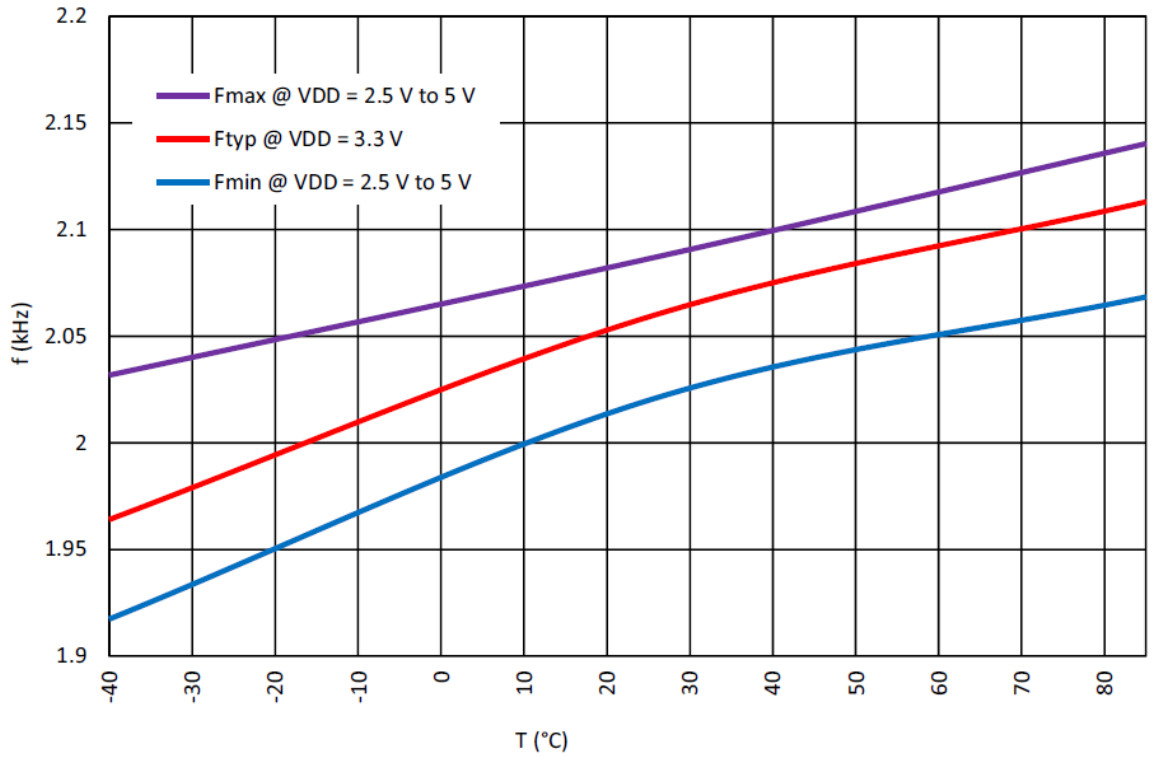


Figure 116. Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

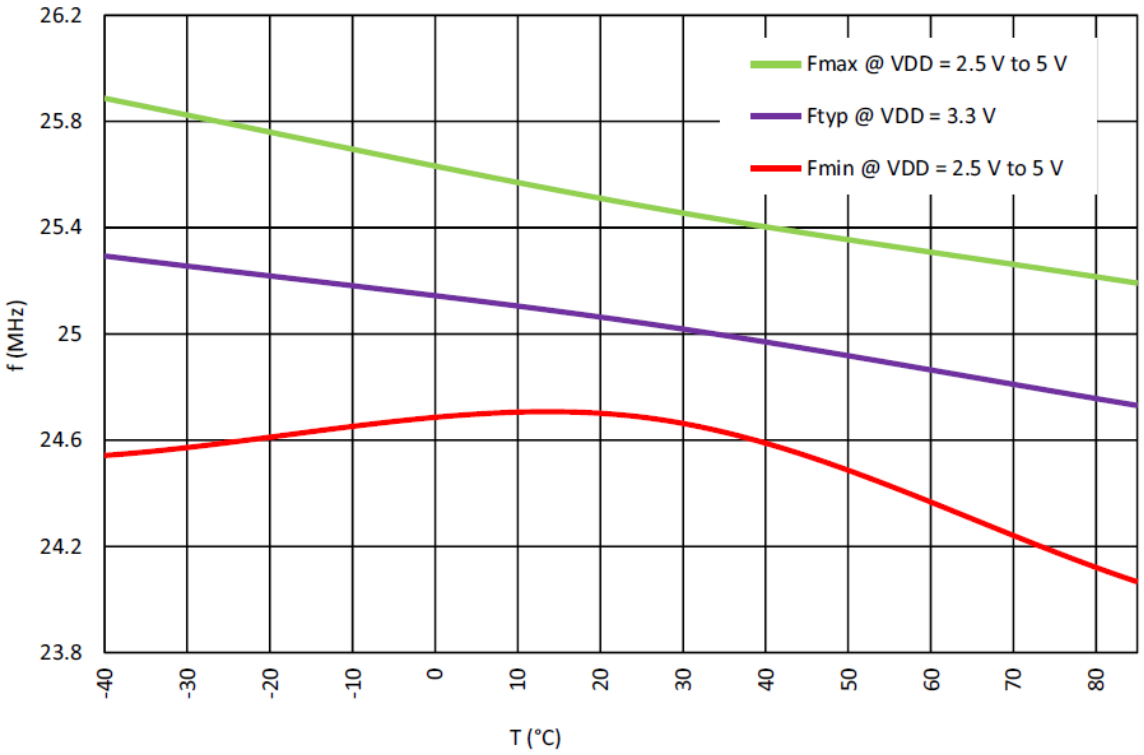


Figure 117. Oscillator1 Frequency vs. Temperature, OSC1 = 25 MHz

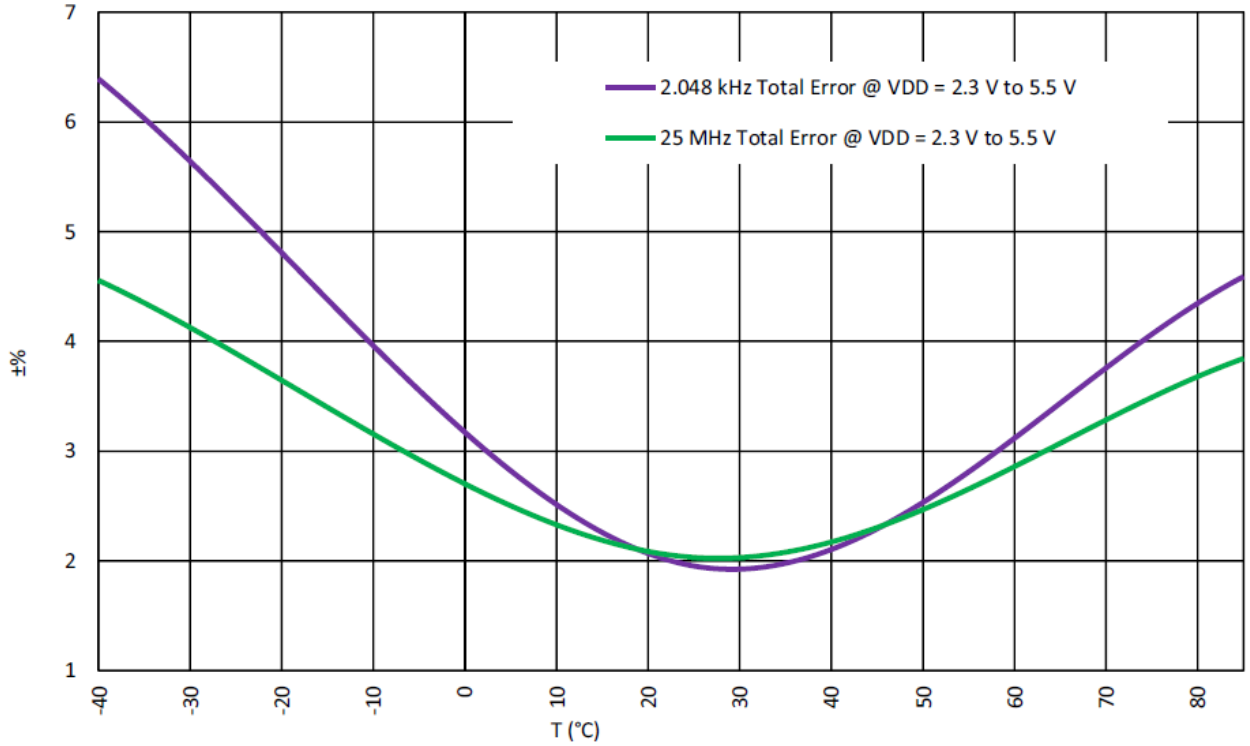


Figure 118. Oscillators Total Error vs. Temperature

Note 2: For more information see section 3.5.8 Oscillator Specifications.

16.9 Oscillators Settling Time

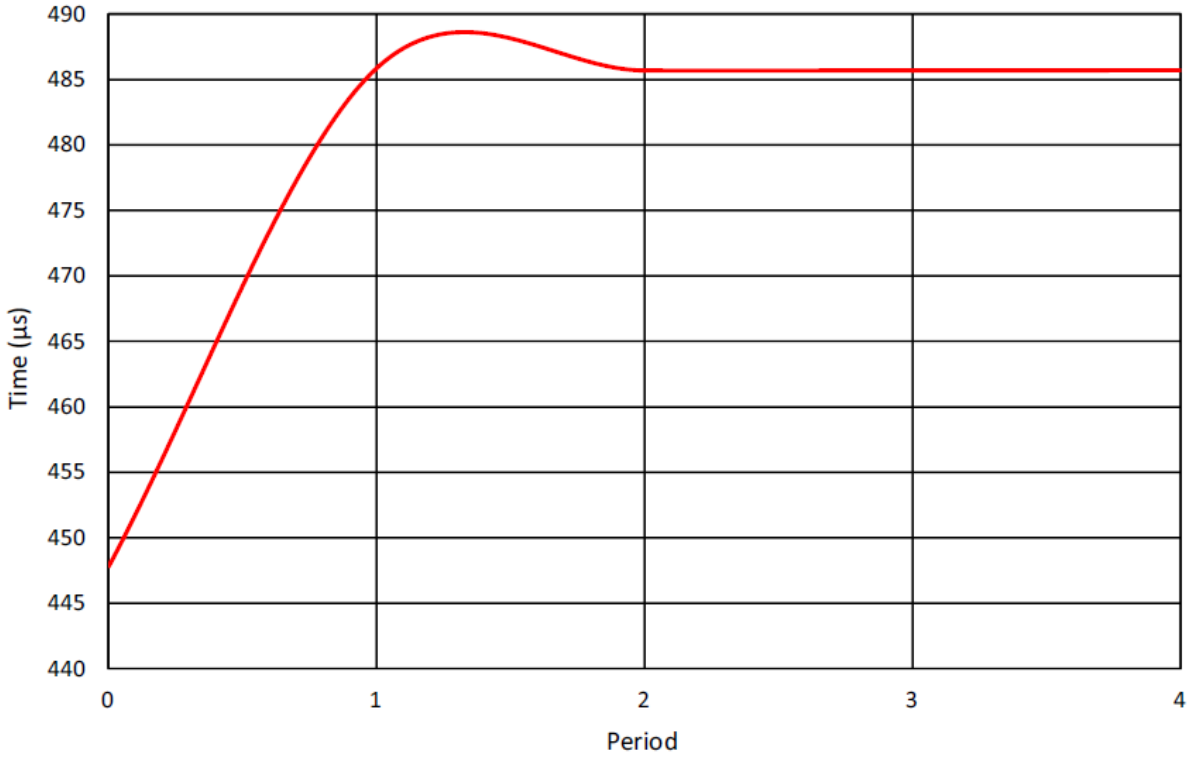


Figure 119. Oscillator0 Settling Time, V_{DD} = 3.3 V, T = +25 °C, OSC0 = 2 kHz

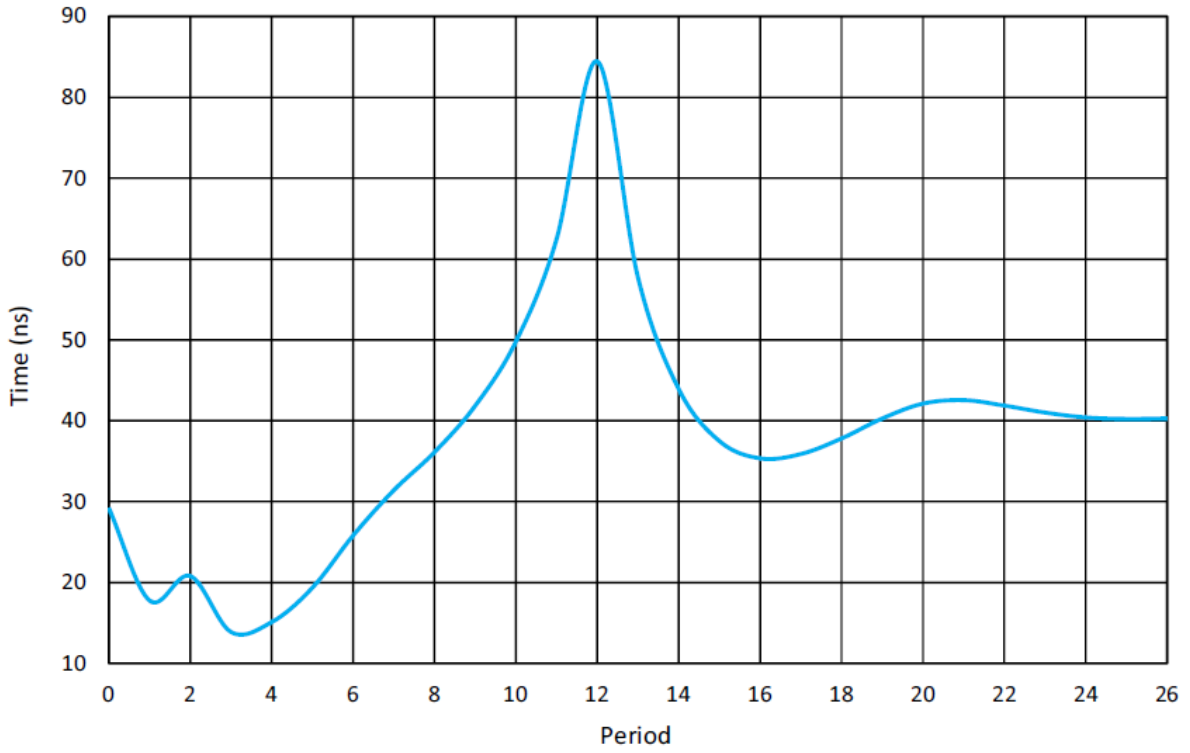


Figure 120. Oscillator1 Settling Time, V_{DD} = 3.3 V, T = +25 °C, OSC1 = 25 MHz (Normal Start)

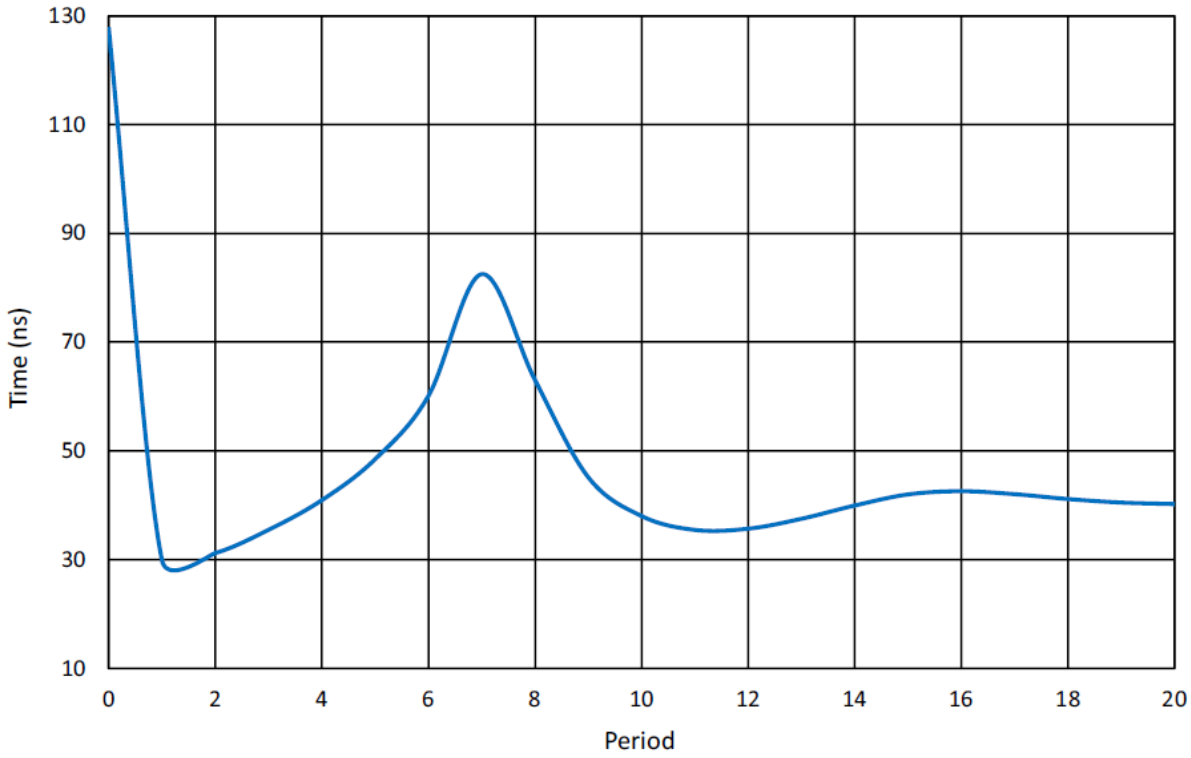


Figure 121. Oscillator1 Settling Time, V_{DD} = 3.3 V, T = +25 °C, OSC1 = 25 MHz (Start with Delay)

16.10 Oscillators Current Consumption

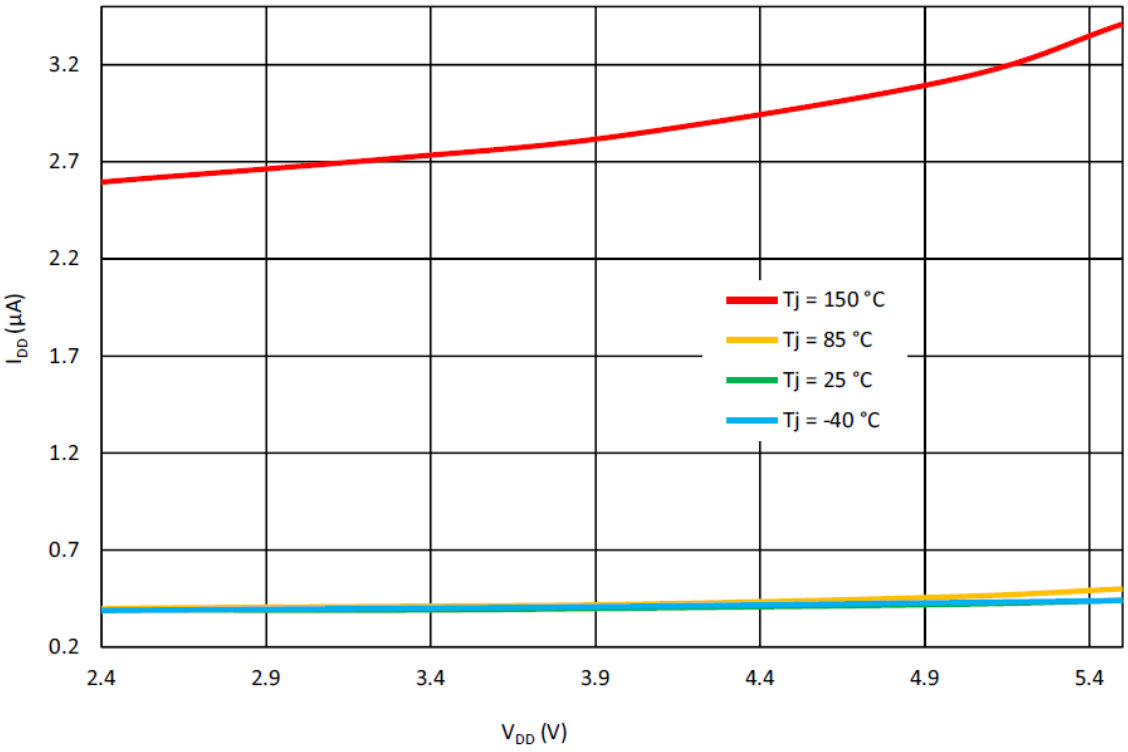


Figure 122. OSC0 Current Consumption vs. V_{DD} (All Pre-Dividers)

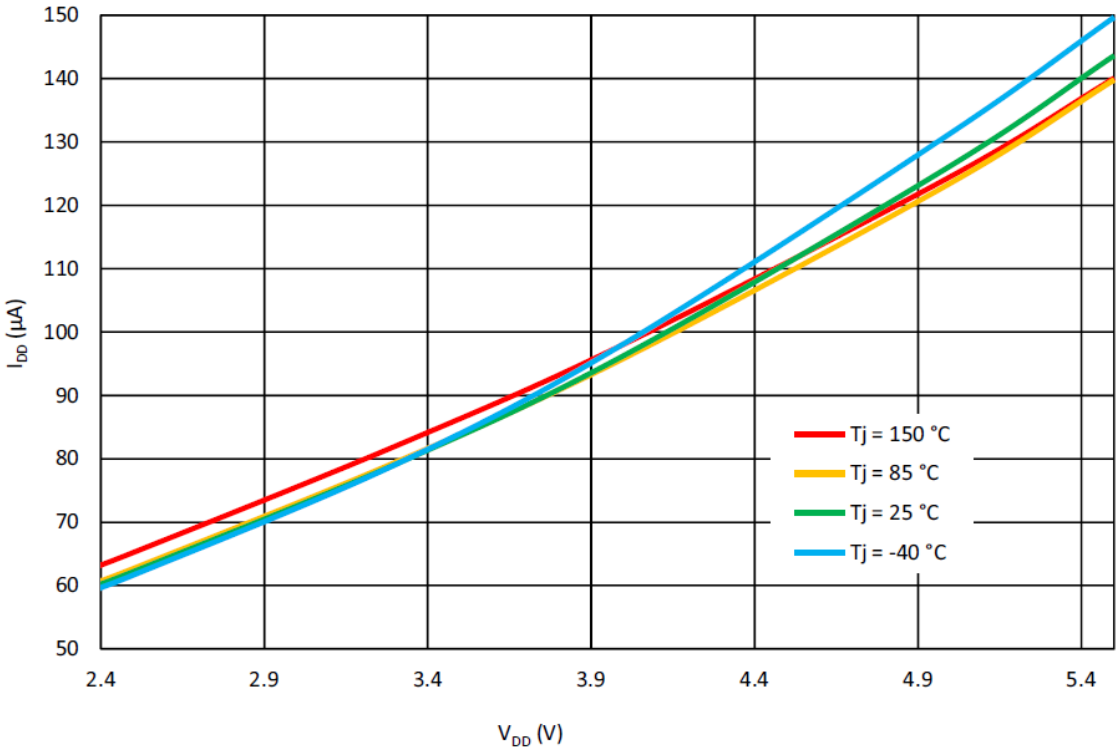


Figure 123. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 1)

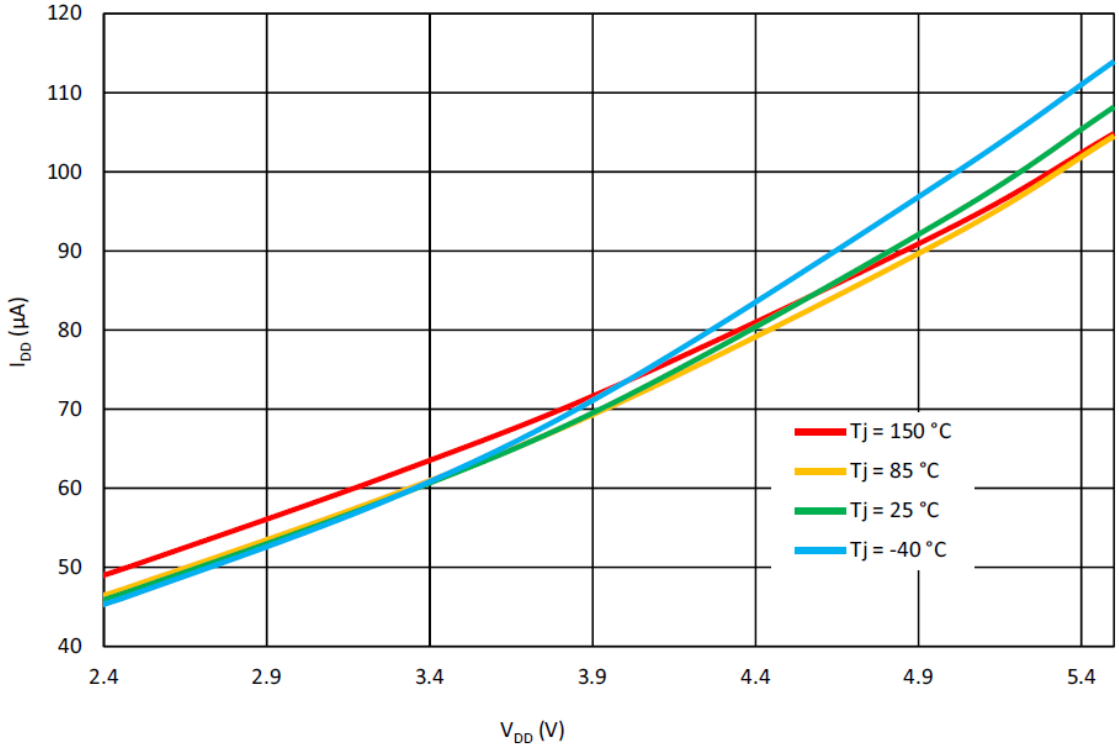


Figure 124. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 2)

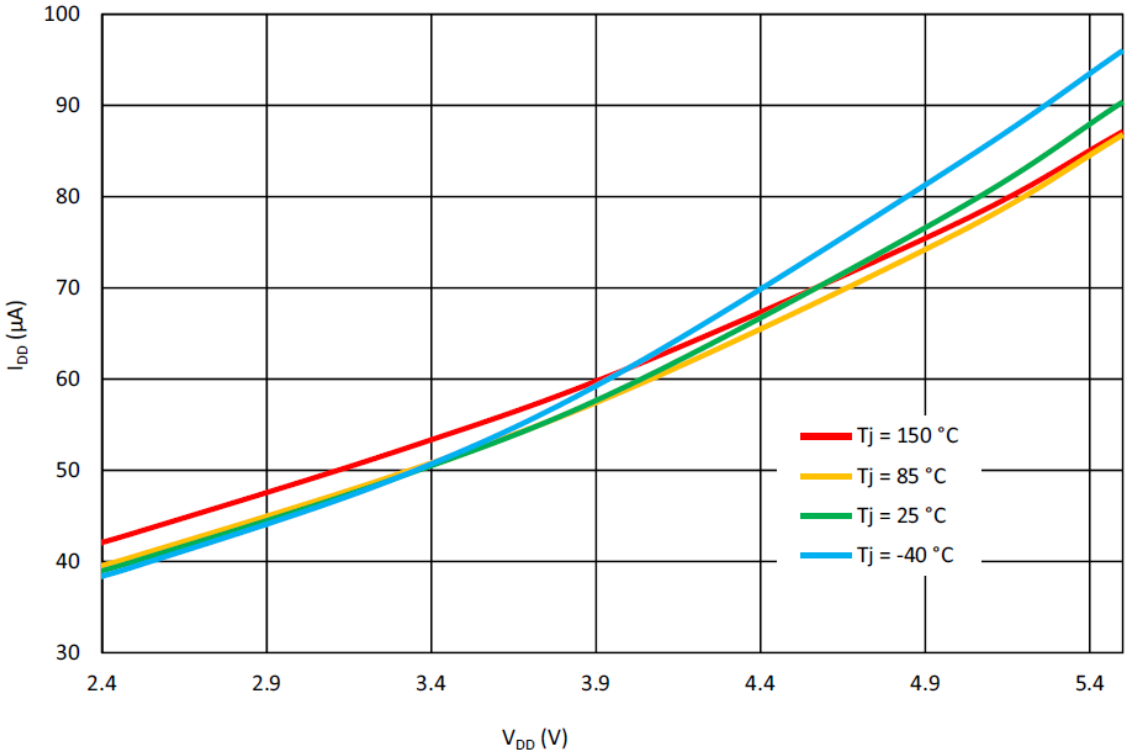


Figure 125. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 4)

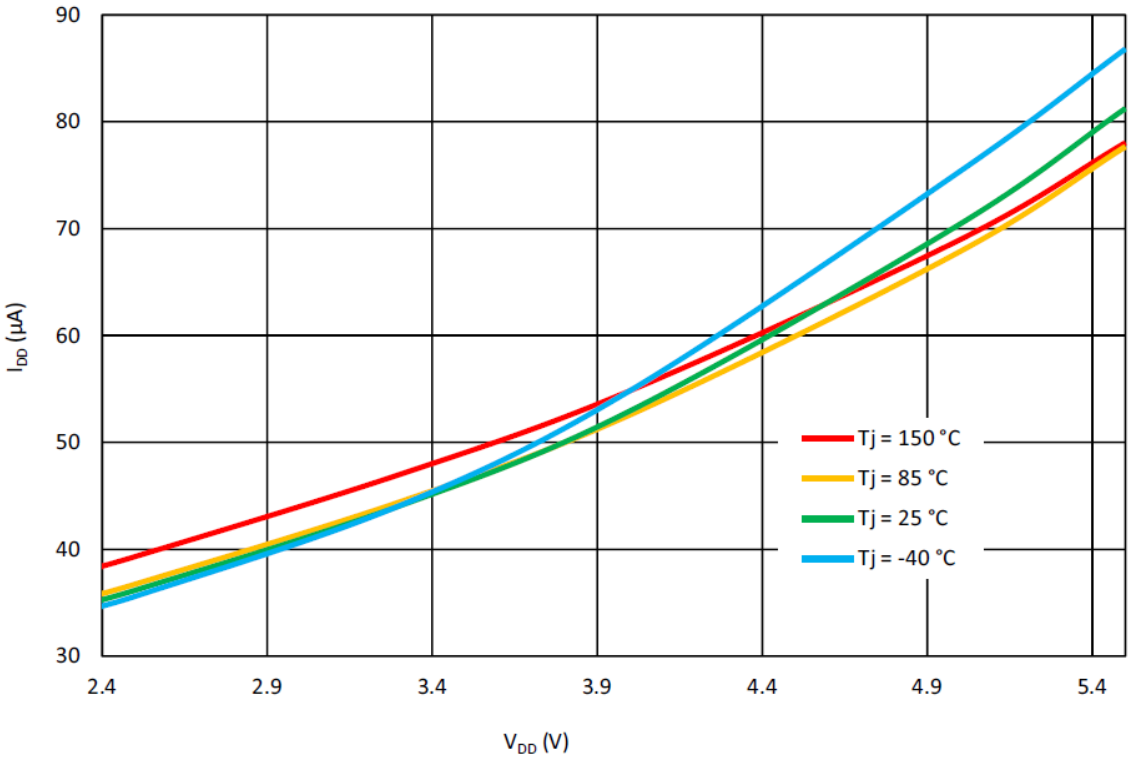


Figure 126. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 8)

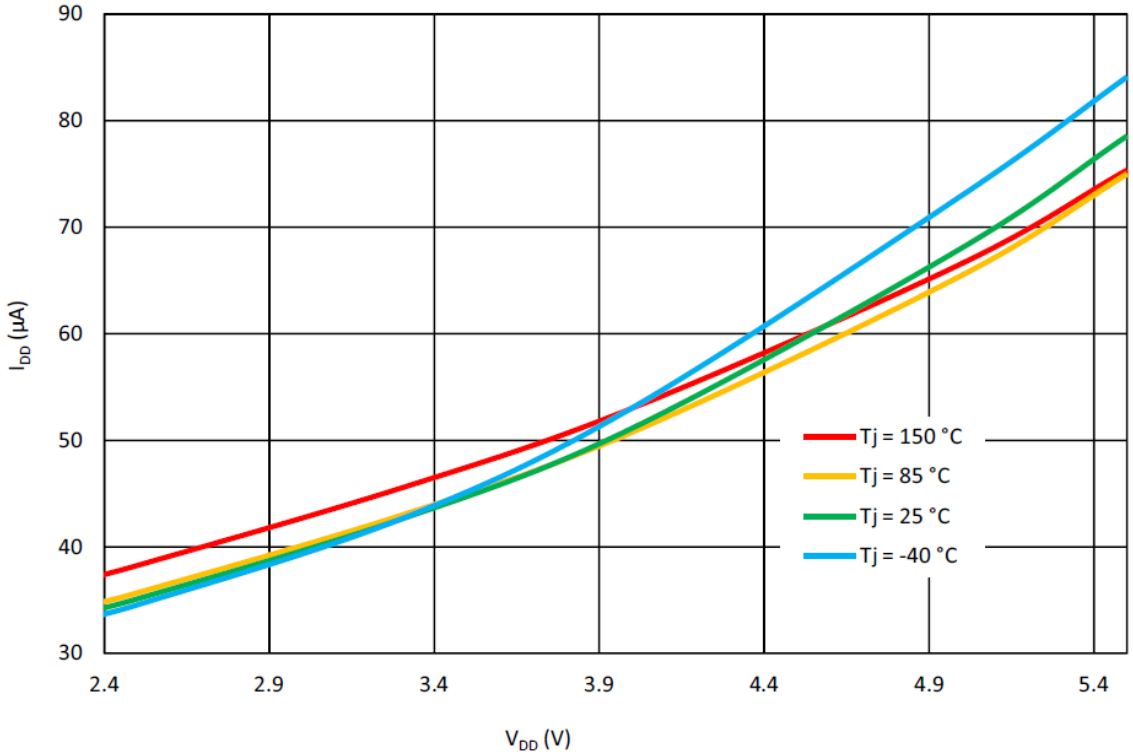


Figure 127. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 12)

17. Low Power Bandgap

Low Power Bandgap (LP_BG) is the analog part, that is used by analog macrocells in HV PAK, such as 25 MHz OSC1, ACMP, HV GPOs, UVLO, and others. The high efficiency low power Bangap consumes just 510 nA. However, it requires about 2 ms Start Up Time for stable functionality. For these reasons, it is recommended to keep LP_BG always on.

It is still possible to turn off the LP_BG through the connection matrix when no analog blocks are used. Please note that OSC0 (2.048 kHz) does not use LP_BG.

18. Power-On Reset

The SLG47104 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

18.1 General Operation

The SLG47104 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on Pin 1) is less than Power-Off Threshold (see section 3.5.1 Logic IO Specifications), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note 2) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other pin is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG47104, the voltage applied on the V_{DD} should be higher than the Power-On Threshold (Note 2). The full operational V_{DD} range for the SLG47104 is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence is started, the SLG47104 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device) and will be ready and completely operational after the POR sequence is complete.

Note 2: The Power-On Threshold is defined in section 3.5.1 Logic IO Specifications.

To power-down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All Pins are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on Pins can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

18.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 128.

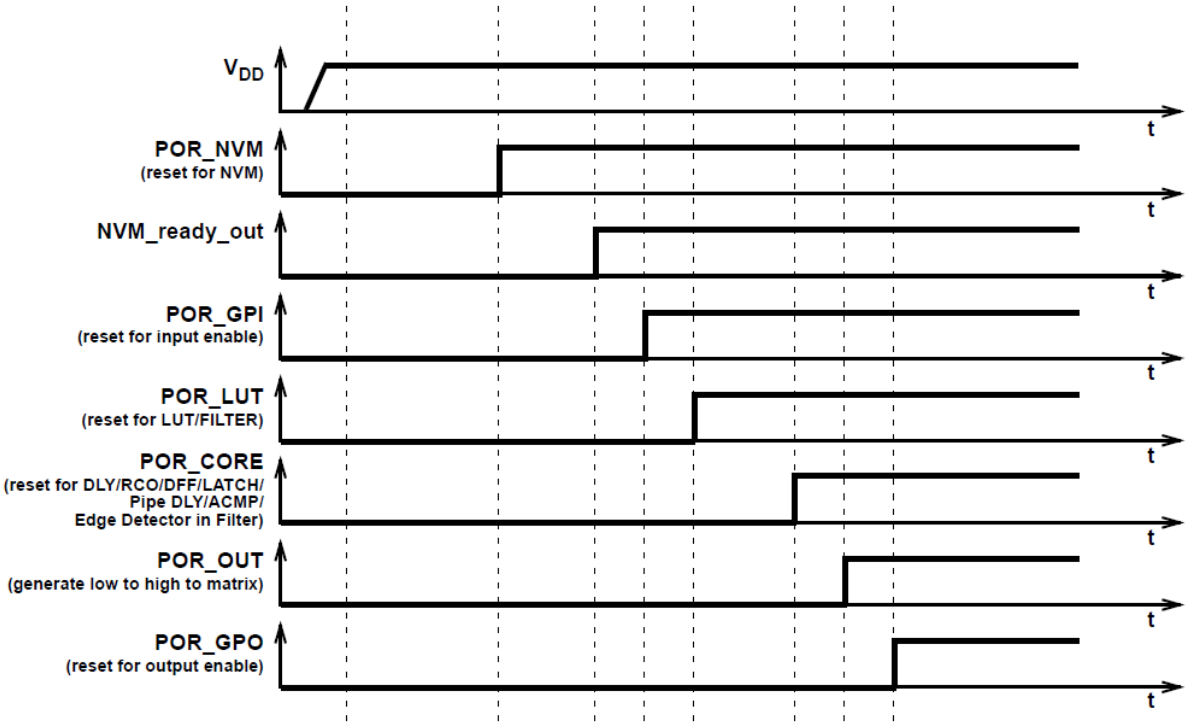


Figure 128. POR Sequence

As can be seen in Figure 128 after the V_{DD} has started ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM and transfers this information to a CMOS LATCH, that serves to configure each macrocell, and the Connection Matrix, which routes signals between macrocells. The third stage causes the reset of the input pins and then enables them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSCs, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

18.3 Macrocells Output States during POR Sequence

To have a full picture of SLG47104 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 129 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. After that input pins are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

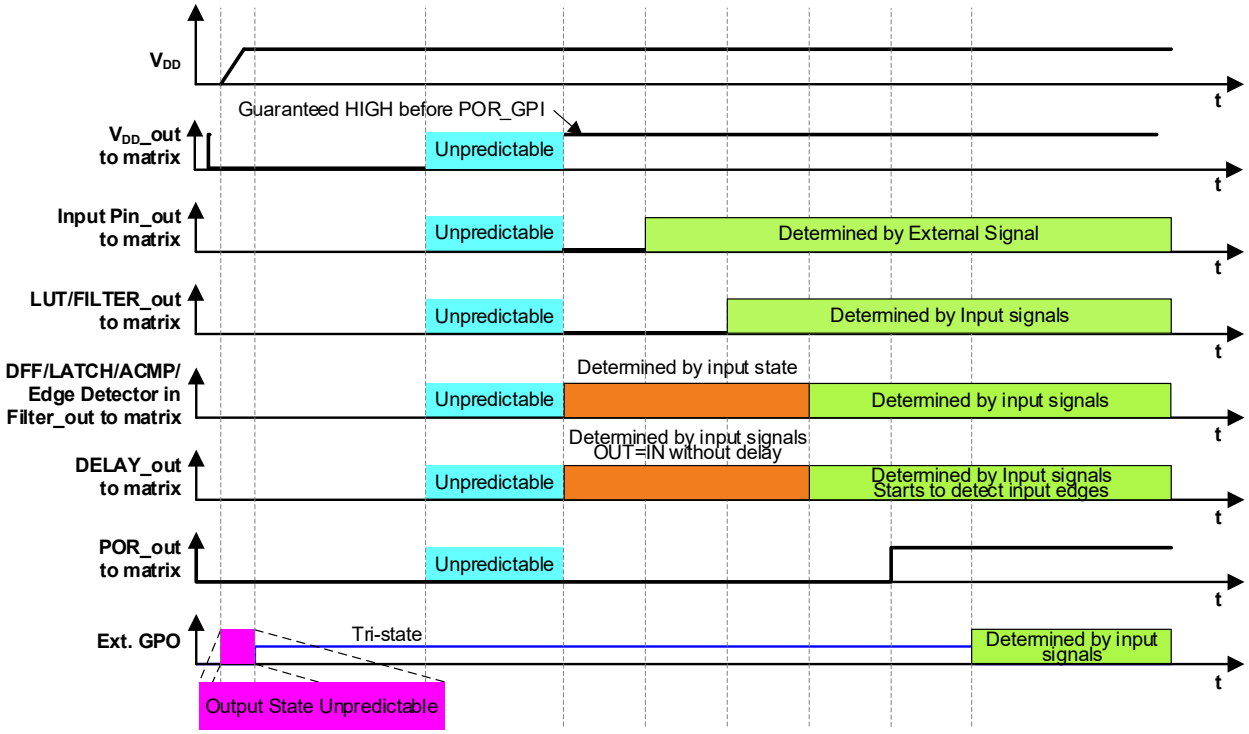


Figure 129. Internal Macrocell States During POR Sequence

18.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of PON_{THR} 1.80 V to 2.16 V, macrocells in SLG47104 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

- Input pins, ACMP, Pull-up/down.
- LUTs.
- DFFs, Delays/Counters, Pipe Delay.
- POR output to matrix.
- Output pin corresponds to the internal logic.

The V_{REF} output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin. There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

18.3.2 Power-Down

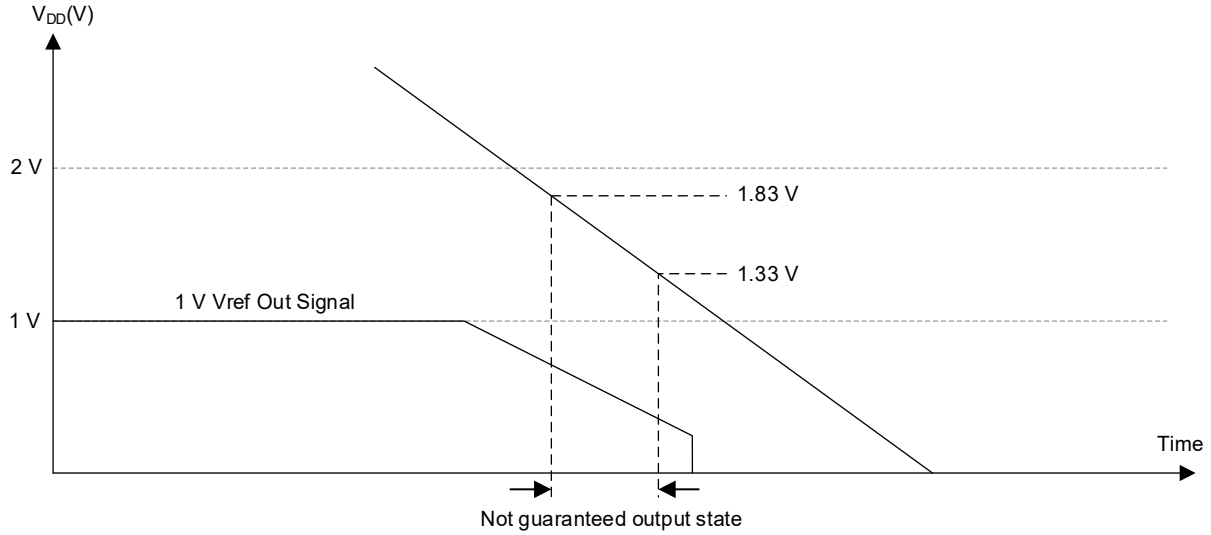


Figure 130. Power-Down

During Power-down, macrocells in SLG47104 are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow ramp down, outputs can possibly switch state during this time.

19. I²C Serial Communications Macrocell

19.1 I²C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Controller to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells and remote changes to signal chains within the device.

The I²C bus Controller is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving the I²C bus Controller the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1967:1965]. See section 19.5.1 Register Read/Write Protection for more details on I²C read/write memory protection.

Normally, when V_{DD} is not applied, the external I²C Pull-up resistors can be connected to the I²C pins of the SLG47104. It does not affect the chip functionality and doesn't increase its current consumption.

19.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 131. After the Start bit, the first four bits are a control code. The address source (the register bit for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other target device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG47104 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG47104.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 131 shows this basic command structure.

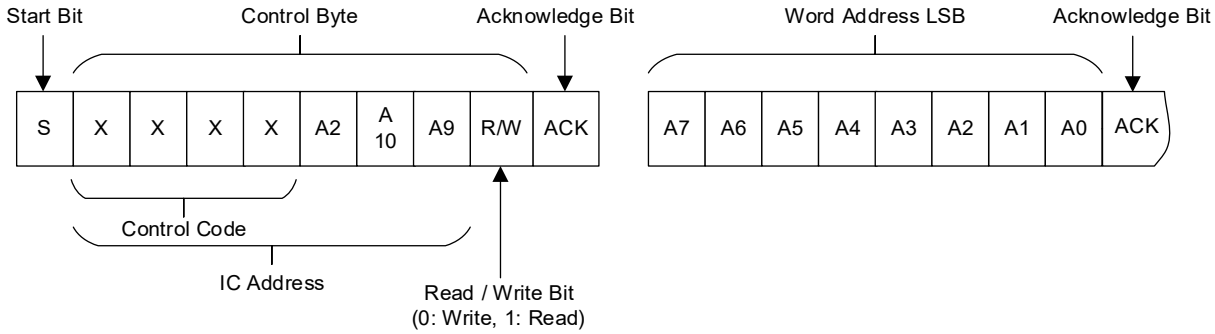


Figure 131. Basic Command Structure

19.3 I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 132. Timing specifications can be found in section 3.5 Electrical Specifications.

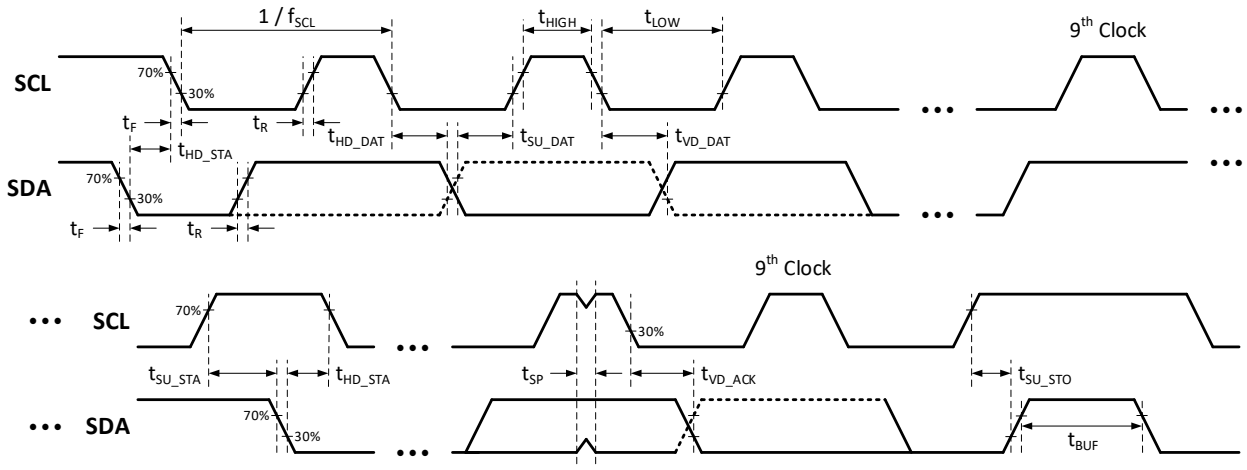


Figure 132. I²C General Timing Characteristics

19.4 I²C Serial Communications Commands

19.4.1 Byte Write Command

Following the Start condition from the Controller, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”) are placed onto the I²C bus by the Controller. After the SLG47104 sends an Acknowledge bit (ACK), the next byte transmitted by the Controller is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG47104, where the data byte is to be written. After the SLG47104 sends another Acknowledge bit, the Controller will transmit the data byte to be written into the addressed memory location. The SLG47104 again provides an Acknowledge bit and then the Controller generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG47104 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1961] = 1 - Enable. It means that IOs will remain their state until the write command is done.

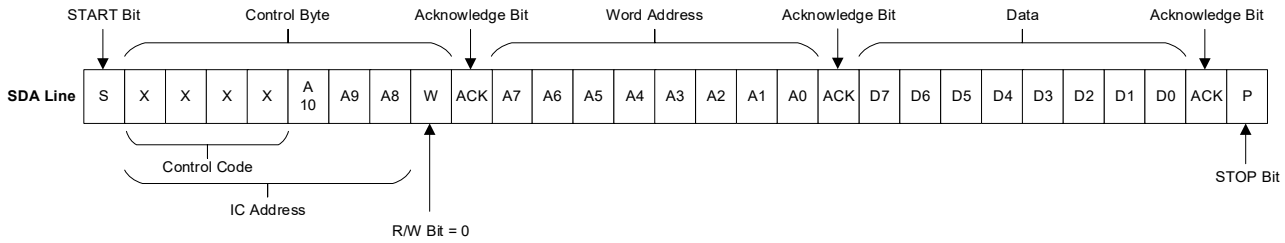


Figure 133. Byte Write Command, R/W = 0

19.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG47104 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Controller continues to transmit data bytes to the SLG47104. Each subsequent data byte will increment the internal address counter and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG47104 generates the Acknowledge bit.

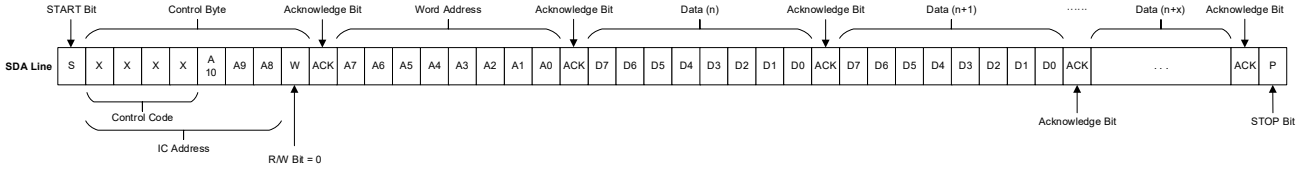


Figure 134. Sequential Write Command

19.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Controller, with the R/W bit = “1”. The SLG47104 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Controller will not issue an Acknowledge bit, and follow immediately with a Stop condition.

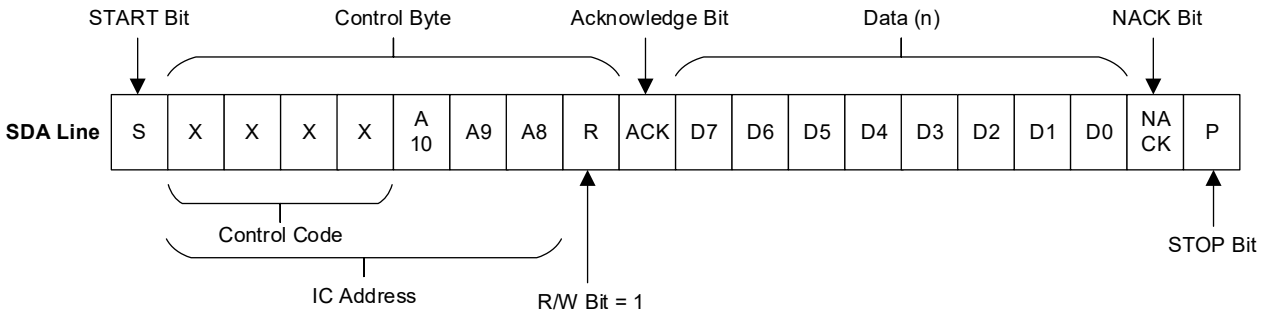


Figure 135. Current Address Read Command, R/W = 1

19.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Controller issues a second control byte with the R/W bit set to “1”, after which the SLG47104 issues an Acknowledge bit, followed by the requested eight data bits.

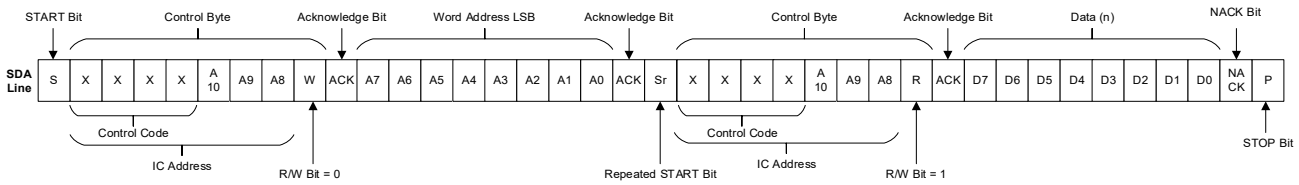


Figure 136. Random Read Command

19.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that, once the SLG47104 transmits the first data byte, the Bus Controller issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Controller can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

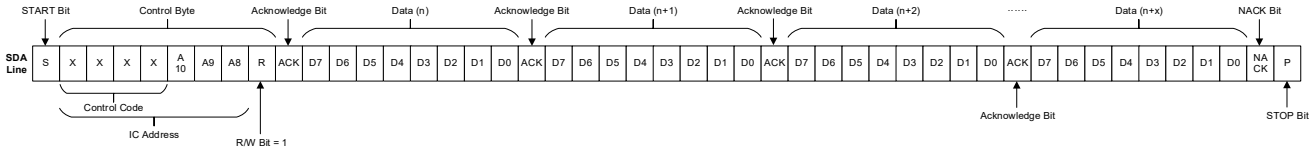


Figure 137. Sequential Read Command

19.5 I²C Serial Command Register Map

19.5.1 Register Read/Write Protection

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 38 for details.

Table 38. Read/Write Protection Options

Configurations	Protection Modes Configuration							Data Output From	Register Address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
I²C Byte Write Bit Masking (section 19.5.5 I2C Byte Write Bit Masking)	R/W	R/W	R/W	R/W	W	R	-	Memory	F6
I²C Serial Reset Command (section 19.5.2 I2C Serial Reset Command)	R/W	R/W	R/W	R/W	W	R	-	Memory	F5,b'0
Outputs LATCHing During I²C Write	R/W	R/W	R/W	R/W	W	R	-	Memory	F5,b'1
Connection Matrix Virtual Inputs (section 9.3 Connection Matrix Virtual Inputs)	R/W	R/W	R/W	R/W	W	R	-	Macrocell	4C
Configuration Bits for All Macrocells (IO Pins, ACMP, Combination Function Macrocells, and others)	R/W	R/W	W	-	W	R	-	Memory	

Configurations	Protection Modes Configuration							Data Output From	Register Address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
Macrocells Inputs Configuration (Connection Matrix Outputs, section 9.2 Matrix Output Table)	R/W	W	W	-	W	R	-	Memory	0~47
Protection Mode Enable	R	R	R	R	R	R	R	Memory	F5,b'4
Protection Mode Selection	R/W	R	R	R	R	R	R	Memory	F5,b'7~5
Macrocells Output Values (Connection Matrix Inputs, section 9.1 Matrix Input Table)	R	R	R	R	-	R	-	Marocell	48~4B; 4D~4F
Counter Current Value (for 8-bit CNT)	R	R	R	R	-	R	-	Marocell	8B, A4, A5
I^2C Control Code (section 19.2 I2C Serial Communications Device Addressing)	R	R	R	R	R	R	R	Memory	FD,b'3~0
Pin Target Address Select	R	R	R	R	R	R	R	Memory	FD,b'7~4
I^2C Disable/Enable	R	R	R	R	R	R	R	Memory	FE,b'0

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I^2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allow identifying silicon family, its revision, and others.

19.5.2 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1960] I²C reset bit to "1", which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1960] will be set to "0" automatically. Figure 138 illustrates the sequence of events for this reset function.

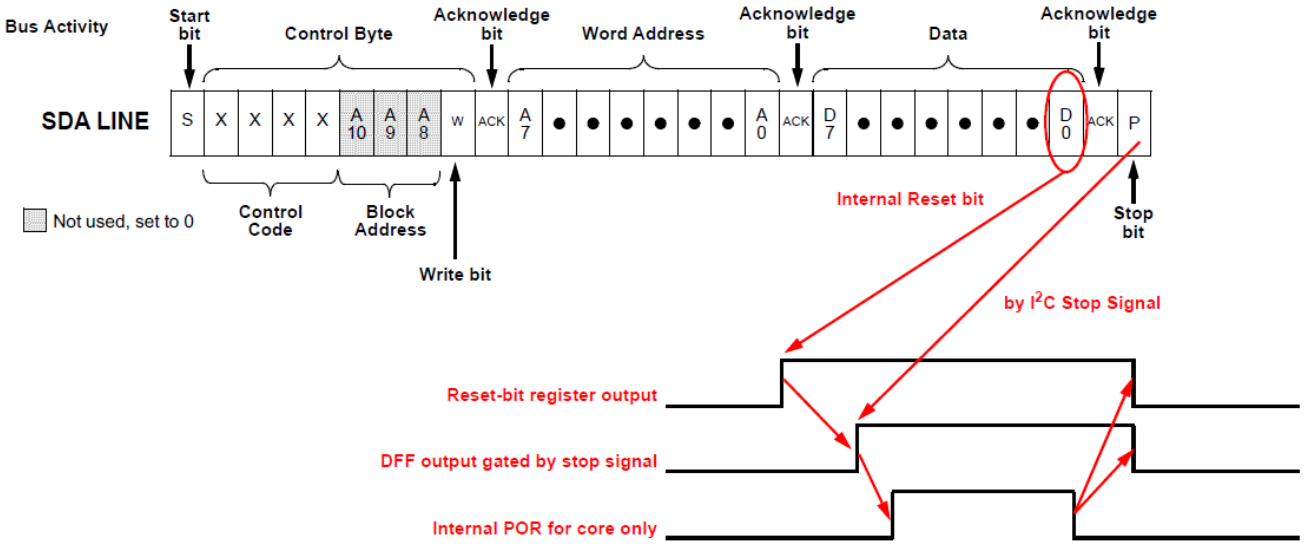


Figure 138. Reset Command Timing

19.5.3 I²C Additional Options

When Output latching during I²C write, register [1961] = 1 allows all Pins output value to be latched until I²C write is done. It will protect the output change due to configuration process during I²C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I²C write.

If the user sets GPIO3 and GPIO2 function to a selection other than SDA and SCL, all access via I²C will be disabled.

Note: Any write commands that come to the device via I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

19.5.4 Reading Current Counter Data via I²C

The current counter value of one counter in the device can be read via I²C. The counters that have this additional functionality is 16-bit CNT0.

19.5.5 I²C Byte Write Bit Masking

The I²C macrocell inside SLG47104 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see section 19.4.1 Byte Write Command for details) on the I²C Byte Write Mask Register (address 0xF6) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to "1" in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 139 shows an example of this function.

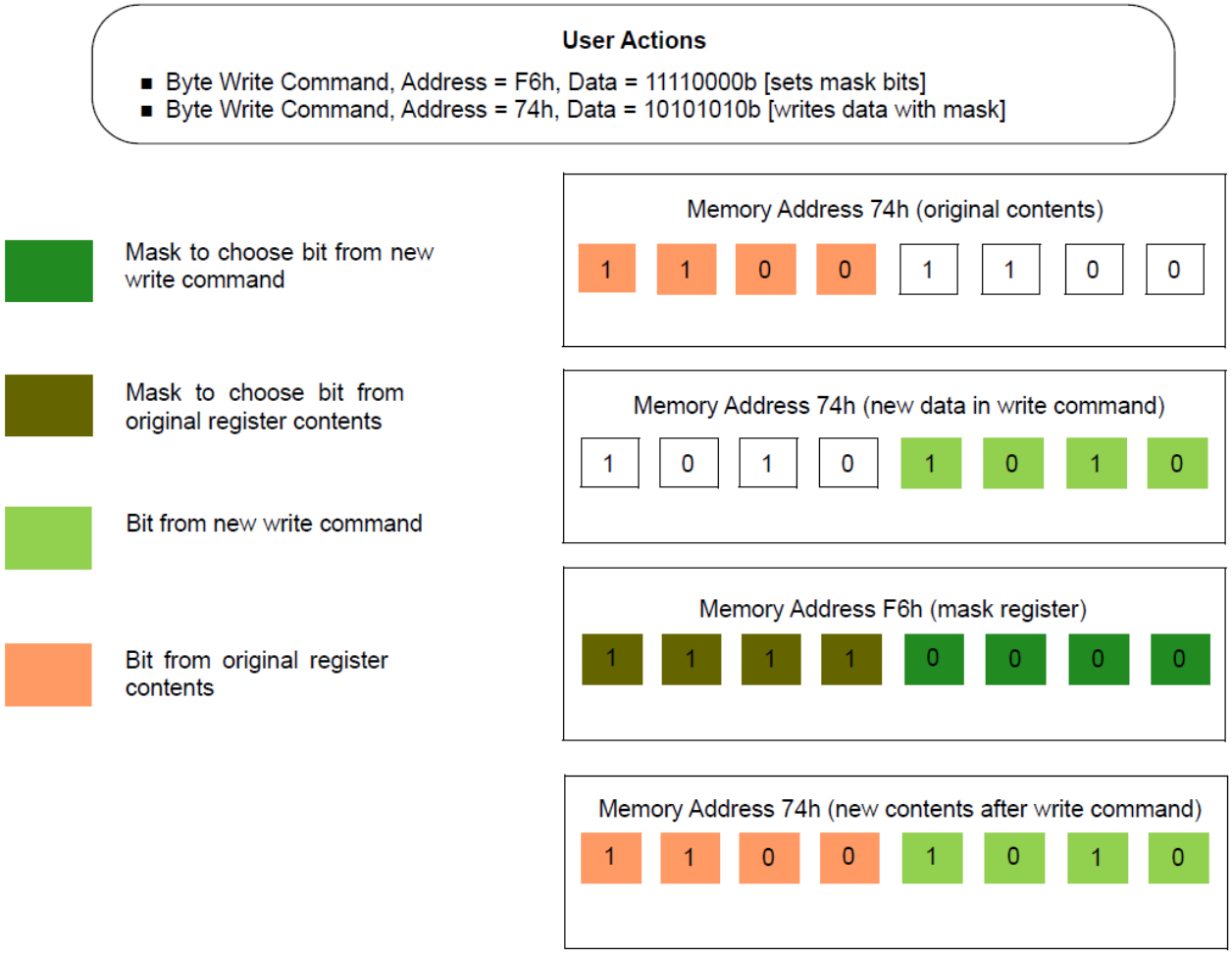


Figure 139. Example of I²C Byte Write Bit Masking

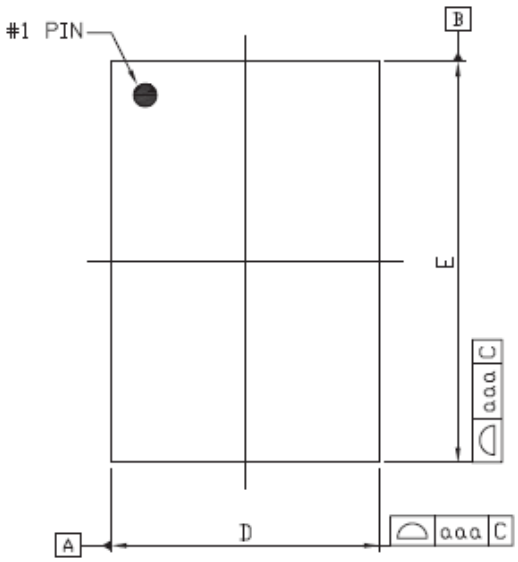
20. Package Information

20.1 Package Outline Drawings

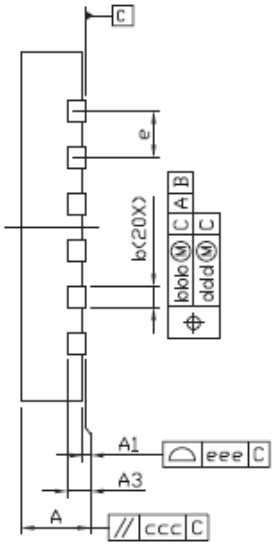
20.1.1 STQFN-20 (2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) FCD

JEDEC MO-220

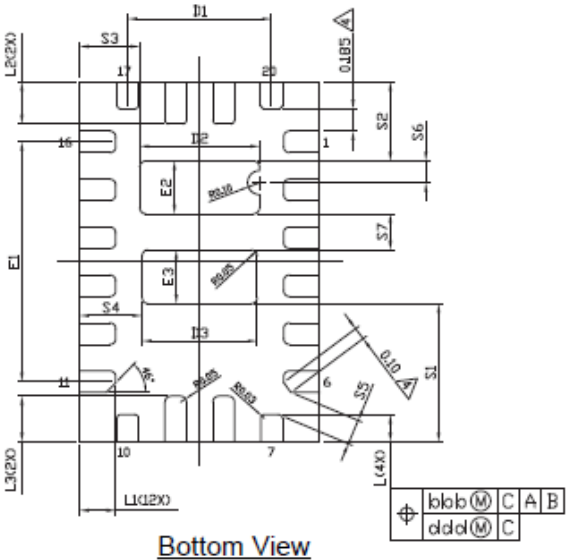
IC Net Weight: 0.008 g



Top View



Side View



Bottom View

Notes:

1. All dimensions are in millimeters.

2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

3. Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminal.

Controlling dimension: mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.95	2.00	2.05	0.077	0.079	0.081
E	2.95	3.00	3.05	0.116	0.118	0.120
D1	1.15	1.20	1.25	0.045	0.047	0.049
E1	1.95	2.00	2.05	0.077	0.079	0.081
D2	0.95	1.00	1.05	0.037	0.039	0.041
E2	0.39	0.44	0.49	0.015	0.017	0.019
D3	0.91	0.96	1.01	0.036	0.038	0.040
E3	0.40	0.45	0.50	0.016	0.018	0.020
S1	1.10	1.15	1.20	0.043	0.045	0.047
S2	0.61	0.66	0.71	0.024	0.026	0.028
S3	0.45	0.50	0.55	0.018	0.020	0.022
S4	0.47	0.52	0.57	0.018	0.020	0.022
S5	0.208 REF			0.008 REF		
S6	0.180 REF			0.007 REF		
S7	0.300 REF			0.012 REF		

“A1” max lead co-planarity 0.05 mm
Standard tolerance: ±0.05

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.250	0.300	0.350	0.010	0.012	0.014
L2	0.300	0.350	0.400	0.012	0.014	0.016
L3	0.330	0.380	0.430	0.013	0.015	0.017
b	0.130	0.180	0.230	0.005	0.007	0.009
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.1			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

Figure 140. STQFN-20 Package Outline Drawing

20.2 Package Top Marking

20.2.1 STQFN-20 (2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) FCD

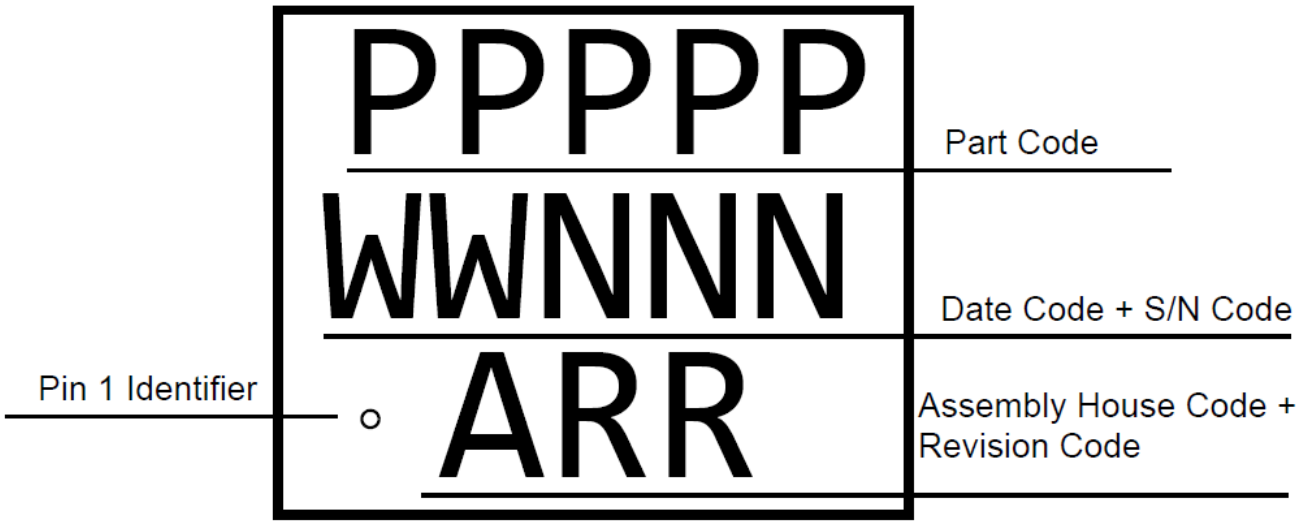


Figure 141. STQFN-20 Package Top Marking

20.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 39.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

Table 39. MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 60 % RH

20.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from www.jedec.org.

21. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to +85 °C. To guarantee reliable operation, the junction temperature of the SLG47104 must not exceed +150 °C.

To avoid overheating of the power MOSFETs (as shown in Figure 142), a good thermal design of the PCB layout must be implemented, especially when device operates near its maximum thermal limits. Refer to section 3.4 Thermal Specifications to find max value of Thermal Resistance.

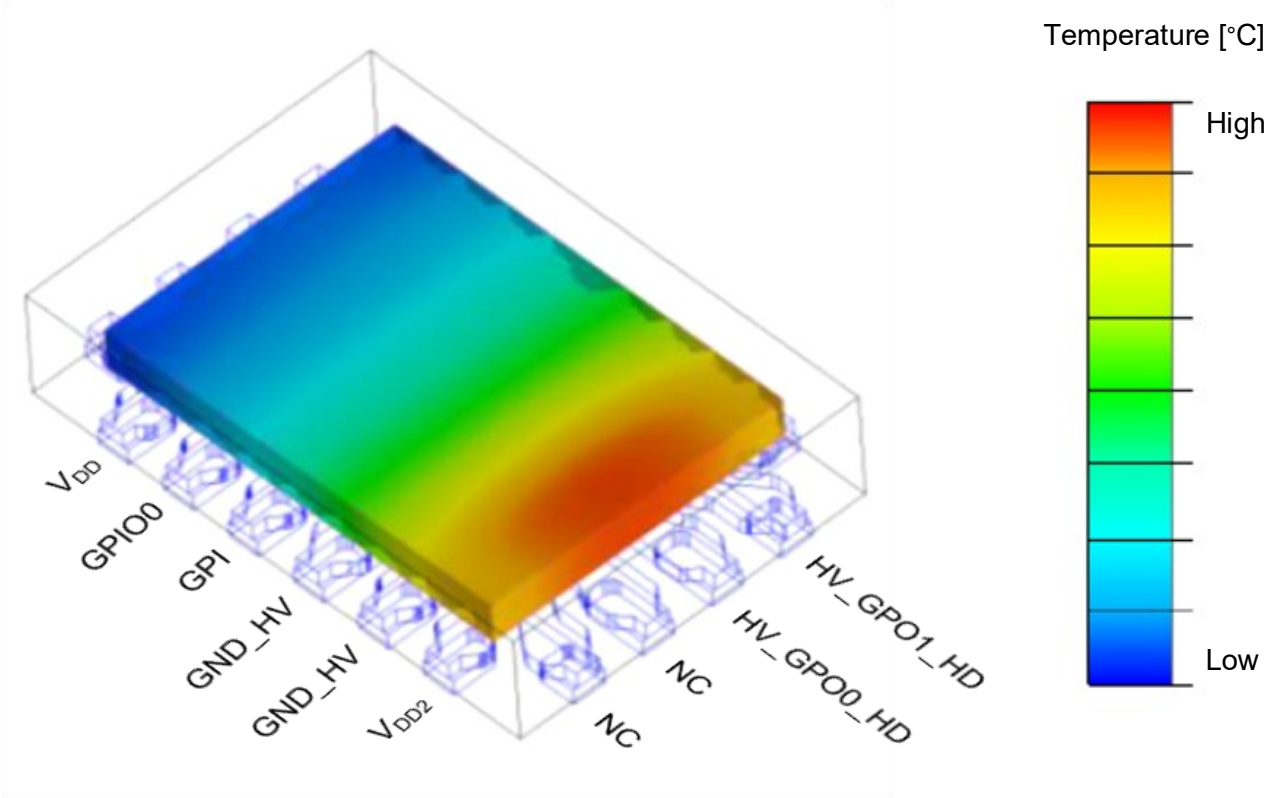


Figure 142. Die Temperature when HV OUTs are Active

22. Layout Consideration

PCB should have enough ground plane to dissipate heat. SLG47104 has two additional pads which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.

The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters. Typical Application Circuit is shown in Figure 143.

Both V_{DD2} pins should be connected together. Also, all three GND_HV pins should be connected together.

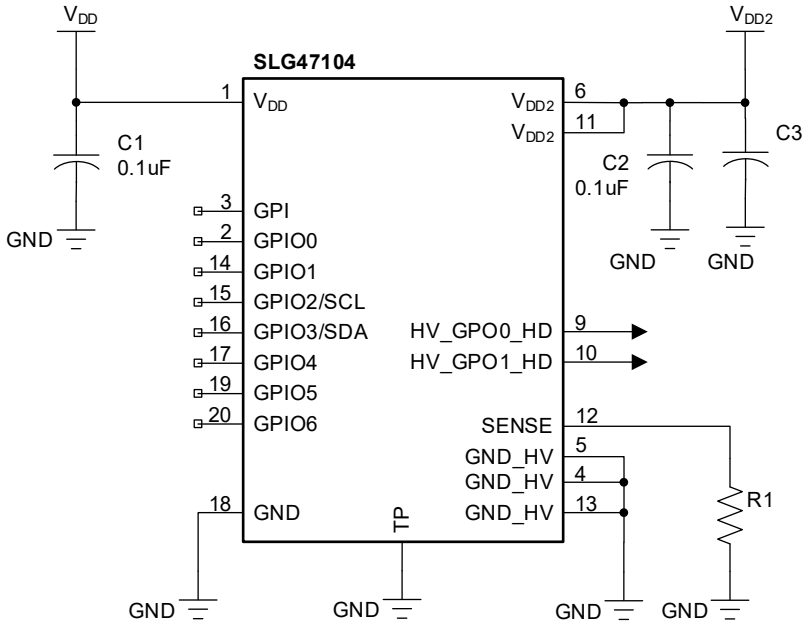


Figure 143. Typical Application Circuit

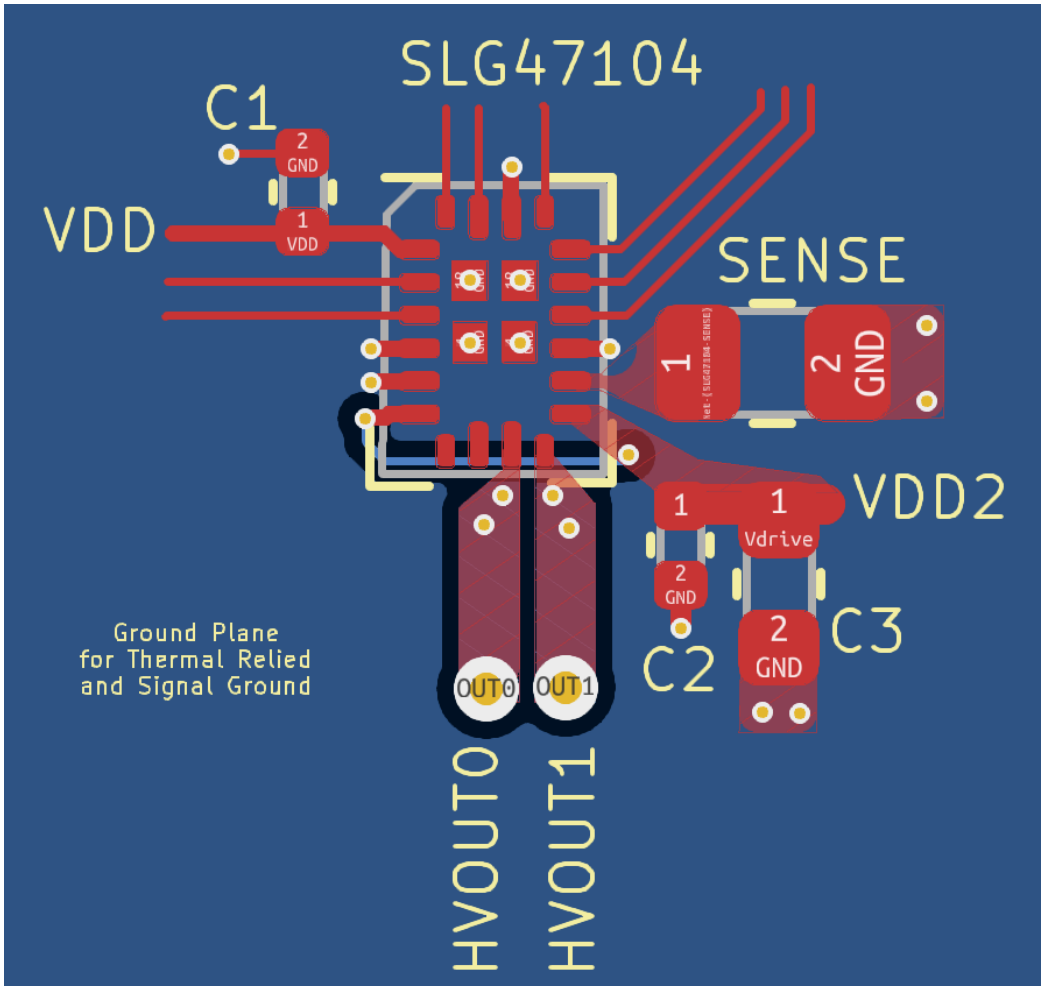


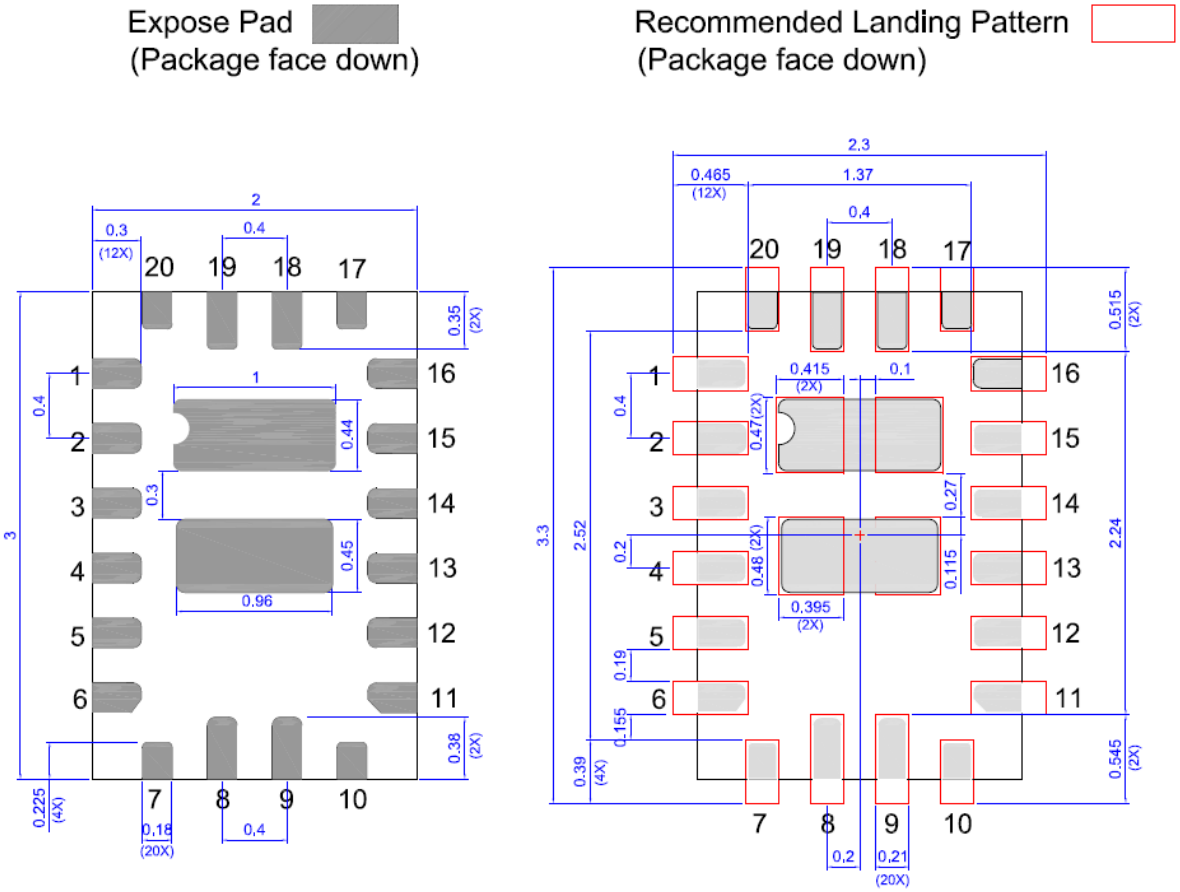
Figure 144. PCB Layout Example

23. Layout Guidelines

23.1 STQFN-20 (2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch), FCD

It's highly recommended to place low-ESR capacitor between V_{DD2}, and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it's highly recommended to place 0.1 µF ceramic capacitor between V_{DD} and GND.



24. Ordering Information

Part Number	Type
SLG47104	20-pin STQFN
SLG47104TR	20-pin STQFN - Tape and Reel (3k units)

Note 1: Use SLG47104 to order. Shipments are automatically in Tape and Reel.

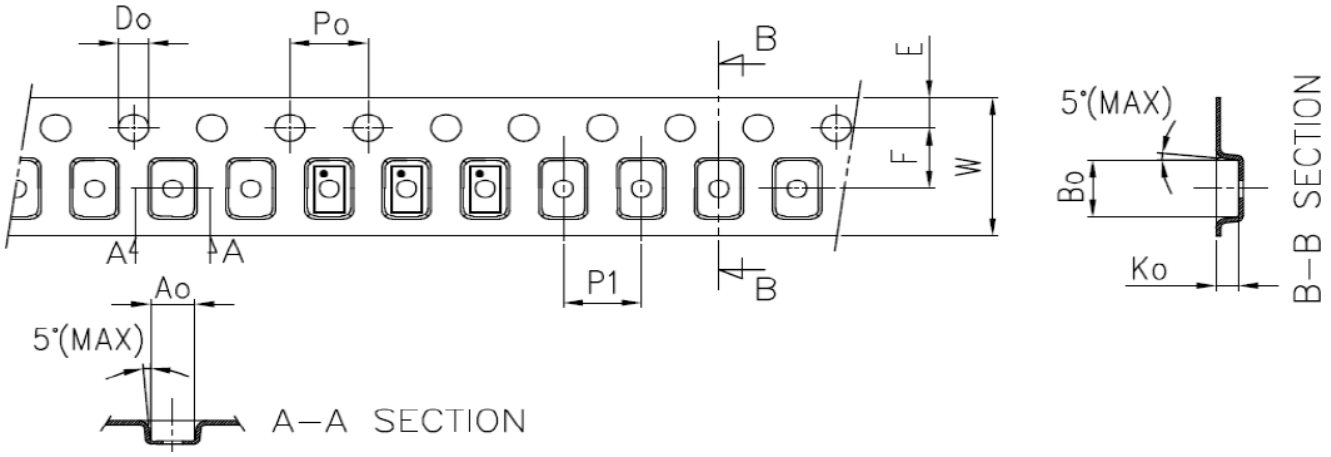
Note 2: “TR” suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

24.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Unit		Reel and Hub [mm]	Leader [mm]		Trailer [mm]		Tape Width [mm]	Part Pitch [mm]
			Per Reel	Per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green	20	2.0 x 3.0 x 0.55	3000	3000	178/60	100	400	100	400	8	4

24.2 Carrier Tape Drawing and Dimensions

Package Type	PocketB™ Length [mm]	PocketB™ Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Glossary

A

ACK	Acknowledge Bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed

B

BG	Bandgap

C

CCMP	Current Sense Comparator
CLK	Clock
CMO	Connection Matrix Output
CNT	Counter

D

DFF	D Flip-flop
DLY	Delay

E

ESD	Electrostatic Discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

H

HD	High Current Drive
HV	High Voltage

I

IN	Input
IO	Input/Output

L

LP_BG	Low Power Bandgap
LPF	Low Pass Filter
LS	Level Shifter
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OCP	Overcurrent Protection
OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PWM	Pulse Width Modulator
PWR	Power

R

RW	Read/Write

S

SCL	I²C Clock Input
SDA	I²C Data Input/Output
SLA	Target Address
SMT	With Schmitt Trigger
SV	nSet Value

T

TSD	Thermal Shutdown

U

UVLO	Under-Voltage Lockout

V

V_{REF}	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
1.00	23-Jun-2025	Initial revision

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
SLG47104	20	STQFN-20	TQFN

A.2 Symbol Pin Information

A.2.1 20 - STQFN

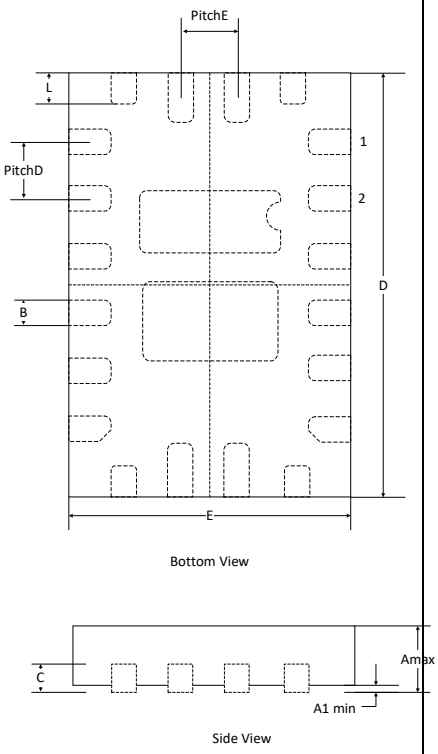
Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	V_{DD}	Power	-
2	GPIO0	I/O	-
3	GPI	Input	-
4	GND_HV	Power	-
5	GND_HV	Power	-
6	V_{DD2}	Power	-
7	NC	nc	-
8	NC	nc	-
9	HV_GPO1_HD	Output	-
10	HV_GPO1_HD	Output	-
11	V_{DD2}	Power	-
12	SENSE	Power	-
13	GND_HV	Power	-
14	GPIO1	I/O	-
15	SCL	I/O	GPIO2
16	SDA	I/O	GPIO3
17	GPIO4	I/O	-
18	GND	Power	-
19	GPIO5	I/O	-
20	GPIO6	I/O	-

A.3 Symbol Parameters

Orderable Part Number	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Interface	GPIO	V_{ref}	ACMP/ CCMP	HV OUT	PWM	Combination. Multi-function	OSC	RoHS
SLG47104	Industrial	SMD	-40 °C	85 °C	2.3 V	5.5 V	I^2C	6	1	2	2	1	12	2	Yes

A.4 Footprint Design Information

IPC Footprint Type	Package Code/ POD number	Number of Pins
	TQFN	20

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.95	
Maximum body span (vertical side)	Dmax	3.05	
Minimum body span (horizontal side)	Emin	1.95	
Maximum body span (horizontal side)	Emax	2.05	
Minimum Lead Width	Bmin	0.13	
Maximum Lead Width	Bmax	0.23	
Minimum Lead Length	Lmin	0.175/0.25/0.30/0.33	
Maximum Lead Length	Lmax	0.275/0.35/0.40/0.43	
Number of pins (vertical side)	PinCountD	6	
Number of pins (horizontal side)	PinCountE	4	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side(center).	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	0.39/0.40	
Maximum thermal pad size (vertical side)	D2max	0.49/0.50	
Minimum thermal pad size (horizontal side)	E2min	0.95/0.91-	
Maximum thermal pad size (horizontal side)	E2max	1.05/1.01	
Maximum Height	Amax	0.60	
Minimum Standoff Height	A1min	0.00	

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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