SLG47920/SLG47921 Datasheet

2K Configurable Digital Array

Description

The SLG47920/SLG47921 are a small size, low-power devices for common FPGA applications. The user creates their circuit design by programming the One Time Programmable (OTP) Non-Volatile Memory (NVM) or providing bitstream through SPI Interface to configure the FPGA Core, the IO pins, and the macrocells of the chip. This highly versatile device allows a wide variety of FPGA applications to be implemented.

Features

- Dense Array of Configurable Logic
  - 2240 5-bit LUTs
  - 2240 DFFs
  - 10 kb Distributed Memory
  - 64 kb BRAM
- Power Supply Domains
  - Two separate domains (16 or 20 GPIOs per domain)
  - V_{DDIO0} and V_{DDIO1}: 1.71 V to 3.465 V
  - V_{DDC}: 1.1 V ± 5 %
- Clocking
  - High-frequency Oscillator
    - 50 MHz High-frequency Oscillator
    - 3 MHz Low-frequency Mode
  - Oscillator Post divider
    - Divide Oscillator clock by a power of 2 (range 1 to 128)
    - Two independent outputs
  - Two Phase-locked Loops (PLL)
    - Input from external source, internal oscillator or LVDS Differential clock
- Power-On Reset (POR)
- Flexible power-consumption control:
  - FPGA Core power control
  - Clock sources power control
  - BRAM deep-sleep/power-gated modes
- General Purpose IOs
  - 32 GPIO (SLG47920)
  - 40 GPIO (SLG47921)
  - Flexible configuration options:
    - Selectable drive strength (4/8/12 mA)
    - Optional pull-up – 1x or 2x
    - Optional pull-up control from FPGA Core
    - Optional Schmitt Trigger input
  - Six LVDS Capable GPIOs (three true-LVDS pairs up to 100 Mbps)
  - Fast Routing capability between pairs of GPIO located in different IO voltage domains
- Bitstream security features:
  - CRC Integrity Check
  - AES Decryption
- Configuration Options
  - OTP Mode – load from built-in OTP memory
  - SPI Controller (Master) Mode – load from external Flash memory
  - SPI Target (Slave) Mode – load from external source (MCU host)
- Boot control logic: can address up to 16 different bitstreams from external memory
- Two idle low-power modes:
  - Sleep mode when configuration is being retained and no device re-configuration is needed
  - Reset mode when device re-configuration is required after exit from this mode
  - Possibility to retain GPIOs and BRAM states in both low power modes
  - Low power consumption in both modes (<85 µA)
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - SLG47920
    - 40-pin LQFN: 5.0 mm x 5.0 mm, 0.4 mm pitch
  - SLG47921:
    - 48-pin LQFN: 6.0 mm x 6.0 mm, 0.4 mm pitch
    - 48-pin WLCSP: 3.241 mm x 2.575 mm, 0.35 mm pitch

Applications

- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Notebooks and Tablet PCs
- Industrial Instrumentation and Control

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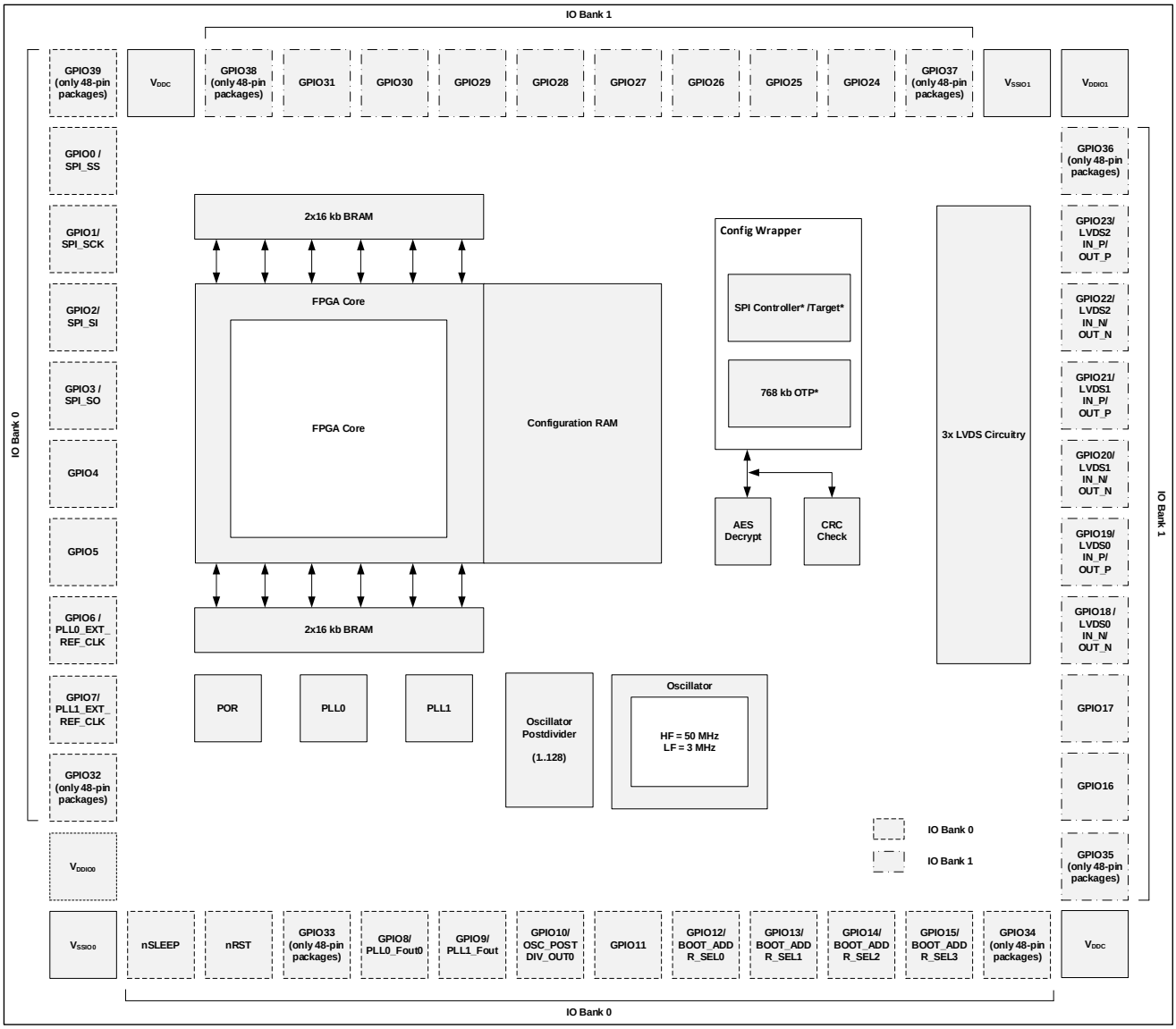
1. Overview

The components of the SLG47920/SLG47921 are shown in the Block Diagram (Figure 1).

1.1 Block Diagram



*SPI Controller/Target and OTP can be accessed only for configuration mode.

Figure 1. Block Diagram

1.2 Block Description

The SLG47920/SLG47921 are FPGA devices with 2.2k of LUTs and 2.2k DFFs available for user-defined digital logic. Main blocks of SLG47920/SLG47921 are described below.

Power-on Reset

The POR circuit monitors the V_{DDIO} (V_{DDIO0} and V_{DDIO1} pins) and V_{DDC} power supplies and keeps the SLG47920/SLG47921 in reset state upon power up until V_{DDIO} and V_{DDC} are within the specified voltage ranges. The POR reset will occur if power rails drop below the specified voltage range after the device has been powered up. A POR reset will tri-state all GPIOs.

GPIOs

The GPIO pins are general purpose programmable Digital IO circuits that can be programmed as an input or an output to the device. The GPIO pins connect to the FPGA Core. GPIO [3:0] are used to configure the device in SPI mode. GPIO[23:18] can operate in LVDS mode.

FPGA Core

The device core consists of the FPGA Core and a ring of interface blocks called Input-Output Buffers (IOBs). The IOBs are inputs/outputs to FPGA Core and are used to communicate between FPGA Core and other sub-blocks. The FPGA Core itself, consists of an array of Configurable Logic Blocks (CLBs). Each CLB contains LUTs, Registers, 4-bit carry chain, and a clock network which are used to implement user-defined logic functions. In addition, some CLBs in the FPGA Core can be configured in Embedded Memory Mode (EMM) and Shift Register Mode (SRM). These modes are used to act as distributed memory. The Configuration RAM is a volatile memory that stores the FPGA design after chip configuration and can be loaded from the OTP or the SPI Blocks.

BRAM

The 64 kb BRAM is an SRAM block that can be programmed in different width and depth configurations. Each 16 kb BRAM has one write port, one read port, and can be configured as a simple dual port SRAM. There are four 16 kb BRAM instances that interface with the FPGA Core. The BRAM does not connect directly with the GPIO. The width and depth configurations for the write and read ports must be the same.

OTP Block

The 768 kb OTP is used to store user defined configuration. OTP is a One Time Programmable NVM block that allows users to store the FPGA design once the design has been finalized. In such case user bitstream is stored inside the device.

SPI

The SPI Controller (Master) (Note) and SPI Target (Slave) (Note) are dedicated circuits that allow to configure SLG47920/SLG47921 FPGA Core from external source of bitstream. The SPI Controller and SPI Target connect to GPIO0 (SPI_CS), GPIO1 (SPI_SCK), GPIO2 (SPI_SI) and GPIO3 (SPI_SO). In this case user's bitstream is stored outside of the device and it transmitted to SLG47920/SLG47921 via SPI line during configuration process.

Note: For SPI Interface Controller is used as substitution for Master and Target is used as substitution for Slave. As for commonly used line names MISO (Master Input Slave Output) and MOSI (Master Output Slave Input) – they are used without change. Also, EC tables parameters related to SPI use M and S indexes.

Clocking

SLG47920/SLG47921 has the following clock sources:

- Oscillator (selectable High Frequency or Low Frequency mode) – available for user only through Oscillator Post Divider or as reference clock for PLLs.
- Oscillator Post Divider (division factor – powers of 2 in range 1 to 128).
- Two PLLs (PLL0 with external Post Divider (two outputs) and PLL1 with internal Post Divider (single output).
- LVDS differential clock.

FPGA Core has totally available 4 clock domain.

Clock distribution network allows user to select which clocks are to be used for user-defined logic.

Other Blocks

AES Decryption mechanism is used to decrypt bitstreams which are received through the SPI interface. It is optional and is disabled by default. Bitstream encryption allows user to ensure security of the design when it is transmitted through open interfaces and does not allow direct copying of the user-project.

A CRC Check mechanism is used to ensure integrity of configuration data that is being transferred during configuration process. It is applied to all configuration data regardless of the source (SPI interface or OTP). The CRC check is performed simultaneously with FPGA Core configuration process.

The nSLEEP(EN) and nRST(PWR) inputs are used to control the behavior and power consumption of SLG47920/SLG47921 as shown in Table 1.

Table 1. Block Control

nRST (PWR)	nSLEEP (EN)	Description
0	X	**Reset Mode**: Configuration of FPGA Core is not retained, and FPGA Core is power-gated. PLLs, OSC, and OTP memory are disabled. BRAM data are not retained unless option to retain content (***BRAM Keep***) is set (separate control for each BRAM). GPIOs in Hi-Z state and output state is not retained unless option to retain GPOs state (***GPIO Keep***) is set (common for all GPIOs).
1	0	**Sleep Mode**: Configuration and DFF states of FPGA Core are retained, and FPGA Core power is gated. PLL, OSC, and OTP memory are disabled. BRAM data are retained if BRAMs are not power gated with ***BRAM Power*** option (separate for each BRAM). GPIO not in Hi-Z state and output state is retained.
1	1	**Configuration Mode**: From internal OTP. From external SPI. From MCU interface. FPGA Core, GPIO, BRAM, PLL, and OSC controlled by Configuration Logic. OR **Functional Mode**: FPGA Core, GPIOs, PLLs, OSC, and others are under user control. Device performs user-defined functions.

2. Pin Information

2.1 Pin Assignments - LQFN-40/LQFN-48

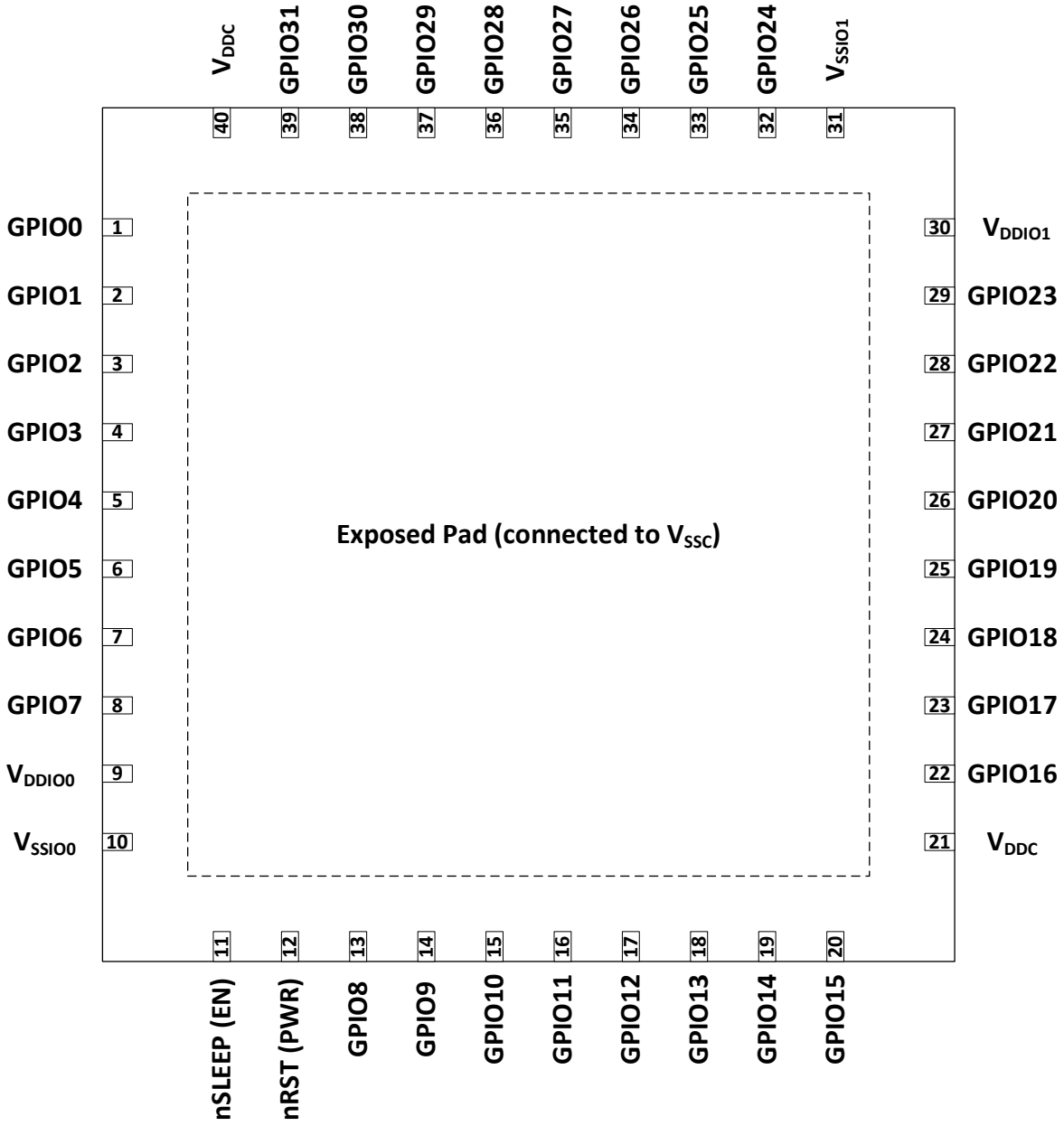


Figure 2. Pinout for 40-pin LQFN Package

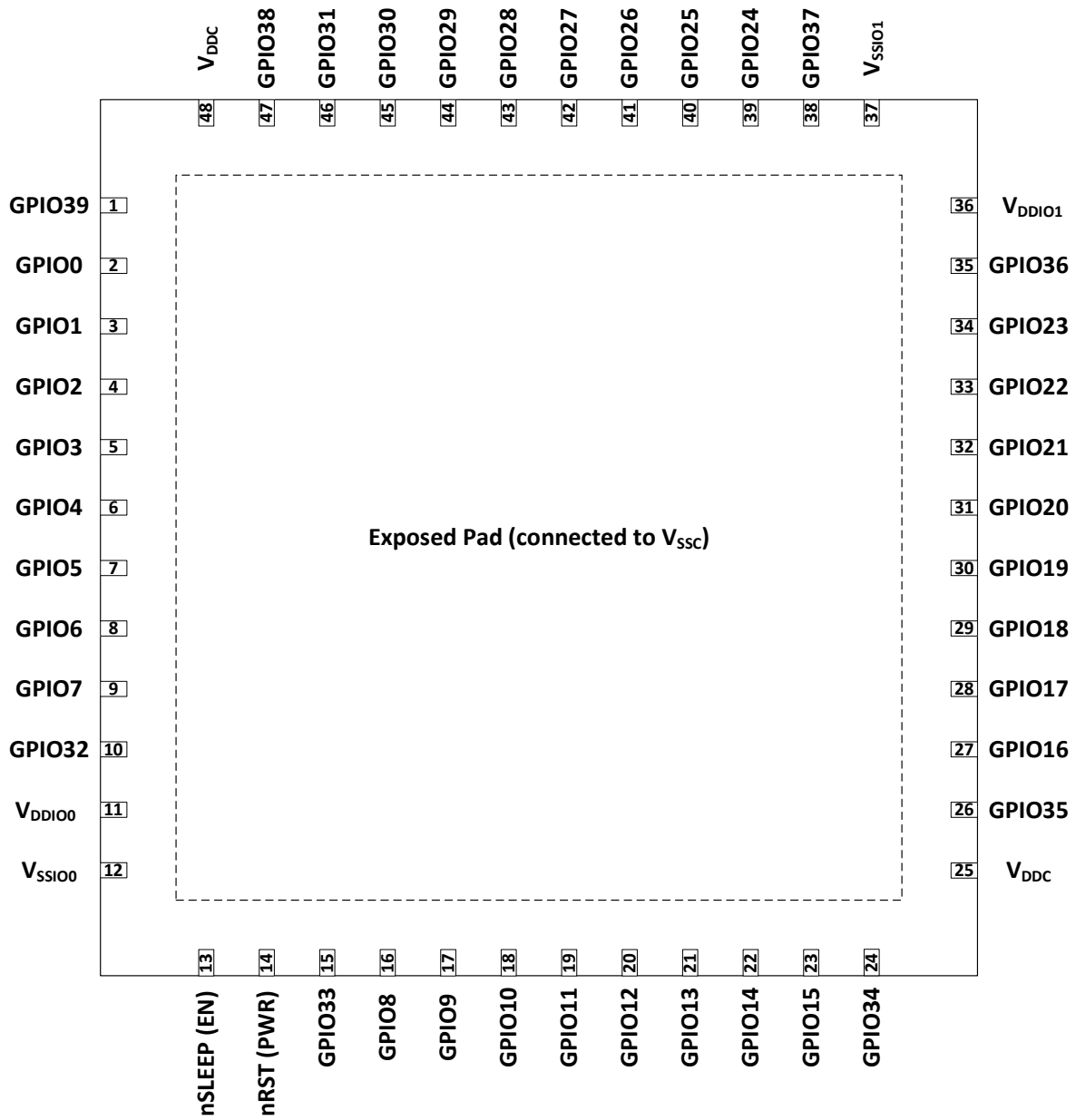


Figure 3. Pinout for 48-pin LQFN Package

Table 2. LQFN-40/48 Pin Configuration

Pin Number		Signal Name	V_{DDIO} Bank	Pin Functions
40 pins	48 pins			
12	14	nRST	V_{DDIO0}	Dedicated input pin to set device into Reset Mode. Active level – LOW.
11	13	nSLEEP	V_{DDIO0}	Dedicated input pin to set device in Sleep Mode. Active level – LOW.
1	2	GPIO0	V_{DDIO0}	General Purpose Input/Output or SPI_CS
2	3	GPIO1	V_{DDIO0}	General Purpose Input/Output or SPI_SCK
3	4	GPIO2	V_{DDIO0}	General Purpose Input/Output or SPI_SI
4	5	GPIO3	V_{DDIO0}	General Purpose Input/Output or SPI_SO or CONF_DONE
5	6	GPIO4	V_{DDIO0}	General Purpose Input/Output
6	7	GPIO5	V_{DDIO0}	General Purpose Input/Output
7	8	GPIO6	V_{DDIO0}	General Purpose Input/Output or PLL0_EXT_REF_CLK
8	9	GPIO7	V_{DDIO0}	General Purpose Input/Output or PLL1_EXT_REF_CLK
13	16	GPIO8	V_{DDIO0}	General Purpose Input/Output or PLL0_FOUT0
14	17	GPIO9	V_{DDIO0}	General Purpose Input/Output or PLL1_FOUT
15	18	GPIO10	V_{DDIO0}	General Purpose Input/Output or OSC_POSTDIV_OUT0
16	19	GPIO11	V_{DDIO0}	General Purpose Input/Output
17	20	GPIO12	V_{DDIO0}	General Purpose Input/Output or BOOT_ADDR_SEL0
18	21	GPIO13	V_{DDIO0}	General Purpose Input/Output or BOOT_ADDR_SEL1
19	22	GPIO14	V_{DDIO0}	General Purpose Input/Output or BOOT_ADDR_SEL2
20	23	GPIO15	V_{DDIO0}	General Purpose Input/Output or BOOT_ADDR_SEL3
22	27	GPIO16	V_{DDIO1}	General Purpose Input/Output
23	28	GPIO17	V_{DDIO1}	General Purpose Input/Output
24	29	GPIO18	V_{DDIO1}	General Purpose Input/Output or LVDS Channel 0 OUT_N/IN_N
25	30	GPIO19	V_{DDIO1}	General Purpose Input/Output or LVDS Channel 0 OUT_P/IN_P
26	31	GPIO20	V_{DDIO1}	General Purpose Input/Output or LVDS Channel 1 OUT_N/IN_N
27	32	GPIO21	V_{DDIO1}	General Purpose Input/Output or LVDS Channel 1 OUT_P/IN_P
28	33	GPIO22	V_{DDIO1}	General Purpose Input/Output or LVDS Channel 2 OUT_N/IN_N
29	34	GPIO23	V_{DDIO1}	General Purpose Input/Output or LVDS Channel 2 OUT_P/IN_P
32	39	GPIO24	V_{DDIO1}	General Purpose Input/Output
33	40	GPIO25	V_{DDIO1}	General Purpose Input/Output
34	41	GPIO26	V_{DDIO1}	General Purpose Input/Output
35	42	GPIO27	V_{DDIO1}	General Purpose Input/Output
36	43	GPIO28	V_{DDIO1}	General Purpose Input/Output
37	44	GPIO29	V_{DDIO1}	General Purpose Input/Output
38	45	GPIO30	V_{DDIO1}	General Purpose Input/Output
39	46	GPIO31	V_{DDIO1}	General Purpose Input/Output

Pin Number		Signal Name	V_{DDIO} Bank	Pin Functions
40 pins	48 pins			
N/A	10	GPIO32	V_{DDIO0}	General Purpose Input/Output
N/A	15	GPIO33	V_{DDIO0}	General Purpose Input/Output
N/A	24	GPIO34	V_{DDIO0}	General Purpose Input/Output
N/A	26	GPIO35	V_{DDIO1}	General Purpose Input/Output
N/A	35	GPIO36	V_{DDIO1}	General Purpose Input/Output
N/A	38	GPIO37	V_{DDIO1}	General Purpose Input/Output
N/A	47	GPIO38	V_{DDIO1}	General Purpose Input/Output
N/A	1	GPIO39	V_{DDIO0}	General Purpose Input/Output
21,40	25,48	V_{DDC}	N/A	Core Supply Voltage
9	11	V_{DDIO0}	N/A	IO Bank 0 Supply Voltage
30	36	V_{DDIO1}	N/A	IO Bank 1 Supply Voltage
ExpPAD [1]	ExpPAD [1]	V_{SSC}	N/A	Core GND
10	12	V_{SSIO0}	N/A	IO Bank 0 GND
31	37	V_{SSIO1}	N/A	IO Bank 1 GND
[1] ExpPAD - Exposed PAD on the bottom side of QFN package.				

Note: Some GPIOs also have secondary functions assigned. These functions are active only in certain operating mode (or activated with dedicated SW options). In other cases, they operate as simple GPIO (when in Functional mode).

2.2 Pin Assignments - WLCSP-48

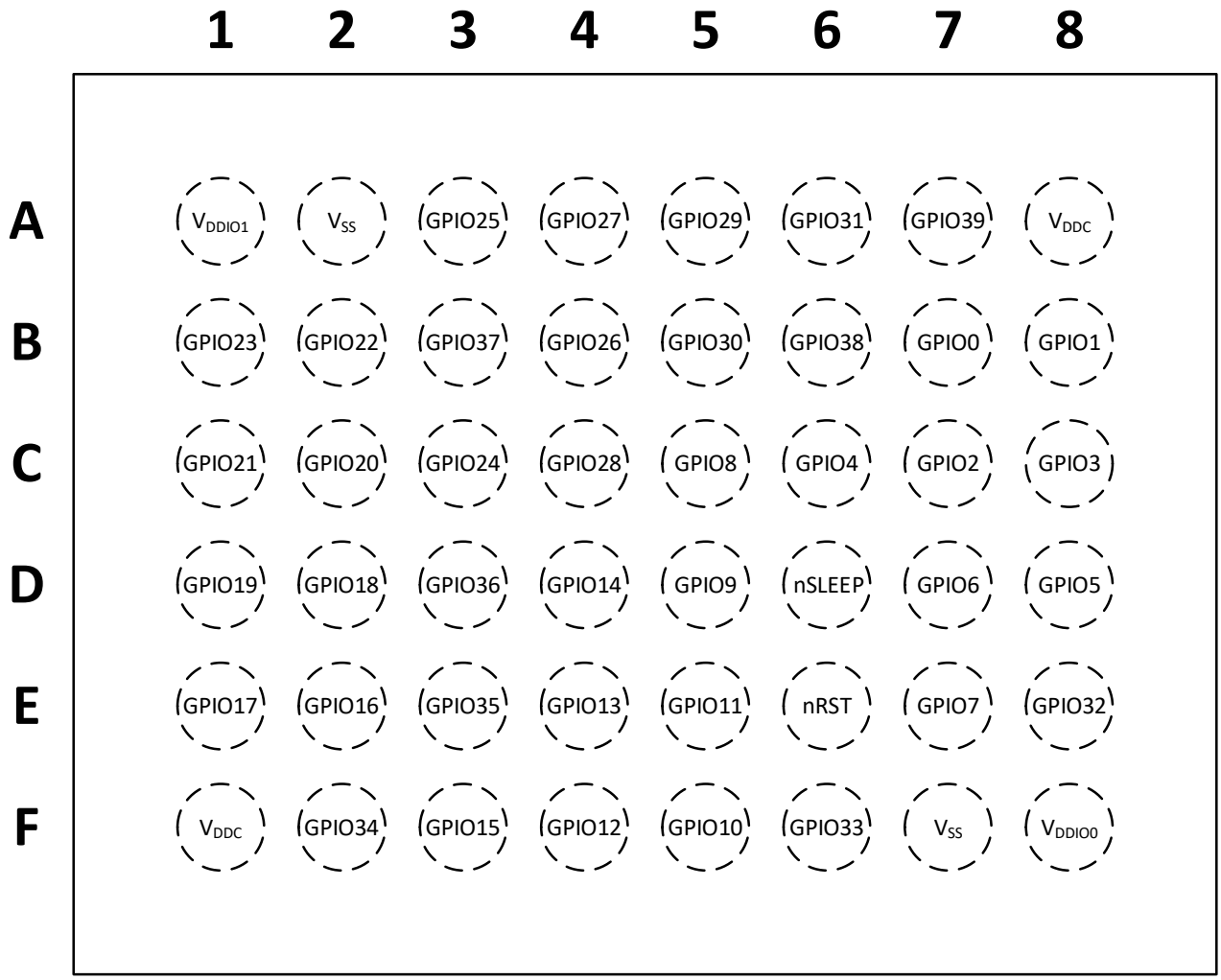


Figure 4. Pinout for 48-pin WLCSP Package (Top View)

Table 3. WLCSP-48 Pin Configuration

Pin#	Signal Name	V_{DDIO} Bank	Pin Function
D6	nSLEEP (EN)	V_{DDIO0}	Dedicated input pin to set device in Sleep Mode. Active level – LOW.
E6	nRST (PWR)	V_{DDIO0}	Dedicated input pin to set device into Reset Mode. Active level – LOW.
B7	GPIO0	V_{DDIO0}	General purpose Input/Output or SPI_CS
B8	GPIO1	V_{DDIO0}	General purpose Input/Output or SPI_SCK
C7	GPIO2	V_{DDIO0}	General purpose Input/Output or SPI_SI
C8	GPIO3	V_{DDIO0}	General purpose Input/Output or SPI_SO or CONF_DONE
C6	GPIO4	V_{DDIO0}	General purpose Input/Output
D8	GPIO5	V_{DDIO0}	General purpose Input/Output
D7	GPIO6	V_{DDIO0}	General purpose Input/Output or PLL0_EXT_REF_CLK
E7	GPIO7	V_{DDIO0}	General purpose Input/Output or PLL1_EXT_REF_CLK
C5	GPIO8	V_{DDIO0}	General purpose Input/Output or PLL0_FOUT0
D5	GPIO9	V_{DDIO0}	General purpose Input/Output or PLL1_FOUT
F5	GPIO10	V_{DDIO0}	General purpose Input/Output or OSC_POSTDIV_OUT0
E5	GPIO11	V_{DDIO0}	General purpose Input/Output
F4	GPIO12	V_{DDIO0}	General purpose Input/Output or BOOT_ADDR_SEL0
E4	GPIO13	V_{DDIO0}	General purpose Input/Output or BOOT_ADDR_SEL1
D4	GPIO14	V_{DDIO0}	General purpose Input/Output or BOOT_ADDR_SEL2
F3	GPIO15	V_{DDIO0}	General purpose Input/Output or BOOT_ADDR_SEL3
E2	GPIO16	V_{DDIO1}	General purpose Input/Output
E1	GPIO17	V_{DDIO1}	General purpose Input/Output
D2	GPIO18	V_{DDIO1}	General purpose Input/Output or LVDS Channel 0 OUT_N/IN_N
D1	GPIO19	V_{DDIO1}	General purpose Input/Output or LVDS Channel 0 OUT_P/IN_P
C2	GPIO20	V_{DDIO1}	General purpose Input/Output or LVDS Channel 1 OUT_N/IN_N
C1	GPIO21	V_{DDIO1}	General purpose Input/Output or LVDS Channel 1 OUT_P/IN_P
B2	GPIO22	V_{DDIO1}	General purpose Input/Output or LVDS Channel 2 OUT_N/IN_N
B1	GPIO23	V_{DDIO1}	General purpose Input/Output or LVDS Channel 2 OUT_P/IN_P
C3	GPIO24	V_{DDIO1}	General purpose Input/Output
A3	GPIO25	V_{DDIO1}	General purpose Input/Output
B4	GPIO26	V_{DDIO1}	General purpose Input/Output
A4	GPIO27	V_{DDIO1}	General purpose Input/Output
C4	GPIO28	V_{DDIO1}	General purpose Input/Output
A5	GPIO29	V_{DDIO1}	General purpose Input/Output
B5	GPIO30	V_{DDIO1}	General purpose Input/Output
A6	GPIO31	V_{DDIO1}	General purpose Input/Output
E8	GPIO32	V_{DDIO0}	General purpose Input/Output

Pin#	Signal Name	V_{DDIO} Bank	Pin Function
F6	GPIO33	V_{DDIO0}	General purpose Input/Output
F2	GPIO34	V_{DDIO0}	General purpose Input/Output
E3	GPIO35	V_{DDIO1}	General purpose Input/Output
D3	GPIO36	V_{DDIO1}	General purpose Input/Output
B3	GPIO37	V_{DDIO1}	General purpose Input/Output
B6	GPIO38	V_{DDIO1}	General purpose Input/Output
A7	GPIO39	V_{DDIO0}	General purpose Input/Output
A8, F1	V_{DDC}	N/A	Core supply voltage
F8	V_{DDIO0}	N/A	IO Bank 0 supply voltage
A1	V_{DDIO1}	N/A	IO Bank 1 supply voltage
A2, F7	V_{SSC}	N/A	Core GND
	V_{SSIO0}		IO Bank 1 GND
	V_{SSIO1}		IO Bank 2 GND

Note: Some GPIOs also have secondary functions assigned. These functions are active only in certain operating modes (or activated with dedicated SW options). In other cases, they operate as simple GPIO.

2.3 Pin Descriptions

Table 4. Configuration/Functional Pin Descriptions

Signal Name		Function	IO	Description
Primary	**Secondary**			
nRST	-	Reset signal	Input	This signal allows to set the device into Reset Mode. Active – LOW.
nSLEEP	-	Sleep signal	Input	This signal allows to set the device into Sleep Mode. Active – LOW. Holding it LOW before OTP Configuration started – activates indication of configuration process success. Also, if it is held LOW after successful configuration – it would prevent the device from proceeding to Functional Mode until it is driven HIGH.
GPIO0	SPI_CS	SPI Controller Mode Configuration	Output	In SPI Controller Mode, this pin outputs Chip Select signal to external Flash memory. Also, depending on configuration method settings, the SPI_CS input is used to define SPI programming mode to be used.
		SPI Target Mode Configuration	Input	In SPI Target Mode, this pin inputs Chip Select signal from external controller. Also, depending on configuration method settings, the SPI_CS input is used to define SPI programming mode to be used.
	-	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO1	SPI_SCK	SPI Controller Mode Configuration	Clock Output	In SPI Controller Mode, this pin outputs SPI clock to external Flash memory.
		SPI Target Mode Configuration	Clock Input	In SPI Target Mode, this pin inputs SPI clock from external controller.
	-	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO2	SPI_SI (MISO)	SPI Controller Mode Configuration	Input	Serial Input (MISO) is a data pin. This pin is used to transmit data from the target to the controller. Whenever the target sends data, that data will be collected over the MISO pin by the controller.
	SPI_SI (MOSI)	SPI Target Mode Configuration		Serial Input (MOSI) is a data pin. This pin is used to transmit data from the controller to the target device. Whenever the controller sends data, that data will be collected over the MOSI pin by the target.
	-	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO3	SPI_SO (MOSI)/ CONFIG_DONE	SPI Controller Mode Configuration	Output	MOSI is a data pin. This pin is used to transmit data from the controller to the target device. Whenever the controller sends data, that data will be collected over the MOSI pin by the target. After configuration process is performed – this pin indicates if configuration was performed successfully or not.
	SPI_SO (MISO)/ CONFIG_DONE	SPI Target Mode Configuration		MISO is a data pin. This pin is used to transmit data from the target to the controller. Whenever the target sends data, that data will be collected over the MISO pin by the controller. In MCU Mode, the CONFIG signal is flagged at this pin. After configuration process is performed – this pin indicates if configuration was performed successfully or not. See section 10 Configuration Modes.

Signal Name		Function	IO	Description
Primary	Secondary			
GPIO3	CONFIG_DONE	OTP Mode Configuration	Output	After configuration process is performed – optionally this pin can indicate if configuration was performed successfully or not. See section 10 Configuration Modes.
	-	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.

Table 5. Global Pins Descriptions

Signal Name	Function	IO	Description
GPIO [5:4]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO [7:6]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	PLL External Reference CLK	Input	This IO can be programmed as a reference clock for the device in user function when receiving clock from PLL. GPIO6: PLL0_EXT_REF_CLK. GPIO7: PLL1_EXT_REF_CLK.
GPIO [10:8]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	Clock source to Pin out	Output	When activated with dedicated SW options – clock from different clock sources can be output to dedicated GPIOs: GPIO8: PLL0 Fout0. GPIO9: PLL1 Fout. GPIO10: Oscillator Postdivider Out0.
GPIO [11]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO [15:12]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	Boot Address Select	Input	When Boot Address Control is enabled – these GPIOs are used (all or only part of them) as controls to select needed boot address. See section 10 Configuration Modes.
GPIO [17:16]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO18	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	LVDS Pair 0 IN_N/OUT_N	IO	The pin functions as an input/output pin for LVDS Channel 0 N-terminal.
GPIO19	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	LVDS Pair 0 IN_P/OUT_P	IO	The pin functions as an input/output pin for LVDS Channel 0 P-terminal.
GPIO20	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	LVDS Pair 1 IN_N/OUT_N	IO	The pin functions as an input/output pin for LVDS Channel 1 N-terminal

Signal Name	Function	IO	Description
GPIO21	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	LVDS Pair 1 IN_P/OUT_P	IO	The pin functions as an input/output pin for LVDS Channel 1 P-terminal.
GPIO22	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	LVDS Pair 2 IN_N/OUT_N	IO	The pin functions as an input/output pin for LVDS Channel 2 N-terminal.
GPIO23	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	LVDS Pair 2 IN_P/OUT_P	IO	The pin functions as an input/output pin for LVDS Channel 2 P-terminal.
GPIO [31:24]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO [39:32]	General IO *(only for 48-pin packages)*	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.

3. Specifications

3.1 Absolute Maximum Ratings

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to the absolute maximum conditions for extended periods may affect the device reliability.

Parameter		Min	Max	Unit
Supply Voltage (V_{DDC})		-0.3	1.5	V
Supply Voltage (V_{DDIO0}, V_{DDIO1})		-0.3	3.6	V
Voltage at Digital Input Pins, IOL = -100 µA		-0.3	3.6	V
Maximum RMS or DC Current (through Single GPIO Pin)		-	40	mA
Current at Digital Input Pin		-1.0	1.0	mA
I_{VDDIO} DC Current through V_{DDIO} Pin [1]		-	650	mA
I_{VDDC} DC Current though V_{DDC} Pin [1]		-	650	mA
I_{GND} DC Current through GND [1]		-	650	mA
Continuous Power Dissipation (JESD51-7, T_A = +85 ºC)	LQFN-40, no Thermal Vias (Derate 38.2 mW/°C above T_A = +85 ºC)	-	2481	mW
	LQFN-48, no Thermal Vias (Derate 42.2 mW/°C above T_A = +85 ºC)	-	2743	mW
	WLCSP-48 (Derate 34.1 mW/°C above T_A = +85 ºC)	-	2218	mW
Storage Temperature Range		-65	150	°C
Junction Temperature		-	150	°C
Moisture Sensitivity Level		1		

[1] Package limit.

3.2 ESD Ratings

Parameter	Conditions	Min	Max	Unit
ESD Protection (Human Body Model)		2000	-	V
ESD Protection (Charge Device Model)		1300	-	V

3.3 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage (V_{DDC}) [1]	1.045	1.1	1.155	V
Supply Voltage (V_{DDIO}) [1]	1.71	2.5	3.465	V
Ambient Temperature (T_A) [2]	-40	25	85	°C
Capacitor Value at V_{DDC}	0.1	-	-	µF

[1] Device operation outside this range is not guaranteed. The nominal operating voltage is 1.1 V for V_{DDC} and 1.8 – 3.3 V for V_{DDIO}. A guard band of +/-5 % is provided to account for the V_{DDC}/V_{DDIO} fluctuation from the nominal voltage level.

[2] Parameters were measured with $T_A = T_J$.

3.4 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typ	Unit
Thermal Resistance	LQFN-40, 5.0 mm × 5.0 mm	θ_{JA}	Junction-to-ambient	26.2	°C/W
	LQFN-48, 6.0 mm × 6.0 mm			23.7	
	WLCSP-48, 3.241 mm × 2.575 mm			29.3	

3.5 Electrical Specifications

3.5.1. PLL Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Clock Frequency [3]	f_{IN}		5	-	500	MHz
Output Clock Frequency [3]	f_{OUT}		10	-	2000 [1] [2]	MHz
VCO Frequency [3]	f_{VCO}		500	-	2000 [2]	MHz
Output Duty Cycle [4]	f_{PLL_DC}	f_{OUT} VCO at any frequency	48	50	55	%
Number of PFD Cycles for PLL to Lock [4]	T_{PLL_LOCK}	Lock is defined as no cycle slips for 256 consecutive cycles	-	600	900	cycles
PFD Frequency Range [3]	f_{PFD}		5		f_{VCO}/16	MHz
Peak to Peak Period Jitter [4]	$t_{JIT\_10.2}$	f_{OUT} = 10.2 MHz	-	245	474	ps
Peak to Peak Period Jitter [4]	$t_{JIT\_55.6}$	f_{OUT} = 55.6 MHz	-	148	474	ps
Peak to Peak Period Jitter [4]	t_{JIT_100}	f_{OUT} = 100 MHz	-	98	581	ps
Peak to Peak Period Jitter [4]	t_{JIT_125}	f_{OUT} = 125 MHz	-	120	581	ps

[1] The PLL block can support this range but in practice it would be much less due to peripheral logic limitations.

[2] PLL0 with External Post Divider is limited with 1000 MHz value.

[3] Guaranteed by design, not tested in production.

[4] Guaranteed by characterization, not tested in production.

3.5.2. GPIOs Specifications

T_A = -40 °C to +85 °C, V_{DDC} = 1.1 V, V_{DDIO} = 1.71 V to 3.46 V, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input/Output Pin Capacitance	C_{IO_PIN}	Non-LVDS GPIO T_J = 25 °C $C_{IO\_PIN} = C_{GPIO} + C_{PAD} + C_{PIN}$	-	5.6	-	pF
		LVDS GPIO T_J = 25 °C $C_{IO\_PIN} = C_{GPIO} + C_{PAD} + C_{PIN}$	-	9.4	-	
Input Leakage Current	I_{I_LKG}	V_{DDIO} = 3.465 V, V_{IN} = 0 to V_{DDIO}	-600	-	600	nA
Max Absolute Data Skew - Output Paths [3]	$T_{SKEW\_DO\_PIN}$	V_{DDC} = 1.1 V ± 5 %	5.4	-	11.3	ns
Max Absolute Data Skew - Input Paths [3]	$T_{SKEW\_DI\_PIN}$	V_{DDC} = 1.1 V ± 5 %	6.5	-	14.6	ns
Minimal/Maximal Voltage Applied to Pins in Hi-Z State [3]	V_{I_LIMIT}		V_{SSIO} – 0.3	-	3.465	V
LVCMOS 1.8 V (Compatible with JESD8-7A, Normal Range), V_{DDIO} = 1.8 V ± 5 %						
V_{DDIO} Leakage Current	I_{DDIO_LKG}		-	0.32	3.9	µA
HIGH-Level Input Voltage	V_{IH}	Simple Input settings	0.65 x V_{DDIO}	-	3.465 [3]	V
		Schmitt-trigger input, no PU settings	0.65 x V_{DDIO}	-	3.465 [3]	V
		Schmitt-trigger input, 1xPU settings [2]	0.65 x V_{DDIO}	-	3.465 [3]	V
		Schmitt-trigger input, 2xPU settings [2]	0.65 x V_{DDIO}	-	3.465 [3]	V
LOW-Level Input Voltage	V_{IL}	Simple Input settings	-0.3 [3]	-	0.35 x V_{DDIO}	V
		Schmitt-trigger input, no PU settings	-0.3 [3]	-	0.35 x V_{DDIO}	V
		Schmitt-trigger input, 1xPU settings [2]	-0.3 [3]	-	0.35 x V_{DDIO}	V
		Schmitt-trigger input, 2xPU settings [2]	-0.3 [3]	-	0.35 x V_{DDIO}	V
HIGH-Level Output Voltage	V_{OH}	Push-pull 4 mA settings, I_{OH} = 0.5 mA [2]	V_{DDIO} - 0.45	-	-	V
		Push-pull 4 mA settings, I_{OH} = 1 mA [2]	V_{DDIO} - 0.45	-	-	V
		Push-pull 4 mA settings, I_{OH} = 2 mA	V_{DDIO} - 0.45	-	-	V
		Push-pull 8 mA settings, I_{OH} = 0.5 mA [2]	V_{DDIO} - 0.45	-	-	V
		Push-pull 8 mA settings, I_{OH} = 1 mA [2]	V_{DDIO} - 0.45	-	-	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-Level Output Voltage	V_{OH}	Push-pull 8 mA settings, I_{OH} = 2 mA	V_{DDIO} - 0.45	-	-	V
		Push-pull 12 mA settings, I_{OH} = 0.5 mA [2]	V_{DDIO} - 0.45	-	-	V
		Push-pull 12 mA settings, I_{OH} = 1 mA [2]	V_{DDIO} - 0.45	-	-	V
		Push-pull 12 mA settings, I_{OH} = 2 mA [2]	V_{DDIO} - 0.45	-	-	V
LOW-Level Output Voltage	V_{OL}	Push-pull 4 mA settings, I_{OL} = 0.5 mA [2]	-	-	0.45	V
		Push-pull 4 mA settings, I_{OL} = 1 mA [2]	-	-	0.45	V
		Push-pull 4 mA settings, I_{OL} = 2 mA	-	-	0.45	V
		Push-pull 8 mA settings, I_{OL} = 0.5 mA [2]	-	-	0.45	V
		Push-pull 8 mA settings, I_{OL} = 1 mA [2]	-	-	0.45	V
		Push-pull 8 mA settings, I_{OL} = 2 mA	-	-	0.45	V
		Push-pull 12 mA settings, I_{OL} = 0.5 mA [2]	-	-	0.45	V
		Push-pull 12 mA settings, I_{OL} = 1 mA [2]	-	-	0.45	V
		Push-pull 12 mA settings, I_{OL} = 2 mA [2]	-	-	0.45	V
		Open-drain 4 mA settings, I_{OL} = 2 mA	-	-	0.45	V
		Open-drain 8 mA settings, I_{OL} = 2 mA	-	-	0.45	V
		Open-drain 12 mA settings, I_{OL} = 2 mA [2]	-	-	0.45	V
HIGH-Level Output Current	I_{OH}	Push-pull 4 mA settings, V_{OH} = 1.35 V [2]	4.96	-	-	mA
		Push-pull 8 mA settings, V_{OH} = 1.35 V [2]	6.46	-	-	mA
		Push-pull 12 mA settings, V_{OH} = 1.35 V	10.83	-	-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Current	I_{OL}	Push-pull 4 mA settings, V_{OL} = 0.45 V [2]	5.95	-	-	mA
		Push-pull 8 mA settings, V_{OL} = 0.45 V [2]	8.57	-	-	mA
		Push-pull 12 mA settings, V_{OL} = 0.45 V	14.07	-	-	mA
		Open-drain 4 mA settings, V_{OL} = 0.45 V [2]	5.95	-	-	mA
		Open-drain 8 mA settings, V_{OL} = 0.45 V [2]	8.57	-	-	mA
		Open-drain 12 mA settings, V_{OL} = 0.45 V	14.07	-	-	mA
Max GPIO Output Frequency (20 % - 80 %) [1] [2]	F_{IO_MAX}	Push-pull 4 mA settings, C_{LOAD} = 10 pF	135	200	300	MHz
		Push-pull 8 mA settings, C_{LOAD} = 10 pF	170	250	380	MHz
		Push-pull 12 mA settings, C_{LOAD} = 10 pF	270	375	530	MHz
LVCMOS 2.5 V (Compatible with JESD8-5A.01, Normal Range), V_{DDIO} = 2.5 V ± 10 %						
V_{DDIO} Leakage Current	I_{DDIO_LKG}		-	1.6	5.8	µA
HIGH-Level Input Voltage	V_{IH}	Simple Input settings	1.7	-	3.465 [3]	V
		Schmitt-trigger input, no PU settings	1.7	-	3.465 [3]	V
		Schmitt-trigger input, 1xPU settings [2]	1.7	-	3.465 [3]	V
		Schmitt-trigger input, 2xPU settings [2]	1.7	-	3.465 [3]	V
LOW-Level Input Voltage	V_{IL}	Simple Input settings	-0.3 [3]	-	0.7	V
		Schmitt-trigger input, no PU settings	-0.3 [3]	-	0.7	V
		Schmitt-trigger input, 1xPU settings [2]	-0.3 [3]	-	0.7	V
		Schmitt-trigger input, 2xPU settings [2]	-0.3 [3]	-	0.7	V
HIGH-Level Output Voltage	V_{OH}	Push-pull 4 mA settings, I_{OH} = 0.5 mA [2]	2.1	-	-	V
		Push-pull 4 mA settings, I_{OH} = 1 mA [2]	2.0	-	-	V
		Push-pull 4 mA settings, I_{OH} = 2 mA	1.7	-	-	V
		Push-pull 8 mA settings, I_{OH} = 0.5 mA [2]	2.1	-	-	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-Level Output Voltage	V_{OH}	Push-pull 8 mA settings, I_{OH} = 1 mA [2]	2.0	-	-	V
		Push-pull 8 mA settings, I_{OH} = 2 mA	1.7	-	-	V
		Push-pull 12 mA settings, I_{OH} = 0.5 mA [2]	2.1	-	-	V
		Push-pull 12 mA settings, I_{OH} = 1 mA [2]	2.0	-	-	V
		Push-pull 12 mA settings, I_{OH} = 2 mA [2]	1.7	-	-	V
LOW-Level Output Voltage	V_{OL}	Push-pull 4 mA settings, I_{OL} = 0.5 mA [2]	-	-	0.2	V
		Push-pull 4 mA settings, I_{OL} = 1 mA [2]	-	-	0.4	V
		Push-pull 4 mA settings, I_{OL} = 2 mA	-	-	0.7	V
		Push-pull 8 mA settings, I_{OL} = 0.5 mA [2]	-	-	0.2	V
		Push-pull 8 mA settings, I_{OL} = 1 mA [2]	-	-	0.4	V
		Push-pull 8 mA settings, I_{OL} = 2 mA	-	-	0.7	V
		Push-pull 12 mA settings, I_{OL} = 0.5 mA [2]	-	-	0.2	V
		Push-pull 12 mA settings, I_{OL} = 1 mA [2]	-	-	0.4	V
		Push-pull 12 mA settings, I_{OL} = 2 mA [2]	-	-	0.7	V
		Open-drain 4 mA settings, I_{OL} = 2 mA	-	-	0.7	V
		Open-drain 8 mA settings, I_{OL} = 2 mA	-	-	0.7	V
		Open-drain 12 mA settings, I_{OL} = 2 mA [2]	-	-	0.7	V
HIGH-Level Output Current [2]	I_{OH}	Push-pull 4 mA settings, V_{OH} = 1.7 V	9.88	-	-	mA
		Push-pull 8 mA settings, V_{OH} = 1.7 V	13.19	-	-	mA
		Push-pull 12 mA settings, V_{OH} = 1.7 V	21.63	-	-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Current [2]	I_{OL}	Push-pull 4 mA settings, V_{OL} = 0.45 V	11.82	-	-	mA
		Push-pull 8 mA settings, V_{OL} = 0.45 V	17.11	-	-	mA
		Push-pull 12 mA settings, V_{OL} = 0.45 V	27.7	-	-	mA
		Open-drain 4 mA settings, V_{OL} = 0.45 V	11.82	-	-	mA
		Open-drain 8 mA settings, V_{OL} = 0.45 V	17.11	-	-	mA
		Open-drain 12 mA settings, V_{OL} = 0.45 V	27.7	-	-	mA
Max GPIO Output Frequency (20 % - 80 %) [1] [2]	F_{IO_MAX}	Push-pull 4 mA settings, C_{LOAD} = 10 pF	180	280	420	MHz
		Push-pull 8 mA settings, C_{LOAD} = 10 pF	240	350	530	MHz
		Push-pull 12 mA settings, C_{LOAD} = 10 pF	355	490	610	MHz
LVCMOS 3.3 V/LVTTL 3.3 V (Compatible with JESD8C.01, Narrow Range), V_{DDIO} = 3.3 V ± 5 %						
V_{DDIO} Leakage Current	I_{DDIO_LKG}		-	5	11	µA
HIGH-Level Input Voltage	V_{IH}	Simple Input settings	2.0	-	3.465 [3]	V
		Schmitt-trigger input, no PU settings	2.0	-	3.465 [3]	V
		Schmitt-trigger input, 1xPU settings [2]	2.0	-	3.465 [3]	V
		Schmitt-trigger input, 2xPU settings [2]	2.0	-	3.465 [3]	V
LOW-Level Input Voltage	V_{IL}	Simple Input settings	-0.3 [3]	-	0.8	V
		Schmitt-trigger input, no PU settings	-0.3 [3]	-	0.8	V
		Schmitt-trigger input, 1xPU settings [2]	-0.3 [3]	-	0.8	V
		Schmitt-trigger input, 2xPU settings [2]	-0.3 [3]	-	0.8	V
HIGH-Level Output Voltage	V_{OH}	Push-pull 4 mA settings, I_{OH} = 0.5 mA [2]	V_{DDIO} - 0.2	-	-	V
		Push-pull 4 mA settings, I_{OH} = 1 mA [2]	2.4	-	-	V
		Push-pull 4 mA settings, I_{OH} = 2 mA	2.4	-	-	V
		Push-pull 8 mA settings, I_{OH} = 0.5 mA [2]	V_{DDIO} - 0.2	-	-	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-Level Output Voltage	V_{OH}	Push-pull 8 mA settings, I_{OH} = 1 mA [2]	2.4	-	-	V
		Push-pull 8 mA settings, I_{OH} = 2 mA	2.4	-	-	V
		Push-pull 12 mA settings, I_{OH} = 0.5 mA [2]	V_{DDIO} - 0.2	-	-	V
		Push-pull 12 mA settings, I_{OH} = 1 mA [2]	2.4	-	-	V
		Push-pull 12 mA settings, I_{OH} = 2 mA [2]	2.4	-	-	V
LOW-Level Output Voltage	V_{OL}	Push-pull 4 mA settings, I_{OH} = 0.5 mA [2]	-	-	0.2	V
		Push-pull 4 mA settings, I_{OH} = 1 mA [2]	-	-	0.4	V
		Push-pull 4 mA settings, I_{OH} = 2 mA	-	-	0.4	V
		Push-pull 8 mA settings, I_{OH} = 0.5 mA [2]	-	-	0.2	V
		Push-pull 8 mA settings, I_{OH} = 1 mA [2]	-	-	0.4	V
		Push-pull 8 mA settings, I_{OH} = 2 mA	-	-	0.4	V
		Push-pull 12 mA settings, I_{OH} = 0.5 mA [2]	-	-	0.2	V
		Push-pull 12 mA settings, I_{OH} = 1 mA [2]	-	-	0.4	V
		Push-pull 12 mA settings, I_{OH} = 2 mA [2]	-	-	0.4	V
		Open-drain 4 mA settings, I_{OL} = 2 mA	-	-	0.4	V
		Open-drain 8 mA settings, I_{OL} = 2 mA	-	-	0.4	V
		Open-drain 12 mA settings, I_{OL} = 2 mA [2]	-	-	0.4	V
HIGH-Level Output Current [2]	I_{OH}	Push-pull 4 mA settings, V_{OH} = 2.4 V	17.08	-	-	mA
		Push-pull 8 mA settings, V_{OH} = 2.4 V	23.07	-	-	mA
		Push-pull 12 mA settings, V_{OH} = 2.4 V	36.97	-	-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW-Level Output Current [2]	I_{OL}	Push-pull 4 mA settings, V_{OL} = 0.4 V	9.39	-	-	mA
		Push-pull 8 mA settings, V_{OL} = 0.4 V	13.81	-	-	mA
		Push-pull 12 mA settings, V_{OL} = 0.4 V	21.43	-	-	mA
		Open-drain 4 mA settings, V_{OL} = 0.4 V	9.39	-	-	mA
		Open-drain 8 mA settings, V_{OL} = 0.4 V	13.81	-	-	mA
		Open-drain 12 mA settings, V_{OL} = 0.4 V	21.43	-	-	mA
Max GPIO Output Frequency (20 % - 80 %) [1] [2]	F_{IO_MAX}	Push-pull 4 mA settings, C_{LOAD} = 10 pF	245	340	480	MHz
		Push-pull 8 mA settings, C_{LOAD} = 10 pF	300	425	545	MHz
		Push-pull 12 mA settings, C_{LOAD} = 10 pF	440	535	630	MHz

[1] Defined from rise/fall time measured for output signal transition form 0.2 x V_{DDIO} to 0.8 x V_{DDIO} and considering 50 % duty cycle of output signal.

[2] Guaranteed by characterization, not tested in production.

[3] Guaranteed by design, not tested in production.

3.5.3. GPIO Pull-up Resistance Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull-up 1x (Single Resistor)	R_{PU1}	V_{DDIO} = 1.71 V to 1.89 V	-	175	-	kΩ
		V_{DDIO} = 2.25 V to 2.75 V	-	110	-	kΩ
		V_{DDIO} = 3.135 V to 3.465 V	-	82	-	kΩ
Pull-up 2x (Two Resistors in Parallel)	R_{PU2}	V_{DDIO} = 1.71 V to 1.89 V	-	88	-	kΩ
		V_{DDIO} = 2.25 V to 2.75 V	-	55	-	kΩ
		V_{DDIO} = 3.135 V to 3.465 V	-	41	-	kΩ

3.5.4. Oscillator Specifications

V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Frequency	f_{OSC_HF}	HF mode , T_J = 25 °C	47.88	50.0	51.32	MHz
		HF mode, T_J = -40 °C to 85 °C	44.42	50.0	52.8	MHz
	f_{OSC_LF}	LF mode, T_J = 25 °C	2.92	3.0	3.04	MHz
		LF mode, T_J = -40 °C to 85 °C	2.85	3.0	3.18	MHz

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Duty Cycle [1]	$f_{OSC\_DC\_HF}$	HF mode, T_J = -40 °C to 85 °C	36.7	48.0	58.3	%
	$f_{OSC\_DC\_LF}$	LF mode, T_J = -40 °C to 85 °C	38.7	50.0	61.4	%
Initial Setting Time [1]	$T_{OSC\_SET\_HF}$	HF mode , T_J = 25 °C	70	110	160	µs
		HF mode, T_J = -40 °C to 85 °C	60	110	190	µs
	$T_{OSC\_SET\_LF}$	LF mode, T_J = 25 °C	350	390	440	µs
		LF mode, T_J = -40 °C to 85 °C	330	390	470	µs
Period Jitter (Peak-to-Peak) [1]	T_{PJIT_HF}	HF mode , T_J = 25 °C	-	0.14	0.22	ns
		HF mode, T_J = -40 °C to 85 °C	-	0.14	0.24	ns
	T_{PJIT_LF}	LF mode, T_J = 25 °C	-	1.5	2.8	ns
		LF mode, T_J = -40 °C to 85 °C	-	1.5	3.2	ns
Postdivider Ratio Range [2]	$N_{POSTDIV\_RATIO}$	Only multiple of 2 values	1	-	128	-

[1] Guaranteed by characterization, not tested in production.

[2] Guaranteed by design, not tested in production.

3.5.5. LVDS Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Tx						
Die Junction Temperature	T_J		-40	25	85	°C
IO Domain Operating Voltage	V_{DDIO}		1.71	1.8	3.465	V
Core Domain Operating Voltage	V_{DDC}		1.045	1.1	1.155	V
PAD_POS/PAD_NEG Leakage Current	$I_{LEAK\_PAD\_POS}$, $I_{LEAK\_PAD\_NEG}$	TX, RX, BIAS are off, V_{DDIO} = 3.465 V, V_{DDC} = 1.155 V	-	0.01	0.29	µA
Operating Current (V_{DDIO}) for BIAS	$I_{Q\_STATIC\_BIAS\_VDDIO}$	See [3]	-	1.7	-	mA
Operating Current (V_{DDIO}) per Tx Channel	$I_{Q\_STATIC\_TX\_VDDIO}$	Static out state, see [3]	-	3.3	4.9	mA
Differential Output Voltage Range [2]	$\|V_{OD\_RANGE}\|$	Tunable range, at R_T = 100 Ω	170	250	390	mV
Differential Output Voltage Accuracy	$\|V_{OD}\|$	Default $\|V_{OD}\|$ = 250 mV, R_T = 100 Ω	200	250	300	mV
Change in V_{OD} Between Opposite Binary States	dV_{OD}	R_T = 100 Ω	-	-	20	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 Ω	0.9	0.975	1.05	V
Change in V_{OCM} Between Opposite Binary States	dV_{OCM}	R_T = 100 Ω	-	-	20	mV
Output Current of OUTP or OUTN per Tx Channel	I_{SA}, I_{SB}	Output terminals short-circuited to the generator circuit common	-	-	24	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Current Between OUTP and OUTN per Tx Channel	I_{SAB}	Output terminals short-circuited to each other	-	-	12	mA
Maximum Data Rate	D_{MAX}	Data or Clock rate (which is higher), see [4]	100 [5]	-	-	Mbps
Rising/Falling Time [1]	T_{TLH}, T_{THL}	TUI = 10 ns at 100 Mbps (below TUI * 30 % by ANSI) 20 % - 80 %, V_{OD} = 250 mV, R_T = 100 Ω, C_L = 5 pF between PAD_POS and PAD_NEG	0.36	0.44	1.03	ns
Difference Between Propagation Delays (Jitter) [1]	T_{JITTER}	Within same channel, R_T = 100 Ω, C_L = 5 pF at PAD_POS and PAD_NEG	-	261	755	ps
Difference Between Propagation Delays (Skew) [1]	T_{SKEW}	Between pair of channels, R_T = 100 Ω, C_L = 5 pF at PAD_POS and PAD_NEG	-	590	-	ps
Rx						
Die Junction Temperature	T_J		-40	25	85	°C
IO Domain Operating Voltage	V_{DDIO}		1.71	1.8	3.465	V
Core Domain Operating Voltage	V_{DDC}		1.045	1.1	1.155	V
Operating Current (V_{DDIO}) per Rx Channel	$I_{Q\_STATIC\_RX\_VDDIO}$	Static input state, see [3]	-	1	1.62	mA
Differential Input Voltage [1]	$\|V_{ID}\|$		100	-	-	mV
Input Common Mode Voltage [1]	V_{ICM}	VDDIO = 1.71 V	0.65	0.975	1.4	V
Maximum Data Rate	D_{MAX}	Data or Clock rate (which is higher), see [4]	100 [5]	-	-	Mbps

[1] Guaranteed by characterization, not tested in production.

[2] Guaranteed by design, not tested in production.

[3] Please note to include LVDS BIAS current for LVDS TX and RX quiescent current estimation. Examples are shown below:
when enabling N TX channels: Iq_vddio= Iq_static_bias_vddio +Iq_tx_vddio x N,
when enabling N RX channels: Iq_vddio= Iq_static_bias_vddio +Iq_rx_vddio x N.

[4] SDR operation (see Figure 5):
Maximum limits over temperature are guaranteed by characterization.
PAIR 0: CLK for 50 MHz with UI_clk = 10 ns (clk rate = 100 Mbps).
PAIR 1/2: Data with UI_data = 20 ns (data rate = 50 Mbps).
DDR operation (see Figure 6):
Maximum limits over temperature are guaranteed by design.
PAIR 0: CLK for 50 MHz with UI_clk = 10 ns (clk rate = 100 Mbps).
PAIR 1/2: Data with UI_data = 10 ns (data rate = 100 Mbps).

[5] Lowest value of maximum data rate which is guaranteed under worst case operating conditions. For other operating conditions achievable data rate will be higher and mostly limited by user design achievable operating frequency.

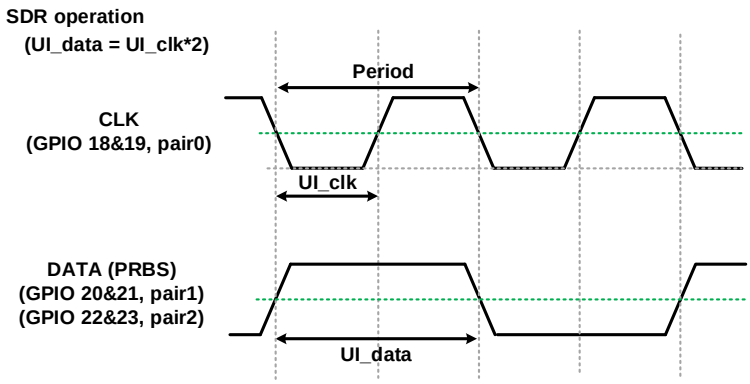


Figure 5. SDR Data and Clock Rates

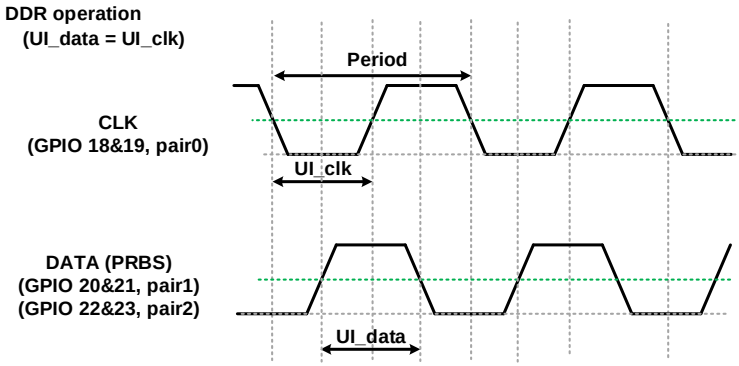


Figure 6. DDR Data and Clock Rates

3.5.6. Power-On Reset Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{DDC} Power-On Reset Delay [1]	$T_{VDDC\_POR\_DELAY}$	V_{DDC} ramp = 300 µs to 10 ms, V_{DDIO} = 2.5 V ± 10 %	1.8	2.15	2.5	ms
V_{DDIO} Power-On Reset Delay [1]	$T_{VDDIO\_POR\_DELAY}$	V_{DDIO} ramp = 300 µs to 10 ms, V_{DDC} = 1.1 V	1.9	2.2	2.54	ms
V_{DDC} Power-On Threshold	$V_{POR\_VDDC\_ON}$	V_{DDIO} = 2.5 V	0.877	0.906	0.955	V
V_{DDC} Power-Off Threshold	$V_{POR\_VDDC\_OFF}$	V_{DDIO} = 2.5 V, other modes	0.323	0.664	0.95	V
		V_{DDIO} = 2.5 V, Configuration mode	0.850	0.87	0.910	V
V_{DDIO} Power-On Threshold	$V_{POR\_VDDIO\_ON}$	V_{DDC} = 1.1 V	1.570	1.634	1.695	V
V_{DDIO} Power-Off Threshold	$V_{POR\_VDDIO\_OFF}$	V_{DDC} = 1.1 V, other modes	0.653	1.093	1.486	V
		V_{DDC} = 1.1 V, Configuration mode	1.390	1.595	1.650	V
V_{DDC}/V_{DDIO} Supply Ramp [2]	T_{POR_VRAMP}	V_{DDC} = 0 V to 1.1 V ± 5 %, V_{DDIO} = 0 V to (1.71 V…3.465 V)	0.3	-	10	ms

[1] Guaranteed by characterization, not tested in production.

[2] Guaranteed by design, not tested in production.

3.5.7. Estimated Current Consumption of Internal Blocks

T_A = 25 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V.

Parameter	Symbol	Conditions	Typ	Unit
V_{DDC} Supply Current Consumption	I_{DDC}	OSC 50 MHz	422	µA
		PLL active (F_{VCO} = 500 MHz)	610	µA
		PLL active (F_{VCO} = 2000 MHz)	2.82	mA
		Single BRAM block quiescent consumption (BRAM_PG = LOW)	5.8	µA
		BRAM block read (RCLK = 50 MHz)	1.53	mA
		BRAM block write (WCLK = 50 MHz)	1.06	mA
		Average consumption during FPGA Core operation with 90+ % utilization at 100 MHz (V_{DDIO} = 1.8 V) [3]	95	mA
[3] Device Utilization is 90+ % of LUTs/FFs in each Slice of CLB; PWR = 1 and EN = 1, BRAM – disabled, F = 100 MHz).				

3.5.8. Timing Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Configuration						
Configuration Time. Time from nRESET(PWR) Asserted HIGH to Device Configuration Ready	t_{CONF_OTP}	OTP Configuration mode	-	9	-	ms
	t_{CONF_MCU}	MCU Configuration mode F_{CLK_SPI} = 16 MHz	-	48	-	ms
	$t_{CONF\_QSPI\_1X}$	QSPI Configuration mode, 1x mode	-	71	-	ms
	$t_{CONF\_QSPI\_2X}$	QSPI Configuration mode, 2x mode	-	36	-	ms
Controller Configuration (Config from QSPI Flash Memory)						
Controller Clock Frequency During Configuration [1]	t_{CLKM}		-	12.5	16.82	MHz
Controller Clock Duty Cycle During Configuration [1]	$CLKM_{DC}$		29.8	50.0	76.1	%
Delay from nRESET(PWR) Rising Edge to SPI_CSn Falling Edge	t_{POR_MCLK}		-	192	-	µs
Data In Setup Time before Clock Rising Edge [1]	$t_{M\_DI\_SU}$		10	-	-	ns
Data In Hold Time after Clock Rising Edge [1]	$t_{M\_DI\_HD}$		10	-	-	ns
SPI_CSn Setup Time before Clock Falling Edge [1]	$t_{M\_CSN\_SU}$		74	-	-	ns
SPI_CSn Hold Time after Clock Rising Edge [1]	$t_{M\_CSN\_HD}$		6	-	-	ns
Clock Rising Faling Edge to Valid Output Delay [1]	$T_{M\_CLK\_VOD}$		0	-	-	ns
SPI_CSn High Time after Wake Up Command before Sending Next SPI FLASH Command [1]	$T_{M\_CSN\_WKUP\_H}$		290	-	-	µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Target Configuration (Config from MCU)						
Max Target Clock Frequency [1]	f_{CLKS_MAX}		-	-	16	MHz
Data In Setup Time before Clock Rising Edge [1]	$t_{S\_DI\_SU}$		0	-	-	ns
Data In Hold Time after Clock Rising Edge [1]	$t_{S\_DI\_HD}$		10	-	-	ns
Min Clock Pulse HIGH [1]	T_{S_CLKH}		10	-	-	ns
Min Clock Pulse LOW [1]	T_{S_CLKL}		10	-	-	ns
SPI_CSn Setup Time before Clock Falling Edge [1]	$T_{S\_CSN\_SU}$		0	-	-	ns
SPI_CSn Hold Time after Clock Rising Edge [1]	$T_{S\_CSN\_HD}$		10	-	-	ns
SPI_CSn High Time (between SyncWord and Bitstream) [1]	$T_{S\_CSN\_H}$		0	-	-	µs
Fast Route						
Fast Route Pin-to-Pin Propagation Delay [2]	T_{FR_PROP}	Between GPIOs in different IO Banks, V_{DDIO} = 1.71 V to 3.465 V	5.9	-	16.2	ns
Fast Route Paths Skew [2]	T_{FR_SKEW}	Between different GPIOs, V_{DDIO} = 1.71 V to 3.465 V	2.9	-	8.3	ns
Programmable Delays						
Differential Input Clock to DDR DFFs Delay (Max Value) [2]	$T_{DLY\_DIFF\_IN\_CLK\_DDR\_MAX}$	V_{DDIO} = 1.71 V to 3.465 V	7.7	11.4	22	ns
Differential Output Clock Delay (Max Value) [2]	$T_{DLY\_DIFF\_OUT\_MAX}$	V_{DDIO} = 1.71 V to 3.465 V	7.9	11.7	22.6	ns
Serial Data Paths Delay (Max Value) [2]	$T_{DLY\_SER\_DATA\_MAX}$	V_{DDIO} = 1.71 V to 3.465 V	7.8	11.5	22.4	ns

[1] Guaranteed by characterization, not tested in production.

[2] Guaranteed by design, not tested in production. Conditions: Max – V_{DDC} = 0.99 V, V_{DDIO} = 1.62 V, SS corner, -40 °C; Typ – V_{DDC} = 1.1 V, V_{DDIO} = 3.3 V, TT corner, 25 °C; Min – V_{DDC} = 1.21 V, V_{DDIO} = 3.6 V, FF corner, 85 °C.

3.5.9. Supply Current

T_A = -40 °C to +85 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{DDC} Power Supply Current, Device in Sleep Mode	I_{DDC_RET}	nRESET(PWR) = 1, nSLEEP(EN) = 0, BRAM_PG = HIGH (power gated [1])	-	77	2950	µA
V_{DDC} Power Supply Current, Device in Sleep Mode with BRAM Retained	$I_{DDC\_RET\_BRAM}$	nRESET(PWR) = 1, nSLEEP(EN) = 0, BRAM_PG = LOW (data retained [2])	-	84	3200	µA
V_{DDC} Power Supply Current, Device in Functional Mode	$I_{DDC\_FUNC\_STAT}$	nRESET(PWR) = 1, nSLEEP(EN) = 1, BRAM_PG = HIGH (power gated [1]), FPGA core in static state	-	118	3500	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{DDC} Power Supply Current, Device in Reset State	I_{DDC_RST}	nRESET(PWR) =0, nSLEEP(EN) = do not care, BRAM_PG = HIGH (power gated [1])	-	77	2950	µA
V_{DDIO} Power Supply Current, Device in Reset State	I_{DDIO_RST}	nRESET(PWR) =0, nSLEEP(EN) = do not care, GPIOs are retained = HIGH [3]	-	0.8	6	µA
V_{DDC} Power Supply Peak Current During Start-Up and Configuration [4]	I_{DDC_PEAK}	During first power on or during exit from Reset Mode, V_{DDIO} = 3.465 V, V_{DDC} = 1.155 V	-	10	20	mA
V_{DDIO} Power Supply Peak Current During Start-Up and Configuration [4]	I_{DDIO_PEAK}	During first power on or during exit from Reset Mode , V_{DDIO} = 3.465 V, V_{DDC} = 1.155 V	-	0.4	6.5	mA

[1] Stands for ***BRAM Power*** = "***Disable***" SW option of BRAM.

[2] Stands for ***BRAM Power*** = "***Enable***" SW option of BRAM.

[3] Stands for ***GPIO Keep*** = "***Enable***" SW option.

[4] Guaranteed by characterization, not tested in production.

3.5.10. BRAM Characteristics

T_A = -40 °C to +85 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Read Max Frequency [1]	f_{RD_MAX}		-	-	83.6	MHz
Read Max Frequency	$f_{RD\_MAX\_25}$	T = 25 °C	-	168	-	MHz
Write Max Frequency [1]	f_{WR_MAX}		-	-	45.8	MHz
Write Max Frequency	$f_{WR\_MAX\_25}$	T = 25 °C	-	167	-	MHz

[1] Guaranteed by characterization, not tested in production.

3.5.11. nRST (PWR) and nSLEEP (EN) Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 2.5 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
nRST(PWR) = (HIGH to LOW) Transition to GPO Retention (or Hi-Z) State Delay [3] [10]	$T_{NRST\_GPO\_RST\_RET\_DLY}$	When OSC_EN = 1 in Functional mode [1] [2]	-	2.1	-	µs
nRST(PWR) = (LOW to HIGH) Transition to Power-On State (Start of Configuration) Delay [9]	T_{NRST_EX}		-	190	270.1	µs
nRST(PWR) = (HIGH to LOW) Transition to Getting in Reset Mode Delay [4] [9]	T_{NRST_ENT}		500	-	-	µs
nSLEEP(EN) = (HIGH to LOW) Transition to GPO Retention State Delay [5] [9]	$T_{NSLEEP\_GPO\_RET\_DLY}$	OSC_EN=1 in Functional mode [1] [2]	-	140	265	ns
nSLEEP(EN) = (LOW to HIGH) Transition to Functional State [9]	T_{NSLEEP_EX}		-	245	327	µs
nSLEEP(EN) = (HIGH to LOW) Transition to Getting into Retention State Delay [6] [7] [10]	T_{NSLEEP_ENT}		500	-	-	µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Max Delay for User Clocks to be Stopped before Transition to Sleep or Reset [10]	$T_{USR\_CLK\_STOP\_MAX\_DLY}$		-	6	-	µs

[1] In case if in Functional mode OSC_EN = 0 – these parameters should be increased by $T_{OSC\_SET\_HF}$.

[2] In case if user uses slow external clock or Logic-as-Clock – these times would be increased by 2 periods of slowest clock up to $T_{USR\_CLK\_STOP\_MAX\_DLY}$ (after that delay all user clocks would be forced to LOW anyway).

[3] Same is for IOB int_rst = HIGH.

[4] During this time nRST(PWR) should be held LOW.

[5] Same is for IOB sleep_start = HIGH.

[6] During this time nSLEEP(EN) should be held LOW.

[7] Same timing should be used between IOB sleep_start rising edge (start enter to Sleep) and nSLEEP(EN) rising edge (initiates exit from Sleep).

[8] Parameters for figures in section 7.3 Power-up and Configuration Sequence:

$$T_{NSLEEP\_CYC} \text{ (nSLEEP(EN) pin cycle time)} = T_{NSLEEP\_ENT} + T_{NSLEEP\_EX}$$

$$T_{NRST\_CYC} \text{ (nRST(PWR) cycle time)} = T_{NRST\_ENT} + T_{NRST\_EX}$$

[9] Guaranteed by characterization, not tested in production.

[10] Guaranteed by design, not tested in production.

4. General Purpose Input Output (GPIO) Buffers

4.1 CMOS GPIO with Configurable Drive Strength

The SLG47920/SLG47921 includes CMOS digital GPIO pins. The GPIO structure is shown in Figure 7.

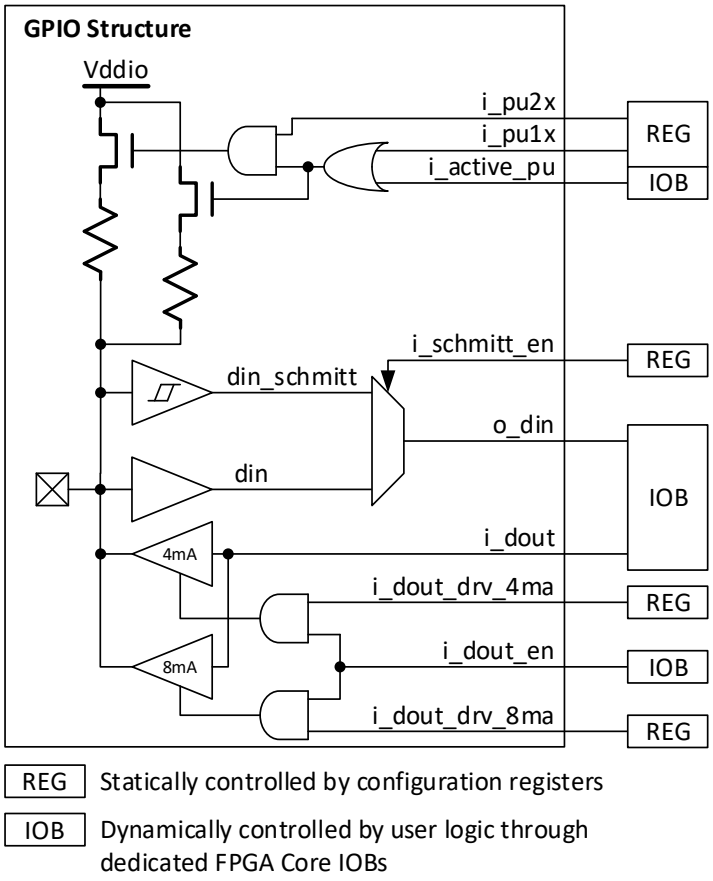


Figure 7. GPIO Buffers

The SLG47920 has 40 pins with 26 are normal CMOS GPIO pins and 6 pins have LVDS capability (3 pairs, see section 4.2 GPIO with LVDS Capability). While SLG47921 has 48 pins with 34 are normal CMOS GPIO pins and 6 pins have LVDS (3 pairs) capability. The remaining pins are V_{DDC}, V_{DDIO0}, V_{DDIO1}, V_{SSC}, V_{SSIO0}, V_{SSIO1}, and input-only pins for nSLEEP(EN) and nRST(PWR).

The following Configuration options are available for each of 26 (or 34) normal CMOS GPIO pin:

- Input (selected by ***Input Mode*** (Note 1) parameter in SW)
  - Simple Input
  - Input with Schmitt-trigger
- Push-pull output with different drive strength (selected by ***Drive Strength Select***)
  - 4 mA
  - 8 mA
  - 12 mA
- Pull-up options (Note 2) (selected by ***Pull Up Enable***)
  - No Pull-up/1x Active Pull-up
  - 1x Pull-up
  - 2x Pull-up

- 2x Active Pull-up.

Note 1: SW controllable option names are referred in text in ***Bold Italic*** font and its respective value is referred with ***"Bold Italic font in quotes"***.

Note 2: For pull-up values see section 3.5.3 GPIO Pull-up Resistance Specifications.

IOB Controls

FPGA Core Input-Output Blocks (IOB, see section 5.2 FPGA Core Composition) allow dynamically control following behavior of GPIOs: Output Data, Output Enable, Active Pull-up. Other parameters are statically defined by bitstream.

Active Pull-up

When pull-up is controller from IOBs of FPGA Core – such mode is called **Active Pull-up**. Using dedicated IOBs allows turn on/off pull-up during operation. 1x **Active Pull-up** can be activated even if in GPIO configuration it is set to No Pull-up. To get 2x **Active Pull-up** – it requires to select this mode in ***Pull Up Enable***.

Configuration Mode Pull-up

This feature allows user to enable pull-up before the device enters **Functional Mode** (includes **Reset Mode** and **Configuration Mode**). For details see section 4.5 Typical IO Behavior During Power-up.

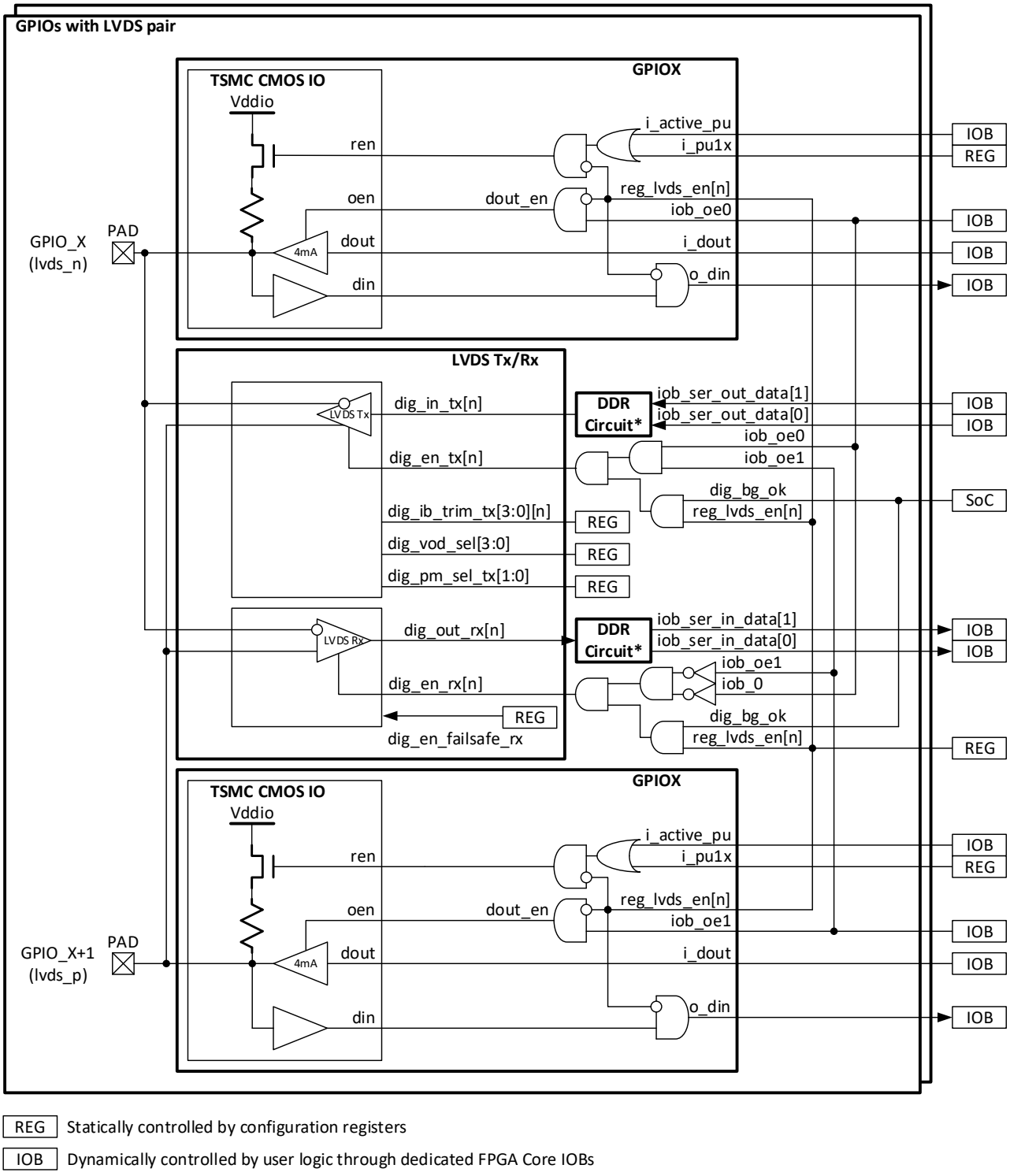
Fail-Safe Input

CMOS GPIOs with Configurable Drive Strength have Fail-Safe input, which means that even when lower V_{DDIO} is used – the input still can be safely fed by input voltage up to maximum operating voltage 3.465 V.

4.2 GPIO with LVDS Capability

GPIO with LVDS capability is composed of a CMOS IO structure with 4mA drive strength and LVDS Tx/Rx cells. Since LVDS is differential and requires two lines, a pair of GPIOs are connected to the same LVDS Tx/Rx.

The structure for the pair of GPIO with LVDS capability is shown in Figure 8.



REG Statically controlled by configuration registers

IOB Dynamically controlled by user logic through dedicated FPGA Core IOBs

Figure 8. GPIOs Pair with LVDS Capability

Each pair of GPIOs can be used as two independent CMOS GPIOs or can be used as a single LVDS differential line transceiver.

The following Configuration options are available for each CMOS GPIO pin:

- Input
  - Simple CMOS input
- Push-pull output with single drive strength
  - 4 mA.

Also, two pull-up options are available (selected by ***Pull Up Enable***):

- No pull-up
- 1x Pull-up.

For GPIO pairs in LVDS mode (selected by ***Enable*** option of LVDS Pair element in SW), the following configurations are available:

- LVDS Tx (selected by ***Tx Vod Selection***)
  - Selectable V_{OD}: 250 mV (typ), tunable range up to 390 mV
- LVDS Rx (fail-safe input) (selected by ***Rx Fail Safe Enable***).

Figure 9 shows LVDS signal levels.

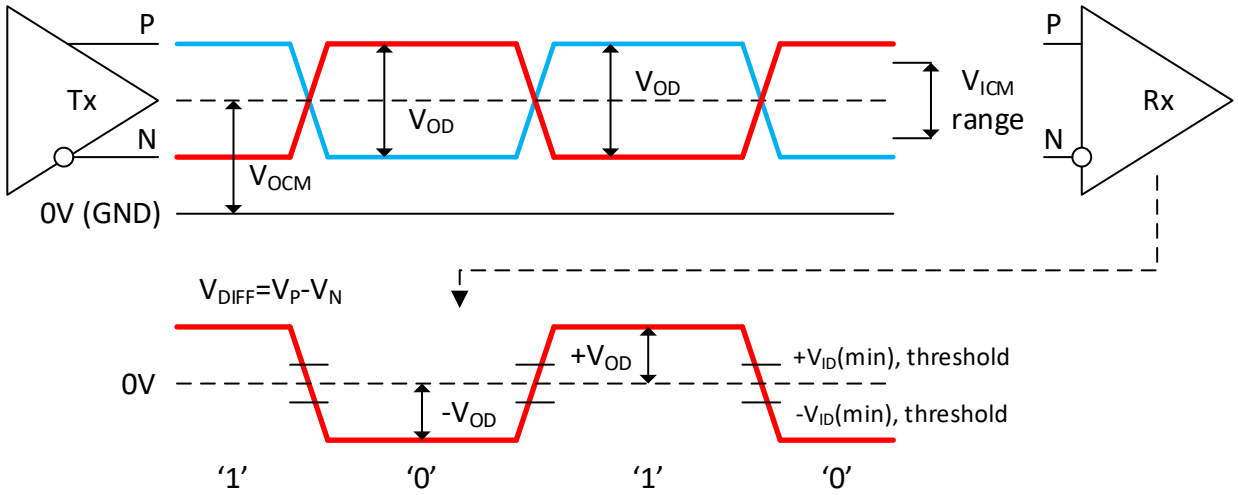


Figure 9. LVDS Signal Levels

IOB Controls

FPGA Core Input-Output Blocks (IOB, see section 5.2 FPGA Core Composition) allow dynamically control following behavior of:

- CMOS GPIO mode
  - Output enable
  - Output data
  - Active Pull-up
- LVDS mode
  - LVDS Tx/Rx Enable
  - Output Serial Data.

Other parameters are statically defined by bitstream.

LVDS Direction Controls

Whenever LVDS mode is enabled the CMOS IO structure will force OE into a disabled state. LVDS Tx/Rx enable will take into account controls of both GPIOs used as an LVDS pair.

GPIOs in LVDS mode allow bi-directional operation. However, there is setup time required to switch between Tx and Rx:

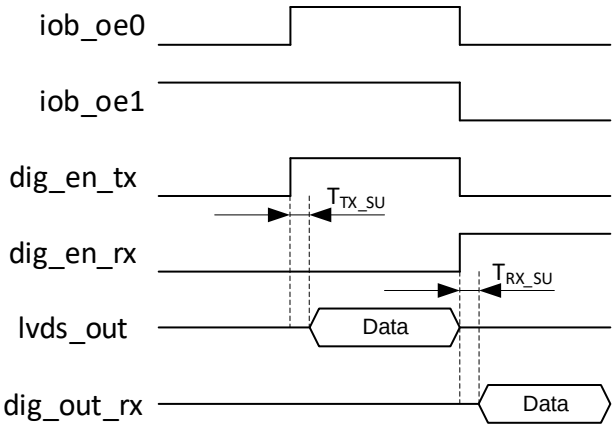


Figure 10. LVDS Bi-Directional Operation

T_{TX_SU} = T_{RX_SU} = 200 ns (worst case).

DDR Circuitry

Data to/from LVDS Tx/Rx is not connected directly to the FPGA Core IOBs, but instead first goes through a DDR circuit which enables data to:

- Transit this circuit without change
- Be latched by DDR DFFs.

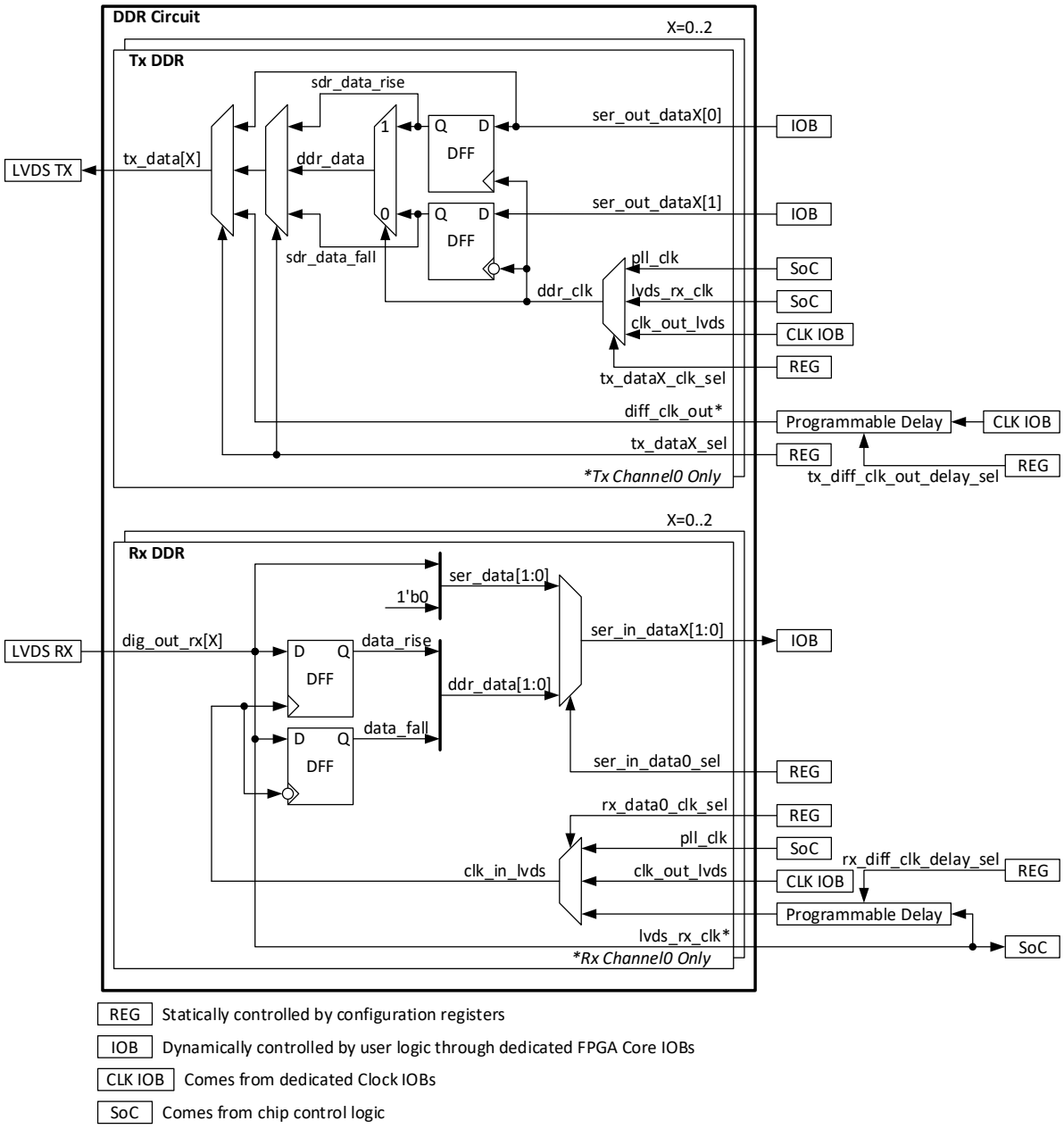


Figure 11. DDR Circuit

Tx DDR Circuit allows Tx LVDS to support the following types of data (selected with ***Tx Data Selection***):

- Serial Data
- DDR Data (latched at both edges of clock)
- SDR Data (latched at either edge of the clock)
- Differential Clock (only for LVDS channel 0).

SDR/DDR data can be clocked by the following (selected with ***Tx Clk Selection***):

- PLL0 clock (Fout0/Fout1)
- Received differential clock (LVDS Rx channel 0)
- Differential LVDS clock from FPGA Core.

The differential LVDS clock from the FPGA Core goes through a programmable delay, which provides delay from 0 ns to 10 ns (selected with ***Tx Diff Clk Out Delay***). This is used to be able to shift the clock edge relative to the data.

Rx DDR Circuit processes data from Rx LVDS as follows (selected with ***Rx Data Selection***):

- Serial Data (no processing)
- DDR Data (latched at both edges of clock) (Note).

Note: As serial data is output as two bits, the DDR DFF out bits can be used separately as SDR DFF latched on its respective edge.

DDR data can be clocked by (selected with ***Rx Clk Selection***):

- PLL0 clock
- Received differential clock (LVDS Rx channel 0)
- Differential LVDS clock from FPGA Core.

Received differential clock (LVDS Rx channel 0) goes through a programmable delay, which provides delay from 0 ps to 10 ns (selected with ***Rx Diff Clk Delay***). This is used to be able to shift the clock edge relative to the data.

LVDS BIAS Circuit is required to provide reference voltages for LVDS Tx/Rx.

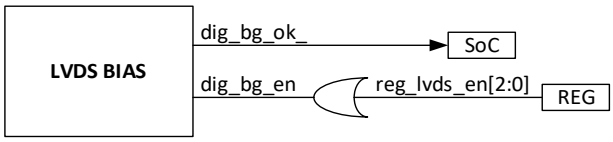


Figure 12. LVDS Bias Circuit

It is automatically enabled whenever any of the LVDS Tx/Rx are enabled.

4.3 GPIO Paths to/from the FPGA Core

The input path (GPI) from PAD to FPGA Core has a gating mechanism (with an AND gate), which is only used by SoC logic in the SLG47920/SLG47921.

This gating mechanism is used in Functional mode to reduce noise and power consumption of unused GPIOs or when a GPIO is used only as output. Gating is possible when the dedicated option (***Input Data Gating***) is set in SW.

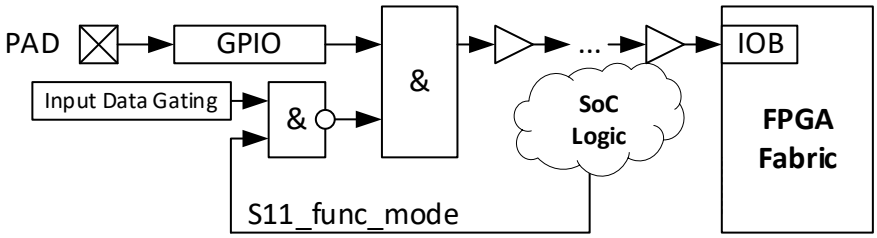


Figure 13. Input Path Optional Gating

This results in not toggling buffer-chain after AND gate when the input signal is not used, which in turn leads to reduced power consumption and reduced noise on internal power lines.

The output path (GPO) from the FPGA Core to the PAD will use a Retention Ring to keep output values when the SLG47920/SLG47921 transits into either **Sleep mode** or **Reset mode**.

4.4 Fast Routing between V_{DDIO} Banks

Fast Routing paths exist between pairs of GPIOs located in different IO Banks (IO Bank 0 → IO bank 1 or IO Bank 1 → IO bank 0). It is activated with ***Fast Route Path*** option in SW.

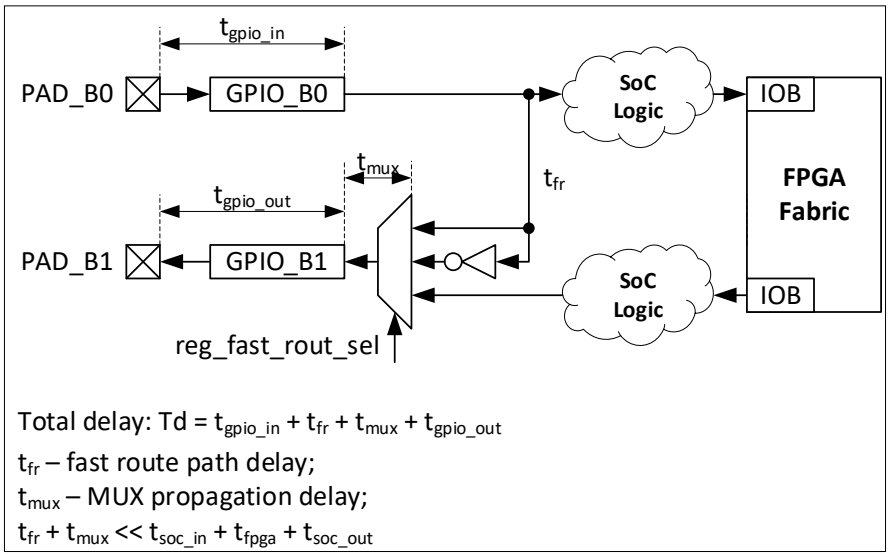


Figure 14. Fast Routing

This allows a fast level conversion (much faster than using a path through the SoC logic and FPGA Core). Delay and skew of fast-route paths can be found in section 3.5.8 Timing Specifications.

The input path to the FPGA Core is not gated in case of fast route usage (to be able to logically process the same signal).

There are two options for fast route paths: non-inverted and inverted (selected with ***Fast Route Path Invertor***).

To minimize delay skew between different pairs of GPIO, correct routing topology and path balancing is implemented.

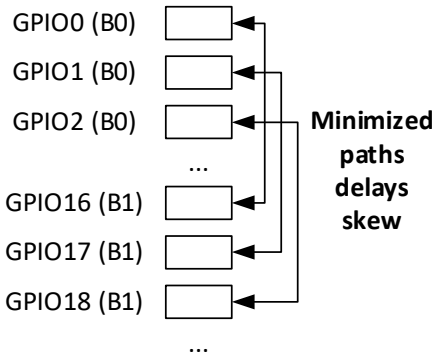


Figure 15. GPIOs Fast Routs Routing Topology

In Table 6 are the GPIO pairs that have Fast Route enabled and their delays. This information might be useful to select paths with acceptable skew, as different paths delays are not matched exactly. Total worst skew between all path is much worse than skew between individual paths (especially adjacent), so correct selection of Fast Route paths might significantly minimize final skew between fast-routed signals.

Table 6. Fast Routes GPIO Pairs and Timings

GPIO in IO Bank0	GPIO in IO Bank1	Direction	Delay			Unit
			Min [1]	Typ [1]	Max [1]	
GPIO0	GPIO16	Bank 0 → Bank 1	4.2	6.1	10.4	ns
		Bank 1 → Bank 0	5.3	7.8	12.9	
GPIO1	GPIO17	Bank 0 → Bank 1	3.1	4.5	8.1	
		Bank 1 → Bank 0	4.7	6.9	11.7	
GPIO2	GPIO18	Bank 0 → Bank 1	6.0	8.9	16.3	
		Bank 1 → Bank 0	4.8	7.2	11.6	
GPIO3	GPIO19	Bank 0 → Bank 1	4.7	7.0	11.8	
		Bank 1 → Bank 0	3.2	4.6	7.9	
GPIO4	GPIO20	Bank 0 → Bank 1	4.8	6.8	11.5	
		Bank 1 → Bank 0	5.1	7.5	12.3	
GPIO5	GPIO21	Bank 0 → Bank 1	5.1	7.5	12.8	
		Bank 1 → Bank 0	4.6	6.6	10.9	
GPIO6	GPIO22	Bank 0 → Bank 1	5.5	8.0	13.1	
		Bank 1 → Bank 0	5.3	7.7	12.4	
GPIO7	GPIO23	Bank 0 → Bank 1	5.2	7.5	12.5	
		Bank 1 → Bank 0	5.1	7.5	12.4	
GPIO8	GPIO24	Bank 0 → Bank 1	4.5	6.6	11.4	
		Bank 1 → Bank 0	4.1	6.0	10.0	
GPIO9	GPIO25	Bank 0 → Bank 1	4.3	6.3	10.9	
		Bank 1 → Bank 0	4.0	5.8	9.7	
GPIO10	GPIO26	Bank 0 → Bank 1	3.6	5.2	9.1	
		Bank 1 → Bank 0	4.1	6.0	10.1	
GPIO11	GPIO27	Bank 0 → Bank 1	3.5	5.0	8.8	
		Bank 1 → Bank 0	4.1	5.9	10.1	
GPIO12	GPIO28	Bank 0 → Bank 1	3.5	5.1	9.0	
		Bank 1 → Bank 0	4.3	6.4	11.6	
GPIO13	GPIO29	Bank 0 → Bank 1	3.3	4.8	8.5	
		Bank 1 → Bank 0	3.6	5.3	9.4	
GPIO14	GPIO30	Bank 0 → Bank 1	4.3	6.4	11.0	
		Bank 1 → Bank 0	4.2	6.1	10.6	
GPIO15	GPIO31	Bank 0 → Bank 1	4.1	5.7	10.0	
		Bank 1 → Bank 0	5.0	7.3	12.2	

[1] Max: V_{DDC} = 0.99 V, V_{DDIO} = 1.62 V, SS process corner, T = -40 °C; Typ: V_{DDC} = 1.1 V, V_{DDIO} = 3.3 V, TT process corner, T = 25 °C; Min: V_{DDC} = 1.21 V, V_{DDIO} = 3.6 V, FF process corner, T = +85 °C.

Note: GPIO32-GPIO39 do not have Fast route paths.

4.5 Typical IO Behavior During Power-up

Upon reaching the defined levels of V_{DDC} and V_{DDIO} in section 3.5.6 Power-On Reset Specifications, the internal power-on-reset (POR) signal is deactivated, and the FPGA core logic is enabled. To ensure the proper functionality of the critical IO banks in your application, it is essential to have all V_{DDIO} banks active with valid input logic levels. By default, the IO pins are tri-stated V_{DDIO} before configuration. This state persists until V_{DDC} and V_{DDIO} reach the defined levels. After the POR signal is deactivated optional pull-ups for **Configuration Mode** can be activated with dedicated SW option ***CONFIG Pull Up Enable***. After configuration read is completed, the IO pins adopt the user-configured settings in the software.

4.6 Supported Standards

The SLG47920/SLG47921 ForgeFPGA GPIO buffer supports single-ended input/output standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). Table 7 shows the IO standards (together with their supply and reference voltages) supported by the SLG47920/SLG47921 ForgeFPGA device.

Table 7. Supported Input/Output Standards

Input/Output Standards	V_{DDIO} (Typ)
Single-ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V
Differential Interfaces	
LVDS33	3.3 V
LVDS25	2.5 V
LVDS18	1.8 V

5. FPGA Core

The SLG47920/SLG47921 includes a FPGA Core, configurable through the ForgeFPGA Workshop software. The FPGA Core allows a user to incorporate in-depth digital functionality into their device such as interface protocols, large-scale glue logic, sensor processing, and other custom functions. The FPGA Core can be configured using pre-designed digital macrocells, Verilog code, or a combination of both.

The FPGA Core interface contains dedicated connections to high-frequency CMOS Digital GPIO (DGPIO), the Oscillator, Oscillator Post Divider, Phase-locked loops (PLLs), BRAMs, LVDS+DDR Circuitry, and configurable IO to the FPGA matrix. A simplified block diagram is shown in Figure 16.

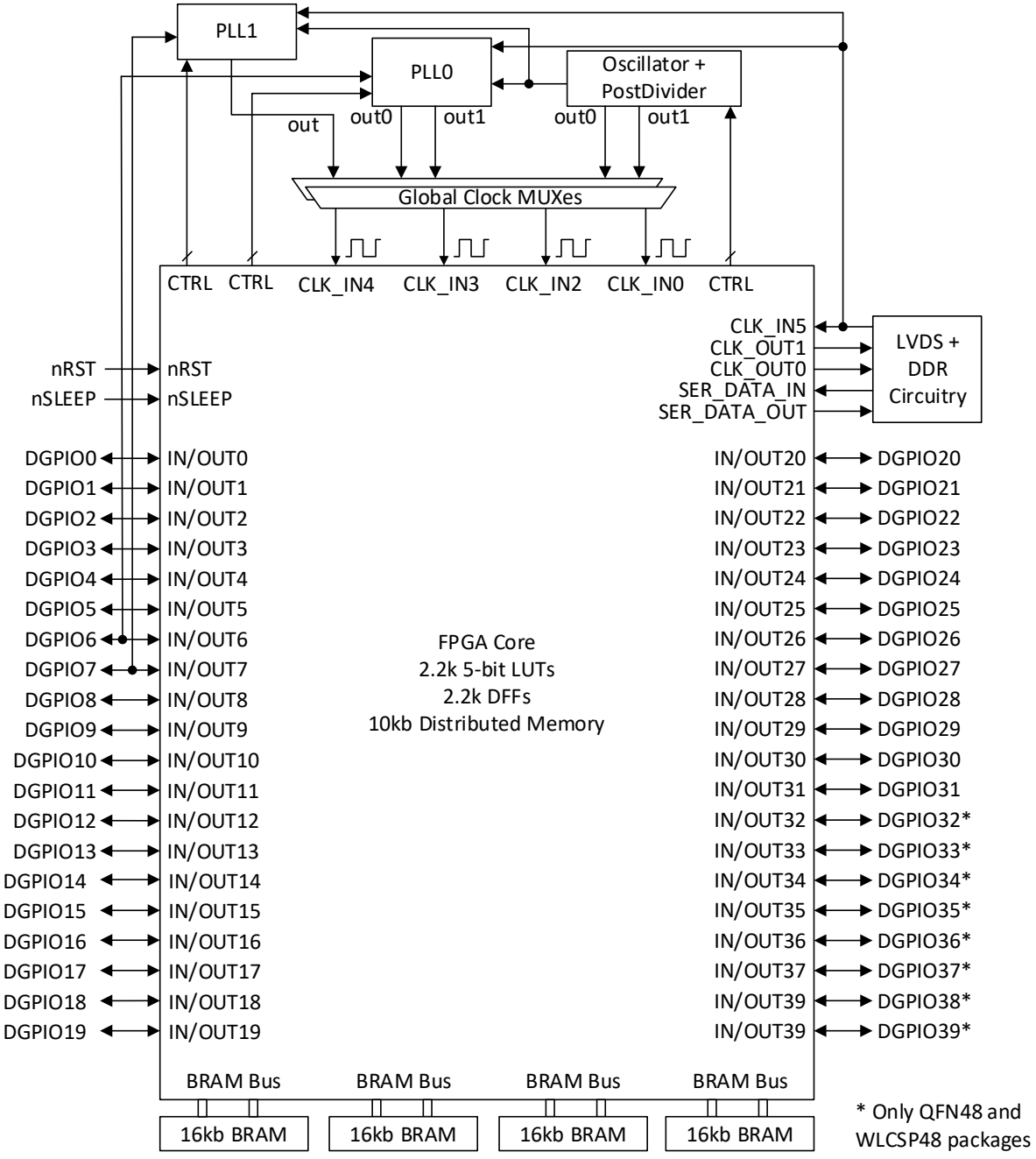


Figure 16. Peripheral Connections to FPGA Core

5.1 Introduction

The FPGA Core is comprised of two tiles adjacent to each other. Each tile is composed of a hierarchy of regular digital logic elements. At the lowest level, 5-bit Look-up Tables (LUTs) are used to support logic elements that can have a user-selectable output based on the five input signals and one output signal. The 5-bit LUTs are arranged two in a pair (with shared inputs), yielding a 6-bit LUT with single output. Each 2x5-bit LUTs has a correspondent pair of D Flip-Flops with selectable input data. Four of these structures (2x5-bit LUT + 2xDFF) are grouped together to form a “Configurable Logic Block” or CLB (see section 5.3 Configurable Logic Blocks), which also includes eight D Flip-Flops.

There is a total of 280 CLBs that make up the FPGA Core, including two different CLB types, Configurable Logic Blocks for Logic (CLBLs) and Configurable Logic Blocks for Memory (CLBMs). The array of CLBs is surrounded by a ring of IO Buffers (IOBs), which serve to make the signal connections to resources outside the device and between tiles.

There are 2240 5-bit LUTs and 2240 DFFs in total in the SLG47920/SLG47921 FPGA Core.

5.2 FPGA Core Composition

Each tile of the FPGA Core is composed of 140 total CLBs, of which 100 are Configurable Logic Blocks for Logic (CLBLs) and 40 are Configurable Logic Blocks for Memory (CLBMs). These result in 1120 x LUT5, 1120 x DFF, 140 4-bit carry chain circuits, and optionally 40x Shift RG or 5kbit distributed memory per tile. Also, each tile has 386 IO Blocks (IOBs), which include 2 inputs and 2 outputs for each. Each input/output can also optionally utilize DFFs.

Clocks are fed to each tile through dedicated clock IOBs. Each tile has only two global clock networks, thus can not utilize more than two different clocks at a time. Clock outputs can be utilized to provide the clock from global clock networks to external circuits.

The Figure 17 below shows the manner that CLBs are tiled across the FPGA Core in each tile and how two tiles are arranged into FPGA Core.

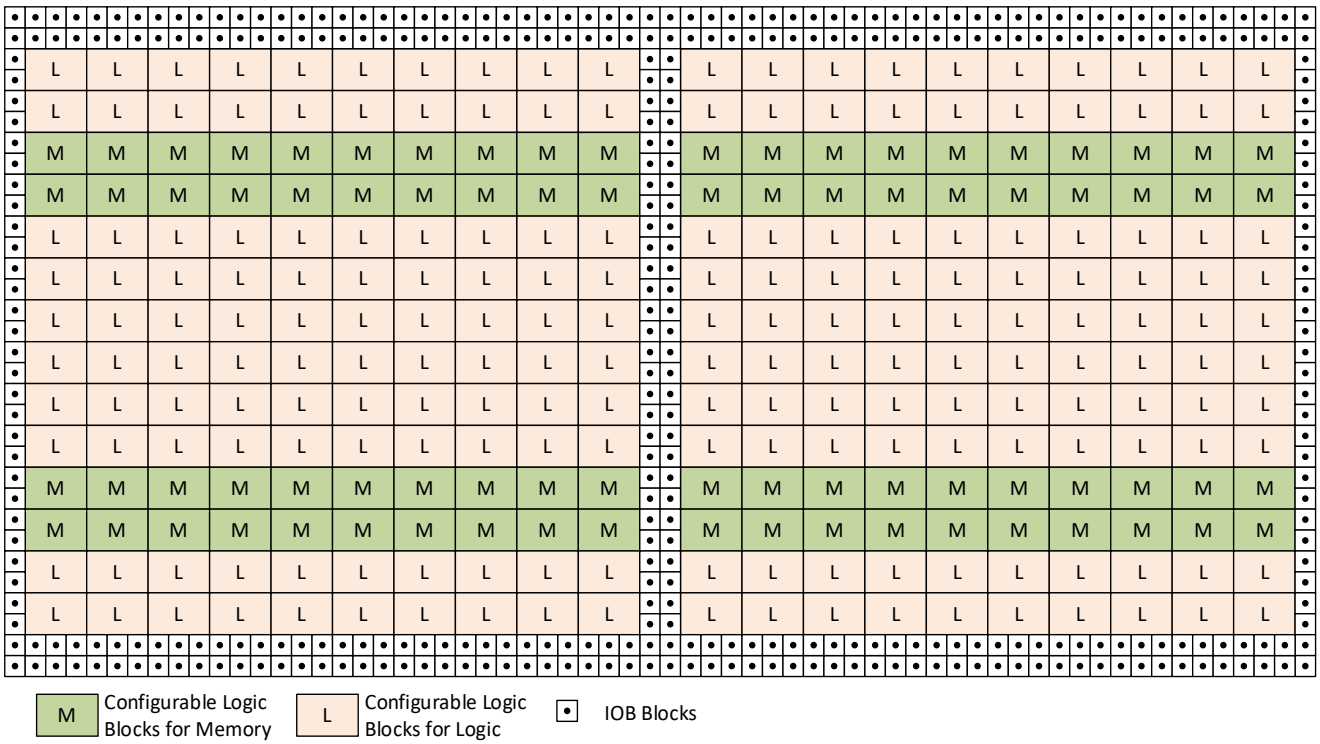


Figure 17. FPGA Core

5.3 Configurable Logic Blocks

The Configurable Logic Block (CLB) is composed of four 6-input/2-output LUTs and eight D Flip-flops. The four 6-Bit LUTs and 4-bit carry chains are grouped in this manner inside the CLBs to support efficient carry arithmetic and implementation of N-bit counters/adders. The further inclusion of the D Flip-Flops in the CLBs support high efficiency and LOW latency mapping of user defined functions. At the output of each CLB there is a cross-point switch to enable the flexible routing of signals going into the interconnect Core. Configurable Logic Blocks for Logic (CLBL) are a subset of Configurable Logic Blocks for Memory (CLBM), with the difference between which is that the CLBM type also includes two additional operating modes, Embedded Memory Mode (EMM) and Shift Register Mode (SRM). These two modes are described in detail in section 5.3.2 Configurable Logic Blocks for Memory.

5.3.1. Configurable Logic Blocks for Logic

The diagram in Figure 18 shows the external connectivity for the Configurable Logic Blocks for Logic, including all the external control signals that are supported. Figure 19 also includes details on internal logic and signal multiplexing within the CLB.

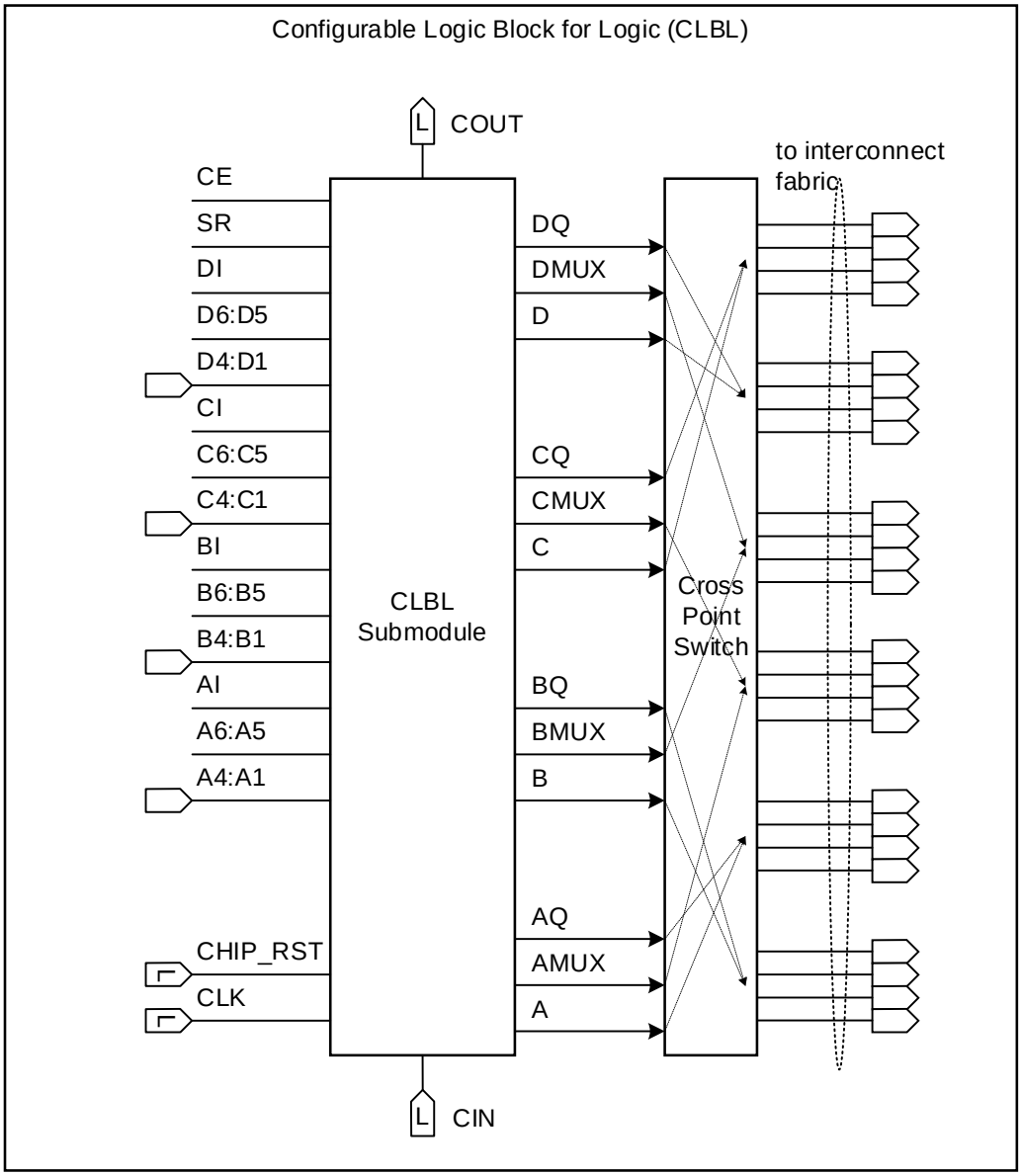


Figure 18. Configurable Logic Blocks for Logic

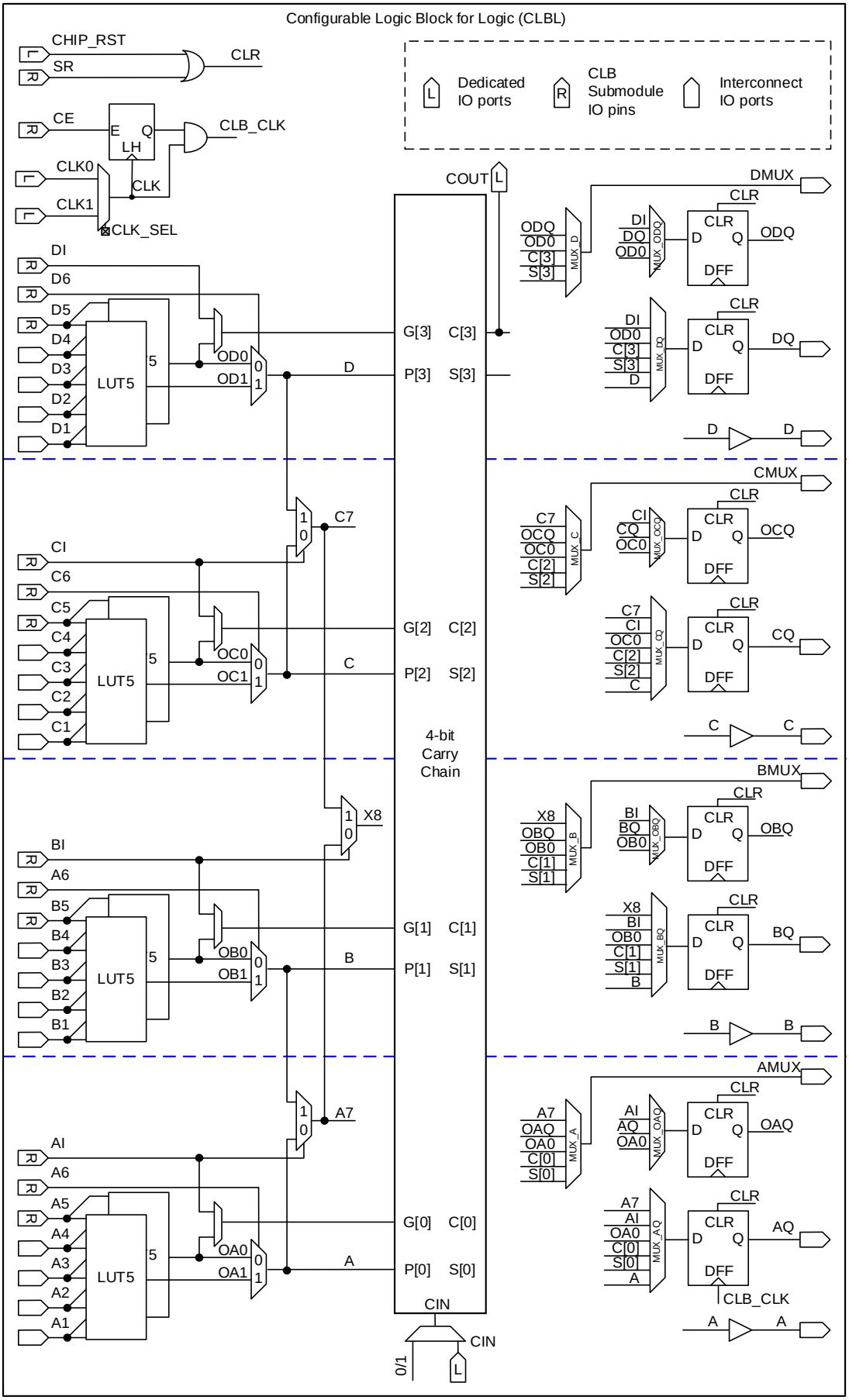


Figure 19. Configurable Logic Blocks for Logic (Cont.)

5.3.2. Configurable Logic Blocks for Memory

The diagram in Figure 20 shows the external connectivity for the Configurable Logic Blocks for Memory (CLBM), including all of the external control signals that are supported. Figure 21 includes details on the internal logic and signal multiplexing within the CLBM when used in one of three different configurations of the Shift Register Mode (SRM). Figure 22 shows internal logic and signal multiplexing within the CLBM when used in one of three different configurations of the Embedded Memory Mode (EMM).

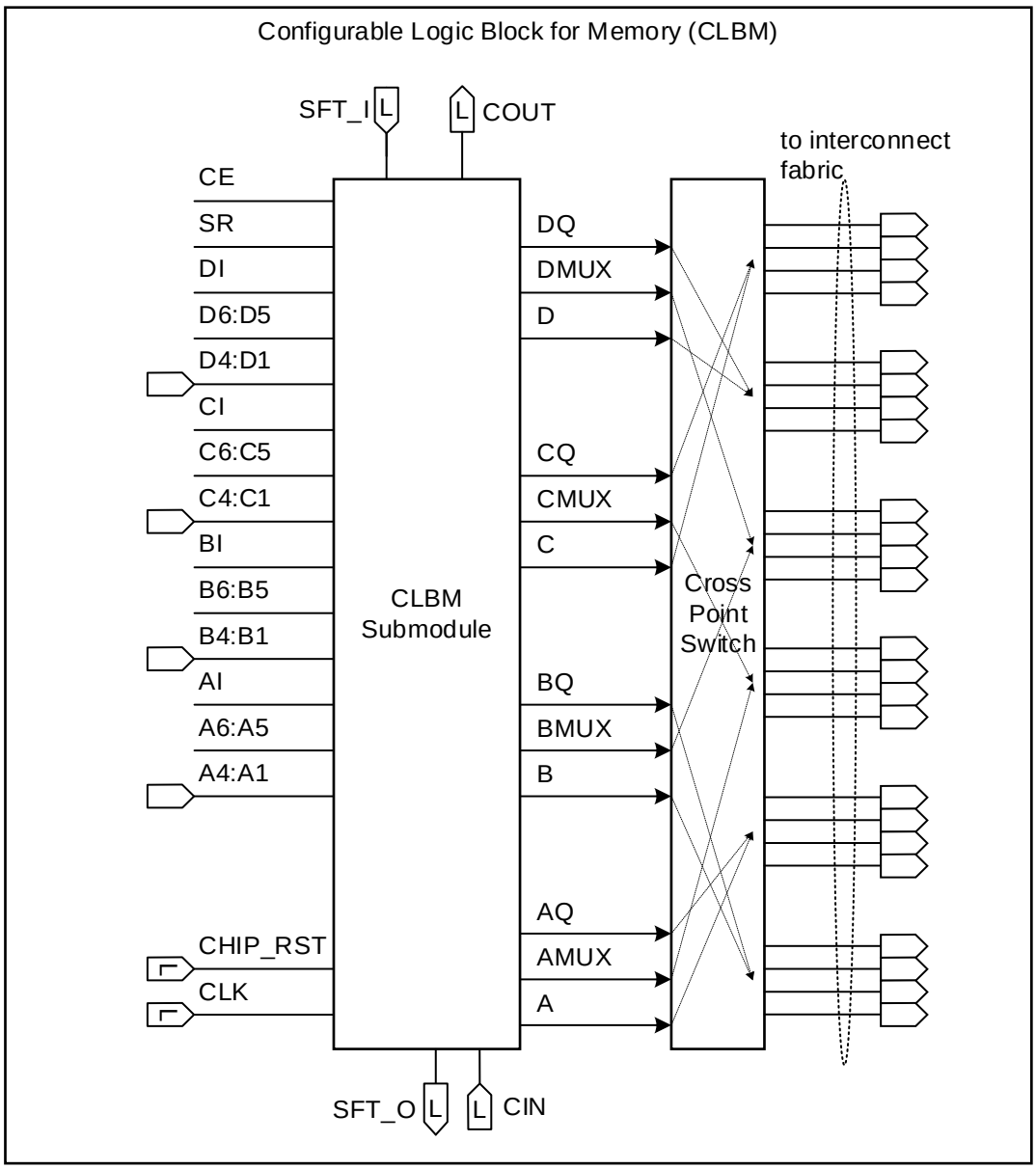


Figure 20. Configurable Logic Blocks for Memory

5.3.2.1. Configurable Logic Block for Memory Used in Shift Register Mode

When using the Configurable Logic Blocks for Memory in Shift Register Mode (SRM), there is a selectable choice in terms of the width of the shift registers that are implemented. The three choices are to have four independent 16-bit shift registers (SRL16E), two independent 32-bit shift registers (SRL32E) or one independent 64-bit shift register (SRL64E). This configuration is a part of the internal 5 kb distributed memory.

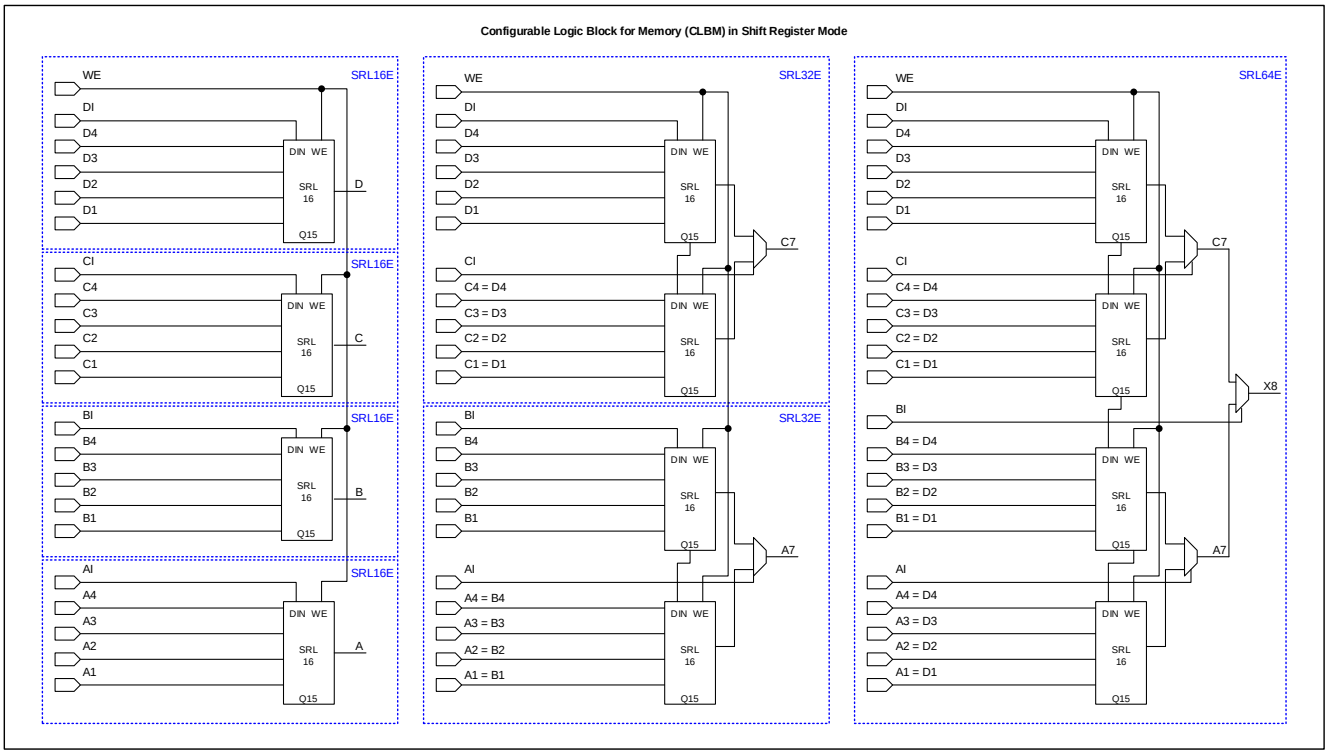


Figure 21. Configurable Logic Blocks for Memory Used in Shift Register Mode

5.3.2.2. Configurable Logic Blocks for Memory used in Embedded Memory Mode

When using the Configurable Logic Blocks for Memory in Embedded Memory Mode (EMM), there is a selectable choice in terms of the width and depth of the memory elements that are implemented. The three choices are to have four independent 32 x 1-bit memory arrays, two independent 64 x 1-bit memory arrays, or one independent 128 x 1-bit memory array that can be used in single or dual-port configuration (applicable only to 32 and 64-bit memory array). This configuration is a part of the internal 5 kb distributed memory.

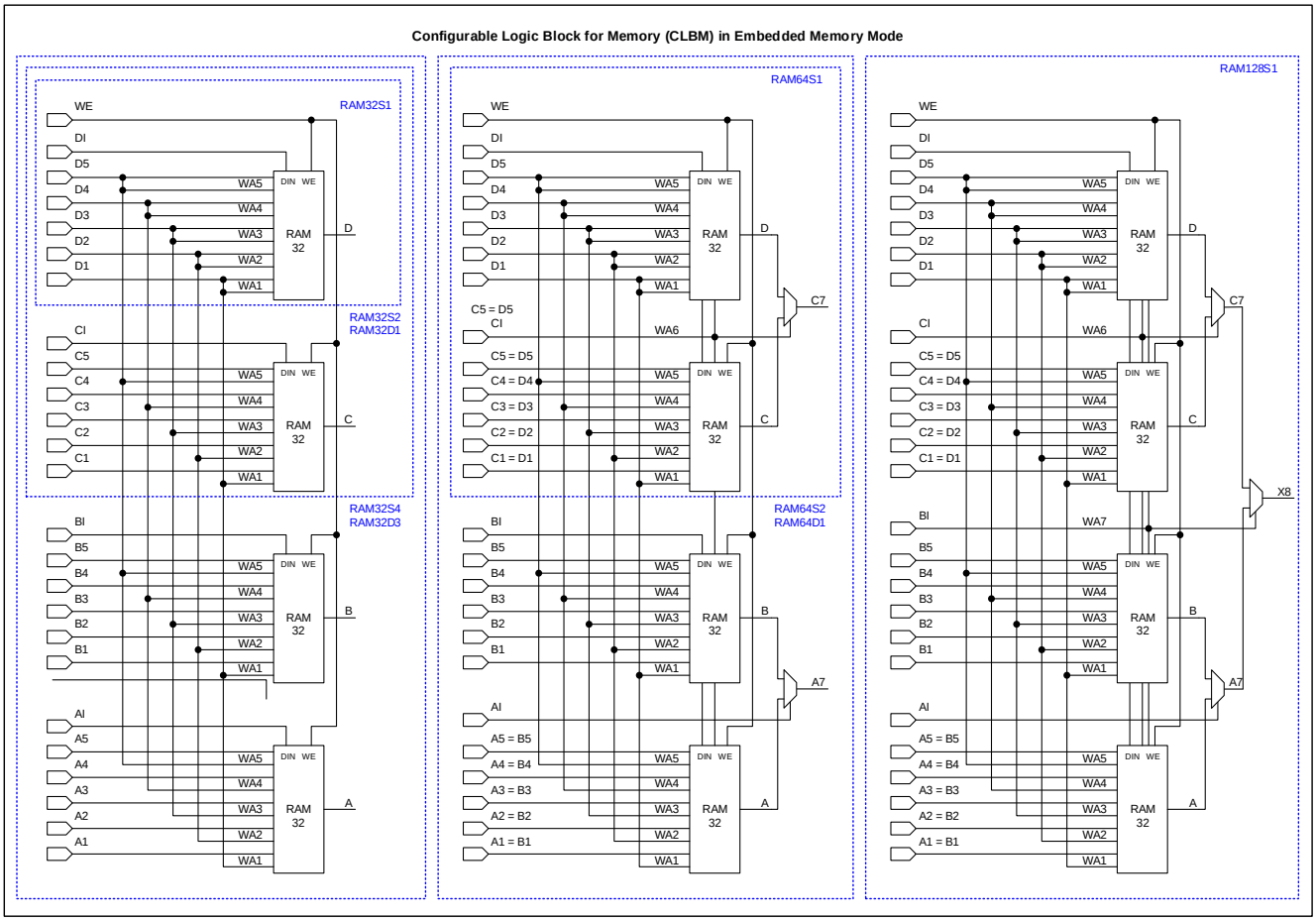


Figure 22. Configurable Logic Blocks for Memory Used in Embedded Memory Mode

5.4 Core IO Buffers (IOBs)

The IO Buffers serve as the interface between the CLBs and resources external to the FPGA Core. These buffers are arranged around the periphery of the Core. Most of the IOBs are utilized for BRAM connections and a significant portion is used for interconnection between the two tiles. Other IOBs are be used for different functions connections, as:

- GPIOs input/output and control signals (output enables, active pull-up enables).
- Clocking sources control
  - 2x PLL (Note) – reference clock select, dividers values, power-down signals, lock signal.
  - Oscillator – enable, mode selection, and ready signal.
  - Oscillator Post Divider – enable, division factor selection, and ready signal.
  - LVDS.
- Boot address select logic controls.
- Internal reset and Sleep mode assertion signals.
- CONFIG signal.
- Oscillator dividers output signal fed as data into tiles.
- Status signals for **Sleep** and **Reset** modes.

Note: PLL0 and PLL1 have different set of control signals, see sections 6.3.2 PLL0 and 6.3.3 PLL1.

The structure of the IOBs is shown in Figure 23. One of the selectable functions provided by the IOBs is clock synchronization.

There are also dedicated clock IOBs to fed clock into/from the FPGA Core.

GPIO-related IOBs have GPIO-to-IOB and IOB-to-GPIO propagation delays. These delays are not matched for all paths. Detailed delays values for these paths can be found in Table 8.

Table 8. GPIO-to-IOB and IOB-to-GPIO Data Path Delays

GPIO in IO Bank0	Direction	Delay (Typ [1])	Unit
GPIO0	GPIO to IOB	7.0	ns
	IOB to GPIO	9.8	
GPIO1	GPIO to IOB	5.0	
	IOB to GPIO	6.3	
GPIO2	GPIO to IOB	9.6	
	IOB to GPIO	7.2	
GPIO3	GPIO to IOB	8.4	
	IOB to GPIO	5.6	
GPIO4	GPIO to IOB	7.5	
	IOB to GPIO	9.6	
GPIO5	GPIO to IOB	6.6	
	IOB to GPIO	9.0	
GPIO6	GPIO to IOB	5.3	
	IOB to GPIO	9.7	
GPIO7	GPIO to IOB	7.8	
	IOB to GPIO	9.6	

GPIO in IO Bank0	Direction	Delay (Typ [1])	Unit
GPIO8	GPIO to IOB	3.9	ns
	IOB to GPIO	4.9	
GPIO9	GPIO to IOB	3.3	
	IOB to GPIO	4.4	
GPIO10	GPIO to IOB	6.1	
	IOB to GPIO	4.7	
GPIO11	GPIO to IOB	3.3	
	IOB to GPIO	4.8	
GPIO12	GPIO to IOB	3.0	
	IOB to GPIO	5.0	
GPIO13	GPIO to IOB	2.9	
	IOB to GPIO	5.2	
GPIO14	GPIO to IOB	2.7	
	IOB to GPIO	4.2	
GPIO15	GPIO to IOB	3.1	
	IOB to GPIO	4.8	
GPIO16	GPIO to IOB	3.2	
	IOB to GPIO	4.7	
GPIO17	GPIO to IOB	3.4	
	IOB to GPIO	4.7	
GPIO18	GPIO to IOB	4.6	
	IOB to GPIO	5.1	
GPIO19	GPIO to IOB	5.4	
	IOB to GPIO	5.0	
GPIO20	GPIO to IOB	3.6	
	IOB to GPIO	5.0	
GPIO21	GPIO to IOB	4.6	
	IOB to GPIO	6.3	
GPIO22	GPIO to IOB	5.5	
	IOB to GPIO	5.4	
GPIO23	GPIO to IOB	5.8	
	IOB to GPIO	4.8	
GPIO24	GPIO to IOB	8.1	
	IOB to GPIO	8.3	
GPIO25	GPIO to IOB	7.9	
	IOB to GPIO	8.7	

GPIO in IO Bank0	Direction	Delay (Typ [1])	Unit
GPIO26	GPIO to IOB	6.9	ns
	IOB to GPIO	8.1	
GPIO27	GPIO to IOB	6.7	
	IOB to GPIO	8.0	
GPIO28	GPIO to IOB	8.2	
	IOB to GPIO	7.4	
GPIO29	GPIO to IOB	6.3	
	IOB to GPIO	7.9	
GPIO30	GPIO to IOB	8.3	
	IOB to GPIO	8.0	
GPIO31	GPIO to IOB	8.9	
	IOB to GPIO	9.2	
GPIO32	GPIO to IOB	6.3	
	IOB to GPIO	9.1	
GPIO33	GPIO to IOB	6.2	
	IOB to GPIO	7.3	
GPIO34	GPIO to IOB	4.8	
	IOB to GPIO	6.5	
GPIO35	GPIO to IOB	2.8	
	IOB to GPIO	4.3	
GPIO36	GPIO to IOB	4.3	
	IOB to GPIO	6.5	
GPIO37	GPIO to IOB	5.9	
	IOB to GPIO	7.5	
GPIO38	GPIO to IOB	12.1	
	IOB to GPIO	12.0	
GPIO39	GPIO to IOB	9.2	
	IOB to GPIO	11.3	

[1] V_{DDC} = 1.1 V, V_{DDIO} = 2.5 V, TT process corner, T = 25 °C.

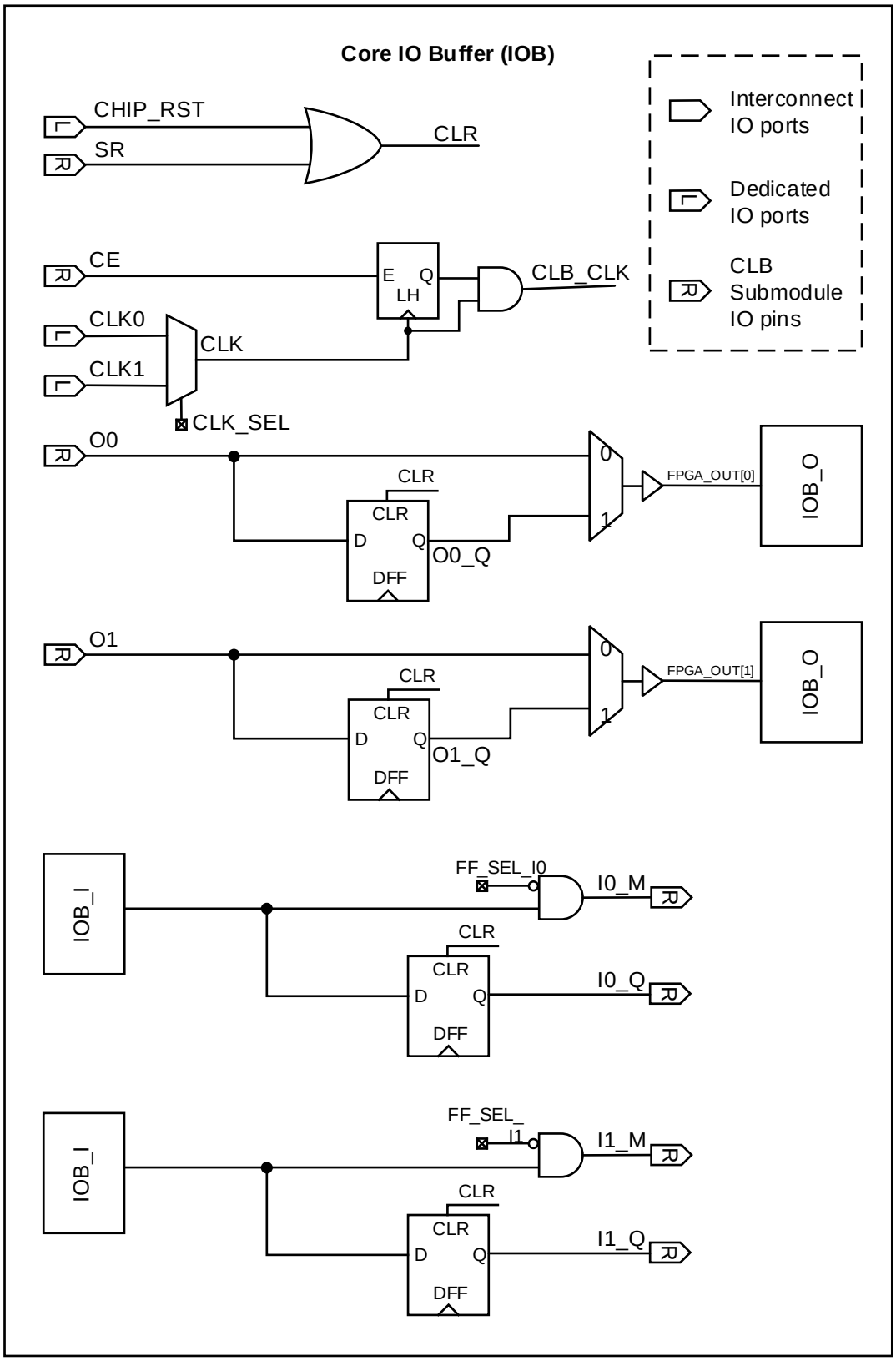


Figure 23. Core IO Buffers

5.5 Power Management and Operating Modes

5.5.1. FPGA Core Power-On Reset

POR circuitry monitors stability of the V_{DDC}, V_{DDIO} to ensure correct device operation and to reset device (including the FPGA Core) when power supplies are not withing acceptable operating range. On first power-on Configuration Registers are read (when POR circuit de-asserts reset) to initialize device.

5.5.2. Configuration Mode

In configuration mode Configuration Registers are read and FPGA Core is configured from correspondent source (see section 10 Configuration Modes). During this mode operation of the device is under SoC logic control. GPIO state is Hi-Z or pulled HIGH (if enabled by corresponding Configuration Registers), or in case if reconfiguration happens after nRST event (see section 5.5.5 nRST: Reset Mode) – it is Hi-Z or retained from previous Functional Mode. SPI interface pins are always overridden by SoC logic if SPI Controller or SPI Target mode is used.

FPGA Core is power gated, but its configuration memory is always on to be able to configure the FPGA Core.

BRAMs are power-on for initialization process, but if not used – power-gated.

Oscillator is power on (as it is clock source for SoC logic), but PLLs are power down.

During configuration process:

- Optionally bitstream received through SPI interface can be decrypted (if bitstream encryption is used).
- CRC integrity check is always performed (independently of configuration source).

5.5.3. Functional Mode

Functional Mode is the user's main operating mode, which user enters after successful configuration. Transition to this mode might be delayed by holding nSLEEP = LOW. Also, if SW option ***Wait for Stable OSC/PLL = "Wait for stable clocks"*** – transition to this mode would be delayed until all used clock sources provide stable clocks; if it is set to ***"Don't wait for stable clocks"*** - there will be no additional delay due to clocks stabilization time.

In this mode the FPGA Core is powered-on, configured and performs user-defined functions.

In this mode all components of the device are under user control: BRAMs, Oscillator, PLLs, GPIOs, LVDS and others.

User can exit from this mode with nSLEEP or nRST events (see sections 5.5.4 nSLEEP: Sleep (Retention) Mode and 5.5.5 nRST: Reset Mode).

5.5.4. nSLEEP: Sleep (Retention) Mode

The nSLEEP signal allows a user to set the FPGA Core into a low-power mode while retaining internal state of the FPGA Core (includes DFFs and distributed memory states). The OSC and PLL are powered down during this time as well. While nSLEEP is LOW and nRST is HIGH the GPIOs configured as outputs retain their logic state. On a LOW → HIGH transition of the nSLEEP signal, a delay is required before the FPGA Core can be utilized (see section 3.5.11 nRST (PWR) and nSLEEP (EN) Specifications).

Transition to **Sleep Mode** can be triggered from nSLEEP pin or from iob_sleep_start (selected with ***nSLEEP Signal Source***).

5.5.5. nRST: Reset Mode

The nRST signal allows a user to reset the device and set it into lowest power state. When the nRST input is LOW the FPGA Core is in its lowest-power state, intended for a long-latency period without use or to perform forced re-configuration of the device. During this time, internal state is not retained in the FPGA Core, the Oscillator and PLLs are disabled as well. However, BRAMs content may be retained in this state if ***BRAM Keep*** option is enabled.

While nRST is LOW by default the GPIOs states are set as Hi-Z but might be retained same as for Sleep (Retention) Mode if ***GPIO Keep*** option is enabled.

On a LOW → HIGH transition of the nRST signal, reconfiguration would happen and delay is required before the FPGA Core can be utilized (see Section 3.5.11 nRST (PWR) and nSLEEP (EN) Specifications), provided nSLEEP signal is high.

Transition to **Reset Mode** can be triggered from nRST pin or from iob_int_rst (selected with ***nRST Signal Source*** option).

Note: If option ***SPI Boot Priority*** is set to ***"Force Boot Over SPI"*** or iob_boot_ctrl_force_spi_boot = HIGH – the SLG47920/SLG47921 will look for an external configuration device once the FPGA Core has met the Power-on Reset Threshold.

5.6 Typical Building Block Performance

Table 9. Pin-to-Pin Performance

Function	Timing [1] [2]	Unit
Pin-to-pin propagation (in/out GPIOs connected to same tile, but on different sides of tile)	18	ns
Pin-to-pin propagation (in/out GPIOs connected to different tiles)	19	ns
5b4b decoder	28	ns
4:1 MUX	23	ns
16:1 MUX	25	ns

[1] Exact performance may vary with device. Parameter was measured with oscilloscope but is not measured on every device during production.

[2] Under typical operating conditions: V_{DDC} = 1.1 V, V_{DDIO} = 2,5 V, TT process corner, E = 25 °C.

Table 10. Register-to-Register Performance

Function	Timing [1]		Unit
	Min [2]	Typ	
16:1 MUX	41	88	MHz
16-bit adder	58	116	MHz
16-bit counter	79	132	MHz
32-bit counter	55	111	MHz
256 x 8 Pseudo Dual Port RAM	52	98	MHz
DFF to DFF	212	365	MHz
DFF to LUT5 to DFF	183	337	MHz

[1] Exact performance may vary with device and tool version. The ForgeFPGA Workshop Software tool uses internal parameters that have been characterized but are not tested on every device.

[2] Under worst-case operating conditions available for STA (V_{DDC} = 0.99 V, -40 °C, SS process corner), which are outside worst-case of Recommended Operating Conditions. Also, depends on which synthesis engine is used – ABC or ABC9 (gives different results for different designs).

5.7 OTP User Area Access

There are 256 bits of user accessible OTP bits (**user_otp_data[255:0]**). To access them simple serial interface should be implemented in user logic (see Figure 24). Content of these data is changed with ***Open Data Editor*** option of ***User OTP Data*** element.

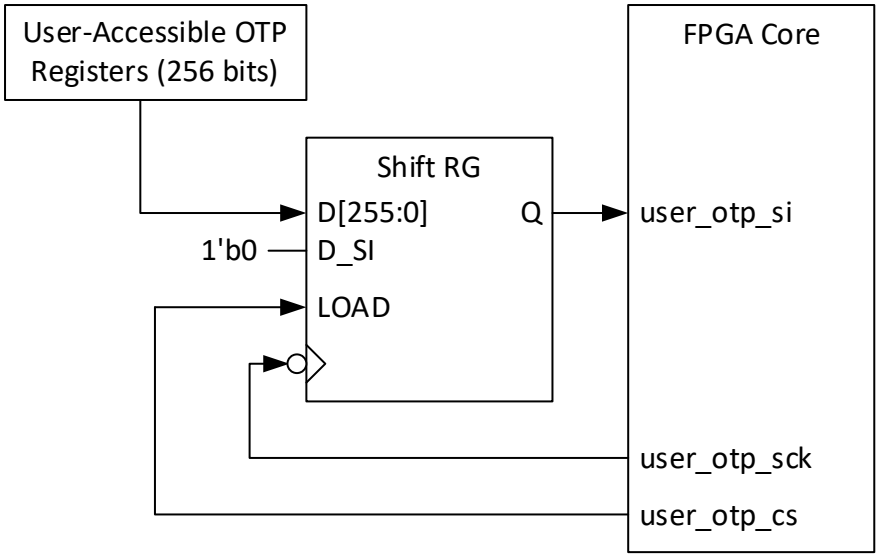


Figure 24. Serial Interface for User Access to OTP

Timing diagram of this interface is shown in Figure 25.

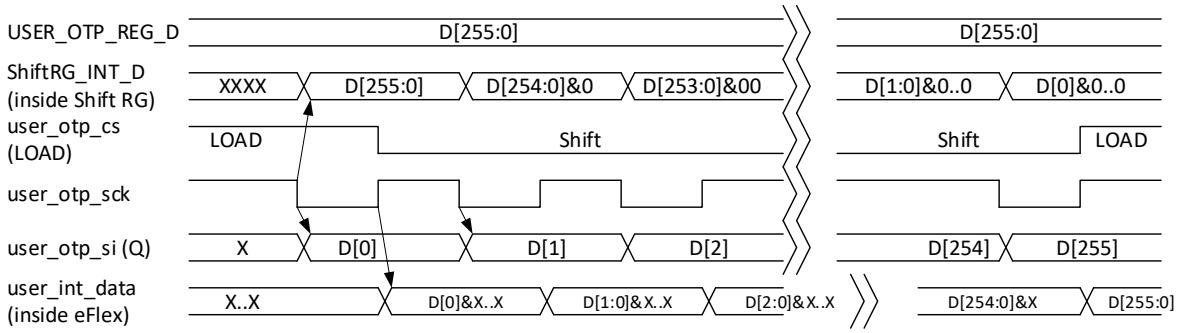


Figure 25. Serial Interface for User Accesses to OTP (Timing Diagram)

This serial interface operates as follows:

- Idle state is when CS and SCK are HIGH.
- Shift RG is clocked with negative edge of user_otp_sck, and user logic shall latch data at positive edge of this clock.
- Falling clock edge required before CS 1 → 0 to load data into Shift RG.
- user_otp_cs shall be changed simultaneously with user_otp_sck (data IOB, not clock IOB) rising edge.
- SCK can run continuously – this would result in continuous re-LOAD of data to ShiftRG when user_otp_cs = HIGH.

Thus, after 256 SCK cycles user logic will acquire 256 bits of data from dedicated OTP User Area. If there are less data stored – this process can be stopped (with user_otp_cs 0 → 1) when required amount of data are received.

Maximum allowed SCK frequency – 50 MHz.

This area can be used to store different kind of data required to customize user's logic operation without changing bitstream itself. Such data might be trim codes, user-defined configuration bits, encryption/decryption keys and others.

These data might be secured from reading it back from OTP in service mode by locking from reading whole user-related configuration area (see section 10 Configuration Modes for security features description). Thus, these data would be accessible only from user-logic inside the FPGA Core.

6. Clocking

6.1 Clock Network

The FPGA Core has four clock domains in total. Each tile has two clock domains, Clock_0 and Clock_1. Each of them may use a unique clock or use same clock, resulting in a total of up to four unique clocks being available. Tiles can exchange clocks or use each clock separately (depending on user application).

Note: Usage of rise and fall edges in the same application would occupy two clock domains (within same tile or separate tiles) due to internal architecture of clock tree.

Figure 26 shows the FPGA Core clock network and their external connections to it.

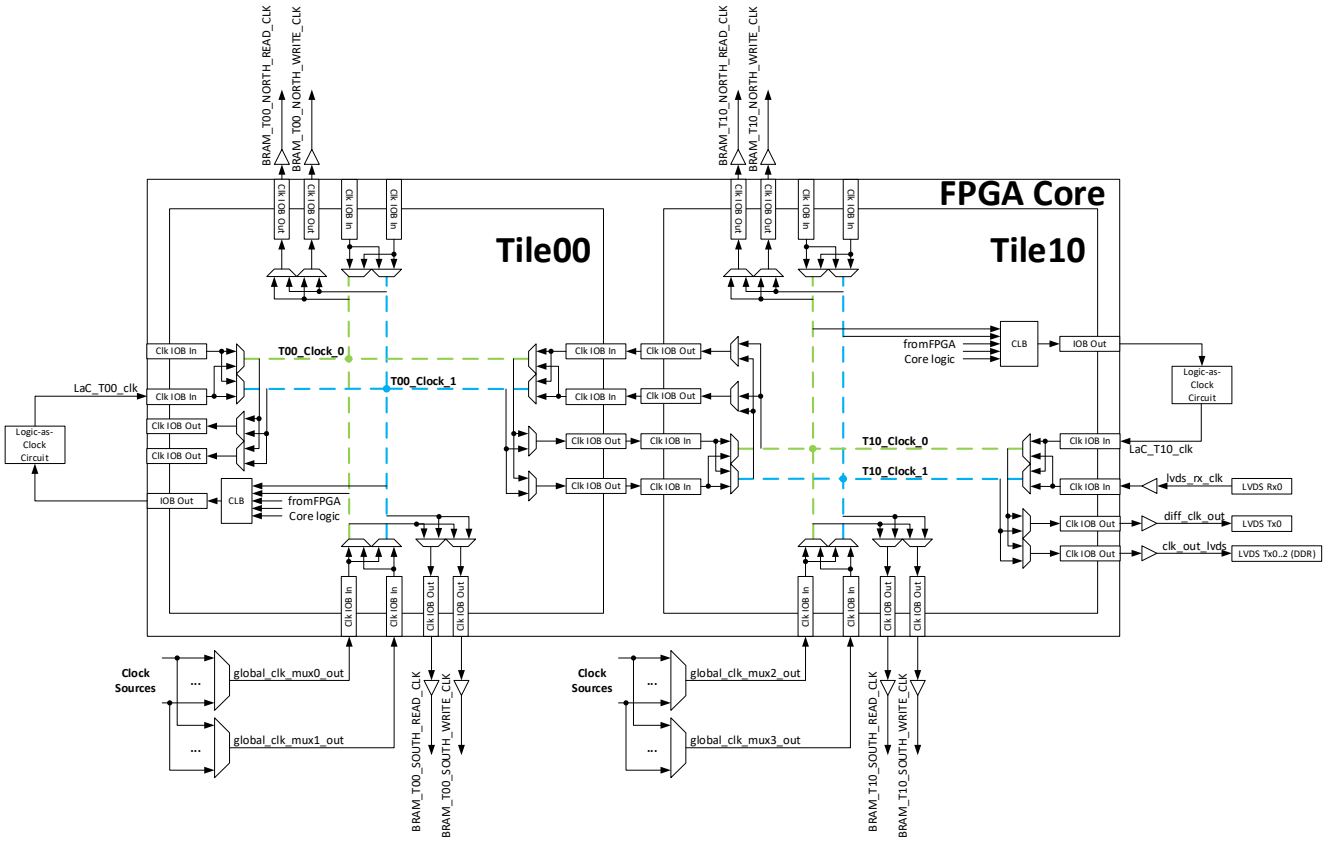


Figure 26. FPGA Core Clock IOBs Connection

Clocks to the FPGA Core are provided via dedicated clock IOBs which are located as 2 IN + 2 OUT on each side of each tile. Clock IOBs along the sides where tiles are interconnected are used for inter-tile clock connections (defined by user logic). Therefore, 6 INs and 6 OUTs are available to be used for external connections.

The core is divided into four directions:

North side

BRAM North (Tile00 and Tile10 respectively) read and write clocks are connected to clock outputs.

Tile00 West side

Logic-as-Clock (Tile00) is connected to clock input. For more details see section 6.4 Logic-As-Clock.

Tile10 East side

Logic-as-Clock (Tile10) is connected to clock input. For more details see section 6.4 Logic-As-Clock.

LVDS received differential clock is connected to dedicated clock input.

Two clock outputs are occupied by two clocks, which are required by the LVDS transmit side:

- Transmit differential clocks

- Clock for DDR circuitry of LVDS.

South side

On BRAM South (Tile00 and Tile10 respectively) read and write clocks are connected to clock outputs.

Two clock inputs on South side of each tile are occupied by the input clocks from the global clock distribution network (see details below).

Global clock distribution network

Each tile has two separate clock IOB inputs fed by clock MUXes to independently select the clock source for each tile. Clocks for the FPGA Core are provided symmetrically to all used tiles to obtain identical timing characteristics. A balanced clock tree is used.

Clock source selection is statically defined by ***Global Clock MUX Select*** option in SW individually for each clock MUX.

Figure 27 shows the global clock distribution network.

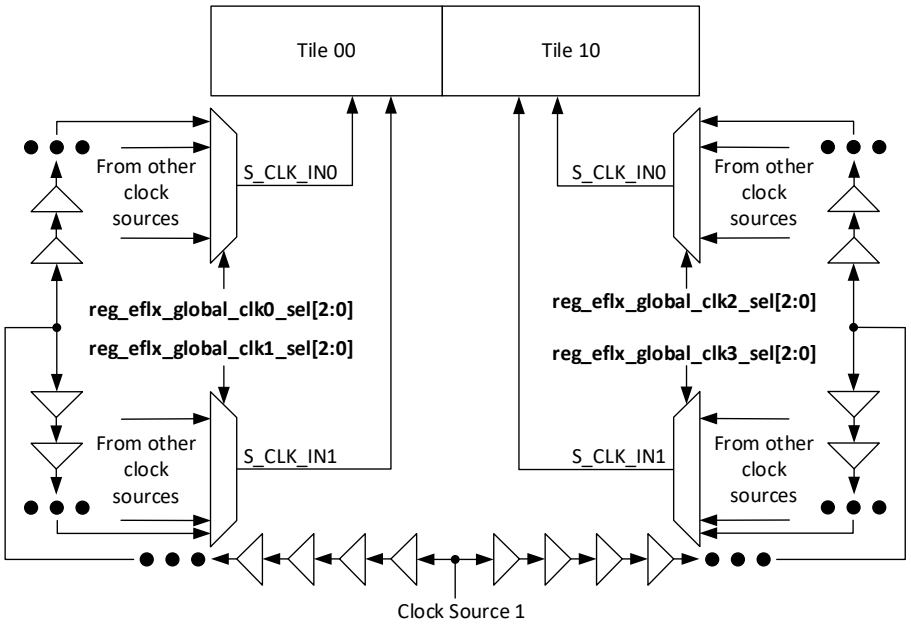


Figure 27. Global Clock Distribution Network

Sources available in the Global Clock Distribution Network consist of:

- PLL0_FOUT0 clock
- PLL0_FOUT1 clock
- PLL1_FOUT clock
- OSC POSTDIV_OUT0 clock
- OSC POSTDIV_OUT1 clock.

6.2 On-Chip Oscillator

6.2.1. Overview

The SLG47920/SLG47921 has a High-frequency on-board oscillator for use within the high-density digital FPGA Core. During either of low-power modes of the FPGA Core (see section 5 FPGA Core) the high-frequency OSC is disabled. When the OSC_CTRL_EN signal is pulled high, there is a delay in receiving the signal at OSC_CLK. This delay allows the signal to stabilize hence, getting rid of any glitches in the output from the start. Oscillator has the following operating features:

- Two operating modes: high frequency (50 MHz) and low frequency (3 MHz).

- Possibility to power-down oscillator with the OSC_EN signal.
- Ready signal to indicate the output clock is stable.

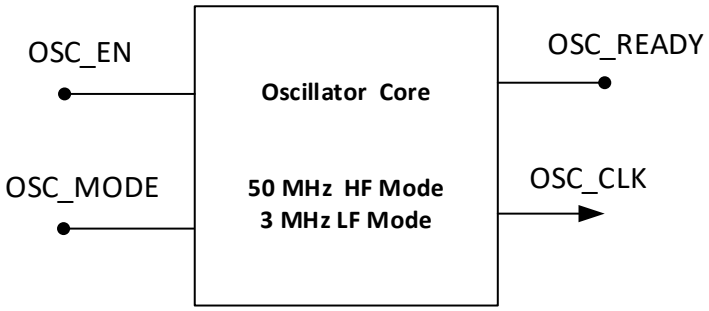


Figure 28. High-Frequency Oscillator Block Diagram

Note: OSC_CLK is not available directly for user. See description below.

6.2.2. Signal Descriptions

Control inputs are derived from the FPGA Core.

- **OSC_EN** – Active HIGH enable signal for the oscillator.
- **OSC_MODE** (Note) – High/Low Frequency Mode selection. A HIGH level input corresponds to 50 MHz, LOW level corresponds to 3 MHz.
- **OSC_CLK** – Buffered oscillator clock output. It can be a clock source for PLLs or Oscillator Post Divider. It is connected to Global Clock Distribution Network only through Post Divider.
- **OSC_READY** – outputs HIGH level on this signal to indicate that the oscillator frequency is stable.

Note: To change OSC_MODE it is required to set OSC_EN = LOW, change OSC_MODE, wait at least 1 µs and then set OSC_EN = HIGH. Changing mode without disabling oscillator is not allowed as it might result in glitches at clock output.

6.2.3. Oscillator Post Divider

This circuit is intended to provide a low-frequency clock by dividing the Oscillator clock. The following functionality is implemented:

- Divide Oscillator clock by factor of N in range 1-128 (step with power of 2).
- Two divided output clocks OUT0/1 (each selected independently).
- IOB to select the division factor for each clock output individually.
- Ability to output raw Oscillator clock.
- Ability to switch between different division factors (Note).
- Two flags to indicate that the output clock is settled for each postdiv_out0/1.

Note: It is not allowed to switch division factor while respective Post Divider output is enabled. First it is required to disable output, switch Post Divider factor and then – enable output again.

Oscillator post divider implementation is shown in Figure 29.

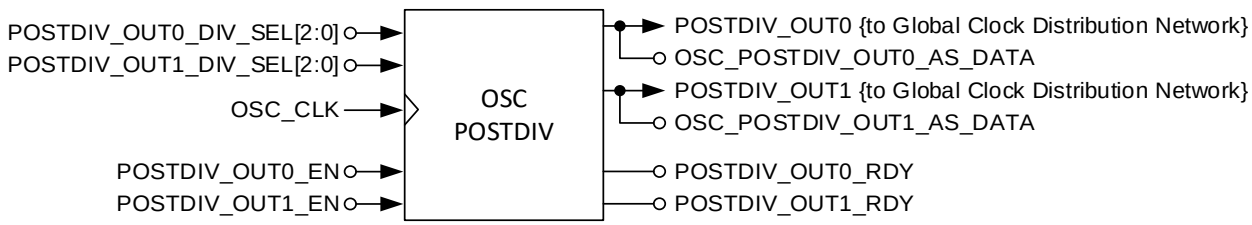


Figure 29. Oscillator Post Divider

Oscillator Post Divider outputs are connected to the Global Clock Distribution Network and at the same time – to dedicated IOBs of FPGA Fabric to be used as low-frequency control signals if needed.

Control inputs are derived from the FPGA Core.

- **POSTDIV_OUT0/1_EN** – Active HIGH enable signal for the Oscillator Post Divider Out0/1 (separate for each), also enables Oscillator if it was previously disabled.
- **POSTDIV_OUT0/1_DIV_SEL** – signal to select division ratio for Out0/1 of Oscillator Post Divider (separate for each).
- **POSTDIV_OUT0/1** – Oscillator Post Divider Out0/1 clock output. It is connected to Global Clock Distribution Network.
- **OSC_POSTDIV_OUT0/1_AS_DATA** – Oscillator Post Divider Out0/1 clock which is fed into FPGA Core as data signal.
- **POSTDIV_OUT0/1_READY** – outputs HIGH level on this signal to indicate that the Oscillator Post Divider Out0/1 is stable (separate for each).

Available division stages and correspondent frequencies of the Post Divider are shown in Table 11.

Table 11. Oscillator Post Divider Available Frequencies

Division Factor	Oscillator High Frequency Mode Output	Oscillator Low Frequency Mode Output
F_{osc}	50 MHz	3 MHz
$F_{osc}/2$	25 MHz	1.5 MHz
$F_{osc}/4$	12.5 MHz	750 kHz
$F_{osc}/8$	6.25 MHz	375 kHz
$F_{osc}/16$	3.125 MHz	187.5 kHz
$F_{osc}/32$	1.56 MHz	93.75 kHz
$F_{osc}/64$	781.25 kHz	46.88 kHz
$F_{osc}/128$	390.625 kHz	23.44 kHz

Oscillator Post Divider OUT0 output frequency might be connected to dedicated GPIO10 using SW option ***OUT0 fout to GPIO10*** to be able to output clock for any external devices.

POSTDIV_OUT0/1_EN can be applied synchronously or asynchronously (relative to POSTDIV_OUT0/1 clock) depending on ***OUT0/1 Enable Mode*** option.

6.3 Phase-Locked Loop

6.3.1. Overview

The SLG47920/SLG47921 includes two low-power, wide input and output integer phase-locked loop (PLL) for use in applications requiring various frequencies. To maintain a low-power state the PLL has power-down option for power management purposes. The input reference clock for the PLL can be either the internal oscillator, or an external clock routed through GPIO6 (for PLL0) or GPIO7 (for PLL1), or the LVDS differential clock. Output clocks from both PLLs are available for FPGA Core through Global Clock Distribution Network.

PLL0 uses two external POSTDIV circuits instead of the internal POSTDIV circuit and produces two in-phase output clocks called PLL0_fout0 and PLL0_fout1. The external POSTDIV circuit is implemented in such a way that it is possible to predict the output phase shift between PLL0 FREF and PLL0_fout0/1. On the contrary, PLL1 uses the internal POSTDIV circuit and provides a single output frequency called PLL1_fout, which phase shift relative to PLL1 FREF is not predictable.

PLL0 is fully controlled from IOBs on the FPGA Core and PLL1 is controlled with a combination of static configuration (set with SW) and control signals from IOBs. PLL0_fout0 and PLL1_fout output clocks are

connected to dedicated GPIO8/9 with dedicated SW options enabled (***PLL Fout0 to GPIO8***/***PLL Fout to GPIO9***) to output clock for any external devices.

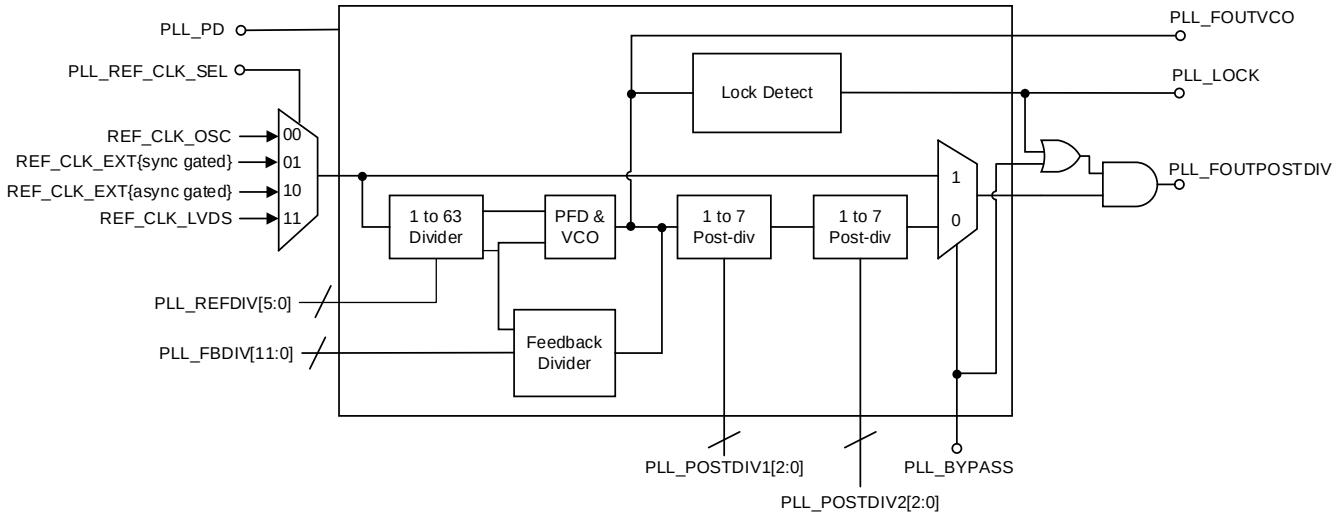


Figure 30. Phase-Locked Loop Block Diagram

The behavior of the SLG47920/SLG47921's PLL is to receive a reference frequency and either divide or multiply the frequency value per the following equation, where $f_{reference\_clock}$ is the reference frequency of the external clock source or on-chip OSC, chosen through PLL_REF_CLK_SEL:

$$PLL\_FOUTVCO = (f_{reference\_clock} \times PLL\_FBDIV)/PLL\_REFDIV$$

$$PLL\_FOUTPOSTDIV = \frac{f_{reference\_clock} \times PLL\_FBDIV}{PLL\_REFDIV \times PLL\_POSTDIV1 \times PLL\_POSTDIV2}$$

Using larger values for the variables in the numerator and denominator will reduce clock jitter at the expense of increased current consumption.

For the PLL to behave correctly several conditions on the input and output clock signals must be met:

- The reference clock input must be a stable, single frequency within the frequency range specified in the SLG47920/SLG47921's EC table. Jitter and duty cycle should also be confirmed to be within the acceptable range specified in the EC tables.
- FOUT must be within the frequency range specified within the SLG47920/SLG47921's FPGA Core operating frequency limits. The LOCK output must be used to ensure a stable output frequency.

6.3.2. PLL0

PLL0 and external post dividers from user perspective are considered as single entity which has two available outputs.

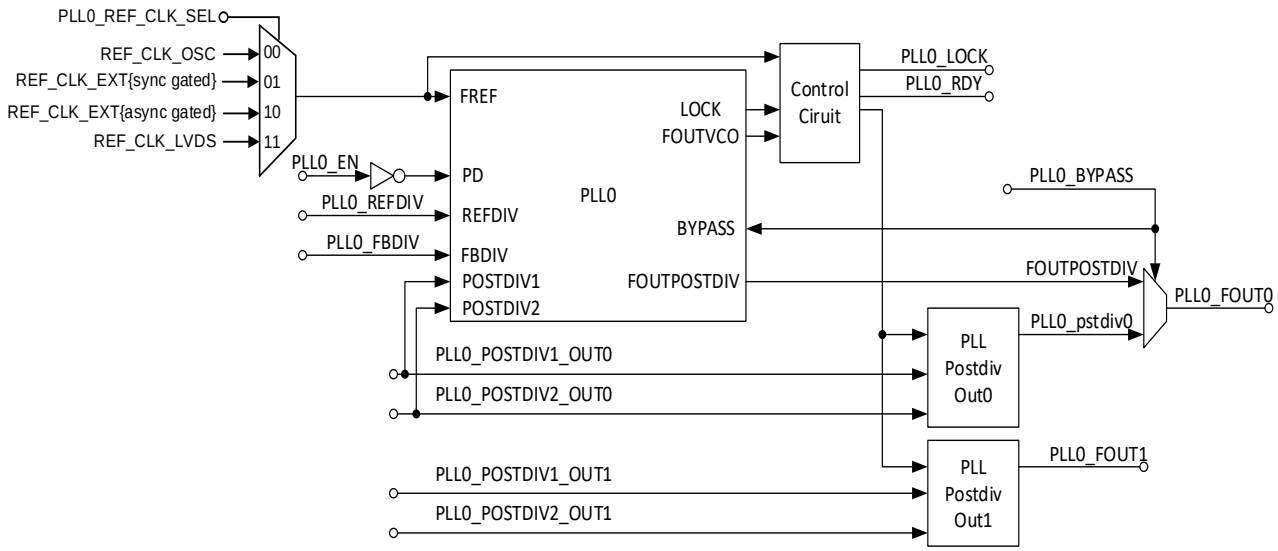


Figure 31. PLL0 with External Post Dividers

Using additional controls from IOBs or Configuration Registers user can obtain access to FOUTPOSTDIV of PLL0 itself on PLL0_FOUT0:

- **PLL0_BYPASS** – to get access to BYPASS mode of the PLL which utilize FOUTPOSTDIV path.

In all other cases FOUTVCO (clock of frequency controlled oscillator of the PLL) is used to feed external post dividers. Control Circuit is intended to control post dividers operation and provide predictable phase shift relative to PLLs reference clock.

6.3.2.1. Signal Descriptions

Clock and control inputs determine the input clock source and intended output frequency.

- **PLL0_REF_CLK_SEL** – selects the PLL Input Clock source between the internal OSC, external clock from GPIO6 or LVDS Rx Differential Clock.
- **PLL0_BYPASS** – active HIGH signal that asserts a direct path between the FREF and PLL0_FOUT0.
- **PLL0_REFDIV [5:0]** – sets the reference divide value (range 1 to 63).
- **PLL0_FBDIV [11:0]** – sets the PLL Feedback Divider value (range 16 to 400).
- **PLL0_POSTDIV1_OUT0[2:0]** and **PLL0_POSTDIV2_OUT0 [2:1]** – the two stages of Post Dividers are used to divide down the VCO Frequency before the FOUT0 clock output. Each stage has options for division from 1 to 7. Total division ratio is POSTDIV1 * POSTDIV2. This set of parameters is shared between PLL's internal post divider and external PLL Postdiv Out0.
- **PLL0_POSTDIV1_OUT1[2:0]** and **PLL0_POSTDIV2_OUT1 [2:1]** – the two stages of external PLL Postdiv Out1 are used to divide down the VCO Frequency before the FOUT0 clock output. Each stage has options for division from 1 to 7. Total division ratio is POSTDIV1 * POSTDIV2.
- **PLL0_FOUT0/PLL0_FOUT1** – output clocks of PLL0.
- **PLL0_LOCK** – lock signal.
- **PLL0_RDY** – ready signals, goes HIGH same time as PLL0_FOUT0/1 becomes available for user.

Power inputs determine the existing power state of the PLL. Enable inputs are used to enable the different clock outputs that can be used in the FPGA Core and can lower power consumption when properly utilized.

All power and Enable inputs are connected to the FPGA Core.

- **PLL0_EN** – power enable for PLL0. Active HIGH.

Dedicated control circuit implements correct PLL operation control in different operating modes of SLG47920/SLG47921.

SW option ***PLL Clock Gating with LOCK*** determines if output clock is gated with LOCK signal or not:

- When "***Not gated***": PLL clock independently of LOCK signal status (only available when FOUTPOSTDIV is used).
- When "***Gated***": PLL clock gated by LOCK signal (default state).

6.3.2.2. External POSTDIV Architecture

The main characteristics of PLL0 external post dividers are:

- Both POSTDIVs shall produce "in-phase" output clocks, thus they are driven by the same clock and are turned on simultaneously.
- Produced clocks shall be aligned with FREF edge.
- POSTDIV_FOUT = 0 when the corresponding PLL0_POSTDIV0/1_sel = 0.

External post dividers operate similar to the PLL's internal post divider (see Figure 32).

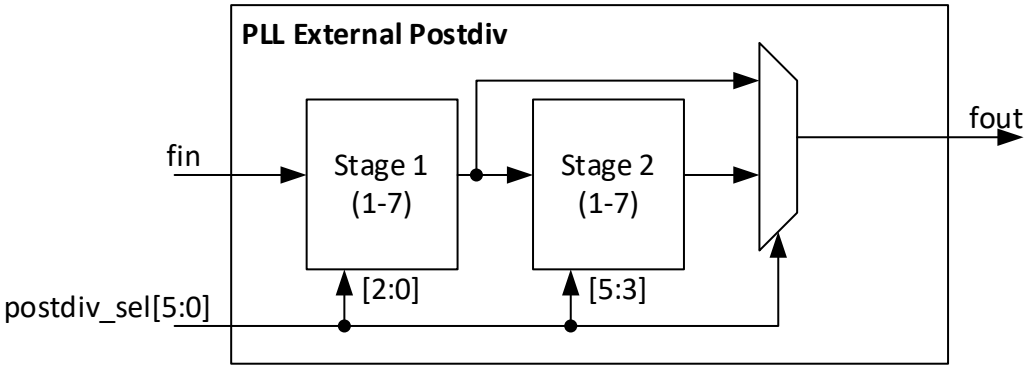


Figure 32. External POSTDIV Architecture

The following characteristics apply:

- Max allowable fin = 1000 MHz.
- 2-stage division.
- Each stage has range of division factor 1 through 7 (including all even and odd numbers in this range) and is controlled by a 3-bit select signal.
- Output clock has ~50 % duty cycle.
- Stages should be utilized to follow the rule Stage1_div_factor >= Stage2_div_factor (same as recommended for the PLL internal POSTDIV).
- When postdiv_sel[5:0] = 0 – FOUT = 0.

6.3.2.3. External Post Divider Clock Phase Shift

Using external Post Dividers user is able to obtain predictable phase shift between FREF and PLL0_FOUT0/1.

This phase shift depends upon several parameters:

- FREF period
- VCO frequency
- Operating mode
- Post Divider settings.

Also, to have pre-defined constant phase shift it is required that FREF and FOUT0/1 period shall have integer ratio (works both with even and odd ratios), as well as FREF and FVCO should have integer ratio too.

Phase shift can be estimated with the following approach. First, PLL initial delay is estimated:

$$T_{init\ dly} = \left(3 + N_{ctrl\ dly} + N_{postdiv\ dly} + (0\ or\ 1)^{*}\right) \times T_{VCO}$$

* (0 or 1) VCO clock cycles might appear due External Post Divider alignment of LOCK signal to FREF and synchronization to VCO clock;

$$N_{ctrl\ dly} = \begin{matrix} 6 & when\ not\ first\ power\ up\ and\ PSOTDIV\ value\ didn't\ changed \\ 8 & when\ not\ first\ power\ up\ and\ PSOTDIV\ value\ changed \\ 17 & when\ first\ power\ up \end{matrix}$$

$$N_{postdiv\ dly} = N_{stage1} + N_{stage2}$$

$$N_{stageX} = \begin{matrix} 0 & if\ divider < 3 \\ 1 & for\ all\ other\ values \end{matrix}$$

where:

$T_{init\ dly}$ – FOUT0/1 first edge initial delay [ns];

T_{VCO} – period of VCO clock [ns];

$N_{ctrl\ dly}$ – delay (in number of clocks) of Control Circuit [no units];

$N_{postdiv\ dly}$, N_{stage1}, N_{stage2} – total delay (in number of clocks) of Post Divider, its' 1st and 2nd stages respectively [no units].

Further there are 2 cases:

$$when\ T_{init\ dly} \geq T_{ref}:\ T_{phase\ shift} = T_{init\ dly}\ rem\ T_{ref}$$

$$when\ T_{init\ dly} < T_{ref}:\ T_{phase\ shift} = T_{init\ dly}\ rem\ T_{fout}$$

where:

$T_{phase\ shift}$ – FOUT0/1 edge phase shift relative to FREF edge [ns];

T_{ref} – period if reference clock [ns];

T_{fout} – period of FOUT0/1 clock (after Post Divider) [ns].

If the ratio between FREF and FOUT0/1 is non-integer – there would be no constant phase shift.

If ratio between FREF and FVCO is non-integer – there would be no constant phase shift.

Example 1:

First power up, FREF = 25 MHz, FVCO = 700 MHz, POSTDIV1 = 7, POSTDIV2 = 1, FOUT0 = 100 MHz.

In this case:

$$T_{ref} = 40\ ns, N_{ctrl\ dly} = 17, N_{postdiv\ dly} = 1, T_{VCO} = 1.43\ ns, T_{fout} = 10\ ns$$

$$T_{init\ dly} = (3 + 17 + 1 + (0\ or\ 1)^{*}) \times T_{VCO} = 21\ to\ 22 \times T_{VCO} = (30.03\ to\ 31.46)\ ns$$

$$T_{init\ dly} < T_{ref} \rightarrow \quad T_{phase\ shift} = T_{init\ dly}\ rem\ T_{fout} = (30.03\ to\ 31.46)\ rem\ 10 = (\mathbf{0.03\ to\ 1.46})\ \boldsymbol{ns}$$

Example 2:

First power up, FREF = 50 MHz, FVCO = 1000 MHz, POSTDIV1 = 5, POSTDIV2 = 2, FOUT0 = 100 MHz.

In this case:

$$T_{ref} = 20\ ns, N_{ctrl\ dly} = 17, N_{postdiv\ dly} = 1, T_{VCO} = 1\ ns, T_{fout} = 10\ ns$$

$$T_{init\ dly} = (3 + 17 + 1 + (0\ or\ 1)^{*}) \times T_{VCO} = 21\ to\ 22 \times T_{VCO} = (21\ to\ 22)\ ns$$

$$T_{init\ dly} \geq T_{ref} \rightarrow \quad T_{phase\ shift} = T_{init\ dly}\ rem\ T_{ref} = (21\ to\ 22)\ rem\ 20 = (\mathbf{1\ to\ 2})\ \boldsymbol{ns}$$

6.3.3. PLL1

PLL1 utilize PLL with internal post divider only (as shown in Figure 33). It is controlled from Configuration Registers, except power-down control which is performed from the FPGA Core.

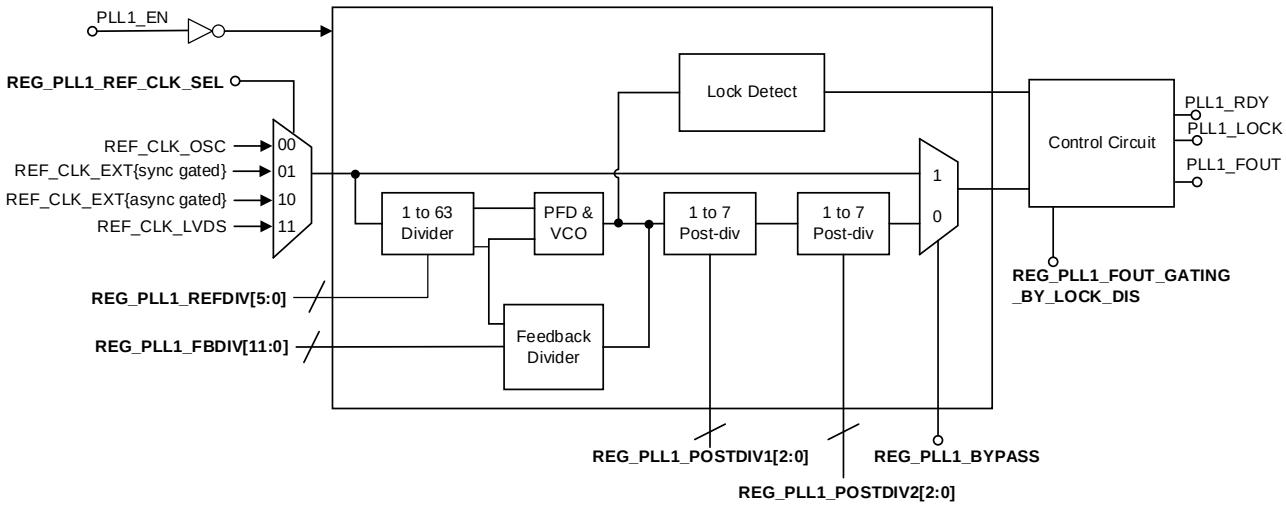


Figure 33. PLL1

Dedicated control circuit implements correct PLL operation control in different operating mode of SLG47920/SLG47921.

SW option ***PLL Clock Gating with LOCK*** determines if output clock is gated with LOCK signal or not:

- When "***Not gated***": PLL clock independently of LOCK signal status (only available when FOUTPOSTDIV is used).
- When "***Gated***": PLL clock gated by LOCK signal (default state).

6.3.3.1. Signal Descriptions

Clock and control inputs determine the input clock source and intended output frequency.

- **REG_PLL1_REF_CLK_SEL** – Selects the PLL Input Clock source between the internal OSC, external clock from GPIO6 or LVDS Rx Differential Clock (selected with Clock source select).
- **REG_PLL1_BYPASS** – is an active HIGH signal that asserts a direct path between the clock input and PLL1_FOUT (selected with Bypass Mode), which allows to route PLL's reference clock without modification and feed it into clock tree (as PLL's output).
- **REG_PLL1_REFDIV [0:5]** – Sets the reference divide value from 1 to 63 (selected with Calculate Dividers)
- **REG_PLL1_FBDIV [0:11]** – Sets the PLL Feedback Divide value from 16 to 400 (selected with Calculate Dividers).
- **REG_PLL1_POSTDIV1[0:2]** and **REG_PLL1_POSTDIV2[0:2]** – The two stages of Post Dividers are used to divide down the VCO Frequency before the FOUT clock output. Each Post Divider has options for division from 1 to 7. Total post divide ratio is POSTDIV1 * POSTDIV2 (selected with Calculate Dividers).
- **PLL1_FOUT** – output clock of PLL1.
- **PLL1_LOCK** – lock signal.
- **PLL1_RDY** – ready signal, goes HIGH same time as PLL1_FOUT becomes available for user.

Power inputs determine the existing power state of the PLL. Enable inputs are used to enable the different clock outputs that can be used in the FPGA Core and can lower power consumption when properly utilized.

All power and Enable inputs are connected to the FPGA Core.

- **PLL1_EN** – Power enable for PLL. Active HIGH.

6.4 Logic-As-Clock

In the SLG47920/SLG47921 FPGA Core, user logic signals can be utilized as a clock signal through a Logic-as-Clock path.

For this purpose, the user signal which is used as the clock should first be output through logic-IOB (LAC_T00/10_OUT) and then looped back into the FPGA core tile as the clock (LAC_T00/10_IN) through clock-IOB (see Figure 34). This is known as Logic-as-Clock circuitry (LaC Circuitry). There are two LaC paths available (see Figure 26).

To activate Logic-as-clock paths there are dedicated IOBs: LAC_T00/10_EN signals.

With Logic-as-Clock circuitry there two ways to transform the data signal into a clock signal:

- The clock signal is generated inside the FPGA Core tile (for example OSC/8) and then fed through LaC path.
- The clock signal is fed through any GPIO to the FPGA Core tile, transfers it without processing (in an asynchronous manner) and is fed through LaC0 path.

LaC circuit gives user following functionality:

- User logic signals as clocks.
- Turn LaC clock on/off using ICG (integrated clock gating cell).
- Optionally use LaC without ICG (defined by ***Clock Path*** option in SW).
- When exit Functional Mode – stop LaC clock in last state (HIGH or LOW).

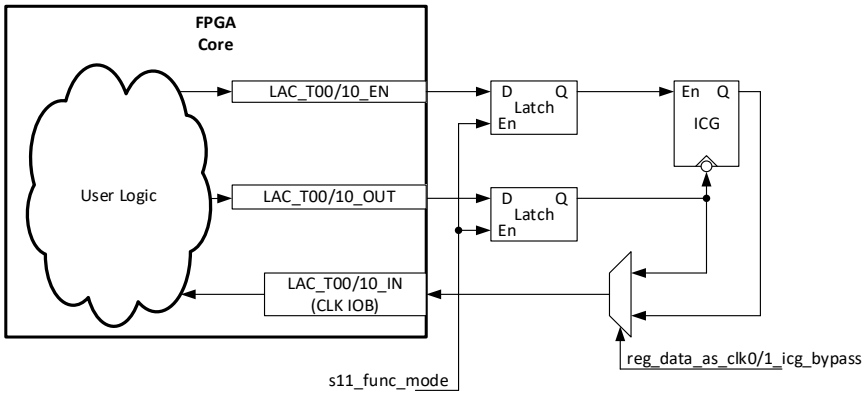


Figure 34. Logic-As-Clock Usage

Note: More information about this in Forge FPGA products documents (guides and applications notes).

7. Power Operating Modes

7.1 nRST Control Pin

nRST pin is used to provide control over operation of the SLG47920/SLG47921. This pin defines if the SLG47920/SLG47921 will be reset or operational. It is used for power-on sequencing, device reconfiguration, and power save features. When the nRST (Note) input is LOW, the SLG47920/SLG47921 is reset to its lowest-power state, intended for a long-latency period without use. During this time, FPGA core internal states are not retained, and the Oscillator and PLLs are disabled as well. However, BRAM and GPIOs may be retained in this state.

Note: Depending on ***nRST Signal Source*** option value - transition to **Reset Mode** can be triggered from nRST pin or from iob_int_rst. In later case nRST pin behaves as digital input.

After POR has released the global reset signal, the SLG47920/SLG47921 checks two conditions and acts as follows:

- If the SLG47920/SLG47921 was configured at least once then, it will check if nRST = HIGH:
  - If nRST = LOW, then it will wait.
  - If nRST = HIGH , then it will initiate the configuration process.
- If the SLG47920/SLG47921 has not been configured even once, then nRST pin state will be ignored and the device will proceed to its configuration process to read the registers related to Configuration Pull Ups and AES Configuration; when the configuration registers are read, nRST state is processed as described above.

SLG47920/SLG47921 will be in following state:

- FPGA Core – in its low power state.
- FPGA Core distributed memory is not retained.
- BRAM is retained ONLY if SW option ***BRAM Keep*** is set (separate for each BRAM).
- GPIOs are retained ONLY if SW option ***GPIO Keep*** is set; else – shall be set to Hi-Z state.
- Oscillator – powered down with global analog PD (power-down) signal.
- PLLs – powered down with PD, FOUTVCOPD, and FOUTPOSTDIVPD signals.
- OTP – power gated.
- LVDS – powered down.

7.2 nSLEEP control pin

The nSLEEP (Note) signal sets the FPGA Core into a low-power mode while retaining the memory state of the FPGA Core. The OSC and PLL are disabled during this time. While nSLEEP is LOW and nRST is HIGH, the GPIO pins which are set as outputs also retain their logic state.

Note: Depending on ***nSLEEP Signal Source*** option value - transition to **Sleep Mode** can be triggered from nSLEEP pin or from iob_sleep_start. In later case nSLEEP pin behaves as digital input.

When the SLG47920/SLG47921 is in **Functional Mode**, it will check if nSLEEP = HIGH. When nSLEEP goes LOW, the SLG47920/SLG47921 will transit to **Sleep mode**. In this mode the SLG47920/SLG47921 will be in following state:

- FPGA Core – in low power state.
- FPGA Core distributed memory is retained.
- BRAM is retained.
- GPIOs are retained.
- Oscillator – powered down with global analog PD (power-down) signal.
- PLL – powered down with PD, FOUTVCOPD, and FOUTPOSTDIVPD signals.

When in **Sleep mode** and nSLEEP goes HIGH – the device will return to **Functional Mode**.

7.3 Power-up and Configuration Sequence

This section describes sequence during power-up and nRST (PWR) or nSLEEP (EN) assertion.

The general sequence is shown in Figure 35.

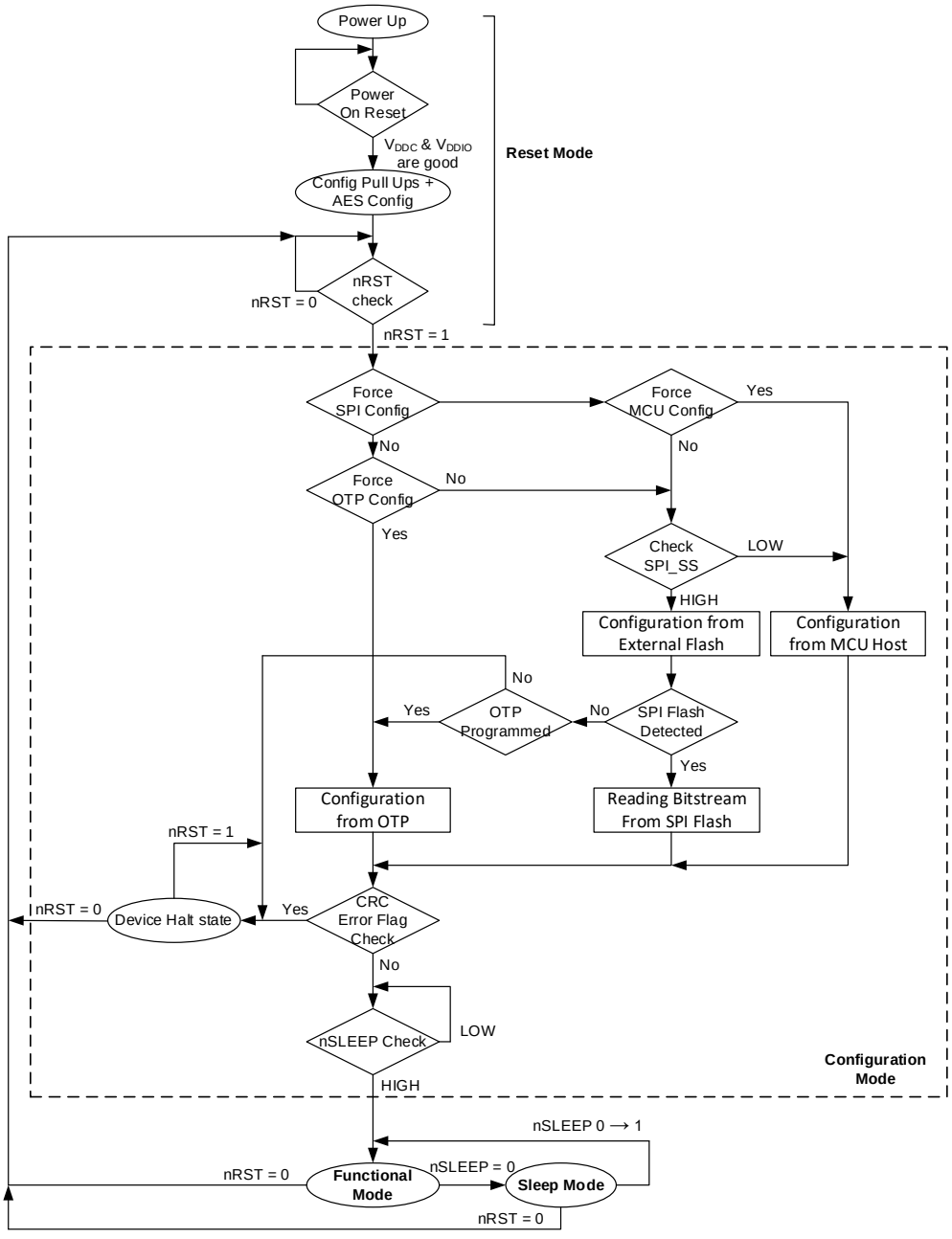


Figure 35. Power-Up Sequence

As the SLG47920/SLG47921 powers up through the V_{DDC}/V_{DDIO} pins, it checks for the state of these voltages. When both voltages are above the threshold then the global reset is removed, and devices starts operation. Specification of the Power-on Reset are given in section 3.5.6 Power-On Reset Specifications.

After POR reset is de-asserted – pull-up control registers set by ***CONFIG Pull Up*** and decryption setting set by ***AES128 Config*** are read and applied. This is done irrespective of the nRST state.

The next step is to check the nRST (PWR) pin state. If nRST = 0, the device stays in its lowest powered state. When nRST = 1, the device transitions to **Configuration Mode**.

Available configuration methods are described in section 10 Configuration Modes.

In **Configuration Mode** there is a hierarchical conditions check to define in which mode to boot:

- Check if device is forced to boot in SPI mode (Note)
  - "YES": Check if device is forced to boot from MCU
    - "YES": Proceed to boot in MCU Target Configuration Mode
    - "NO": Check SPI_CS state to decide which SPI boot mode to use
      - "LOW": Proceed to boot in MCU Target Configuration Mode
      - "HIGH": Proceed to boot in QSPI Controller Configuration Mode
  - "NO": Check if device is forced to boot from OTP
    - "YES": Proceed to boot in OTP Configuration Mode
    - "NO": Check SPI_CS state to decide which SPI boot mode to use
      - "LOW": Proceed to boot in MCU Target Configuration Mode
      - "HIGH": Proceed to boot in QSPI Controller Configuration Mode.

Note: Having boot from SPI higher priority than boot from OTP allows to override boot method if OTP boot was already forced. It can be done by constantly forcing SPI boot method with ***Boot Priority = "Force SPI boot"*** SW option or with dedicated IOB **boot_ctrl_force_spi_boot**. The later option allows to manage boot method dynamically (for ex., use OTP bitstream as bootloader configuration, then force SPI boot and utilize Boot Control (see section 10 Configuration Modes) to select required bitstream from external Flash).

In QSPI Controller Configuration mode the device will first try to read SyncWord (synchronization word to make sure read data are SLG47920/SLG47921 bitstream) from external Flash and only then proceed to bitstream reading. In case of SyncWord read fail – it will repeat attempt 5 more times, and if all of them are fails – it would be considered that external Flash is absent. In this case – the device would try to boot from OTP. If OTP happens to be unprogrammed in this case – the device will go to **Device Halt state**. In this state the device powers down all its' modules to reduce power consumption and keeps GPIOs in state that preceded this state. To exit this state it is required to set nRST = LOW.

During configuration in either of available modes – bitstream CRC checks is performed. After configuration process completion – resulting CRC Error Flag is checked:

- If no CRC Error – proceed to nSLEEP state check
  - nSLEEP = LOW: halt in current state until it is set HIGH (allows to postpone transition to **Functional Mode**).
  - nSLEEP = HIGH: transit to **Functional Mode**.
- If CRC Error is present – go to **Device Halt state**.

Dedicated signal **FPGA_CONFIG_READY** (dedicated IOB) indicates when FPGA Core has been configured. It goes HIGH before entering **Functional mode**. The **FPGA_CONFIG_READY** signal can be used as reset or enable signal for user logic. This signal is set low only upon re-configuration process.

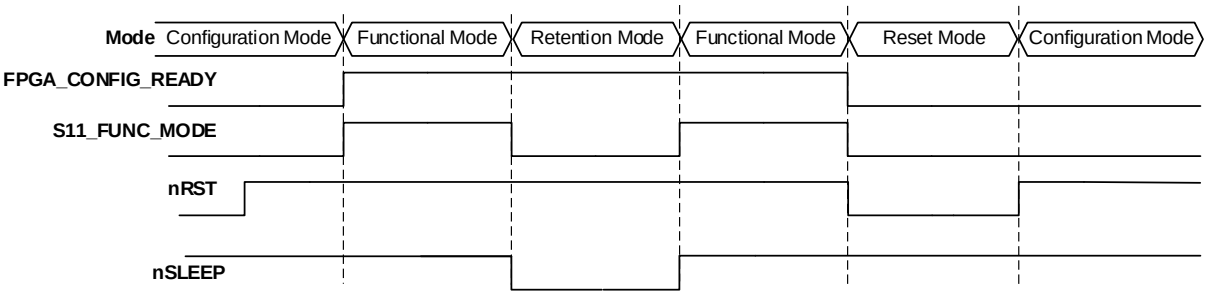


Figure 36. Dedicated Signals Behavior

When **Configuration Mode** is completed successfully the device transits to **Functional Mode** where user-configured logic becomes active and GPIOs are switched to the modes defined by user bitstream.

Configuration Mode cannot be interrupted at any time. nRST = 0 will be processed after configuration is completed with error (to be able to restart config process) or before entering **Functional Mode** after successful configuration. This results in transition to **Reset Mode**.

When in **Functional Mode** – dedicated signal **S11_FUNC_MODE** (dedicated IOB) is set HIGH, user configured logic is active, and controls chip behaviour.

Functional Mode can be interrupted in two ways: nRST (PWR) or nSLEEP (EN) assertion.

If nRST = 1 and nSLEEP = 0, the chip transitions to **Sleep Mode** (see details above).

Note: If while in Sleep Mode nRST is set LOW – the device will transit to **Reset Mode**.

When a rising edge is detected on the nSLEEP (EN) pin – the device transitions back to **Functional Mode**: no reconfiguration needed, and the internal states of the FPGA Core and BRAMs are restored. User configured logic continues operation. The minimal nSLEEP (EN) low-pulse duration should be 45 µs (if OSC was ON in Functional mode) or 300 µs (if OSC was OFF in Functional mode)

If nRST = 0, the device transits to its initial state after POR – **Reset Mode** (see details above).

When a HIGH level is detected on the nRST (PWR) pin the device proceeds to **Configuration Mode**. In this case the FPGA Core is re-configured and its previous internal states are not restored. Whenever nRST or nSLEEP is set LOW – to transition from **Functional mode** to **Sleep Mode** (or **Reset Mode**) it is required to wait until all user clocks are stopped. This requires two falling edges of the respective clock or a 5 µs delay (Note) (in case the clock is very slow and the time to get two falling edges is greater than this delay) after which all user clocks are forced into a LOW state anyway.

Note: This delay can be disabled by selecting corresponding value of ***5us Timeout Disable*** SW option.

Figure 37 depicts general behaviour during nRST (PWR) and nSLEEP (EN) assertion.

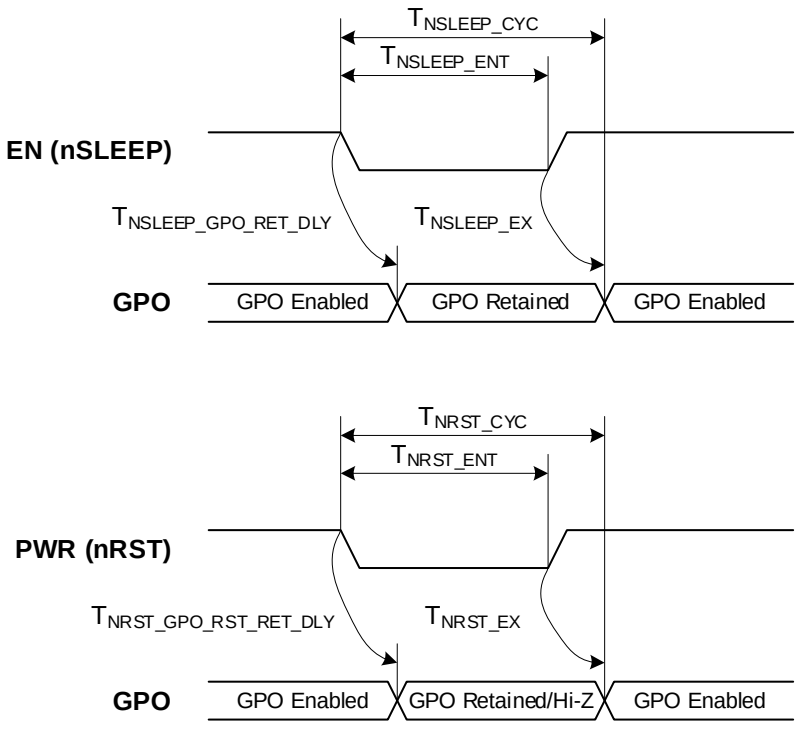


Figure 37. Device On/Off State Cycle Timing Diagram (PWR/EN Pin)

Note:

1. When nRST (PWR) = 0 and nSLEEP (EN) = X – GPIO is Hi-Z (unless SW option ***GPIO Keep*** = "***Enable***") state and BRAM content is not retained (unless SW option ***BRAM Keep*** = "***Enable***" for specific BRAM instance).
2. When nRST (PWR) = 1 and nSLEEP (EN) = 0 – device is in Sleep Mode, GPIO and the data are retained.
3. When nRST (PWR) = 1 and nSLEEP (EN) = 1 – device is in Functional Mode, GPIOs and BRAMs operate under user configured logic control.
4. Refer to section 3.5.11 nRST (PWR) and nSLEEP (EN) Specifications for the nRST (PWR) and nSLEEP (EN) Power Down and Sleep Characteristics.

Table 12 gives information on state of different modules in different operating modes.

Table 12. State of Modules in Different Chip Modes

Mode	Module					
	FPGA Core	**BRAM**	**OSC**	**PLLs**	**GPIO**	**User logic**
Configuration	Reconfiguration	Reconfiguration	Reconfiguration	Reconfiguration	(Hi-Z or Pull-up or Retained) [1] or Config Pins [2]	Reconfiguration
Functional	Operation	Operation [1]	Operation [1]	Operation [1]	Operation	Operation
Sleep	Retained, Power-gated [3]	Retained	Power Down	Power Down	Retained	Retained
Reset	Not retained, Power-gated [3]	Retained or Not retained [4]	Power Down	Power Down	Retained or Hi-Z [5]	Not retained

[1] Depends on user configuration.

[2] Pins used for configuration process are overridden in Configuration Mode and are not controlled in accordance with user configuration.

[3] Power-gated means that power is cut off from the FPGA Core, but internal states might be retained (and later restored) or not retained (and reconfiguration required) – this depends on mode.

[4] Depends on the value of BRAM Keep SW option.

[5] Depends on the value of GPIO Keep SW option.

8. LVDS Support

SLG47920/SLG47921 supports LVDS based applications. For this purpose, part of GPIOs can be configured as LVDS Tx/Rx (see section 4.2 GPIO with LVDS Capability). Also, SoC logic has paths for data to propagate to/from these GPIOs to FPGA Core.

8.1 LVDS Input Paths

LVDS input paths are shown in Figure 38. There are three LVDS GPIO pairs, each with its own data path to the FPGA Core. Pair 0 is used to receive a differential clock (if needed).

Data from LVDS Rx goes through DDR Circuitry, which makes it possible to have unchanged serial data or have data latched at the input DFF (SDR or DDR mode). For more details see section 4.2 GPIO with LVDS Capability.

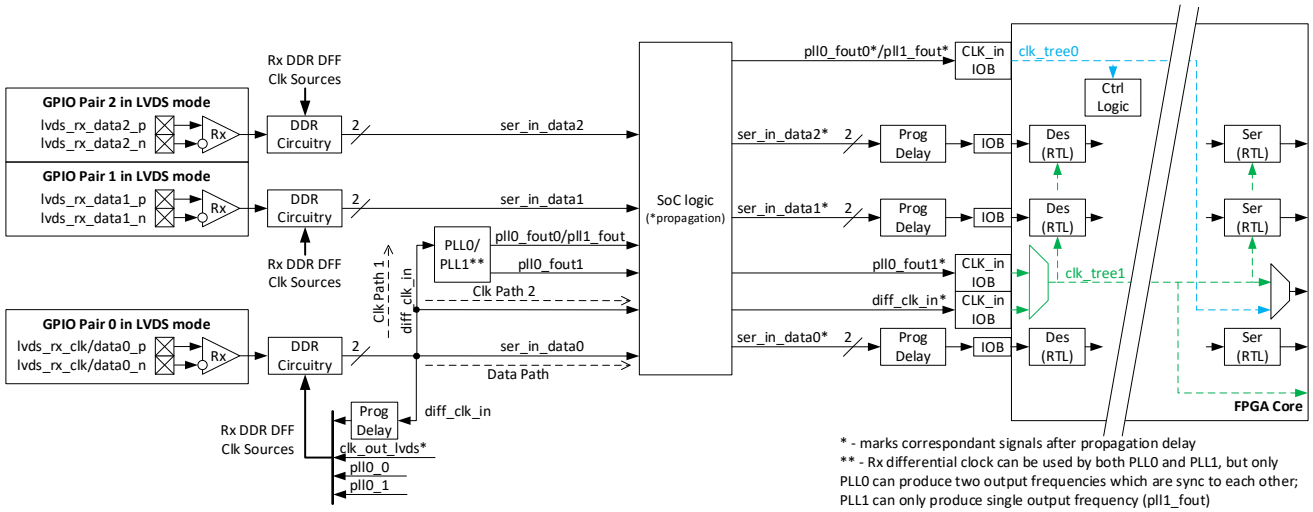


Figure 38. LVDS Input Paths

The serial data propagates through SoC logic and through Programmable Delay. This delay is required to match differential clock propagation with serial data propagation at the boundary of the FPGA Core (IOB). Value of delay is selected with ***Rx Serial Data Path Delay***.

Therefore, serial data can be de-serialized in the FPGA Core for further processing. Deserialization should be implemented by user logic.

In case the Rx Differential Clock is received by LVDS Pair 0, there are two possible paths for it to propagate to the FPGA Core:

Clock Path 1: Differential clock → PLL0 or PLL1 → 1-2 output clocks → FPGA Core.

In this case the differential clock is used as the PLL reference clock. In its turn, PLL produces up to two clocks (Note 1) (in phase with each other) which further are used within the FPGA Core to clock user logic. Also, the PLL0 output clocks are used to clock DDR Circuitry. PLL0 output frequencies have predictable phase shift relative to reference clock (see section 6.3.2.3 External Post Divider Clock Phase Shift).

Note 1: Only PLL0 can produce two in-phase clocks; PLL1 can only produce one clock, for which alignment to the reference clock is not guaranteed – so, it can be used only to synthesize clock from Rx Differential Clock but can not provide alignment to it.

As the PLL incurs additional latency of the clock, which is further increased by clock network latency – Programmable delay (Note 2) might be used to match clock latency with serial data latency at the FPGA Core IOB.

Note 2: Max delay value (at TT corner) is up to delay_max = 10 ns; number of steps: 32 (including zero-delay). Delay has balanced rise/fall times.

Clock Path 2: Differential clock → FPGA Core.

In this case the differential clock is directly fed into FPGA Core to clock user logic. This is the shortest path with minimal clock latency. It requires to use not Global Clock MUXes outputs, but dedicated clock IOB called LVDS_RX_CLK (see section 6.1 Clock Network).

Note 3: In this case it is expected that clock path latency is matched with serial data latency by default, thus Programmable delay is not required to be used.

DDR Circuitry input DFFs are clocked with a selectable set of clocks (depending on actual use case). Differential input clock paths to the DDR DFFs have programmable delay to be able to shift clock edge relative to data edge (if it is not shifted by transmitter) to reliably latch data.

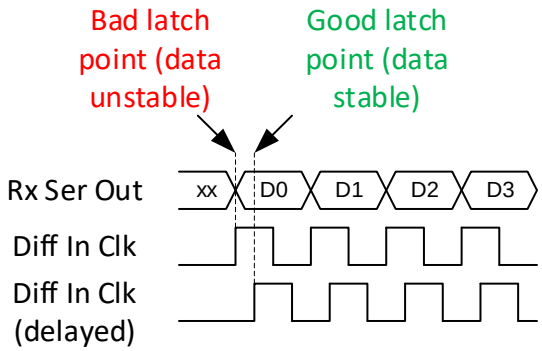


Figure 39. Delayed Input Differential Clock Usage

Note 4: Max delay value (at TT corner) is expected to be up to clock period at max data rate: at 100Mbps clk_period = 10 ns → delay_max = 10 ns; number of steps: 32 (including zero-delay).

8.2 LVDS Output Paths

LVDS Output Paths are shown in Figure 40. There are three LVDS GPIO pairs, each with its own data path from the FPGA Core. Pair 0 is also used to transmit a differential clock (if needed).

First, data is serialized by user logic inside FPGA Core. Further data is output through IOBs. Data from the FPGA Core goes through SoC logic and further through DDR Circuitry, which allows for unchanged serial data or latched data at the output DFF (SDR or DDR mode). For more details see section 4.2 GPIO with LVDS Capability.

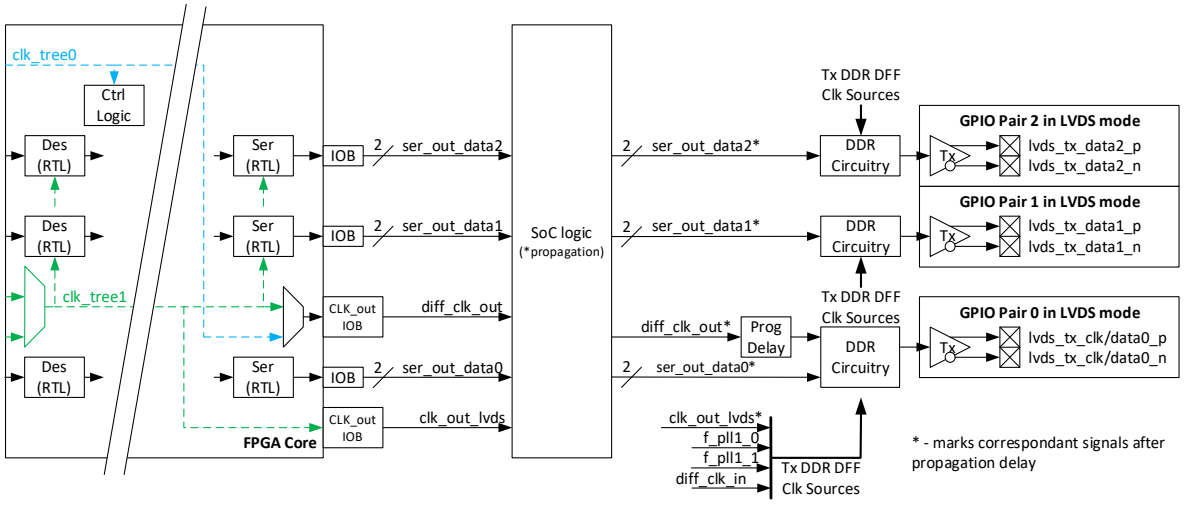


Figure 40. LVDS Output Paths

After DDR circuitry, data is transmitted by LVDS Tx. Data transmission rate depends on the DDR Circuitry configuration used:

- For Serial data or DDR DFF mode (rise or fall) – the data rate is equal to the serializer clock rate.
- For DDR DFF mode – the data rate is 2x of the serialized clock rate.

Note 1: In DDR mode the serializer should produce two bits per clock, each of which would be separately latched by DDR circuitry at its respective clock edge.

DDR circuitry output DFFs can be clocked with a selectable set of clocks (depending on actual use cases).

In the case where a differential clock is required to be transmitted – LVDS Pair 0 has such an option. The differential output clock and the DDR clock (clk_out_lvds) might be the same clock (if clock of the data rate is transmitted) or might be different clocks (in case when transmitted differential clock is of lower frequency than the data rate).

The differential output clock path LVDS Tx has programmable delay to shift the clock edge relative to the data edge – it might be needed to achieve the differential clock at the Rx side to be shifted relative to data.

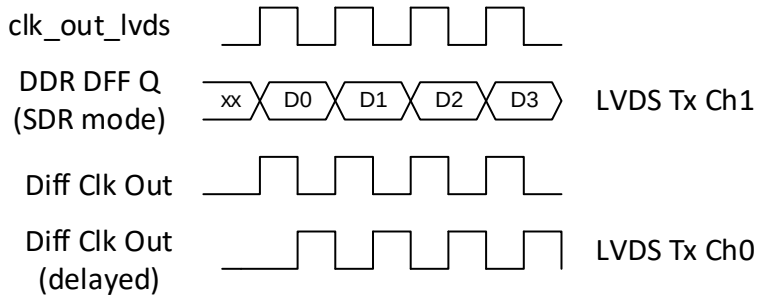


Figure 41. Delayed Output Differential Clock Usage

This is required to align the clock edge with valid data, to simplify processing on the receiving side.

Note 2: For the shown example to operate correctly, propagation delays of clk_out_lvds and diff_clk_out should be matched, and delay should happen relative to moment of data latching at the DFFs.

Note 3: Max delay value (at TT corner) is expected to be up to clock period at max data rate: at100Mbps clk_period = 10 ns → delay_max = 10 ns; number of steps: 32 (including zero-delay).

8.3 LVDS Use Cases

The main use cases for LVDS applications include the following:

LVDS Controller side

In this case the Device is expected to be the source of all LVDS-related clocks. It is expected to use PLL0 to generate up to two in-phase clocks – for Control Logic (low frequency) and another for Ser/Des Logic (high frequency).

The device might transmit the differential clock simultaneously with data. DDR Circuits (if used) are expected to be clocked with high frequency clock.

Input and Output LVDS data are sampled with the high frequency clock.

LVDS Target side

In this case the Device is expected to receive a differential clock to be used for input/output data sampling. This clock can be used directly by Ser/Des logic or as reference clock for PLL0 to generate clocks for user logic.

Input and Output LVDS data are sampled with a differential clock or PLL0 clock (which is derived from the differential clock).

Absence of a differential clock might be acceptable only for cases when the data rate is low enough so that the PLL0 generated clock difference and drift does not compromise receiving data. These cases are highly dependent on implementation and might require external high stability clock source, specific synchronization methods and others.

9. Block RAM (BRAM)

The SLG47920/SLG47921 contains 64 kb of 2-port Embedded Block RAM that is connected directly to the FPGA cores. The diagram below highlights the IOBs that are reserved for interfacing with the BRAM. The BRAM configuration will take the majority of IOB connections within the device, including the entire top and bottom row of the design.

Key aspects of BRAM:

- 4 x 4kbit SRAM 2-port memory slices per BRAM instance.
- Selectable ratio (data/addresses): 8 x 512, 4 x 1024, 2 x 2048, 1 x 4096.
- Read/write interface enable signals for pair of slices.
- Read/Write clock enable signals for each slice.
- Read/Write clock inversion signals (to define if read/write is performed on rising or falling edge of clock) for each slice.
- Deep-sleep function for each slice disables logic, but retains power (and therefore content) for SRAM itself.
- SRAM slices isolation from control logic with dedicated control signal.
- Power-gating: for maximum power saving disables power to all SRAM slices, thus – data are lost.
- BRAM content initialization.

Power-gating (PG) of BRAMs is controlled by ***BRAM Power*** option in SW. Each BRAM instance is connected to the FPGA Core as follows:

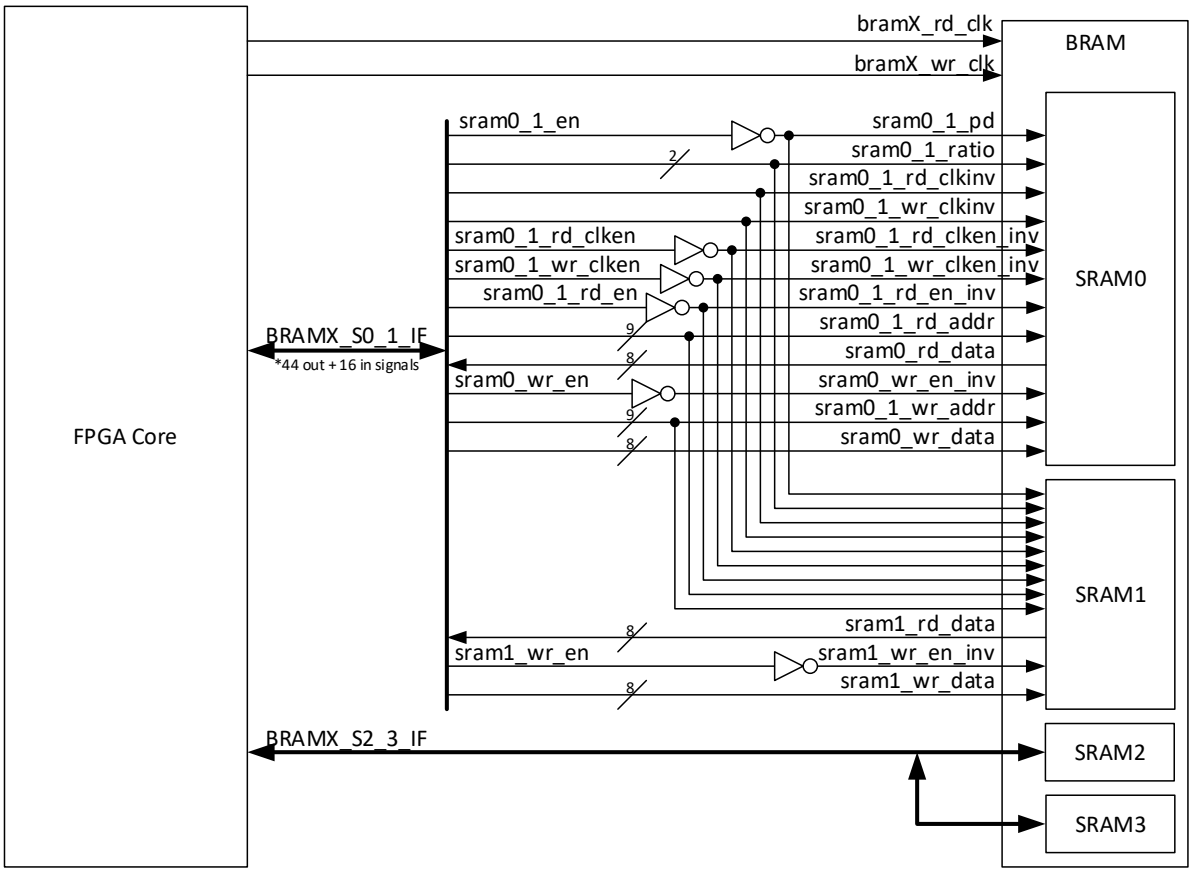


Figure 42. BRAM Connections

Each pair of SRAM slices shares most of their signals, except write enable, write data, and read data. Thus, minimal used amount of BRAM memory is 8kbit.

Read/write enable, read/write clock enable, and PD (power-down) signals are inverted at SoC level. This provides a HIGH-active level from user logic side, while at SRAM level it is a LOW-active level.

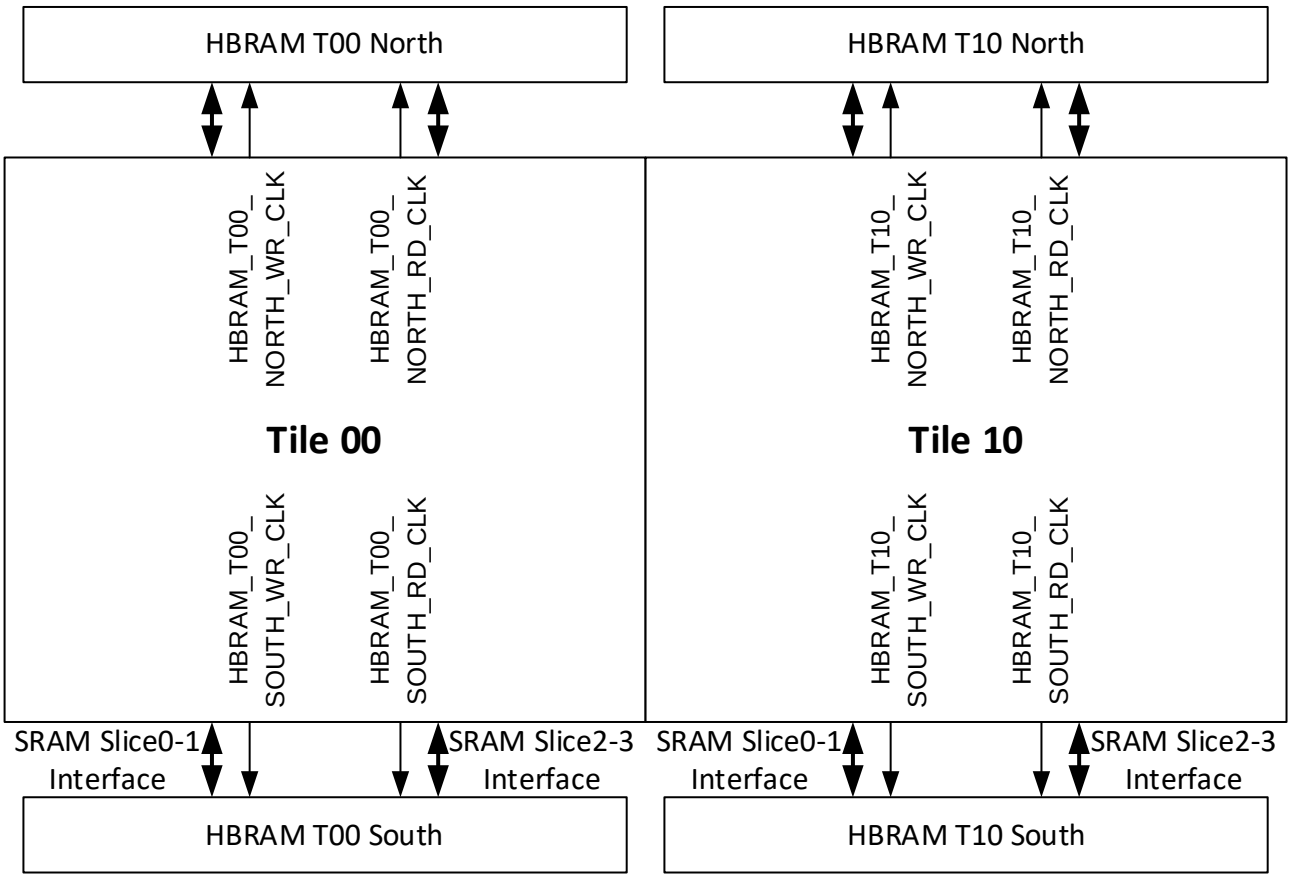


Figure 43. Embedded Block RAM

9.1 BRAM Instance

The SLG47920/SLG47921 64 kb of BRAM is divided into four individual 16 kbit blocks, each of which is further broken down into 4 kb (512 x 8) slices. Each 4 kb slice provides its own set of IOB connections to the core, allowing for individual access to any slice. Each slice may also be configured to contain either an 8, 4, 2, or 1-bit data width.

Single BRAM will provide the following operation modes:

- **Normal operation mode**: 4 slices of 4 kbit SRAM with customizable ratio (data width and address depth combination).
- **Initialization mode:** each BRAM instance will be able to be initialized with pre-defined content provided in the configuration data.
- **Sleep mode (power-down mode):** each SRAM slice can be set in low-power mode with ability to retain its content.
- **Power-gated mode**: each BRAM instance can be set completely disconnected from power supply to cut power consumption as much as possible; in this mode memory content should not be retained.

Users access each BRAM through set of following ports:

Table 13. BRAM Ports

Name	Direction	Description
HBRAM_TXX_SOUTH/NORTH _WR_CLK	Input	Reference Write Clock (common for all 4 slices).
HBRAM_TXX_SOUTH/NORTH_RD_CLK	Input	Reference Read Clock (common for all 4 slices).
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_EN	Input	Slices 0 and 1 Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_RATIO[1:0]	Input	Slices 0 and 1 Data Bus Width Selection Bits. 00: 512 x 8 01: 1024 x 4 10: 2048 x 2 11: 4096 x 1
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_WR_CLKEN	Input	Slices 0 and 1 Write Clock Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_WR_CLKINV	Input	Slices 0 and 1 Write Clock Inversion Control (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM0_WR_EN	Input	Slice 0 Write Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM1_WR_EN	Input	Slice 1 Write Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH _SRAM0_1_WR_ADDR[8:0]	Input	Slices 0 and 1 Write Address Bus. For anything deeper than 512, the unused DINs can be repurposed as WADDR (see section 9.3 Address Extension).
HBRAM_TXX_SOUTH/NORTH_SRAM0_WR_DATA[7:0]	Input	Slice 0 Write Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM1_WR_DATA[7:0]	Input	Slice 1 Write Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_RD_CLKEN	Input	Slices 0 and 1 Read Clock Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_RD_CLKINV	Input	Slices 0 and 1 Read Clock Inversion Control (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_RD_EN	Input	Slices 0 and 1 Read Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM0_1_RD_ADDR[8:0]	Input	Slices 0 and 1 Read Address Bus. For anything deeper than 512, the unused DINs can be repurposed as RADDR (see section 9.3 Address Extension).
HBRAM_TXX_SOUTH/NORTH_SRAM0_RD_DATA[7:0]	Output	Slice 0 Read Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM1_RD_DATA[7:0]	Output	Slice 1 Read Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_EN	Input	Slices 2 and 3 Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_RATIO[1:0]	Input	Slices 2 and 3 Data Bus Width Selection Bits. 00: 512 x 8 01: 1024 x 4 10: 2048 x 2 11: 4096 x 1
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_WR_CLKEN	Input	Slices 2 and 3 Write Clock Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_WR_CLKINV	Input	Slices 2 and 3 Write Clock Inversion Control (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_WR_EN	Input	Slice 2 Write Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM3_WR_EN	Input	Slice 3 Write Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_WR_ADDR[8:0]	Input	Slices 2 and 3 Write Address Bus. For anything deeper than 512, the unused DINs can be repurposed as WADDR (see section 9.3 Address Extension).

Name	Direction	Description
HBRAM_TXX_SOUTH/NORTH_SRAM2_WR_DATA[7:0]	Input	Slice 2 Write Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM3_WR_DATA[7:0]	Input	Slice 3 Write Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_RD_CLKEN	Input	Slices 2 and 3 Read Clock Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_RD_CLKINV	Input	Slices 2 and 3 Read Clock Inversion Control (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_RD_EN	Input	Slices 2 and 3 Read Enable (active HIGH).
HBRAM_TXX_SOUTH/NORTH_SRAM2_3_RD_ADDR[8:0]	Input	Slices 2 and 3 Read Address Bus. For anything deeper than 512, the unused DINs can be repurposed as RADDR (see section 9.3 Address Extension).
HBRAM_TXX_SOUTH/NORTH_SRAM2_RD_DATA[7:0]	Output	Slice 2 Read Data Bus.
HBRAM_TXX_SOUTH/NORTH_SRAM3_RD_DATA[7:0]	Output	Slice 3 Read Data Bus.

9.2 BRAM Considerations

- Read Data Register is undefined immediately after configuration.

The initial value of RDATA read value is '0' during configuration. But once configured, the RDATA port does not automatically reset unlike the FFs in the Programmable Logic Blocks and Programmable IO pins.

- LOW Power Setting.

To place the BRAM block in its lowest power mode, keep WR_CLKEN = 0 and RD_CLKEN = 0. In other words, when not actively using the BRAM block, disable the clock inputs.

BRAM can be power gated with dedicated SW option ***BRAM Power*** to minimize the power consumption.

9.3 Address Extension

To accommodate the previously mentioned bit-width configurability, a method for extending the memory address beyond its native 9 bits is required. This is accomplished by utilizing specific bits of the WR_DATA byte as address extension bits. In all address extension cases, the WR_DATA bits used will represent the least significant bits of the address.

Table 14. Write Address Extension Using Bits 5-7

	WR_ADDR									WR_DATA								WR_DATA
512 x 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[7:0]
	A8	A7	A6	A5	A4	A3	A2	A1	A0									
1024 x 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[3:0]
	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								
2048 x 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[1:0]
	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0							
4096 x 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[0]
	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						

For write addressing, the WR_ADDR and WR_DATA bits are shown above for each data width.

For read addressing, the same method of address extension is used, except bits 2-4 are used instead of bits 5-7.

Table 15. Read Address Extension Using Bits 2-4

	BRAMx_RADDR									BRAMx_RDATA								RD_DATA
512 x 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[7:0]
	A8	A7	A6	A5	A4	A3	A2	A1	A0									
1024 x 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[3:0]
	A9	A8	A7	A6	A5	A4	A3	A2	A1				A0					
2048 x 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[1:0]
	A10	A9	A8	A7	A6	A5	A4	A3	A2				A1	A0				
4096 x 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[0]
	A11	A10	A9	A8	A7	A6	A5	A4	A3				A2	A1	A0			

9.3.1. Write Operations for BRAM

All write operations are synchronized to the rising edge of WR_CLK (default) when WR_CLKINV = 0; if WR_CLKINV = 1, then write operation happens on the falling edge.

To write data into the BRAM block, perform the following operations:

- Supply a valid address on the WR_ADDR [8:0] address input port.
- Supply valid data on the WR_DATA [7:0] data input port.
- Enable the BRAM write port (WR_EN = 1).
- Enable the BRAM write clock (WK_CLKEN = 1).
- Apply a rising clock edge on WR_CLK (assuming WR_CLKINV = 0).

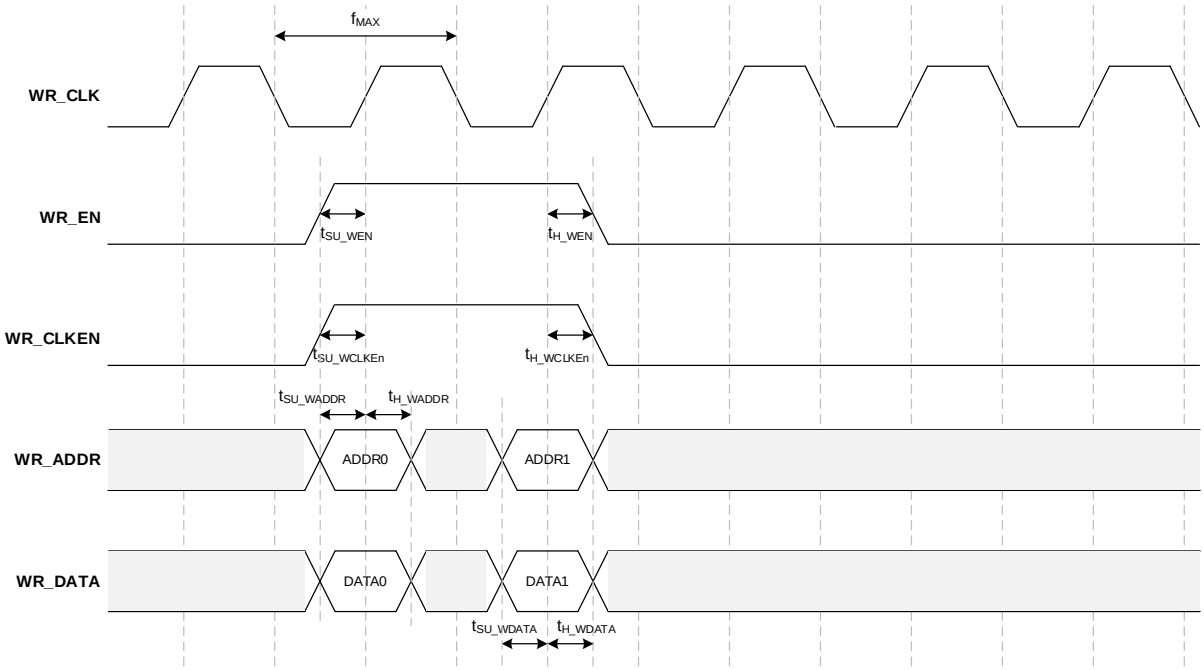


Figure 44. BRAM Write Timing Diagram

Note: Exact timing information for the diagram in not provided. Instead, Read Max Frequency and Write Max Frequency parameters provided (see section 3.5.10 BRAM Characteristics), as an aggregate parameter of all timings essential for BRAM to operate correctly.

9.3.2. Read Operation for BRAM

All read operations are synchronized to the rising edge of RD_CLK when RD_CLKINV = 0; if RD_CLKINV = 1, then read operation happens on the falling edge.

To read data from the BRAM block, perform the following operations:

- Supply a valid address on the RD_ADDR [8:0] address input port.
- Enable the BRAM read port (RD_EN = 1).
- Enable the BRAM read clock (RD_CLKEN = 1).
- Apply a rising clock edge on RD_CLK(assuming RD_CLKINV = 0).
- After the clock edge, the BRAM contents located at the specified address (RD_ADDR) appear on the RD_DATA output port.
- The read data is held when RD_EN is de-asserted.

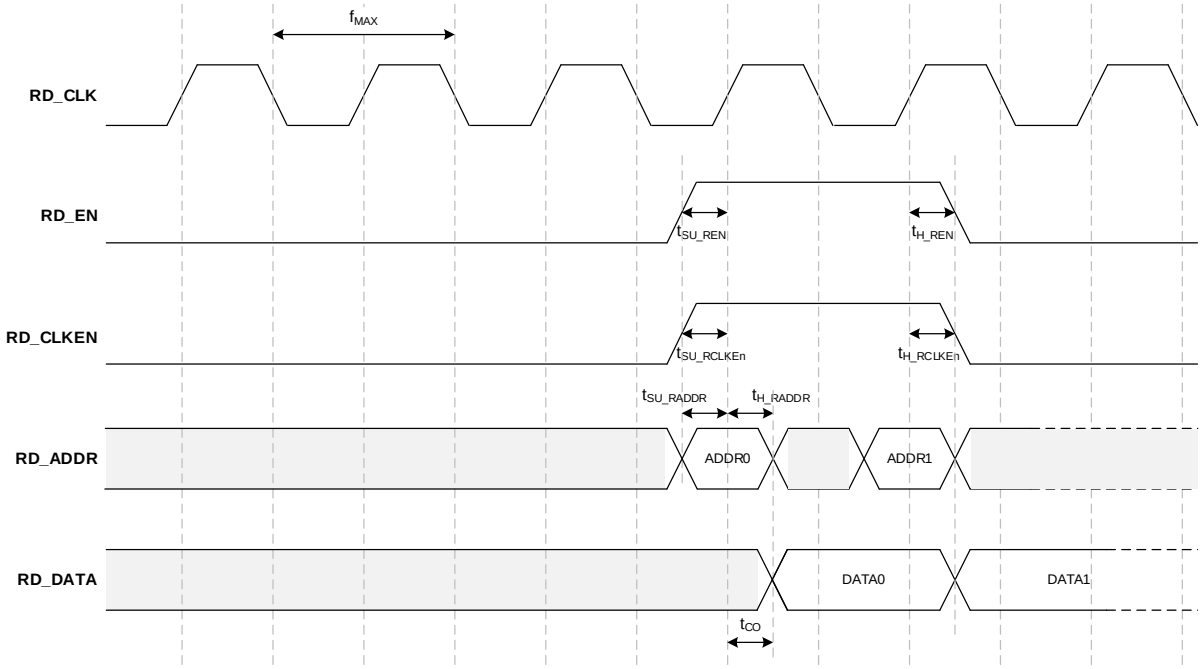


Figure 45. BRAM Read Timing Diagram

Note: Exact timing information for the diagram in not provided. Instead, Read Max Frequency and Write Max Frequency parameters provided (see section 3.5.10 BRAM Characteristics), as an aggregate parameter of all timings essential for BRAM to operate correctly.

9.4 BRAM Initialization

The BRAM Initialization allows to pre-set content of each BRAM instance. Initialization data are part of bitstream.

The initialization process for each BRAM instance will be enabled/disabled based on a set of Configuration Registers values.

The **BRAM Keep** SW option allows to keep content of each BRAM separately. Also, setting ***BRAM Initialization Mode*** to ***"Initialized disregarding of BRAM Keep value"*** forces BRAM initialization (during configuration) even if they contain kept data.

The value of ***BRAM Keep*** from the previous configuration will be stored separately to be taken into account during initialization, while ***BRAM Keep*** from a new configuration will influence BRAM data retention during next transition into **Reset mode**.

BRAM initialization logic is described in Table 16.

Table 16. BRAM Initialization

BRAM Initialization Mode	BRAM Keep [X] from Previous Configuration	Action
Initialize only if BRAM Keep disabled	Disable	BRAM_X content is initialized during configuration.
	Enable	BRAM_X content is NOT initialized during configuration and data from previous configuration are retained.
Initialized disregarding of BRAM Keep value	x	BRAM_X content is initialized during configuration and data from previous configuration (if were kept) is overwritten.

This separate initialization control for each BRAM instance allows data to be kept from previous configurations in one instance, while having initial data defined by new configuration in other instances.

10. Configuration Modes

An internal configuration wrapper is used to configure SLG47920/SLG47921 FPGA Core. The GoConfigure software is used to generate the bitstream. The configuration can be performed using three different configuration bitstream sources:

1. External SPI Flash (SPI Controller Mode)

In this mode the SLG47920/SLG47921 is the SPI Controller and the external SPI Flash is the SPI Target. During SPI mode, GPIO1 is used to output the SPI_SCLK. GPIO0, GPIO2, and GPIO3 are used as SPI_CS, SPI_SI and SPI_SO respectively. To enter SPI Controller mode, the SPI_CS line should be HIGH when the chip configuration process starts. SW option ***QSPI Mode*** allows to select between ***"Single mode"*** or ***"Dual mode"*** modes.

2. MCU as a host (SPI Target Mode)

In this mode the SLG47920/SLG47921 is the SPI Target and a connected MCU is the SPI Controller. During SPI mode, GPIO1 is used to input the SPI_SCLK. GPIO0, GPIO2, and GPIO3 are used as SPI_CS, SPI_SI, and SPI_SO respectively. To enter MCU Target mode, the SPI_CS line should be LOW when the chip configuration process starts.

3. Internal One Time Programmable memory (OTP Mode)

In this mode, the configuration for the FPGA is stored in the One Time Programmable (OTP) Non-Volatile Memory (NVM). The FPGA core is configured by reading the bitstream from OTP memory. To enter OTP mode, the SW option ***Boot Priority*** should be set to ***"Force boot From OTP"*** and OTP Only Registers programmed to OTP before configuration process starts.

For more information on details of configuration process, refer to the ForgeFPGA Configuration Guide.

The FPGA Core has a configuration interface that can be configured three ways with user logic (see Figure 46).

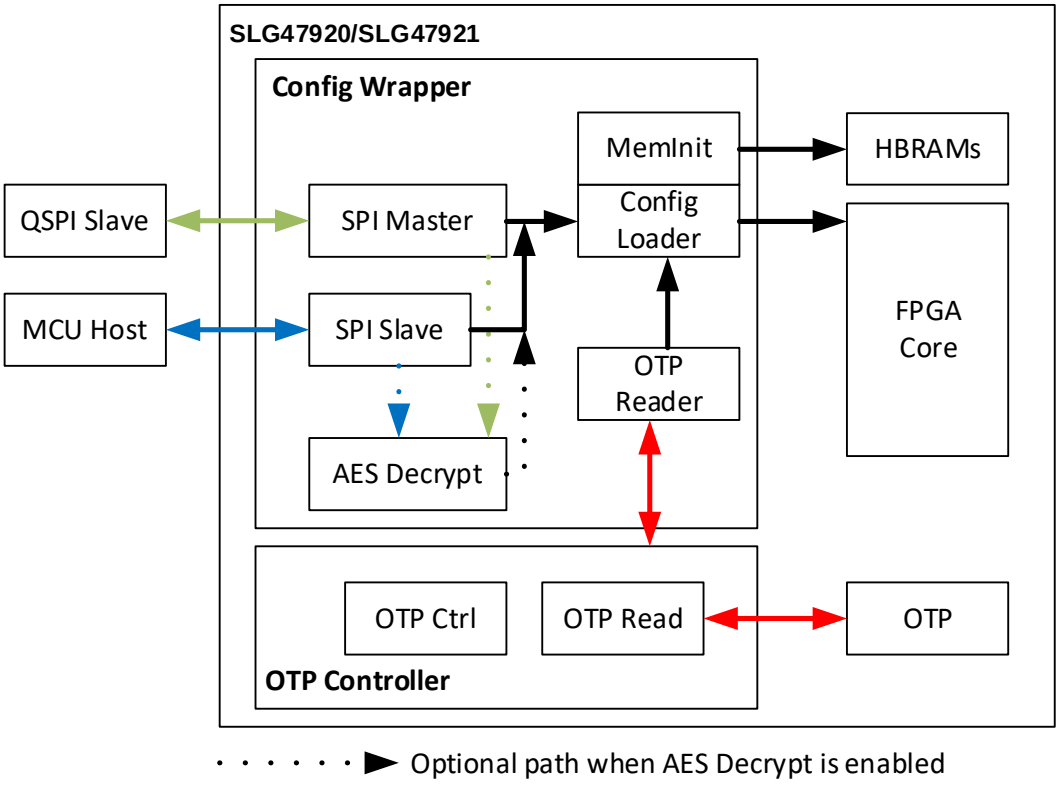


Figure 46. FPGA Core Configuration Paths

Configuration Done Indication

GPIO3 is used to perform indication if configuration was completed successfully or not (indication is available for all modes, but in OTP mode it is optional – controlled with state of nSLEEP pin at OTP Mode configuration process start). For more information refer to the ForgeFPGA Configuration Guide.

AES Decryption

To secure the bitstream content, which is used to boot through SPI, bitstream might be encrypted with AES128 algorithm. This option is enabled in ***AES128 Config*** block in SW. It includes following parameters: ***AES Enable*** – enables/disables AES128 encryption of bitstream in SW and enables AES128 decryption in SLG47920/SLG47921; ***AES128 Key*** and ***AES128 Init Vector*** – parameters used for encryption/decryption process. Separate encrypted bitstream file would be generated. For decryption process to be enabled in SLG47920/SLG47921– OTP Only Registers required to be written into OTP.

Boot Control

Boot Control feature allows user to control the start address of bitstream read process in SPI Controller mode. This allows to have up to 16 different bitstreams stored in external Flash memory and to be accessed by SLG47920/SLG47921 as needed. For this purpose, GPIOs 12-15 (or dedicated IOBs) are used as select address.

To enable this feature – ***QSPI Boot Control Logic*** option in SW should be set to "***Enable***".

Each bit of selection can be enabled or disabled (considered to be 0) by ***QSPI BOOT Control Code Selection → BIT*** option in SW, as well as its source can be selected (GPIO or IOB (Note)) with ***QSPI BOOT Control Code Selection → GPIO/IOB*** option. External Flash memory Start Adress values for each control code value are defined with ***QSPI BOOT Control Code Selection → Control Code + QSPI Boot Address*** option (24-bit addresses).

Note: GPIO controls are applicable for first and all consecutive boots. IOB controls are applied only starting from second boot after nRST has been applied.

OTP Read/Write Protection

To secure the bitstream content stored in OTP from unauthorized access – OTP content access might be limited for reading or writing. SW option ***Lock Status*** provide user ability to lock OTP reading or writing (or both).

Secondary Path for MCU Boot

For engineering purposes there is secondary path for MCU boot method, that allows override boot method even if OTP boot method is forced. User can block this path with SW option ***Secondary path for MCU boot = "Locked"***. But it limits abilities for future analysis in case of device failure.

Recommended SPI Flash Memory

SLG47920/SLG47921 requires 769 kbit to store bitstream. Recommended type of Flash memory is for this purpose is:

AT25EU0011A: 1-Mbit, Ultra-Low Energy Serial Flash Memory.

If **Boot Control** mechanism is used to switch between multiple configurations or configuration storage device is shared with other data, bigger devices can be used (see Table 17).

Table 17. Recommended Flash Memory Devices

Part number	Size	SPI Interface	SOIC 150 mil	SOIC 208 mil	UDFN 2x3 mm	WLCSP
AT25EU0011A	1 Mbit	Up to QSPI	●		●	
AT25EU0021A	2 Mbit	Up to QSPI	●		●	
AT25EU0041A	4 Mbit	Up to QSPI	●		●	
AT25EU0081A	8 Mbit	Up to QSPI	●	●	●	
AT25EU0161A	16 Mbit	Up to QSPI	●	●	●	● [1]

[1] Contact Renesas.

11. Package Information

11.1 Package Outline Drawings

11.1.1. LQFN 40L (5.0 mm x 5.0 mm x 0.85 mm, 0.4P) WB

JEDEC MO-220

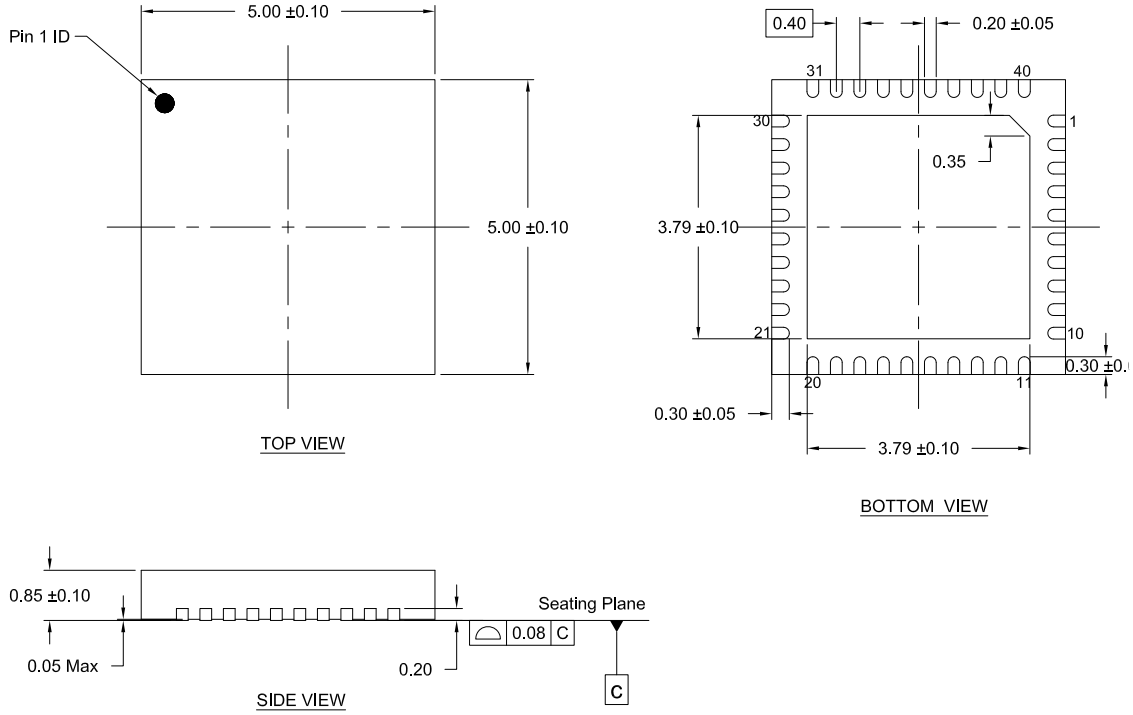


Figure 47. Package Outlines Drawing LQFN-40

11.1.2. LQFN 48L (6.0 mm x 6.0 mm x 0.85 mm, 0.4P) WB

JEDEC MO-220

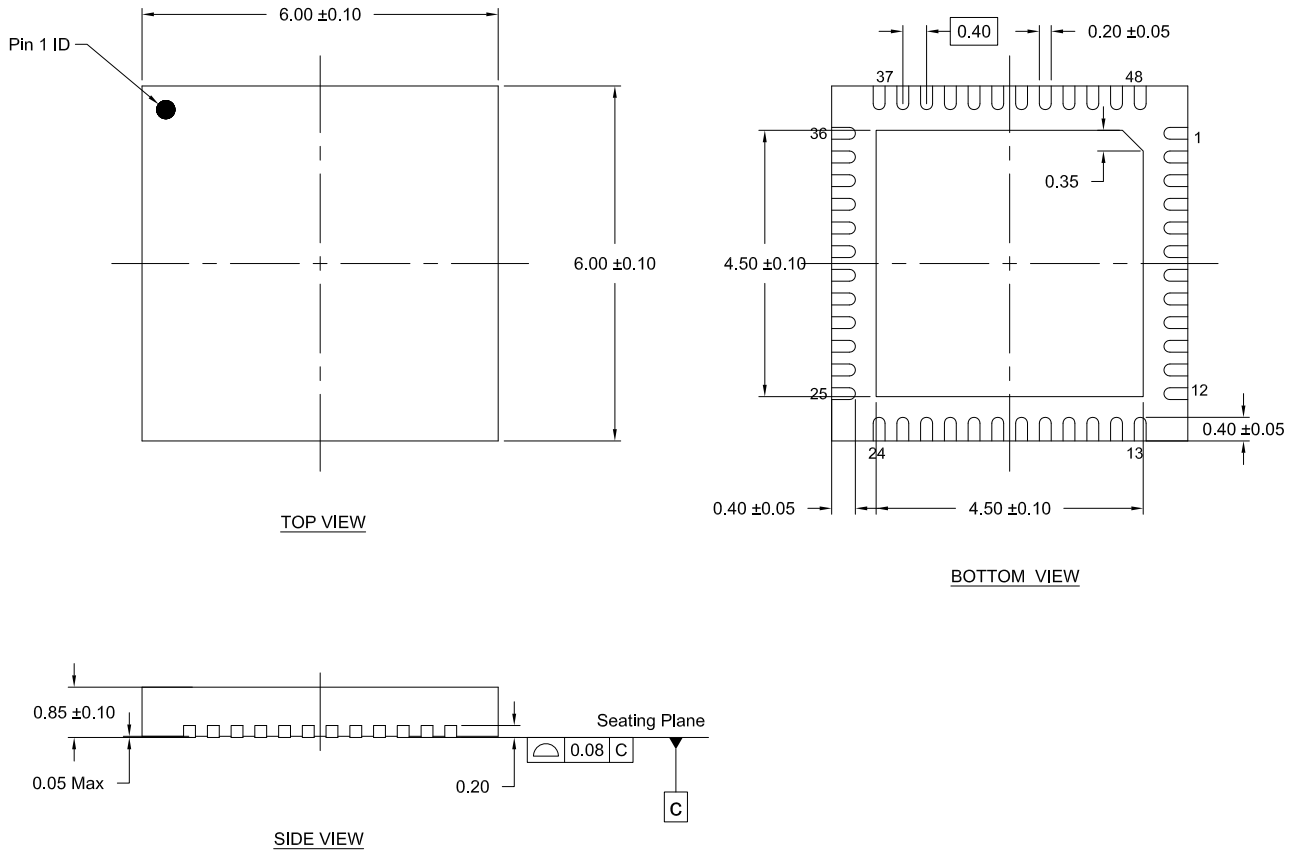


Figure 48. Package Outlines Drawing LQFN-48

11.1.3. WLCSP 48L (3.241 mm x 2.575 mm x 0.495 mm, 0.35P)

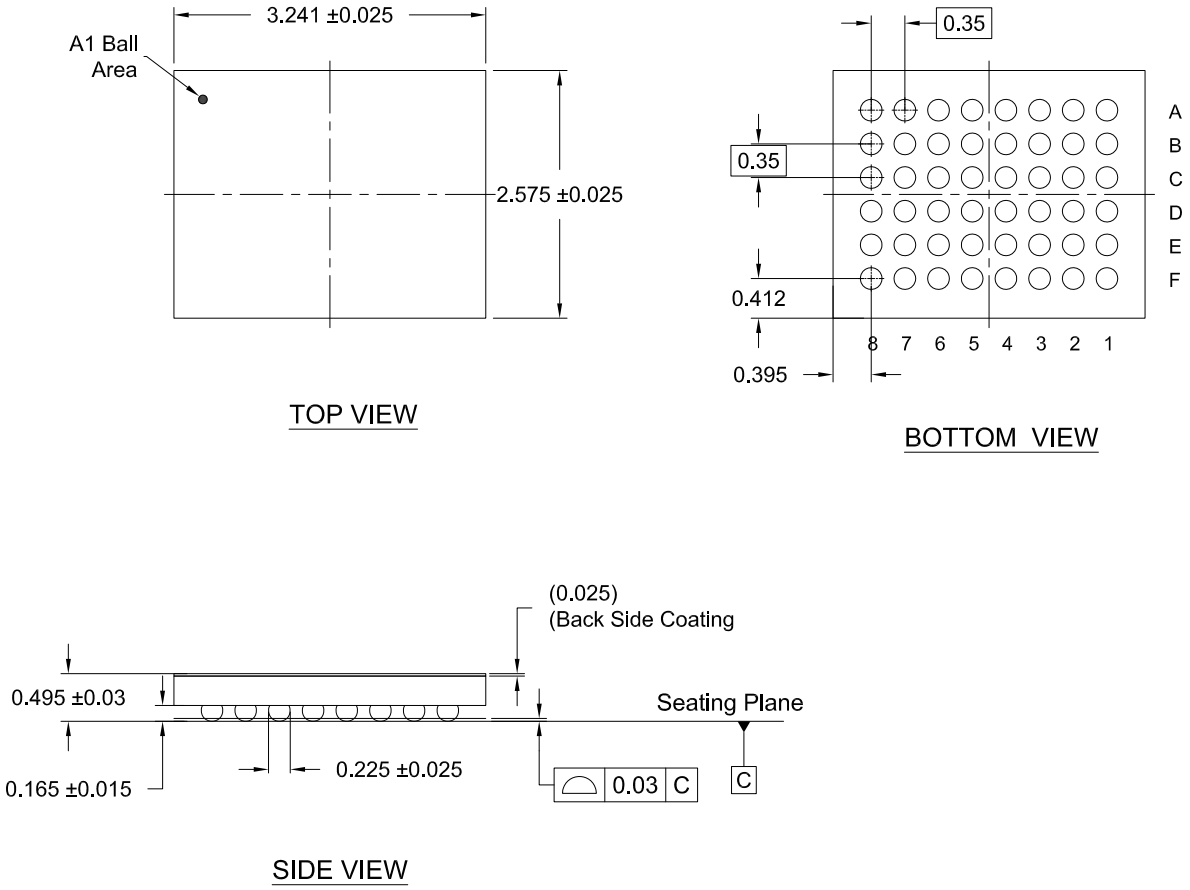


Figure 49. Package Outline Drawing WLCSP-48

11.2 Package Top Marking

11.2.1. LQFN 40L (5.0 mm x 5.0 mm x 0.85 mm, 0.4P) WB

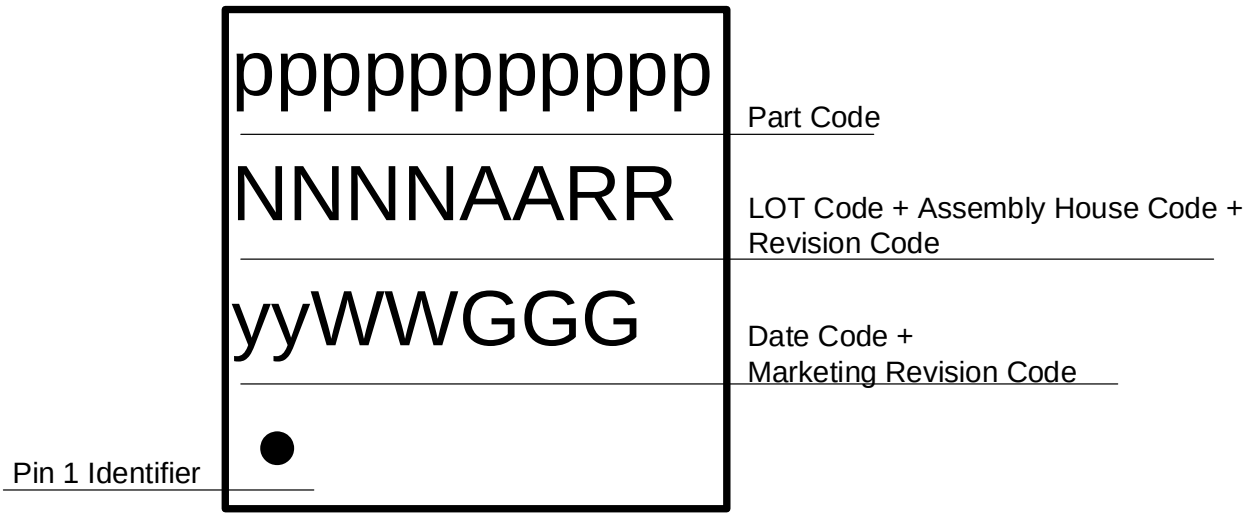


Figure 50. Package Top Marking LQFN-40

11.2.2. LQFN 48L (6.0 mm x 6.0 mm x 0.85 mm, 0.4P) WB

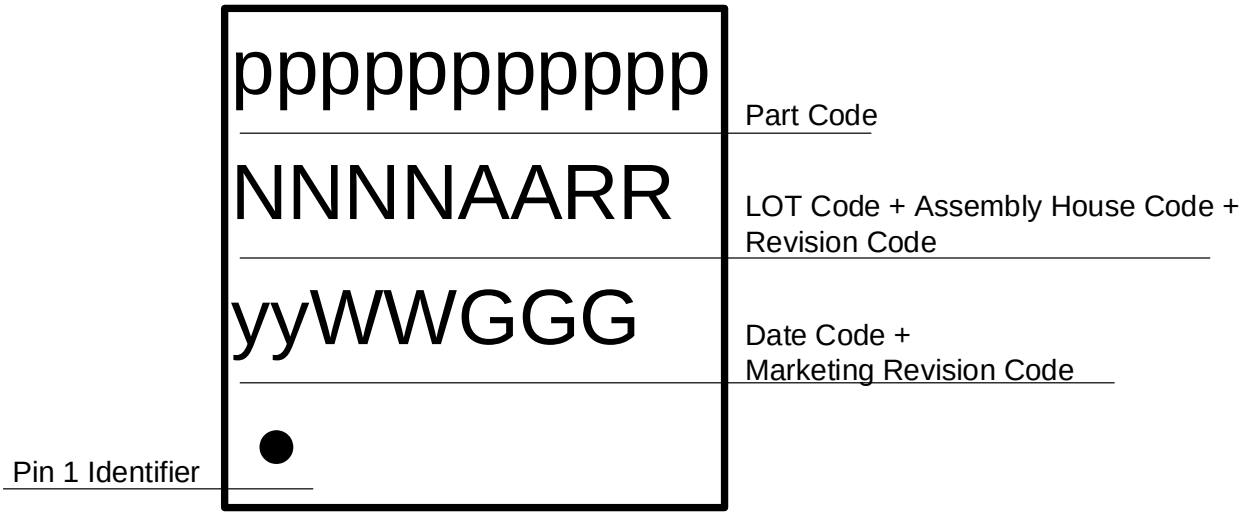


Figure 51. Package Top Marking LQFN-48

11.2.3. WLCSP 48L (3.241 mm x 2.575 mm x 0.495 mm, 0.35P)

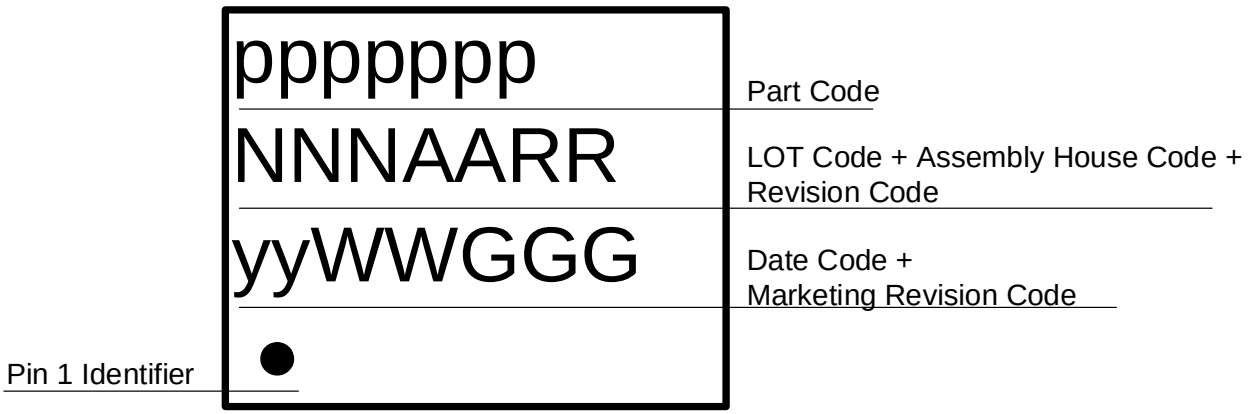


Figure 52. Package Top Marking WLCSP-48

11.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 18.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

All available packages are qualified for MSL 1.

Table 18. MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C/60 % RH
MSL 3	168 hours	30 °C/60 % RH
MSL 2A	4 weeks	30 °C/60 % RH
MSL 2	1 year	30 °C/60 % RH
MSL 1	Unlimited	30 °C/60 % RH

11.4 Handling

Be sure to handle package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle LQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

11.5 Soldering Information

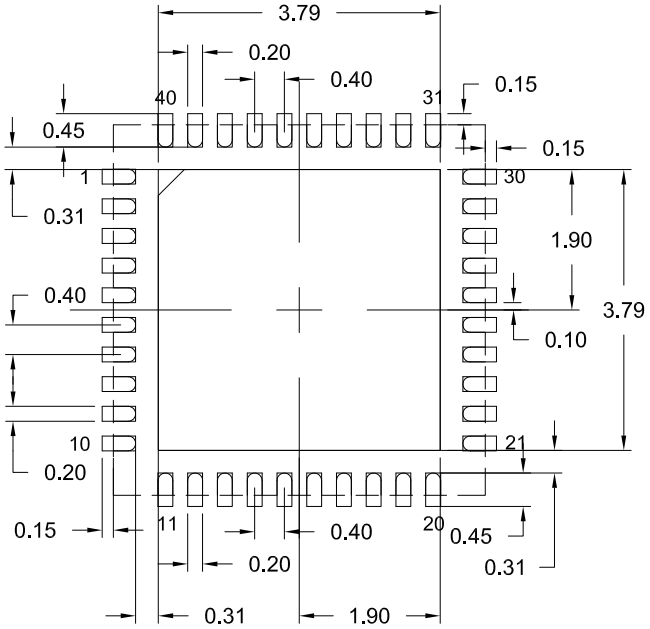
Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to +85 °C. To guarantee reliable operation, the junction temperature of the SLG47920/SLG47921 must not exceed +150 °C.

13. Layout Guidelines

13.1 LQFN 40L (5.0 mm x 5.0 mm x 0.85 mm, 0.4P) WB



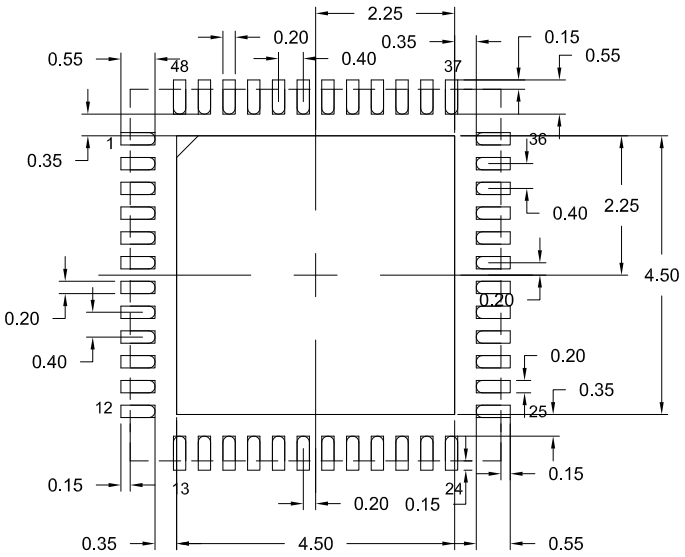
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Figure 53. Recommended Landing Pattern for LQFN 40L

13.2 LQFN 48L (6.0 mm x 6.0 mm x 0.85 mm, 0.4P) WB



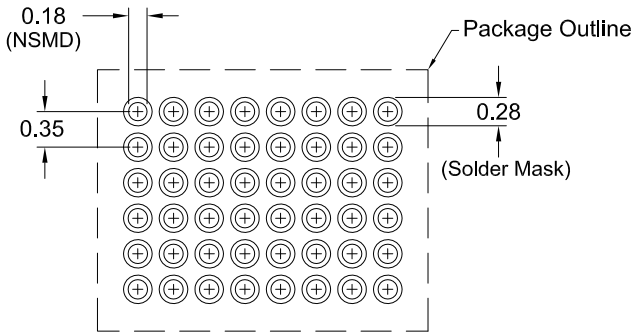
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Figure 54. Recommended Landing Pattern for LQFN 48L

13.3 WLCSP 48L (3.241 mm x 2.575 mm x 0.495 mm, 0.35P)



NOTES:

1. JEDEC compatible.
2. All dimension are in mm and angles are in degrees.
3. Use ±0.05mm for the non-tolerenced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solder ball diameter is Ø0.21 mm.
6. UBM diameter is Ø0.20 mm.

RECOMMENDED LAND PATTERN
(PCB Top view, NSMD Design)

Figure 55. Recommended Landing Pattern for WLCSP 48L

14. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
SLG47921C	48-pin WLCSP	Tape and Reel	-40 °C to +85 °C
SLG47921V	48-pin LQFN	Tape and Reel	-40 °C to +85 °C
SLG47920V[1]	40-pin LQFN	Tape and Reel	-40 °C to +85 °C
[1] Not available for order yet. Expected to be released in early 2026. For more information contact Renesas.			

14.1 Tape and Reel Specifications

Package type	# of pins	Nominal Package size [mm]	Max units		Reel and Hub size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
LQFN 40L 5.0 mm x 5.0 mm 0.4P Green	40	5 x 5	4000	4000	330/102	42	336	42	336	12	8
LQFN 48L 6.0 mm x 6.0 mm 0.4P Green	48	6 x 6	4000	4000	330/102	42	336	42	336	16	12
WLCSP 48L 3.241 mm x 2.575 mm 0.35P	48	3.24 x 2.57	2000	2000	178/60	250	2000	250	2000	12	8

14.2 Carrier Tape Drawing and Dimensions

Package type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
LQFN 40L 5.0 mm x 5.0 mm 0.4P Green	5.25	5.25	1.1	4	8	1.5	1.75	5.5	12
LQFN 48L 6.0 mm x 6.0 mm 0.4P Green	6.3 ± 0.1	6.3 ± 0.1	1.1 ± 0.1	4	12	1.5	1.75	7.5	16
WLCSP 48L 3.241 mm x 2.575 mm 0.35P	2.72	3.39	0.7	4	8	1.50	1.75	5.50	12

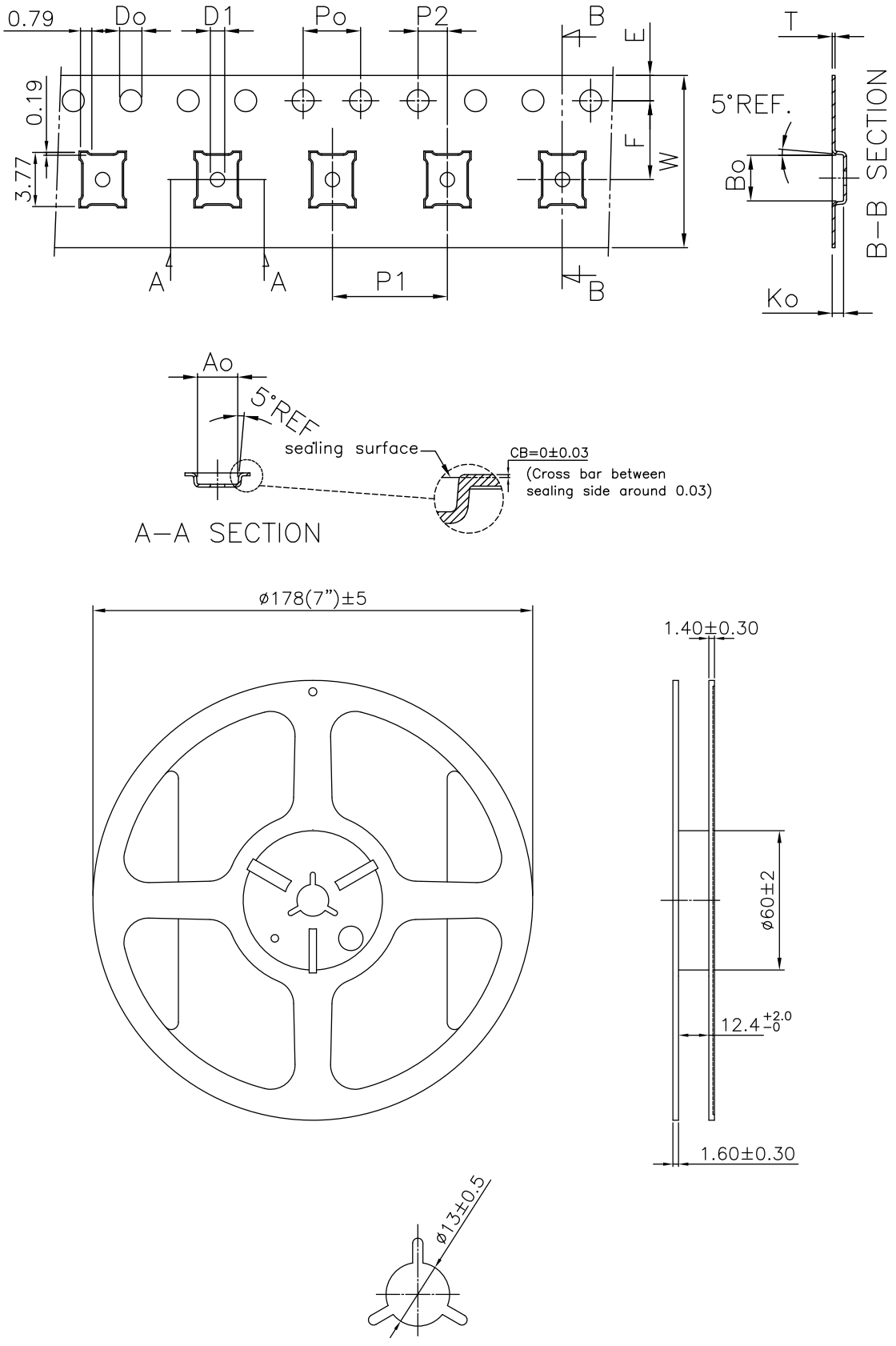


Figure 56. Tape and Reel Drawing for WLCSP 48L

.

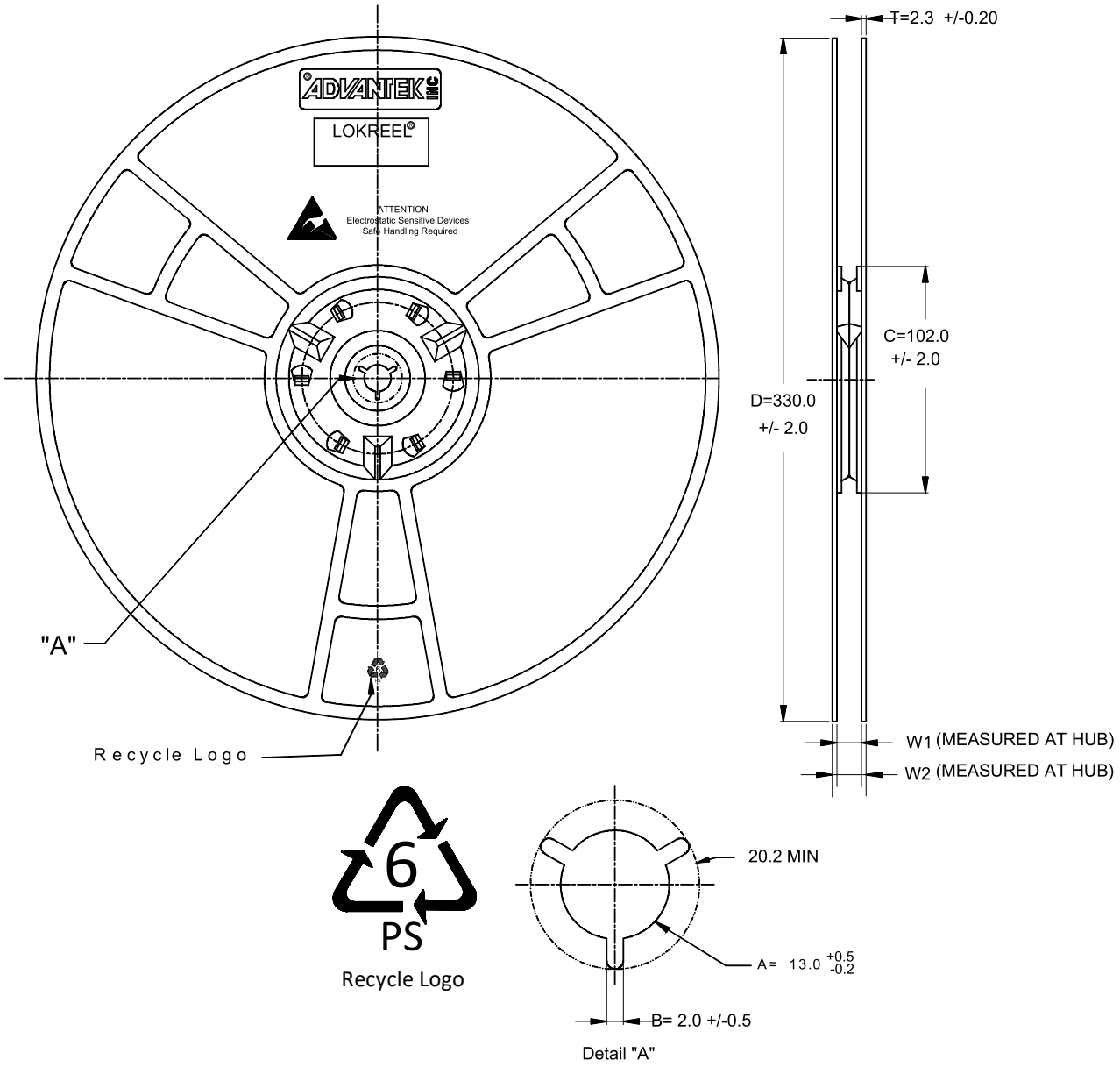
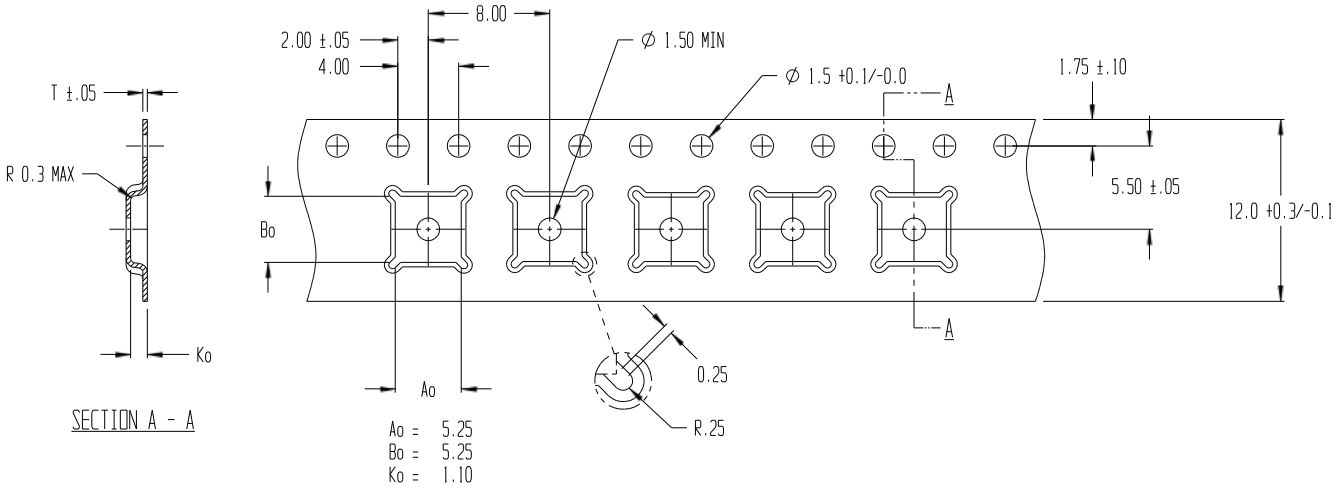


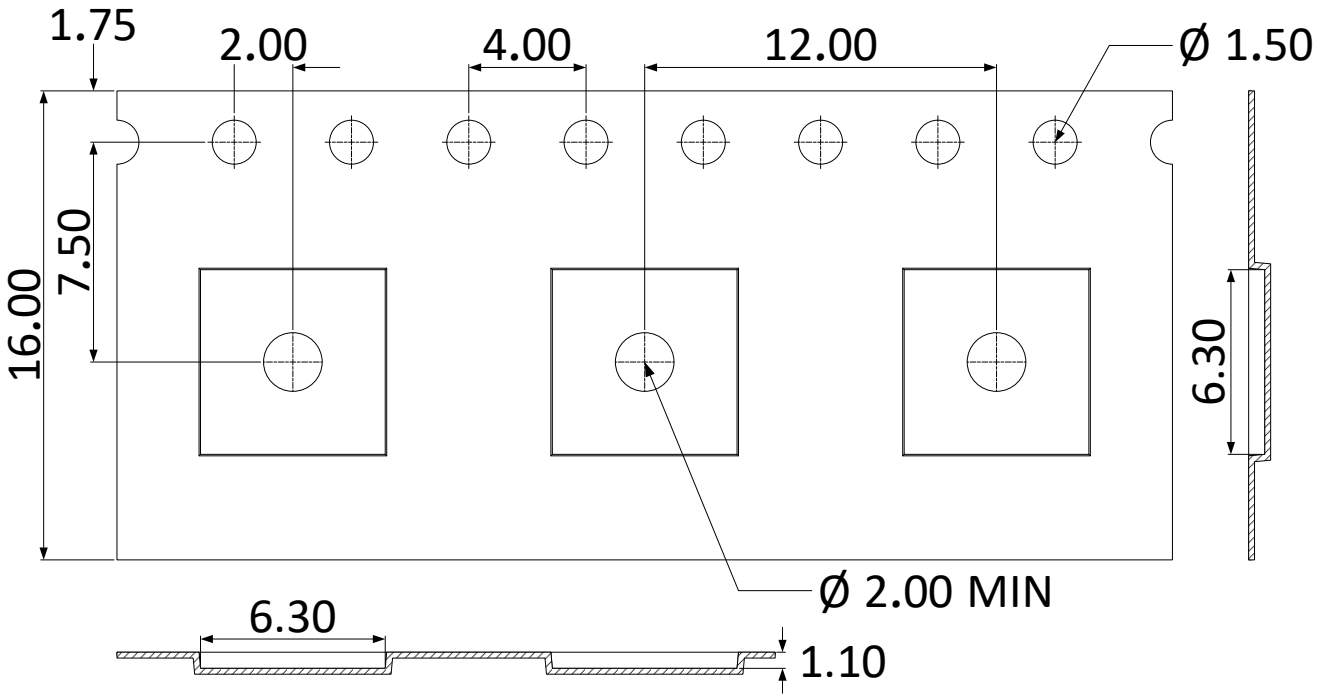
Figure 57. Reel Drawing for LQFN 40L and LQFN 48L



Note 1: Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Note 2: Other material is available.

Figure 58. Tape Drawing for LQFN 40L



Note 1: Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Note 2: Other material is available.

Figure 59. Tape Drawing for LQFN 48L

Glossary

B

BRAM	Block Random Access Memory

C

CLB	Configurable Logic Blocks
CLBL	Configurable Logic Blocks for Logic
CLBM	Configurable Logic Blocks for Memory
CS	Chip Select for SPI

D

DFF	D Flip-flop

F

FPGA	Field Programmable Gate Array
FREF	Reference Frequency

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IOB	Input Output Buffer

L

LUT	Look-up Table
LaC	Logic-as-Clock
LQFN	Low-profile Quad Flat No-lead Package

M

MCU	Microcontroller Unit
MISO	Master Input Slave Output
MOSI	Master Output Slave Input

N

NVM	Non-volatile Memory

O

OE	Output Enable
OSC	Oscillator
OTP	One-time Programmable

P

PD	Power-down
PLL	Phase Locked Loop
POR	Power-on Reset
PP	Push-pull
PU	Pull-up

Q

QFN	Quad Flat No-lead Package

S

SCK	Serial Clock for SPI
SDI	Serial Data Input for SPI
SI	Serial (Data) Input for SPI
SDO	Serial Data Output for SPI
SO	Serial (Data) Output for SPI
SPI	Serial Peripheral Interface
SRM	Shift Register Mode

V

VCO	Voltage Controlled Oscillator

W

WLCSP	Wafer Level Chip Scale Packaging

Revision History

Revision	Date	Description
1.01	Oct 31, 2025	Cover page: fixed number of GPIOs for SLG47920 (from 36 to 32). WLCSP package size – used 3-digit precision everywhere. All QFN mentions changed to LQFN.
1.00	Sep 26, 2025	Initial Release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
SLG47920V	40	LQFN	QV0040AB/PSC-5114-01
SLG47921V	48	LQFN	QV0048AD/PSC-5115-01
SLG47921C	48	WLCSP	WB0048AA/PSC-5127-01

A.2 Symbol Pin Information

A.2.1 40-LQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	GPIO0	I/O	SPI_CS
2	GPIO1	I/O	SPI_SCK
3	GPIO2	I/O	SPI_SI
4	GPIO3	I/O	SPI_SO/CONFIG_DONE
5	GPIO4	I/O	-
6	GPIO5	I/O	-
7	GPIO6	I/O	PLL0_EXT_REF_CLK
8	GPIO7	I/O	PLL1_EXT_REF_CLK
9	V_{DDIO0}	Power	-
10	V_{SSIO0}	Power	-
11	nSLEEP	Input	-
12	nRST	Input	-
13	GPIO8	I/O	PLL0_FOUT0
14	GPIO9	I/O	PLL1_FOUT
15	GPIO10	I/O	OSC_POSTDIV_OUT0
16	GPIO11	I/O	-
17	GPIO12	I/O	BOOT_ADDR_SEL0
18	GPIO13	I/O	BOOT_ADDR_SEL1
19	GPIO14	I/O	BOOT_ADDR_SEL2
20	GPIO15	I/O	BOOT_ADDR_SEL3
21	V_{DDC}	Power	-
22	GPIO16	I/O	-
23	GPIO17	I/O	-
24	GPIO18	I/O	LVDS0_IN_N/LVDS0_OUT_N
25	GPIO19	I/O	LVDS0_IN_P/LVDS0_OUT_P
26	GPIO20	I/O	LVDS1_IN_N/LVDS1_OUT_N
27	GPIO21	I/O	LVDS1_IN_P/LVDS1_OUT_P

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
28	GPIO22	I/O	LVDS2_IN_N/LVDS2_OUT_N
29	GPIO23	I/O	LVDS2_IN_P/LVDS2_OUT_P
30	V_{DDIO1}	Power	-
31	V_{SSIO1}	Power	-
32	GPIO24	I/O	-
33	GPIO25	I/O	-
34	GPIO26	I/O	-
35	GPIO27	I/O	-
36	GPIO28	I/O	-
37	GPIO29	I/O	-
38	GPIO30	I/O	-
39	GPIO31	I/O	-
40	V_{DDC}	Power	-
EPAD41	V_{SSC}	Power	-

A.2.2 48-LQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	GPIO39	I/O	-
2	GPIO0	I/O	SPI_CS
3	GPIO1	I/O	SPI_SCK
4	GPIO2	I/O	SPI_SI
5	GPIO3	I/O	SPI_SO/CONFIG_DONE
6	GPIO4	I/O	-
7	GPIO5	I/O	-
8	GPIO6	I/O	PLL0_EXT_REF_CLK
9	GPIO7	I/O	PLL1_EXT_REF_CLK
10	GPIO32	I/O	-
11	V_{DDIO0}	Power	-
12	V_{SSIO0}	Power	-
13	nSLEEP	Input	-
14	nRST	Input	-
15	GPIO33	I/O	-
16	GPIO8	I/O	PLL0_FOUT0
17	GPIO9	I/O	PLL1_FOUT
18	GPIO10	I/O	OSC_POSTDIV_OUT0
19	GPIO11	I/O	-
20	GPIO12	I/O	BOOT_ADDR_SEL0
21	GPIO13	I/O	BOOT_ADDR_SEL1
22	GPIO14	I/O	BOOT_ADDR_SEL2
23	GPIO15	I/O	BOOT_ADDR_SEL3
24	GPIO34	I/O	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
25	V_{DDC}	Power	-
26	GPIO35	I/O	-
27	GPIO16	I/O	-
28	GPIO17	I/O	-
29	GPIO18	I/O	LVDS0_IN_N/LVDS0_OUT_N
30	GPIO19	I/O	LVDS0_IN_P/LVDS0_OUT_P
31	GPIO20	I/O	LVDS1_IN_N/LVDS1_OUT_N
32	GPIO21	I/O	LVDS1_IN_P/LVDS1_OUT_P
33	GPIO22	I/O	LVDS2_IN_N/LVDS2_OUT_N
34	GPIO23	I/O	LVDS2_IN_P/LVDS2_OUT_P
35	GPIO36	I/O	-
36	V_{DDIO1}	Power	-
37	V_{SSIO1}	Power	-
38	GPIO37	I/O	-
39	GPIO24	I/O	-
40	GPIO25	I/O	-
41	GPIO26	I/O	-
42	GPIO27	I/O	-
43	GPIO28	I/O	-
44	GPIO29	I/O	-
45	GPIO30	I/O	-
46	GPIO31	I/O	-
47	GPIO38	I/O	-
48	V_{DDC}	Power	-
EPAD49	V_{SSC}	Power	-

A.2.3 48-WLCSP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
A1	V_{DDIO1}	Power	-
A2	V_{SSC}	Power	V_{SSIO0}/V_{SSIO1}
A3	GPIO25	I/O	-
A4	GPIO27	I/O	-
A5	GPIO29	I/O	-
A6	GPIO31	I/O	-
A7	GPIO39	I/O	-
A8	V_{DDC}	Power	-
B1	GPIO23	I/O	LVDS2_IN_P/LVDS2_OUT_P
B2	GPIO22	I/O	LVDS2_IN_N/LVDS2_OUT_N
B3	GPIO37	I/O	-
B4	GPIO26	I/O	-
B5	GPIO30	I/O	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
B6	GPIO38	I/O	-
B7	GPIO0	I/O	SPI_CS
B8	GPIO1	I/O	SPI_SCK
C1	GPIO21	I/O	LVDS1_IN_P/LVDS1_OUT_P
C2	GPIO20	I/O	LVDS1_IN_N/LVDS1_OUT_N
C3	GPIO24	I/O	-
C4	GPIO28	I/O	-
C5	GPIO8	I/O	PLL0_FOUT0
C6	GPIO4	I/O	-
C7	GPIO2	I/O	SPI_SI
C8	GPIO3	I/O	SPI_SO/CONFIG_DONE
D1	GPIO19	I/O	LVDS0_IN_P/LVDS0_OUT_P
D2	GPIO18	I/O	LVDS0_IN_N/LVDS0_OUT_N
D3	GPIO36	I/O	-
D4	GPIO14	I/O	BOOT_ADDR_SEL2
D5	GPIO9	I/O	PLL1_FOUT
D6	nSLEEP	Input	-
D7	GPIO6	I/O	PLL0_EXT_REF_CLK
D8	GPIO5	I/O	-
E1	GPIO17	I/O	-
E2	GPIO16	I/O	-
E3	GPIO35	I/O	-
E4	GPIO13	I/O	BOOT_ADDR_SEL1
E5	GPIO11	I/O	-
E6	nRST	Input	-
E7	GPIO7	I/O	PLL1_EXT_REF_CLK
E8	GPIO32	I/O	-
F1	V_{DDC}	Power	-
F2	GPIO34	I/O	-
F3	GPIO15	I/O	BOOT_ADDR_SEL3
F4	GPIO12	I/O	BOOT_ADDR_SEL0
F5	GPIO10	I/O	OSC_POSTDIV_OUT0
F6	GPIO33	I/O	-
F7	V_{SSC}	Power	V_{SSIO0}/V_{SSIO1}
F8	V_{DDIO0}	Power	-

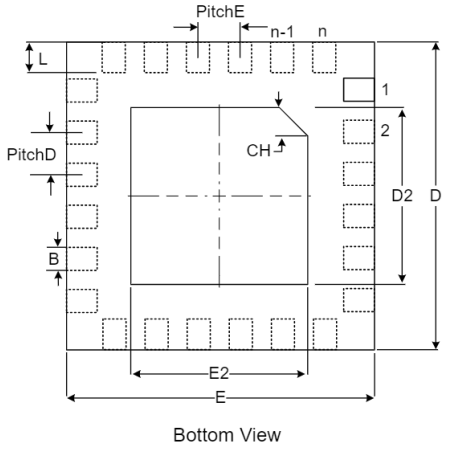
A.3 Symbol Parameters

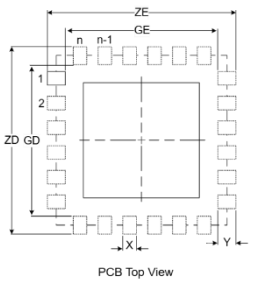
Orderable Part Number	Qualification	Min Operating Temperature	Max Operating Temperature	Min Core Voltage	Max Core Voltage	Min GPIO Voltage	Max GPIO Voltage	Number of LUT5	Number of DFF	BRAM and Distributed Memory	Number of GPIO	Number of GPIO Domains	Number of OSC	Number of PLL	LVDS Channels	Configuration Methods	RoHS
SLG47920V	Industrial	-40 °C	+85 °C	1.05 V	1.15 V	1.71 V	3.465 V	2240	2240	64 kbit/ 10 kbit	32	2	1	2	3	SPI/OTP	Compliant
SLG47921V	Industrial	-40 °C	+85 °C	1.05 V	1.15 V	1.71 V	3.465 V	2240	2240	64 kbit/ 10 kbit	40	2	1	2	3	SPI/OTP	Compliant
SLG47921C	Industrial	-40 °C	+85 °C	1.05 V	1.15 V	1.71 V	3.465 V	2240	2240	64 kbit/ 10 kbit	40	2	1	2	3	SPI/OTP	Compliant

A.4 Footprint Design Information

A.4.1 40-LQFN

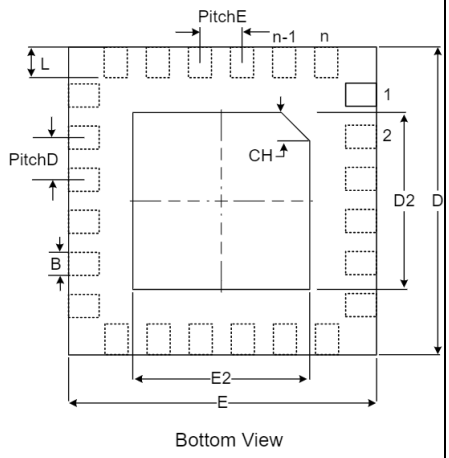
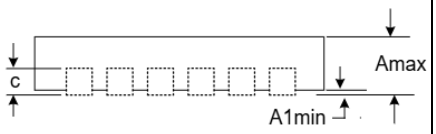
IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	QV0040AB/PSC-5114-01	40

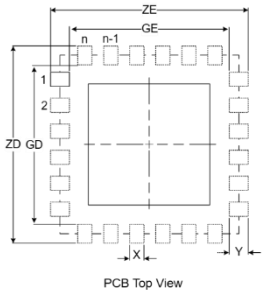
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	4.90	
Maximum body span (vertical side)	Dmax	5.10	
Minimum body span (horizontal side)	Emin	4.90	
Maximum body span (horizontal side)	Emax	5.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Number of pins (vertical side)	PinCountD	10	
Number of pins (horizontal side)	PinCountE	10	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side(center).	Pin1	S2	
Thermal pad Chamfer. If not present give hyphen (-).	CH	0.35	
Minimum thermal pad size (vertical side)	D2min	3.69	
Maximum thermal pad size (vertical side)	D2max	3.89	
Minimum thermal pad size (horizontal side)	E2min	3.69	
Maximum thermal pad size (horizontal side)	E2max	3.89	
Maximum Height	Amax	0.95	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	5.31	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	5.31	
Distance between left pad heel to right pad heel (horizontal side)	GE	4.41	
Distance between top pad heel to bottom pad heel (vertical side)	GD	4.41	
Pad Width	X	0.20	
Pad Length	Y	0.45	

A.4.2 48-LQFN

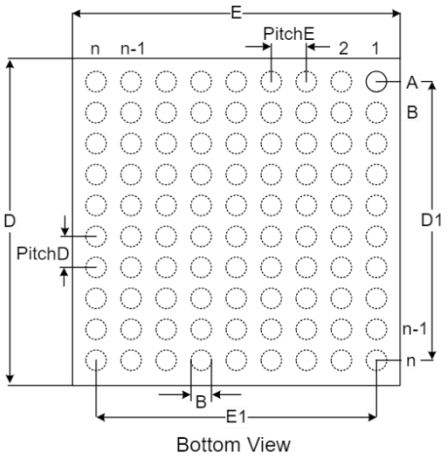
IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	QV0048AD/PSC-5115-01	48

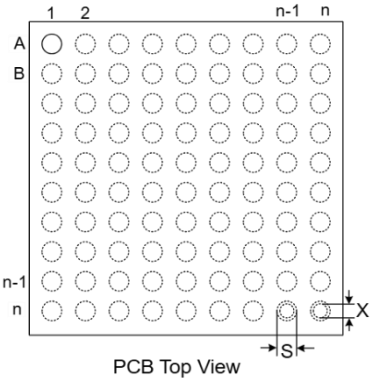
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	5.90	 Bottom View
Maximum body span (vertical side)	Dmax	6.10	
Minimum body span (horizontal side)	Emin	5.90	
Maximum body span (horizontal side)	Emax	6.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.45	
Number of pins (vertical side)	PinCountD	12	
Number of pins (horizontal side)	PinCountE	12	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side(center).	Pin1	S2	
Thermal pad Chamfer. If not present give hyphen (-).	CH	0.35	
Minimum thermal pad size (vertical side)	D2min	4.40	
Maximum thermal pad size (vertical side)	D2max	4.60	
Minimum thermal pad size (horizontal side)	E2min	4.40	
Maximum thermal pad size (horizontal side)	E2max	4.60	
Maximum Height	Amax	0.95	 Side View
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	6.30	 PCB Top View
Distance between top pad toe to bottom pad toe (vertical side)	ZD	6.30	
Distance between left pad heel to right pad heel (horizontal side)	GE	5.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	5.20	
Pad Width	X	0.20	
Pad Length	Y	0.55	

A.4.3 48-WLCSP

IPC Footprint Type	Package Code/POD Number	Number of Pins
WLCSP	WB0048AA/PSC-5127-01	48

Description	Dimension	Value (mm)	Diagram
Minimum body Length (vertical side)	Dmin	2.55	
Maximum body Length (vertical side)	Dmax	2.6	
Average length of grid (vertical side)	D1ave	1.75	
Minimum body Width (horizontal side)	Emin	3.216	
Maximum body Width (horizontal side)	Emax	3.266	
Average length of grid (horizontal side)	E1ave	2.45	
Average ball diameter	Bnom	0.225	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.35	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.35	
P = Plain Grid, S = Staggered Grid	GridType	P	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	F	
Number of balls (vertical side)	Rows	6	
Number of balls (horizontal side)	Columns	8	
Maximum number of ball positions (Rows x Columns)	Nmax	48	
Number of actual balls present	PinCount	48	
Ball positions removed from matrix. Example: C5-H10,B6-B9,A1	DepopulateBalls	-	
Ball positions added back into depopulated matrix. Example: C8,D6-F9	RepopulateBalls	-	
Minimum Standoff Height	A1min	0.15	
Maximum Height	Amax	0.525	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Diameter of pad. If specified this overrides the calculated value. This can be used to specify a manufacturer's recommended pad size.	X	0.18	
Solder Mask Expansion.	S	0.28	