SLG4AC42401

GreenPAK ™

Dual OSFP Low-Speed Host Controller

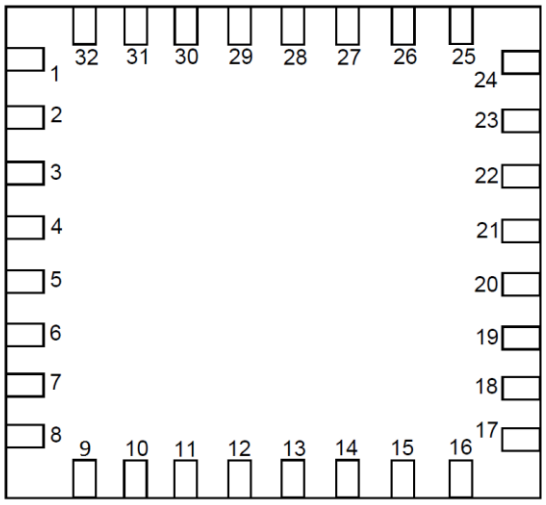
General Description

Renesas SLG4AC42401 is a low power and small form device. The SoC is housed in a 4mm x 4mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 32 Package

Pin Configuration



STQFN-32 (Top view)

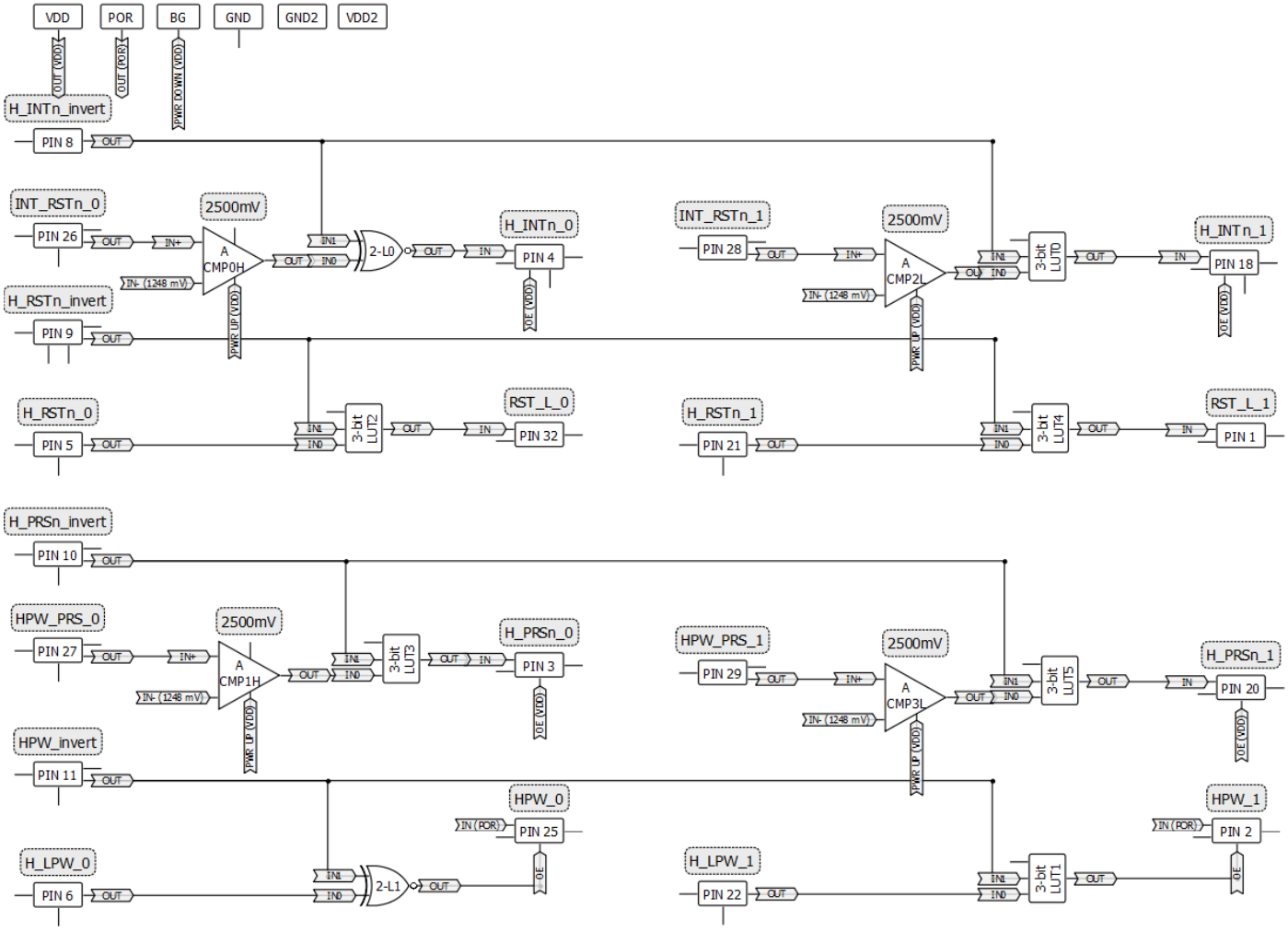
Output Summary

2 Outputs - 3-State Output 1X
2 Outputs - Open Drain NMOS 1X
4 Outputs - Push Pull 1X

Pin Name

Pin #	Pin name	Pin #	Pin name
1	RST_L_1	17	NC
2	HPW_1	18	H_INTn_1
3	H_PRSn_0	19	NC
4	H_INTn_0	20	H_PRSn_1
5	H_RSTn_0	21	H_RSTn_1
6	H_LPW_0	22	H_LPW_1
7	NC	23	NC
8	H_INTn_invert	24	NC
9	H_RSTn_invert	25	HPW_0
10	H_PRSn_invert	26	INT_RSTn_0
11	HPW_invert	27	HPW_PRS_0
12	NC	28	INT_RSTn_1
13	NC	29	HPW_PRS_1
14	GND	30	GND
15	VDD2	31	VDD
16	NC	32	RST_L_0

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	RST_L_1	Digital Output	Open Drain NMOS 1X	floating
2	HPW_1	Digital Output	3-State Output 1X	floating
3	H_PRSn_0	Digital Output	Push Pull 1X	floating
4	H_INTn_0	Digital Output	Push Pull 1X	floating
5	H_RSTn_0	Digital Input	Digital Input without Schmitt trigger	10kΩ pulldown
6	H_LPW_0	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
7	NC	Digital Input	Digital Input without Schmitt trigger	floating
8	H_INTn_invert	Digital Input	Digital Input without Schmitt trigger	floating
9	H_RSTn_invert	Digital Input	Digital Input without Schmitt trigger	floating
10	H_PRSn_invert	Digital Input	Digital Input without Schmitt trigger	floating
11	HPW_invert	Digital Input	Digital Input without Schmitt trigger	floating
12	NC	--	Keep Floating or Connect to GND	--
13	NC	--	Keep Floating or Connect to GND	--
14	GND	GND	Ground	--
15	VDD2	PWR	Supply Voltage	--
16	NC	--	Keep Floating or Connect to GND	--
17	NC	--	Keep Floating or Connect to GND	--
18	H_INTn_1	Digital Output	Push Pull 1X	floating
19	NC	--	Keep Floating or Connect to GND	--
20	H_PRSn_1	Digital Output	Push Pull 1X	floating
21	H_RSTn_1	Digital Input	Digital Input without Schmitt trigger	10kΩ pulldown
22	H_LPW_1	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
23	NC	--	Keep Floating or Connect to GND	--
24	NC	--	Keep Floating or Connect to GND	--
25	HPW_0	Digital Output	3-State Output 1X	floating
26	INT_RSTn_0	Analog Input/Output	Analog Input/Output	floating
27	HPW_PRS_0	Analog Input/Output	Analog Input/Output	floating
28	INT_RSTn_1	Analog Input/Output	Analog Input/Output	floating
29	HPW_PRS_1	Analog Input/Output	Analog Input/Output	floating
30	GND	GND	Ground	--
31	VDD	PWR	Supply Voltage	--
32	RST_L_0	Digital Output	Open Drain NMOS 1X	floating

Ordering Information

Part Number	Package Type
SLG4AC42401V	32-pin STQFN - Tape and Reel (5k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
Current at Input Pin	-1.0	1.0	mA
Input leakage Current (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD} (Note 4)	Supply Voltage		3	3.3	3.6	V
V_{DD2} (Note 4)	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		0.1	--	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PIN7, 8, 9, 10, 11, 26, 27, 28, 29 are LOW	--	71	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3 (Note 1)	V
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 2)	0.7xVDD (Note 1)	--	VDD+0.3 (Note 1)	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 2)	GND-0.3	--	0.3xVDD (Note 1)	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=3mA at VDD=3.3V (Note 1)	2.704	2.790	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V (Note 1)	--	0.158	0.217	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V (Note 1)	--	0.063	0.087	V
I_{OH}	HIGH-Level Output Current (Note 3)	Push-Pull 1X, VOH=2.4V at VDD=3.3V (Note 1)	5.54	7.48	--	mA
I_{OL}	LOW-Level Output Current (Note 3)	Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V (Note 1)	5.26	7.00	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V (Note 1)	12.90	17.14	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 6, 22	7	--	17	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 5, 21	7	--	17	kΩ

V_{ACMP0}	Analog Comparator0, 1, 2, 3, Threshold Voltage	Low to High transition, at temperature 25°C	2485	--	2525	mV
		Low to High transition, at temperature -40 +85°C (Note 4)	2485	--	2527	mV
		High to Low transition, at temperature 25°C	2470	--	2508	mV
		High to Low transition, at temperature -40 +85°C (Note 4)	2469	--	2509	mV
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.13	1.72	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V

Note 1 GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7 are powered from V_{DD} and GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4 are powered from V_{DD2}.
Note 2 No hysteresis.
Note 3 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 4 Guaranteed by Design.

Description

The SLG4AC42401 Dual OSFP Low-Speed Host Controller device contains two pairs of INT_RSTn and HPW_PRS signals transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when M_RSTn is asserted low. The module (SLG4AX42397) signals an interrupt to the host when M_INT_L is asserted low.

HPW_PRS is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG4AX42397) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when M_RSTn is asserted low.

For ease of system use, four invert input pins have been added to invert the default polarity of output signals. Refer to Table 7.

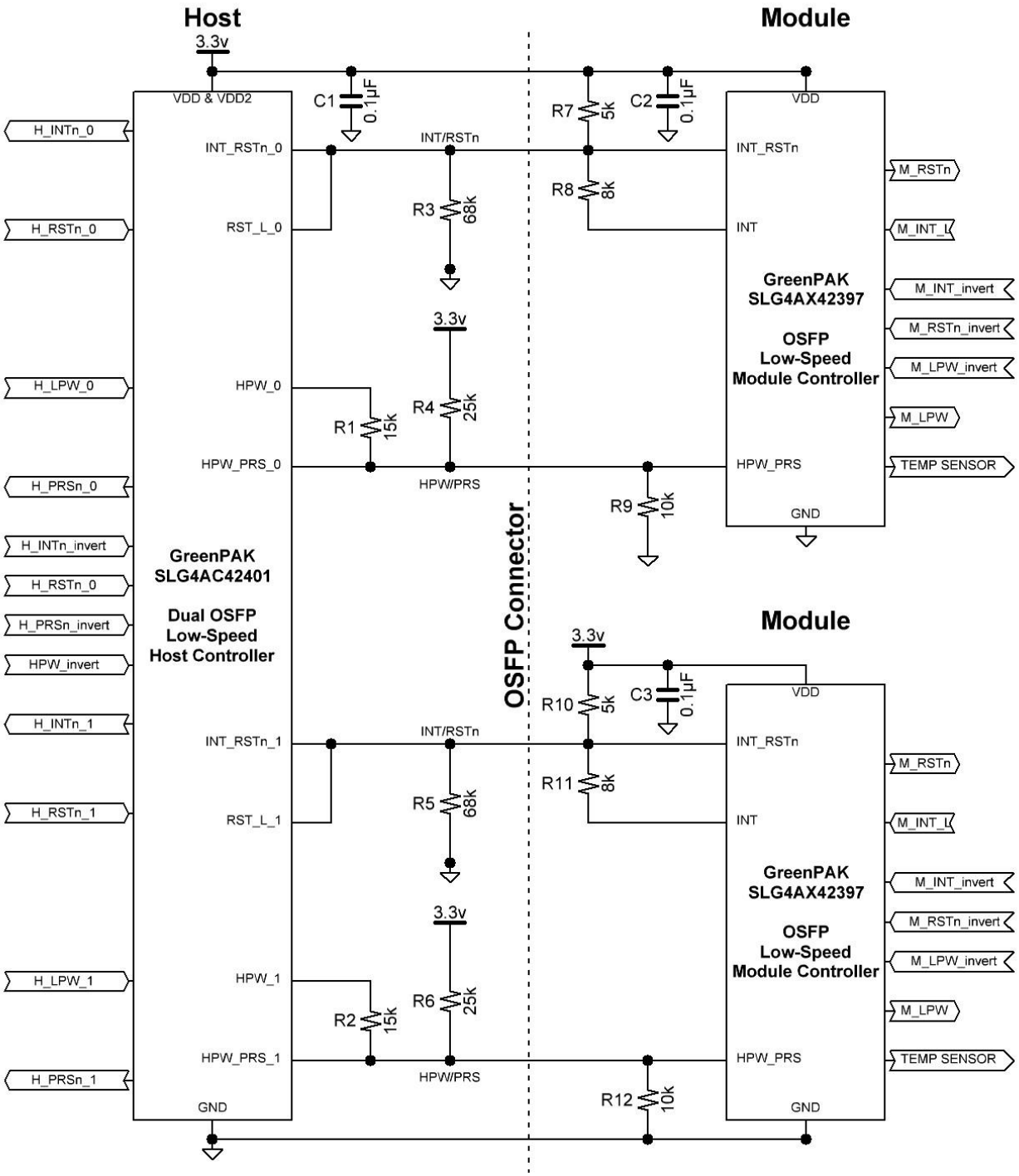
Output Polarity Control

Invert Pin Name	Status	Output Polarity
H_INTn_invert	Low	Active Low
	High	Active High
H_RSTn_invert	Low	Active Low
	High	Active High
H_PRSn_invert	Low	Active Low
	High	Active High
HPW_invert	Low	Active High
	High	Active Low

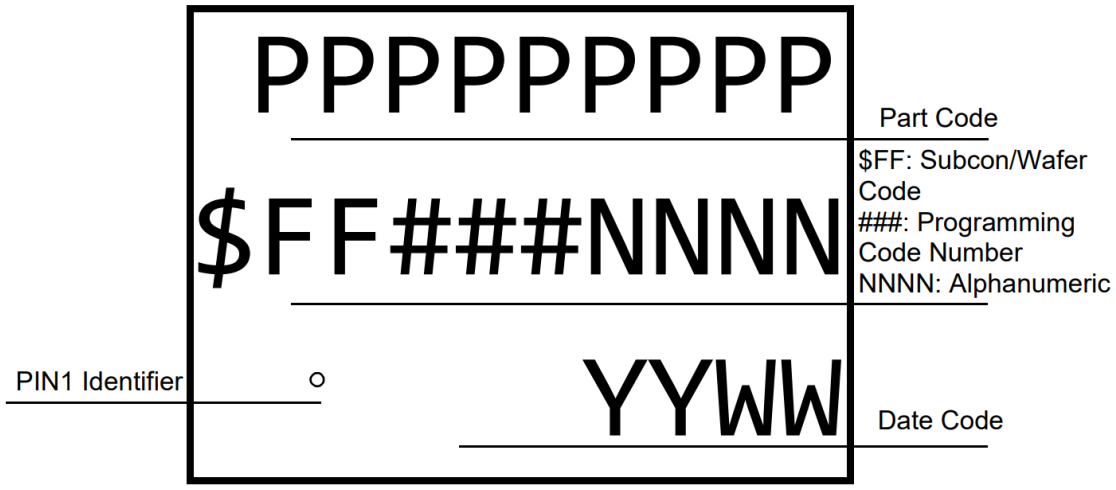
Dialog Compatible OSFP Parts

Part Number	Description
SLG4AC42401	Dual OSFP Low-Speed Host Controller
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Typical Application Circuit



Package Top Marking



Note: For this package type, Revision code is not marked on the part but may be present on labels and other materials. Instead, Wafer Code and Programming Code Number are marked on the part.

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	005	U	0xF4FD575D	4AC42401V	A	02/05/2026

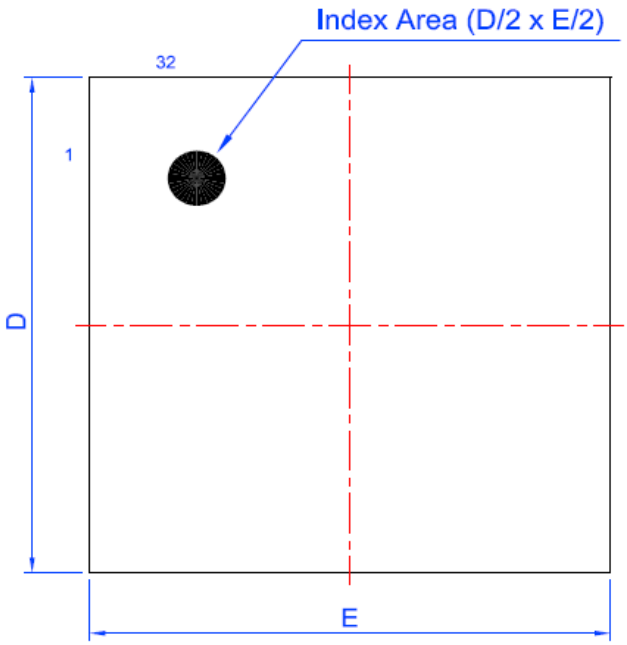
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

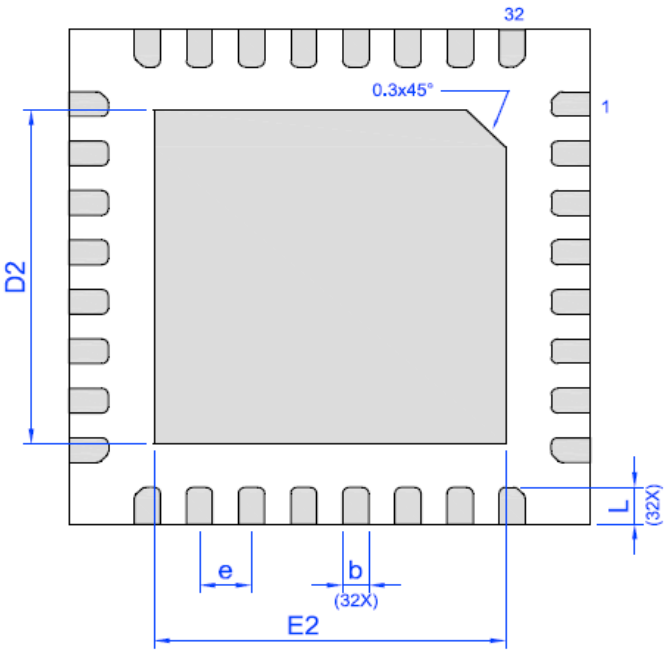
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

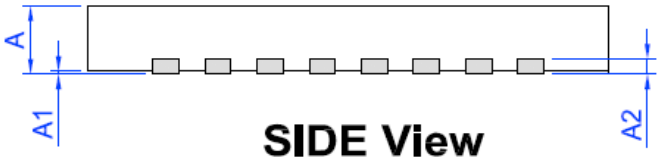
STQFN 32L 4x4mm 0.4P Package
IC Net Weight: 0.028 g



Marking View



BTM View



SIDE View

Unit: mm

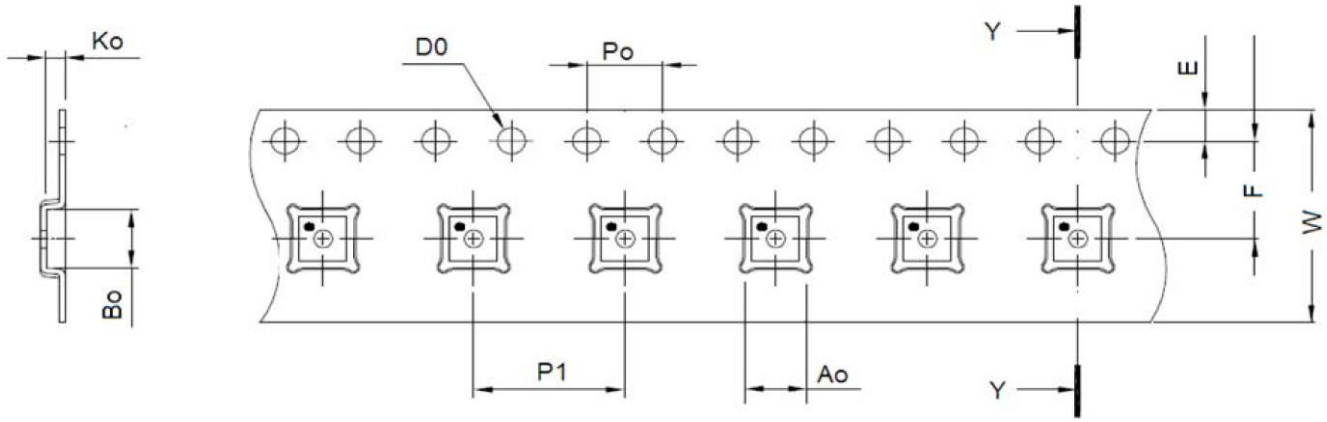
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	3.950	4.000	4.050
A1	0.00	-	0.050	E	3.950	4.000	4.050
A2	0.150 REF			D2	2.650	2.700	2.750
b	0.150	0.200	0.250	E2	2.650	0.270	2.750
e	0.400 BSC			L	0.250	0.300	0.350

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 32L 4x4 mm 0.4P Green	32	4 x 4 x 0.55	5000	10000	330/100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 4x4 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12

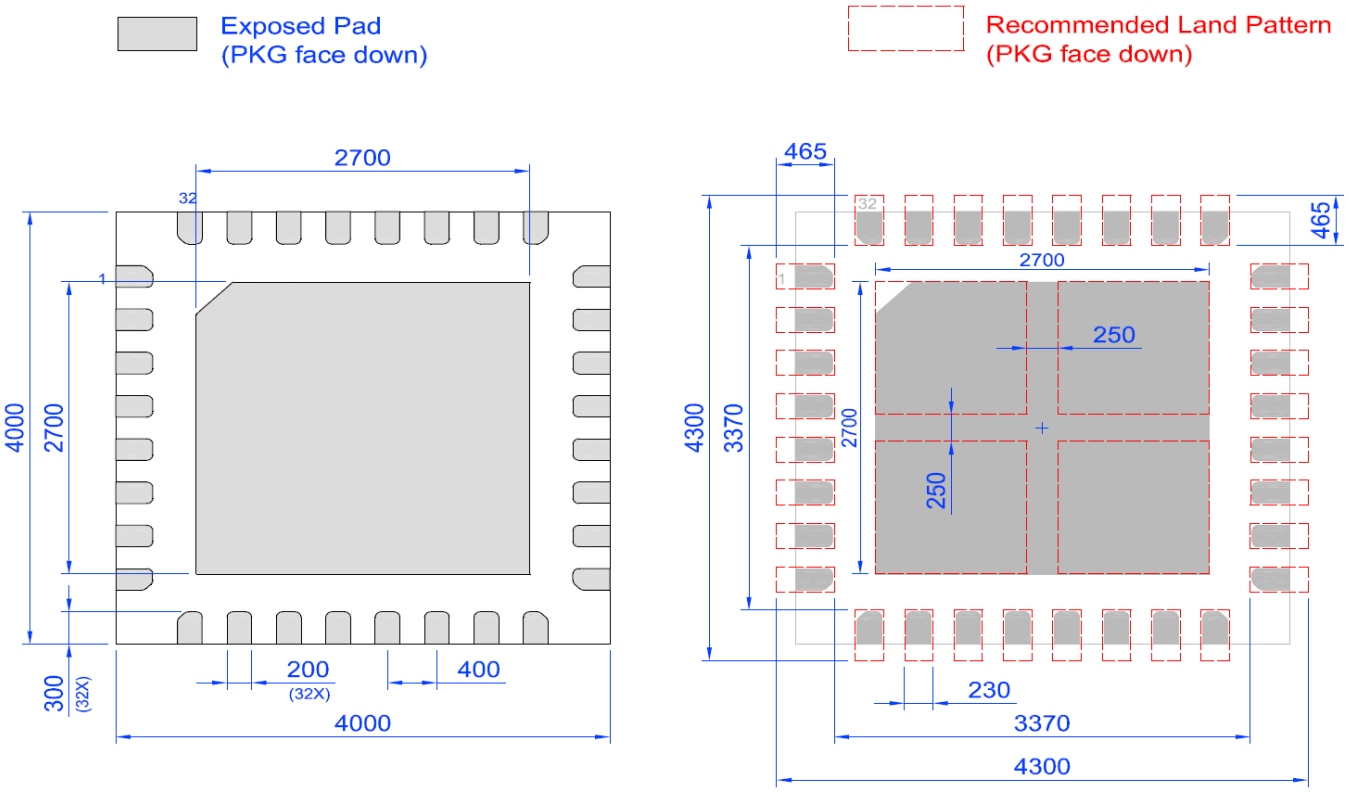


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines



Units: µm

Datasheet Revision History

Date	Version	Change
04/02/2018	0.10	New design for SLG46880 chip based on SLG4P42332
04/23/2018	0.11	Updated DS formatting
04/23/2018	0.12	Updated HPW polarity
05/02/2018	0.13	Updated DS formatting
05/04/2018	0.14	Updated DS formatting
07/25/2018	0.15	Updated pinout and added inverting functionality
08/28/2018	0.16	Updated DS formatting
10/28/2022	0.17	Updated Device Revision Table
01/10/2024	0.18	Moved to Renesas template
04/24/2024	0.19	Updated Quiescent Current Condition. Updated Analog Comparator0, 1, 2, 3, Threshold Voltage
05/03/2024	1.00	Production Release
02/05/2026	1.01	Added name for PIN 7