PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

General Description

SLG51000 contains seven compact and customizable low dropout regulators and is designed for high performance camera modules and other small multi-rail applications.

Two integrated LDOs are optimized to meet the requirements of high-performance analog circuits. They provide very low output voltage noise characteristics of 13 µV (rms) in addition to high PSRR of 81 dB at 1 MHz and tight output voltage accuracy of ±1 % over temperature.

Two LDOs can be configured to operate as load switches which are optimized to meet the requirements of low R_{ON}. By using efficient DC-DC switching regulators upstream in conjunction with SLG51000's linear regulators and load switches downstream, applications can leverage the best characteristics of each to simultaneously achieve low power, low noise, and low voltage dropout, respectively.

Built-in safety protection such as under-voltage lockout, over-temperature protection, and current limit ensures that the ICs are operating under nominal conditions. SLG51000 has an I^2C-compatible interface for flexible power control. SLG51000 is available in a small 20-pin WLCSP package with a wide ambient operating temperature range of -40 °C to 85 °C.

Key Features

- Input voltage range:
  - 2.8 V to 5.0 V (2 x HP LDO)
  - 1.7 V to 5.0 V (3 x HV LDO)
  - 0.8 V to 1.5 V (2 x LV LDO)
  - 0.5 V to 1.25 V (2 x load switch)
- Separate input supply and enable pins for flexible power configurations
- Output voltage range:
  - 2.4 V to 3.3 V (2 x HP LDO)
  - 1.2 V to 3.75 V (3 x HV LDO)
  - 0.5 V to 1.2 V (2 x LV LDO)
- Output current levels:
  - Up to 475 mA (2 x HP LDO)
  - Up to 500 mA (3 x HV LDO)
  - Up to 800 mA (2 x LV LDO)
  - Up to 800 mA (2 x load switch)
- High PSRR of 102 dB at 1 kHz and 81 dB at 1 MHz (2 x HP LDO)
- Ultra-low output voltage noise of 13 µV (2 x HP LDO)
- Low dropout voltage (10 mV per 100 mA of load) for high current LDO supply rails (2 x LV LDO)
- Ultra-low R_{ON} load switches with low leakage and slew rate control for low V_{IN} supplies
- Tight output voltage accuracy of ±1 % over-temperature
- Low shutdown current of 300 nA
- Low quiescent current of 14 µA
- User configurable settings via I^2C interface and OTP
  - Including output voltage, power sequencing, soft-start timing, and current limit threshold
- Soft start and soft shutdown
- Under-voltage lockout (UVLO)
- Thermal shutdown
- Configurable temperature alerts
- Wide -40 °C to +85 °C operating temperature
- 20-pin WLCSP: 1.675 mm x 2.075 mm x 0.465 mm, 0.4 mm pitch

Applications

- High End Camera Module Applications
- Smartphones
- Digital Cameras
- Smart Devices with Imaging

Contents

Figures

Tables

1 Block Diagram

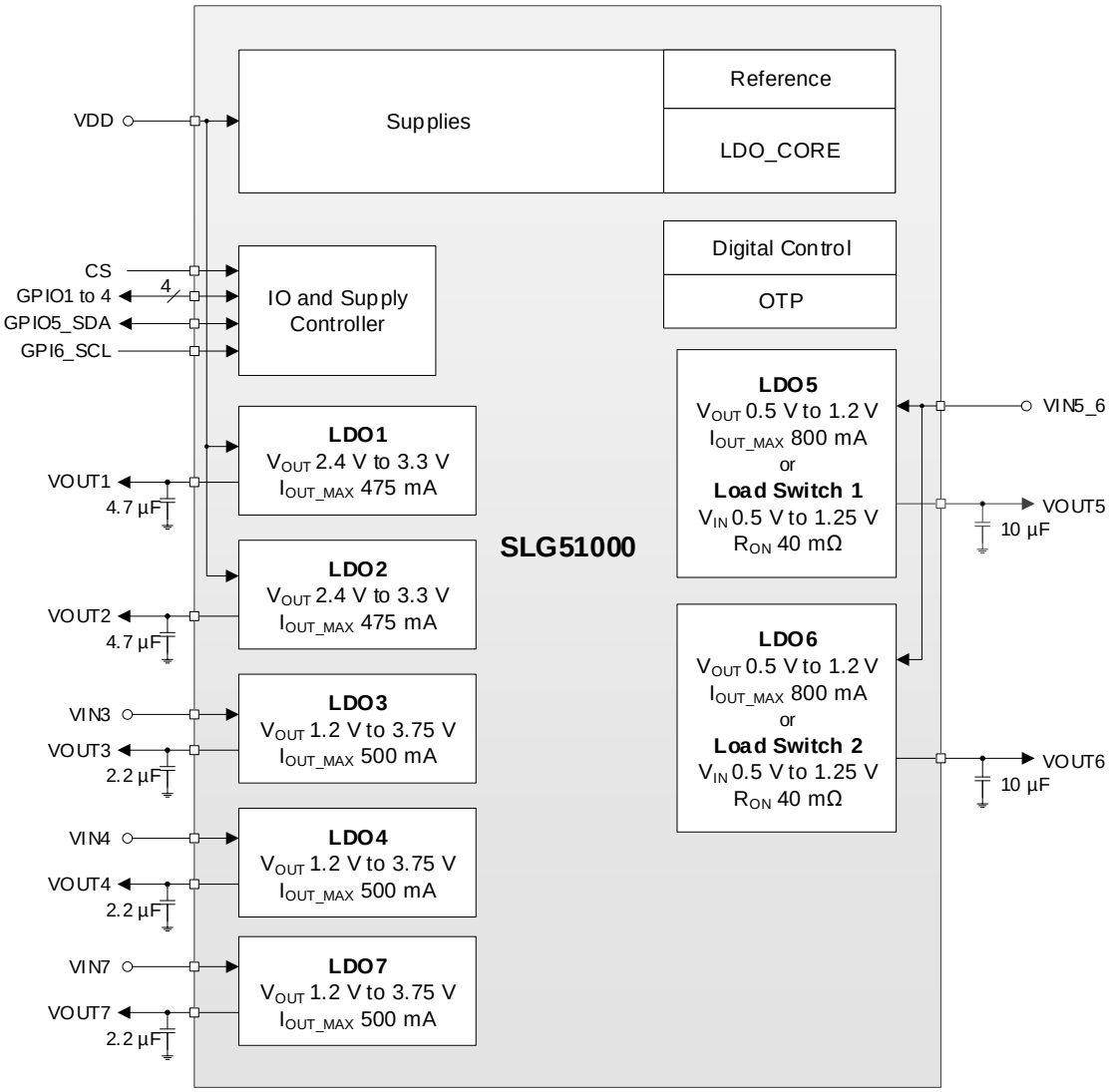


Figure 1: Block Diagram

2 Characteristics

2.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 1: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature	Non operational	-40	+150	°C
T_J	Junction temperature		-25	+125	°C
T_A	Ambient temperature		-40	+85	°C
V_{DD}	Power supply voltage on VDD pin		-0.3	+6.0	V
	Power supply voltage on VIN3, VIN4, VIN7 pins		-0.3	+6.0	V
	Power supply voltage on VIN5_6 pin		-0.3	+1.8	V
V_{PIN_LV}	Voltage on low-voltage pins	GPIO1 to GPIO5 and GPI6	-0.3	+1.98	V
V_{PIN_HV}	Voltage on high-voltage pins	CS	-0.3	V_{DD} + 0.3	V
ESD	ESD Protection (Human Body Model)		2000		V
	ESD Protection (Charged Device Model)		500		V

2.1.1 Guidelines for Reliable Operation

- Low Voltage Pins: take care that the low voltage pins (GPIO1 to GPIO5, GPI6, and VIN5_6) do not exceed their Abs. Max. ratings, even briefly. Transients both positive (above max) and negative (below min) can cause EOS (Electrical Overstress) damage.
- Power sequencing: CS should be held low before VDD is powered up. CS pin should also be pulled low before VDD falls out of operating range. VIN supplies for LDO_HV and LDO_LV channels (VIN3, VIN4, VIN7, VIN5_6) can be safely biased even if VDD is not present. VIN supplies should be powered up before enabling their respective LDO channels. GPIO's configured as inputs are allowed to be forced high before VDD is powered up.

2.2 Recommended Operating Conditions

Table 2: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature		-40		+85	°C
V_{DD}	Power supply voltage on VDD pin		2.8		5.0	V
	Power supply voltage on VIN3, VIN4, VIN7 pins		1.7		5.0	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Power supply voltage on VIN5_6 pin	LDO Mode	0.8		1.5	V
	Power supply voltage on VIN5_6 pin	Load Switch Mode	0.5		1.25	V
V_{PIN_LV}	Voltage on low-voltage pins	GPIO1 to GPIO5 and GPI6	0		1.8	V
V_{PIN_HV}	Voltage on high-voltage pins	CS	0		VDD	V

2.3 Thermal Characteristics

Table 3: Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{Θ_JA}	Package thermal resistance	Junction to ambient JEDEC standard PCB		55.3		K/W

2.4 Current Consumption

Note: Current consumption electrical characteristics apply over the full operating temperature range.

Table 4: Current Consumption

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
I_{Q_SLEEP}	Current consumption in SLEEP. I_{Q_SLEEP} is the I_Q in LOW IQ RESET State	V_{IN} = 3.8 V All references disabled I^2C interface disabled All rails disabled		0.15	0.65	µA
$I_{Q\_READY\_DIS}$	Current consumption in READY State	V_{IN} = 3.8 V All references enabled I^2C interface enabled All rails disabled		14	24	µA
$I_{Q\_READY\_EN}$	Current consumption in READY State	V_{IN} = 3.8 V All references enabled I^2C interface enabled All rails enabled, no load		785	1800	µA
$I_{Q\_OFF\_25C}$	Quiescent current in OFF Mode	T_A = 25 °C			1	µA
I_{Q_OFF}	Quiescent current in OFF Mode	T_A =-40 °C to 85 °C			7.6	µA

2.5 Chip Select Digital I/O Characteristics

Digital I/O electrical characteristics apply over the full operating temperature range, see Section 2.1.1.

Table 5: High-Voltage Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{IH}	CS input high voltage		0.9		VDD	V
V_{IL}	CS input low voltage		0		0.2	V
I_{LKG}	CS input leakage current	CS < 2V			1	µA
t_{ON_READY}	Turn-on time from CS HIGH to Ready State				10	ms

2.6 1.2 V/1.8 V Digital I/O Characteristics

1.2 V/1.8 V digital I/O electrical characteristics apply over the full operating temperature range, see Section 2.1.1. The voltage thresholds for all I/Os are referenced to VDDIO, where VDDIO can be 1.2 V or 1.8 V. The supply configuration options depend on the I/O, see Section **Error! Reference source not found.**.

Table 6: 1.2 V/1.8 V Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
GPIO1 to GPIO4						
V_{THR_POS}	Positive going threshold voltage		0.4*V DDIO		0.7*V DDIO	V
V_{THR_NEG}	Negative going threshold voltage		0.3*V DDIO		0.6*V DDIO	V
V_{OL}	Output low voltage	$I_{OUT} \le I_{OL}$	0		0.3	V
I_{OL}	Output current	V_{OL} = 0.3 V	2	13		mA
I_{LKG}	Input leakage				500	nA
SCL, SDA, GPIO5 and GPI6						
V_{THR_POS}	Positive going threshold voltage		0.4*V DDIO		0.7*V DDIO	V
V_{THR_NEG}	Negative going threshold voltage		0.3*V DDIO		0.6*V DDIO	V
V_{HYS}	Schmitt trigger hysteresis		0.1*V DDIO			V
V_{OL}	Output low voltage SDA, GPIO5	$I_{OUT} \le I_{OL}$	0		0.3	V
I_{OL}	Output current	V_{OL} = 0.3 V	20			mA
I_{LKG}	Input leakage				500	nA
C_{IN}	Pin capacitance				10	pF

2.7 LDO_HP Characteristics

Table 7: LDO_HP (LDO1 and 2) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		2.8		5	V
C_{OUT}	Output capacitance	Effective capacitance after derating	2.2	4.7	10	µF
I_{OUT_MAX}	Maximum output current	V_{IN} = 3.3 V V_{OUT} drops 50 mV	475			mA
Programmable Conditions						
V_{OUT}	Selectable output voltage		2.4	2.85	3.3	V
V_{OUT_LSB}	LSB of output voltage programming DAC (8-bit control)			5		mV
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable range Note 1	At 90 % V_{OUT}	11	140	240	mA
Electrical Performance						
Static Parameters						
V_{OUT_PP}	Part to part output voltage accuracy Note 2	I_{OUT} = 1 mA T_A = 25 °C	-5		5	mV
V_{OUT_TEMP}	Temperature dependence of V_{OUT} Note 2	I_{OUT} = 1 mA	-0.65		0.65	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 2	I_{OUT} = 1 mA V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) to V_{IN} (Max)	-2		2	mV
$V_{OUT\_STATIC\_LD}$	Static load regulation Note 2	1 mA < I_{OUT} < 300 mA	-4		2	mV
$V_{DROPOUT}$	Dropout voltage	@ V_{OUT} = V_{OUT} (V_{IN} (Max)) - 10 mV I_{OUT} = 300 mA			200	mV
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) + 100 mV to V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) V_{OUT} = V_{OUT} (Typ) I_{OUT} = 300 mA t_R = t_F = 1 µs			0.3	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) V_{OUT} = V_{OUT} (Typ) I_{OUT} = 1 mA to 300 mA t_R = t_F = 1 µs			20	mV
t_{ON}	Turn-on time	Time to 90 % of V_{OUT} I_{OUT} = 0 mA		0.15		ms
t_{OFF}	Turn-off time	Time to 10 % of V_{OUT} I_{OUT} = 0 mA			2	ms
AC Parameters						
$PSRR_{1kHz}$	Power supply rejection ratio	f = 1 kHz V_{IN} = 3.2 V V_{OUT} = V_{OUT} (Typ) I_{OUT} = 150 mA Note 3		102		dB
$PSRR_{100kHz}$	Power supply rejection ratio	f = 100 kHz V_{IN} = 3.2 V V_{OUT} = V_{OUT} (Typ) I_{OUT} = 150 mA Note 3		87		dB
$PSRR_{1MHz}$	Power supply rejection ratio	f = 1 MHz V_{IN} = 3.2 V V_{OUT} = V_{OUT} (Typ) I_{OUT} = 150 mA Note 3		81		dB
V_{N_100kHz}	Output noise	f = 10 Hz to 100 kHz V_{IN} = 3.2 V V_{OUT} = V_{OUT} (Typ) I_{OUT} > 30 mA		13		µV
V_{N_1MHz}	Output noise	f = 10 Hz to 1 MHz V_{IN} = 3.2 V V_{OUT} = V_{OUT} (Typ) I_{OUT} > 10 mA		21		µV
Current Limit Accuracy						
$I_{OUT\_FUNC\_LIM}$	Functional current limit		500			mA
$I_{OUT\_STARTUP\_LIM\_ACC}$	Start-up current limit accuracy	$I_{OUT\_STARTUP\_LIM}$ > 11 mA	-50		50	%
$I_{OUT\_STARTUP\_LIM\_ACC\_11}$	Start-up current limit accuracy	$I_{OUT\_STARTUP\_LIM}$ = 11 mA	-75		75	%
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current	I_{OUT} = 0 mA			515	µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{Q\_ON\_1mA}$	Quiescent current	I_{OUT} = 1 mA			560	µA
$I_{Q\_ON\_300mA}$	Quiescent current	I_{OUT} = 300 mA			3.2	mA
R_{PD_OFF}	Output pull down resistance	V_{OUT} = 0.5 V LDO disabled			40	Ω

Note 1 For programmable selections, refer to Section 4.4.1

Note 2 The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$.

Note 3 For V_{IN} - V_{OUT} < 350 mV, PSRR will be degraded.

2.8 LDO_HV Characteristics

In the LDO_HV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 5 V, for V_{IN} as defined in the table, and apply over the full operating temperature range, see Section 2.1.1.

Table 8: LDO_HV (LDO3, 4, and 7) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		1.7 Note 1	3.8	5	V
C_{OUT}	Output capacitance	Effective capacitance after derating	0.45	2.2	20	µF
I_{OUT_MAX}	Maximum output current	V_{OUT} drops 50 mV Note 2	500			mA
Programmable Conditions						
V_{OUT}	Selectable output voltage		1.2	3.3	3.75	V
V_{OUT_LSB}	LSB of output voltage programming DAC (8-bit control)			10		mV
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable in 12 mA steps Note 3	At 90 % V_{OUT}	30	150	606	mA
$I_{OUT\_FUNC\_LIM}$	Functional current limit, programmable in 12 mA steps Note 3		30	550	606	mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
Static Parameters						
V_{OUT_PP}	Part to part output voltage accuracy Note 4	I_{OUT} = 1 mA T_A = 25 °C	-10 Note 5		10 Note 5	mV
V_{OUT_TEMP}	Temperature dependence of V_{OUT} Note 4	I_{OUT} = 1 mA Note 6	-0.65		0.65	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 4	I_{OUT} = 1 mA V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) to V_{IN} (Max)	-2		2	mV
$V_{OUT\_STATIC\_LD}$	Static load regulation Note 4	1 mA < I_{OUT} < I_{OUT_MAX}	-6		2	mV
$V_{DROPOUT}$	Dropout voltage	@ V_{OUT} = V_{OUT} (V_{IN} (Max)) - 10 mV I_{OUT} = 250mA Note 7			200 Note 8	mV
R_{ON}	On resistance	@ V_{IN} = V_{OUT} (V_{IN} (Max)) - 50 mV I_{OUT} = I_{OUT_MAX} Note 7			800	mΩ
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) + 0.6 V to V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX} t_R = t_F = 100 mV/µs		2	5 Note 9	mV
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) V_{OUT} = V_{OUT} (Typ) I_{OUT} = 1 mA to I_{OUT_MAX}/2 t_R = t_F = 1 µs		28	37	mV
t_{ON}	Turn-on time	Time to 90 % of V_{OUT} I_{OUT} = 0 mA		0.2		ms
t_{OFF}	Turn-off time	Time to 10 % of V_{OUT} I_{OUT} = 0 mA		0.2	10	ms
AC Parameters						
$PSRR_{1kHz}$	Power supply rejection ratio	f = 1 kHz V_{IN} = V_{OUT} + 500 mV V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX}/2		83		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
$PSRR_{100kHz}$	Power supply rejection ratio	f = 100 kHz V_{IN} = V_{OUT} + 500 mV V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX}/2		56		dB
$PSRR_{1MHz}$	Power supply rejection ratio	f = 1 MHz V_{IN} = V_{OUT} + 500 mV V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX}/2		47		dB
V_N	Output noise	f = 10 Hz to 100 kHz I_{OUT} = I_{OUT_MAX}/2		152		µV
Current Limit Accuracy						
I_{OV_SINK}	Current sink at over-voltage	V_{OV} = V_{OUT} + 100 mV Note 10	10	77		mA
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current	I_{OUT} = 0 mA Note 11		7	13	µA
$I_{Q\_ON\_1mA}$	Quiescent current	I_{OUT} = 1 mA Note 11		30	38	µA
$I_{Q\_ON\_IMAX}$	Quiescent current	I_{OUT} = I_{OUT_MAX} Note 11		2.25	3.5	mA
R_{PD_OFF}	Output pull down resistance	V_{OUT} = 0.5 V LDO disabled		30	100	Ω

Note 1 I_{OUT_MAX} below 2.1 V is limited to 200 mA. For V_{IN} above 2.1 V, I_{OUT_MAX} of 500 mA is guaranteed.

Note 2 Guaranteed for V_{IN} > 2.1 V, between 1.7 V and 2.1 V the I_{OUT_MAX} guaranteed is 200 mA.

Note 3 Accuracy ±30 %

Note 4 The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$.

Note 5 +10 mV / -10 mV accuracy applies to factory-trimmed V_{OUT} values targeted between 1.23 V to 3.72 V. V_{OUT} targets from 1.20 V to 1.22 V can be trimmed to +24 mV/ -10 mV accuracy. V_{OUT} targets from 3.73 V to 3.75 V can be trimmed to +10 mV / -30 mV accuracy

Note 6 Guaranteed for V_{IN} ≥ 2.5 V.

Note 7 Guaranteed for V_{IN} > 1.8 V.

Note 8 Dropout voltage is linear with the load current. If using a lower I_{OUT_MAX} than specified, the dropout can be calculated using 80 mV per 100 mA of load.

Note 9 Guaranteed for V_{IN} > 2.1 V. Otherwise, maximum line transient is 20 mV.

Note 10 Guaranteed for V_{IN} > 2.35 V.

Note 11 Internal regulator current flowing to ground.

2.9 LDO_LV Characteristics

In the LDO_LV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 4.9 V, for V_{IN} as defined in the table, and apply over the full operating temperature range, see Section 2.1.1.

The characteristics for the LDOs in Load Switch Mode are given in Section 2.9.1.

Table 9: LDO_LV (LDO5 and 6) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input supply (pass device + part of controller)		0.8	1.25	1.5	V
V_{DD_CTRL}	Supply for controller (VDD)		2.3	3.8	5	V
C_{OUT}	Output capacitance	Effective capacitance after derating	10 Note 1	20	80	µF
ESL_{COUT}	Output capacitor series inductance	f > 100 kHz			1	nH
I_{OUT_MAX}	Maximum output current	V_{OUT} drops 50 mV	800			mA
Programmable Conditions						
V_{OUT}	Selectable output voltage		0.5 Note 2	1.175	1.2	V
V_{OUT_LSB}	LSB of output voltage programming DAC (8-bit control)			5		mV
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable in 13 mA steps Note 3	At 90 % V_{OUT}	15	150	1211 Note 4	mA
$I_{OUT\_FUNC\_LIM}$	Functional current limit, programmable in 13 mA steps Note 3		15	1000	1211 Note 4	mA
Electrical Performance						
Static Parameters						
V_{OUT_PP}	Part to part output voltage accuracy Note 5	I_{OUT} = 1 mA T_A = 25 °C	-5		5	mV
V_{OUT_TEMP}	Temperature dependence of V_{OUT} Note 5	I_{OUT} = 1 mA Note 6	-1.1		1.1	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 5	I_{OUT} = 1 mA V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) to V_{IN} (Max)	-2		2	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_STATIC\_LD}$	Static load regulation Note 5	1 mA < I_{OUT} < I_{OUT_MAX}	-8		2	mV
$V_{DROPOUT}$	Dropout voltage	@ V_{OUT} = V_{OUT} (V_{IN} (Max)) - 10 mV I_{OUT} = I_{OUT_MAX} Note 6			80 Note 7	mV
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) + 100 mV to V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX} t_R = t_F = 100 mV/µs		2	5	mV
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) V_{OUT} = V_{OUT} (Typ) I_{OUT} = 1 mA to I_{OUT_MAX}/2 t_R = t_F = 1 µs		21	29	mV
t_{ON}	Turn-on time	Time to 90 % of V_{OUT} I_{OUT} = 0 mA C_{OUT} = 20 µF		0.15		ms
t_{OFF}	Turn-off time	Time to 10 % of V_{OUT} I_{OUT} = 0 mA C_{OUT} = 20 µF		2	5 Note 8	ms
AC Parameters						
$PSRR_{1kHz}$	Power supply rejection ratio	f = 1 kHz V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) + 200 mV V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX}/2		70		dB
$PSRR_{100kHz}$	Power supply rejection ratio	f = 100 kHz V_{IN} = V_{OUT} + $V_{DROPOUT}$ (Max) + 200 mV V_{OUT} = V_{OUT} (Typ) I_{OUT} = I_{OUT_MAX}/2		50		dB
V_N	Output noise	f = 10 Hz to 100 kHz I_{OUT} = I_{OUT_MAX}/2		100		µV
Current Limit Accuracy						
I_{OV_SINK}	Current sink at over-voltage	V_{OV} = V_{OUT} + 100 mV	10			mA
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current, no load	I_{OUT} = 0 mA Note 9		8	15	µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{Q\_ON\_1mA}$	Quiescent current, low load	I_{OUT} = 1 mA Note 9		10	16	µA
$I_{Q\_ON\_IMAX}$	Quiescent current, I_{OUT_MAX}	I_{OUT} = I_{OUT_MAX} Note 9		0.35	1.5	mA
R_{PD_OFF}	Output pull down resistance	V_{OUT} = 0.5 V LDO disabled		35	100	Ω

Note 1 For currents less than 400 mA, a minimum of 1.2 µF (after derating) can be used.

Note 2 Output is capable down to 0.4 V at reduced accuracy. Please contact Dialog Semiconductor for more information

Note 3 Accuracy ±30 %

Note 4 LDO5 and 6 share a supply pin and so their combined current limit must not exceed 1.5 A.

Note 5 The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$.

Note 6 Spec guaranteed for V_{DD_CTRL} ≥ 2.8 V.

Note 7 Dropout voltage is linear with the load current. If using a lower I_{OUT_MAX} than specified, the dropout can be calculated using 10 mV per 100 mA of load.

Note 8 Max t_{OFF} of 20 ms achieved for C_{OUT} = 80 µF.

Note 9 Internal regulator current flowing to ground.

2.9.1 Load Switch Mode Characteristics

Table 10: Load Switch Mode Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		0.5 Note 1 Note 2		1.25	V
I_{OUT_MAX}	Maximum output current		800			mA
Programmable Conditions						
SR	Slew rate, programmable to (4, 6, 8, 10) mV/µs		4		10	mV/µs
I_{LIM}	Current limit, programmable from 15 mA to 1.211 A in 13 mA steps Note 3		15		1211 Note 4	mA
Electrical Performance						
R_{ON}	On resistance			40		mΩ
SR_{ACC}	Slew rate accuracy		-35		35	%
I_{LIM_ACC}	Current limit accuracy		-35		35	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_OFF}	Quiescent current in off mode	T_A = 25 °C			2	µA

Note 1 Input is capable down to 0.4 V. Please contact Dialog Semiconductor for more information

Note 2 Register bit SEL_BYP_VGATE must be set to 0 for V_{IN} between 0.5 V and 0.8 V, and is recommended to be set to 1 for V_{IN} between 0.8 V and 1.25 V.

Note 3 Current limit is guaranteed for V_{IN} > 0.7 V. Below 0.7 V, a functional current limit is not guaranteed.

Note 4 Load switch 1 and 2 share a supply pin and so their combined current limit must not exceed 1.5 A.

2.10 VREF, IREF, Temperature Supervision Characteristics

Table 11: VREF, IREF, Temperature Supervision Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable Conditions						
V_{REF}	Reference voltage	Internal VREF		1.2		V
T_{WARN}	Warning temperature threshold, programmable to (90, 100, 110, 120) °C		90		120	°C
T_{WARN_HYS}	Warning temperature hysteresis, programmable to (0, 14) °C			14		°C
Electrical Performance						
V_{REF_ACC}	Reference voltage accuracy	Internal VREF	-1		1	%
T_{OT}	Thermal shutdown over-temperature		125	140	155	°C
T_{WARN_ACC}	Warning temperature threshold accuracy		-5		5	°C

2.11 Internal Oscillator Characteristics

Table 12: Internal Oscillator Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
f_{CLK}	Internal clock frequency		7.2	8	8.8	MHz

2.12 UVLO Characteristics

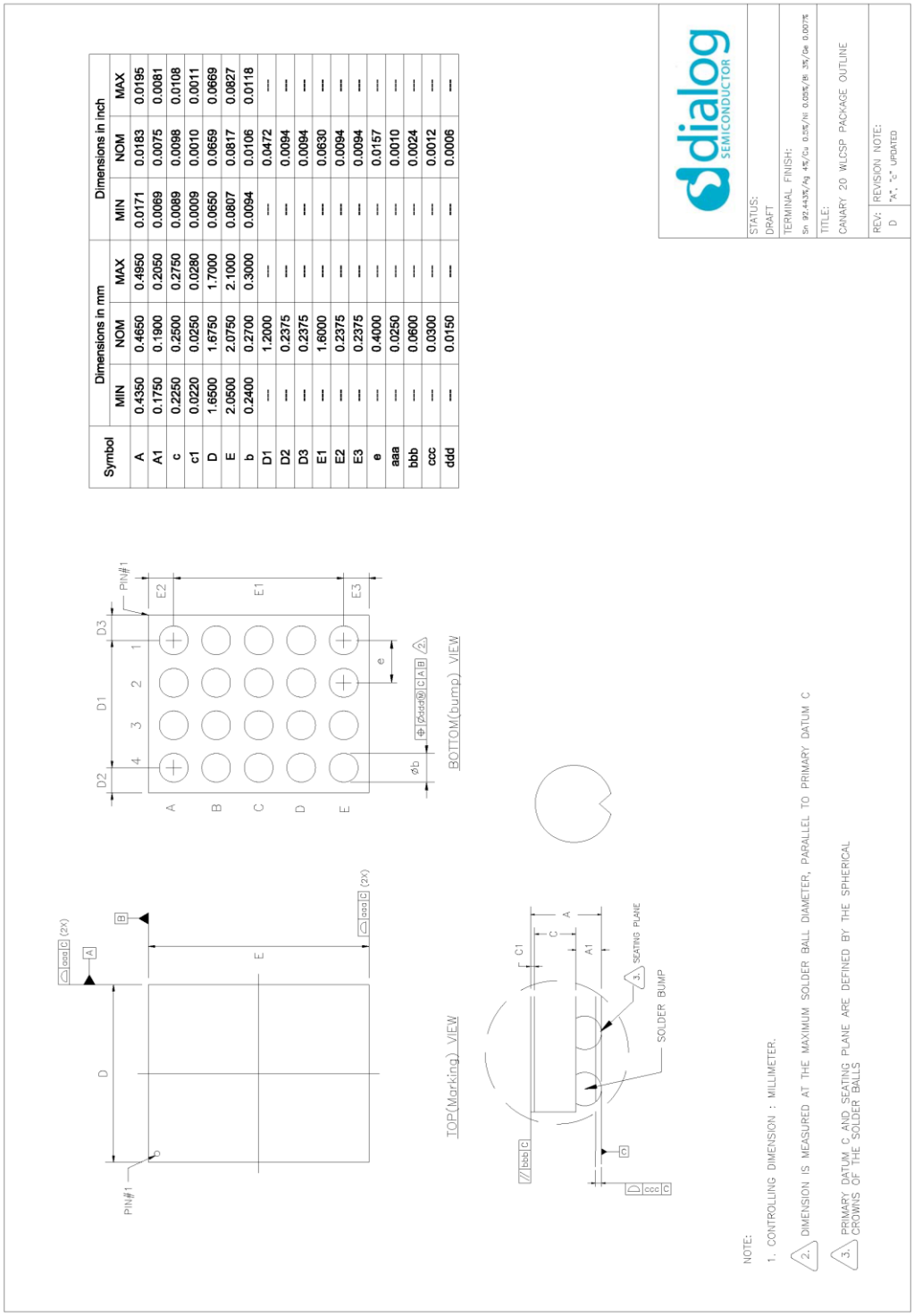
Table 13: UVLO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable Conditions						
$V_{DD\_UVLO\_LWR}$	Under-voltage lower threshold (falling edge) Note 1		2.215		2.658	V
$V_{DD\_UVLO\_UPPER}$	Under-voltage upper threshold (rising edge)			VDD_UVLO_LWR + 3 %		V
Electrical Performance						
$V_{DD\_POR\_UPPER}$	Deep discharge lockout upper threshold			2.1	2.2	V
$V_{DD\_POR\_LWR}$	Deep discharge lockout lower threshold			1.9		V
$V_{DD\_UVLO\_STAT\_ACC}$	Under-voltage lower threshold static accuracy with flip gate bandgap reference		-1.5		1.5	%

Note 1 This voltage is programmed from OTP in 24.6 mV steps.

3 Package Information

3.1 Package Outlines



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.4350	0.4650	0.4950	0.0171	0.0183	0.0195
A1	0.1750	0.1900	0.2050	0.0069	0.0075	0.0081
c	0.2250	0.2500	0.2750	0.0089	0.0098	0.0108
c1	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
D	1.6500	1.6750	1.7000	0.0650	0.0659	0.0669
E	2.0500	2.0750	2.1000	0.0807	0.0817	0.0827
b	0.2400	0.2700	0.3000	0.0094	0.0106	0.0118
D1	---	1.2000	---	---	0.0472	---
D2	---	0.2375	---	---	0.0094	---
D3	---	0.2375	---	---	0.0094	---
E1	---	1.6000	---	---	0.0630	---
E2	---	0.2375	---	---	0.0094	---
E3	---	0.2375	---	---	0.0094	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.0250	---	---	0.0010	---
bbb	---	0.0600	---	---	0.0024	---
ccc	---	0.0300	---	---	0.0012	---
ddd	---	0.0150	---	---	0.0006	---

Figure 2: Package Outline Drawing

3.2 PCB Landing Pattern

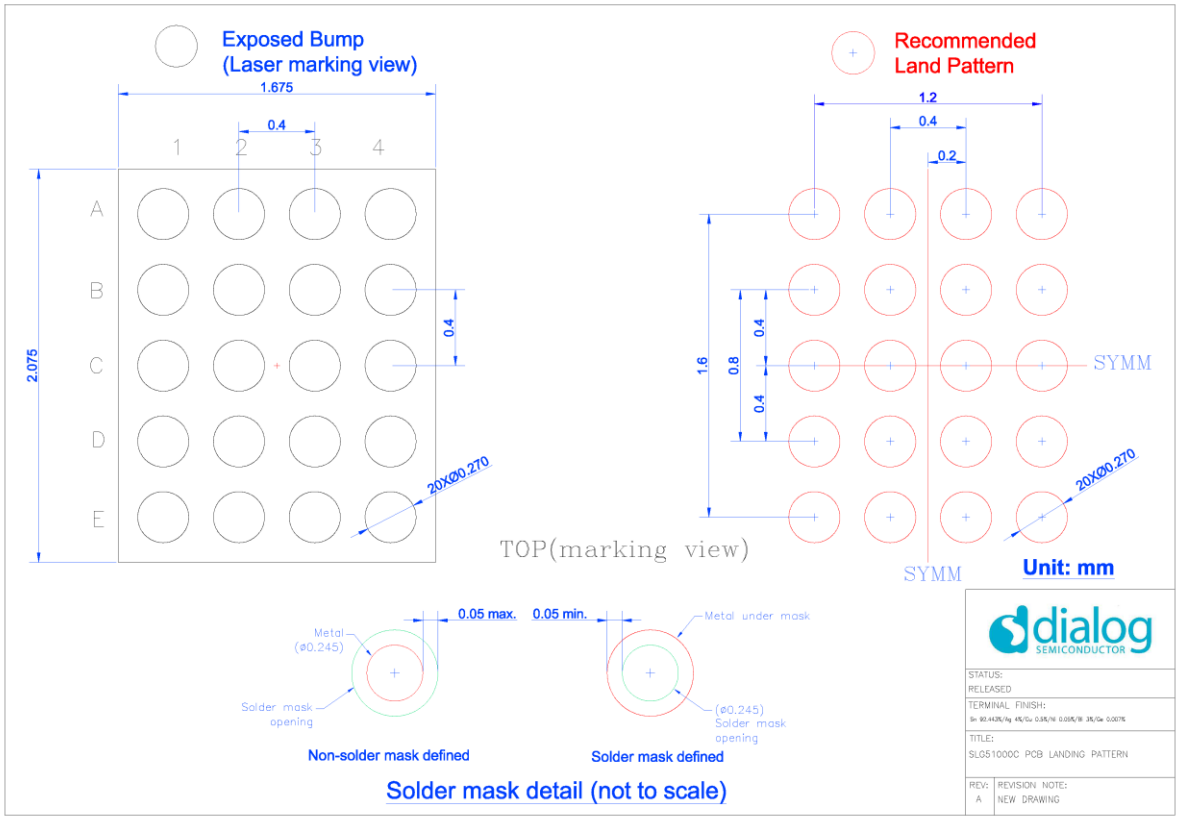


Figure 3: PCB Landing Pattern

3.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 14

.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

MSL rating does not apply to this device as it is not plastic encapsulated.

Table 14: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

3.4 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

3.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

4 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 15: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
SLG51000CTR	WLCSP-20	1.675 x 2.075	T & R	

5 Layout Recommendation

To ensure stability and best performance:

1. Place input and output decoupling capacitors as close to their respective device pins as possible, on same side as the device, and connected via wide tracks and paralleled vias to reduce inductance.
2. Separate VIN, VDD and VOUT grounds by star connecting these grounds to the main GND as close to the GND ball as possible. Avoid sharing of GND return paths of decoupling caps to chip. Avoid GND loops between input supplies (VIN, VDD) and VOUT. See Figure 4**.**
3. Use wide tracks where possible for high current carrying paths such as VIN and VOUT.
4. Do not allow VIN and VOUT routes to run alongside each other too closely for too long a length. This may cause crosstalk or coupling effects.
5. Place VIN and VOUT grounds directly above the VDD plane for high PSRR LDOs.

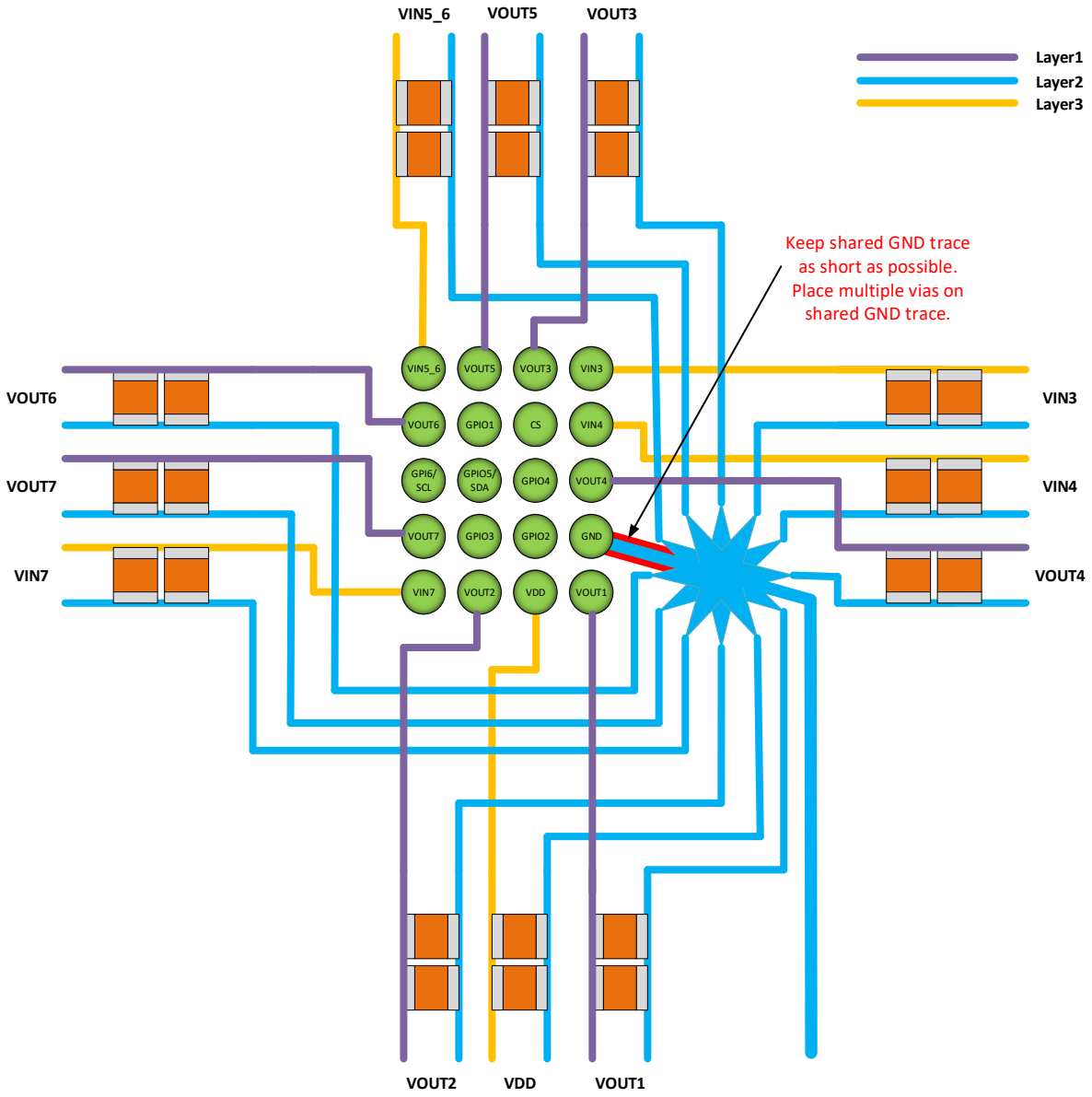
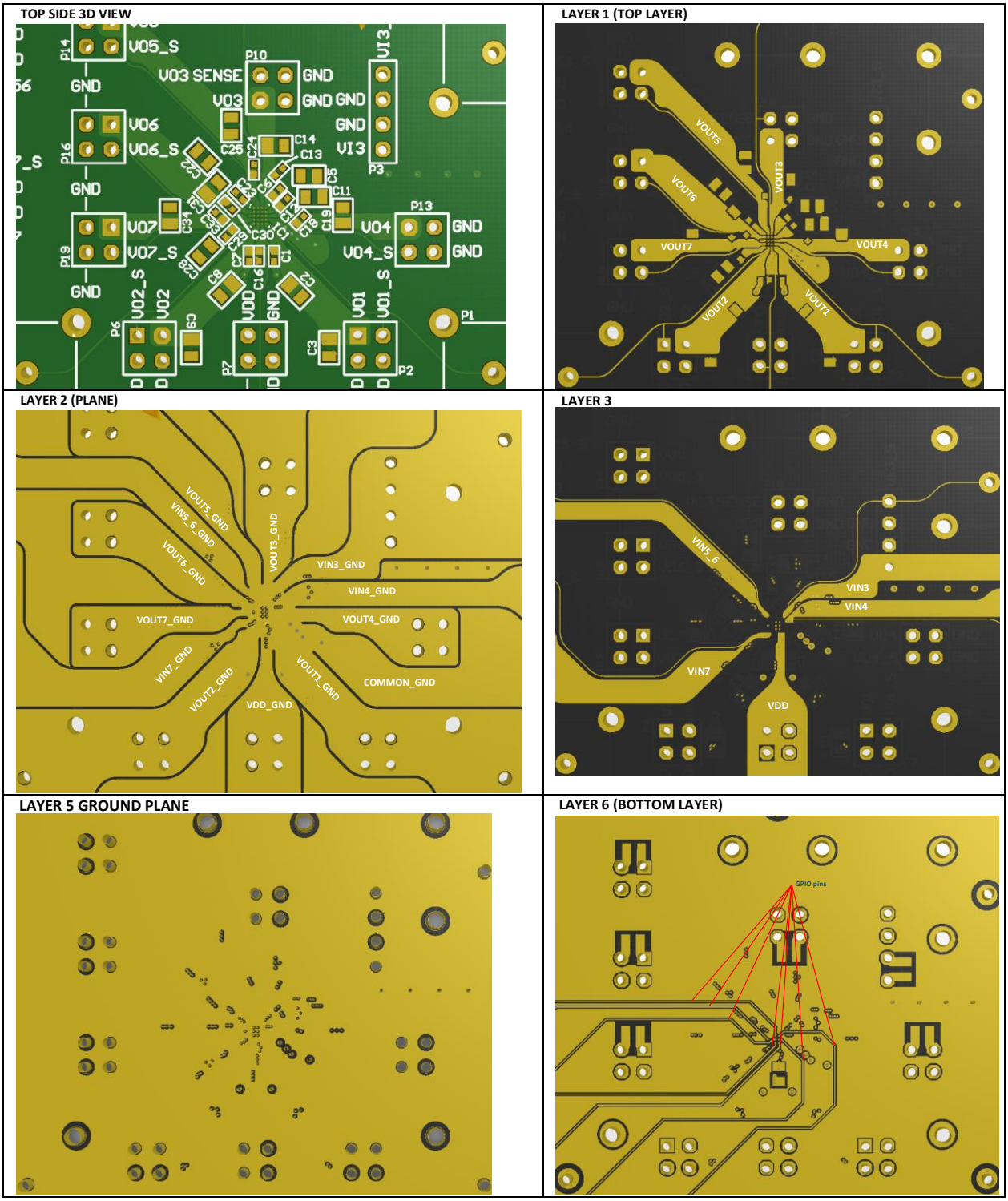


Figure 4: Star point for LDO Ground connection

Table 16: PCB layers recommendation view



Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via website
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.