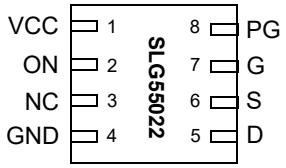
Features

- 12 V Power supply
- Drain Voltage Range 1.0 V to 20 V
- Internal Gate Voltage Charge Pump
- Controlled Turn on Delay
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- 2mm x 2mm TDFN-8 Package
- Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

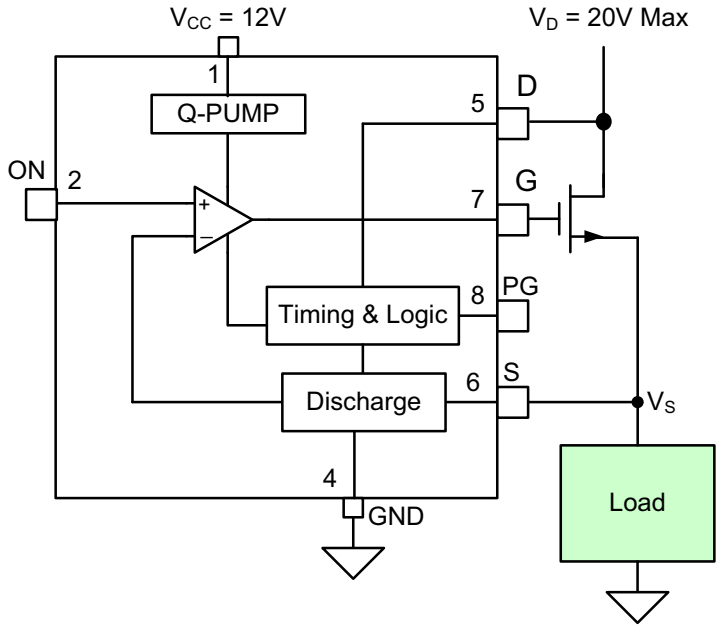


8-pin TDFN
(Top View)

Applications

- Power Rail Switches
- Hot Plugging Applications
- Soft Switching
- Personal computers and Servers
- Data Communications Equipment

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
VCC	1	Power	Supply Voltage
ON	2	Input	CMOS Logic Level. High True
NC	3	--	No Connect.
GND	4	GND	Ground.
D	5	Input	FET Drain Connection
S	6	Input	Source Connection
G	7	Output	FET Gate Drive
PG	8	Output	Output CMOS Open Drain - Power Good, indicates external FET fully on. Pull-up resistor greater than 300 kΩ recommended.

Overview

The SLG55022 N-Channel FET Gate Driver is used for controlling a delayed turn on and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the SLG55022 also integrates circuits to discharge opened switched voltage rails. The gate driver is available in a variety of configurations supporting a range of turn-on slew rates from 0.80 V/ms up to 4 V/ms which, depending on load supplying source voltages in the range of 1.0 V to 20 V results in ramp times from 200µs to over 20 ms (see Application Section). Delays until the ramp begins are source voltage independent and range from 250µs to 5ms. A power good condition is output to indicate that the ramp-up slew of the source voltage is finished. Additionally, an internal discharge circuit provides a controlled path to remove charge from open power rails. The SLG55022 gate drive is packaged in an 8 pin DFN package.

When used with external N-Channel FETs, the SLG55022 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0V to 20V.

Ordering Information

Part Number	Type
SLG55022-200030V	TDFN-8
SLG55022-200030VTR	TDFN-8 - Tape and Reel (3k units)

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_D or V_S to GND	-0.3	40.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C
ESD Human Body Model	--	2000	V
ESD Machine Model	--	200	V
Moisture Sensitivity Level	1		

Electrical Characteristics

T_A = -10 °C to 75 °C

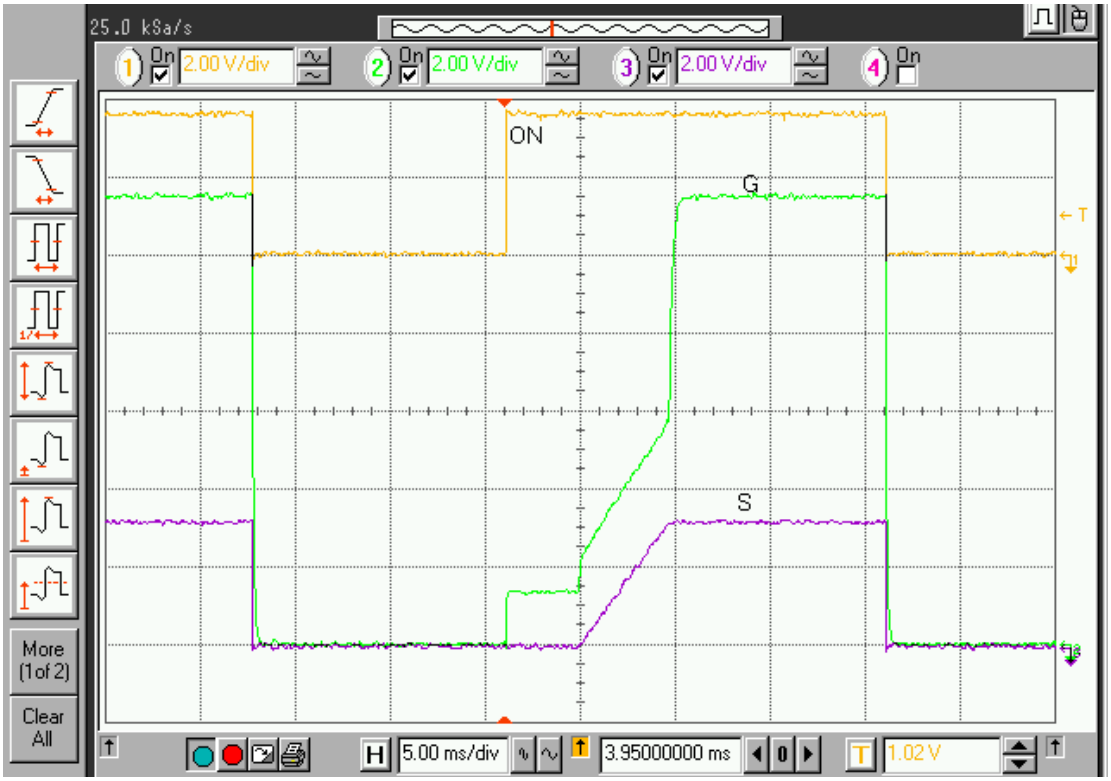
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		11.5	12.0	12.5	V
T_{VCC_RAMP}	V_{CC} Ramp-up Rate	See Note 1	0.25	--	--	V/ms
I_q	Quiescent Current	V_G not ramping FET = ON		50	80	µA
		V_G not ramping FET = OFF		0.1	1	µA
V_D	FET Drain Voltage		1.0	--	21	V
V_{GS}	Gate-Source Voltage		8.0	11.5	16	V
C_G	FET Gate Capacitance		500	--	8000	pF
T_{DELAY}	Ramp Delay Range	1.5ms Default, 500µs step	0	500	750	µs
T_{SLEW}	FET Turn on Slew Rate		1.2	2.0	2.8	V/ms
$I_{DISCHARGE}$	Internal Discharge Resistor	Nominal discharge time of ~100ms 10mA max rate	180	300	420	Ω
V_{IH}	HIGH-level input voltage	ON (200mV Hysteresis)	2.4	--	5.5	V
V_{IL}	LOW-level Input voltage	ON (200mV Hysteresis)	--	--	0.4	V
V_{OH}	HIGH-level output voltage	PG Open Drain	--	--	5.5	V
I_{OL_LOGIC}	Logic LOW level output	PG Sink Current	1	2	3	mA
I_{IH}*	HIGH-level input current	V_{IH} = 3.3V	--	--	<1.0	µA

Notes:
1. If T_{VCC_RAMP} > 5V/ms and ON is asserted, Gate charging will begin after 1ms.

Device Operation

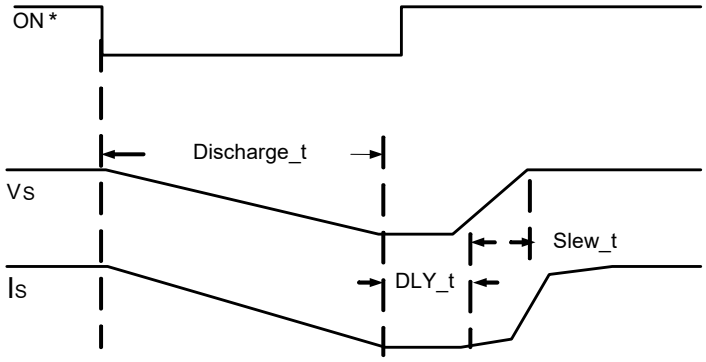
In a typical application, de-asserting ON (low) turns off the external power N-FET. When the FET is turned off, the voltage at the load is discharged through a resistor (300 Ohms) internal to the SLG55022. When ON is asserted (high), the device will not begin driving the gate of the external power FET unless the voltage at the drain of the device is at or above 0.8 V (e.g. $V_D \geq 0.8$ V) to prevent a 'shoothrough' situation to the FET's source load. Gate voltage is not applied to the gate of the external power N-FET after DLY_t then the gate source (Vgs) voltage is ramped up to 11.5V above the source voltage V_S at a slew rate determined by the internal slew rate control element internal to the SLG55022. Monotonic rise of Vs is maintained even as ID increases dramatically after the load device turn on threshold voltage is reached. After the source voltage has ramped up to its maximum steady state value, the Open Drain PG (Power Good) signal is asserted. PG may be used as the ON control of a second SLG55022 thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other PG signals to indicate all switched power rails are in a power good condition.

The waveforms shown illustrate the monotonic rise of the source voltage of a FET as gate voltage is controlled to accommodate for variations in load current as the voltage is applied.



Delay Time and Slew Rates

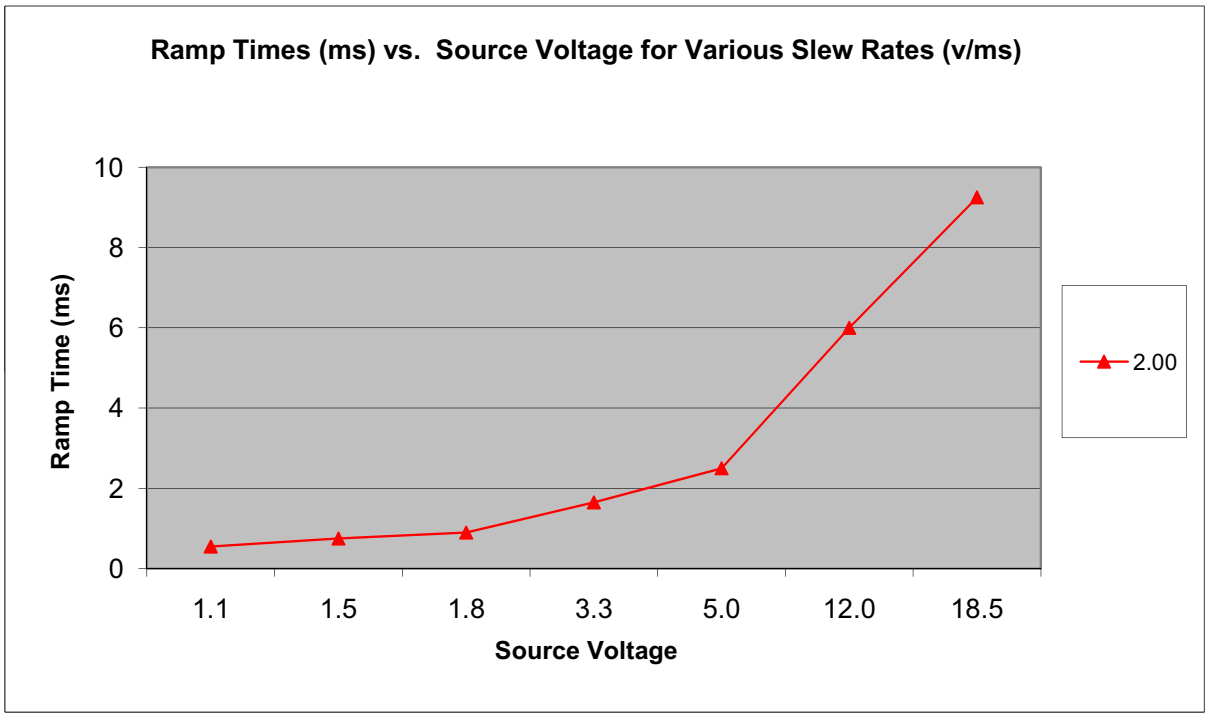
The two components of controlling the application of FET source voltage to the load are a fixed time delay before beginning turn on of the FET (DLY_t below) and the Slew Time of the source voltage (Slew_t below).



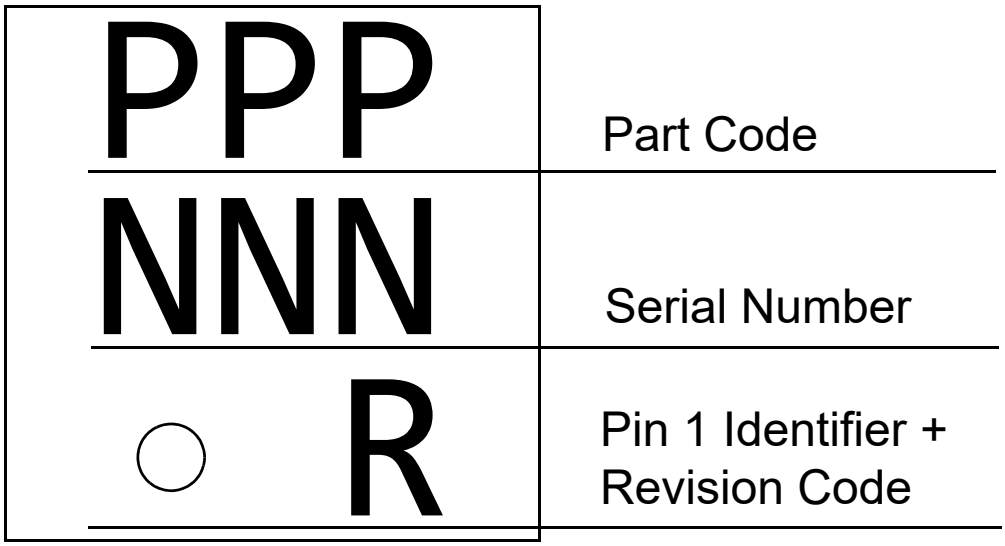
Having control over the Slew Rate of the FET's source voltage as the FET is turning on is important in controlling dv/dt caused transients. A power FET, for example, switching a 5 V rail which has a total of 500 µF of decoupling, fully on in 10 µs will generate a 250 A current surge which is very undesirable. If the FET turn on time can be stretched to 1 ms, the current surge to charge the decoupling capacitors is reduced to 2.5 A. The SLG55022 controls slew rate of a FET's source voltage as it is turned on. A range of slew rates are available as device order options. Obviously the time to fully slew the source voltage to fully on is a function of the drain supply voltage. The table and graph below shows source voltage ramp times for various slew rates supported by the SLG55022 for a range of specific source voltages.

Slew Rates (V/ms)	Ramp Times (ms) vs. Source Voltages (V)						
	1.1 V	1.5 V	1.8 V	3.3 V	5.0 V	12 V	18.5 V
2.00	0.55	0.75	0.90	1.65	2.50	6.00	9.25

* The minimum time that ON can be de-asserted between switching cycles is 100 ms.

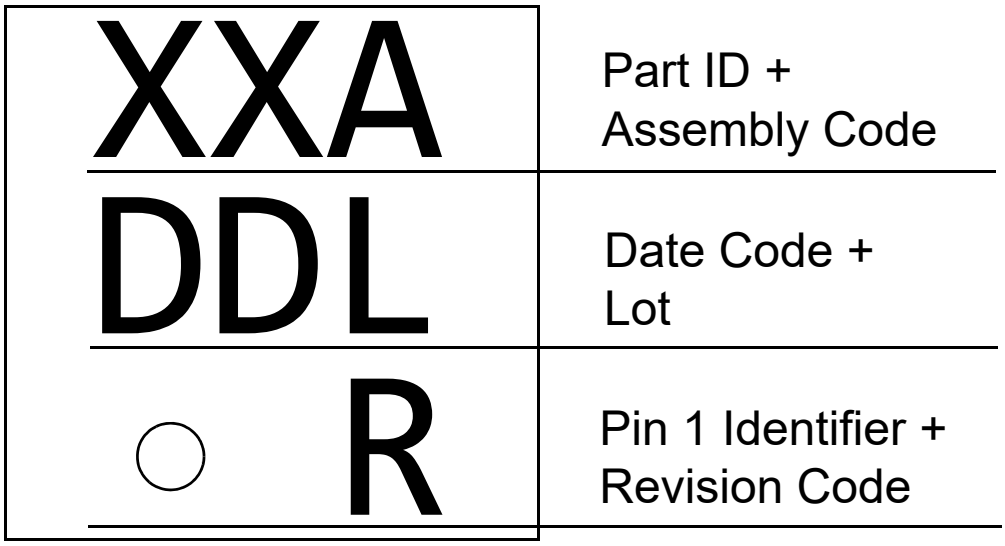


Package Top Marking System Definition
For devices manufactured after 2021



PPP - Part Code Field: Identifies the specific device Configuration
NNN - Serial Number Field: Serial number
R - Revision Code Field: Device Revision

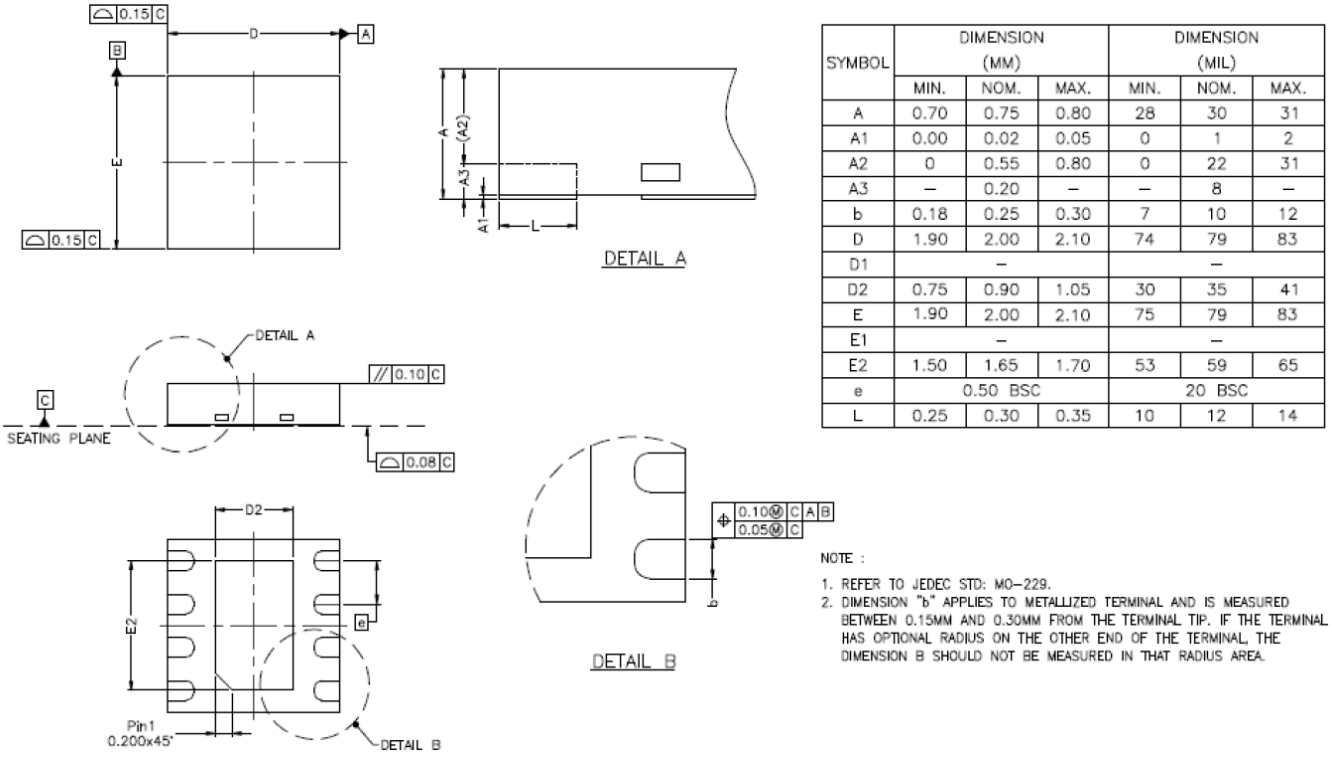
For devices manufactured before 2021



XX - Part ID Field: Identifies the specific device Configuration
A - Assembly Code Field: Assembly Location of the device
DD - Date Code Field: Coded Date of Manufacture
L - Lot Code: Designates Lot #
R - Revision Code: Device Revision

Package Drawing and Dimensions

8 Lead TDFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.50	1.65	1.70	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

NOTE :

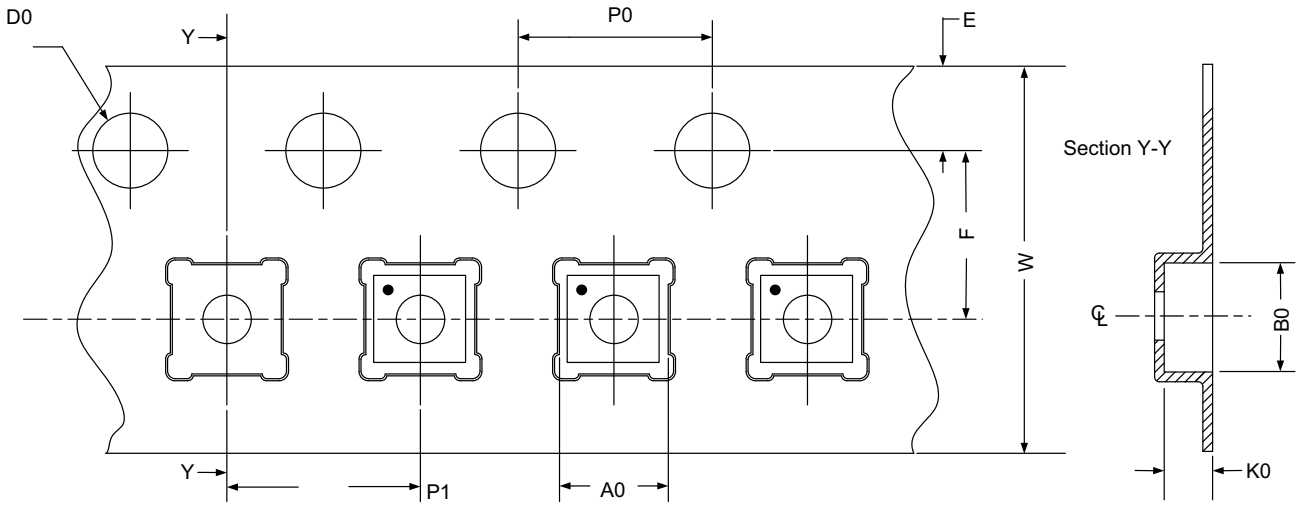
1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
6/8/2023	1.05	Updated Part Marking Definition
2/9/2022	1.04	Updated Company name and logo Fixed typos
7/10/2018	1.03	Updated style and formatting
7/29/2017	1.02	Added Pb-Free/Halogen Free/RoHS compliance Added MSL

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.