Dual Power High Voltage Gate Driver

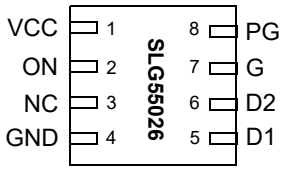
Features

- 12 V Power supply
- Drain Voltage Range 1.0 V to 20 V
- Internal Gate Voltage Charge Pump
- Controlled Turn on Delay
- Controlled Turn on Slew Rate
- 2mm x 2mm TDFN-8 Package

Applications

- Power Rail Switches
- Hot Plugging Applications
- Soft Switching
- Personal computers and Servers
- Data Communications Equipment

Pin Configuration

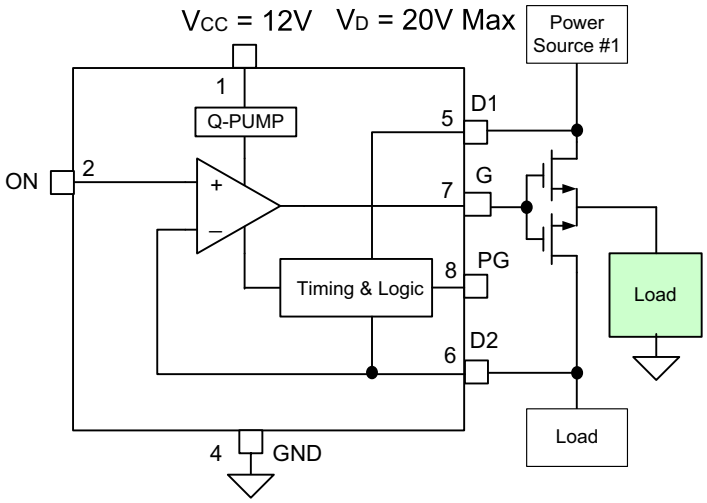


8-pin TDFN
(Top View)

Environmental

- Pb-Free / RoHS compliant
- Halogen Free

Block Diagram



SLG55026
For N-MOSFETS with 8V < V_{GD2} < 16V

Pin Description

Pin #	Pin Name	Type	Pin Description
1	VCC	Power	Supply Voltage
2	ON	Input	CMOS Logic Level. High True
3	NC	--	No Connect.
4	GND	GND	Ground.
5	D1	Input	FET1 Drain Connection
6	D2	Input	FET2 Drain Connection
7	G	Output	FET Gate Drive
8	PG	Output	Output Open Drain - Power Good, indicates external FET fully on. Pull-up resistor greater than 300kΩ recommended.

Overview

The SLG55026-200300V N-Channel FET Gate Driver is used for controlling a delayed turn on and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. The gate driver exhibits a turn-on slew rate of 2 V/ms which, depending on load supplying source voltages in the range of 1.0 V to 20 V results in ramp times from 500 µs to over 10 ms (see Application Section). Start up ramp delay is 250 µs. A power good condition is output to indicate that the ramp-up slew of the source voltage is finished. The SLG55026 gate driver is packaged in an 8 pin TDFN package.

When used with external N-Channel FETs, the SLG55026 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0 V to 20 V.

Ordering Information

Part Number	Type
SLG55026-200300V	TDFN-8
SLG55026-200300VTR	TDFN-8 - Tape and Reel (3k units)

Configuration Options

Code	Slew Rate (V/ms)	Delay (ms)	Discharge (Ω)
200300	2.0	0.25	Open

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{D1} or V_{D2} to GND	-0.3	40.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Operating temperature range	-55	125	°C
Junction temperature	--	150	°C
ESD Human Body Model	--	2000	V
ESD Machine Model	--	200	V

Electrical Characteristics (0°C to 70°C)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		11.5	12.0	12.5	V
T_{VCC_RAMP}	V_{CC} Ramp-up Rate	See Note 1	0.25	--	--	V/ms
I_q	Quiescent Current	V_G not ramping FET = ON	--	50	80	µA
		V_G not ramping FET = OFF	--	0.1	1	µA
V_{D1}	FET Drain Voltage		1.0	--	20	V
V_{D2}	Gate-Drain Voltage		8.0	11.5	16	V
C_G	FET Gate Capacitance		500	--	16000	pF
T_{DELAY}	Ramp Delay Range		--	0.25	0.325	ms
T_{SLEW}	FET Turn on Slew Rate	2.0V/ms config option	1.4	2.0	2.6	V/ms
$I_{DISCHARGE}$	Internal Discharge Resistor		--	Open	--	Ω
V_{IH}	HIGH-level input voltage	ON (200mV Hysteresis)	2.4	--	5.5	V
V_{IL}	LOW-level Input voltage	ON (200mV Hysteresis)	--	--	0.4	V
V_{OH}	HIGH-level output voltage	PG Open Drain	--	--	5.5	V
I_{OL_LOGIC}	Logic LOW level output	PG Sink Current (0.4V)	--	0.02	--	mA

Note 1: If T_{VCC_RAMP} > 5 V/ms and ON is asserted, Gate charging will begin after 1 ms.

Device Operation

In a typical application, de-asserting ON (low) turns off the external power N-FET. When ON is asserted (high), the device will not begin driving the gate of the external power FET unless the voltage at the drain of the device is at or above 1 V (e.g. $V_{D1} \geq 1$ V). Gate voltage is applied to the gate of the external power N-FET after T_{DELAY} then the gate drain (V_{GD2}) voltage is ramped up to 11.5V above the output voltage V_{D2} at a slew rate determined by the internal slew rate control circuit in SLG55026. Monotonic rise of V_{D2} is maintained even as ID increases dramatically after the load device turn on threshold voltage is reached. After the output voltage has ramped up to its maximum steady state value, the Open Drain PG (Power Good) signal is asserted. PG may be used as the ON control of a second SLG55026 thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other PG signals to indicate all switched power rails are in a power good condition.

If the ON signal has been asserted prior to the application of V_{CC}, the device will begin turning on the external power FET after V_{CC} ramps up

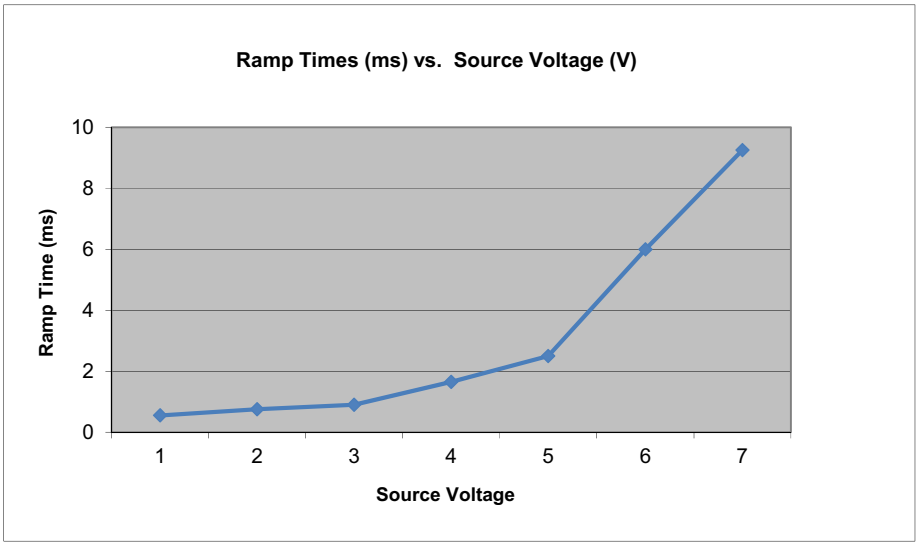
Delay Time and Slew Rates

The two components of controlling the application of FET source voltage to the load are a fixed time delay before beginning turn on of the FET (T_{DELAY}) and the Ramp Time of the output voltage. The Delay Time before gate voltage to the FET is applied is 250µs, independent of FET drain voltage, source voltage or SLG55026 supply voltage.

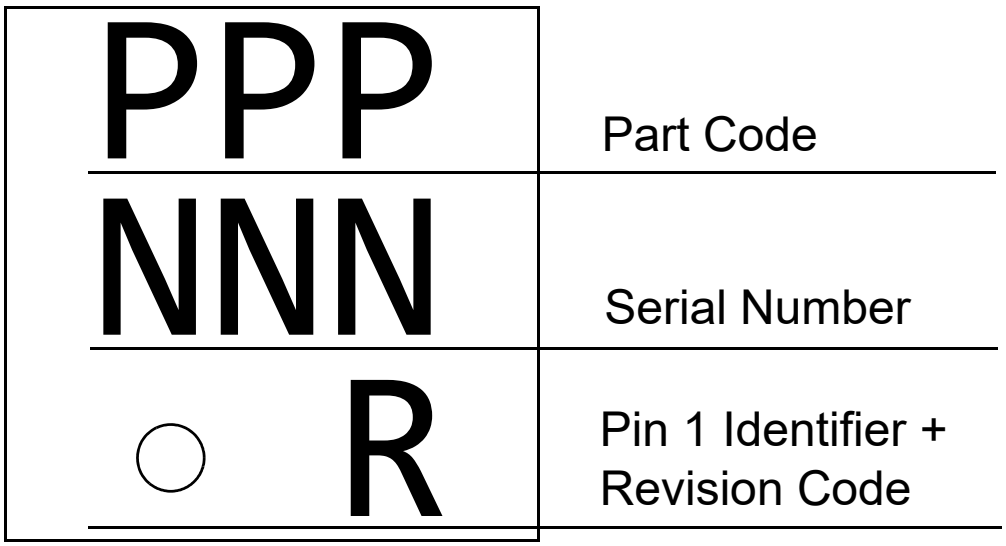
During FET turn on, it is important to control transients (caused by dv/dt) by being able to control the Slew Rate of the FET's output voltage. A power FET, for example, switching a 5 V rail which has a total of 500 µF of decoupling, fully on in 10µs will generate a 250 A current surge which is very undesirable. If the FET turn on time can be stretched to 1ms, the current surge to charge the decoupling capacitors is reduced to 2.5 A. The SLG55026 controls slew rate of a FET's output voltage as it is turned on. Obviously, the time to fully slew the output voltage to fully on is a function of the drain supply voltage. The table and graph below shows output voltage ramp times for a 2 V/ms slew rate supported by the SLG55026 for a range of specific source voltages.

Slew Rate (V/ms)	Ramp Times (ms) vs. Source Voltages (V)						
	1.1 V	1.5 V	1.8 V	3.3 V	5.0 V	12 V	18.5 V
2.00	0.56	0.76	0.90	1.66	2.50	6.00	9.26

* The minimum time that ON can be de-asserted between switching cycles is 100 µs.

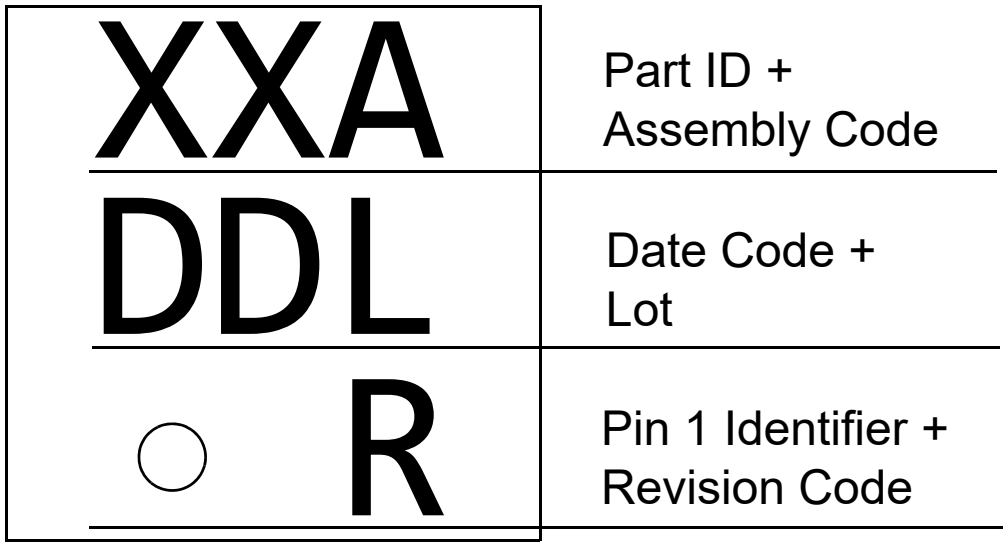


Package Top Marking System Definition
For devices manufactured after 2021



PPP - Part Code Field: Identifies the specific device Configuration
NNN - Serial Number Field: Serial number
R - Revision Code Field: Device Revision

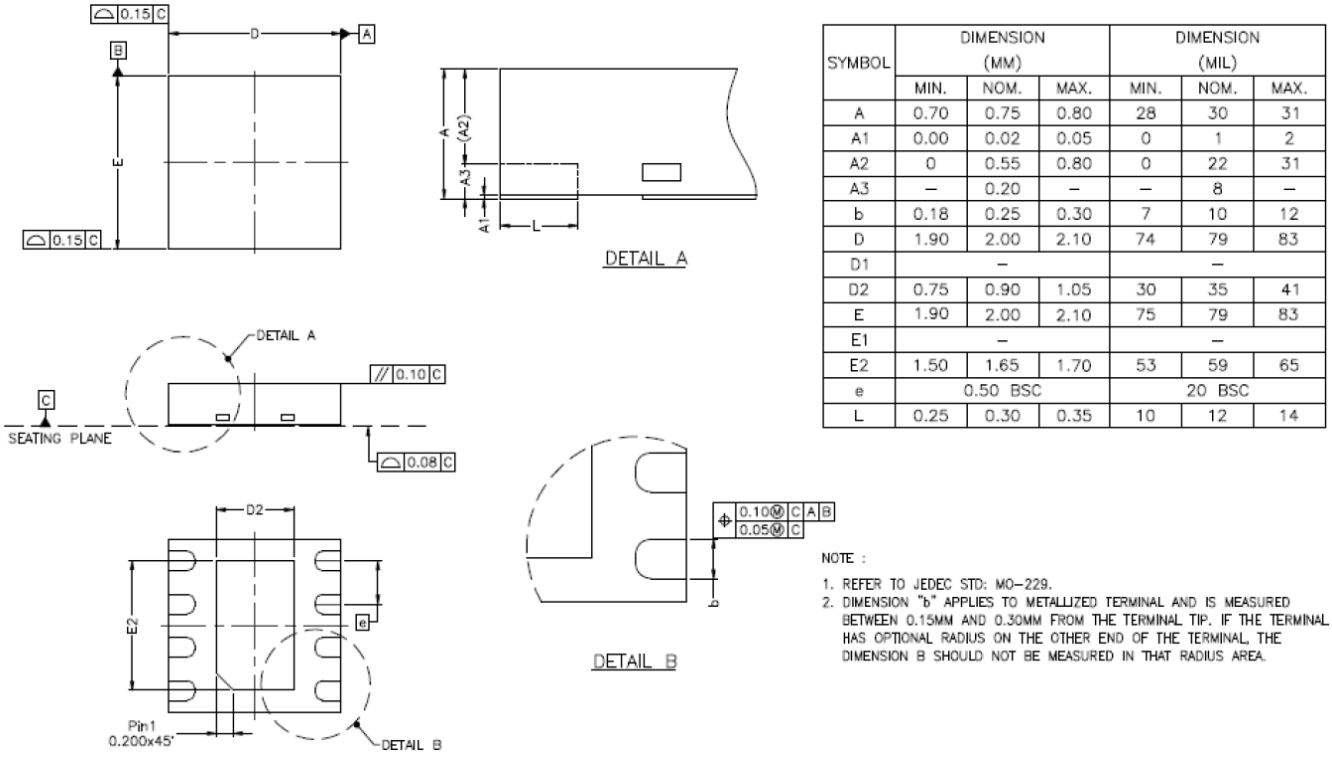
For devices manufactured before 2021



XX - Part ID Field: Identifies the specific device Configuration
A - Assembly Code Field: Assembly Location of the device
DD - Date Code Field: Coded Date of Manufacture
L - Lot Code: Designates Lot #
R - Revision Code: Device Revision

Package Drawing and Dimensions

8 Lead TDFN Package
JEDEC MO-229, Variation WCCD



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.50	1.65	1.70	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

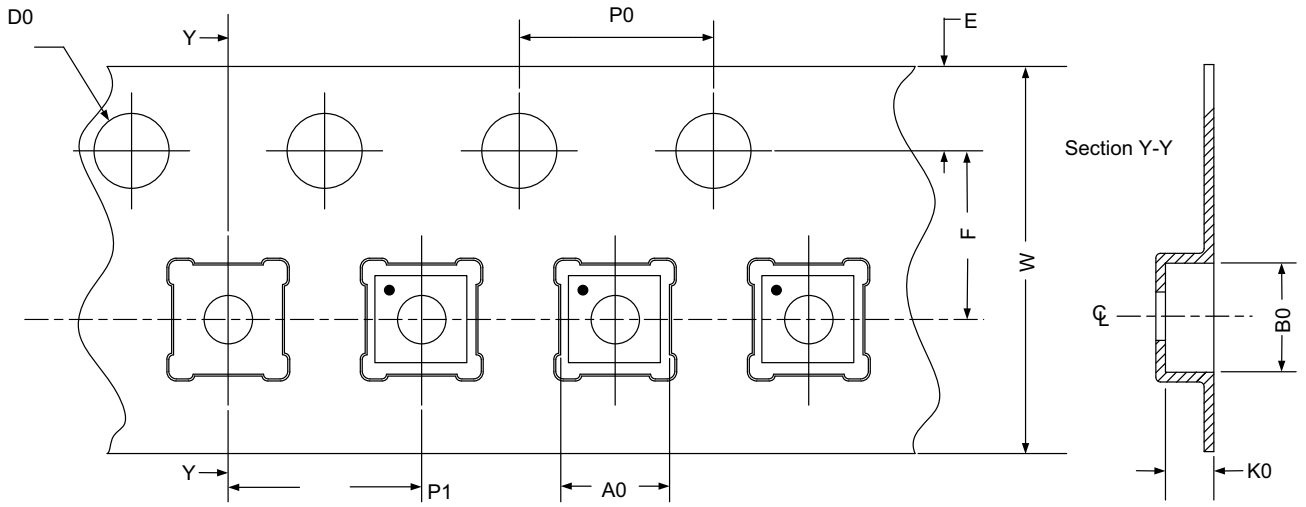
NOTE :
1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
6/8/2023	1.03	Updated Part Marking Definition
2/9/2022	1.02	Updated Company name and logo Fixed typos

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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