SLG55593
SLG55593A
USB Host Charger Identification Analog Switches

General Description

The SLG55593/SLG55593A is a USB device that combines high speed USB switches with a USB host charger (dedicated charger) identification circuit. The device supports both the latest USB Battery Charging Specification Revision 1.2 including data contact detection and a set resistor bias for Apple* compliant devices as well as legacy USB D+/D- short detection using data line pull-up.

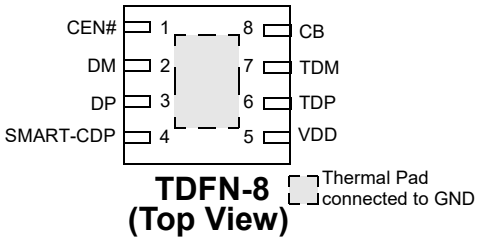
The SLG55593/SLG55593A can also support CDP mode (FAST charging and data communication available mode if smartphone can support CDP mode.)

The SLG55593/SLG55593A can also support low speed / full speed mouse/keyboard wake-up from S3 mode.

Features

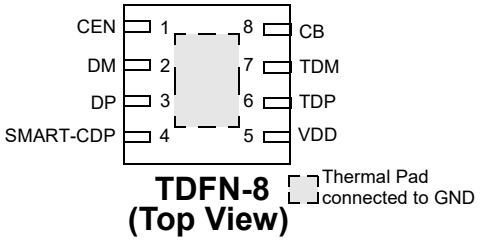
- High Speed USB Switching
- Low 4.0pF (typ) On Capacitance
- Low 4.0Ω (typ) On Resistance
- Low 0.5Ω (typ) On Resistance Flatness
- 4.5V to 5.5V Supply Range
- Low Supply Current
- Automatic Current-Limit Switch Control
- Automatic USB Charger Identification Circuit
- CDP Support (active USB 2.0 data communication with 1.5A charging)
- Apple iPad* @ 2A charging current support
- Automatic CDP/SDP mode support with SMART-CDP=1 for "Always Data Communication"
- Chinese Telecom Standard YD/T 1591-2009 specification support
- Samsung Galaxy Tab** charge scheme support
- Pb-Free / RoHS Compliant / Halogen-Free
- TDFN-8 Package

Pin Configuration - SLG55593



TDFN-8
(Top View)

Pin Configuration - SLG55593A



TDFN-8
(Top View)

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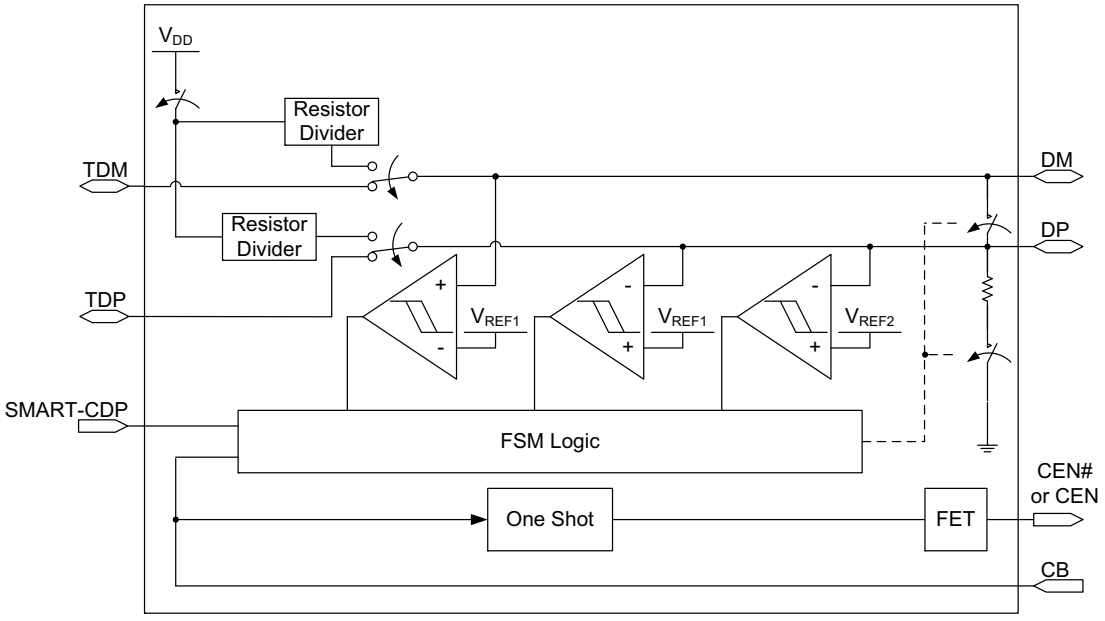
** Samsung Galaxy Tab are trademarks of Samsung Electronics, registered in Korea and other countries.

Block Diagram



Pin Description - SLG55593

Pin #	Pin Name	Type	Pin Description
1	CEN#	Output	P-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN# will be high for 2 seconds (typ)
2	DM	Input/Output	USB Connector D-
3	DP	Input/Output	USB Connector D+
4	SMART-CDP	Input	Input Control logic (see truth table)
5	VDD	PWR	Power Supply. Connect a 0.1µF capacitor between VDD and GND as close as possible to the device.
6	TDP	Input/Output	Host USB Transceiver D+ Connection
7	TDM	Input/Output	Host USB Transceiver D- Connection
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging downstream port with active USB2.0 data communication mode with 1.5A support
9	Thermal Pad	GND	Ground

Pin Description - SLG55593A

Pin #	Pin Name	Type	Pin Description
1	CEN	Output	N-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN will be low for 2 seconds (typ)
2	DM	Input/Output	USB Connector D-
3	DP	Input/Output	USB Connector D+
4	SMART-CDP	Input	Input Control logic (see truth table)
5	VDD	PWR	Power Supply. Connect a 0.1µF capacitor between VDD and GND as close as possible to the device.
6	TDP	Input/Output	Host USB Transceiver D+ Connection
7	TDM	Input/Output	Host USB Transceiver D- Connection
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging downstream port with active USB2.0 data communication mode with 1.5A support
9	Thermal Pad	GND	Ground

Truth Table

CB	SMART-CDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.

Ordering Information

Part Number	Type
SLG55593V	TDFN-8
SLG55593VTR	TDFN-8 - Tape and Reel
SLG55593AV	TDFN-8
SLG55593AVTR	TDFN-8 - Tape and Reel

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltage	-0.3	6.0	V
Continuous Current into any terminal	-30	+30	mA
Continuous Power Dissipation	--	954	mW
Operating Temperature Range	-40	85	°C
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10s)		260	°C

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics - Power Supply

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Range	$V_{CB} > V_{IH}$	4.5	5.0	5.5	V
		V_{CB} = 0V	4.75	--	5.25	V
I_{DD}	Supply Current V_{DD} = 5V	CB = LOW, SMART-CDP = X (autodetect with wakeup)	--	120	140	µA
		CB = HIGH, SMART- = LOW (SDP)	--	20	30	µA
		CB = HIGH, SMART- = HIGH (CDP)	--	40	70	µA

Electrical Characteristics - Analog Switch

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
V_{DP}, V_{DM}	Analog signal Range		0	--	V_{DD}	V
R_{ON}	On Resistance TDP/TDM Switch	V_{DD} = -0.4V to 0.4V, I = 10mA	--	3.5	--	Ω
		V_{DP} = V_{DM} = 0V to 3.3V V_{DD}= 5V	--	4.0	7	Ω
ΔR_{ON}	On Resistance Match between channels TDP/TDM Switch	V_{DD} = 5.0V V_{DP} = V_{DM} = 400mV I_{DP} = I_{DM} = 10mA	--	0.1	--	Ω
R_{FLAT}	On Resistance flatness TDP/TDM Switch	V_{DD} = 5.0V V_{DP} = V_{DM} = 0V to V_{DD} I_{DP} = I_{DM} = 10mA	--	0.5	--	Ω
R_{SHORT}	On Resistance of TDP/TDM Short	V_{CB} = 0V V_{DP} = 1V I_{DP} = I_{DM} = 10mA	--	50	70	Ω
I_{TDPOFF}, I_{TDMOFF}	Off-Leakage Current	V_{DD} = 3.6V V_{DP} = V_{DM} = 0.3V to 3.3V V_{TDP} = V_{TDM} = 3.3V to 0.3V V_{CB} = 0V	-250	--	250	nA
I_{DPON}, I_{DMON}	Off-Leakage Current	V_{DD} = 3.6V V_{DP} = V_{DM} = 3.3V to 0.3V V_{CB} = V_{DD}	-250	--	250	nA

Electrical Characteristics - Dynamic Performance

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
T_{ON}	Turn On Time	V_{TDP} or V_{TDM} = 1.5V R_L = 300Ω C_L = 35pF	--‘	20	100	µs
T_{OFF}	Turn Off Time	V_{TDP} or V_{TDM} = 1.5V R_L = 300Ω C_L = 35pF	--‘	1	5	µs
T_{PLH}, T_{PHL}	TDP/TDM Switch Propagation Delay	R_L = R_S = 50Ω	--	60	--	ps
T_{SKEW}	Output Skew	Skew between DP and DM when connected to TDP and TDM R_L = R_S = 50Ω	--	40	--	ps
C_{OFF}	TDP/TDM Off-Capacitance	f = 1MHz	--‘	2.0	--	pF
C_{ON}	DP/DM On-Capacitance	f = 240MHz	--‘	4.0	5.5	pF
BW	-3dB Bandwidth	R_L = R_S = 50Ω	--	1000	--	MHz
V_{ISO}	Off-Isolation	V_{TDP}, V_{DP} = 0dBm R_L = R_S =5 0Ω f = 250MHz	--	-20	--	dB
V_{CT}	Crosstalk	V_{TDP}, V_{DP} = 0dBm R_L = R_S = 50Ω f = 250MHz	--	-25	--	dB

Electrical Characteristics - Internal Resistors

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
R_{PD}	DP/DM Short Pull-down		350	500	700	kΩ
RT_{RP}	RP1/RP2 Ratio		0.8544	0.863	0.872	Ratio
R_{RP}	RP1 + RP2 Resistance		69.75	93.0	115.18	kΩ
RT_{RM}	RM1/RM2 Ratio		1.485	1.5	1.515	Ratio
R_{RM}	RM1 + RM2 Resistance		93.75	125.0	156.25	kΩ

Electrical Characteristics - Logic Input CB

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
V_{IH}	CB Input Logic High		1.4	--	--	V
V_{IL}	CB Input Logic Low		--	--	0.4	V
I_{IN}	CB Input Leakage Current	V_{DD} = 5.5V $0 \le V_{CB} \le V_{IL}$ or $V_{IH} \le V_{CB} \le V_{DD}$	-1	--	1	µA

Electrical Characteristics - Logic Input SMART-CDP

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
V_{IH}	SMART-CDP input Logic High		3.0	--	--	V
V_{IL}	SMART-CDP input Logic Low		--	--	0.8	V
I_{IN}	SMART-CDP Input Leakage Current	V_{DD} = 5.5V 0V < $V_{SMART-CDP}$ < V_{IL} or V_{IH} < $V_{SMART-CDP}$ < V_{DD}	-1	--	1	µA

Electrical Characteristics - CEN#/CEN Outputs

V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

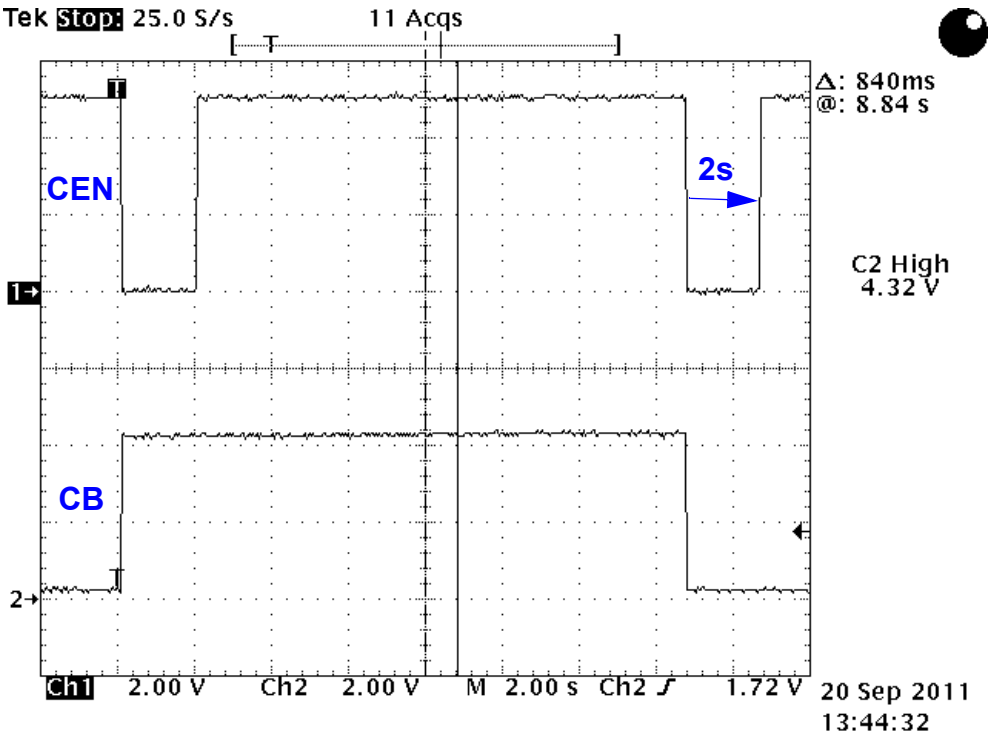
Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
T_{VBT}	V_{BUS} Toggle Time	CB = Logic 0 to Logic 1 or Logic 1 to Logic 0	1.5	2.0	2.5	s
$V_{OH\_CEN\#}$	CEN# Output Logic High Voltage	CB = Logic 0 to Logic 1 I_{SOURCE} = 2mA	V_{DD}-0.4V	--	--	V
$I_{OUT\_CEN\#}$	CEN# Output Leakage Current	V_{DD} = 5.5V $V_{CEN\#}$ = 0V or CEN# deasserted	--	--	1	µA
V_{OL_CEN}	CEN Output Logic Low Voltage	CB = Logic 0 to Logic 1 I_{SINK} = 2mA	--	--	0.4V	V
I_{OUT_CEN}	CEN Output Leakage Current	V_{DD} = 5.5V V_{CEN} = 5.5V or CEN deasserted	--	--	1	µA

Electrical Characteristics - ESD Protection

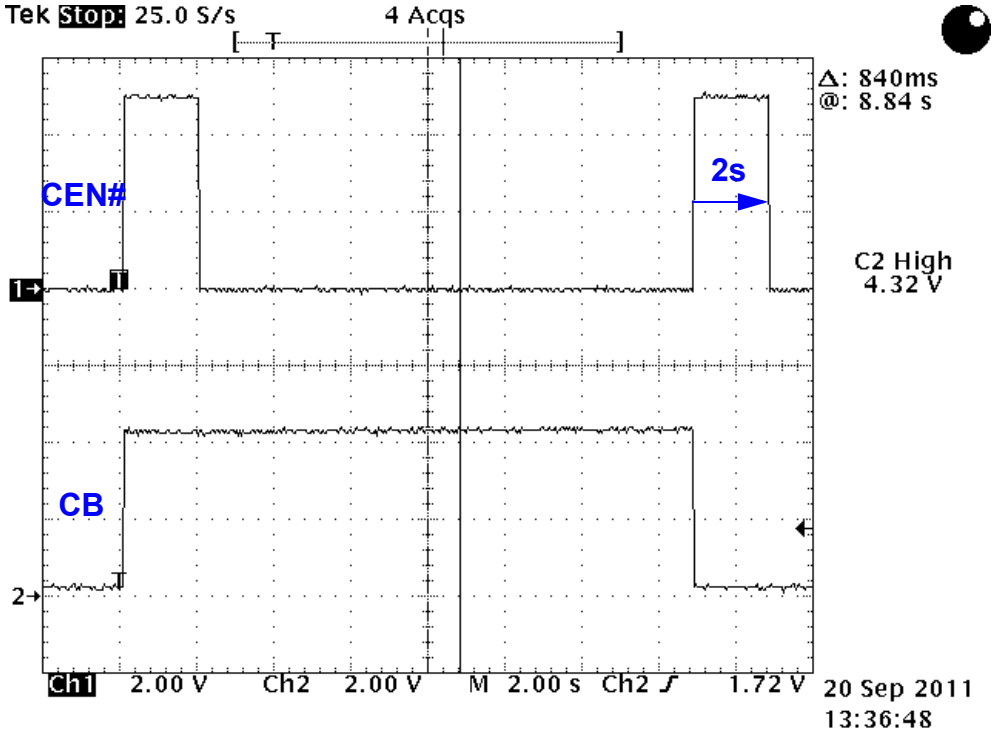
V_{DD} = 4.5V to 5.5V, T_A = 25°C (unless specified otherwise)

Parameter	Description	Condition/Note	Min.	Typ.	Max.	Unit
V_{ESD}	ESD Protection Level (DP and DM Only)	Human Body Model	--	±8	--	kV
V_{ESD}	ESD Protection Level (All other pins)	Human Body Model	--	±2	--	kV

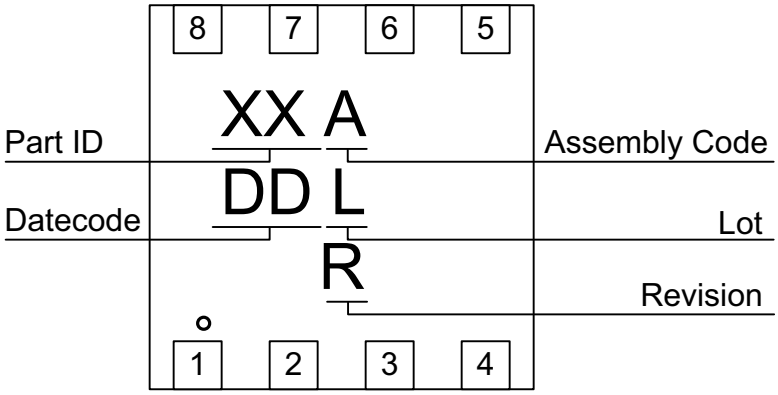
CEN Function Waveform



CEN# Function Waveform



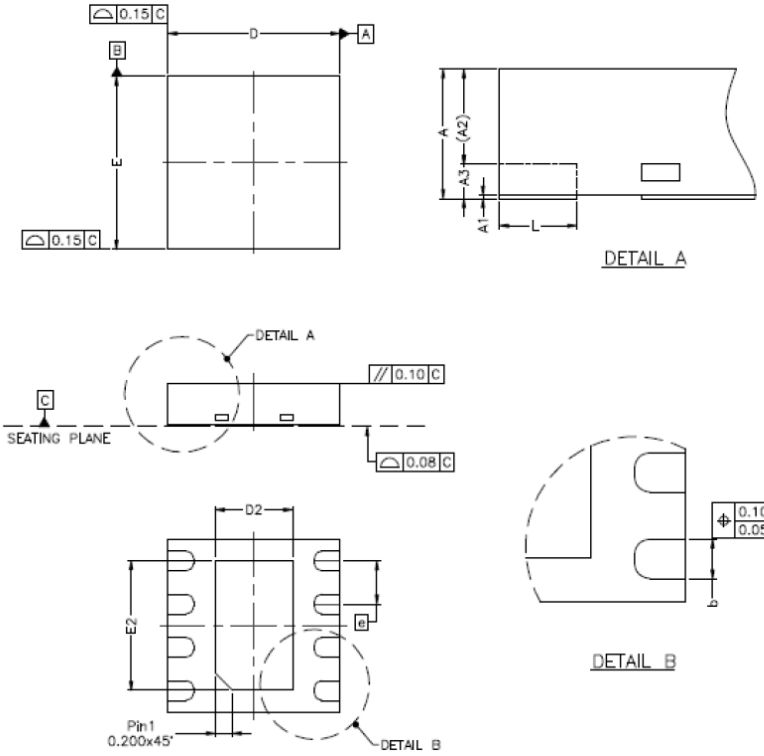
Package Top Marking System Definition



XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

Package Drawing and Dimensions

8 Lead TDFN Package
JEDEC MO-229, Variation WCCD



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.50	1.65	1.70	53	59	65
e		0.50 BSC			20 BSC	
L	0.25	0.30	0.35	10	12	14

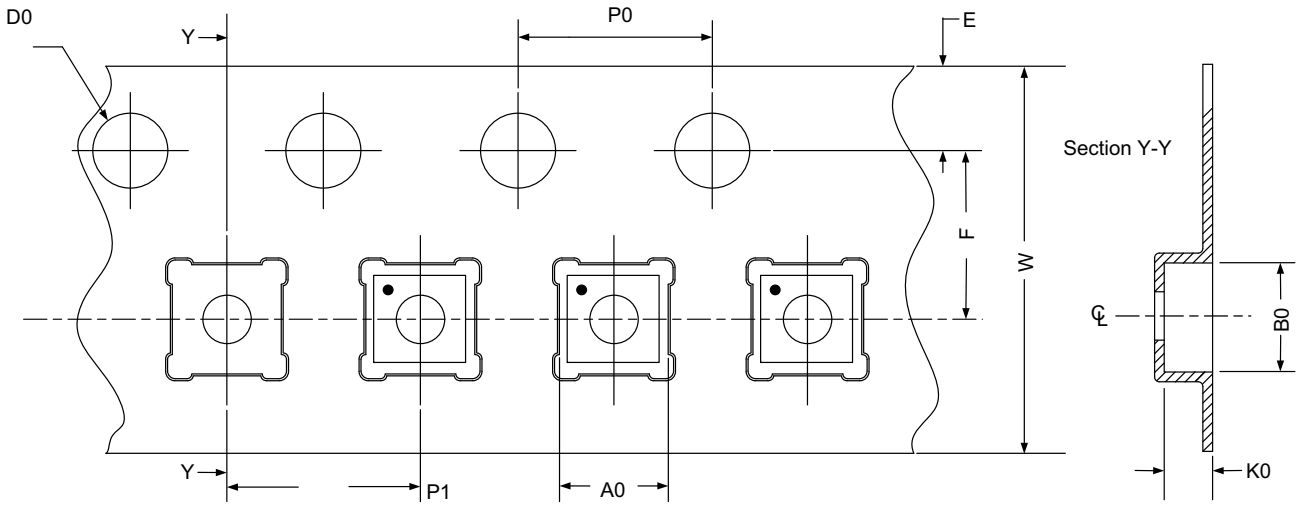
NOTE :
1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

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