A Reverse Blocking 70 mΩ, 1.5 A nFET Load Switch in 1.46 mm^2 WLCSP

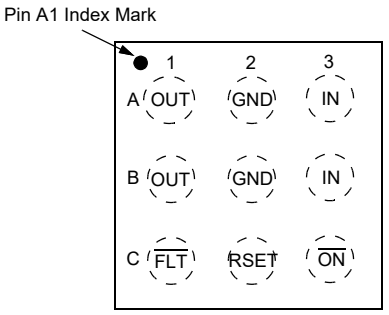
General Description

Operating from a 2.7 V to 5.5 V power supply, the SLG59H1342C is a self-powered, high-performance, 70 mΩ nFET load switch designed for high-side power-rail applications up to 1.5 A. When ON, internal reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a $V_{OUT} > V_{IN} + 50$ mV condition opens the switch). When OFF, an internal back-to-back reverse-current blocking circuit prevents reverse path leakage current.

Features

- Integrated 1.5 A Continuous I_{DS} nFET Load Switch
- Integrated Low RDS_{ON} nFET switch: 70 mΩ
- Input Voltage: 2.7 V to 5.5 V
- Operating Temperature: -40 °C to 85 °C
- Resistor-adjustable Active Current Limit
  - ±10% accuracy for 0.27 A to 1.81 A Current Limit Thresholds
  - ±15% accuracy for < 0.27 A Current Limit Thresholds
- Open Drain $\overline{FLT}$ Signaling
- Input Over-Voltage Protection
- Absolute V_{IN} maximum voltage rating: 28 V_{DC}
- Over-temperature Protection
- Under-Voltage Lockout
- True Reverse-Current Blocking
- Active Low ON signal control
- Low θ_{JA}, 9-pin 1.21 mm x 1.21 mm, 0.4 mm pitch 9L WLCSP Packaging
- Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

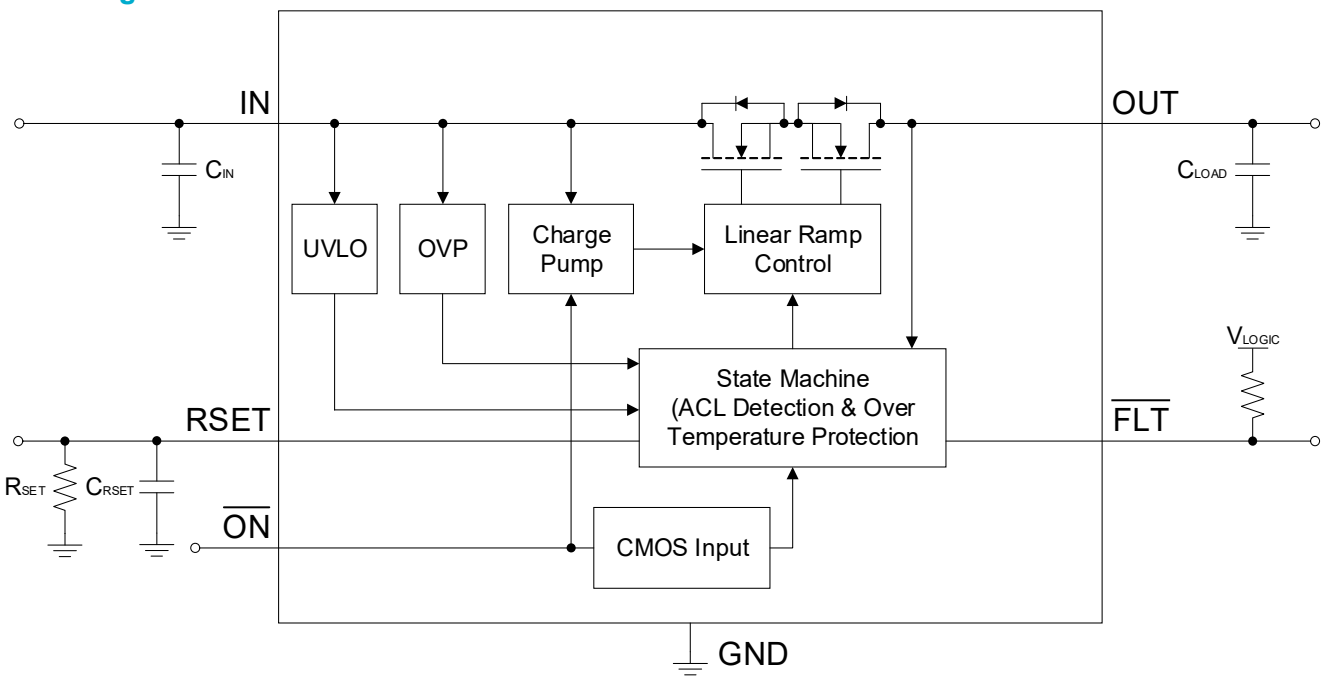


9L WLCSP
(Laser Marking View)

Applications

- Fast Turn On/Off power rail switching
- Frequent wake & sleep power cycle
- Mobile devices and portable devices

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A1, B1	OUT	MOSFET	Output terminal connection of the n-channel MOSFET. Capacitors used at OUT should be rated at a voltage higher than maximum input voltage ever present.
A2, B2	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.
A3, B3	IN	MOSFET	Input terminal connection of the n-channel MOSFET. Capacitors used at IN should be rated at a voltage higher than maximum input voltage ever present.
C1	$\overline{FLT}$	Output	An open drain output, $\overline{FLT}$ is asserted within $T\overline{FLT}_{LOW}$ when a current-limit condition is detected.
C2	RSET	Input	A 1%-tolerance, metal-film resistor between 6.49 kΩ and 604 Ω sets the SLG59H1342C's active current limit. A 6.49 kΩ resistor sets the SLG59H1342C's active current limit to 0.16 A and a 604 Ω resistor sets the active current limit to 1.81 A. In addition, it is recommended to bypass the RSET pin to GND with a 10 pF capacitor.
C3	$\overline{ON}$	Input	A high-to-low transition on this pin initiates the operation of the SLG59H1342C. ON is an asserted LOW, level-sensitive CMOS input with ON_V_{IL} < 0.65 V and ON_V_{IH} > 1.15 V. While there is an internal pull-down circuit to GND (~14 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.

Ordering Information

Part Number	Type	Production Flow
SLG59H1342C	WLCSP 9L	Industrial, -40 °C to 85 °C
SLG59H1342CTR	WLCSP 9L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage		--	--	28	V
V_{OUT} to GND	Power Switch Output Voltage to GND	Continuous	-0.3	--	6	V
$\overline{ON}$, $\overline{FLT}$, RSET to GND	$\overline{ON}$, $\overline{FLT}$, and RSET Pin Voltages to GND		-0.3	--	6	V
T_S	Storage Temperature		-65	--	140	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
ESD_{SYS}	IEC 61000-4-2 System ESD	Air Gap (V_{IN}, V_{OUT}, V_{ON} to GND)	15	--	--	kV
		Contact (V_{IN}, V_{OUT}, V_{ON} to GND)	8	--	--	kV
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.21 x 1.21 mm 9L WLCSP; Determined using a 0.5 in^2, 1 oz. copper pad under each IN and OUT terminal and FR4 pcb material.	--	76	--	°C/W
MOSFET IDS_{PK}	Peak Current from IN to OUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	2.1	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Typical values are at V_{IN} = 5 V, C_{IN} = 1 µF, C_{LOAD} = 1 µF, and T_A = 25 °C. Min/Max values are T_A = -40 °C to 85 °C; unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage	-40 °C to 85 °C	2.7	--	5.5	V
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	V_{IN} ↑	--	2.45	--	V
		V_{IN} ↓	--	2.25	--	V
$V_{IN(OVP)}$	V_{IN} Overvoltage Lockout Threshold	V_{IN} ↑	5.4	5.6	5.8	V
		V_{IN} ↓	--	5.3	--	V
$V_{IN(OVP)\_HYS}$	V_{IN} Overvoltage Lockout Hysteresis	V_{IN} ↓	--	300	--	mV
t_{OVP}	OVP Response Time	V_{IN} step from 5.5 V to 6 V; I_{DS} = 0.5 A, C_{LOAD} = 1 µF; T_A = 25 °C	1	--	10	µs
I_{IN}	Power Switch Current (Pin A3, B3)	When OFF, No load; V_{OUT} = Open; V_{ON} = 5 V	--	0.5	2	µA
		When ON, No load	--	80	115	µA
I_{ON_LKG}	$\overline{ON}$ Pin Input Leakage	V_{ON} = 0 V to 5 V	--	--	1	µA

Electrical Characteristics (continued)

Typical values are at V_{IN} = 5 V, C_{IN} = 1 µF, C_{LOAD} = 1 µF, and T_A = 25 °C. Min/Max values are T_A = -40 °C to 85 °C; unless otherwise noted.

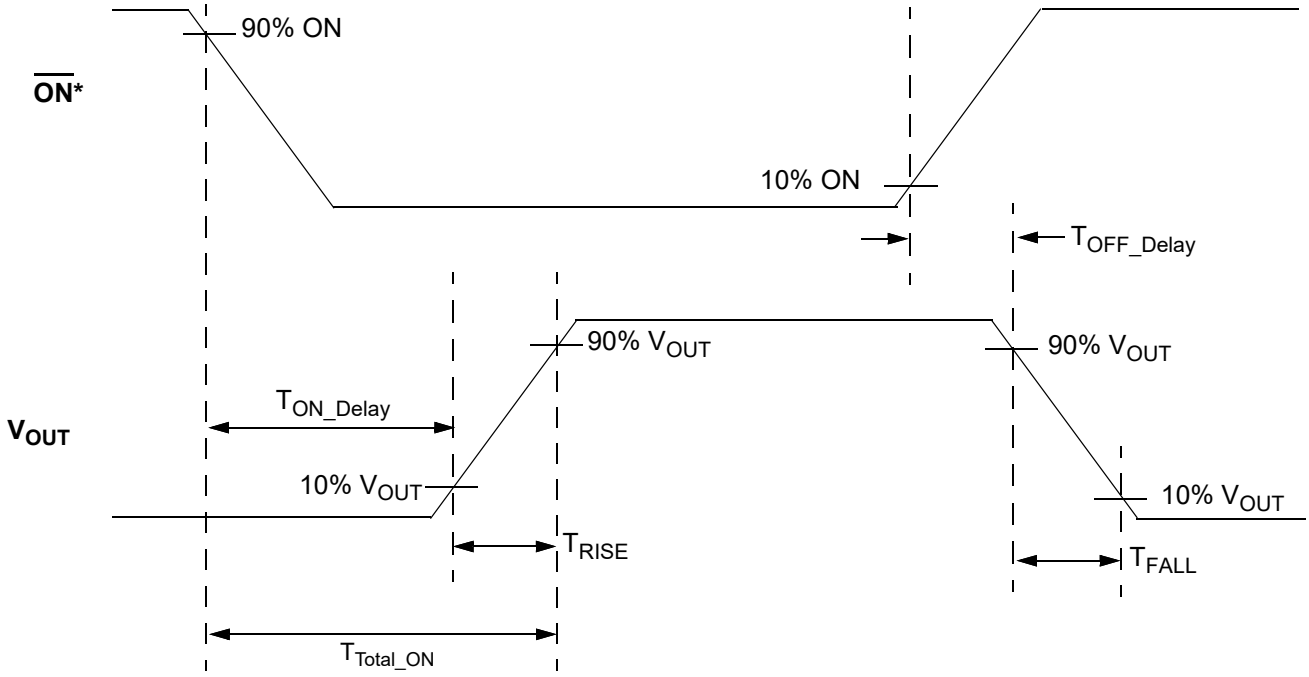
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
RDS_{ON}	ON Resistance	V_{IN} = 3.0 V, I_{DS} = 0.5 A	--	90	--	mΩ
		V_{IN} = 3.5 V, I_{DS} = 0.5 A	--	80	--	mΩ
		V_{IN} = 3.7 V, I_{DS} = 0.5 A	--	75	105	mΩ
		V_{IN} = 4.0 V, I_{DS} = 0.5 A	--	75	--	mΩ
		V_{IN} = 4.5 V, I_{DS} = 0.5 A	--	75	--	mΩ
		V_{IN} = 5.0 V, I_{DS} = 0.5 A	--	70	100	mΩ
		V_{IN} = 5.5 V, I_{DS} = 0.5 A	--	70	--	mΩ
MOSFET IDS	Current from IN to OUT	Continuous	--	--	1.5	A
I_{LIMIT}	Active Current Limit, I_{ACL}	V_{IN} = 5 V; R_{SET} = 2.1 kΩ; C_{IN} = 30 µF; C_{RSET} = 10 pF; V_{OUT} > 1.68 V; C_{LOAD} = 1 µF	0.47	0.52	0.57	A
		V_{IN} = 5 V; R_{SET} = 1.07 kΩ; C_{IN} = 30 µF; C_{RSET} = 10 pF; V_{OUT} > 1.68 V; C_{LOAD} = 4.4 µF	0.92	1.02	1.12	A
T_{ACL}	Active Current Limit Response Time	I_{DS} > I_{ACL}, V_{OUT} ≤ V_{IN}	--	7	--	µs
T_{HACL}	Hard Active Current Limit Response Time	I_{DS} > I_{ACL}, V_{OUT} = 0 V	--	6	--	µs
I_{FET_OFF}	MOSFET OFF Leakage Current	V_{ON} = 5.5 V; V_{OUT} = 0 V, V_{IN} = 5.5 V	--	0.5	4	µA
V_{RVD_T}	Reverse-voltage Detect Threshold Voltage	V_{OUT} – V_{IN};	--	50	--	mV
T_{RVD_T}	Reverse-voltage Detect Threshold Response Time		--	2	--	µs
V_{RVD_HYS}	Reverse-voltage Detect Hysteresis		--	50	--	mV
$I_{REVERSE}$	MOSFET Reverse Leakage Current	V_{IN} = 0 V, ON = HIGH, V_{OUT} = 5.5 V	--	10	--	µA
T_{ON_Delay}	ON Delay Time	90% ON to 10% V_{OUT} ↑; V_{IN} = 5 V; R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF	--	1.1	--	ms
T_{Total_ON}	Total Turn ON Time	90% ON to 90% V_{OUT} ↑; V_{IN} = 5 V; R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF	--	2.2	--	ms
T_{RISE}	V_{OUT} Rise Time	10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 5 V; R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF	--	1.1	--	ms
T_{OFF_Delay}	OFF Delay Time	10% ON to 90% V_{OUT} ↓; V_{IN} = 5 V; R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF	--	10	--	µs
T_{FALL}	V_{OUT} Fall Time	90% V_{OUT} to 10% V_{OUT}; ON = LOW-to-HIGH; V_{IN} = 5 V; R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF	--	250	--	µs
$T\overline{FLT}_{LOW}$	$\overline{FLT}$ Assertion Time	Abnormal Step Load Current event to $\overline{FLT}$ ↓;	--	8	--	ms
$\overline{FLT}_{VOL}$	$\overline{FLT}$ Output Low Voltage	I_{SINK} = 10 mA; V_{IN} = 5 V;	--	0.1	0.2	V
		I_{SINK} = 10 mA; V_{IN} = 3.5 V;	--	0.15	0.3	V
$I_{\overline{FLT}\_Leakage}$	$\overline{FLT}$ Output High Leakage Current	V_{IN} = 5 V; Switch is in On state	--	--	1	µA

Electrical Characteristics (continued)

Typical values are at V_{IN} = 5 V, C_{IN} = 1 µF, C_{LOAD} = 1 µF, and T_A = 25 °C. Min/Max values are T_A = -40 °C to 85 °C; unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ON_V_{IH}	High Input Voltage on $\overline{ON}$ pin	V_{IN} = 2.7 V to 5.5 V	1.15	--	--	V
ON_V_{IL}	Low Input Voltage on $\overline{ON}$ pin	V_{IN} = 2.7 V to 5.5 V	-0.3	0	0.65	V
$THERM_{ON}$	Thermal Protection Shutdown Threshold		--	150	--	°C
$THERM_{OFF}$	Thermal Protection Restart Threshold		--	130	--	°C

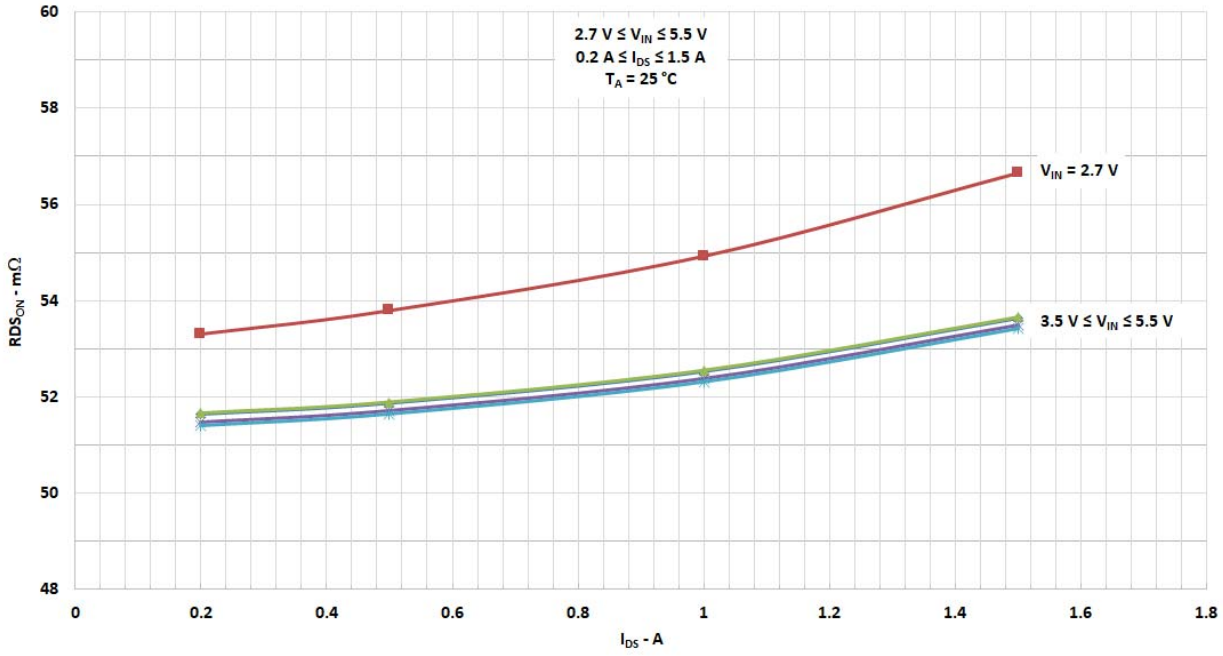
Timing Parameter Details



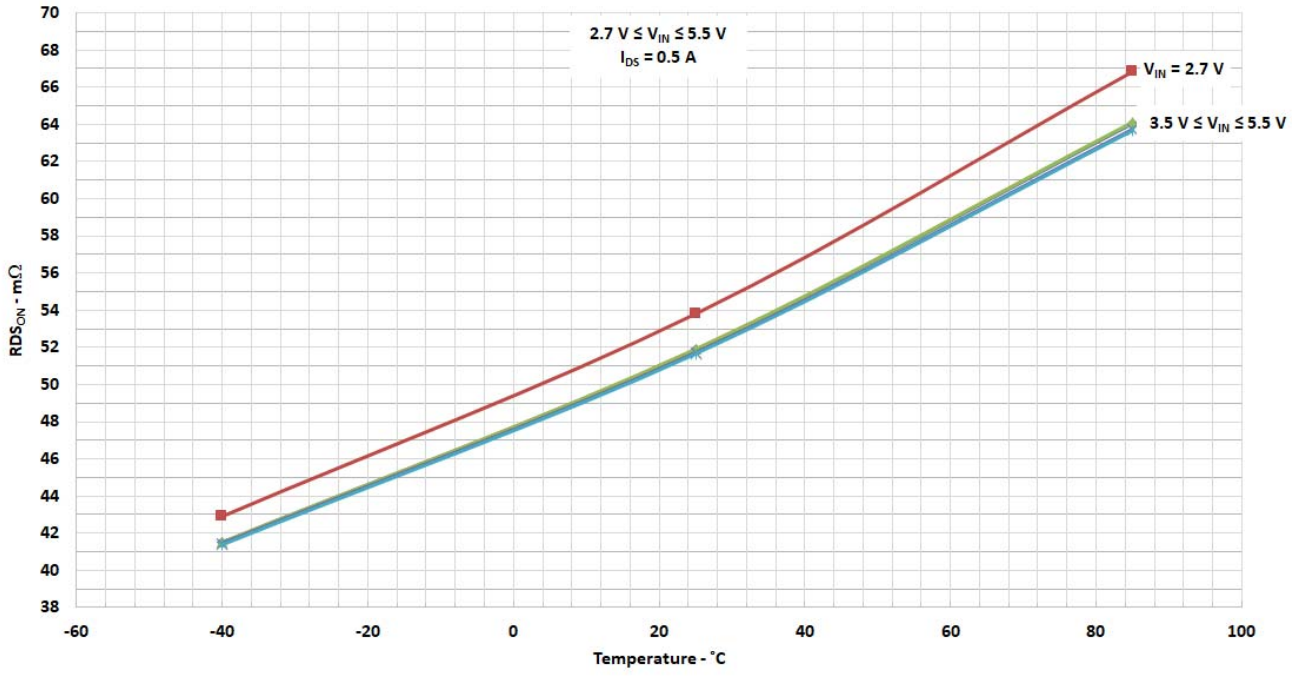
*Rise and Fall Times of the ON Signal are 100 ns

Typical Performance Characteristics

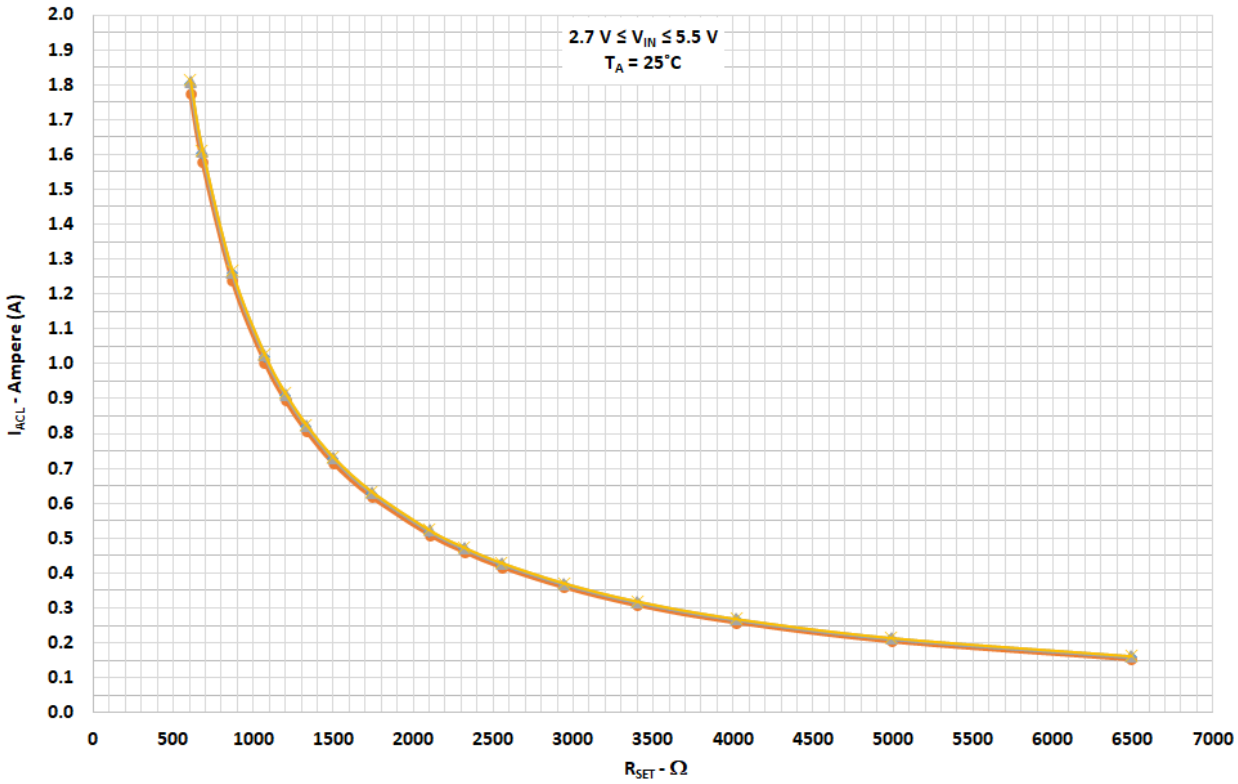
RDS_{ON} vs. I_{DS} and V_{IN}



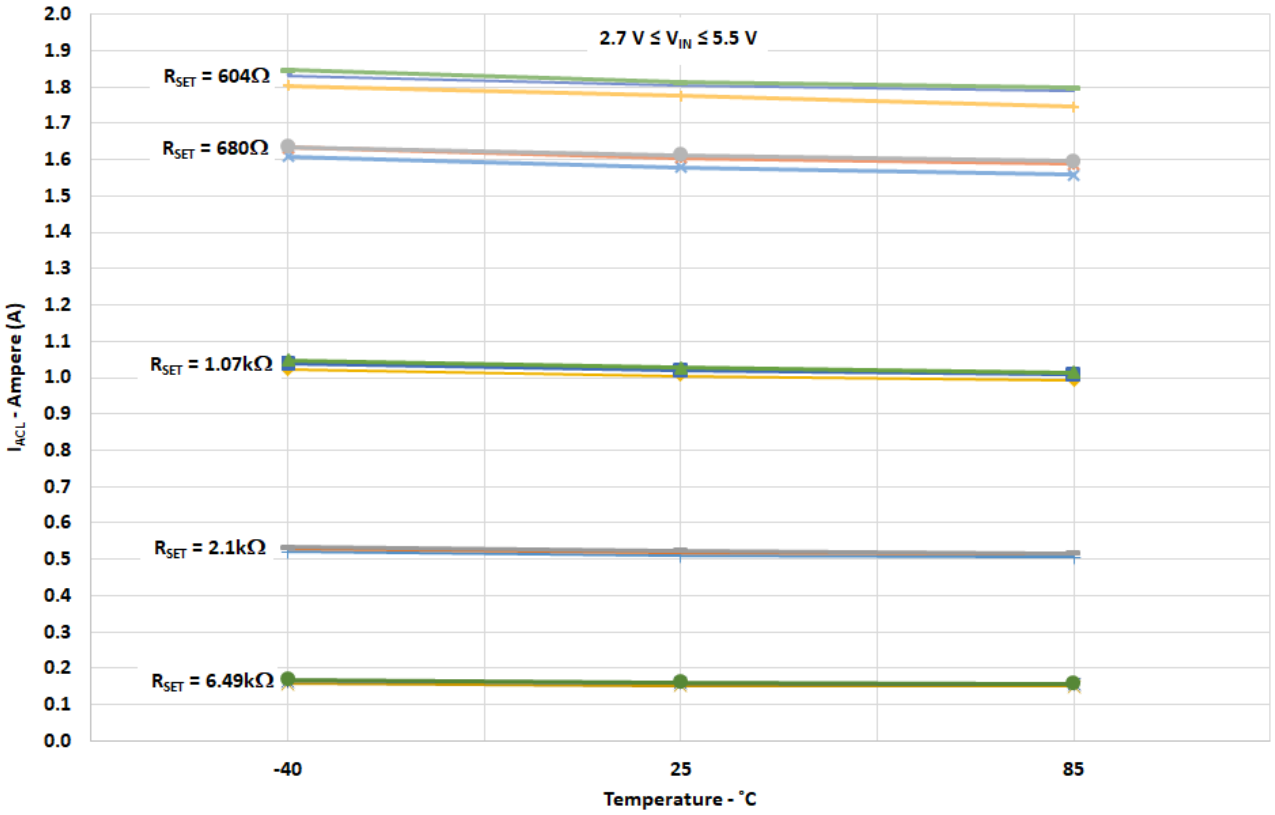
RDS_{ON} vs. Temperature and V_{IN}



I_{ACL} vs. R_{SET} and V_{IN}



I_{ACL} vs. Temperature, V_{IN}, and R_{SET}



Typical Turn ON Operation Waveforms

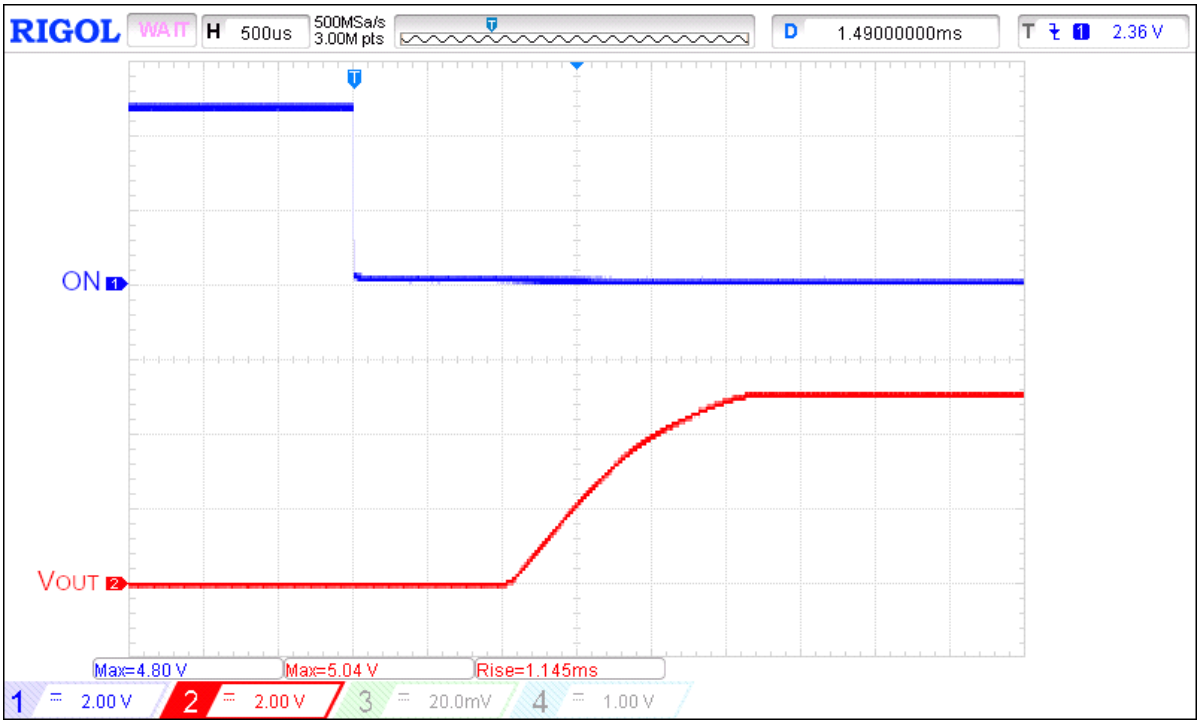


Figure 1. Typical Turn ON operation waveform for V_{IN} = 5 V, R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF

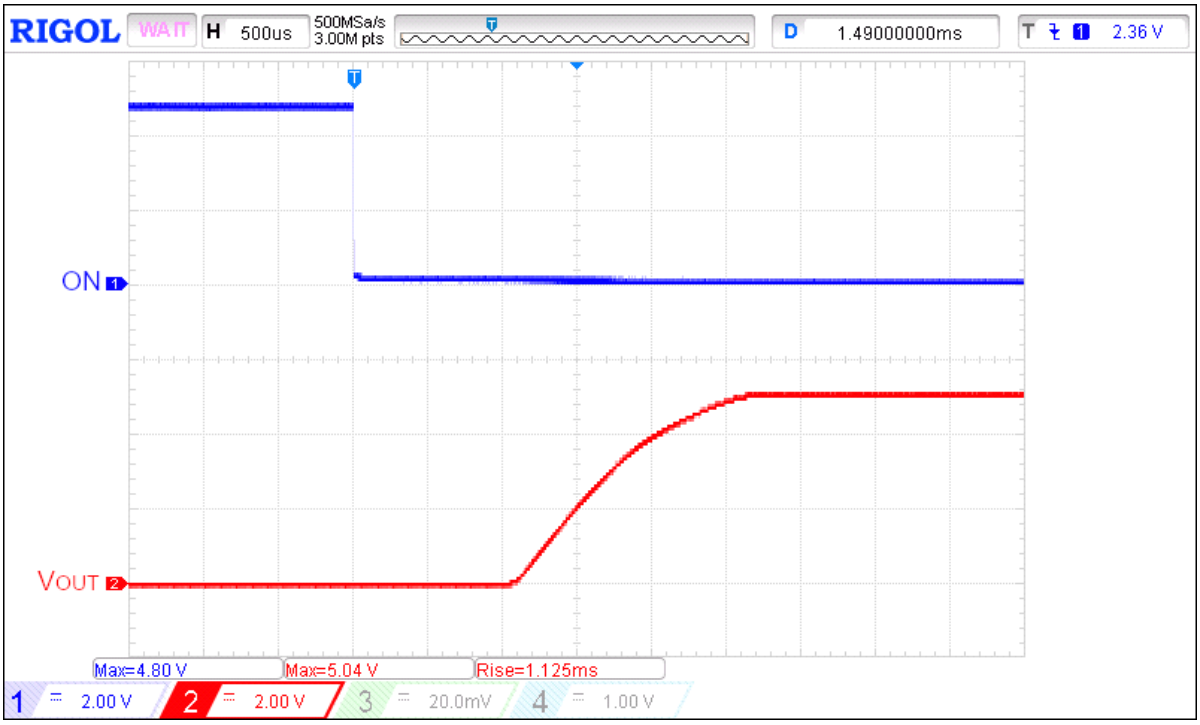


Figure 2. Typical Turn ON operation waveform for V_{IN} = 5 V, R_{LOAD} = 100 Ω, C_{LOAD} = 4.4 µF

Typical Turn OFF Operation Waveforms

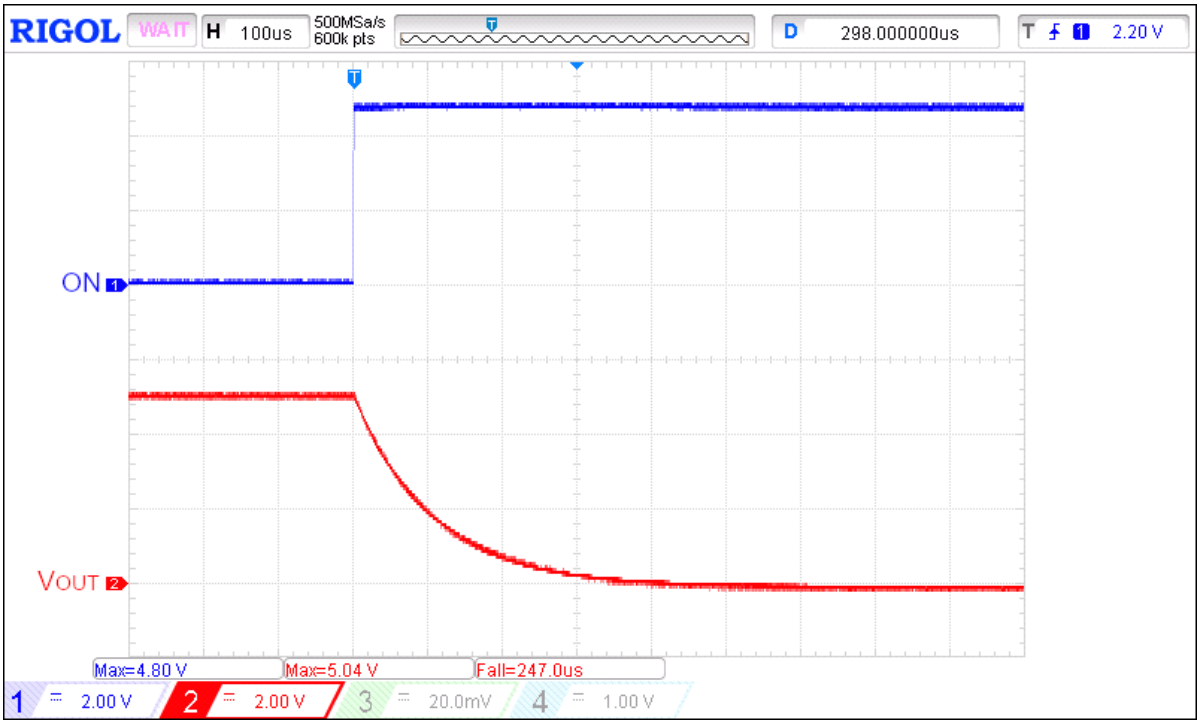


Figure 3. Typical Turn OFF operation waveform for V_{IN} = 5 V, R_{LOAD} = 100 Ω, C_{LOAD} = 1 µF

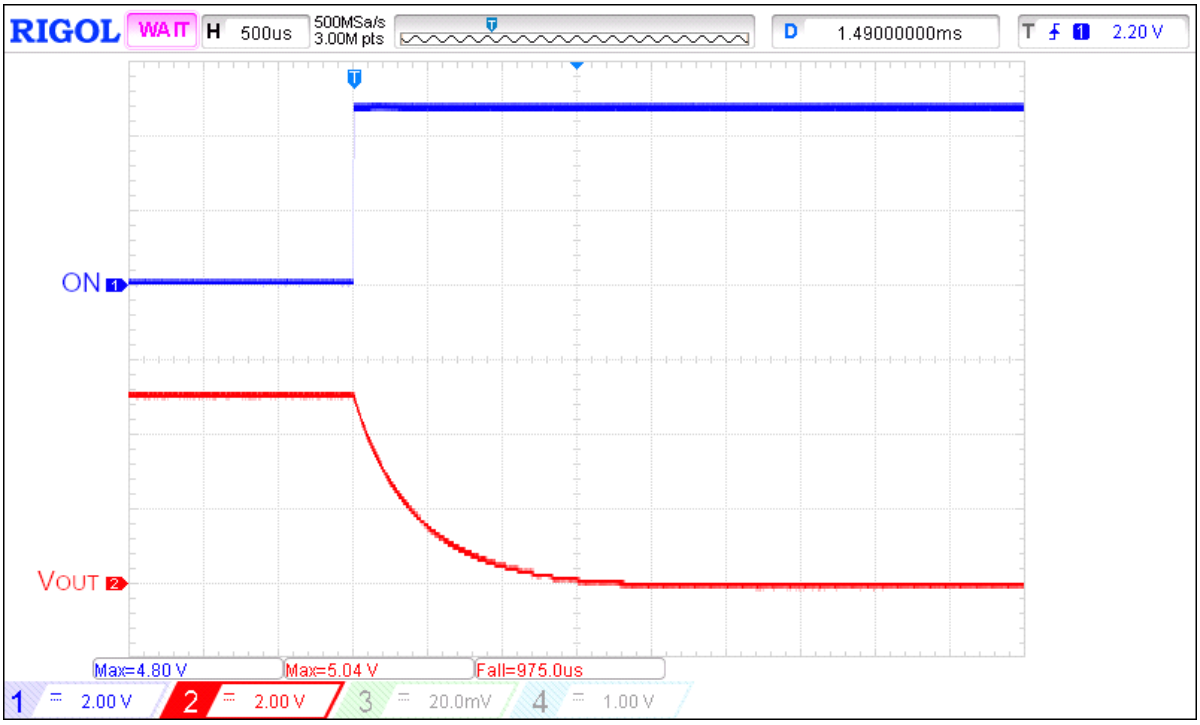


Figure 4. Typical Turn OFF operation waveform for V_{IN} = 5 V, R_{LOAD} = 100 Ω, C_{LOAD} = 4.4 µF

Typical $\overline{\text{FLT}}$ Operation Waveforms

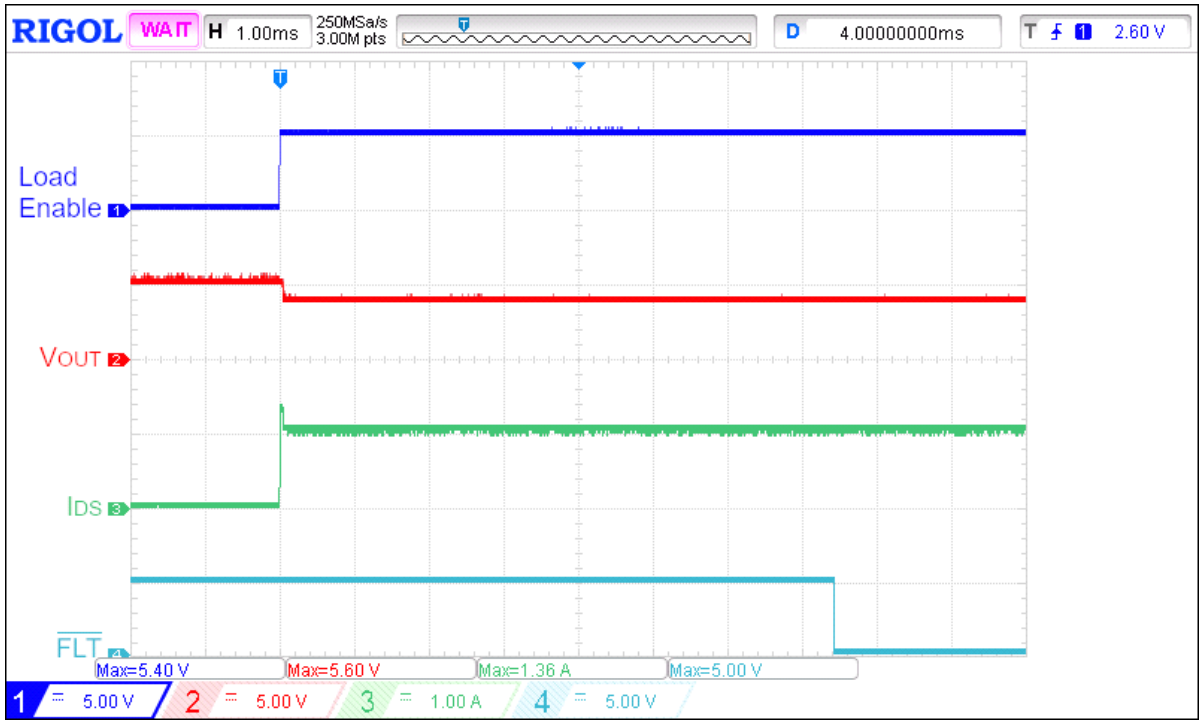


Figure 5. $\overline{\text{FLT}}$ assertion operation waveform for V_{IN} = 5 V, R_{LOAD} = 4 Ω, R_{SET} = 1.07 kΩ, C_{LOAD} = 1 µF

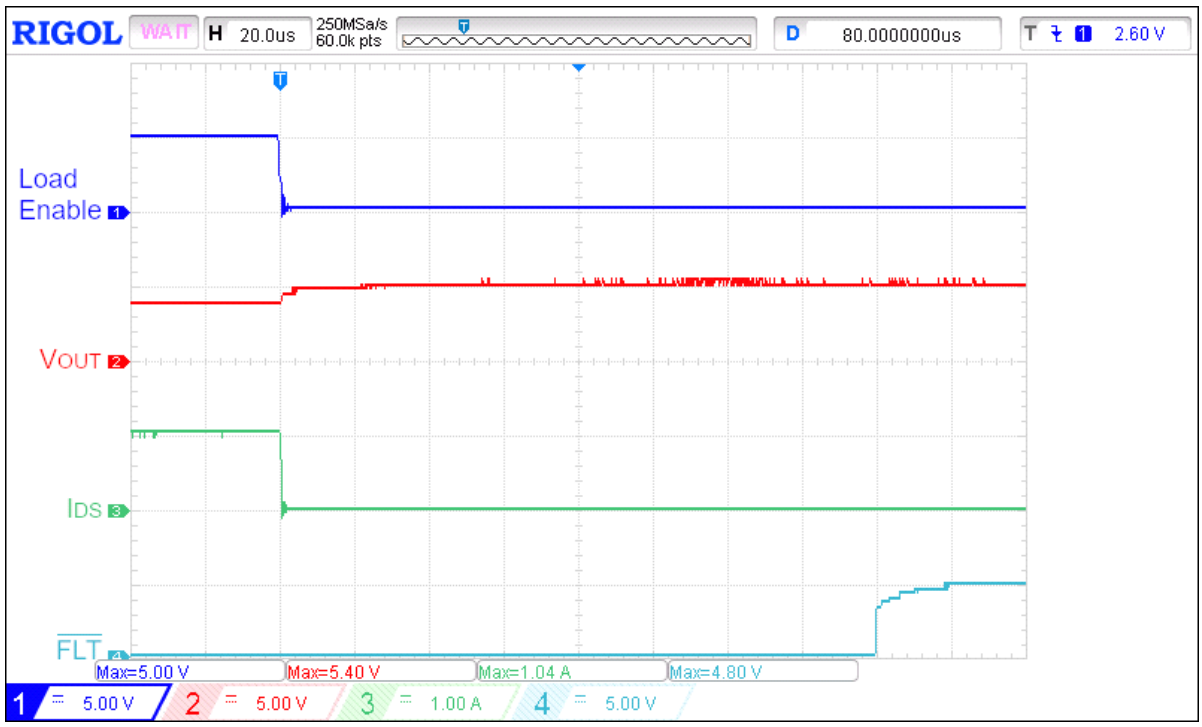


Figure 6. $\overline{\text{FLT}}$ de-assertion operation waveform for V_{IN} = 5 V, R_{LOAD} = 4 Ω, R_{SET} = 1.07 kΩ, C_{LOAD} = 1 µF

Typical ACL Operation Waveforms

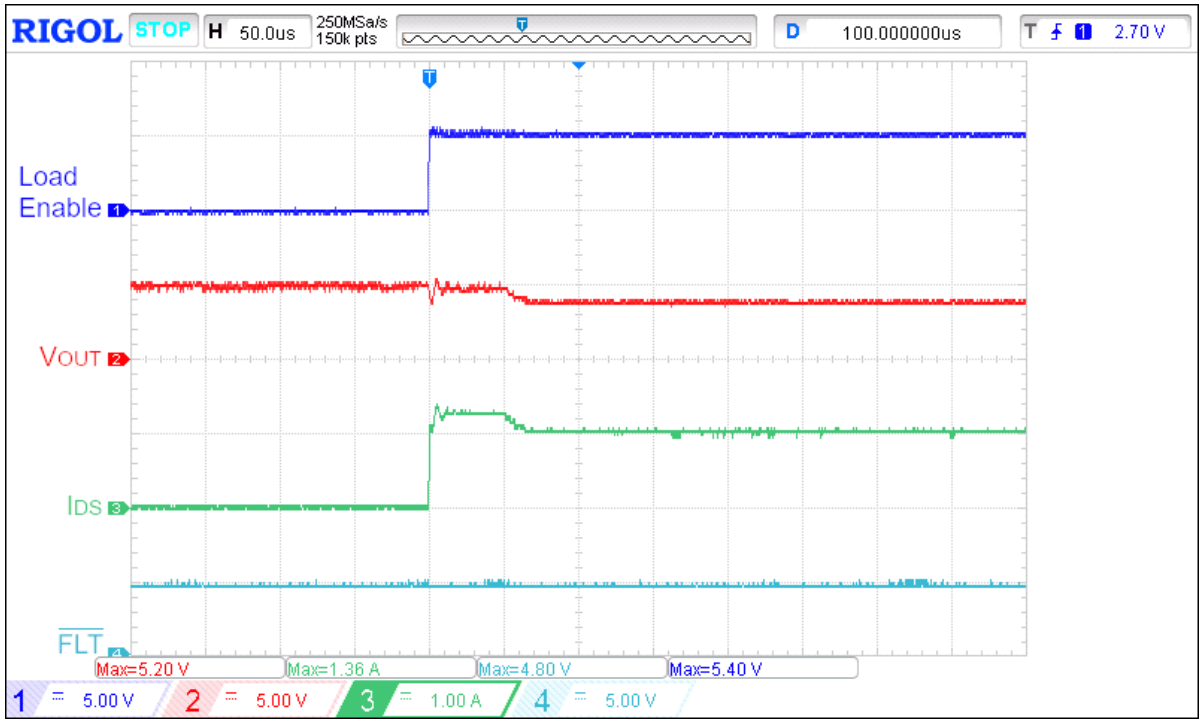


Figure 7. Typical ACL operation waveform for V_{IN} = 5 V, R_{LOAD} = 3.9 Ω, R_{SET} = 1.07 kΩ, C_{LOAD} = 1 µF

Typical OVP Operation Waveforms

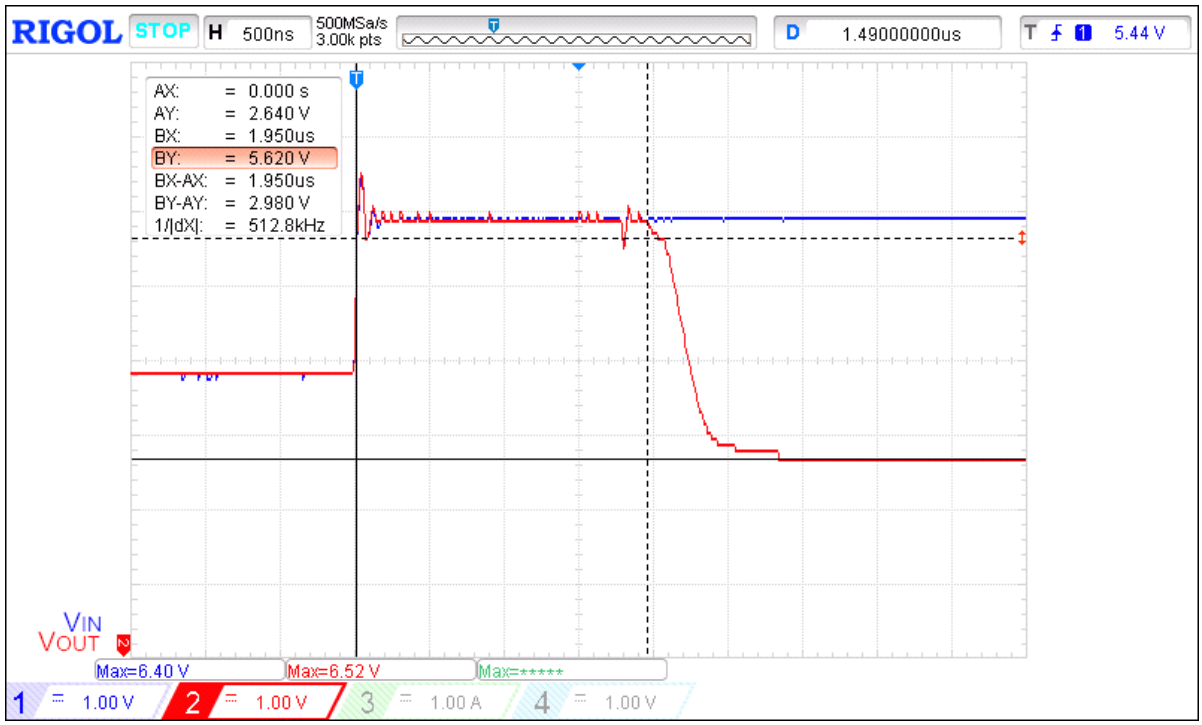


Figure 8. OVP Response operation waveform for V_{IN} step from 4 V to 6 V, no R_{LOAD}, no C_{LOAD}

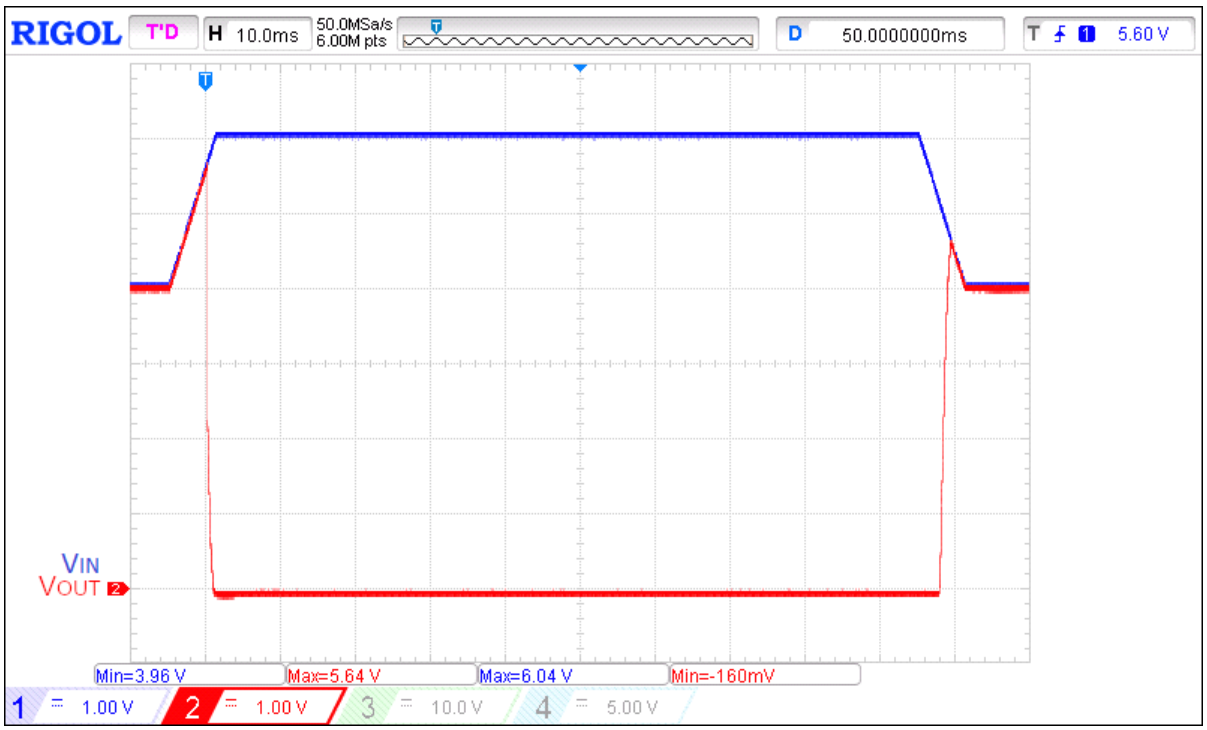


Figure 9. Typical Overvoltage Protection operation waveform for V_{IN} step from 4 V to 6 V to 4 V, no R_{LOAD}, no C_{LOAD}

SLG59H1342C Current Limiting Operation

After power up the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold. During active current-limit operation, V_{OUT} is also reduced by I_{ACL} x $RDS_{ON(ACL)}$.

When a current-limit event is detected, the $\overline{FLT}$ signal becomes asserted in approximately $\overline{TFLT}_{LOW}$ and the SLG59H1342C operates in constant current mode with the output current set by R_{SET} (see R_{SET}-Current Limit Table). The SLG59H1342C continues to operate in constant current mode indefinitely until the current-limit event has elapsed.

SLG59H1342C $\overline{FLT}$ Operation

As previously stated in the Pin Description section, the open-drain $\overline{FLT}$ output is asserted when an active-current limit (ACL) condition is detected. This output becomes asserted in $\overline{TFLT}_{LOW}$ upon the detection of a fault condition. If the $\overline{ON}$ pin is toggled LOW-to-HIGH while the $\overline{FLT}$ output is low, the $\overline{FLT}$ output is deasserted without delay.

Setting the SLG59H1342C Output Current Limit with R_{SET}

The current-limit operation of the SLG59H1342C begins by choosing the appropriate ±1%-tolerance R_{SET} value for the application. The recommended range for R_{SET} is:

$$6.49\ k\Omega \geq R_{SET} \geq 604\ \Omega$$

which corresponds to an output constant current limit in the following range:

$$0.16\ A \leq I_{ACL} \leq 1.81\ A$$

Table 1: Setting Current Limit Threshold vs. R_{SET}, C_{IN} = 30 µF, C_{RSET} = 10 pF

R_{SET} (Ω)	Min. Current Limit (A)	Typ. Current Limit (A)	Max. Current Limit (A)	Recommended Max. C_{LOAD} (µF)
604	1.63	1.81	1.99	220
680	1.45	1.61	1.77	220
866	1.13	1.26	1.39	220
1070	0.92	1.02	1.12	220
1200	0.82	0.91	1.00	220
1330	0.74	0.82	0.90	220
1500	0.66	0.73	0.80	220
1740	0.57	0.63	0.69	220
2100	0.47	0.52	0.57	220
2320	0.42	0.47	0.52	10
2550	0.38	0.43	0.47	4.4
2940	0.33	0.37	0.41	2.2
3400	0.29	0.32	0.35	2.2
4020	0.24	0.27	0.30	1
4990	0.18	0.21	0.24	1
6490	0.13	0.16	0.19	0.47

Power Dissipation Considerations

The junction temperature of the SLG59H1342C depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON} generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59H1342C is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59H1342C's power dissipation can also be calculated by taking into account the voltage drop across the switch (V_{IN} - V_{OUT}) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} – (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

V_{IN} = Switch input Voltage, in Volts (V)

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

I_{DS} = Switch output current, in Amps (A)

V_{OUT} = Switch output voltage, or $R_{LOAD} \times I_{DS}$

In current-limit mode, the SLG59H1342C's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN}-V_{OUT}) and the magnitude of the output current in current-limit mode (I_{ACL}):

$$PD = (V_{IN}-V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} – (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$

Layout Guidelines

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 10. illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59H1342Cs VIN and VOUT pins;
3. The GND pin should be connected to system analog or power ground plane.

SLG59H1342C Evaluation Board:

4. A High Voltage GreenFET Evaluation Board for SLG59H1342C is designed according to the statements above and is illustrated on Figure 10. Please note that evaluation board has Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

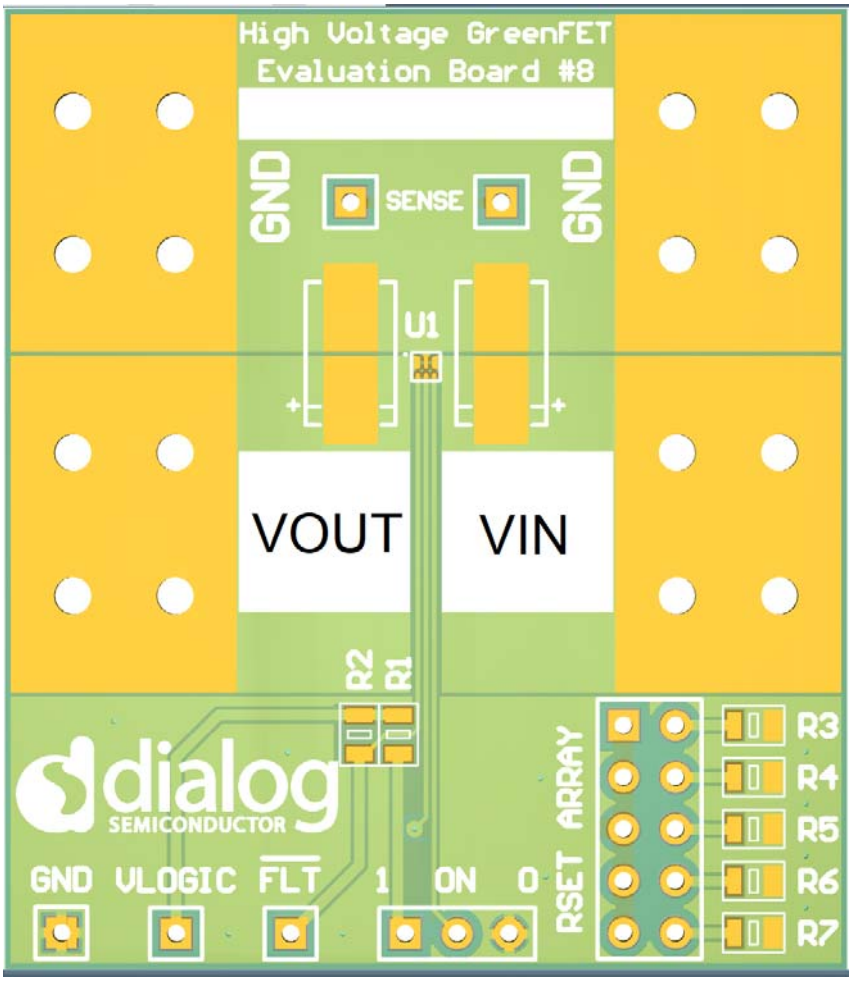


Figure 10. SLG59H1342C Evaluation Board

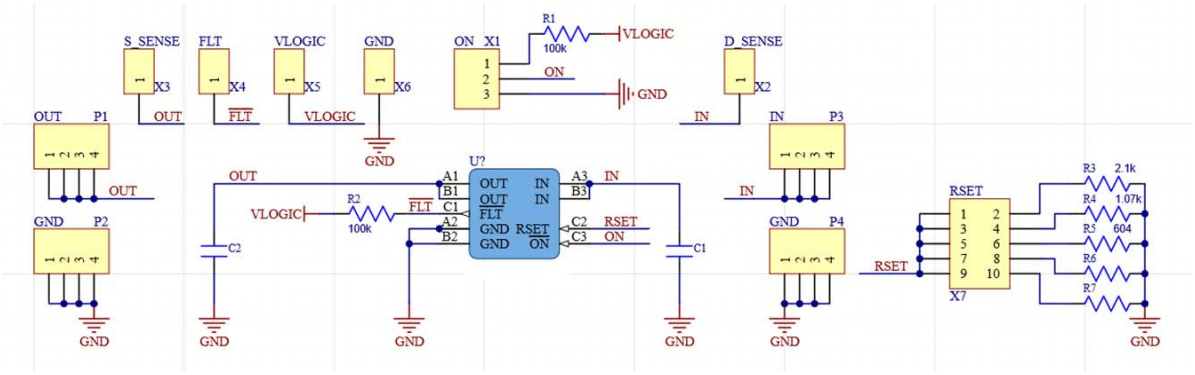
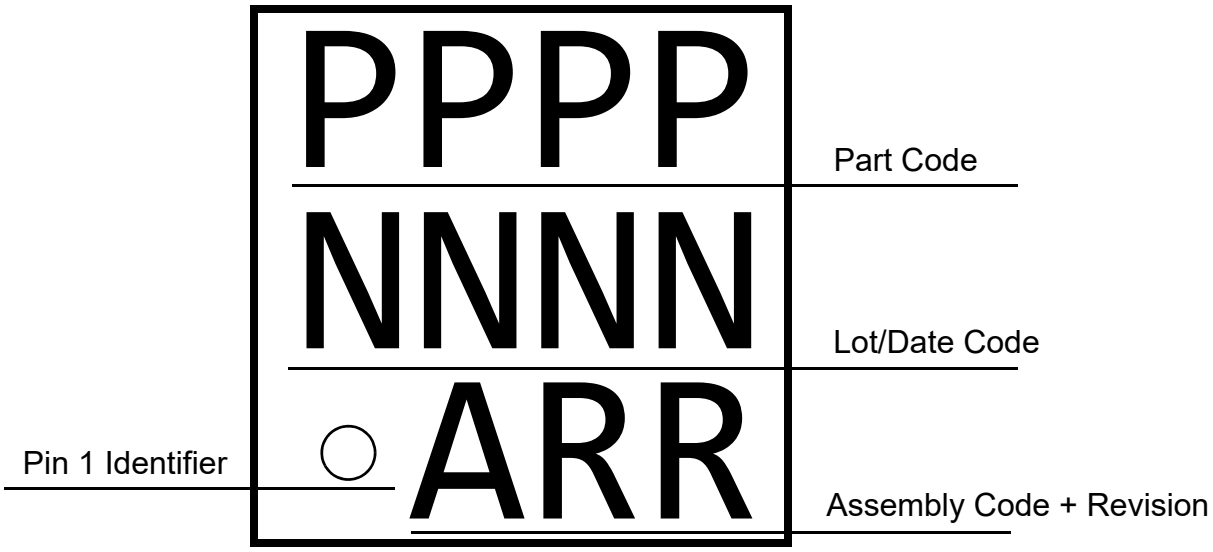


Figure 11. SLG59H1342C Evaluation Board Connection Circuit

Basic EVB Configuration

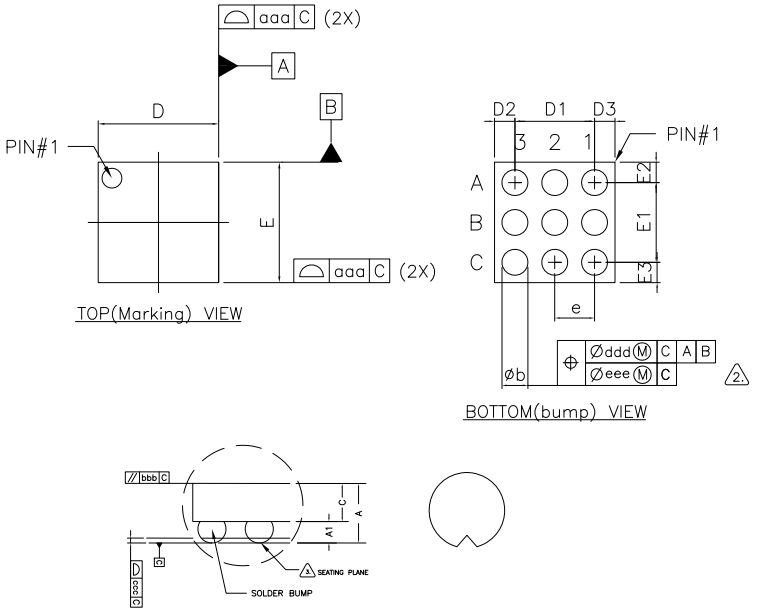
1. Connect oscilloscope probes to VIN, VOUT, ON, etc.;
2. Turn on Power Supply and set desired V_{IN} from 2.7 V…5.5 V range;
3. Toggle ON signal High or Low to observe SLG59H1342C operation;

Package Top Marking System Definition



Package Drawing and Dimensions

9 Pin WLCSP Green Package 1.21x 1.21 mm



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.5470	0.5860	0.6250	0.0215	0.0231	0.0246
A1	0.1870	0.2080	0.2290	0.0074	0.0082	0.0090
c	0.3530	0.3780	0.4030	0.0139	0.0149	0.0159
D	1.1850	1.2100	1.2350	0.0467	0.0476	0.0486
E	1.1850	1.2100	1.2350	0.0467	0.0476	0.0486
b	0.2340	0.2600	0.2860	0.0092	0.0102	0.0113
D1	---	0.8000	---	---	0.0315	---
D2	---	0.2050	---	---	0.0081	---
D3	---	0.2050	---	---	0.0081	---
E1	---	0.8000	---	---	0.0315	---
E2	---	0.2050	---	---	0.0081	---
E3	---	0.2050	---	---	0.0081	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.025	---	---	0.001	---
bbb	---	0.060	---	---	0.002	---
ccc	---	0.030	---	---	0.001	---
ddd	---	0.050	---	---	0.002	---
eee	---	0.050	---	---	0.002	---

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

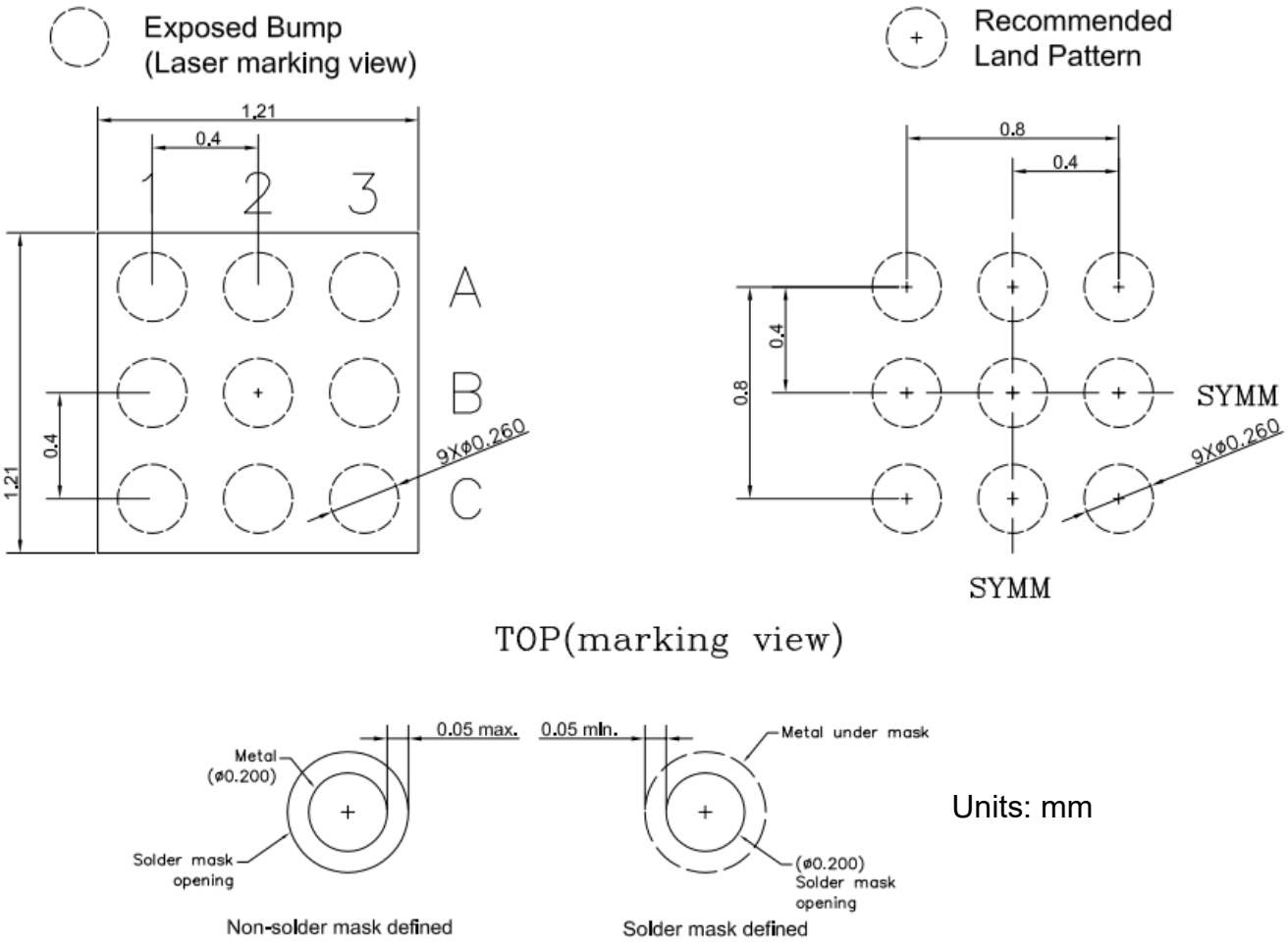
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

4. THE SOLDER BALL SIZE PRIOR REFLOW IS 250 UM.

STATUS:	RELEASED
TERMINAL FINISH:	SAC405
TITLE:	CABRERA WLCSP 9L 1.21x1.21x0.586mm 0.4P PACKAGE OUTLINE
REV:	A
REVISION NOTE:	NEW DRAWING

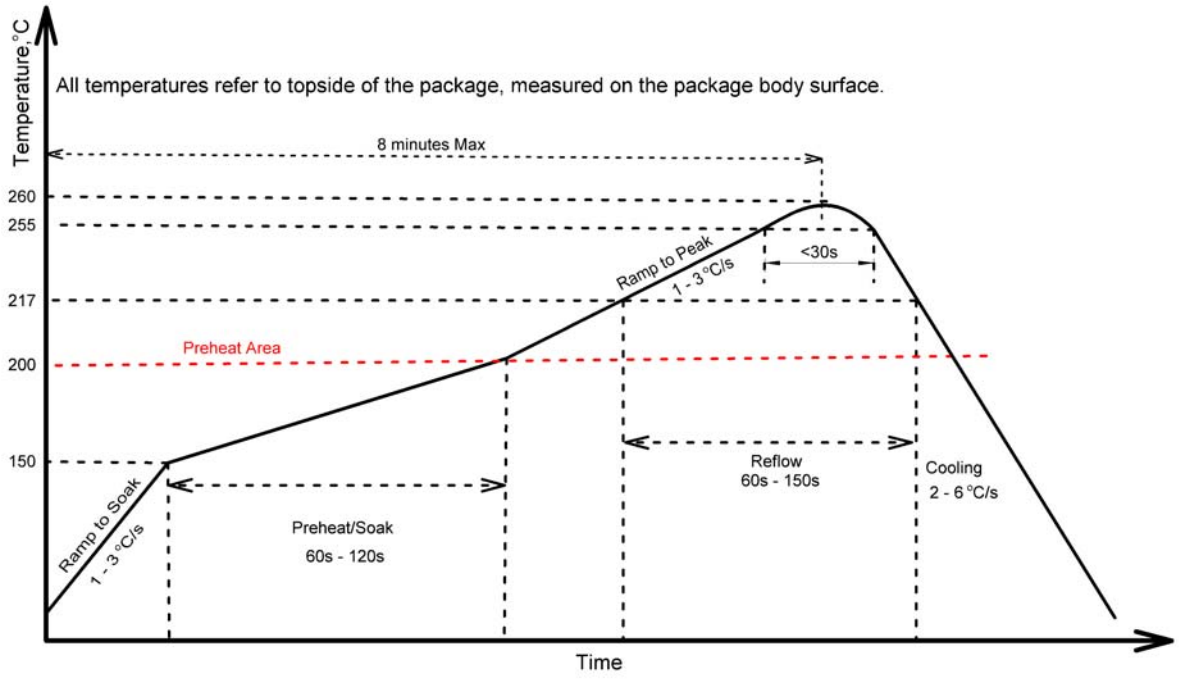
Recommended Landing Pattern



Units: mm

Recommended Reflow Soldering Profile

For successful reflow of the SLG59H1342C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

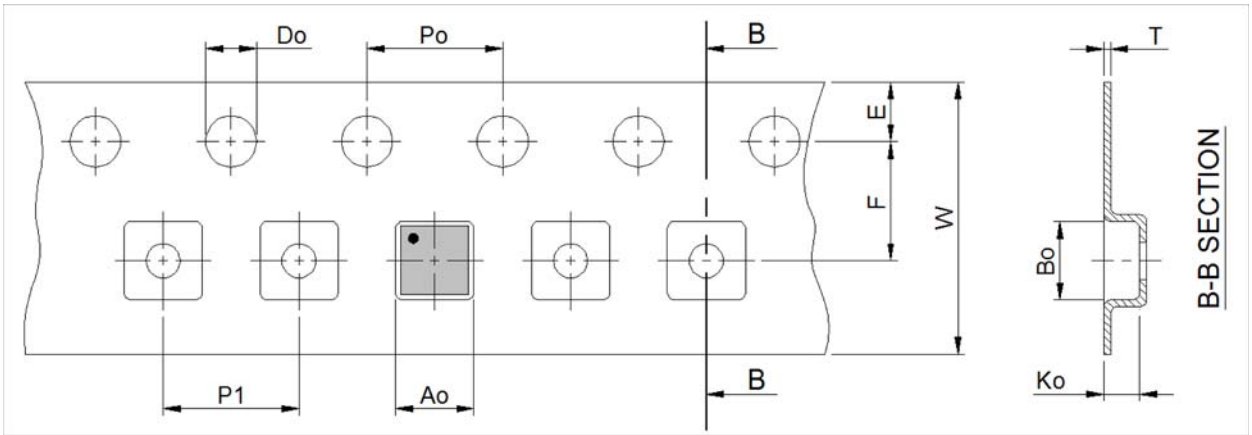
Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.553 mm^3 (nominal).

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 9L 1.21 x 1.21 mm 0.4P Green	9	1.21 x 1.21 x 0.586	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 9L 1.21x 1.21 mm 0.4P Green	1.38	1.38	0.7	4	4	1.5	1.75	3.5	8	0.2



Note: 1.Orientation in carrier: Pin1 is at upper left corner (Quadrant 1). **Refer to EIA-481 specification**

Revision History

Date	Version	Change
27-Jan-2023	1.02	Updated Block Diagram and Pin description with C_{RSET} recommendation Updated $I_{REVERSE}$ condition for VIN = 0 V Fixed typos in Layout Guidelines
29-Aug-2022	1.01	Fixed typo in Scope shots
15-Jul-2022	1.0	Production Release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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