SLG59M1440V

An Ultra-small 40 mΩ, 1 A, Load Switch with Discharge

General Description

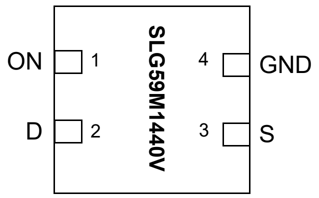
The SLG59M1440V is designed for load switching applications. The part comes with one 40 mΩ, 1 A rated MOSFET controlled by a single ON control pin. The MOSFET's ramp rate is adjustable depending on the input current level of the ON pin.

The product is packaged in an ultra-small 1.0 x 1.0 mm package.

Features

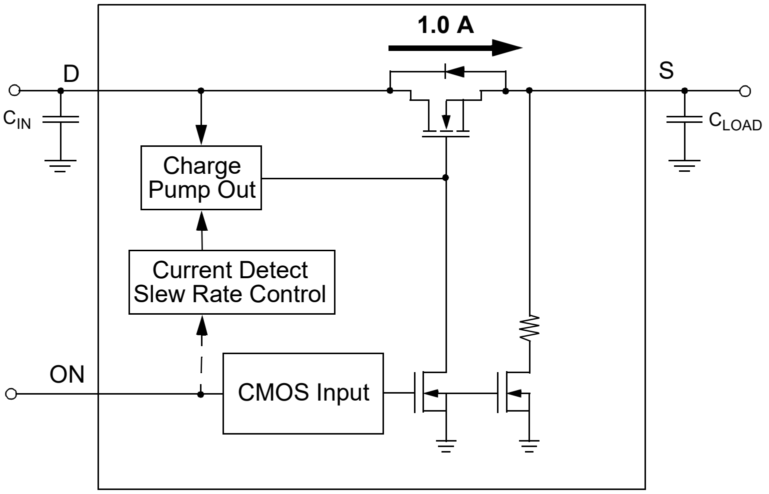
- One 40 mΩ, 1 A MOSFET
- One integrated VGS Charge Pump
- User selectable ramp rate with external resistor
- Integrated Discharge Resistor
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 4L, 1.0 x 1.0 x 0.55 mm

Pin Configuration



4-pin STDFN
(Top View)

Block Diagram



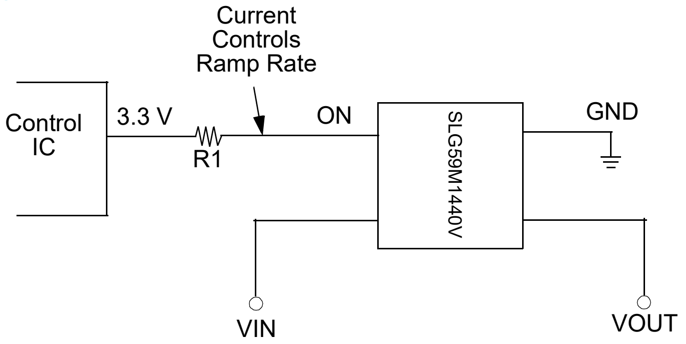
Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin closes the load switch. ON is an asserted-HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH_INI} > 1.2 V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. A resistor connected in series to ON signal sets the V_S Slew Rate. Please read more information on Adjustable Slew Rate description.
2	D	MOSFET	Drain/Input terminal of Power MOSFET. Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at D should be rated at 10 V or higher.
3	S	MOSFET	Source/Output terminal of Power MOSFET. Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at S should be rated at 10 V or higher.
4	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1440V	STDFN 4L	Industrial, -40 °C to 85 °C
SLG59M1440VTR	STDFN 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Application Diagram



Adjustable Ramp Rate vs. ON Pin Current (5.5 V, 25 °C)

ON Pin Current	$V_{S(SR)}$ (typ)
20 µA	0.56 V/ms
50 µA	1.34 V/ms
100 µA	2.53 V/ms
150 µA	3.71 V/ms
200 µA	4.68 V/ms
250 µA	5.63 V/ms

Adjustable Slew Rate (ON Pin 1)

SLG59M1440V has a built in configurable slew control feature. The configurable slew control uses current detection method on Pin 1. When ON voltage rises above ON_V_{IH_INI} (1.2 V typical), the slew control circuit will measure the current flowing into Pin 1. Based on the current flowing into pin 1, different slew rates will be selected by the internal control circuit. See ON Pin Curent vs. $V_{S(SR)}$ table. The slew rate is configurable by selecting a different R1 resistor value as shown on application diagram. Calculating the R1 value depends on both the desired slew rate, and the GPIO_V_{OH} level of the device driving the ON Pin 1.

ON Pin Current = (GPIO_V_{OH} – ON_V_{REF} (1.05 V typical)) / R1

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_D	Load Switch Input Voltage		--	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
MSL	Moisture Sensitivity Level		1			
W_{DIS}	Package Power Dissipation		--	--	0.5	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	1.5	A
Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.						

Electrical Characteristics

T_A = -40 °C to 85 °C unless otherwise noted. Typical values are at T_A = 25 °C.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_D	Load Switch Input Voltage	-40 °C to 85 °C	2.5	--	5.5	V
I_D	Load Switch Current (PIN 2)	when OFF	--	0.1	1	µA
		when ON, No load	--	18	30	µA
RDS_{ON}	ON Resistance	T_A = 25 °C; I_{DS} = 100 mA	--	40	50	mΩ
		T_A = 70 °C; I_{DS} = 100 mA	--	50	55	mΩ
		T_A = 85 °C; I_{DS} = 100 mA	--	55	65	mΩ
MOSFET IDS	Current from D to S	Continuous	--	--	1.0	A
T_{ON_Delay}	ON Delay Time	50% ON to V_S Ramp Start; ON Pin Current (PIN1) = 20 µA; V_D = 5 V; C_{LOAD} = 10 µF; R_{LOAD} = 20 Ω	--	2.4	4.0	ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Set by External Resistor[1]			ms
		Example: ON Pin Current (PIN1) = 20 µA; V_D = 5 V; C_{LOAD} = 10 µF; R_{LOAD} = 20 Ω	--	11.7	--	ms
$V_{S(SR)}$	V_S Slew Rate	10% V_S to 90% V_S	Set by External Resistor[1]			V/ms
		Example: ON Pin Current (PIN1) = 20 µA; V_D = 5 V; C_{LOAD} = 10 µF; R_{LOAD} = 20 Ω	--	0.56	--	V/ms
$R_{DISCHRG}$	Discharge Resistance	V_D = 2.5 V to 5.5 V; V_S = 0.4 V Input bias	100	150	300	Ω
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from S to GND	--	--	100	µF
ON_V_{REF}	ON Pin Reference Voltage[2]		0.99	1.05	1.10	V
$ON\_V_{IH\_INI}$	Initial Turn On Voltage	Internal Charge Pump ON	1.2	--	V_D	V
ON_V_{IL}	Low Input Voltage on ON pin	Internal Charge Pump OFF	-0.3	0	0.3	V
ON_R	Input Impedance on ON pin		100	--	--	MΩ
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	120	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C

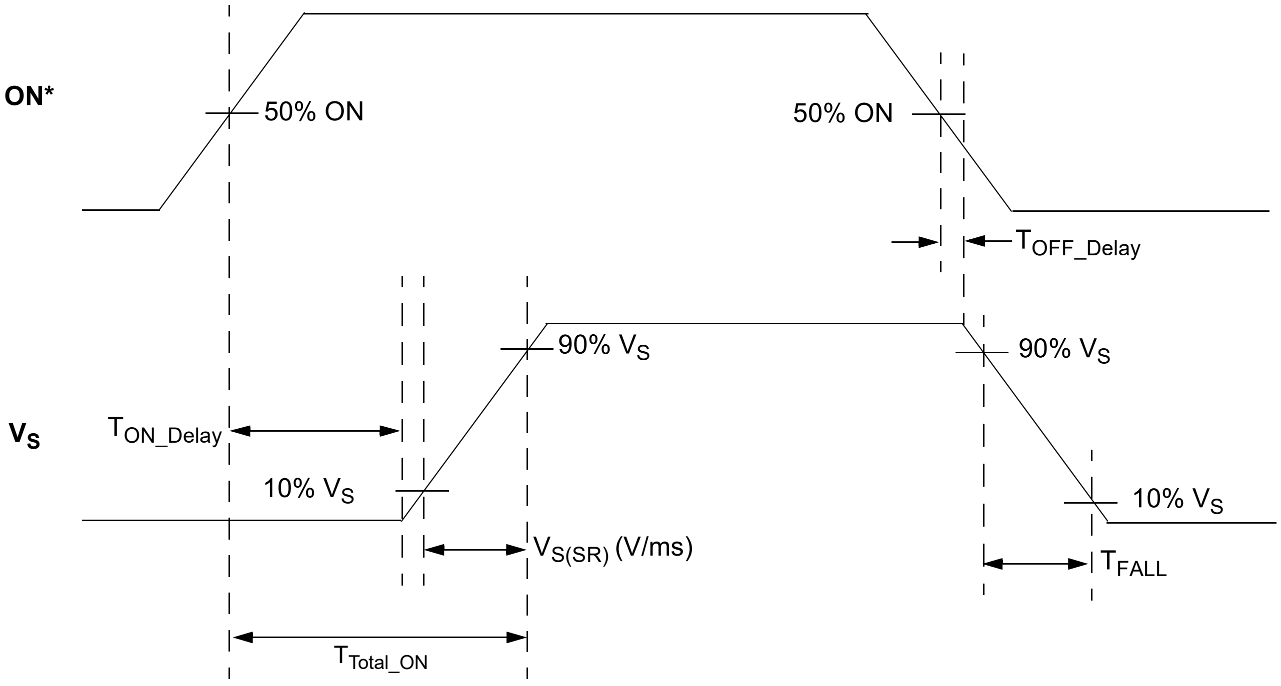
Electrical Characteristics **(continued)**

T_A = -40 °C to 85 °C unless otherwise noted. Typical values are at T_A = 25 °C.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall Start; V_D = 5 V; R_{LOAD} = 20 Ω, no C_{LOAD}	--	6.5	20	µs
T_{FALL}	V_S Fall Time	90% V_S to 10% V_S; V_D = 5 V; R_{LOAD} = 20 Ω; no C_{LOAD}	--	1.2	2	µs

Notes:
1. Refer to table for configuration details.
2. Voltage before ON pin resistor needs to be higher than 1.2 V to generate required I_{ON}

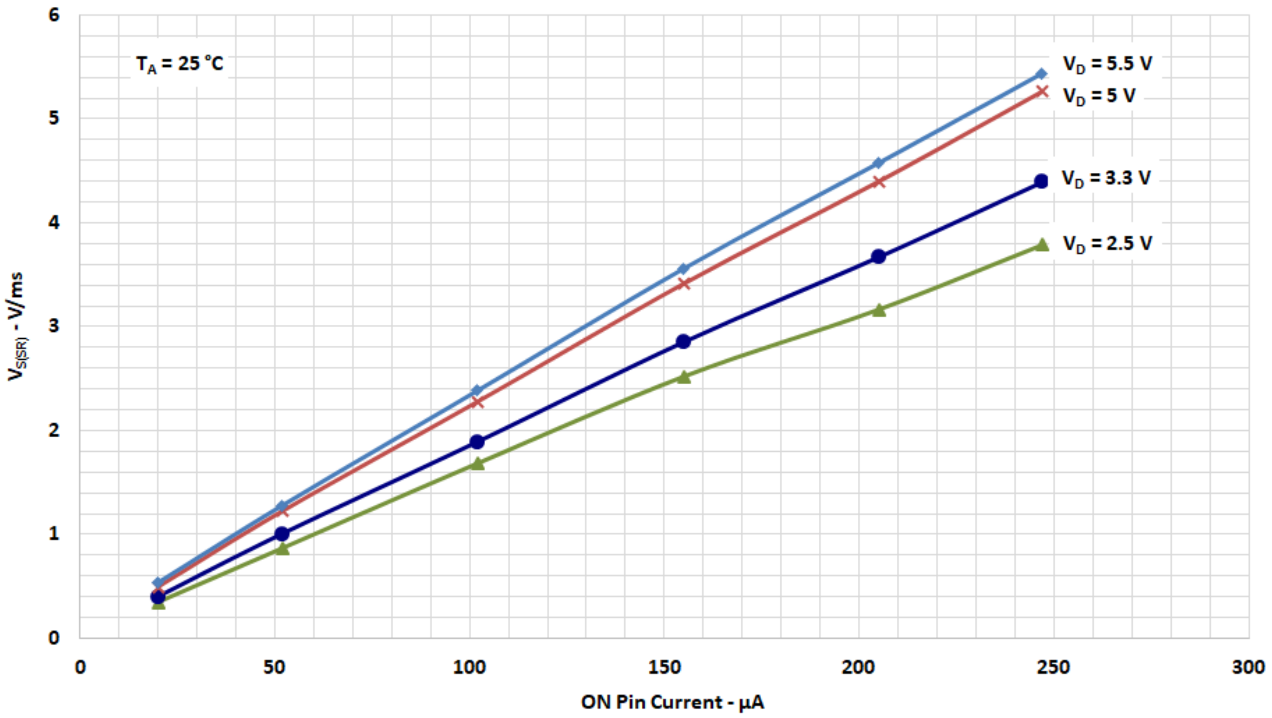
T_{ON_Delay}, $V_{S(SR)}$, and T_{Total_ON} Timing Details



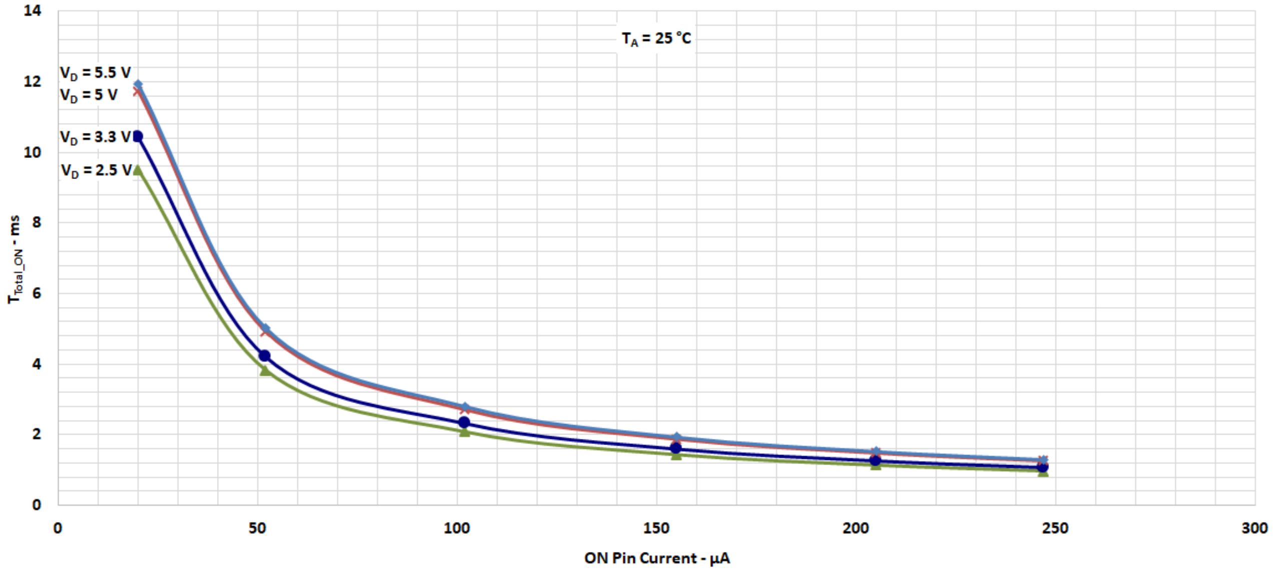
Note: * Rise and Fall times of the ON signal are 100 ns

Typical Performance Characteristics

Slew Rate vs. ON Pin Current



T_{Total_ON} vs. ON Pin Current



SLG59M1440V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_D and toggle the ON pin LOW-to-HIGH after V_D is at least 90% of its final value. A nominal power-down sequence is the power-up sequence in reverse order. If V_D ramp is too fast, a voltage glitch may appear on the output pin at S. To prevent glitches at the output, it is recommended to connect at least 0.1uF capacitor from the S pin to GND and to keep the V_D ramp time higher than 2 ms.

Power Dissipation Considerations

The junction temperature of the SLG59M1440V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across the power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1440V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)
and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout
T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59M1440V's power dissipation can also be calculated by taking into account the voltage drop across the switch (V_D - V_S) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_D - V_S) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_D - (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)
V_D = Switch input Voltage, in Volts (V)
R_{LOAD} = Output Load Resistance, in Ohms (Ω)
I_{DS} = Switch output current, in Amps (A)
V_S = Switch output voltage, or $R_{LOAD} \times I_{DS}$

Layout Guidelines:

1. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum width of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2.To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1440V's D and S pins;

4\. The GND pin should be connected to system analog or power ground plane.

4\. 2 oz. copper is recommended for high current operation.

SLG59M1440V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1440V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1440V here

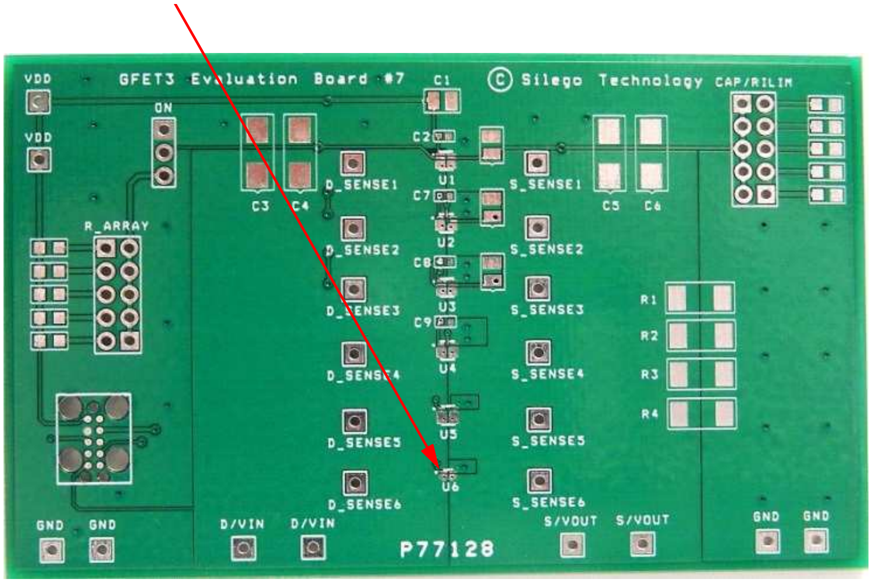


Figure 1. SLG59M1440V Evaluation Board.

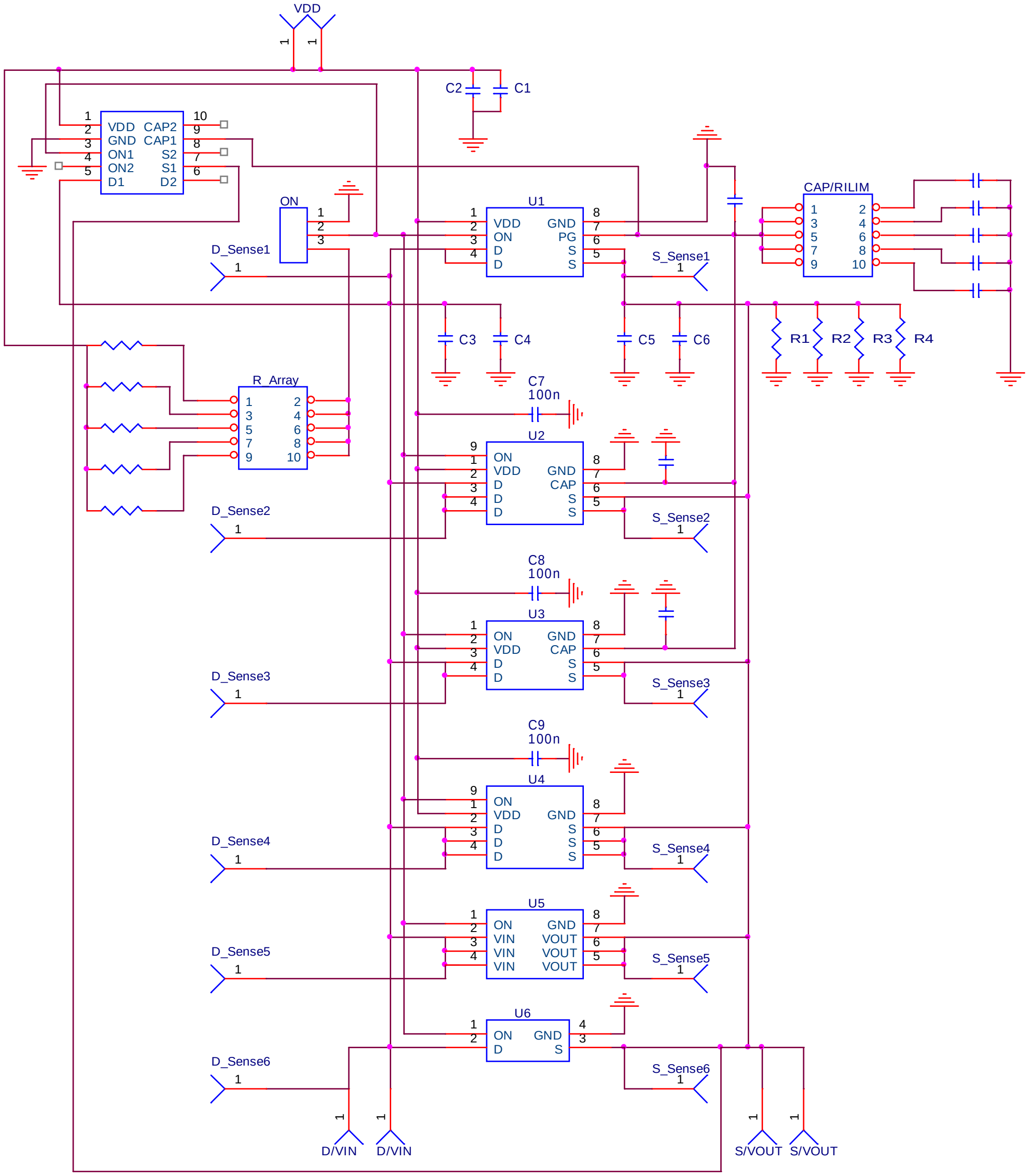


Figure 2. SLG59M1440V Evaluation Board Connection Circuit.

Basic Test Setup and Connections

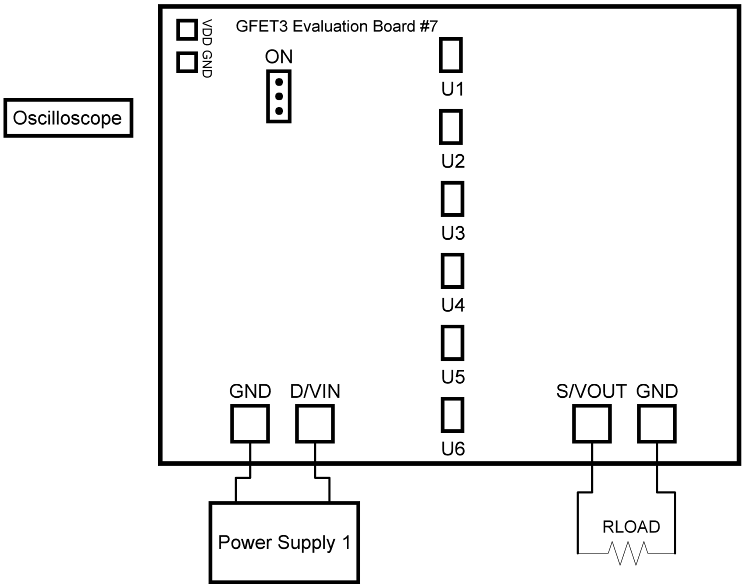


Figure 3. Typical connections for GreenFET Evaluation.

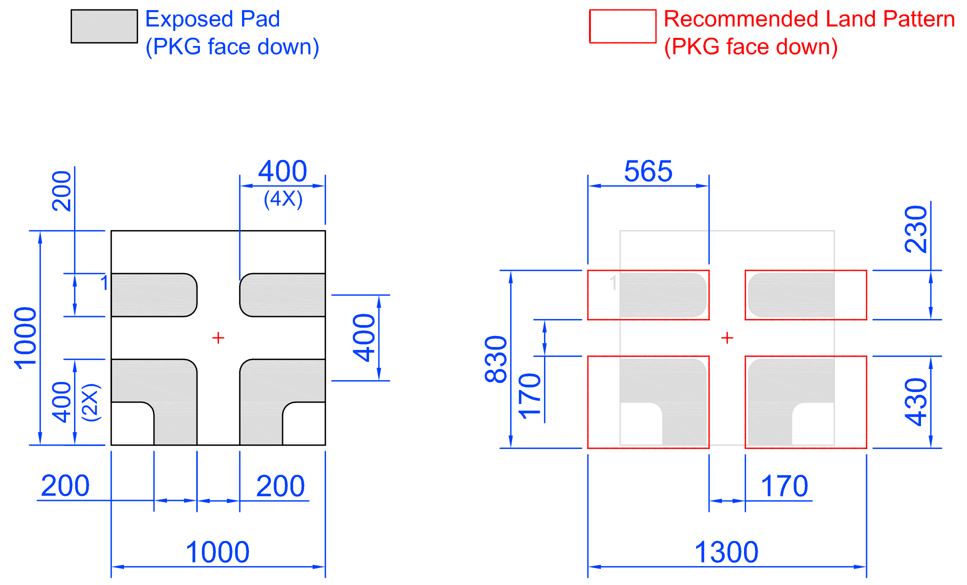
EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2. Turn on Power Supply 1 and set desired V_D from 2.5 V…5.5 V range;

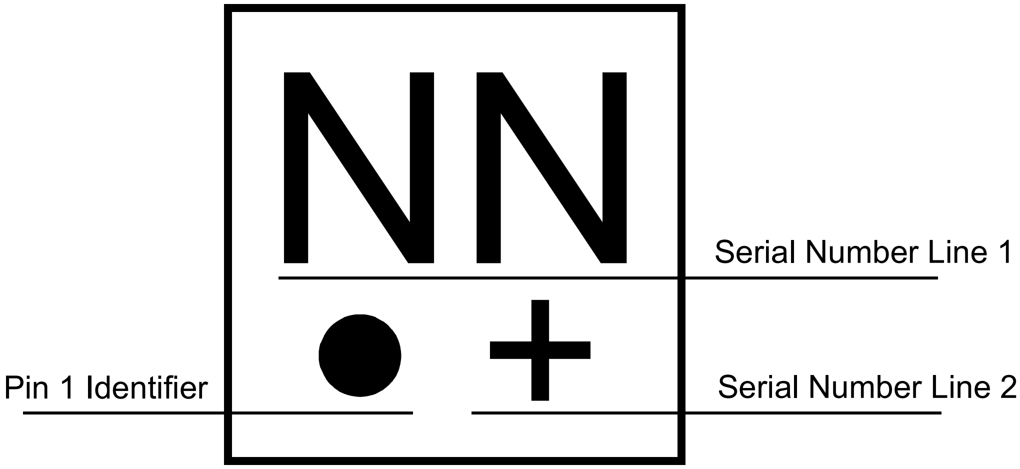
3. Toggle the ON signal High or Low to observe SLG59M1440V operation.

SLG59M1440V Layout Suggestion



Note: All dimensions shown in micrometers (µm)

Package Top Marking System Definition

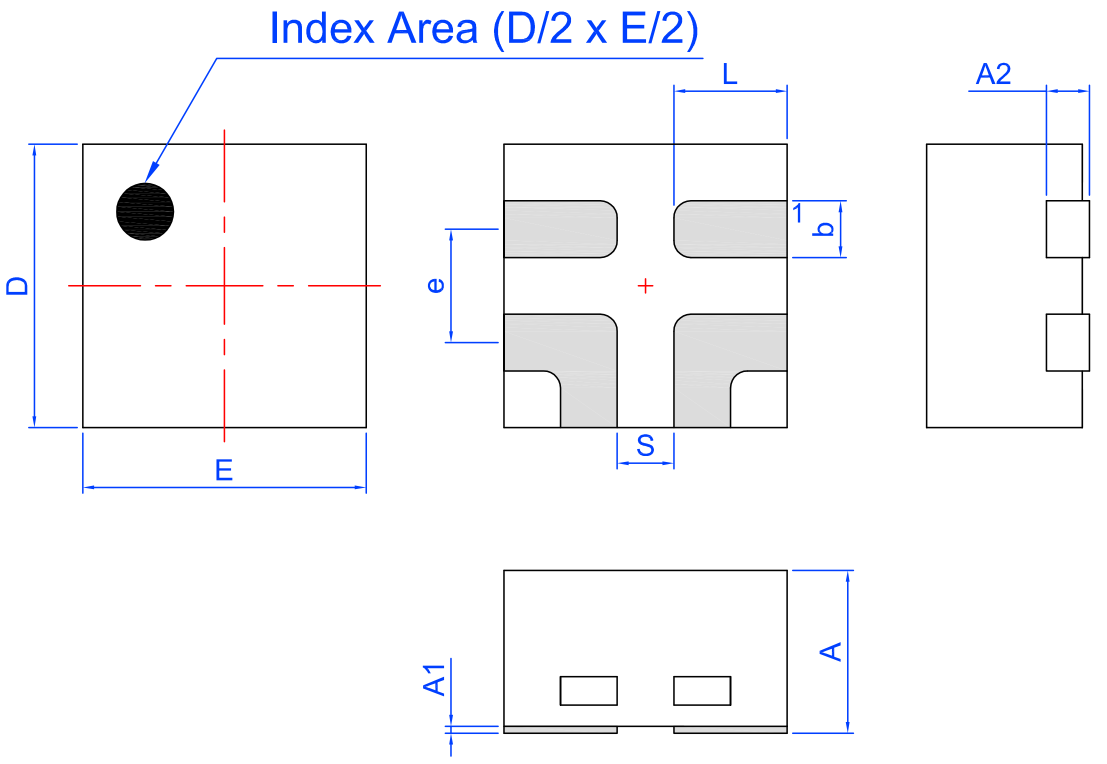


NN - Part Serial Number Field Line 1
where each “N” character can be A-Z and 0-9

\+ - Part Serial Number Field Line 2
where “+” character can be +, -, =, or blank

Package Drawing and Dimensions

4 Lead STDFN Package 1.0 x 1.0 mm



Unit: mm

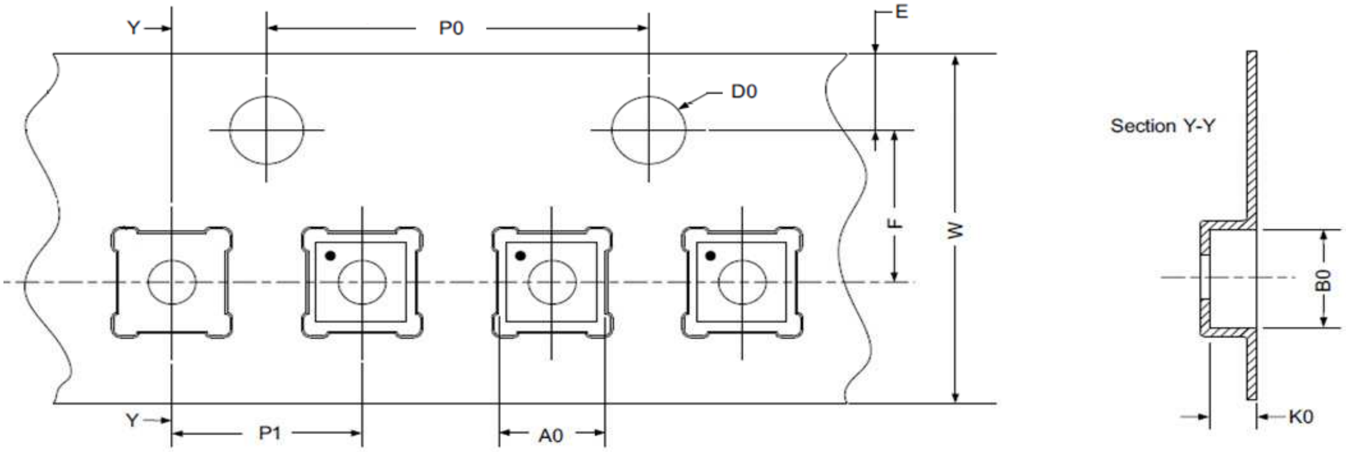
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	0.95	1.00	1.05
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.15	0.20	0.25	S	0.2 REF		
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 4L Green	4	1.0 x 1.0 x 0.55	8000	8000	178 / 60	200	400	200	400	8	2

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 4L Green	1.16	1.16	0.63	4	2	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.55 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/3/2022	1.14	Updated Company name and logo Fixed typos
9/1/2020	1.13	Updated Style and Formatting Updated Charts Added Layout Guidelines
11/20/2017	1.12	Updated Package Marking Definition Updated Layout Suggestion
12/11/2013	1.11	changed temp range to -40 to 85C

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