SLG59M1639V

Ultra-small 2-Channel 45 mΩ/2 A Load Switch with Reverse-Current Blocking

General Description

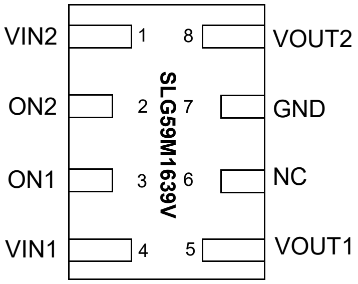
The SLG59M1639V is a dual-channel, 45 mΩ pFET load switch designed to switch 1.5 to 5.5 V power rails up to 2 A in each channel. When either channel is enabled, reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a $V_{OUT} > V_{IN} + 50$ mV condition opens the switch). In the event that the channel's V_{IN} voltage is too low, the load switch also contains an internal $V_{IN(UVLO)}$ threshold monitor to keep or to turn the switch OFF. Each load switch is independently controlled via its own low-voltage compatible CMOS input.

Designed to operate over a -40°C to 85°C range, the SLG59M1639V is available in a RoHS-compliant, ultra-small 1.6 x 1.0 mm STDFN package.

Features

- Integrated 2-Channel pFET Load Switch
- 2 A Maximum Continuous Switch Current per Channel
- Low Typical RDS_{ON}:
  - 45 mΩ at V_{IN} = 5 V
  - 60 mΩ at V_{IN} = 2.5 V
  - 80 mΩ at V_{IN} = 1.5 V
- Operating Voltage: 1.5 V to 5.5 V
- Reverse-current/voltage Protection
- Low-voltage CMOS Logic Compatible Switch Control
- Operating temperature range: -40°C to 85°C
- Pb-Free / Halogen-Free / RoHS compliant packaging

Pin Configuration

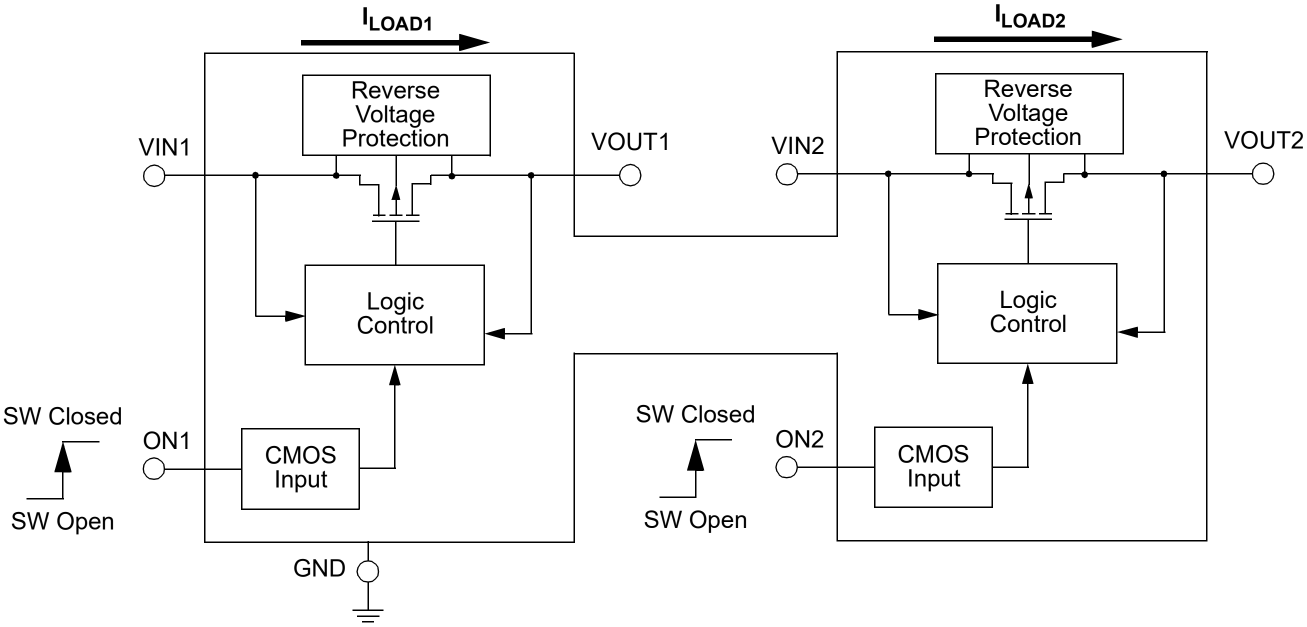


8-pin STDFN
(Top View)

Applications

- Power-Rail Switching:
  - Notebook/Laptop/Tablet PCs
  - Smartphones/Wireless Handsets
  - High-definition Digital Cameras
  - Set-top Boxes
- Point of Sales Pins
- GPS Navigation Devices

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VIN2	MOSFET	Input and source terminal of MOSFET #2. Bypass the VIN2 pin to GND with a 1 μF (or larger), low-ESR capacitor.
2	ON2	Input	ON2 turns Channel 2 MOSFET ON and is a low logic-level CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 1 V. As the ON2 input circuit does not have an internal pull-down resistor, connect ON2 pin directly to a GPIO controller – do not allow this pin to be open circuited.
3	ON1	Input	ON1 turns Channel 1 MOSFET ON and is a low-logic level CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 1 V. As the ON1 input circuit does not have an internal pull-down resistor, connect ON1 pin directly to a GPIO controller – do not allow this pin to be open circuited.
4	VIN1	MOSFET	Input and source terminal of MOSFET #1. Bypass the VIN1 pin to GND with a 1 μF (or larger), low-ESR capacitor.
5	VOUT1	MOSFET	Output and drain terminal of MOSFET #1.
6	NC	No Connect	No connection. Do not make connection to any other pin - leave Pin 6 as an open circuit.
7	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.
8	VOUT2	MOSFET	Output and drain terminal of MOSFET #2.

Ordering Information

Part Number	Type	Production Flow
SLG59M1639V	STDFN	Industrial, -40 °C to 85 °C
SLG59M1639VTR	STDFN (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN[1,2]}$	Load Switch Input Voltage		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance	1.0 x 1.6 mm 8L STDFN	--	82	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS_{CONT}	Continuous Current from VIN to VOUT	Each channel, T_J< 150°C	--	--	2	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	2.5	A
Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.						

Electrical Characteristics

1.5 V ≤ $V_{IN[1,2]}$ ≤ 5.5 V; C_{IN} = 1 μF, T_A =-40 °C to 85 °C, unless otherwise noted.
Typical values are at T_A = 25°C (unless otherwise stated)

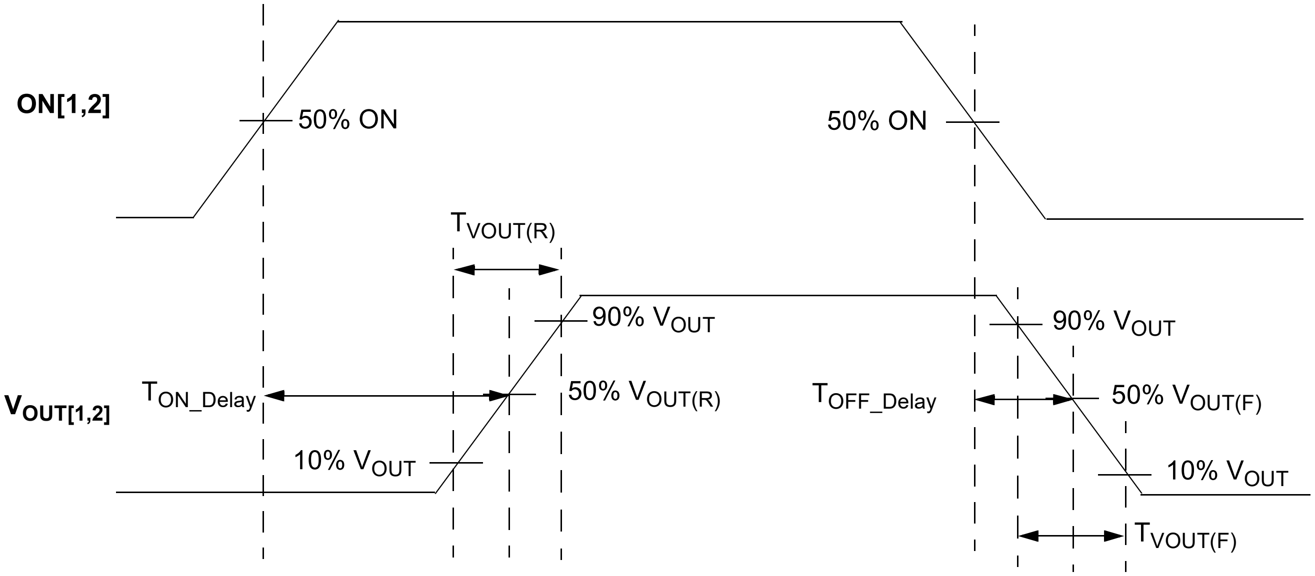
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN[1,2]}$	Load Switch Input Voltage		1.5	--	5.5	V
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	V_{IN} ↑, V_{ON} = 0 V, R_{LOAD} = 10 Ω	--	--	1.2	V
		V_{IN} ↓, V_{ON} = 0 V, R_{LOAD} = 10 Ω	0.5	--	--	V
I_{IN}	Quiescent Supply Current, Both Channels	V_{IN} = 5.25V, V_{ON} = HIGH, no Load	--	3.5	5.3	μA
		V_{IN} = 1.5 V, V_{ON} = HIGH, no Load	--	2.5	4	μA
$I_{IN(OFF)}$	OFF Mode Supply Current, Both Channels	V_{IN} = 5.25 V, V_{ON} = LOW, R_{LOAD} = 1 MΩ	--	1	1.5	μA
		V_{IN} = 1.5 V, V_{ON} = LOW, R_{LOAD} = 1 MΩ	--	0.4	1.0	μA
RDS_{ON}	ON Resistance	T_A = 25°C, V_{IN} = 5.0 V, I_{DS} = -200 mA	--	45	55	mΩ
		T_A = 25°C, V_{IN} = 2.5 V, I_{DS} = -200 mA	--	60	72	mΩ
		T_A = 25°C, V_{IN} = 1.5 V, I_{DS} = -200 mA	--	80	96	mΩ
$V_{REVERSE}$	Reverse-current Voltage Threshold		--	50	--	mV
$I_{REVERSE}$	Reverse-current Leakage Current after Reverse Current Event	V_{OUT} – V_{IN} > $V_{REVERSE}$; T_A = 25°C; ON1, ON2 = GND	--	0.6	--	μA
$V_{ON[1,2]}$	ON[1,2] Pin Voltage Range		0	--	$V_{IN[1,2]}$	V
$I_{ON(Leakage)}$	ON[1,2] Pin Leakage Current	1.4 V ≤ V_{ON} ≤ V_{IN} or V_{ON} = GND	--	--	1	μA
ON_V_{IH}	ON[1,2] Pin Input High Voltage		1	--	$V_{IN[1,2]}$	V
ON_V_{IL}	ON[1,2] Pin Input Low Voltage		-0.3	0	0.3	V
ON_{HYS}	ON[1,2] Hysteresis		--	60	--	mV

Electrical Characteristics (continued)

1.5 V ≤ $V_{IN[1,2]}$ ≤ 5.5 V; C_{IN} = 1 μF, T_A =-40 °C to 85 °C, unless otherwise noted.
Typical values are at T_A = 25°C (unless otherwise stated)

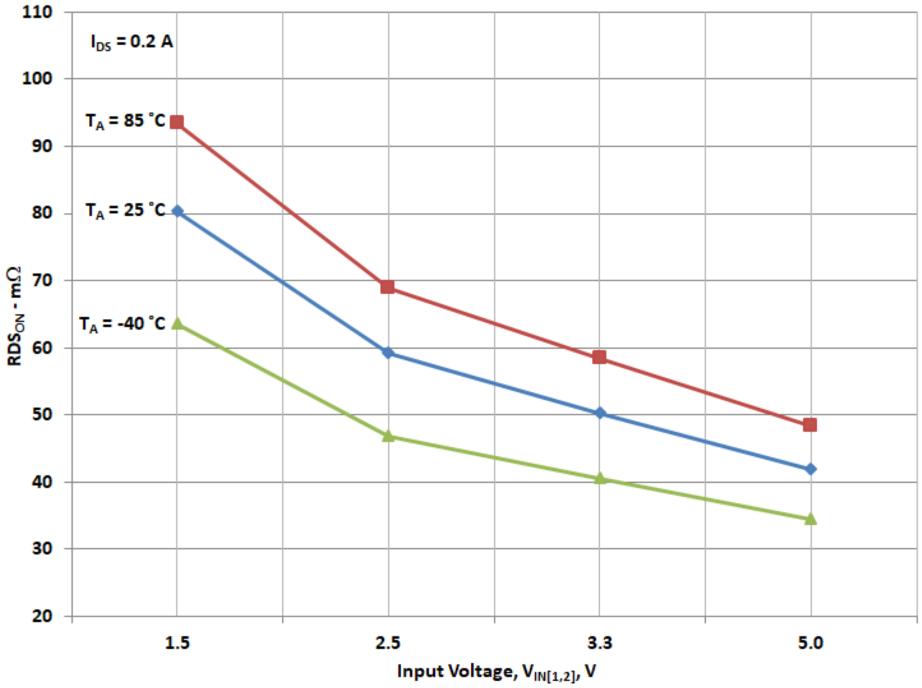
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{REV}	Reverse-current Detect Response Delay	V_{IN} = 5 V	--	10	--	μs
T_{REARM}	Reverse Detect Rearm Time		--	0.6	--	ms
T_{ON_Delay}	ON[1,2] Delay Time	50% ONx to 50% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω , C_{LOAD} = 0.1 μF	--	1.1	1.65	ms
		50% ONx to 50% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	0.8	1.2	ms
$T_{VOUTx(R)}$	$V_{OUT[1,2]}$ Rise Time	10% to 90% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	1.0	1.4	ms
		10% to 90% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	0.5	0.71	ms
$T_{VOUTx(F)}$	$V_{OUT[1,2]}$ Fall Time	90% to 10% V_{OUTx} ↓; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	2.3	3	μs
		90% to 10% V_{OUTx} ↓; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	2.3	3	μs
T_{OFF_Delay}	OFF Delay Time	50% ONx to 50% V_{OUTx} ↓; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	3.1	4.1	μs
		50% ONx to 50% V_{OUTx} ↓; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF	--	5	6.5	μs

T_{ON_Delay}, $V_{S(SR)}$, and T_{Total_ON} Timing Details

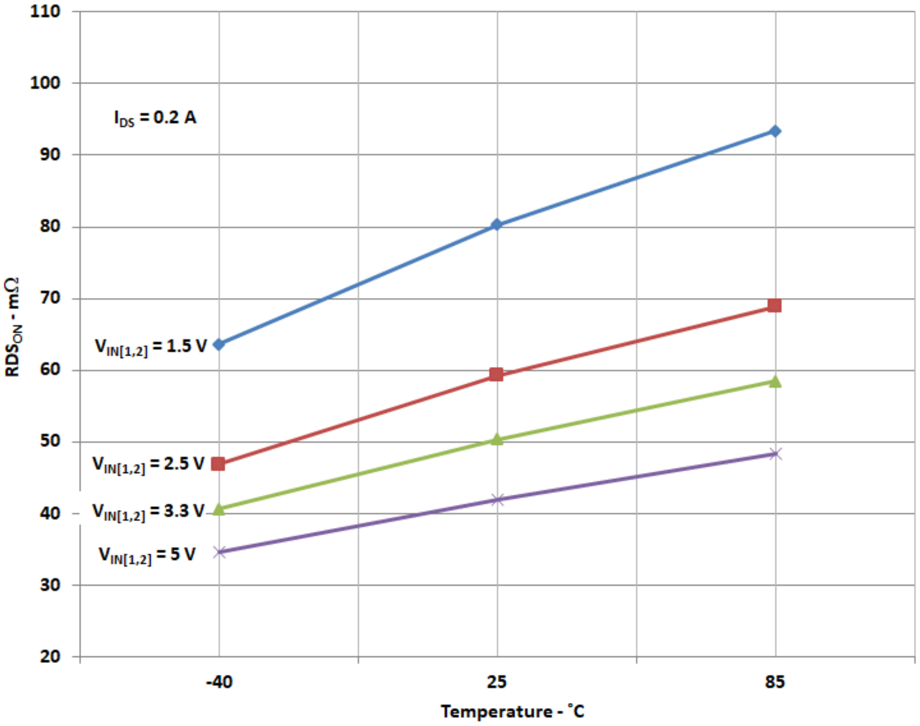


Typical Performance Characteristics

RDS$_{ON}$ vs. V$_{IN[1,2]}$ and Temperature



RDS$_{ON}$ vs.Temperature and V$_{IN[1,2]}$



$V_{IN[1,2]}$ Inrush Current Details

When either channel of the SLG59M1639V is enabled with ON[1,2] ↑, the load switch closes to charge the $V_{OUT[1,2]}$ output capacitor to $V_{IN[1,2]}$. The charging current drawn from $V_{IN[1,2]}$ is commonly referred to as “V_{IN} inrush current” and can cause the input power source to collapse if the V_{IN} inrush current is too high.

Since the $V_{OUT[1,2]}$ rise time of the SLG59M1639V is fixed, $V_{IN[1,2]}$ inrush current is then a function of the output capacitance at $V_{OUT[1,2]}$. The expression relating $V_{IN[1,2]}$ inrush current, the SLG59M1639V $V_{OUT[1,2]}$ rise time, and $C_{LOAD[1,2]}$ is:

$$V_{IN[1,2]} \text{ Inrush Current} = C_{LOAD[1,2]} \times \frac{\Delta V_{OUT[1,2]}}{V_{OUT[1,2]} \text{ Rise Time}}$$

where in this expression $\Delta V_{OUT[1,2]}$ is equivalent to $V_{IN[1,2]}$ if the initial SLG59M1639V’s output voltages are zero.

In the table below are examples of $V_{IN[1,2]}$ inrush currents assuming zero initial charge on $C_{LOAD[1,2]}$ as a function of $V_{IN[1,2]}$.

$V_{IN[1,2]}$	$V_{OUT[1,2]}$ Rise Time	$C_{LOAD[1,2]}$	Inrush Current
1.5 V	0.5 µs	0.1 µF	0.3 mA
5 V	1 µs	0.1 µF	0.5 mA

Since the relationship is linear and If $C_{LOAD[1,2]}$ were increased to 1 µF, then the $V_{IN[1,2]}$ inrush currents would be 10x higher in either example. If a large $C_{LOAD[1,2]}$ capacitor is required in the application and depending upon the strength of the input power source, it may very well be necessary to increase the C_{IN}-to-C_{LOAD} ratio to minimize $V_{IN[1,2]}$ droop during turn-on.

For other $V_{OUT[1,2]}$ rise time options, please contact Renesas for additional information.

Power Dissipation

The junction temperature of the SLG59M1639V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1639V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON1} \times I_{DS1}^2) + (RDS_{ON2} \times I_{DS2}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$RDS_{ON[1,2]}$ = Channel 1 and Channel 2 Power MOSFET ON resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

In nominal operating mode, the SLG59M1639V's power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{INx}-V_{OUTx}) and the magnitude of that channel's output current (I_{OUTx}):

$$PD_{TOTAL} = [(V_{IN1}-V_{OUT1}) \times I_{DS1}] + [(V_{IN2}-V_{OUT2}) \times I_{DS2}] \text{ or}$$

$$PD_{TOTAL} = [(V_{IN1} - (R_{LOAD1} \times I_{DS1})) \times I_{DS1}] + [(V_{IN2} - (R_{LOAD2} \times I_{DS2})) \times I_{DS2}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

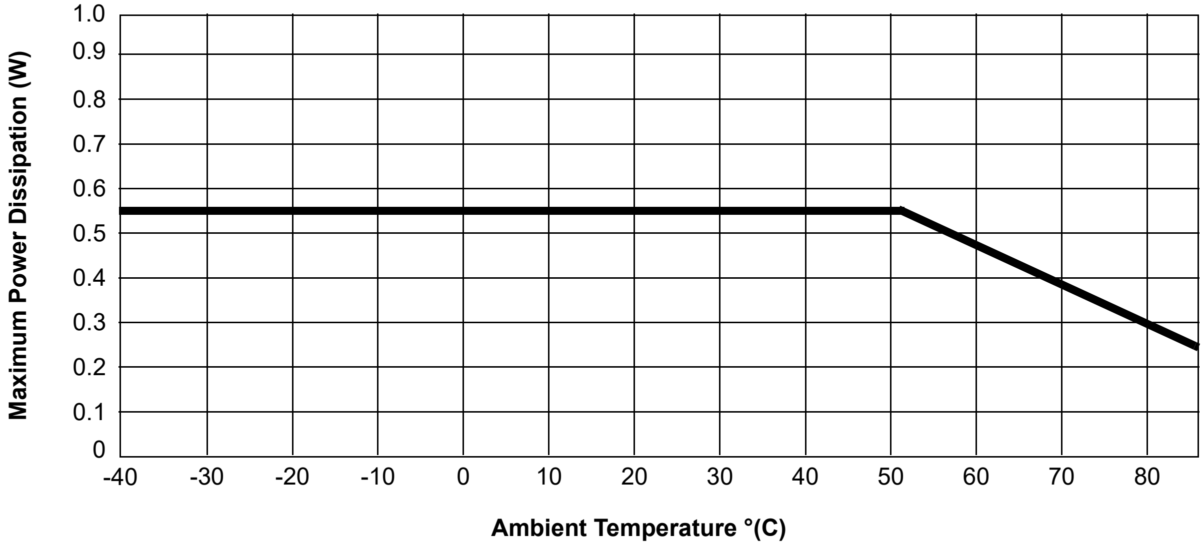
$V_{IN[1,2]}$ = Channel 1 and Channel 2 Input Voltage, in Volts (V), respectively

$R_{LOAD[1,2]}$ = Channel 1 and Channel 2 Output Load Resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 output current, in Amps (A), respectively

$V_{OUT[1,2]}$ = Channel 1 and Channel 2 output voltage, or $R_{LOAD[1,2]} \times I_{DS[1,2]}$, respectively

Power Dissipation Derating Curve



Note: Each V_{IN}, V_{OUT} = 1 in^2 1.2 oz. copper on FR4

Layout Guidelines:

1.Since the VIN[1,2] and VOUT[1,2] pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2.To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1639V's VIN[1,2] and VOUT[1,2] pins;

3.The GND pin should be connected to system analog or power ground plane.

4. 2 oz. copper is recommended for high current operation.

SLG59M1639V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1639V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1639V here

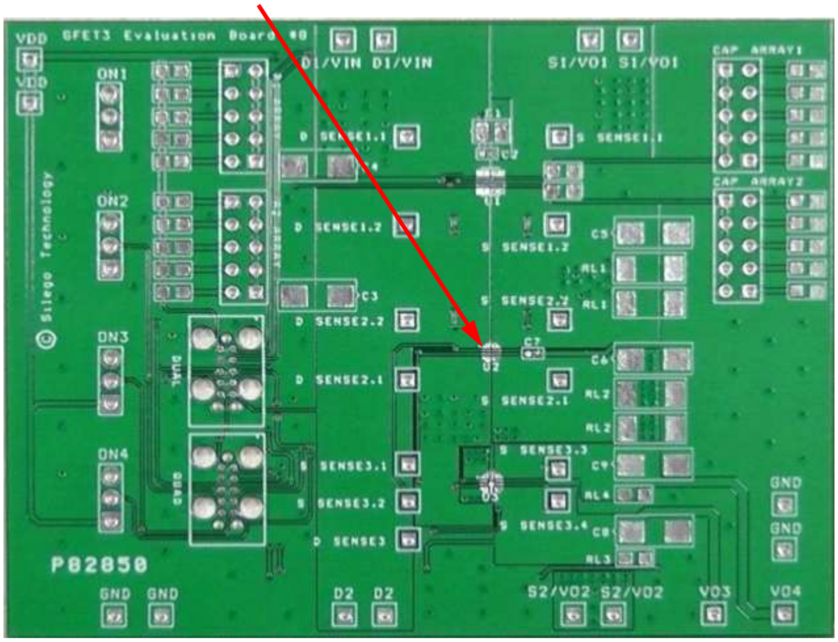


Figure 1. SLG59M1639V Evaluation Board

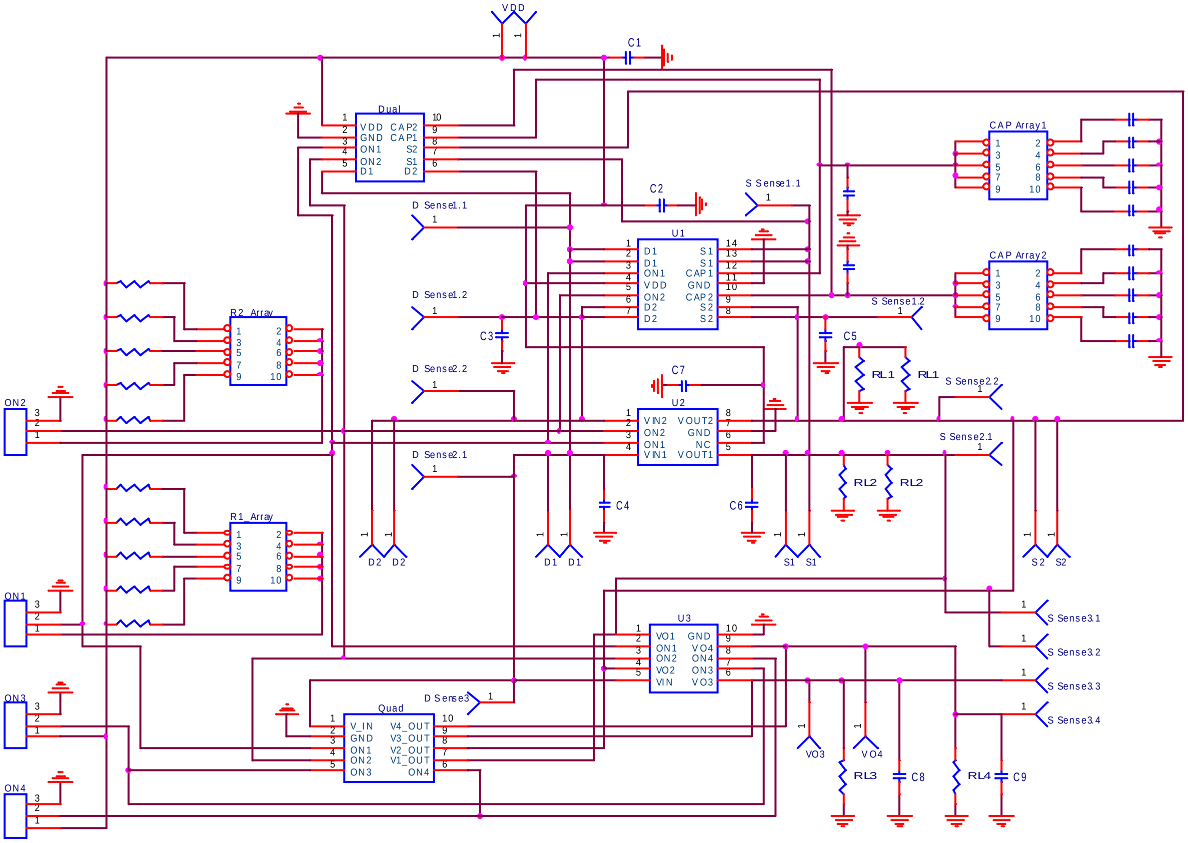


Figure 2. SLG59M1639V Evaluation Board Connection Circuit

Basic Test Setup and Connections

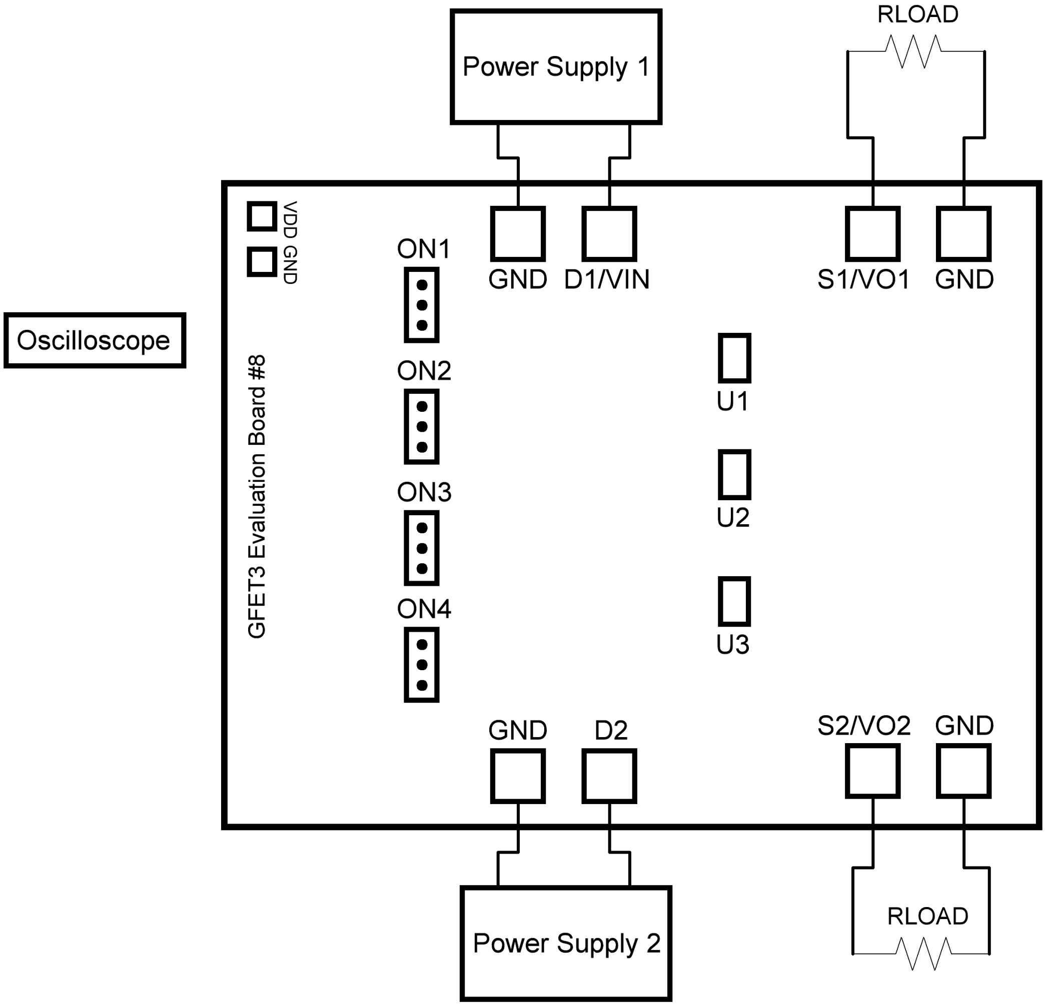


Figure 3. SLG59M1639V Evaluation Board Connection Circuit

EVB Configuration

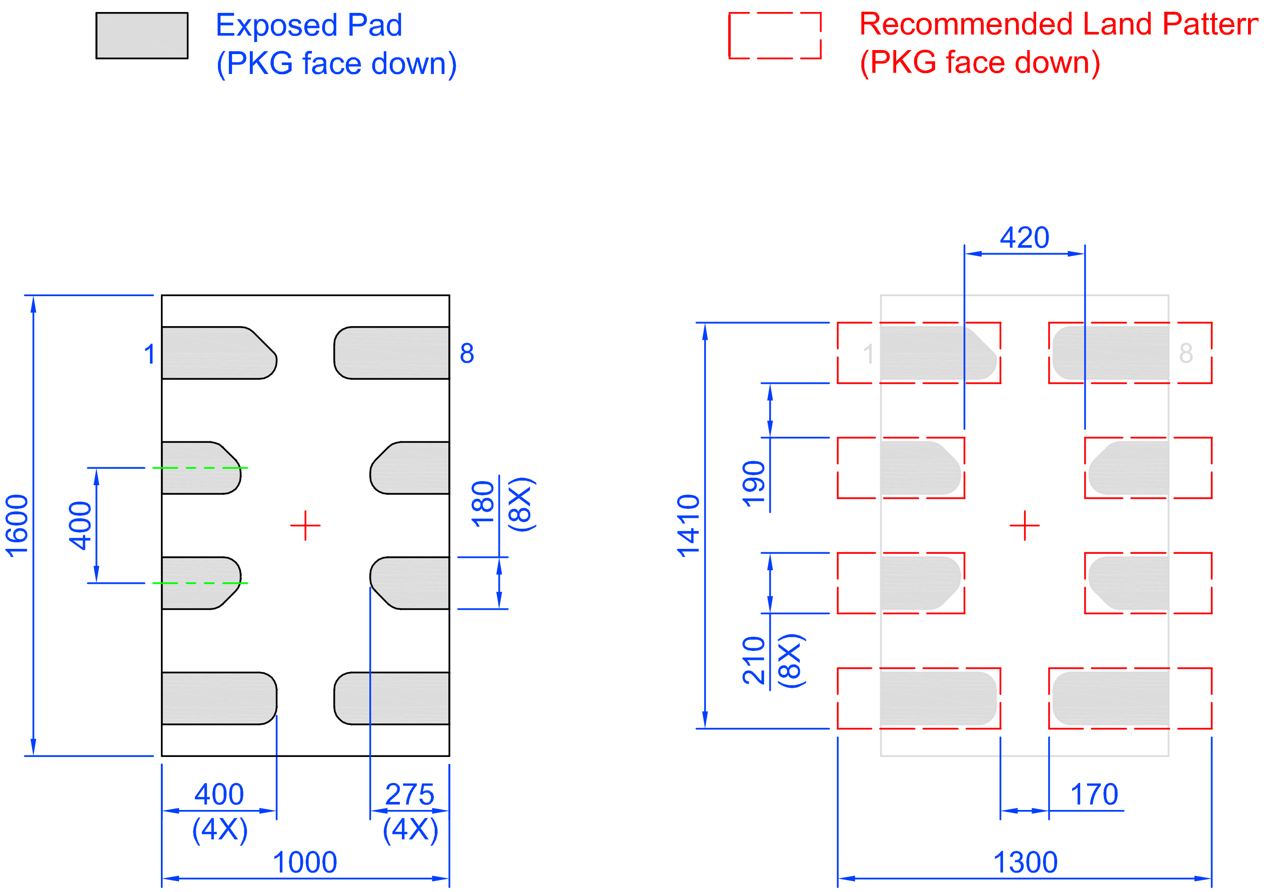
1. Connect oscilloscope probes to D1/VIN, D2, S1/VO1, S2/VO2, ON1, ON2 etc.;

2. Turn on Power Supply 1 and set desired V_{IN1} from 1.5 V…5.5 V range;

3. Turn on Power Supply 2 and set desired V_{IN2} from 1.5 V…5.5 V range;

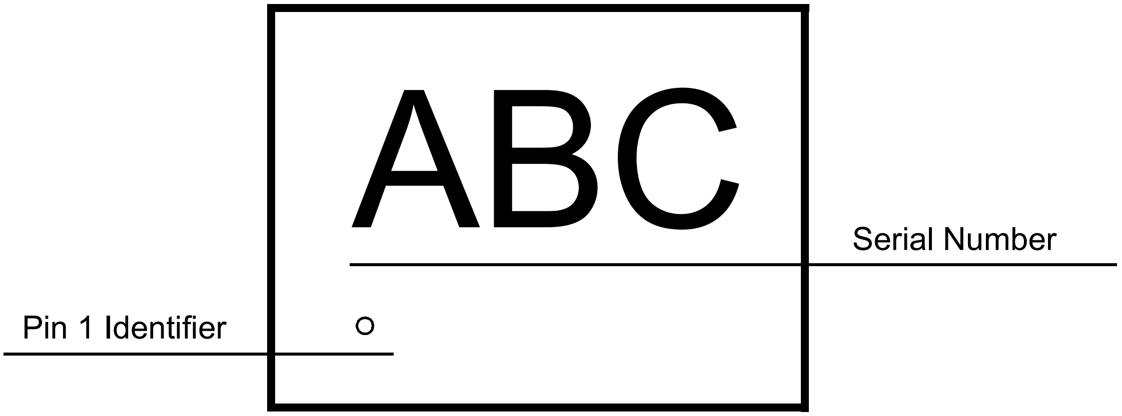
4. Toggle the ON[1,2] signal High or Low to observe SLG59M1639V operation.

SLG59M1639V Layout Suggestion



Note: All dimensions shown in micrometers (µm)

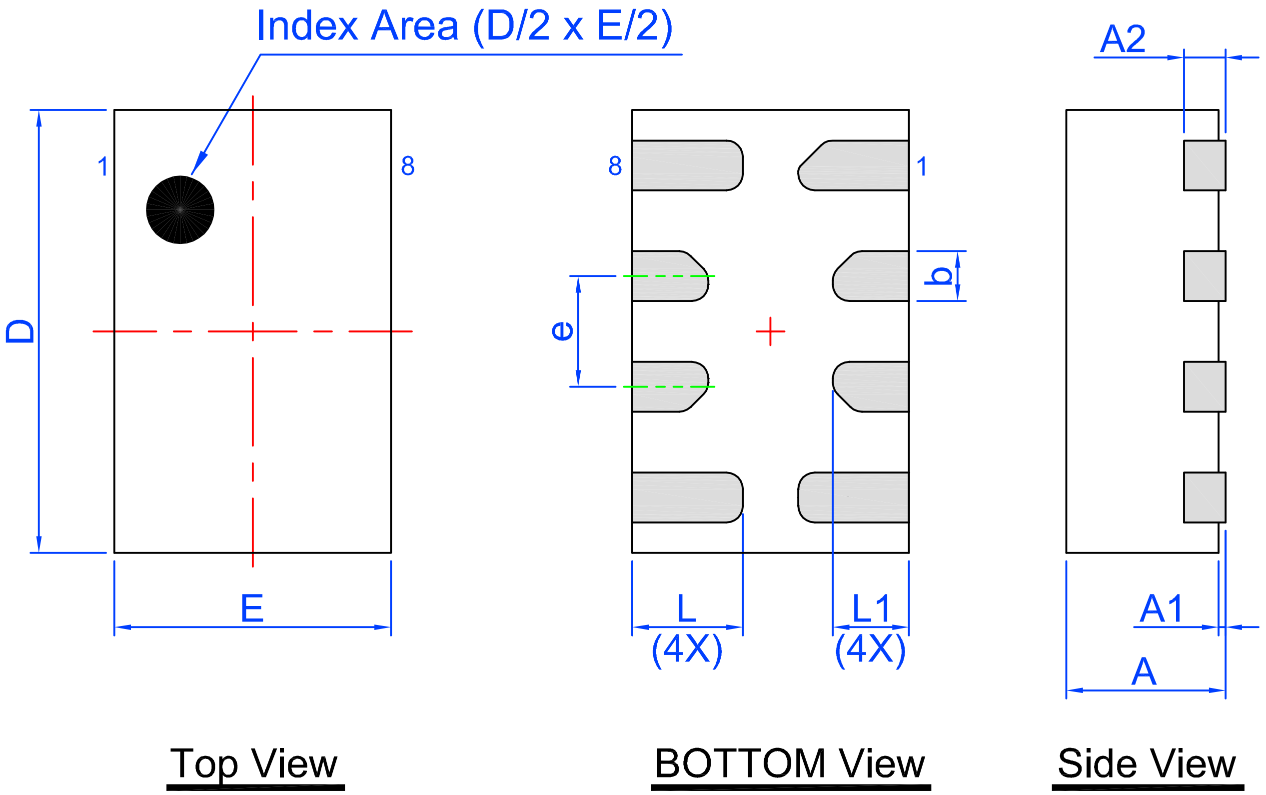
Package Top Marking System Definition



ABC - 3 alphanumeric Part Serial Number
where A, B, or C can be A-Z and 0-9

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

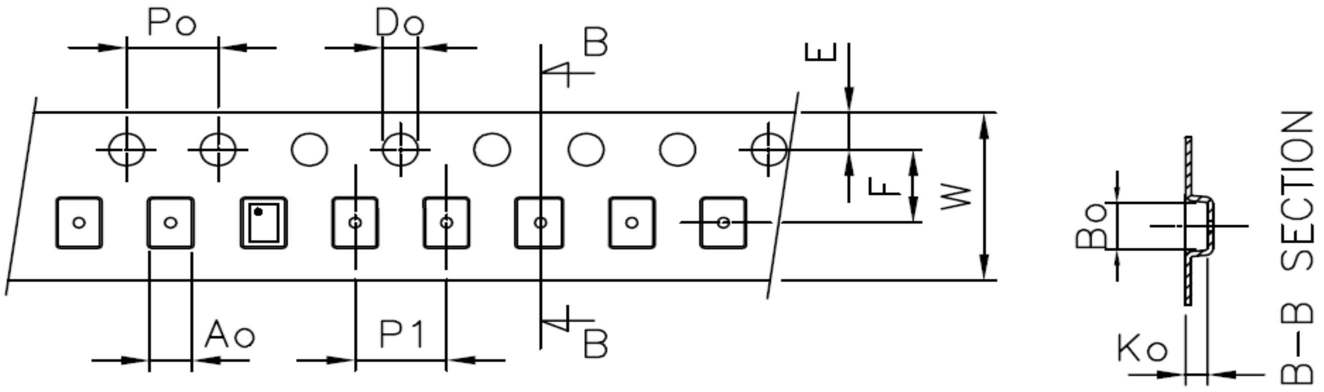
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.225	0.275	0.325
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FCD Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FCD Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/4/2022	1.08	Updated Company name and logo Fixed typos Added Layout Guidelines
9/17/2018	1.07	Updated style and formatting Updated Charts
8/29/2017	1.06	Updated Inrush Current Details Fixed typos
4/13/2017	1.05	Fixed Reverse Voltage Detection equation
4/18/2016	1.04	Updated Electrical Characteristics
4/1/2016	1.03	Fixed typo in Pin Configuration
2/17/2016	1.02	Updated POD and Landing Pattern
2/9/2016	1.01	Updated Electrical Characteristics
2/3/2016	1.00	Production Release

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