SLG7BC48195

GreenPAK ™

OSFP Low-Speed Host Controller

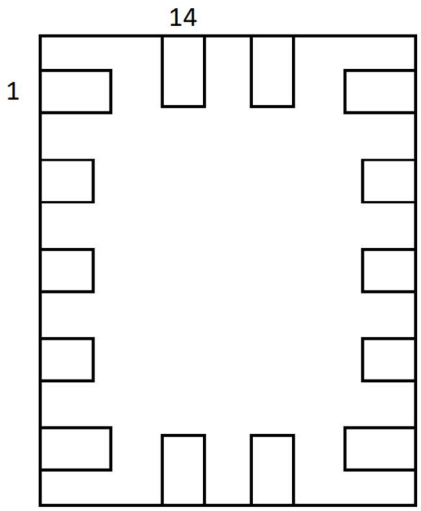
General Description

Renesas SLG7BC48195 is a low power and small form device. The SoC is housed in a 1.6mm x 2.0mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Pin Configuration



14-pin STQFN (Top View)

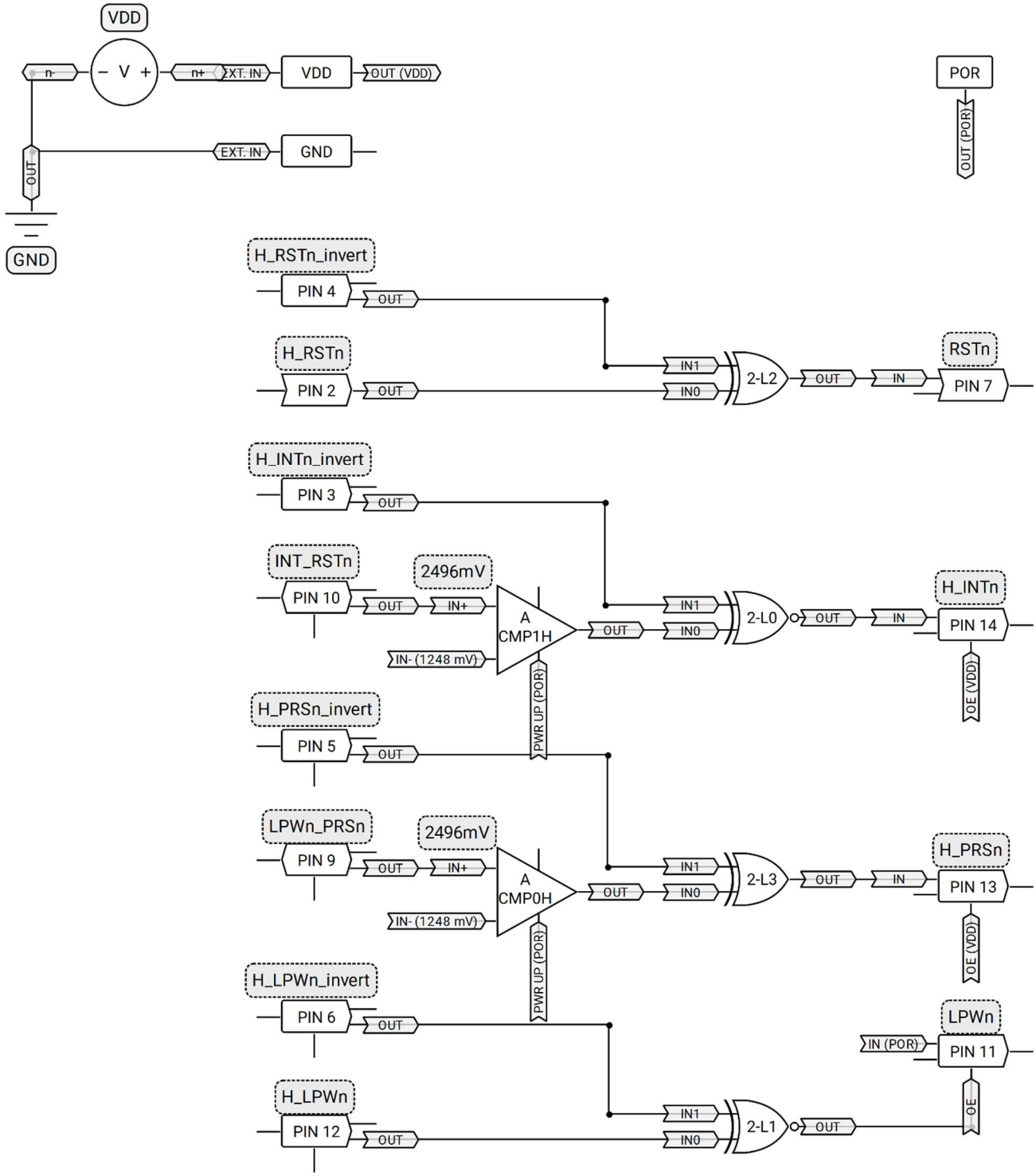
Output Summary

1 Output - 3-State Output 1X
1 Output - Open Drain NMOS 1X
2 Outputs - Push Pull 1X

Pin Name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	H_RSTn	9	LPWn_PRSn
3	H_INTn_invert	10	INT_RSTn
4	H_RSTn_invert	11	LPWn
5	H_PRSn_invert	12	H_LPWn
6	H_LPWn_invert	13	H_PRSn
7	RSTn	14	H_INTn

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	H_RSTn	Digital Input	Digital Input without Schmitt trigger	10kΩ pulldown
3	H_INTn_invert	Digital Input	Digital Input without Schmitt trigger	floating
4	H_RSTn_invert	Digital Input	Digital Input without Schmitt trigger	floating
5	H_PRSn_invert	Digital Input	Digital Input without Schmitt trigger	floating
6	H_LPWn_invert	Digital Input	Digital Input without Schmitt trigger	floating
7	RSTn	Digital Output	Open Drain NMOS 1X	floating
8	GND	GND	Ground	--
9	LPWn_PRSn	Analog Input/Output	Analog Input/Output	floating
10	INT_RSTn	Analog Input/Output	Analog Input/Output	floating
11	LPWn	Digital Output	3-State Output 1X	floating
12	H_LPWn	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
13	H_PRSn	Digital Output	Push Pull 1X	floating
14	H_INTn	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7BC48195V	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	V_{DD}+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	OD 1x	--	11	
Current at Input Pin		-1.0	1.0	mA
Input leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		0.1	--	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	57	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 1)	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 1)	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.7	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.218	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.087	V
I_{OH}	HIGH-Level Output Current (Note 2)	Push-Pull 1X, V_{OH}=2.4V at VDD=3.3V	5.61	--	--	mA
I_{OL}	LOW-Level Output Current (Note 2)	Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	5.42	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	13.35	--	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 12	--	10	--	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	--	10	--	kΩ
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	2403	--	2539	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	2356	--	2577	mV
		High to Low transition, at temperature 25°C	2403	--	2539	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2356	--	2577	mV

V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	2392	--	2555	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	2350	--	2583	mV
		High to Low transition, at temperature 25°C	2392	--	2555	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2350	--	2583	mV
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note 1 No hysteresis.
Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 3 Guaranteed by Design.

Description

The SLG7BC48195 OSFP Low-Speed Host Controller device contains INT_RSTn and LPWn_PRSn signal transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when H_RSTn is asserted low. The module signals an interrupt to the host when H_INTn is asserted low.

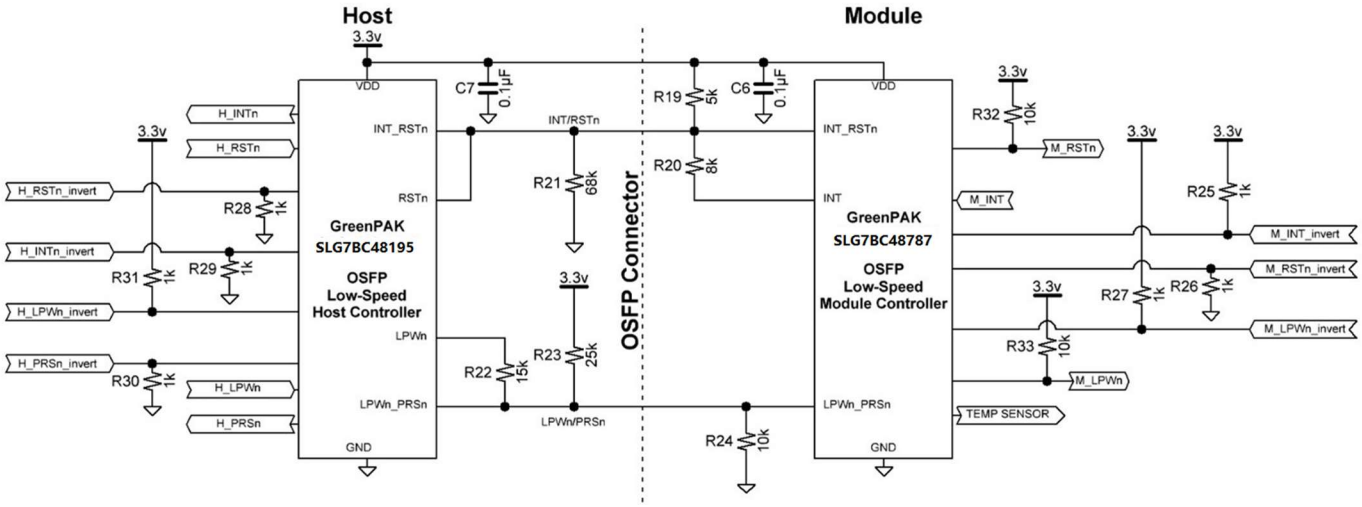
LPW_PRS is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG7BC48195) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when H_LPWn is asserted low.

The MSA defines the multi-level signaling of the INT_RSTn and LPWn_PRSn lines. The MSA also defines the polarities of the Host and Module signals (i.e. M_RSTn, M_INT, H_INTn, H_LPWn). In order to guarantee the SLG7BC48195 operates with all polarities following the MSA spec, tie according to Table1 below.

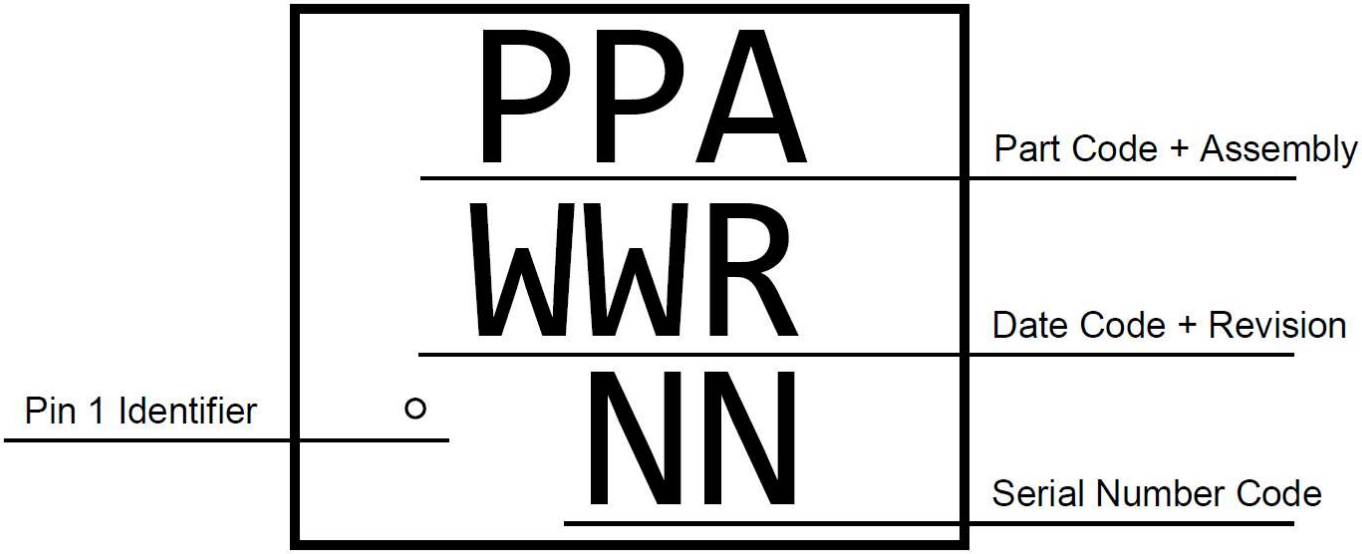
Table 1: Pullups/downs to conform to MSA Standard Polarities

Pin Name	Resistor
H_INTn_invert	1kΩ Pull Down
H_RSTn_invert	1kΩ Pull Down
H_PRSn_invert	1kΩ Pull Down
H_LPWn_invert	1kΩ Pull Up

Typical Application Circuit



Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	001	L	0xB7FA8FDB	1LK	A	04/17/2025

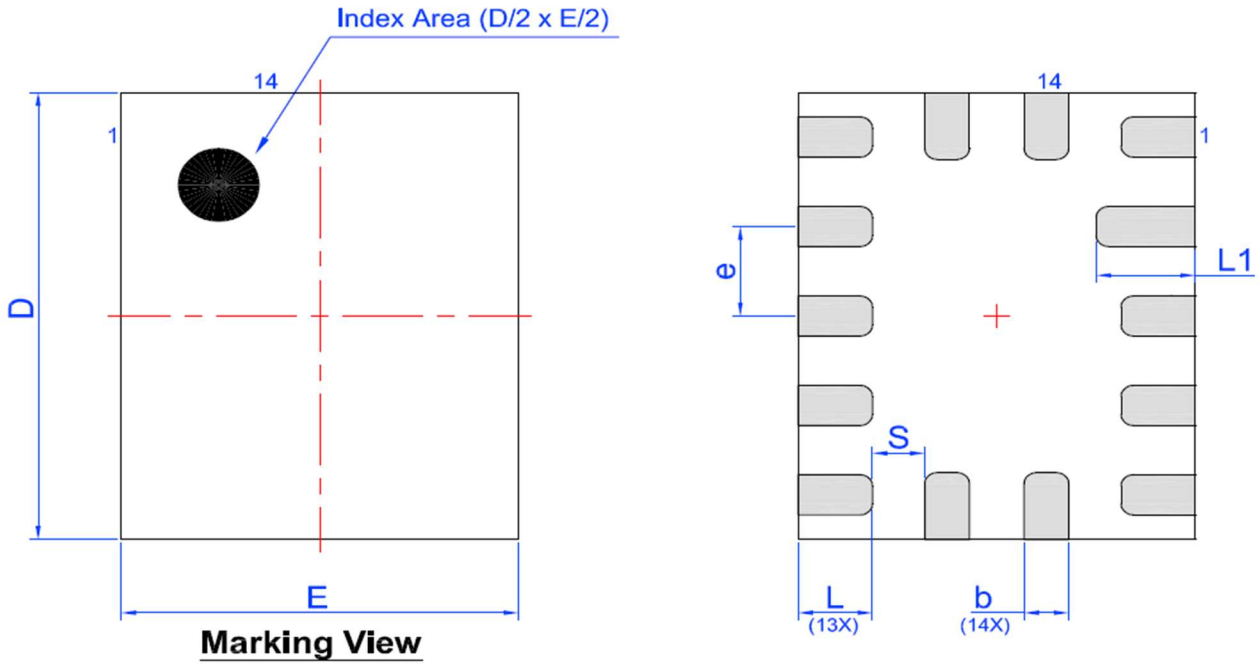
Lock coverage for this part is indicated by √, from one of the following options:

	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
√	All lock read/write (mode 6)

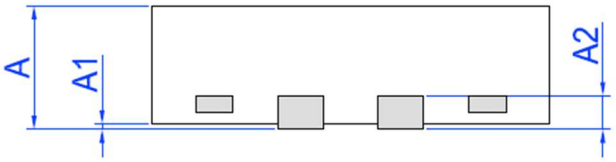
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Marking View



Marking View

Unit: mm

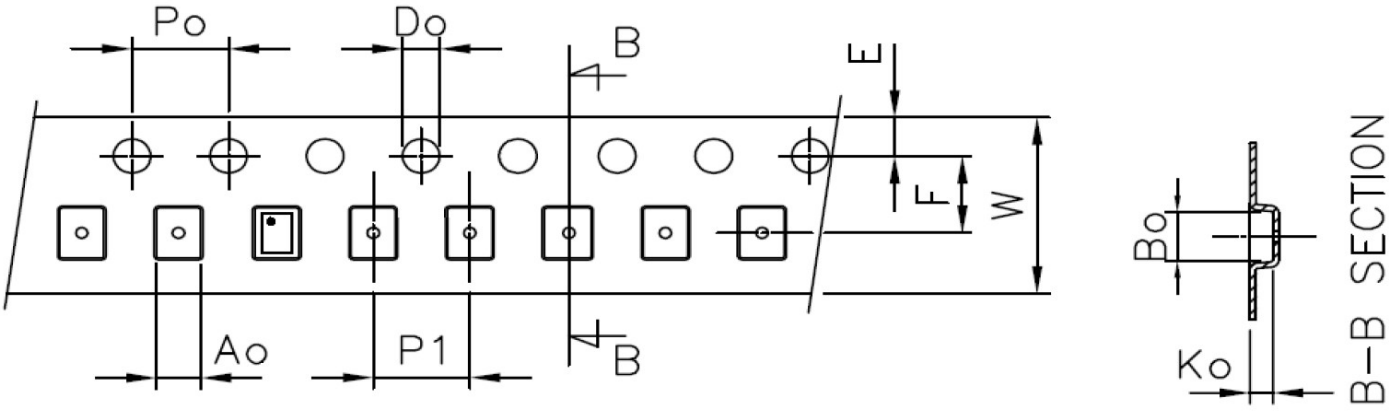
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

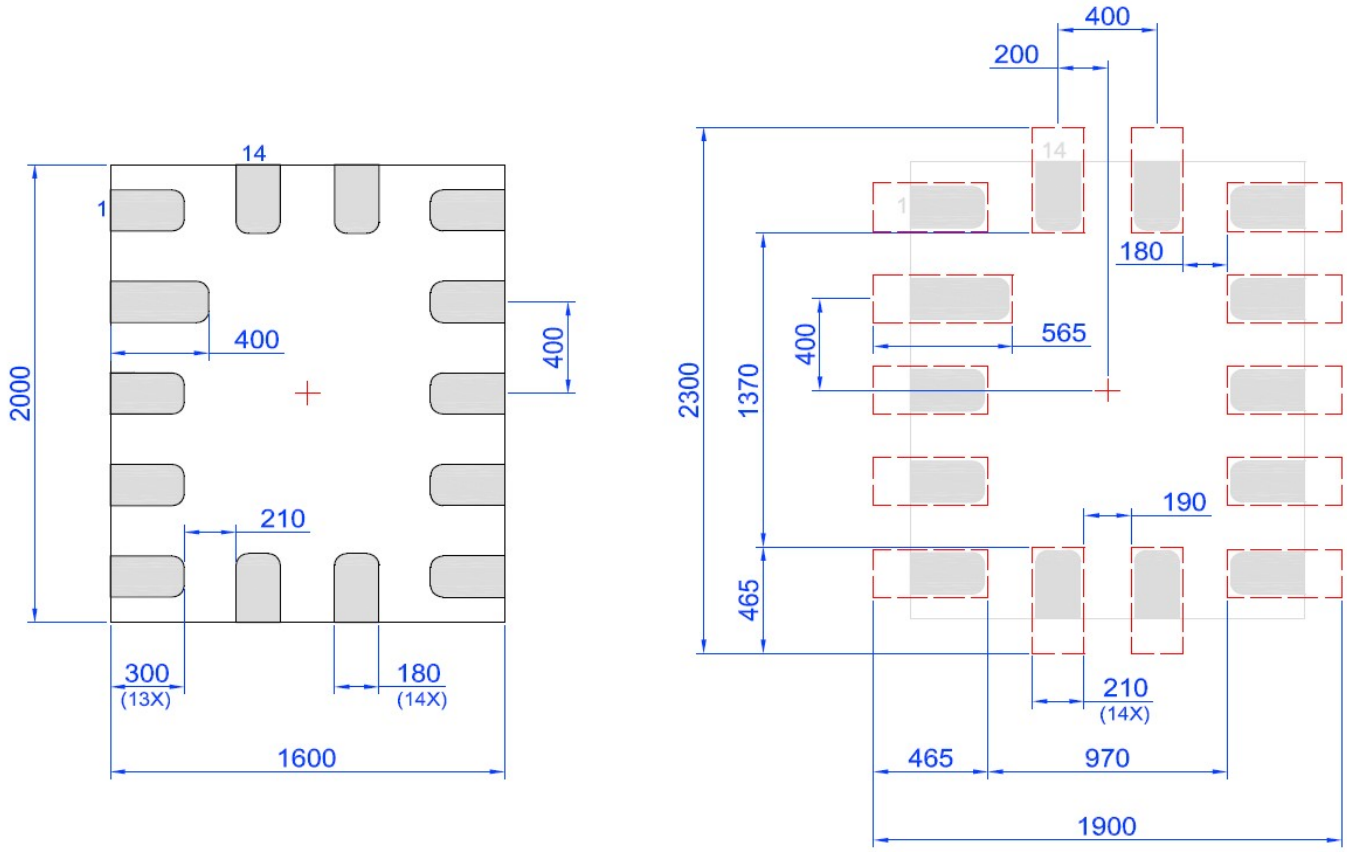
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Layout Guidelines



Unit: um

Datasheet Revision History

Date	Version	Change
10/16/2024	0.10	New design
12/17/2024	0.11	Updated DRS Table
01/07/2025	1.00	Updated to Production Datasheet
04/17/2025	1.01	Add Descriptions and application circuits to DS