SLG7MD47679

Full Bridge PWM Motor Driver

The SLG7MD47679 is a versatile solution for H-Bridge motor driving applications, offering configurable PWM macro cells and high voltage outputs. These outputs, with their high voltage and current handling capabilities, provide a robust foundation for complex motor or load drive applications, smart level translators, and efficient management of high voltage, high current loads.

The SLG7MD47679 has a compact design, versatile functionality, and low power consumption, making it an ideal choice for designers and engineers seeking innovative solutions in modern electronics. It prioritizes power efficiency, operating with minimal energy expenditure due to its low power consumption. PWM current control is possible by utilizing a resistor between the RS PIN and GND.

Additionally, the device includes important protection features such as undervoltage lockout, overcurrent protection, and thermal shutdown, ensuring reliable and safe operation in various environments.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations visit the GreenPAK website.

Click here to download the GreenPAK file for the SLG7MD47679 design.

Email GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

- Two high voltage high current drive GPOs
- 3 A peak, 1.5 A RMS per Full Bridge
- Current up to 3 A peak, 1.5 A RMS per GPO/Half Bridge and up to 6 A peak, 3 A RMS for two HV GPOs connected in parallel
- Current sense comparator with dynamical Vref mode
- Two PWM macrocells
- Low power consumption
- RoHS compliant/Halogen-free
- 20-pin STQFN: 2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm pitch

Applications

- Printers
- Vacuum cleaners/vacuum robots
- Medical devices
- Metering devices (electric, water)
- Dispensing machines
- Robotics

Output Summary

- Two Outputs – analog input/output
- High Voltage High Current Drive GPO

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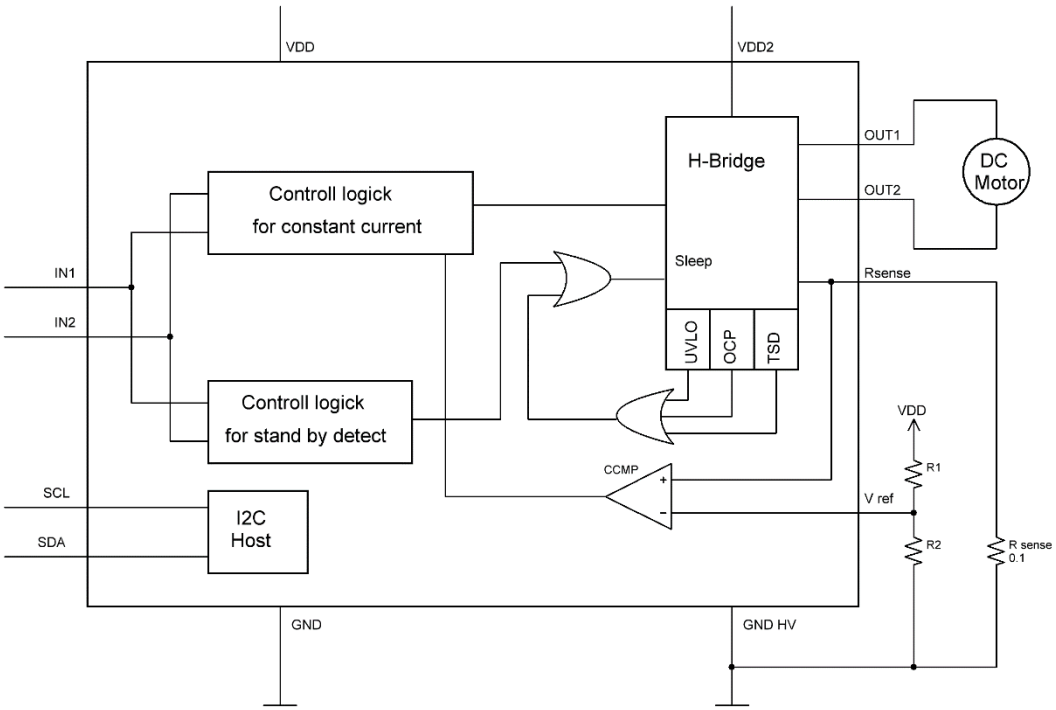


Figure 1. Functional Block Diagram

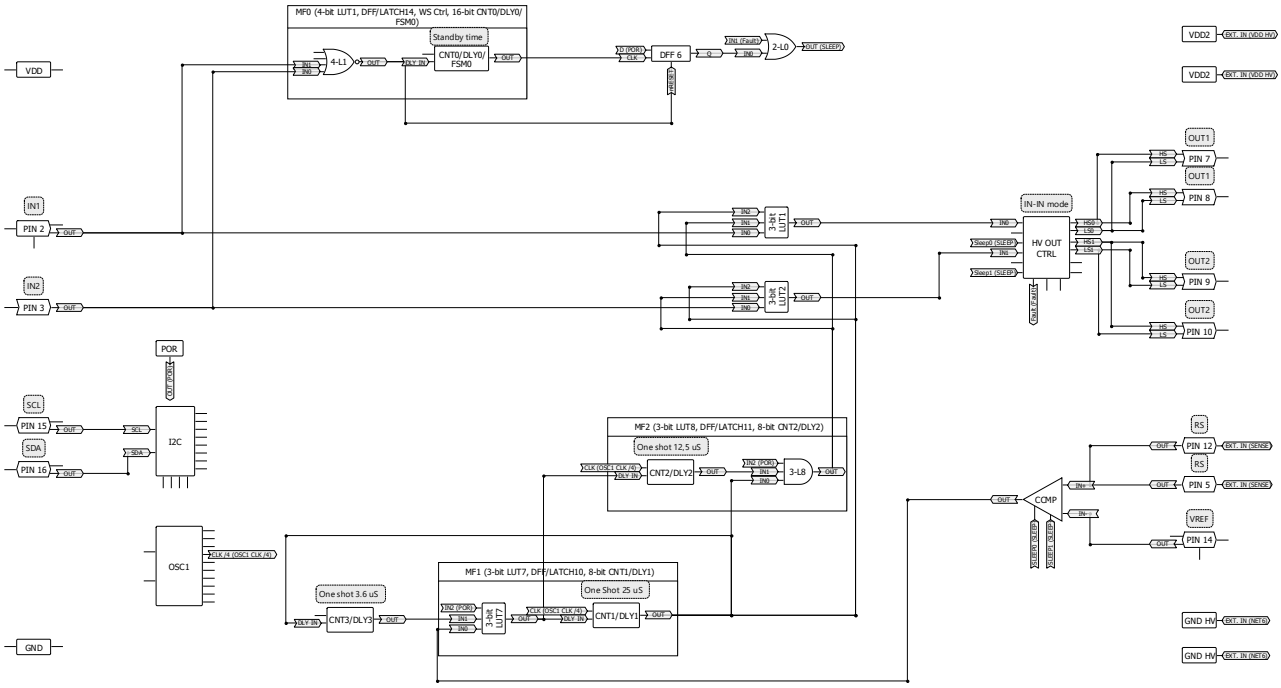
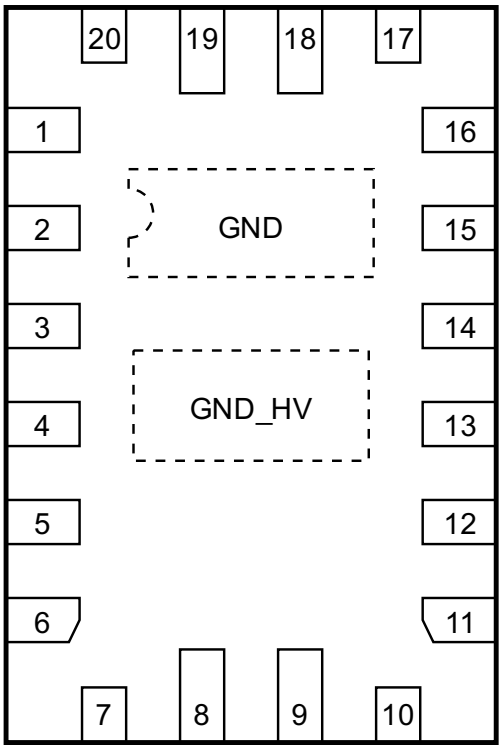


Figure 2. Design Block Diagram

2. Pin Information

2.1 Pin Assignments



STQFN-20L

(Top View)

Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin #	Pin Name	Type	Description	Internal Resistor
1	V_{DD}	PWR	Supply Voltage	--
2	IN1	Digital Input	Digital Input with Schmitt Trigger	100 kΩ Pull-Down
3	IN2	Digital Input	Digital Input with Schmitt Trigger	100 kΩ Pull-Down
4	GND_HV	GND_HV	High Voltage Ground	--
5	RS	Analog Input/Output	Analog Input/Output/Analog Input/Output	Floating
6	V_{DD2}	PWR	Supply Voltage	--
7	OUT1	Digital Output	High and Low MOSFET On	--
8	OUT1	Digital Output	High and Low MOSFET On	--

Pin #	Pin Name	Type	Description	Internal Resistor
9	OUT2	Digital Output	High and Low MOSFET On	--
10	OUT2	Digital Output	High and Low MOSFET On	--
11	V_{DD2}	PWR	Supply Voltage	--
12	RS	Analog Input/Output	Analog Input/Output/Analog Input/Output	Floating
13	GND_HV	GND_HV	High Voltage Ground	--
14	Vref	Analog Input/Output	Analog Input/1x 3-State Output	Floating
15	SCL	Digital Input	--	Floating
16	SDA	Digital Input	--	Floating
17	NC	--	Keep Floating or Connect to GND	--
18	GND	GND	Ground	--
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--

3. Specifications

3.1 Absolute Maximum Ratings

Parameter		Description	Condition	Min	Max	Unit
Supply Voltage on V_{DD} relative to GND				-0.3	7.0	V
Supply Voltage on V_{DD2} relative to GND				-0.3	32	V
DC Input Voltage				GND - 0.5	V_{DD} + 0.5	V
Maximum V_{DD} Average or DC Current		(Through V_{DD} or GND Pin) for V_{DD} Group		--	120	mA
Maximum V_{DD2} or Sense Average or DC Current		Through V_{DD2} or SENSE Pin		--	2000	mA
Maximum Average or DC Current (V_{DD} Power Supply)	Push-Pull 1x	Through V_{DD} Group Pins	T_J = -40 °C to 85 °C	--	11	mA
			T_J = -40 °C to 150 °C	--	3.8	mA
Maximum Average or DC Current (V_{DD2} Power Supply)	Push-Pull/ Half Bridge	Through V_{DD2} High Current Group Pins		--	1500	mA
Current at Input Pin		Through V_{DD} Group Pin		-0.1	1.0	mA
Input Leakage Current (Absolute Value)				--	1000	nA
Storage Temperature Range				-65	150	°C
Junction Temperature				--	150	°C
ESD Protection (Human Body Model)				4000	--	V
ESD Protection (Charged Device Model)				1300	--	V
Moisture Sensitivity Level				1		

3.2 Thermal Information

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance	Θ_{JA}	4L JEDEC PCB	--	--	65	°C/W
		4L JEDEC PCB with a thermal vias that connect thermal pad through all layers of the PCB	--	--	56	°C/W
Junction-to-case (top) Thermal Resistance	$\Theta_{JC(top)}$		--	38.40	--	°C/W
Junction-to-board Thermal Resistance	Θ_{JB}		--	34.88	--	°C/W

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Junction-to-case (top) Characterization Parameter	$\Psi_{JC(top)}$		--	13.46	--	°C/W
Junction-to-board Characterization Parameter	Ψ_{JB}		--	27.24	--	°C/W

3.3 Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.3	3.3	5.5	V
Supply Voltage	V_{DD2}		4.5	24	26.4	V
Operating Temperature	T_A		-40	25	85	°C
Capacitor Value at V_{DD}	C_{VDD}		--	0.1	--	µF
Input Capacitance	C_{IN}		--	2.5	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs	--	22	--	µA
Quiescent Current	I_{Q_VDD2}	Static inputs and floating outputs	--	1	--	µA
Maximum Voltage Applied to any PIN in High Impedance State	V_O	For V_{DD} Group	--	--	V_{DD} + 0.3	V
Maximum Voltage Applied to any PIN in High Impedance State	V_{O2}	For V_{DD2} Group	--	--	V_{DD2} + 0.3	V
HIGH-Level Input Voltage for V_{DD} Group [1]	V_{IH}	Logic input with Schmitt Trigger	0.8 x V_{DD}	--	V_{DD} + 0.3	V
LOW-Level Input Voltage V_{DD} Group[1]	V_{IL}	Logic input with Schmitt Trigger	GND - 0.3	--	0.2 x V_{DD}	V
HIGH-Level Output Voltage for V_{DD} Group, T_J = -40 °C to 85 °C	V_{OH}	Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.1	--	--	V
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.5	--	--	V
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, I_{OH} = 5 mA	4.0	--	--	V
HIGH-Level Output Voltage for V_{DD} Group, T_J = -40 °C to 150 °C		Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.1	--	--	V
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.5	--	--	V
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, I_{OH} = 5 mA	3.9	--	--	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-Level Output Voltage for V_{DD2} High Current Group	V_{OH2}	Push-Pull, V_{DD2} = 5 ± 10 %, I_{OH2} = 10 mA	4.5	--	--	V
		Push-Pull, V_{DD2} = 9 V ± 10 %, I_{OH2} = 10 mA	8.1	--	--	V
		Push-Pull, V_{DD2} = 12 V ± 10 %, I_{OH2} = 10 mA	10.8	--	--	V
		Push-Pull, V_{DD2} = 18 V ± 10 %, I_{OH2} = 10 mA	16.2	--	--	V
		Push-Pull, V_{DD2} = 24 V ± 10 %, I_{OH2} = 10 mA	21.6	--	--	V
LOW-Level Output Voltage for V_{DD} Group, T_J = -40 °C to 85 °C	V_{OL}	Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.1	V
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.2	V
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.2	V
LOW-Level Output Voltage for V_{DD} Group, T_J = -40 °C to 150 °C		Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.1	V
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.2	V
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.3	V
LOW-Level Output Voltage for V_{DD2} High Current Group	V_{OL2}	Push-Pull, V_{DD2} = 5 ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 9 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 12 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 18 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 24 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
HIGH-Level Output Pulse Current [3] Voltage for V_{DD} Group, T_J = -40 °C to 85 °C	I_{OH}	Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	1.4	--	--	mA
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	4.8	--	--	mA
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, V_{OH} = 2.4 V	18.6	--	--	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-Level Output Pulse Current [3] Voltage for V_{DD} Group, T_J = -40 °C to 150 °C	I_{OH}	Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	1.3	--	--	mA
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	4.4	--	--	mA
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, V_{OH} = 2.4 V	16.7	--	--	mA
LOW-Level Output Pulse Current [3] Voltage for V_{DD} Group, T_J = -40 °C to 85 °C	I_{OL}	Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	1.9	--	--	mA
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	6.2	--	--	mA
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, V_{OL} = 0.4 V	9.0	--	--	mA
LOW-Level Output Pulse Current [3] Voltage for V_{DD} Group, T_J = -40 °C to 150 °C		Push-Pull 1x, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	1.6	--	--	mA
		Push-Pull 1x, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	5.2	--	--	mA
		Push-Pull 1x, V_{DD} = 5 V ± 10 %, V_{OL} = 0.4 V	7.5	--	--	mA
Internal Pull-Down Resistance	R_{PULL_DOWN}	Pull-down on PINs 2, 3	--	100	--	kΩ
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	0.91	1.2	ms
Power-On Threshold	PON_{THR}	V_{DD} level required to start up the chip, T_J = -40 °C to 150 °C	1.80	1.98	2.20	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip, T_J = -40 °C to 150 °C	1.30	1.55	1.80	V
Pulse3 Width	T_{OSH3}	At temperature 25 °C	3.4	3.6	3.9	µs
		At temperature -40 °C to 85 °C [4]	3.3	3.6	4.0	µs
Delay0 Time	T_{DLY0}	At temperature 25 °C	0.98	1	1.03	ms
		At temperature -40 °C to 85 °C [4]	0.96	1	1.04	ms
Pulse1 Width	T_{OSH1}	At temperature 25 °C	24.0	25.0	26.0	µs
		At temperature -40 °C to 85 °C [4]	24.0	25.0	26.2	µs
Pulse2 Width	T_{OSH2}	At temperature 25 °C	12.0	12.0	14.0	µs
		At temperature -40 °C to 85 °C [4]	11.0	12.0	14.0	µs

[1] ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}.
[2] No hysteresis.
[3] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
[4] Guaranteed by Design.
[5] Not production tested.

3.4 HV Output Electrical Specifications (Full Bridge or Half Bridge Modes)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Rise Time HV OUT in Motor Drive Mode	t_R	V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to 150 °C	56	107	168	ns
Fall Time HV OUT in Motor Drive Mode	t_F	V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 85 °C	57	129	216	ns
Dead Band Time of HV_GPOx_HD in Motor Drive Mode	T_{DEAD}	V_{DD2} = 4.5 V, T_J = -40 °C to 150 °C	--	91	--	ns
		V_{DD2} = 12 V, T_J = -40 °C to 150 °C	--	85	--	ns
		V_{DD2} = 26.4 V, T_J = -40 °C to 150 °C	--	121	--	ns
Dead Band Time, Generated by PWM Block	PWM_t_{DEAD}	Configured in PWM block	0; 1·Tclk	2·Tclk	3·Tclk	CLK time
HS FET on Resistance (SENSE, GND_HV, and GND Pins are Connected Together)	$R_{DS(ON)}$	V_{DD2} = 4.5 V to 5.5 V, I_O = 500 mA, T_J = 25 °C	--	240	--	mΩ
		V_{DD2} = 4.5 V to 5.5 V, I_O = 500 mA, T_J = 150 °C	--	276	336	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_O = 500 mA, T_J = 25 °C	--	239	--	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_O = 500 mA, T_J = 150 °C	--	276	336	mΩ
LS FET on Resistance (SENSE, GND_HV, and GND Pins are Connected Together, $R_{DS(ON)}$ with Sense Pin = GND, if Sense Pin V_{DD} = 0.5 V, Additional 100 mΩ at Worst Case)	$R_{DS(ON)}$	V_{DD2} = 4.5 V to 5.5 V, I_O = 500 mA, T_J = 25 °C	--	239	--	mΩ
		V_{DD2} = 4.5 V to 5.5 V, I_O = 500 mA, T_J = 150 °C	--	274	338	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_O = 500 mA, T_J = 25 °C	--	235	--	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_O = 500 mA, T_J = 150 °C	--	270	327	mΩ
Off-state Leakage Current	I_{OFF}	GPO0_HD, GPO1_HD [1], V_{DD2} = 5.0 V, T_J = -40 °C to 85 °C, PWM is off, including the charge pump OSC	0	--	9.3	µA
		GPO0_HD, GPO1_HD [1], V_{DD2} = 5.0 V, T_J = -40 °C to 150 °C, PWM is off, including the charge pump OSC	0	--	10.2	µA
Single HV Driver Current Consumption (Including Support Circuits), without Output Load	I_{DD2}	V_{DD2} = 5.0 V, T_J = -40 °C to 150 °C Static (PWM is off), including the charge pump OSC	--	--	115.9	µA
		V_{DD2} = 5.0 V, T_J = -40 °C to 150 °C Switching (PWM = 250 kHz)	--	0.7	1.4	mA
Wake-up Time	t_{WAKE}	HV SLEEP OUT high to output transition, BG is always on, another pins SLEEP - disable	--	80	130	µs

[1] There is a resistive voltage divider in front of Diff Amplifier that is connected to GPO0_HD and GPO1_HD.

3.5 Protection Circuits

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Overcurrent Protection Threshold	I_{OCP}	Per any HS or LS FET	--	3.0	--	A
IN-IN Mode OCP Retry Time	t_{OCP2}_1	Delay = 492 µs	--	490	--	µs
IN-IN Mode OCP Retry Time	t_{OCP2}_2	Delay = 492 µs	--	490	--	µs
Undervoltage Lockout	V_{UVLO}	At falling edge of V_{DD2}	--	2.66	2.8	V
Thermal Shutdown Temperature	T_{TSD}	Junction temperature T_J	135.0	147.4	159.2	°C
Thermal Shutdown Hysteresis	T_{HYST}		--	16.2	--	°C

3.6 I²C Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Clock Frequency, SCL	F_{SCL}		--	--	400	kHz
Clock Pulse Width Low	t_{LOW}		1300	--	--	ns
Clock Pulse Width High	t_{HIGH}		600	--	--	ns
Input Filter Spike Suppression (SCL, SDA)	t_I		--	--	50	ns
Clock Low to Data Out Valid	t_{AA}		--	--	900	ns
Bus Free Time between Stop and Start	t_{BUF}		1300	--	--	ns
Start Hold Time	t_{HD_STA}		600	--	--	ns
Start Set-up Time	t_{SU_STA}		600	--	--	ns
Data Hold Time	t_{HD_DAT}		0	--	--	ns
Data Set-up Time	t_{SU_DAT}		100	--	--	ns
Inputs Rise Time	t_R		--	--	300	ns
Inputs Fall Time	t_F		--	--	300	ns
Stop Set-up Time	t_{SU_STO}		600	--	--	ns
Data Out Hold Time	t_{DH}		50	--	--	ns
[1] Please follow official I²C specification UM10204.						

3.7 Chip Address

HEX	BIN	DEC
0x08	0001000	8

4. Description

Table 1. Truth Table for Inputs and Outputs

IN1	IN2	OUT1	OUT2	Mode
LOW	LOW	Hi-Z	Hi-Z	STOP
				Standby mode after 1 ms
HIGH	LOW	HIGH	LOW	Forward
LOW	HIGH	LOW	HIGH	Reverse
HIGH	HIGH	LOW	LOW	Brake

4.1 Standby Mode

When both IN1 and IN2 pins are set to LOW for 1 ms (typ), the operation mode translates to the standby mode. The following period in which both IN1 and IN2 pins are set to LOW is the standby transition period.

Do not change the input states during this period since the IC becomes unstable.

- If [STOP] mode is used, set period of IN1 = L and IN2 = L to 0.7 ms or less.
- If [Standby] mode is used, set period of IN1 = L and IN2 = L to 1.3 ms or more.

In standby mode, when IN1 or IN2 is set to HIGH, the mode returns from the standby mode, and enters to the operation mode. Maximum 200 µs is required for the return time from the standby release.

The OUT1 and OUT2 outputs operate after 200 µs (max) from the standby release. See Figure 4.

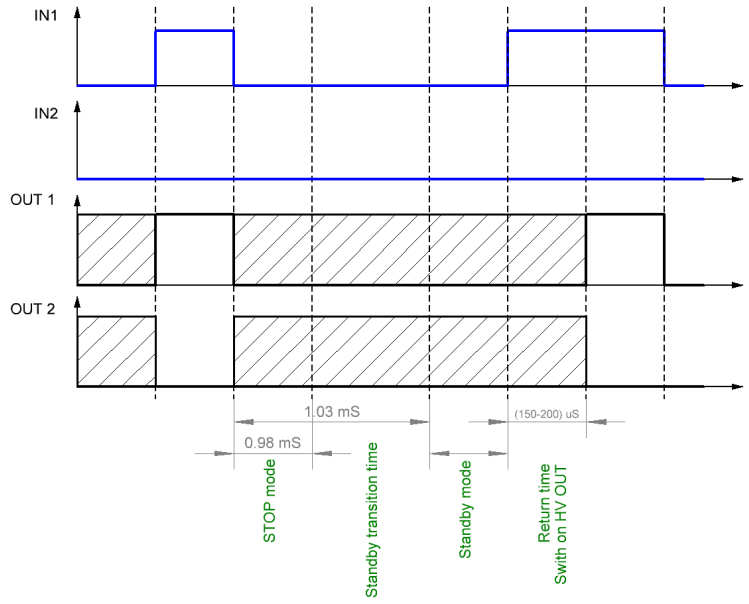


Figure 4. Timing Diagram 1

4.2 Constant Current PWM Blanking Time

In SLG7MD47679, the following blanking time is set to prevent a spike current and external noise which are generated during driving a motor coil. tBLK (for preventing incorrect detection of a spike current at changing from Decay to Charge): 3.6 µs (typ), See Figure 5.

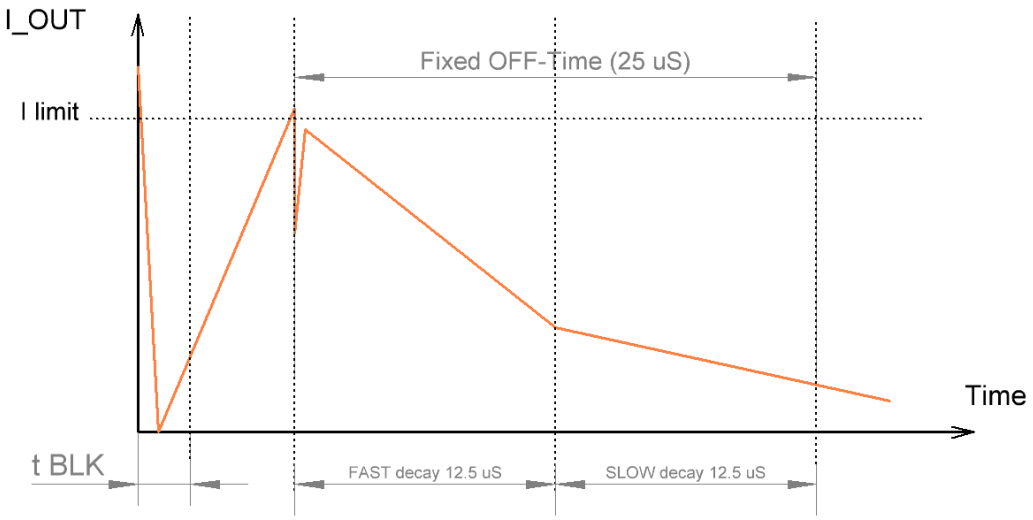


Figure 5. Timing Diagram 2

5. I²C Description

5.1 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 6. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by GPI, GPIO6, GPIO4, and GPIO1. The LSB of the control code is defined by the value of GPI, while the MSB is defined by the value of GPIO1. The address source (either register bit or Pin for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/$\overline{W}$ bit, which selects whether a read command or write command is requested, with a “1” selecting for a Read command, and a “0” selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either “1111” or “0000” in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I² Macrocell on the SLG7MD47679 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be “0” for all commands to the SLG7MD47679.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 6 shows this basic command structure.

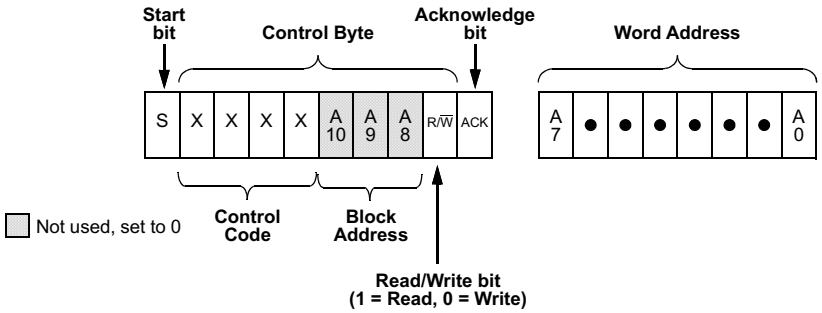


Figure 6. Basic Command Structure

5.2 I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 7. Timing specifications can be found in section 3.6 I2C Specifications.

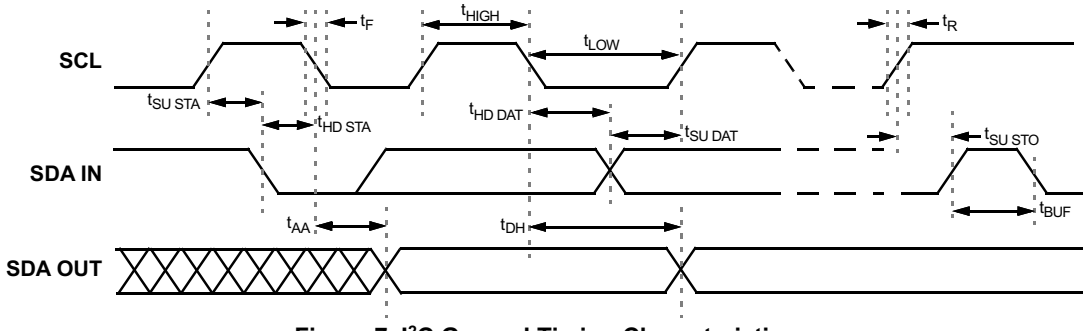


Figure 7. I²C General Timing Characteristics

5.3 I²C Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/$\overline{W}$ bit (set to “0”) are placed onto the I²C bus by the Master. After the SLG7MD47679 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG7MD47679, where the data byte is to be written. After the SLG7MD47679 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG7MD47679 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7MD47679 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1961] = 1 - Enable. It means that IOs will remain their state until the write command is done.

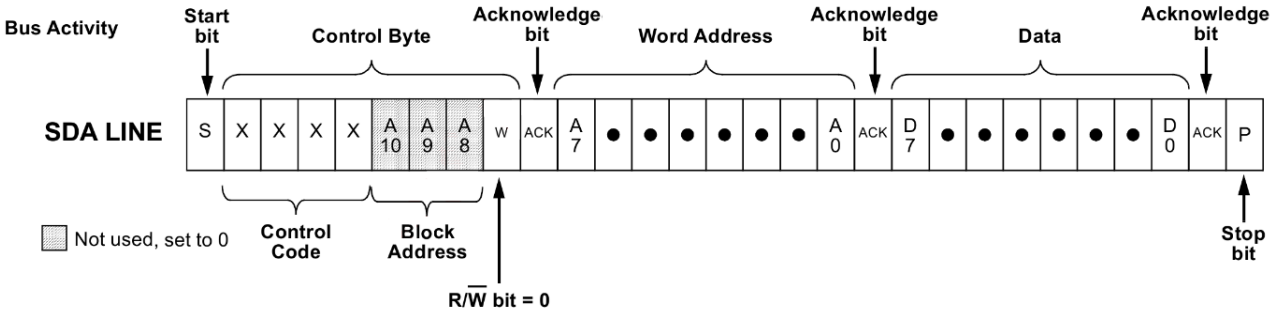


Figure 8. Byte Write Command, R/$\overline{W}$ = 0

5.4 I²C Random Read Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7MD47679 issues an Acknowledge bit, followed by the requested eight data bits.

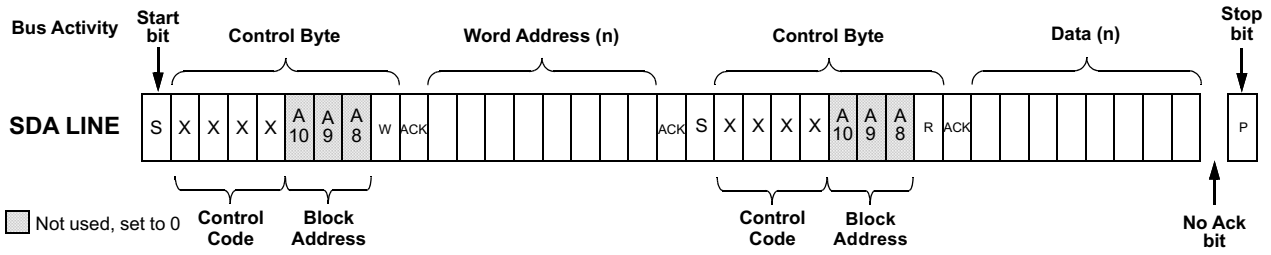


Figure 9. Random Read Command

6. Typical Application Circuit

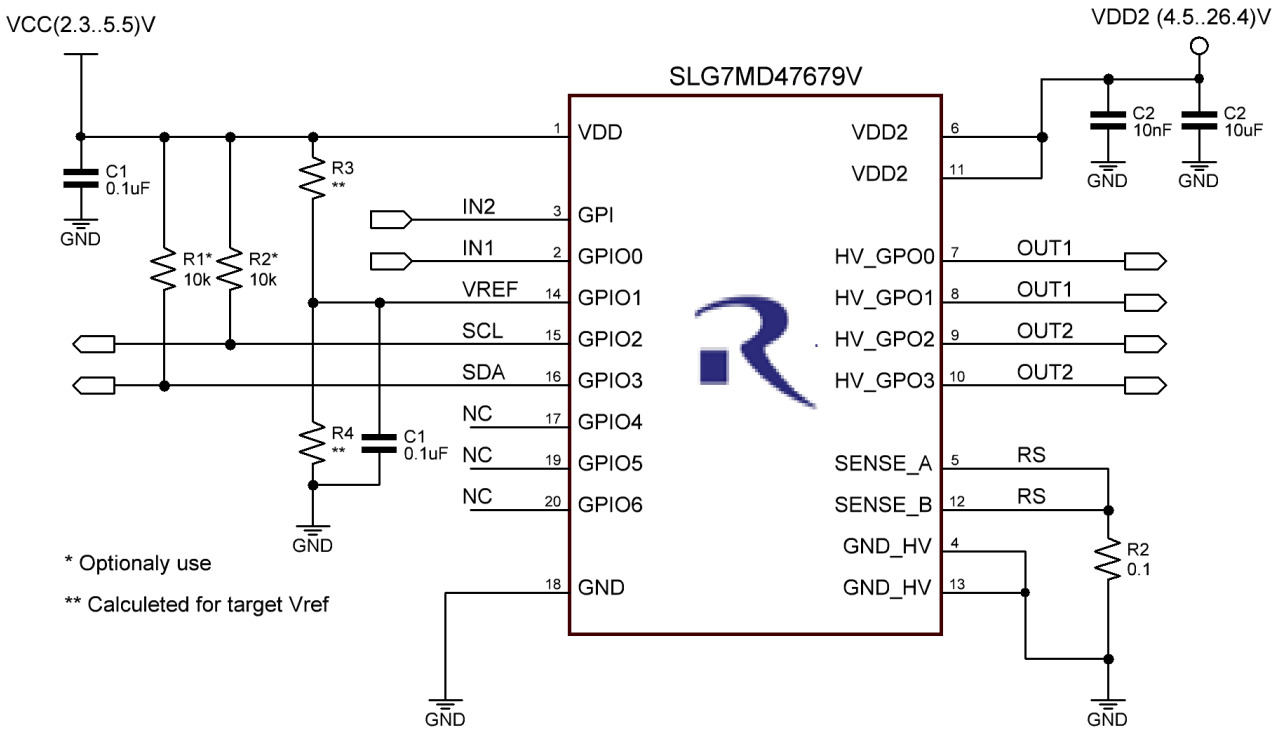
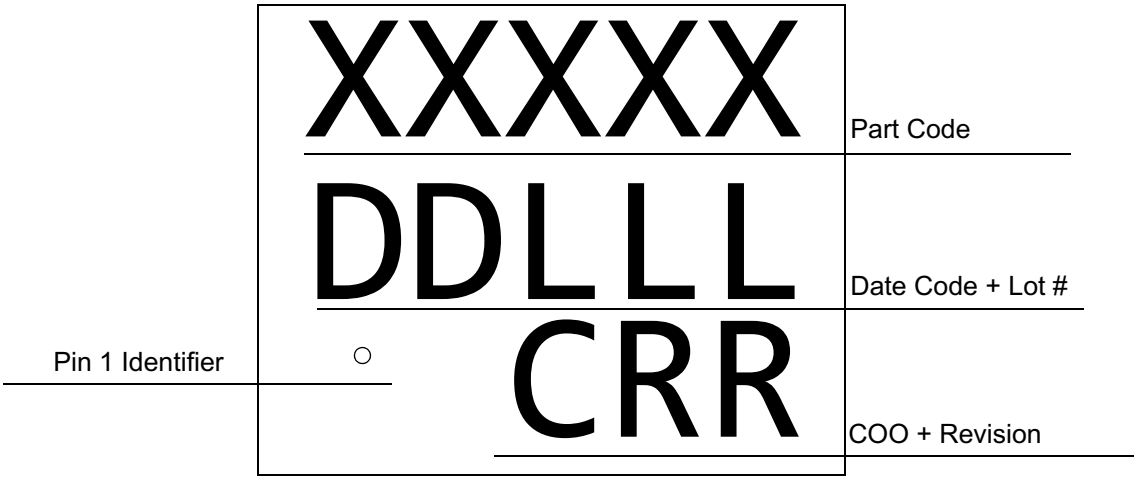


Figure 10. Typical Application Circuit

7. Package Top Marking Definitions



XXXXX - Part ID Field identifies the specific device configuration

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0xD73D6238			6/27/2024

8. Memory Lock Options

Option	Status
Registers	Unlocked

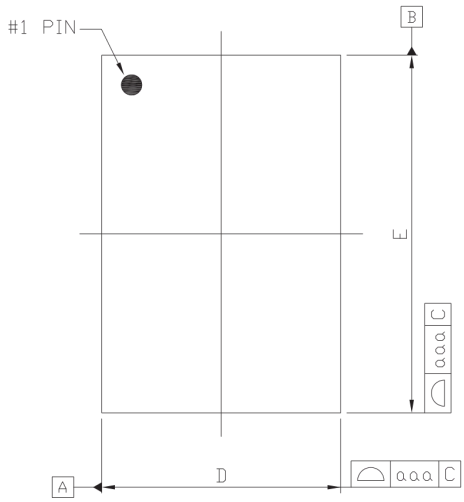
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

9. Package Outlines

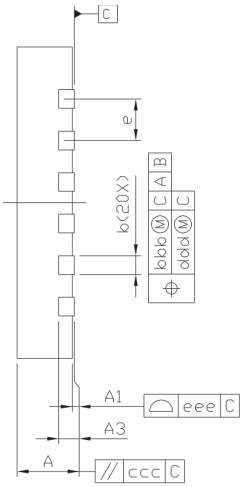
9.1 Package Outlines for STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green Package

JEDEC MO-220

IC Net Weight: 0.008 g



Top View



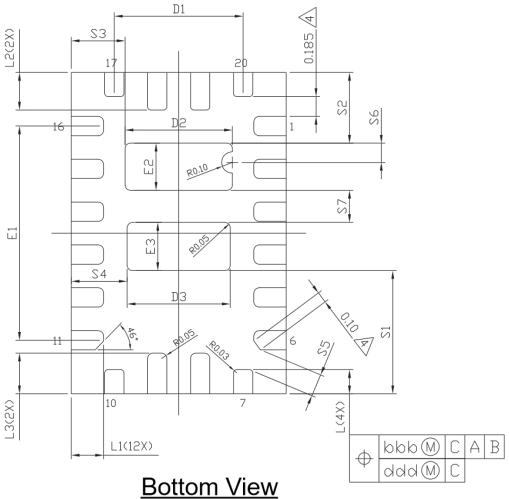
Side View

Notes:

1. All dimensions are in millimeters.

2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

3. Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminal.



Bottom View

Controlling dimension: mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.95	2.00	2.05	0.077	0.079	0.081
E	2.95	3.00	3.05	0.116	0.118	0.120
D1	1.15	1.20	1.25	0.045	0.047	0.049
E1	1.95	2.00	2.05	0.077	0.079	0.081
D2	0.95	1.00	1.05	0.037	0.039	0.041
E2	0.39	0.44	0.49	0.015	0.017	0.019
D3	0.91	0.96	1.01	0.036	0.038	0.040
E3	0.40	0.45	0.50	0.016	0.018	0.020
S1	1.10	1.15	1.20	0.043	0.045	0.047
S2	0.61	0.66	0.71	0.024	0.026	0.028
S3	0.45	0.50	0.55	0.018	0.020	0.022
S4	0.47	0.52	0.57	0.018	0.020	0.022
S5	0.208 REF			0.008 REF		
S6	0.180 REF			0.007 REF		
S7	0.300 REF			0.012 REF		

“A1” max lead co-planarity 0.05 mm
Standard tolerance: ±0.05

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.250	0.300	0.350	0.010	0.012	0.014
L2	0.300	0.350	0.400	0.012	0.014	0.016
L3	0.330	0.380	0.430	0.013	0.015	0.017
b	0.130	0.180	0.230	0.005	0.007	0.009
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.1			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

10. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to 85 °C. To guarantee reliable operation, the junction temperature of the SLG7MD47679 must not exceed 150 °C.

To avoid overheating of the power MOSFETs (as shown in Figure 11), a good thermal design of the PCB layout must be implemented, especially when device operates near its maximum thermal limits. Refer to section 3.2 Thermal Information to find maximum value of Thermal Resistance.

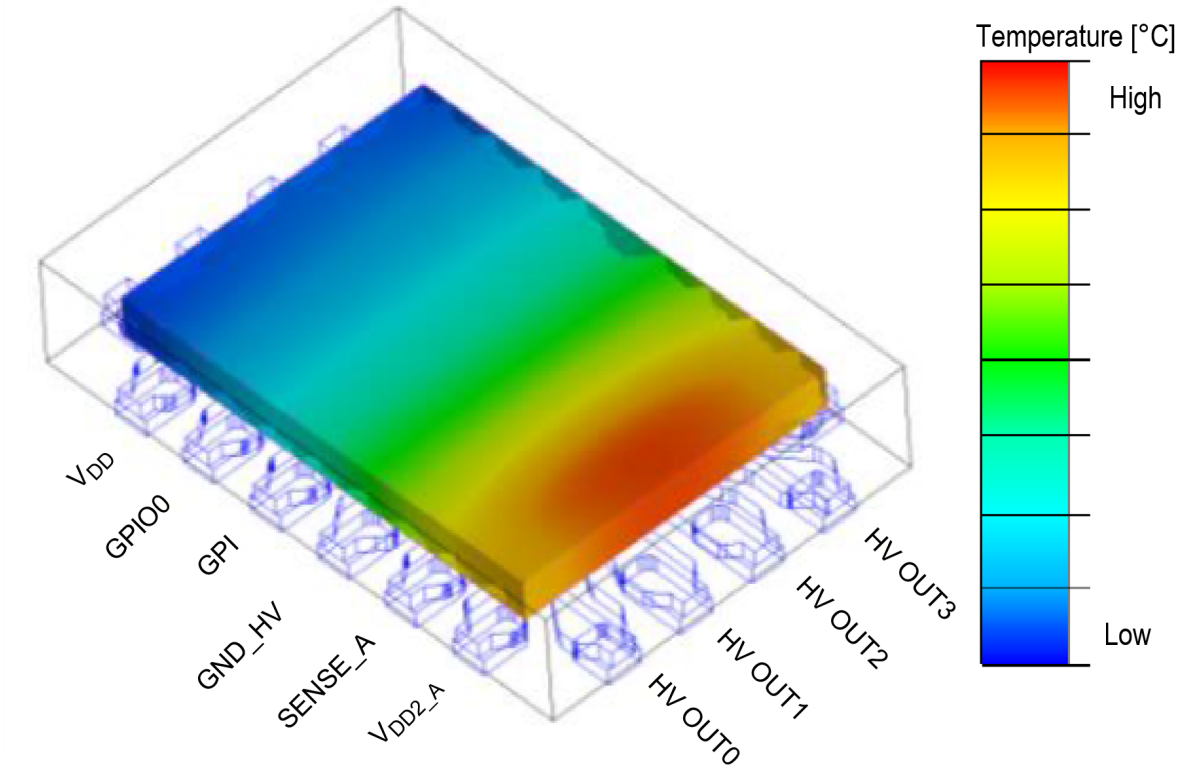


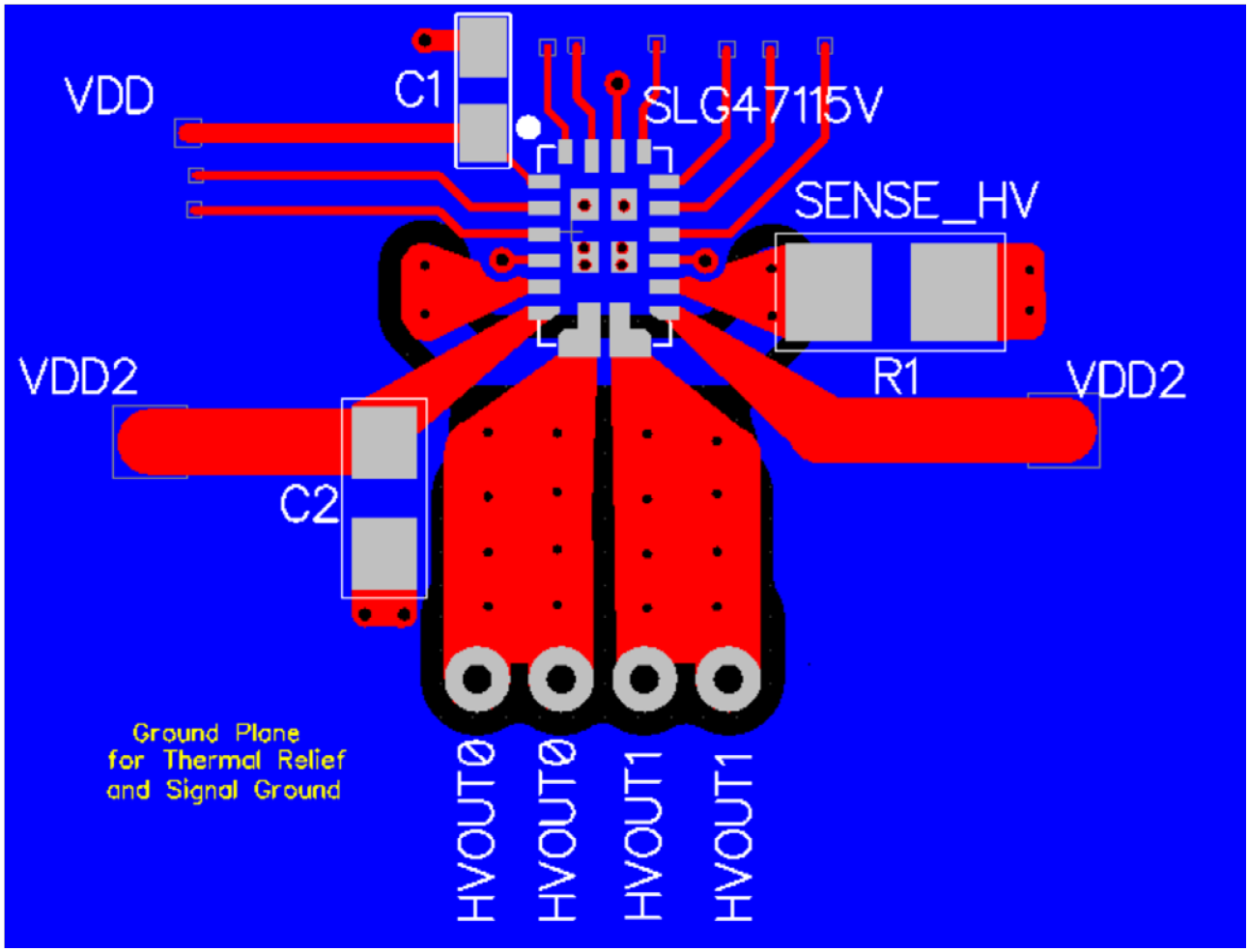
Figure 11. Die Temperature when HV OUTs are Active

11. Layout Consideration

PCB should have enough ground plane to dissipate heat. SLG7MD47679 has two additional pads, which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.

The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters.

11.1 PCB Layout Example

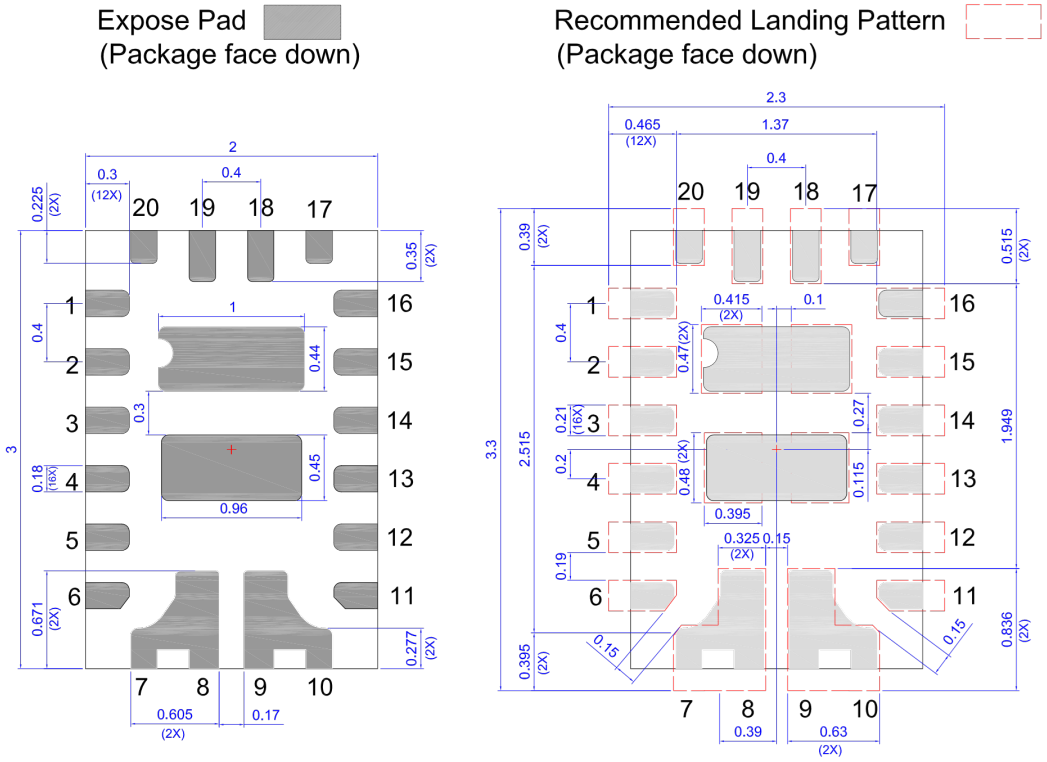


12. Layout Guidelines

12.1 STQFN 20L 2.0 mm x 3.0 mm x 0.55 mm 0.4P FCD Package

It is highly recommended to place low-ESR capacitor between V_{DD2} and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it is highly recommended to place 0.1 µF ceramic capacitor between V_{DD} and GND.



12.2 Recommended Reflow Soldering Profile

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

13. Ordering Information

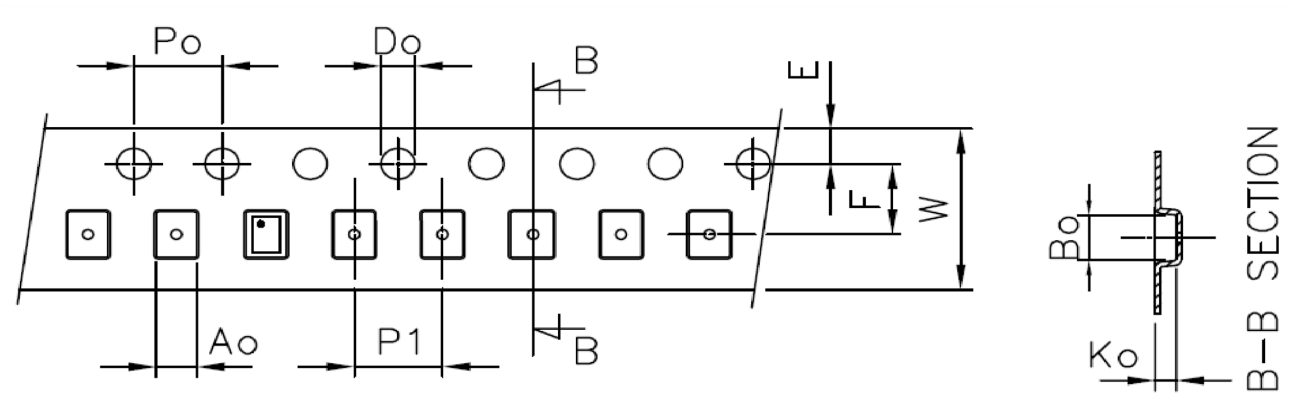
Part Number	Temperature Range
SLG7MD47679	20-pin STQFN - Tape and Reel (3k units)

13.1 Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green	20	2.0x3.0x0.55	3000	3000	178/60	100	400	100	400	8	4

13.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



14. Revision History

Revision	Date	Description
1.00	Jun 27, 2024	Initial release