



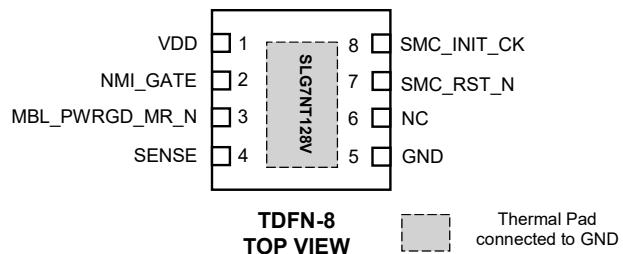
### General Description

Renesas SLG7NT128V is a low power and small form device. The SoC is housed in a 2mm x 2mm TDFN package which is optimal for using with small devices.

### Features

- Low Power Consumption
- 3.3V Supply
- Pb-Free / RoHS Compliant
- Halogen-Free
- TDFN-8 Package

### Pin Configuration



### Output Summary

- 2 Outputs – Open Drain

**Pin Configuration**

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	3.3V Supply Voltage
2	NMI_GATE	Input	Digital Input
3	MBL_PWRGD_MR_N	Input	Digital Input
4	SENSE	Input	Analog input
5	GND	GND	Ground
6	NC	--	Connect to GND or keep floating
7	SMC_RST_N	Output	Open Drain
8	SMC_INIT_CK	Output	Open Drain
Exposed Bottom Pad	GND	GND	Ground

**Ordering Options & Configuration**

Part Number	Package Type
SLG7NT128V	V = TDFN-8
SLG7NT128VTR	VTR = TDFN-8 – Tape and Reel (3k units)

**Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
$V_{DD}$ to GND	-0.3	4.6	V
Voltage at input pins	-0.3	4.6	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

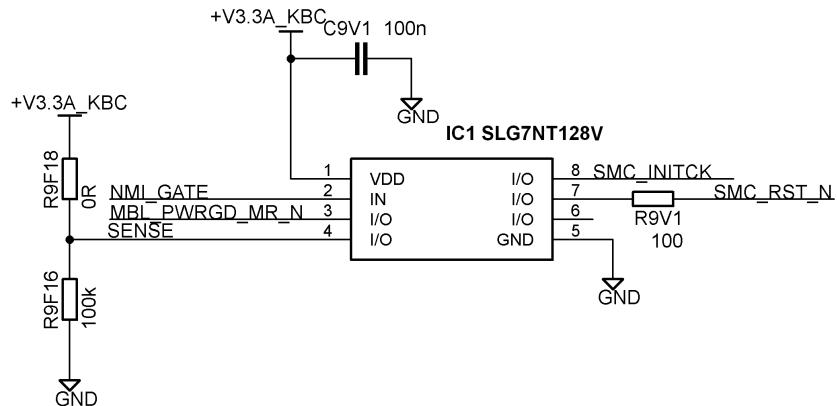
**Electrical Characteristics**

Symbol	Parameter	Condition / Note	Min	Typ	Max	Unit
$V_{DD}$	Supply Voltage		3.0	3.3	3.6	V
$I_Q$	Quiescent Current	Static Inputs and Outputs	--	30	--	µA
$T_A$	Operating temperature		-40	25	85	°C
$V_{AIR}$	Analog Input Voltage Range		0	--	2.2	V
$V_{IH}$	HIGH-Level Input Voltage	Logic Input	1.8	--	3.3	V
$I_{IH}$	HIGH-Level Input Leakage Current	Logic Input Pins; VIN=3.3V	-100	--	100	nA
$I_{IL}$	LOW-Level Input Leakage Current	Logic Input Pins; VIN=0V	-100	--	100	nA
$V_{IL}$	LOW-Level Input Voltage	Logic Input	-0.3	--	0.8	V
$V_{OL}$	LOW-Level Output Voltage	Open Drain Logic Level Outputs	0	--	0.4	V
$I_{OH}$	Low-Level Output Current	Open Drain	--	20	--	mA
$V_{REF}$	Reference voltage	Analog Comparator 0	--	400	--	mV
$V_{HYST}$	Analog Comparator hysteresis	Analog Comparator 0	--	50	--	mV
$R_{PULL\_UP}$	Internal Pull Up Resistance	Pull up on PIN7 and PIN8	80	100	120	kΩ
$T_{StUp}$	Start Up Time		--	7	--	ms

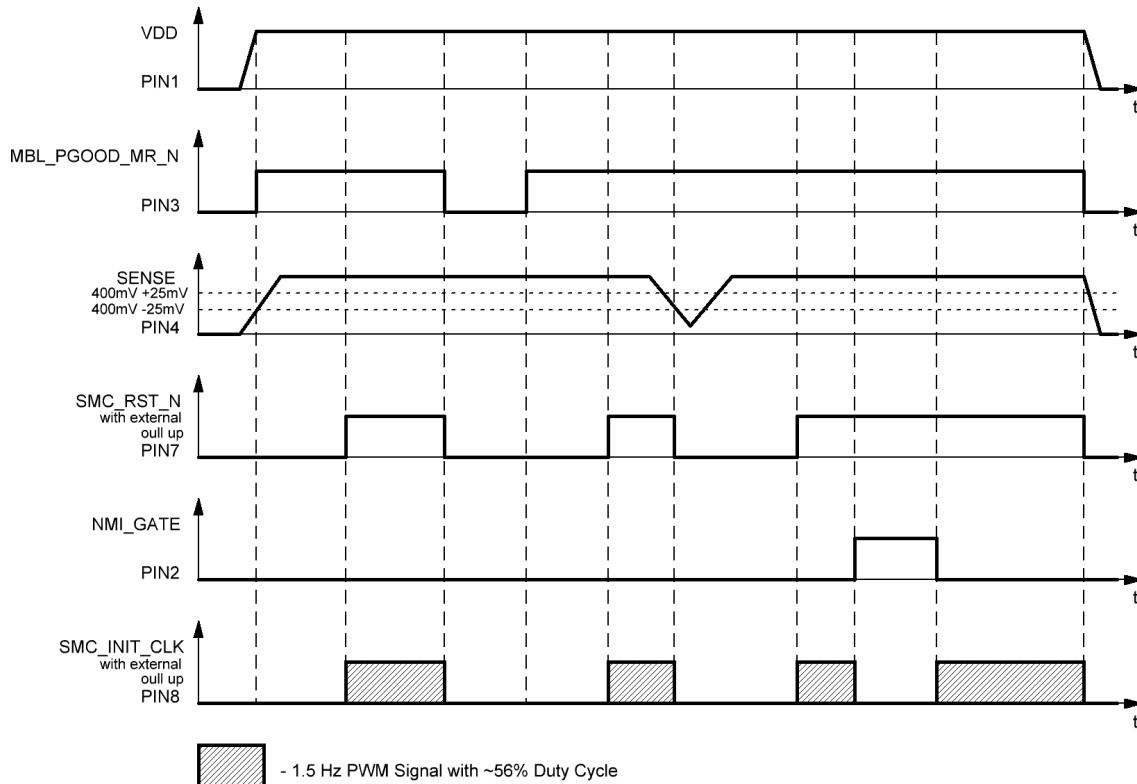
## Description

This is a special oscillator with supervisor system. Three inputs are used to control the oscillator. PIN4 controls the voltage supply of the chip. If supply voltage decreases to 2.8V, the chip disables the oscillator and sets SMC\_INICK to LOW. When voltage > 2.8V is detected on the SENSE pin, SMC\_RST\_N is set to HIGH with 20 ms delay and enables the oscillator. MBL\_PWRGD\_MR\_N is used for manual reset of SMC\_RST\_N. Use NMI\_GATE to disable the oscillator.

## Typical Application Circuit



## Timing Diagrams



### SLG7NT128V Functionality Waveforms

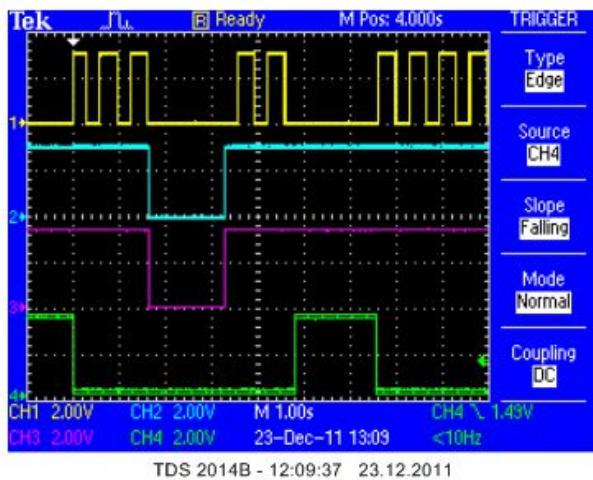
Channel 1 (yellow/top line) – Pin# 8 (SMC\_INIT\_CLK)

Channel 2 (light blue/2<sup>nd</sup> line) – Pin# 7 (SMC\_RST\_N)

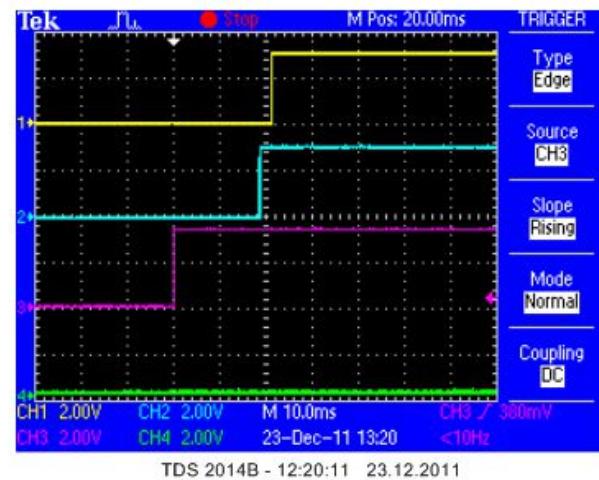
Channel 3 (magenta /3<sup>rd</sup> line) – Pin# 3 (MBL\_PGOOD\_MR)

Channel 4 (green /bottom line) – Pin# 2 (NMI\_GATE)

#### 1. OSC enable



#### 2. 20ms delay supervisor



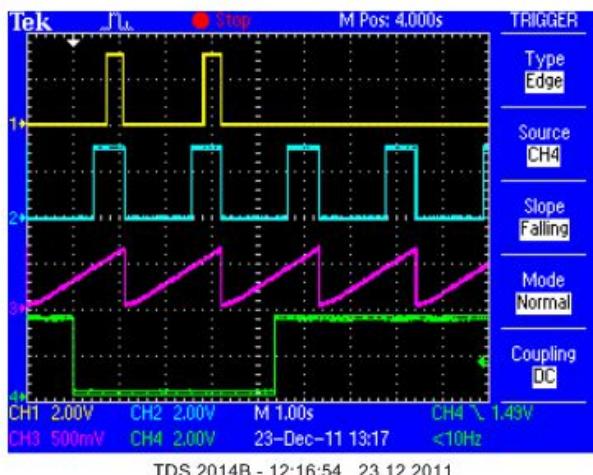
Channel 1 (yellow/top line) – pin# 8 (SMC\_INIT\_CLK)

Channel 2 (light blue/2<sup>nd</sup> line) – pin# 7 (SMC\_RST\_N)

Channel 3 (magenta /3<sup>rd</sup> line) – pin# 4 (SENSE)

Channel 4 (green /bottom line) – pin# 2 (NMI\_GATE)

#### 3. Power voltage detect



### Package Top Marking

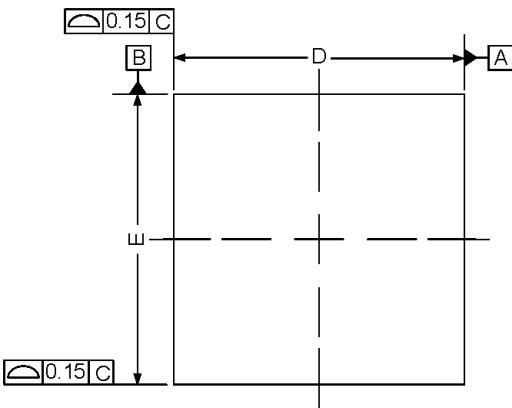
Part Code	<u>XX</u> <u>A</u>	Assembly Code
Date Code	<u>DD</u> <u>L</u>	Lot
	<u>R</u> o	Revision

XX – Part Code Field: identifies the specific device configuration  
A – Assembly Code Field: Assembly Location of the device.  
DD – Date Code Field: Coded date of manufacture  
L – Lot Code: Designates Lot #  
R – Revision Code: Device Revision

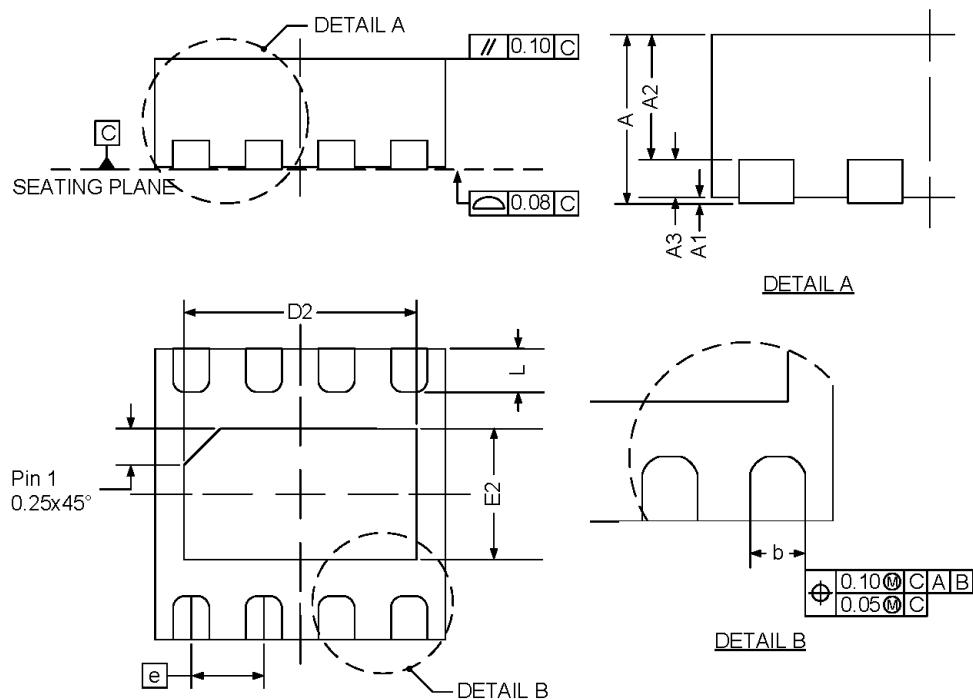
Datasheet Revision	Programming Code Number	Part Code	Revision	Date
1.01	01	KN	A	02/25/2022

## Package Drawing and Dimensions

## TDFN-8 Package



Symbol	Min (mm)	NOM (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	--	0.05
A2	--	0.55	--
A3	--	0.20	--
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.50 BSC		
L	0.20	0.30	0.40

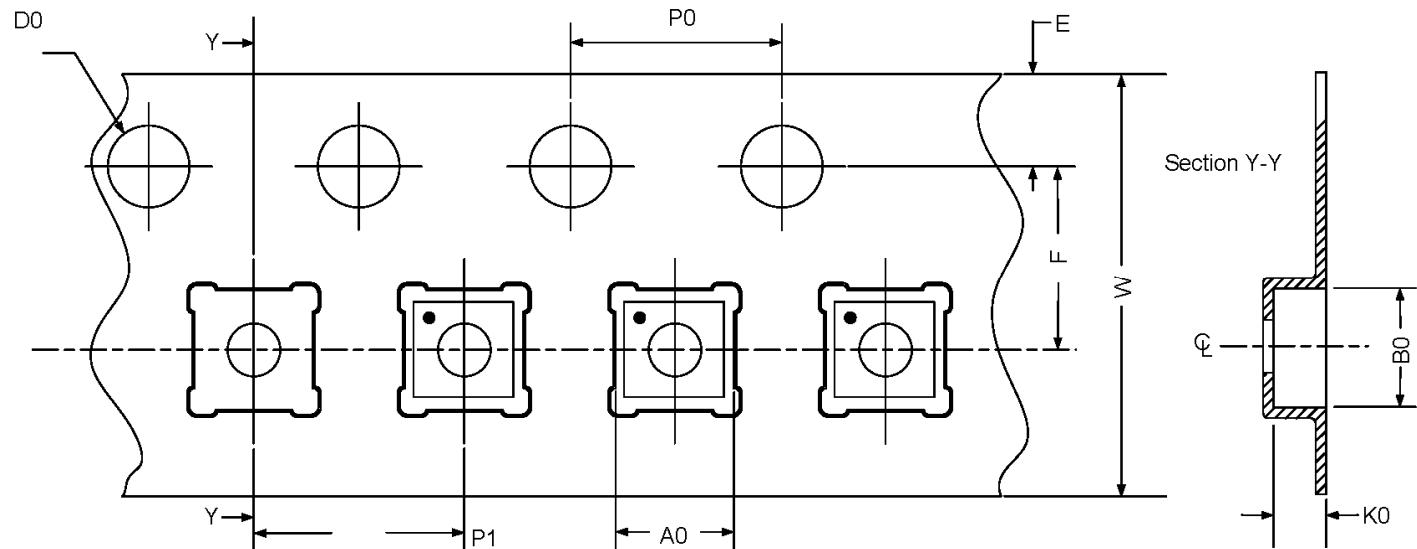


## Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 8L 2x2mm Green	8	2x2x0.75	3000	3000	178/60	42	168	42	168	8	4

## Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L 2x2mm Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

**Datasheet Revision History**

<b>Date</b>	<b>Version</b>	<b>Change</b>
02/08/2012	0.1	New Design
06/05/2012	0.11	Changed name of design to “1Hz Interrupt Generator”
03/08/2013	0.12	Updated Device Revision Table
03/18/2013	0.13	Corrected Timing Diagrams
03/25/2013	0.14	Updated Device Revision Table
03/29/2013	1.0	Production Release
02/25/2022	1.01	Updated Company name and logo

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