

General Description

Renesas SLG7RN45323 is a low power and small form device. The SoC is housed in a 1.6mm x 1.6mm STQFN package which is optimal for using with small devices.

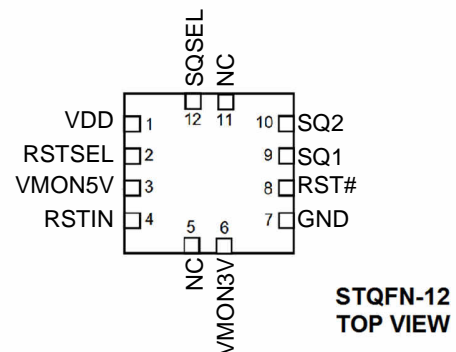
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

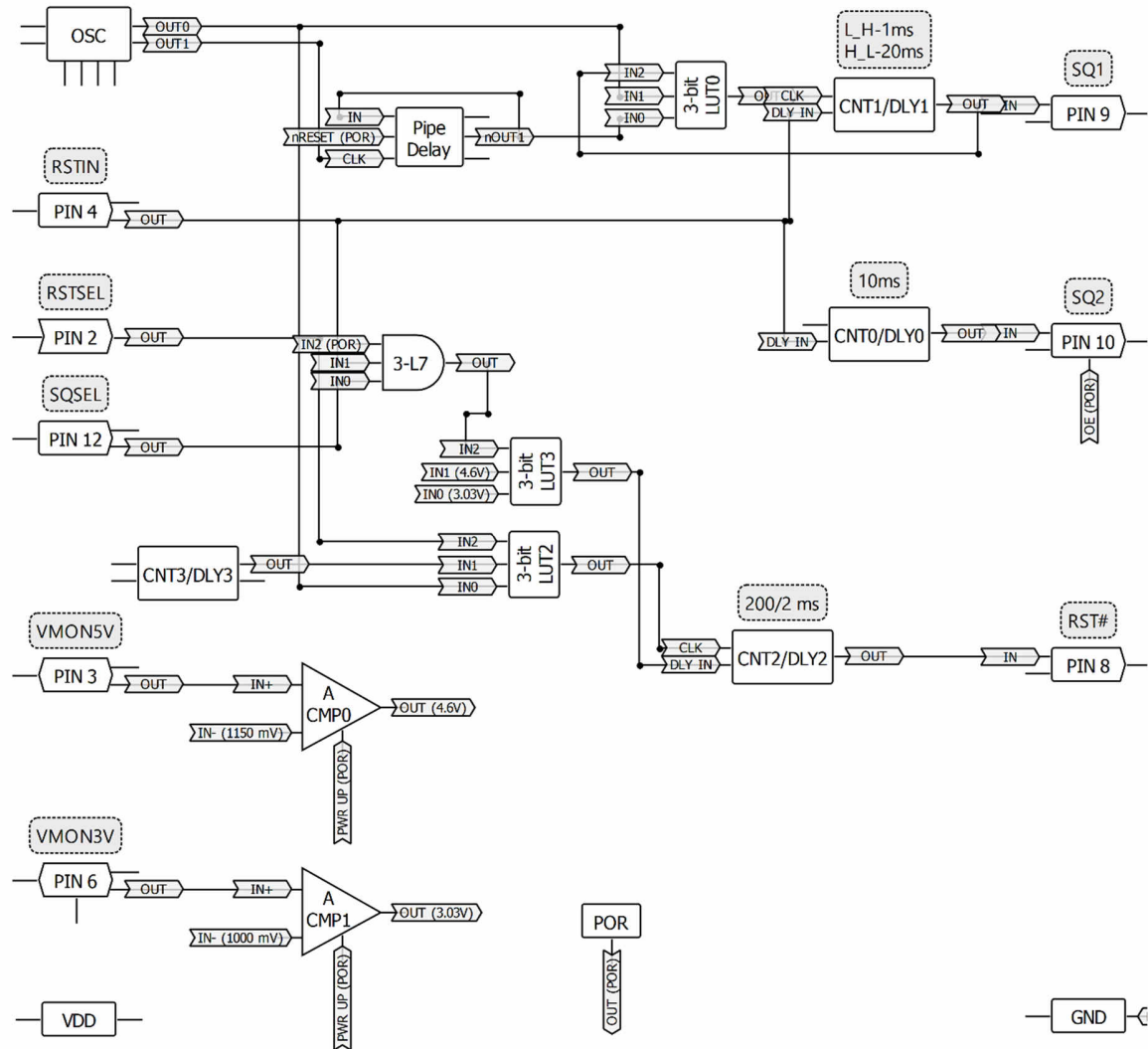
Output Summary

1 Output - Open Drain NMOS 1X
2 Outputs - Push Pull 1X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	RSTSEL	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	VMON5V	Analog Input/Output	Analog Input/Output	floating
4	RSTIN	Digital Input	Digital Input with Schmitt trigger	10kΩ pullup
5	NC	--	Keep Floating or Connect to GND	--
6	VMON3V	Analog Input/Output	Analog Input/Output	floating
7	GND	GND	Ground	--
8	RST#	Digital Output	Open Drain NMOS 1X	floating
9	SQ1	Digital Output	Push Pull 1X	floating
10	SQ2	Digital Output	Push Pull 1X	floating
11	NC	--	Keep Floating or Connect to GND	--
12	SQSEL	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown

Ordering Information

Part Number	Package Type
SLG7RN45323V	STQFN-12 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD relative to GND	-0.5	7	V
DC Input Voltage	GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	12	mA
	OD 1x	18	
Current at Input Pin	-1.0	1.0	mA
Input leakage (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

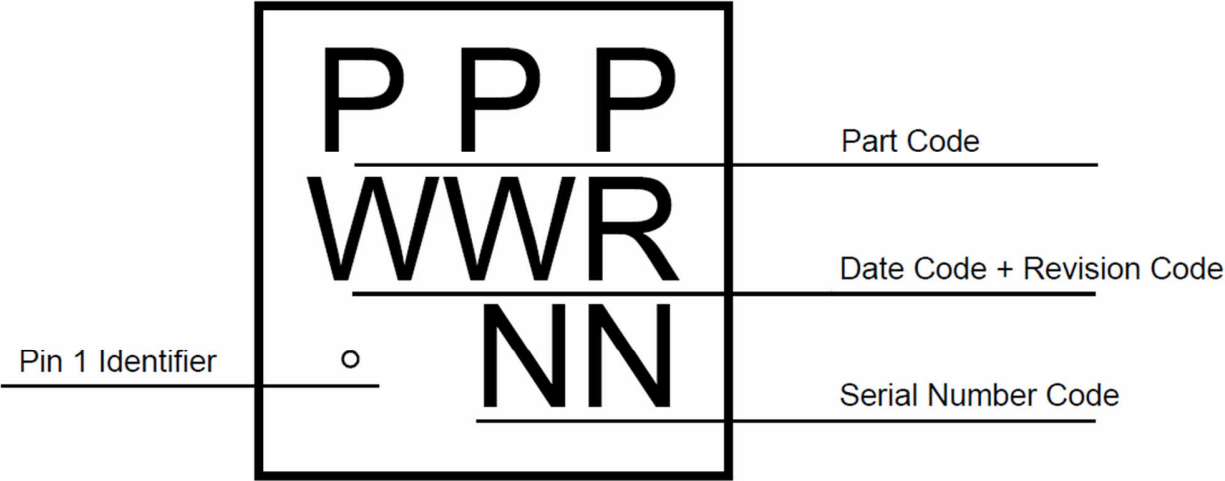
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		1.71	5	5.5	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	Static inputs and floating outputs	--	76	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	73	mA
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 110°C	--	--	35	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	92	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 110°C	--	--	44	mA
V _{IH}	HIGH-Level Input Voltage	Logic Input at VDD=1.8V	1.100	--	VDD	V
		Logic Input at VDD=3.3V	1.780	--	VDD	V
		Logic Input at VDD=5.0V	2.640	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=1.8V	1.270	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=3.3V	2.130	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=5.0V	3.160	--	VDD	V
V _{IL}	LOW-Level Input Voltage	Logic Input at VDD=1.8V	0	--	0.690	V
		Logic Input at VDD=3.3V	0	--	1.210	V
		Logic Input at VDD=5.0V	0	--	1.840	V

		Logic Input with Schmitt Trigger at VDD=1.8V	0	--	0.440	V
		Logic Input with Schmitt Trigger at VDD=3.3V	0	--	0.950	V
		Logic Input with Schmitt Trigger at VDD=5.0V	0	--	1.510	V
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I _{OH} =100μA, at VDD=1.8V	1.680	1.790	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I _{OH} =3mA, at VDD=3.3V	2.720	3.090	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I _{OH} =5mA, at VDD=5.0V	4.170	4.740	--	V
V _{OL}	LOW-Level Output Voltage	Push-Pull 1X, I _{OL} =100μA, at VDD=1.8V	--	0.020	0.030	V
		Push-Pull 1X, I _{OL} =3mA, at VDD=3.3V	--	0.180	0.280	V
		Push-Pull 1X, I _{OL} =5mA, at VDD=5.0V	--	0.230	0.330	V
		Open Drain NMOS 1X, I _{OL} =100μA, at VDD=1.8V	--	0.010	0.020	V
		Open Drain NMOS 1X, I _{OL} =3mA, at VDD=3.3V	--	0.090	0.130	V
		Open Drain NMOS 1X, I _{OL} =5mA, at VDD=5.0V	--	0.120	0.160	V
I _{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V _{OH} =VDD-0.2V, at VDD=1.8V	1.000	1.390	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V _{OH} =2.4V, at VDD=3.3V	6.010	10.150	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V _{OH} =2.4V, at VDD=5.0V	21.980	29.001	--	mA
I _{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V _{OL} =0.15V, at VDD=1.8V	0.760	1.340	--	mA
		Push-Pull 1X, V _{OL} =0.4V, at VDD=3.3V	4.060	6.440	--	mA
		Push-Pull 1X, V _{OL} =0.4V, at VDD=5.0V	6.010	9.730	--	mA
		Open Drain NMOS 1X, V _{OL} =0.15V, at VDD=1.8V	1.530	2.670	--	mA
		Open Drain NMOS 1X, V _{OL} =0.4V, at VDD=3.3V	8.130	12.410	--	mA
		Open Drain NMOS 1X, V _{OL} =0.4V, at VDD=5.0V	11.760	19.460	--	mA
R _{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 4	--	10	--	kΩ
R _{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 12	--	1	--	MΩ
T _{DLY0}	Delay0 Time	At temperature 25°C	9.22	10	10.69	ms

		At temperature -40 +85°C (Note 3)	8.62	10	12.65	ms
T _{CNT3}	Counter3 Period	At temperature 25°C	7.26	7.84	8.35	ms
		At temperature -40 +85°C (Note 3)	6.78	7.84	9.88	ms
V _{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	4400	--	4793	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	4250	--	4859	mV
		High to Low transition, at temperature 25°C	4399	--	4792	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	4248	--	4857	mV
V _{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	2855	--	3130	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	2763	--	3175	mV
		High to Low transition, at temperature 25°C	2854	--	3129	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2760	--	3174	mV
T _{SU}	Startup Time	From VDD rising past 1.35 V	--	0.31	--	ms
PON _{THR}	Power On Threshold	V _{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
POFF _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
Note: 1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions. 2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10, 11 and 12 to another. 3. Guaranteed by Design.						

Package Top Marking

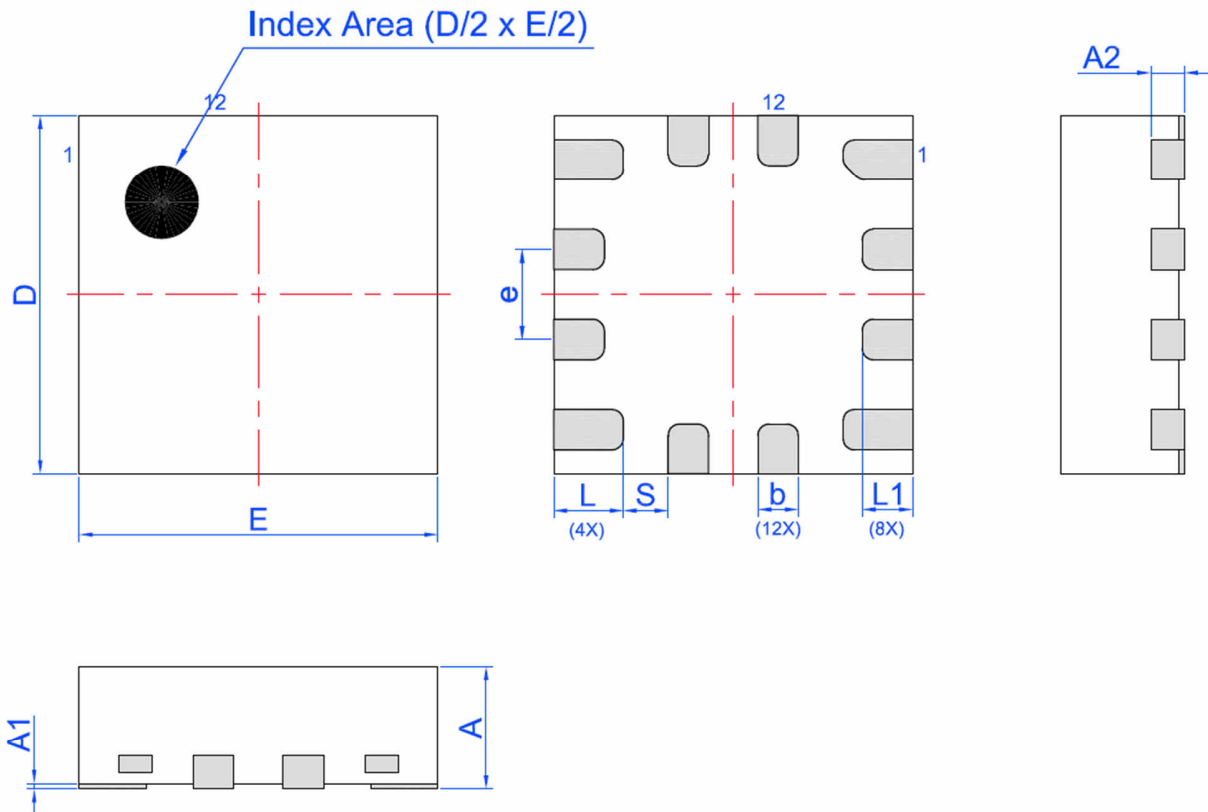


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0x85F199C6			07/11/2023

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

12 Lead STQFN FCA Package 1.6 x 1.6 mm



Unit: mm

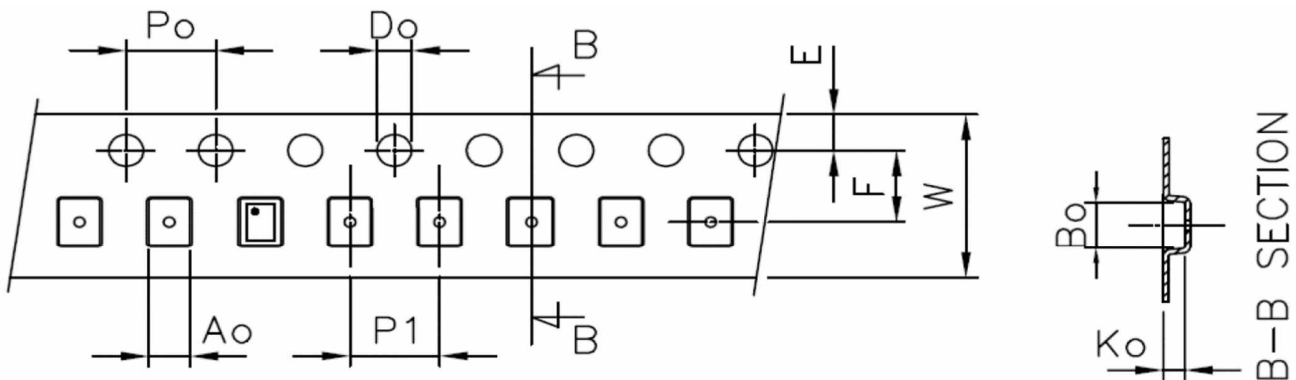
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FCA 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FCA 0.4P Green	1.80±0.05	1.80±0.05	±0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

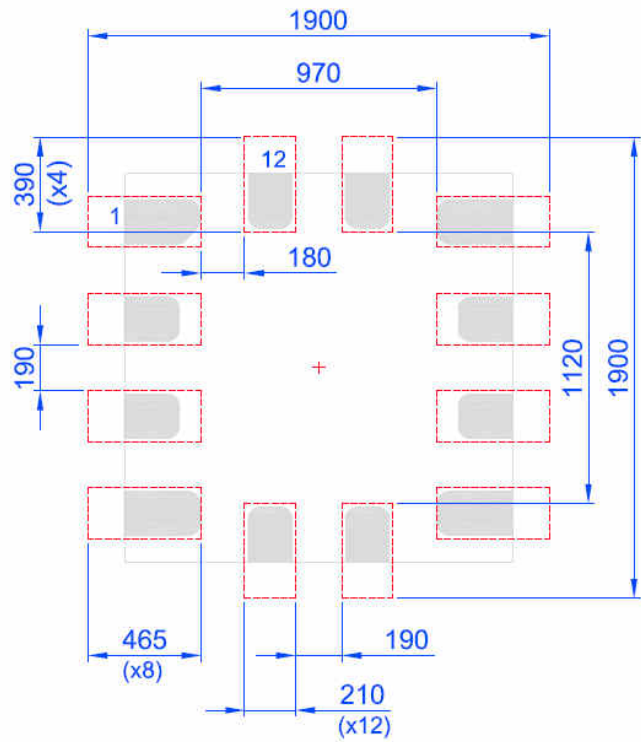
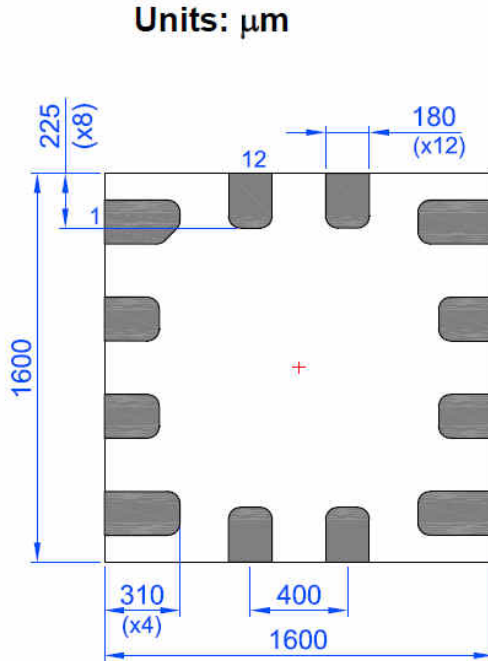
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm³ (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

 Exposed Pad
(PKG face down)

 Recommended Land Pattern
(PKG face down)

Units: μm



Datasheet Revision History

Date	Version	Change
10/21/2021	0.10	New design
07/11/2023	0.11	Moved to Renesas template

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.