

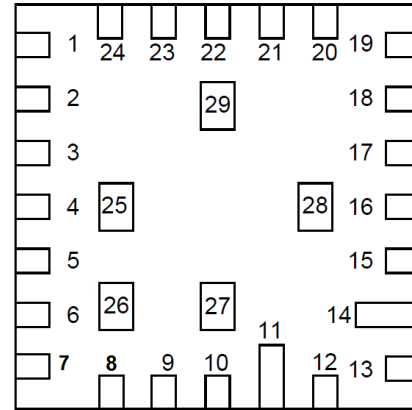
General Description

Renesas SLG7RN46112 is a low power and small form device. The SoC is housed in a 3mm x 3mm MSTQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- MSTQFN - 29 Package

Pin Configuration

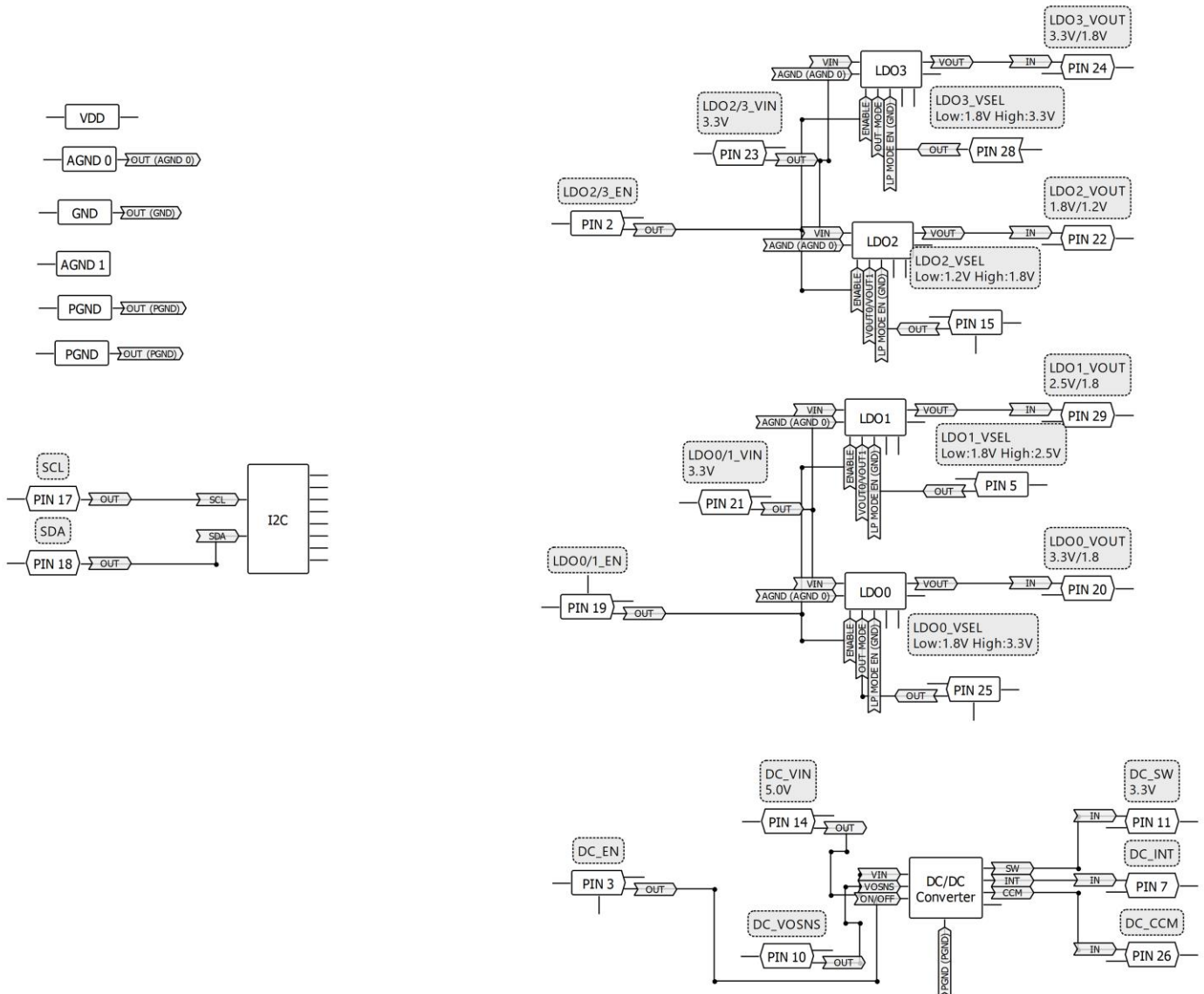


MSTQFN-29 (Top View)

Pin name

| Pin # | Pin name | Pin # | Pin name |
|-------|------------------------------|-------|------------------------------|
| 1 | AGND | 16 | VDD |
| 2 | LDO2/3_EN | 17 | SCL |
| 3 | DC_EN | 18 | SDA |
| 4 | GND | 19 | LDO0/1_EN |
| 5 | LDO1_VSEL Low:1.8V High:2.5V | 20 | LDO0_VOUT 3.3V/1.8 |
| 6 | AGND | 21 | LDO0/1_VIN 3.3V |
| 7 | DC_INT | 22 | LDO2_VOUT 1.8V/1.2V |
| 8 | NC | 23 | LDO2/3_VIN 3.3V |
| 9 | NC | 24 | LDO3_VOUT 3.3V/1.8V |
| 10 | DC_VOSNS | 25 | LDO0_VSEL Low:1.8V High:3.3V |
| 11 | DC_SW 3.3V | 26 | DC_CCM |
| 12 | PGND | 27 | NC |
| 13 | PGND | 28 | LDO3_VSEL Low:1.8V High:3.3V |
| 14 | DC_VIN 5.0V | 29 | LDO1_VOUT 2.5V/1.8 |
| 15 | LDO2_VSEL Low:1.2V High:1.8V | | |

Block Diagram



Pin Configuration

| Pin # | Pin Name | Type | Pin Description | Internal Resistor |
|-------|---------------------------------|---------------------|---------------------------------|-------------------|
| 1 | AGND | AGND | Ground | -- |
| 2 | LDO2/3_EN | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 3 | DC_EN | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 4 | GND | GND | Ground | -- |
| 5 | LDO1_VSEL Low:1.8V High:2.5V | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 6 | AGND | AGND | Ground | -- |
| 7 | DC_INT | Analog Input/Output | DC INT Analog Input/Output | floating |
| 8 | NC | -- | Keep Floating or Connect to GND | -- |
| 9 | NC | -- | Keep Floating or Connect to GND | -- |
| 10 | DC_VOSNS | Analog Input/Output | DC VOSNS Analog Input/Output | floating |
| 11 | DC_SW 3.3V | Analog Input/Output | DC SW Analog Input/Output | floating |
| 12 | PGND | PGND | Ground | -- |
| 13 | PGND | PGND | Ground | -- |
| 14 | DC_VIN 5.0V | Analog Input/Output | DC VIN Analog Input/Output | floating |
| 15 | LDO2_VSEL Low:1.2V High:1.8V | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 16 | VDD | PWR | Supply Voltage | -- |
| 17 | SCL | Digital Input | Low Voltage Digital Input | floating |
| 18 | SDA | Digital Input | Low Voltage Digital Input | floating |
| 19 | LDO0/1_EN | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 20 | LDO0_VOUT 3.3V/1.8 | Analog Input/Output | LDO0 VOUT Analog Output | floating |
| 21 | LDO0/1_VIN 3.3V | Analog Input/Output | LDO0/1 VIN Analog Input | floating |
| 22 | LDO2_VOUT 1.8V/1.2V | Analog Input/Output | LDO2 VOUT Analog Output | floating |
| 23 | LDO2/3_VIN 3.3V | Analog Input/Output | LDO2/3 VIN Analog Input | floating |
| 24 | LDO3_VOUT 3.3V/1.8V | Analog Input/Output | LDO3 VOUT Analog Output | floating |
| 25 | LDO0_VSEL Low:1.8V High:3.3V | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 26 | DC_CCM | Analog Input/Output | DC CCM Analog Input/Output | floating |
| 27 | NC | -- | Keep Floating or Connect to GND | -- |
| 28 | LDO3_VSEL Low:1.8V High:3.3V | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 29 | LDO1_VOUT 2.5V/1.8 | Analog Input/Output | LDO1 VOUT Analog Output | floating |

Ordering Information

| Part Number | Package Type |
|----------------|--|
| SLG7RN46112M | 29-pin MSTQFN |
| SLG7RN46112MTR | 29-pin MSTQFN - Tape and Reel (3k units) |

Absolute Maximum Conditions

| Parameter | Min. | Max. | Unit |
|---------------------------------------|------------|------------|------|
| Supply Voltage on VDD relative to GND | -0.3 | 7 | V |
| DC Input Voltage | GND - 0.5V | VDD + 0.5V | V |
| Current at Input Pin | -1.0 | 1.0 | mA |
| Input leakage (Absolute Value) | -- | 1000 | nA |
| Storage Temperature Range | -65 | 150 | °C |
| Junction Temperature | -- | 150 | °C |
| ESD Protection (Human Body Model) | 2000 | -- | V |
| ESD Protection (Charged Device Model) | 1300 | -- | V |
| Moisture Sensitivity Level | 1 | | |

Electrical Characteristics

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|------------------------|---|---|---------|------|---------|------|
| V _{DD} | Supply Voltage (Note 2) | | 2.5 | 3.3 | 5 | V |
| T _A | Operating Temperature | | 15 | 25 | 30 | °C |
| C _{VDD} | Capacitor Value at VDD | | -- | 0.1 | -- | µF |
| C _{IN} | Input Capacitance | | -- | 4 | -- | pF |
| I _Q | Quiescent Current | Static inputs and floating outputs | -- | 17 | -- | µA |
| V _O | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | VDD+0.3 | V |
| I _{VDD} | Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 73 | mA |
| | | T _J = 110°C | -- | -- | 35 | mA |
| I _{GND} | Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 152 | mA |
| | | T _J = 110°C | -- | -- | 72 | mA |
| V _{IH} | HIGH-Level Input Voltage | Low-Level Logic Input | 1.25 | -- | VDD+0.3 | V |
| V _{IL} | LOW-Level Input Voltage | Low-Level Logic Input | GND-0.3 | -- | 0.5 | V |
| R _{PULL_DOWN} | Internal Pull Down Resistance | Pull down on PINs 2, 3, 5, 15, 19, 25, 28 | -- | 1 | -- | MΩ |
| T _{SU} | Startup Time | From VDD rising past P _{ON} THR | -- | 1.3 | -- | ms |
| P _{ON} THR | Power On Threshold | V _{DD} Level Required to Start Up the Chip | 1.34 | 1.55 | 1.74 | V |
| P _{OFF} THR | Power Off Threshold | V _{DD} Level Required to Switch Off the Chip | 1.05 | 1.25 | 1.45 | V |

Note:

- DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
- The GreenPAK's power rails are divided in two sides. PINs 2, 5, 15, 19, 25 and 28 are connected to one side, PINs 3, 17 and 18 to another.
- Guaranteed by Design.

I²C Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|-------------------|------------------------|---------------------------------|------|------|------|------|
| F _{SCL} | Clock Frequency, SCL | V _{DD} = (2.3...5.5) V | -- | -- | 400 | kHz |
| t _{LOW} | Clock Pulse Width Low | V _{DD} = (2.3...5.5) V | 1300 | -- | -- | ns |
| t _{HIGH} | Clock Pulse Width High | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |

| | | | | | | |
|---------------------|---|---------------------------------|------|----|-----|----|
| t _i | Input Filter Spike Suppression (SCL, SDA) | V _{DD} = 2.5V ± 8% | -- | -- | 95 | ns |
| | | V _{DD} = 3.3V ± 10% | -- | -- | 95 | ns |
| | | V _{DD} = 5.0V ± 10% | -- | -- | 111 | ns |
| t _{AA} | Clock Low to Data Out Valid | V _{DD} = (2.3...5.5) V | -- | -- | 900 | ns |
| t _{BUF} | Bus Free Time between Stop and Start | V _{DD} = (2.3...5.5) V | 1300 | -- | -- | ns |
| t _{HD_STA} | Start Hold Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{SU_STA} | Start Set-up Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{HD_DAT} | Data Hold Time | V _{DD} = (2.3...5.5) V | 0 | -- | -- | ns |
| t _{SU_DAT} | Data Set-up Time | V _{DD} = (2.3...5.5) V | 100 | -- | -- | ns |
| t _R | Inputs Rise Time | V _{DD} = (2.3...5.5) V | -- | -- | 300 | ns |
| t _F | Inputs Fall Time | V _{DD} = (2.3...5.5) V | -- | -- | 300 | ns |
| t _{SU_STO} | Stop Set-up Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{DH} | Data Out Hold Time | V _{DD} = (2.3...5.5) V | 50 | -- | -- | ns |

DC/DC Converter Electrical Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|--|------|------|------|------|
| Typical values are at T _A = 25°C | | | | | | |
| V _{IN} | Operating Input Voltage | | 2.7 | -- | 5.5 | V |
| I _{DD} | Power Supply Current | when OFF | -- | 0.17 | -- | μA |
| | | when ON, No load | -- | 79 | -- | μA |
| V _{OUT} | Output Voltage | sel_vo [2:0] = 000; V _{IN} = 2.7 to 5.5 V | 1.16 | 1.20 | 1.24 | V |
| | | sel_vo [2:0] = 001; V _{IN} = 2.7 to 5.5 V | 1.46 | 1.50 | 1.55 | V |
| | | sel_vo [2:0] = 010; V _{IN} = 2.7 to 5.5 V | 1.75 | 1.80 | 1.85 | V |
| | | sel_vo [2:0] = 011; V _{IN} = 3.0 to 5.5 V | 1.94 | 2.50 | 2.06 | V |
| | | sel_vo [2:0] = 100; V _{IN} = 3.5 to 5.5 V | 2.53 | 3.00 | 2.58 | V |
| | | sel_vo [2:0] = 101; V _{IN} = 3.8 to 5.5 V | 3.20 | 3.30 | 3.40 | V |
| V _{RIPPLE} | Output Voltage Ripple | V _{IN} =3.3V; V _{OUT} =1.2V; in CCM Mode | -- | 10 | -- | mV |
| R _{DS(ON)_P} | HS Switch ON Resistance | | -- | 90 | -- | mΩ |
| R _{DS(ON)_N} | LS Switch ON Resistance | | -- | 51 | -- | mΩ |
| I _{LIMIT} | Current Limit Threshold | Default sel_ocp<1:0> = 00 | -- | 2.5 | -- | A |
| η _{EF} | Efficiency | V _{IN} =5V, V _{OUT} =1.2V; I _{LOAD} =0.5A; Temp=27°C, f _{SW} =1.5MHz; Inductor DCR=10mΩ | -- | 88 | -- | % |
| f _{SW} | Switching Frequency | Default sel_fsw<1:0> = 00 | -- | 1.5 | -- | MHz |
| | | Default sel_fsw<1:0> = 01 | -- | 2 | -- | MHz |
| T _{Total_ON} | Total Turn-on Time from Enable to DC_VOUT | | -- | 0.6 | -- | ms |
| T _{SS} | Soft Start Time | | -- | 0.5 | -- | ms |
| DC _{MAX} | Maximum Duty Cycle | V _{OUT} =3.3V, f _{SW} =1.5MHz | -- | 85 | -- | % |
| | | V _{OUT} =3.3V, f _{SW} =2.0MHz | -- | 80 | -- | % |
| DC _{MIN} | Minimum Duty Cycle | | -- | 20 | -- | % |

| | | | | | | |
|-----------------|---|---|-----|-----|-----|-------------|
| $I_{SW(LKG)}$ | SW Leakage Current | Set on/off=0, $V_{IN}=5.5V$, $V_{SW}=0V$ and $5.5V$ | -- | 0 | -- | μA |
| $T_{INT(Low)}$ | INT De-assertion Time | $V_{IN}=3.3V$, Temp= $27^{\circ}C$ | -- | 60 | -- | ns |
| $T_{INT(High)}$ | INT Assertion Time | $V_{IN}=3.3V$, Temp= $27^{\circ}C$ | -- | 2 | -- | μs |
| $V_{UVLO(TH)}$ | Undervoltage Lockout Threshold Voltage | Low to High Transition | TBD | TBD | TBD | V |
| | | High to Low Transition | TBD | TBD | TBD | V |
| $THERM_{ON}$ | Thermal Protection Restart Threshold | | -- | 125 | -- | $^{\circ}C$ |
| $THERM_{OFF}$ | Thermal Protection Shutdown Threshold | | -- | 100 | -- | $^{\circ}C$ |

Note:

1. INT Interrupt is an open-drain output. Logic high level becomes asserted within $T_{INT(HIGH)}$ when an over-current condition has been detected. After the over-current event no longer persist the INT becomes de-asserted after $T_{INT(LOW)}$.
2. CCM - Continuous Conduction Mode Indicator Output. CCM is an open-drain digital output that becomes Low when the load is high and the converter switches to the continuous conduction mode (CCM). The CCM output continues to toggle when the converter is in non-CCM mode. Customers might use LP filter to convert the toggling signal to a DC signal, and based on DC level to identify the converter operation mode.

Chip address

| HEX | BIN | DEC |
|------|---------|-----|
| 0x30 | 0110000 | 48 |

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

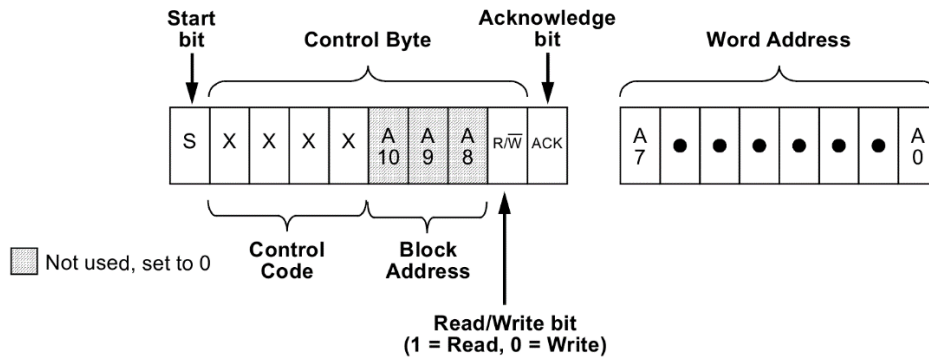


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

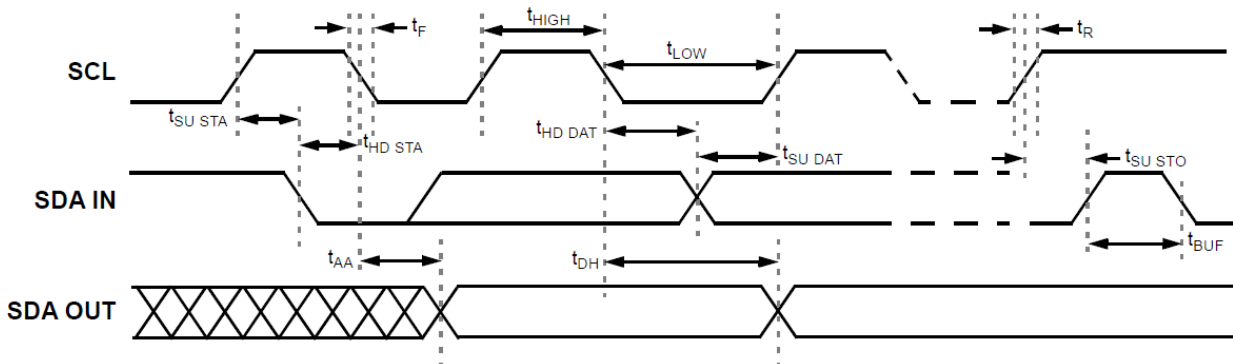


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46112 to the correct data byte to be written. After the SLG7RN46112 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46112 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46112 generates the Acknowledge bit.

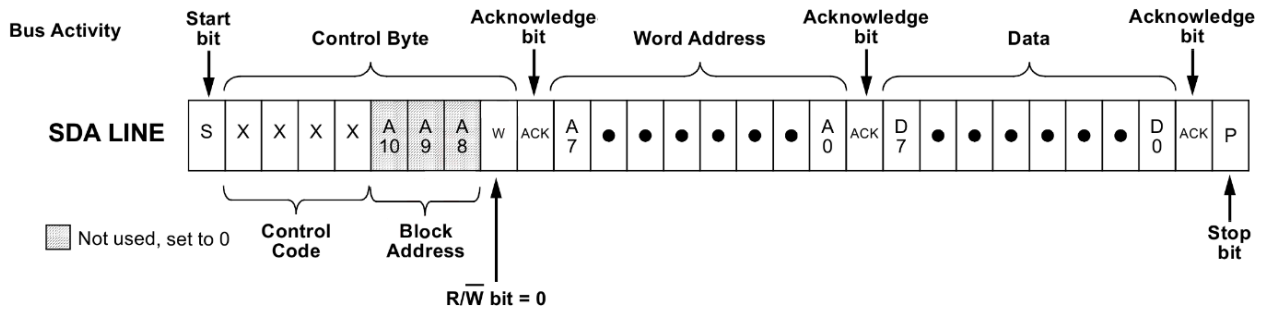


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/\bar{W} bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/\bar{W} bit set to “1”, after which the SLG7RN46112 issues an Acknowledge bit, followed by the requested eight data bits.

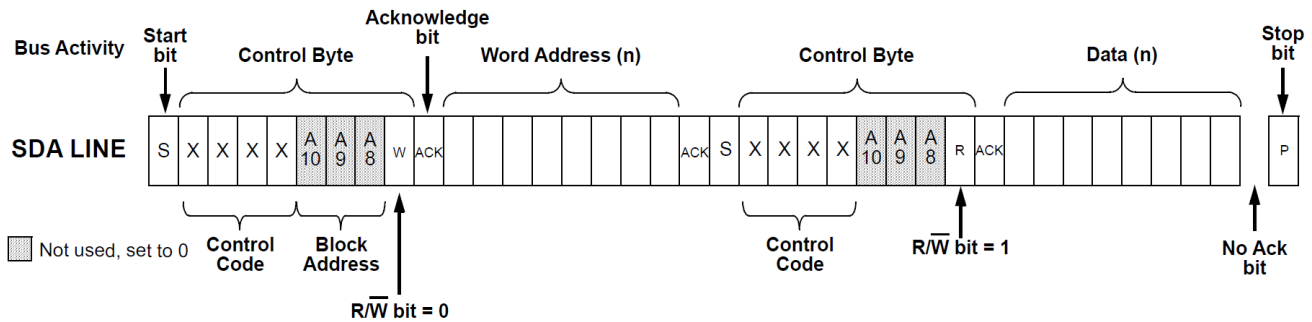
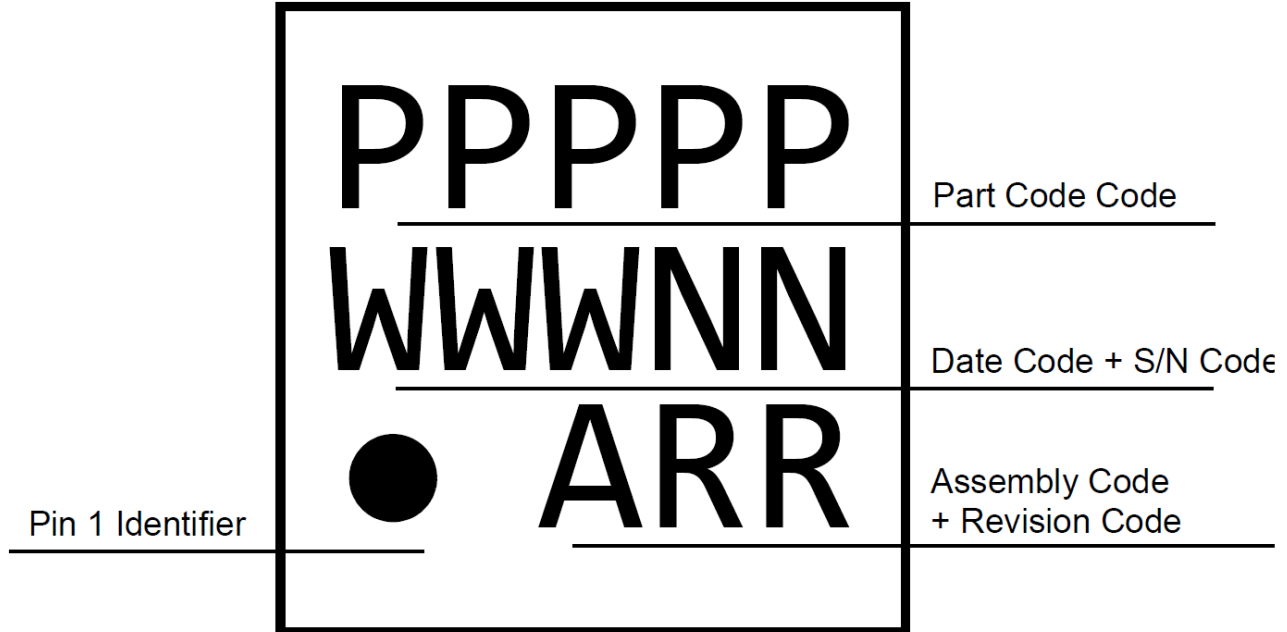


Figure4. I2C Random Read Command

Package Top Marking



| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|--------------------|-------------------------|-------------|-----------|-----------|----------|------------|
| 0.13 | 002 | U | 0x530EAC8 | 46112 | AB | 03/17/2023 |

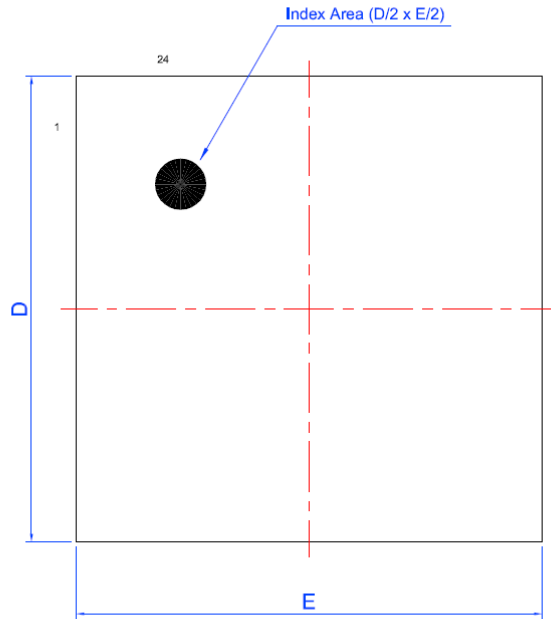
Lock coverage for this part is indicated by \checkmark , from one of the following options:

| | |
|--------------|---|
| \checkmark | Unlocked |
| | Locked for read, bits <1535:0> |
| | Locked for write, bits <1535:0> |
| | Locked for write all bits |
| | Locked for read and write bits <1535:0> |
| | Locked for read bits <1535:0> and write of all bits |

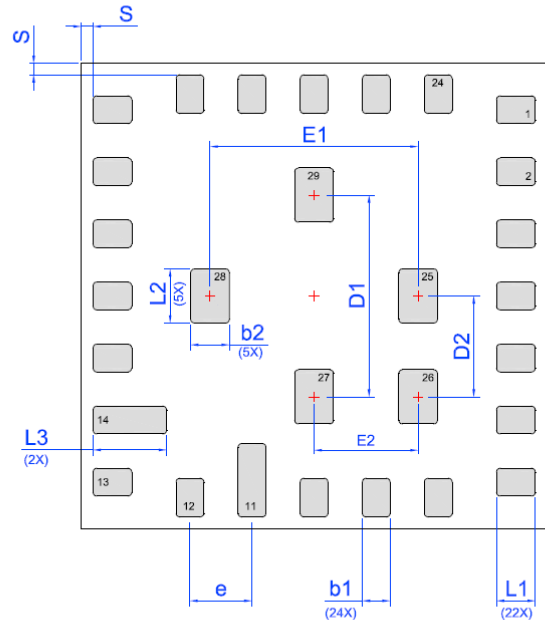
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

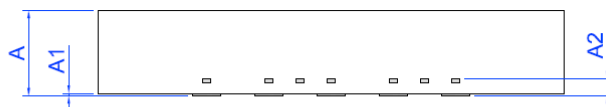
MSTQFN 29L 3x3mm 0.4P FC Package
JEDEC MO-220, Variation WECE



Laser Marking View



BTM View



Side View

UNIT: mm

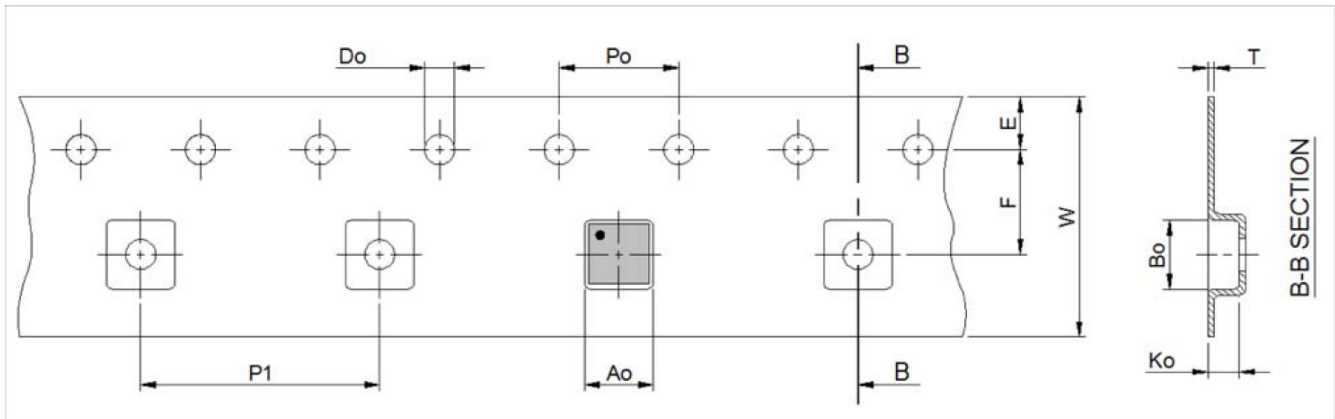
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|-----------|------|------|--------|----------|-------|-------|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.00 | - | 0.01 | E | 2.95 | 3.00 | 3.05 |
| A2 | 0.11 REF | | | e | 0.40 BSC | | |
| b1 | 0.13 | 0.18 | 0.23 | L1 | 0.20 | 0.25 | 0.30 |
| b2 | 0.20 | 0.25 | 0.30 | L2 | 0.30 | 0.35 | 0.40 |
| S | 0.075 REF | | | L3 | 0.425 | 0.475 | 0.525 |
| D1 | 1.30 BSC | | | E1 | 1.34 BSC | | |
| D2 | 0.65 BSC | | | E2 | 0.67 BSC | | |

Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| MSTQFN 29L 3x3mm 0.4P FC Green | 29 | 3 x 3 x 0.55 | 5000 | 10000 | 330 / 100 | 42 | 336 | 42 | 336 | 12 | 8 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width | Tape Thickness |
|---|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|----------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W | T |
| MSTQFN 29L 3x3mm 0.4P FC Green | 3.3 | 3.3 | 0.8 | 4 | 8 | 1.55 | 1.75 | 5.5 | 12 | 0.3 |



Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Refer to EIA-481 specification

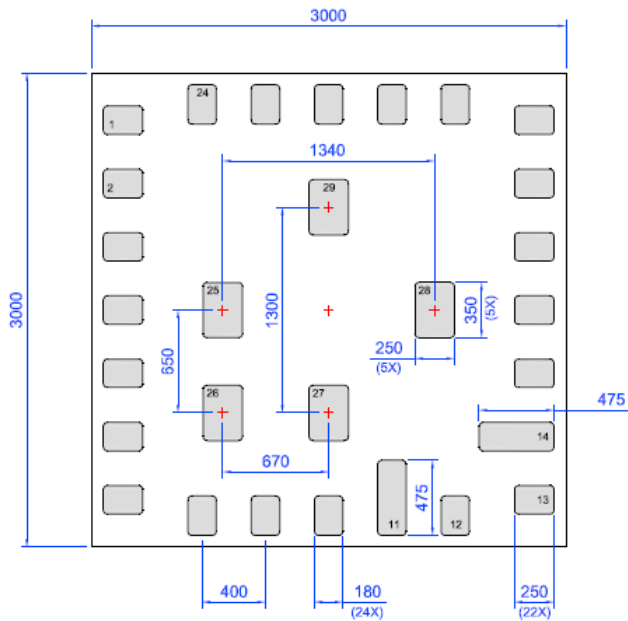
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm³ (nominal). More information can be found at www.jedec.org.

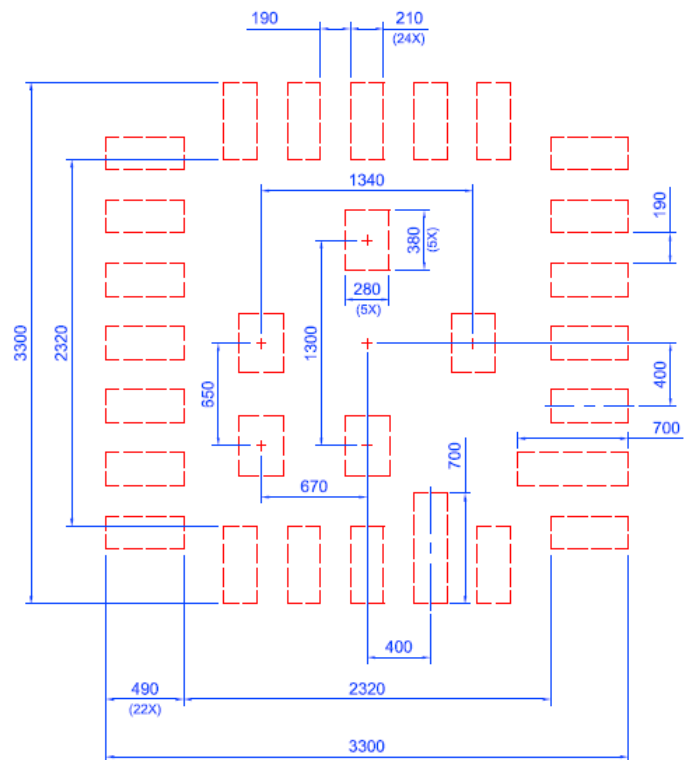
Recommended Land Pattern

 Exposed Pad
(Laser Marking view-PKG face down)

 Recommended Land Pattern
(PKG face down)



UNIT: um



Datasheet Revision History

| Date | Version | Change |
|------------|---------|-------------------------------|
| 10/28/2022 | 0.10 | New design for SLG46585M chip |
| 11/04/2022 | 0.11 | Updated Device Revision Table |
| 12/01/2022 | 0.12 | Updated the Pin name |
| 03/17/2023 | 0.13 | Updated Device Revision Table |
| | | |

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TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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