

General Description

Renesas SLG7RN46382 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

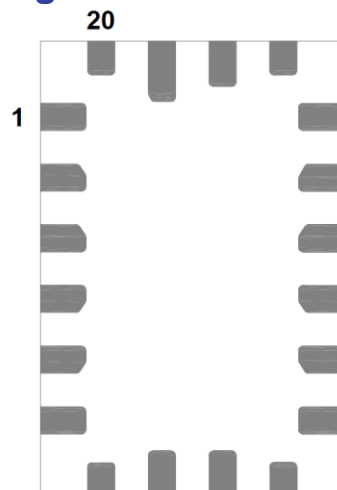
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

6 Outputs - Push Pull 2X

Pin Configuration

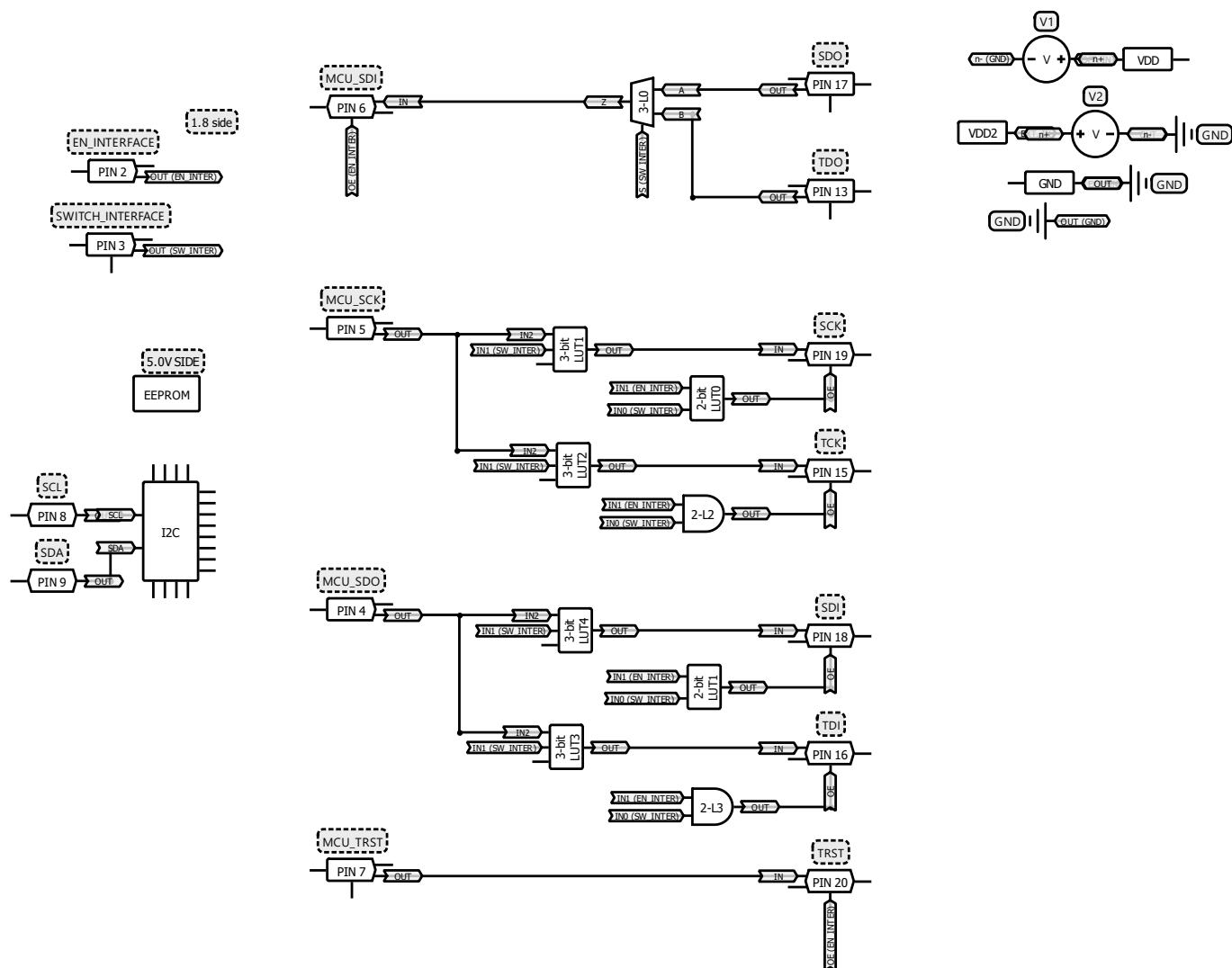


20-pin STQFN
(Top View)

Pin name

| Pin # | Pin name | Pin # | Pin name |
|-------|------------------|-------|----------|
| 1 | VDD | 11 | GND |
| 2 | EN_INTERFACE | 12 | NC |
| 3 | SWITCH_INTERFACE | 13 | TDO |
| 4 | MCU_SDO | 14 | VDD2 |
| 5 | MCU_SCK | 15 | TCK |
| 6 | MCU_SDI | 16 | TDI |
| 7 | MCU_TRST | 17 | SDO |
| 8 | SCL | 18 | SDI |
| 9 | SDA | 19 | SCK |
| 10 | NC | 20 | TRST |

Block Diagram



Pin Configuration

| Pin # | Pin Name | Type | Pin Description | Internal Resistor |
|-------|------------------|----------------|--|-------------------|
| 1 | VDD | PWR | Supply Voltage | -- |
| 2 | EN_INTERFACE | Digital Input | Digital Input without Schmitt trigger | 10kΩ pulldown |
| 3 | SWITCH_INTERFACE | Digital Input | Digital Input without Schmitt trigger | 10kΩ pulldown |
| 4 | MCU_SDO | Digital Input | Digital Input without Schmitt trigger | floating |
| 5 | MCU_SCK | Digital Input | Digital Input without Schmitt trigger | floating |
| 6 | MCU_SDI | Bi-directional | Digital Input without Schmitt trigger / Push Pull 2X | floating |
| 7 | MCU_TRST | Digital Input | Digital Input without Schmitt trigger | floating |
| 8 | SCL | Digital Input | Digital Input without Schmitt trigger | floating |
| 9 | SDA | Digital Input | Digital Input without Schmitt trigger | floating |
| 10 | NC | -- | Keep Floating or Connect to GND | -- |
| 11 | GND | GND | Ground | -- |
| 12 | NC | -- | Keep Floating or Connect to GND | -- |
| 13 | TDO | Digital Input | Digital Input without Schmitt trigger | floating |
| 14 | VDD2 | PWR | Supply Voltage | -- |
| 15 | TCK | Bi-directional | Digital Input without Schmitt trigger / Push Pull 2X | floating |
| 16 | TDI | Bi-directional | Digital Input without Schmitt trigger / Push Pull 2X | floating |
| 17 | SDO | Digital Input | Digital Input without Schmitt trigger | floating |
| 18 | SDI | Bi-directional | Digital Input without Schmitt trigger / Push Pull 2X | floating |
| 19 | SCK | Bi-directional | Digital Input without Schmitt trigger / Push Pull 2X | floating |
| 20 | TRST | Bi-directional | Digital Input without Schmitt trigger / Push Pull 2X | floating |

Ordering Information

| Part Number | Package Type |
|--------------|---|
| SLG7RN46382V | 20-pin STQFN |
| SLG7RN46382V | 20-pin STQFN - Tape and Reel (3k units) |

Absolute Maximum Conditions

| Parameter | | Min. | Max. | Unit |
|--|--------------|----------|----------|------|
| V _{HIGH} to GND | | -0.3 | 7 | V |
| Voltage at Input Pin | | GND-0.5V | VDD+0.5V | V |
| Maximum Average or DC Current Through V _{DD} Pin | | -- | 90 | mA |
| Maximum Average or DC Current Through V _{DD2} Pin | | -- | 90 | mA |
| Maximum Average or DC Current Through GND Pin (Per chip side, (Note 1)) | | -- | 100 | mA |
| Maximum Average or DC Current (Through pin) | Push-Pull 2x | -- | 22.1 | mA |
| Current at Input Pin | | -1.0 | 1.0 | mA |
| Input leakage (Absolute Value) | | -- | 1000 | nA |
| Storage Temperature Range | | -65 | 150 | °C |
| Junction Temperature | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | 2000 | -- | V |
| ESD Protection (Charged Device Model) | | 1300 | -- | V |
| Moisture Sensitivity Level | | 1 | | |

Note 1 The GreenPAK's GND rail is divided in two sides. IOs 0 to 6, SCL, SDA are connected to one side and IOs 7 to 14 are connected to another side.

Electrical Characteristics

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|------------------------|--|---|---------|------|---------|------|
| V _{DD} | Supply Voltage | | 5 | 5 | 5 | V |
| V _{DD2} | Supply Voltage | | 5 | 5 | 5 | V |
| T _A | Operating Temperature | | -40 | 25 | 85 | °C |
| C _{VDD} | Capacitor Value at VDD | | -- | 0.1 | -- | μF |
| C _{IN} | Input Capacitance | | -- | 4 | -- | pF |
| I _Q | Quiescent Current | Static inputs and floating outputs PIN8 and PIN9 are HIGH PINs 4 - 7, 13, 15 - 20 are LOW | -- | 1 | -- | μA |
| V _O | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | VDD+0.3 | V |
| V _{IH} | HIGH-Level Input Voltage | Logic Input | 0.7xVDD | -- | VDD+0.3 | V |
| V _{IL} | LOW-Level Input Voltage | Logic Input | GND-0.3 | -- | 0.3xVDD | V |
| V _{OH} | HIGH-Level Output Voltage (Note 1) | Push-Pull 2X, I _{OH} =5mA at VDD=5.0V | 4.821 | -- | -- | V |
| V _{OL} | LOW-Level Output Voltage (Note 1) | Push-Pull 2X, I _{OL} =5mA, at VDD=5.0V | -- | -- | 0.145 | V |
| I _{OH} | HIGH-Level Output Current (Note 1) | Push-Pull 2X, V _{OH} =2.4V at VDD=5.0V | 48.49 | -- | -- | mA |
| I _{OL} | LOW-Level Output Current (Note 1) | Push-Pull 2X, V _{OL} =0.4V, at VDD=5.0V | 13.52 | -- | -- | mA |
| R _{PULL_DOWN} | Internal Pull Down Resistance (Note 1) | Pull down on PINs 2, 3 | -- | 10 | -- | kΩ |
| T _{SU} | Startup Time | From VDD rising past PON _{THR} | -- | 1.66 | 2.59 | ms |
| PON _{THR} | Power On Threshold | VDD Level Required to Start Up the Chip | 1.60 | 1.85 | 2.07 | V |
| POFF _{THR} | Power Off Threshold | VDD Level Required to Switch Off the Chip | 0.97 | 1.23 | 1.46 | V |

Note:

1. PINs 1 to 10 are powered from VDD and PINs 12 to 20 are powered from VDD2.
2. Guaranteed by Design.

I²C Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---------------------|---|---------------------------------|------|------|------|------|
| F _{SCL} | Clock Frequency, SCL | V _{DD} = (2.3...5.5) V | -- | -- | 400 | kHz |
| t _{LOW} | Clock Pulse Width Low | V _{DD} = (2.3...5.5) V | 1300 | -- | -- | ns |
| t _{HIGH} | Clock Pulse Width High | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _i | Input Filter Spike Suppression (SCL, SDA) | V _{DD} = (2.3...5.5) V | -- | -- | 95 | ns |
| t _{AA} | Clock Low to Data Out Valid | V _{DD} = (2.3...5.5) V | -- | -- | 900 | ns |
| t _{BUF} | Bus Free Time between Stop and Start | V _{DD} = (2.3...5.5) V | 1300 | -- | -- | ns |
| t _{HD_STA} | Start Hold Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{SU_STA} | Start Set-up Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{HD_DAT} | Data Hold Time | V _{DD} = (2.3...5.5) V | 0 | -- | -- | ns |
| t _{SU_DAT} | Data Set-up Time | V _{DD} = (2.3...5.5) V | 100 | -- | -- | ns |
| t _R | Inputs Rise Time | V _{DD} = (2.3...5.5) V | -- | -- | 300 | ns |
| t _F | Inputs Fall Time | V _{DD} = (2.3...5.5) V | -- | -- | 300 | ns |
| t _{SU_STO} | Stop Set-up Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{DH} | Data Out Hold Time | V _{DD} = (2.3...5.5) V | 50 | -- | -- | ns |

Chip address

| HEX | BIN | DEC |
|------|---------|-----|
| 0x78 | 1111000 | 120 |

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1623:1620>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read ("1") or written ("0") by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

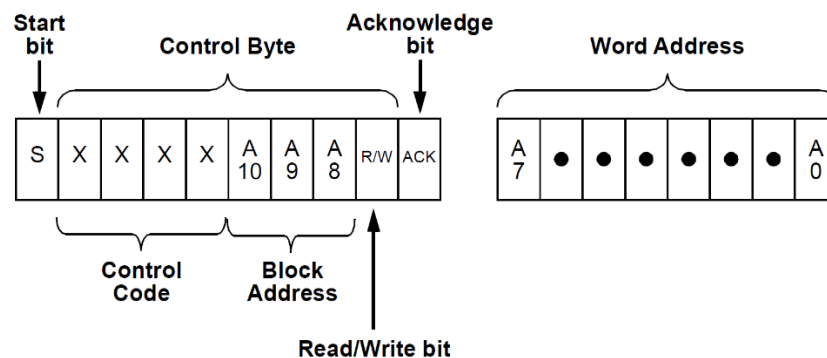


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

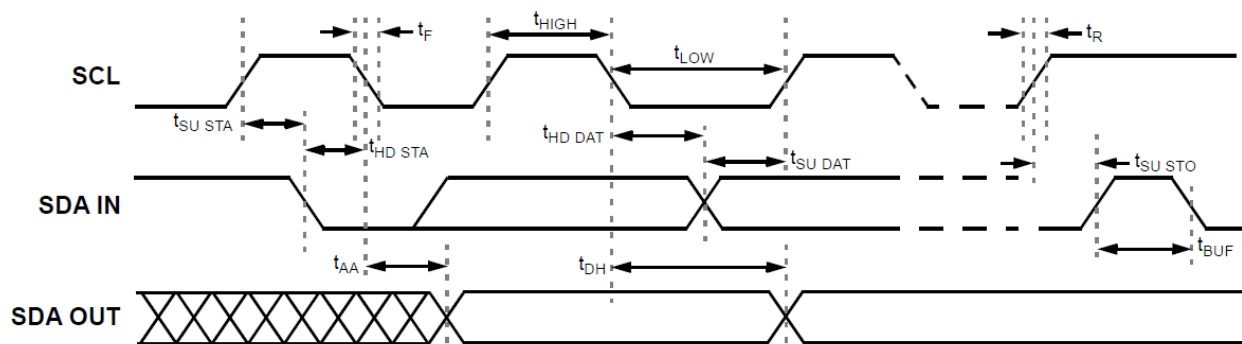


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46382 to the correct data byte to be written. After the SLG7RN46382 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46382 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46382 generates the Acknowledge bit.

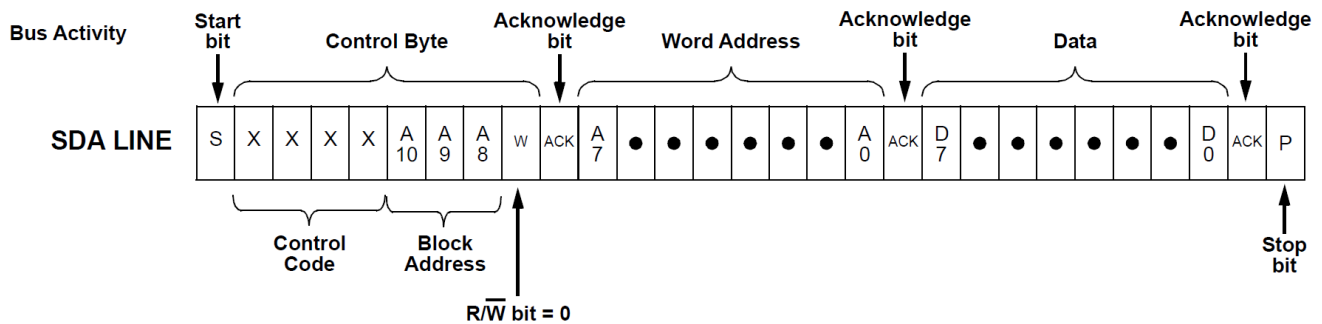


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with $\overline{R/W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the $\overline{R/W}$ bit set to “1”, after which the SLG7RN46382 issues an Acknowledge bit, followed by the requested eight data bits.

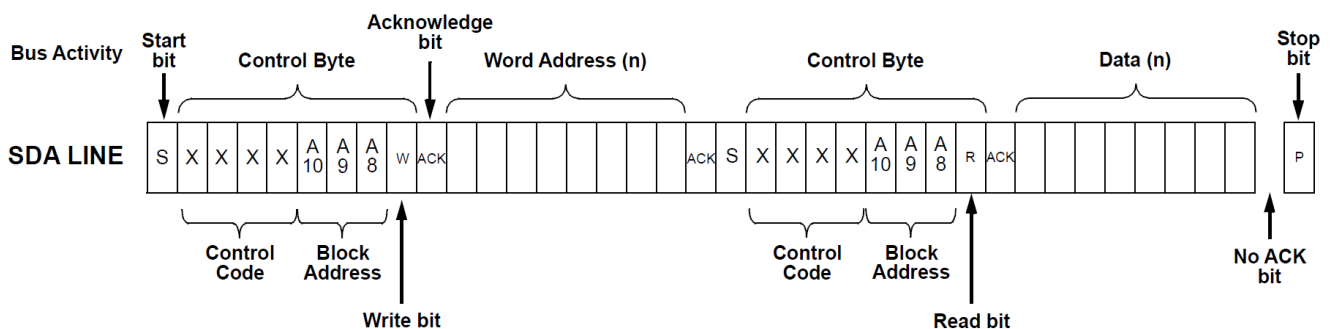


Figure4. I2C Random Read Command

4. Chip reconfiguration

SLG7RN46382 has an ISP capability. This means that the chip internal blocks configuration may be changed on the fly or even re-programmed via I2C. If there is a need for temporary change of the chip configuration (it will be reset to the programmed configuration after the chip is reset or powered ON again) one should use Registers (A10, A9, A8 = “000”). To reprogram a configuration via I2C NVM should be accessed with A10, A9, A8 = “010”. Please keep in mind that random byte write procedure is not supported, this may lead to incorrect chip configuration. Only page write procedure is supported.

Package Top Marking

| | | |
|------------------|-------|----------------|
| Part Code | XXXXX | |
| Date Code | DDLLL | Lot # |
| Pin 1 Identifier | ● CRR | COO + Revision |

- XXXXX - Part ID FieldL identifies the specific device configuration
- DD - Date Code Field: Coded date of manufacture
- LLL - Lot Code: Designates Lot #
- C - Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR - Revision Code: Device Revision

| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|--------------------|-------------------------|-------------|------------|-----------|----------|------------|
| 0.11 | 001 | U | 0x624AE845 | 46382 | AA | 03/22/2023 |

Lock coverage for this part is indicated by √, from one of the following options:

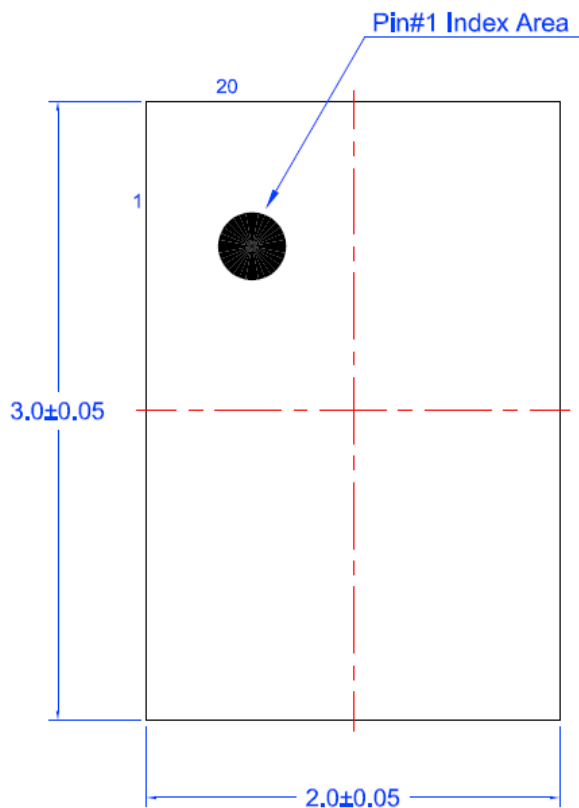
| | |
|---|---------------------------------|
| √ | Unlocked |
| | Partly lock read |
| | Partly lock write |
| | Partly lock read and write |
| | Partly lock read and lock write |
| | Lock read and partly lock write |
| | Read lock |
| | Write lock |
| | Lock read and write |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

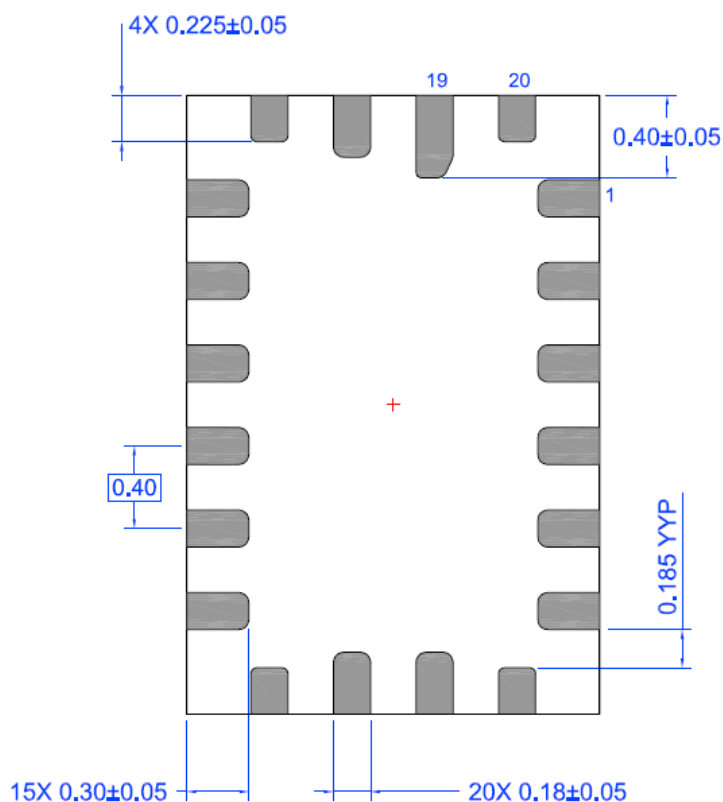
Package Outlines

STQFN 20L 2x3mm 0.4P FCD Package

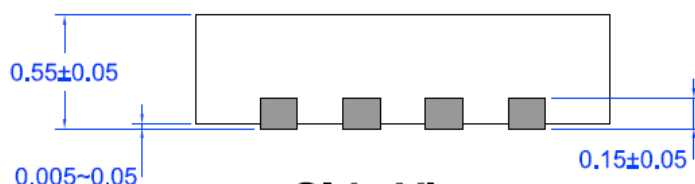
IC Net Weight: 0.008 g



Marking View



BTM View



Side View

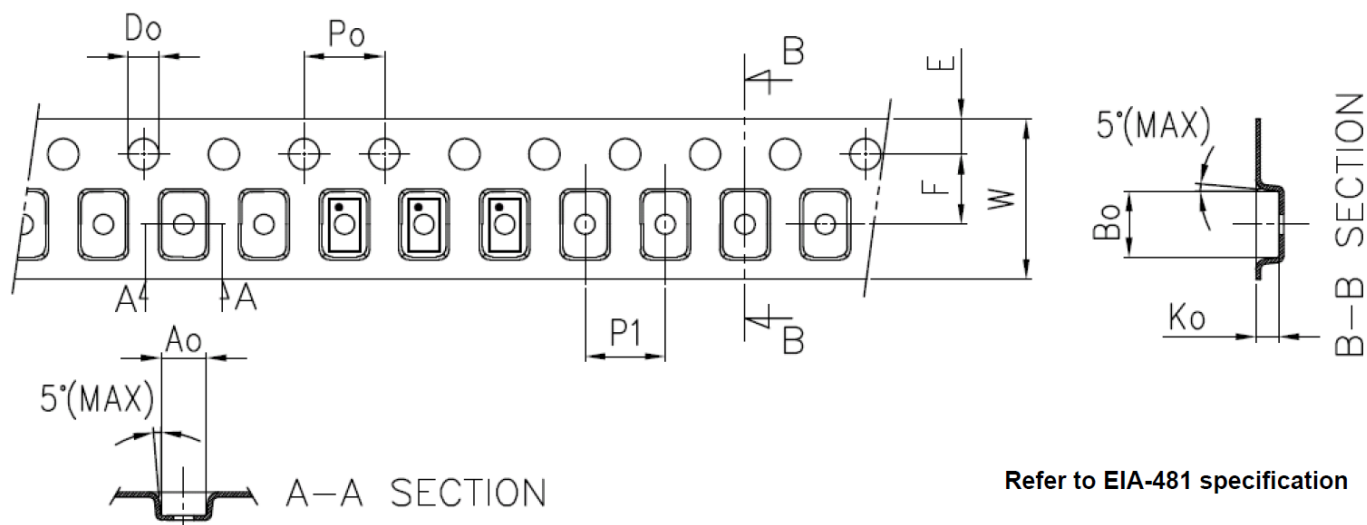
Unit: mm

Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|--------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2x3mm 0.4P FCD | 20 | 2 x 3 x 0.55 | 3000 | 3000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|--------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2x3mm 0.4P FCD | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



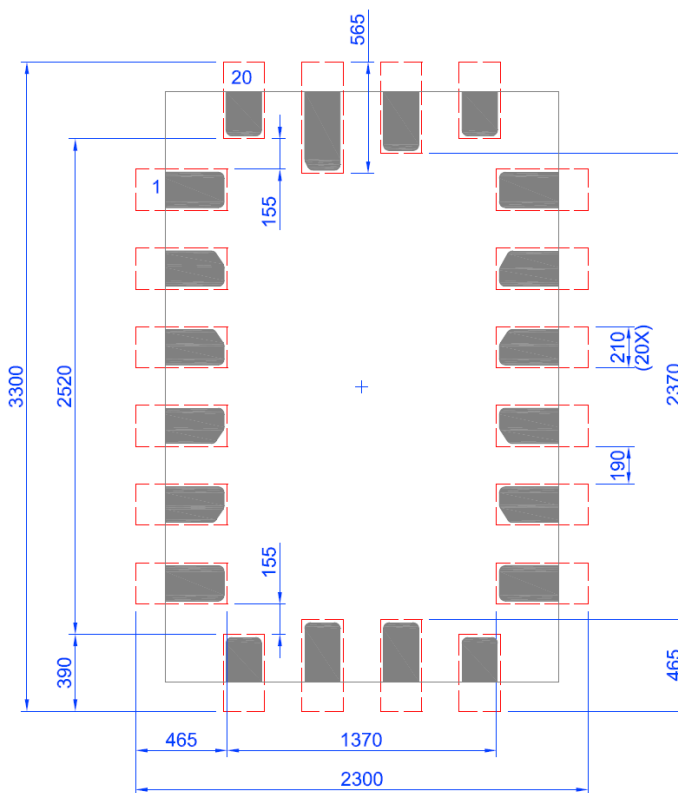
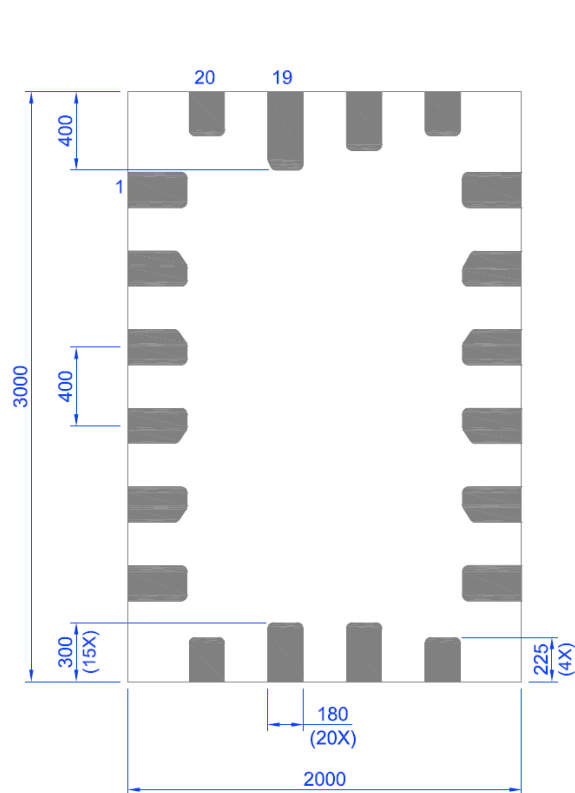
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm³ (nominal). More information can be found at www.jedec.org.

Layout Guidelines

 Exposed Pad
(PKG face down)

 Recommended Land Pattern
(PKG face down)



Unit: μm

Datasheet Revision History

| Date | Version | Change |
|------------|---------|-------------------------------|
| 03/14/2023 | 0.10 | New design for SLG46826 chip |
| 03/22/2023 | 0.11 | Updated Device Revision Table |

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