SLG7RN46468

GreenPAK ™

Sequencer prototype for RZ/T2 Series

General Description

Renesas SLG7RN46468 is a low power and small form device. The SoC is housed in a 1.6mm x 2.0mm STQFN package which is optimal for using with small devices.

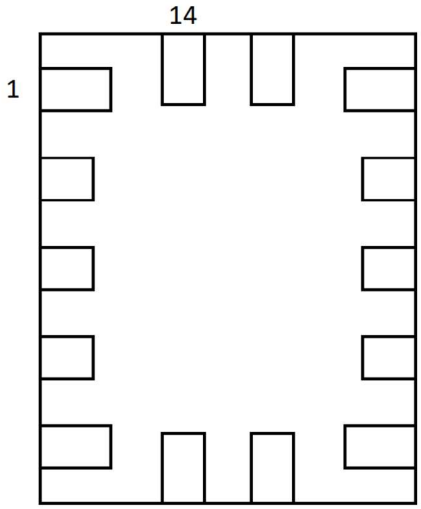
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Output Summary

5 Outputs - Push Pull 1X

Pin Configuration

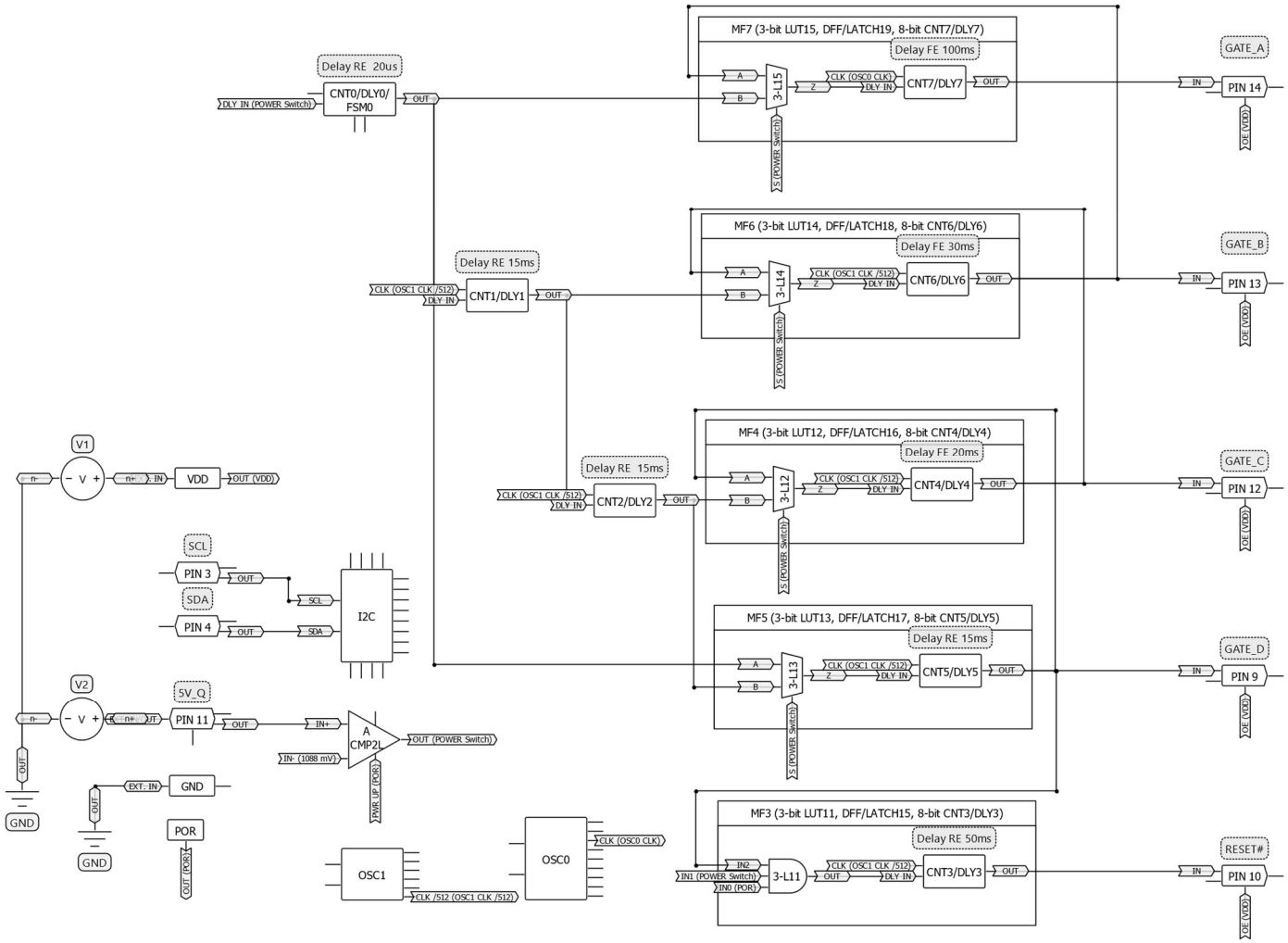


14-pin STQFN (Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	NC	9	GATE_D
3	SCL	10	RESET#
4	SDA	11	5V_Q
5	NC	12	GATE_C
6	NC	13	GATE_B
7	NC	14	GATE_A

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	SCL	Digital Input	Digital Input without Schmitt trigger	floating
4	SDA	Digital Input	Digital Input without Schmitt trigger	floating
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	NC	--	Keep Floating or Connect to GND	--
8	GND	GND	Ground	--
9	GATE_D	Digital Output	Push Pull 1X	floating
10	RESET#	Digital Output	Push Pull 1X	floating
11	5V_Q	Analog Input/Output	Analog Input/Output	floating
12	GATE_C	Digital Output	Push Pull 1X	floating
13	GATE_B	Digital Output	Push Pull 1X	floating
14	GATE_A	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN46468V	14-pin STQFN
SLG7RN46468V	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	V_{DD}+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PIN#3 and PIN#4 are HIGH, PIN#11 are LOW	--	48	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=1mA at VDD=2.5V	2.15	--	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.7	--	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD=5.0V	4.16	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=1mA, at VDD=2.5V	--	--	0.103	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.218	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	--	0.270	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, V_{OH}=VDD-0.2V at VDD=2.5V	1.37	--	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD=3.3V	5.61	--	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD=5.0V	20.42	--	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=2.5V	1.52	--	--	mA

		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	5.42	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	7.36	--	--	mA
T_{DLY0}	Delay0 Time	At temperature 25°C	20	22	24	µs
		At temperature -40 +85°C (Note 3)	19	22	27	µs
T_{DLY1}	Delay1 Time	At temperature 25°C	14.8	15.1	15.5	ms
		At temperature -40 +85°C (Note 3)	14.7	15.1	15.7	ms
T_{DLY2}	Delay2 Time	At temperature 25°C	14.8	15.1	15.5	ms
		At temperature -40 +85°C (Note 3)	14.7	15.1	15.7	ms
T_{DLY3}	Delay3 Time	At temperature 25°C	49.3	50.1	51.0	ms
		At temperature -40 +85°C (Note 3)	49.2	50.1	51.6	ms
T_{DLY4}	Delay4 Time	At temperature 25°C	19.7	20.1	20.6	ms
		At temperature -40 +85°C (Note 3)	19.6	20.1	20.8	ms
T_{DLY5}	Delay5 Time	At temperature 25°C	14.8	15.1	15.5	ms
		At temperature -40 +85°C (Note 3)	14.7	15.1	15.7	ms
T_{DLY6}	Delay6 Time	At temperature 25°C	29.6	30.1	30.7	ms
		At temperature -40 +85°C (Note 3)	29.5	30.1	31.1	ms
T_{DLY7}	Delay7 Time	At temperature 25°C	99.0	100.3	102.6	ms
		At temperature -40 +85°C (Note 3)	97.9	100.3	109.7	ms
V_{ACMP2}	Analog Comparator2 Threshold Voltage	Low to High transition, at temperature 25°C	2082	--	2229	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1979	--	2372	mV
		High to Low transition, at temperature 25°C	1708	--	1840	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1624	--	1959	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 3)	ACMP 2 at temperature 25°C	187	192	197	mV
		ACMP 2 at temperature -40 +85°C	186	192	198	mV
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.60	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.

I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (2.3...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5V ± 8%	--	--	95	ns
		V_{DD} = 3.3V ± 10%	--	--	95	ns
		V_{DD} = 5.0V ± 10%	--	--	111	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (2.3...5.5) V	--	--	900	ns

t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (2.3...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (2.3...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (2.3...5.5) V	50	--	--	ns

Chip address

HEX	BIN	DEC
0x08	0001000	8

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<2027:2024>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

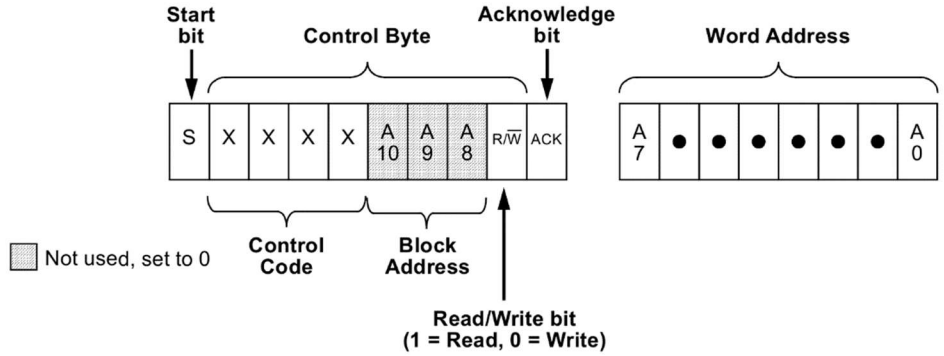


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

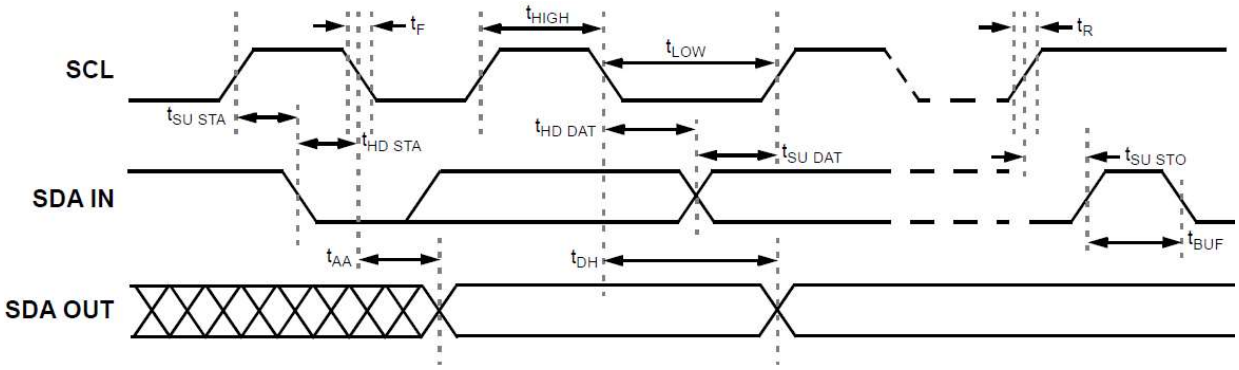


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46468 to the correct data byte to be written. After the SLG7RN46468 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46468 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46468 generates the Acknowledge bit.

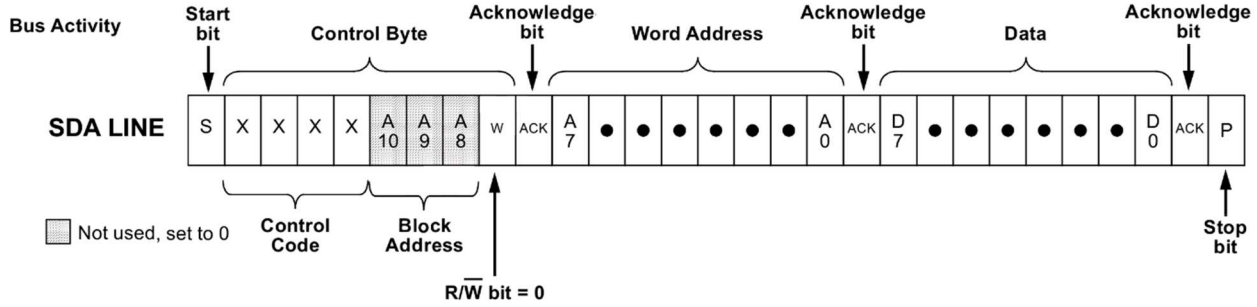


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN46468 issues an Acknowledge bit, followed by the requested eight data bits.

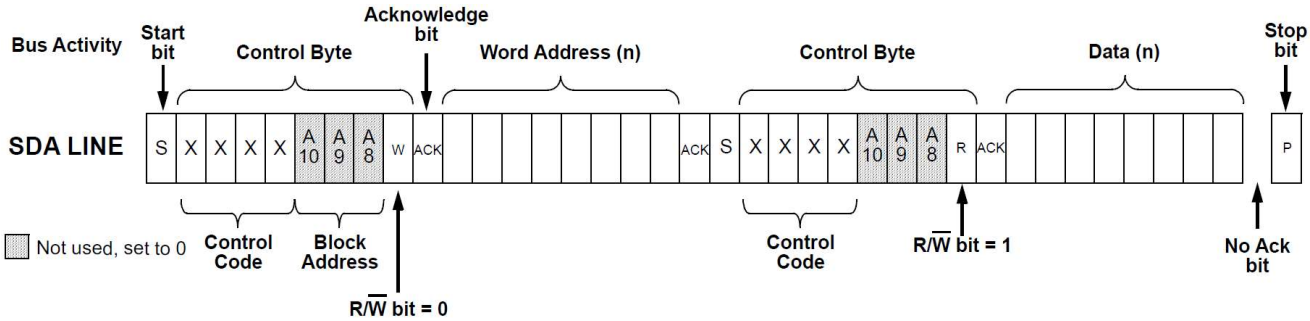
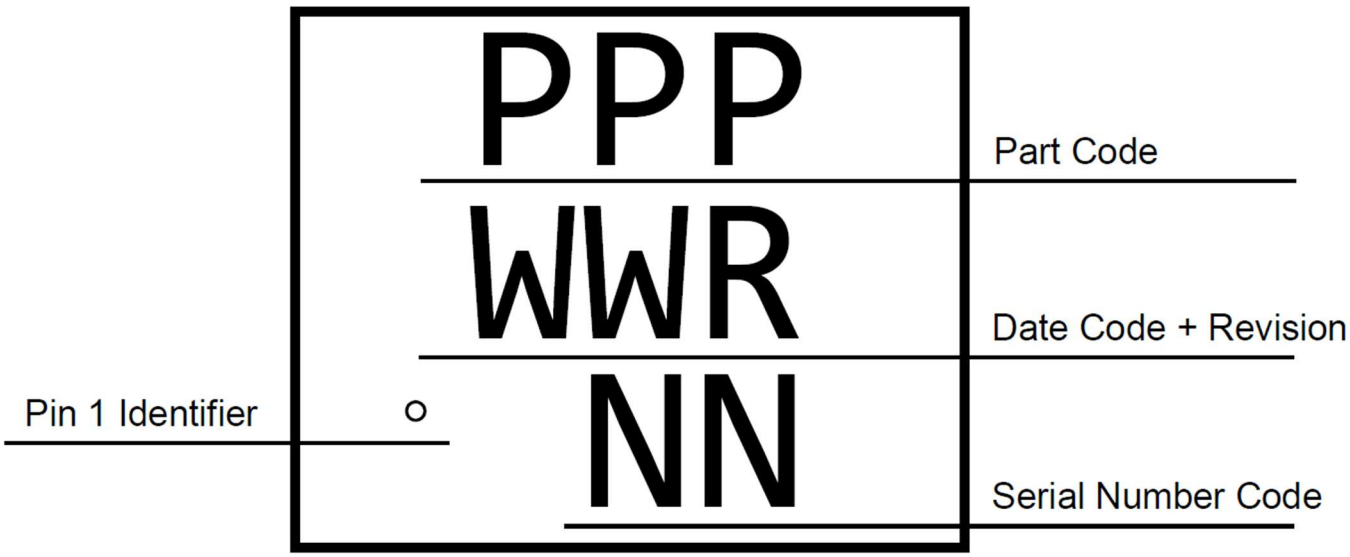


Figure4. I2C Random Read Command

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	002	U	0x33D4EE26			04/27/2023

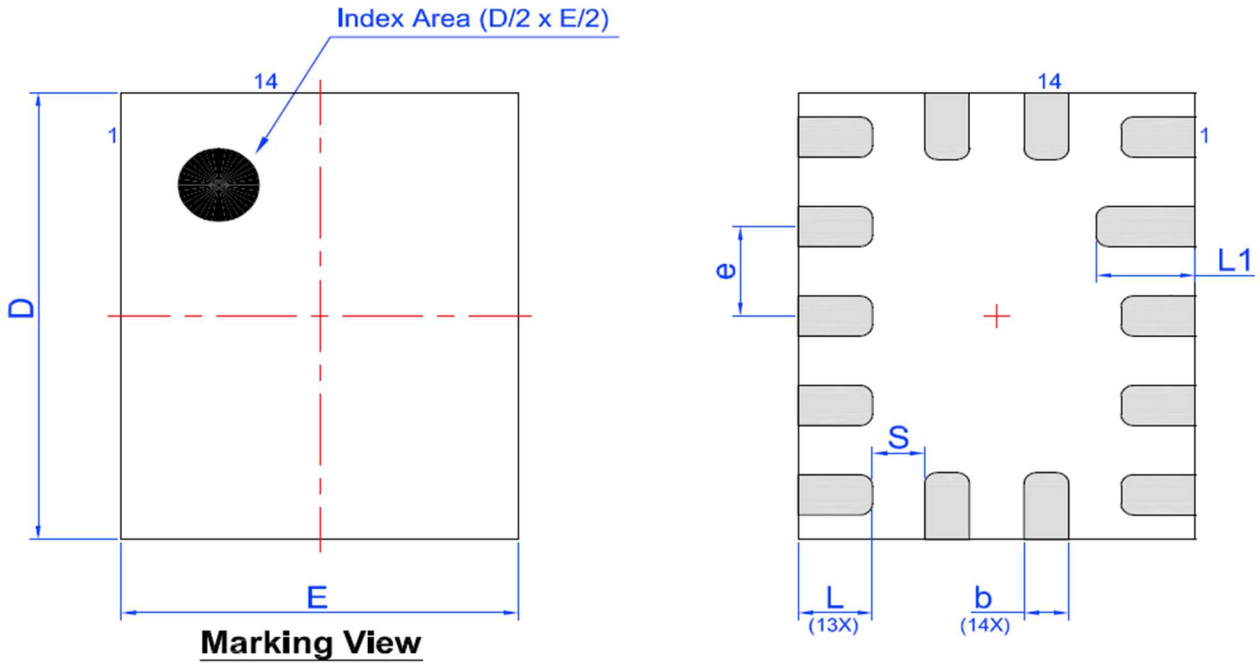
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

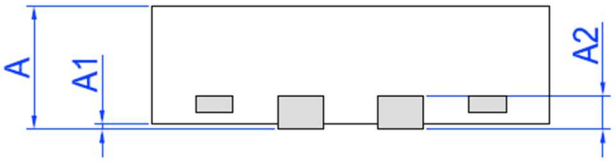
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Marking View



Marking View

Unit: mm

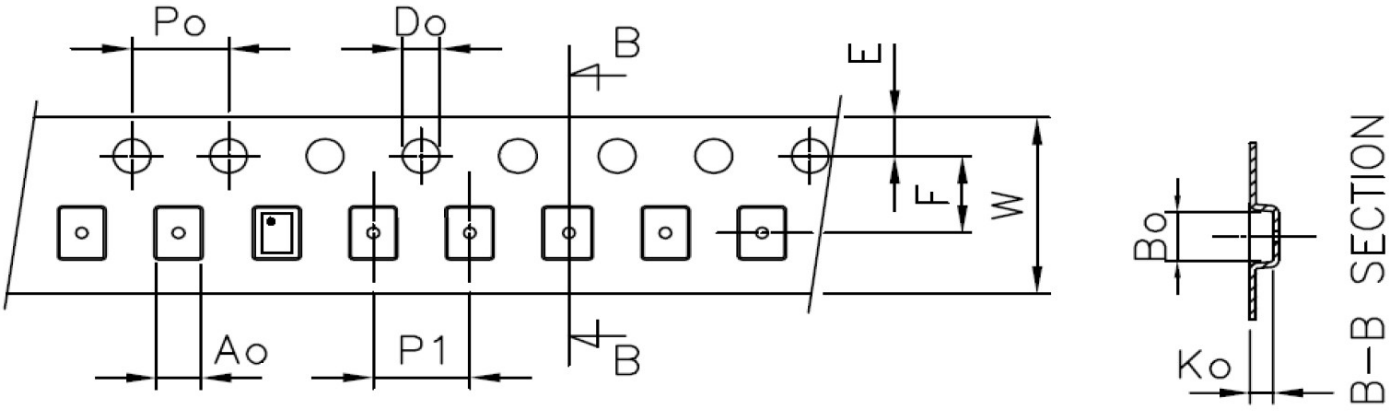
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

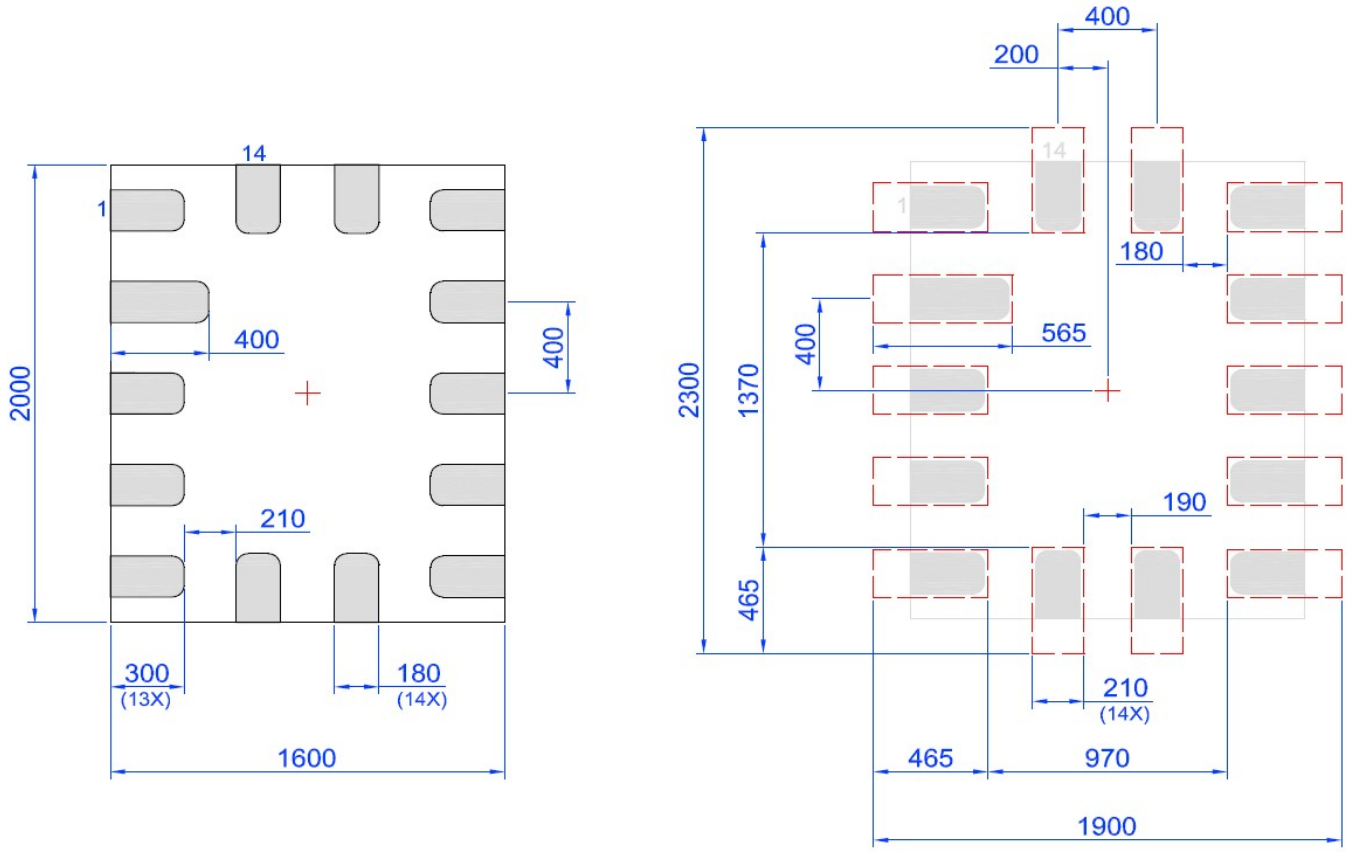
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Layout Guidelines



Unit: um

Datasheet Revision History

Date	Version	Change
04/10/2023	0.10	New design for SLG46855 chip, based on the SLG7RN46304V
04/27/2023	0.11	Changed design, added ACMP2L

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