SLG7RN46471

GreenPAK ™

Emulator/Manual Reset Switching Circuit

General Description

Renesas SLG7RN46471 is a low power and small form device. The SoC is housed in a 6.5mm x 6.4mm TSSOP package which is optimal for using with small devices.

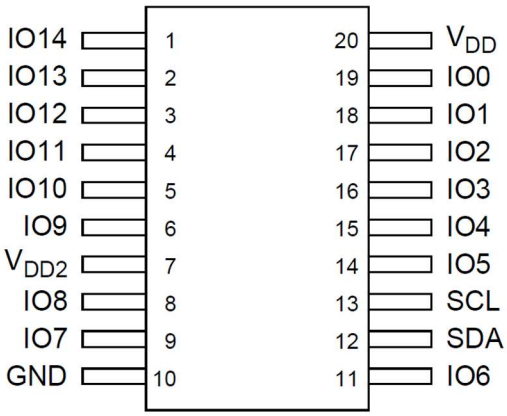
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- TSSOP - 20 Package

Output Summary

2 Outputs - Open Drain NMOS 1X

Pin Configuration

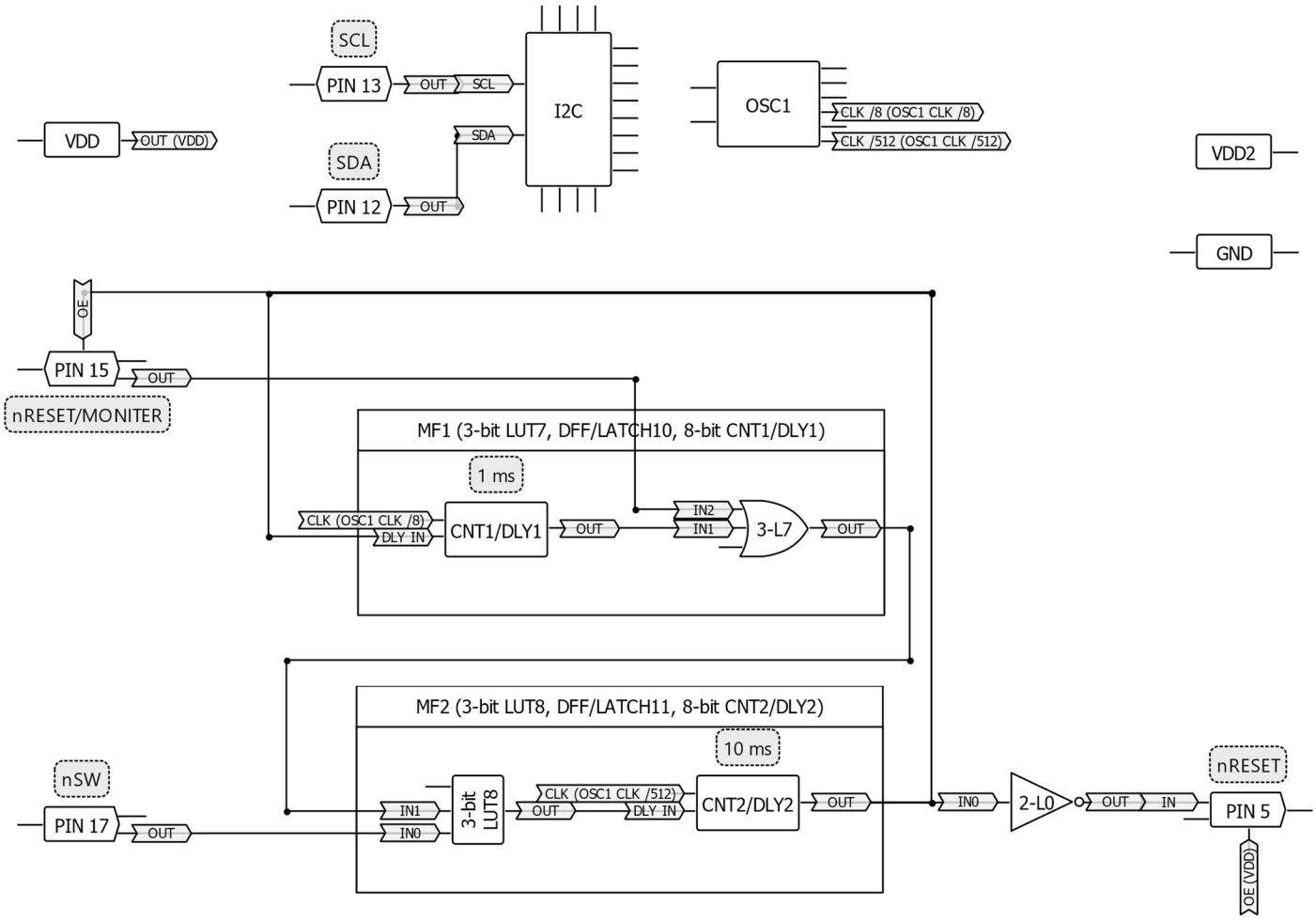


TSSOP-20
(Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	NC	11	NC
2	NC	12	SDA
3	NC	13	SCL
4	NC	14	NC
5	nRESET	15	nRESET/MONITER
6	NC	16	NC
7	VDD2	17	nSW
8	NC	18	NC
9	NC	19	NC
10	GND	20	VDD

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	NC	--	Keep Floating or Connect to GND	--
2	NC	--	Keep Floating or Connect to GND	--
3	NC	--	Keep Floating or Connect to GND	--
4	NC	--	Keep Floating or Connect to GND	--
5	nRESET	Digital Output	Open Drain NMOS 1X	100kΩ pullup
6	NC	--	Keep Floating or Connect to GND	--
7	VDD2	PWR	Supply Voltage	--
8	NC	--	Keep Floating or Connect to GND	--
9	NC	--	Keep Floating or Connect to GND	--
10	GND	GND	Ground	--
11	NC	--	Keep Floating or Connect to GND	--
12	SDA	Digital Input	Digital Input without Schmitt trigger	floating
13	SCL	Digital Input	Digital Input without Schmitt trigger	floating
14	NC	--	Keep Floating or Connect to GND	--
15	nRESET/MONITER	Bi-directional	Digital Input without Schmitt trigger / Open Drain NMOS 1X	100kΩ pullup
16	NC	--	Keep Floating or Connect to GND	--
17	nSW	Digital Input	Digital Input with Schmitt trigger	100kΩ pullup
18	NC	--	Keep Floating or Connect to GND	--
19	NC	--	Keep Floating or Connect to GND	--
20	VDD	PWR	Supply Voltage	--

Ordering Information

Part Number	Package Type
SLG7RN46471G	20-pin TSSOP
SLG7RN46471GTR	20-pin TSSOP - Tape and Reel (4k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current Through V_{DD} Pin		--	90	mA
Maximum Average or DC Current Through V_{DD2} Pin		--	90	mA
Maximum Average or DC Current Through GND Pin (Per chip side, (Note 1))		--	100	mA
Maximum Average or DC Current (Through pin)	OD 1x	--	15.5	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		
Note 1 The GreenPAK's GND rail is divided in two sides. IOs 0 to 6, SCL, SDA are connected to one side and IOs 7 to 14 are connected to another side.				

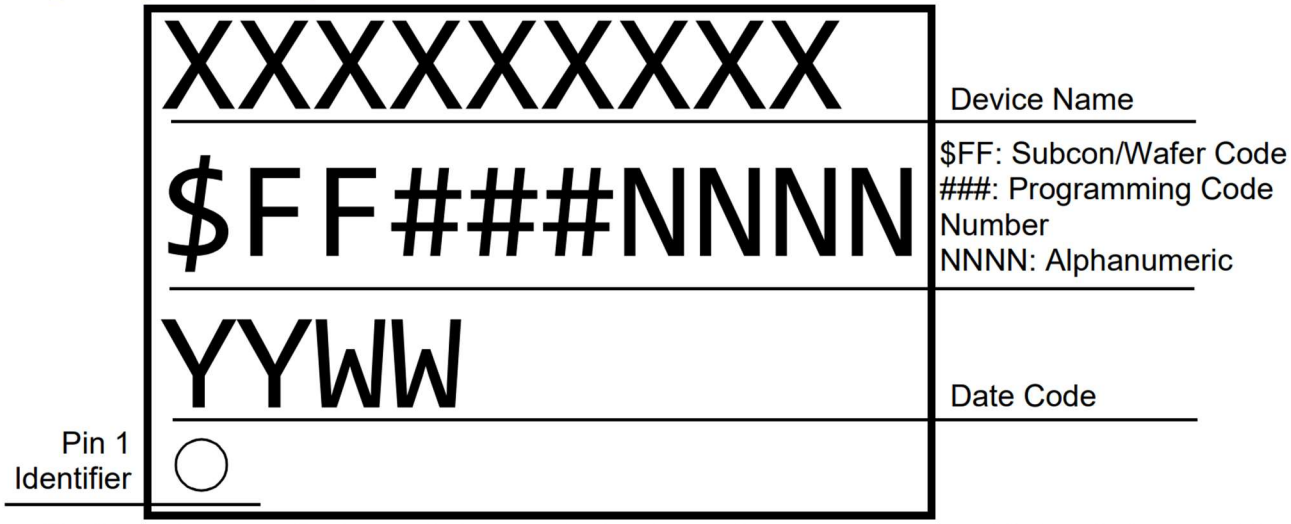
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
V_{DD2}	Supply Voltage		1.71	1.8	2	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		0.1	--	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3 (Note 1)	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
		Logic Input with Schmitt Trigger	0.8xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xVDD	V
V_{OL}	LOW-Level Output Voltage	Open Drain NMOS 1X, I_{OL}=1mA, at VDD=2.5V	--	--	0.035	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.088	V
I_{OL}	LOW-Level Output Current	Open Drain NMOS 1X, V_{OL}=0.15V, at VDD=2.5V	4.19	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	13.02	--	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 5, 15, 17	--	100	--	kΩ
T_{DLY1}	Delay1 Time	At temperature 25°C	0.98	1	1.02	ms
		At temperature -40 +85°C	0.98	1	1.04	ms
T_{DLY2}	Delay2 Time	At temperature 25°C	9.89	10.12	10.37	ms
		At temperature -40 +85°C	9.83	10.12	10.53	ms
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.66	2.59	ms

PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.60	1.85	2.07	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.97	1.23	1.46	V

Note:
1. The GreenPAK's power rails are divided in two sides. PINs 11 to 20 are powered from VDD (one side) and PINs 1 to 9 are powered from VDD2 (another side).

Package Top Marking



Note: For this package type, Revision code is not marked on the part but may be present on labels and other materials. Instead, Wafer Code and Programming Code Number are marked on the part.

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	U	0x5607B56B			04/18/2023

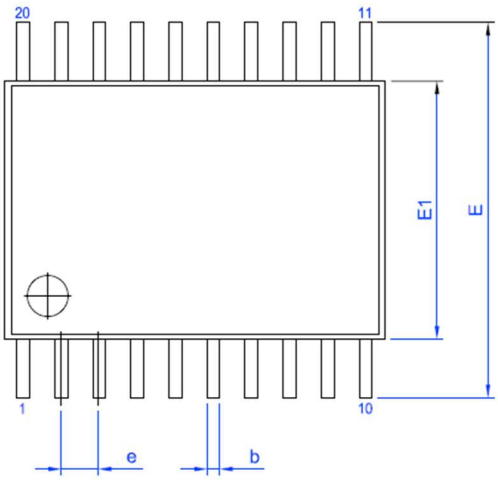
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read
	Partly lock write
	Partly lock read and write
	Partly lock read and lock write
	Lock read and partly lock write
	Read lock
	Write lock
	Lock read and write

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

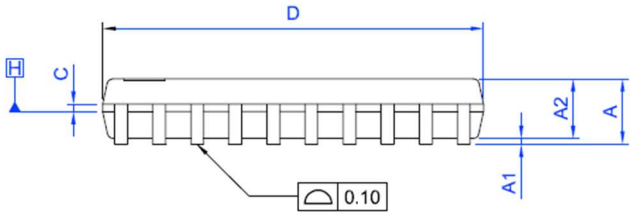
Package Outlines

IC Net Weight: 0.083 g

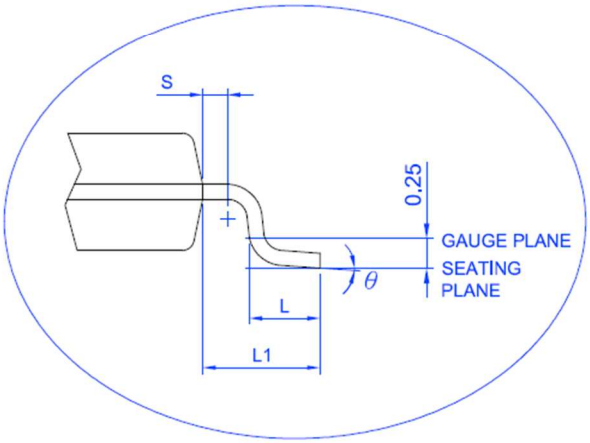


Marking View

Side View



Side view



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	-	-	1.20	D	6.40	6.50	6.60
A1	0.05	-	0.15	E1	4.30	4.40	4.50
A2	0.80	0.90	1.05	E	6.40 BSC		
b	0.19	-	0.30	L	0.50	0.60	0.75
C	0.09	-	0.20	L1	1.00 REF		
e	0.65 BSC			S	0.20	-	-
				Θ	0°	-	8°

NOTES:

1.JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F

2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.

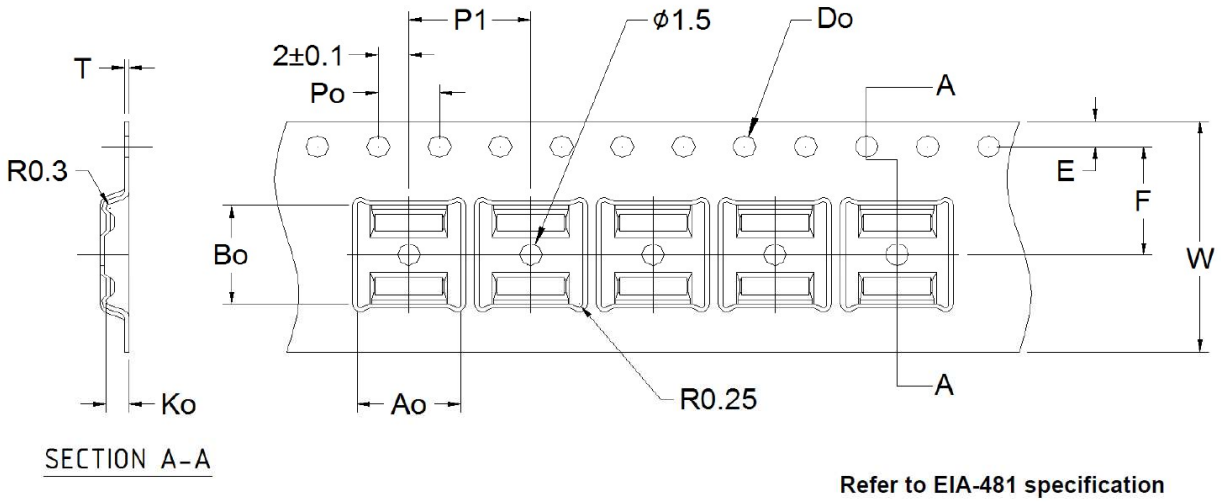
5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TSSOP 20L 173 MIL Green Package	20	6.5 x 6.4	4000	4000	330/100	42	336	42	336	16	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TSSOP 20L 173 MIL Green Package	6.8	6.9	1.6	4	8	1.5	1.75	7.5	16



Refer to EIA-481 specification

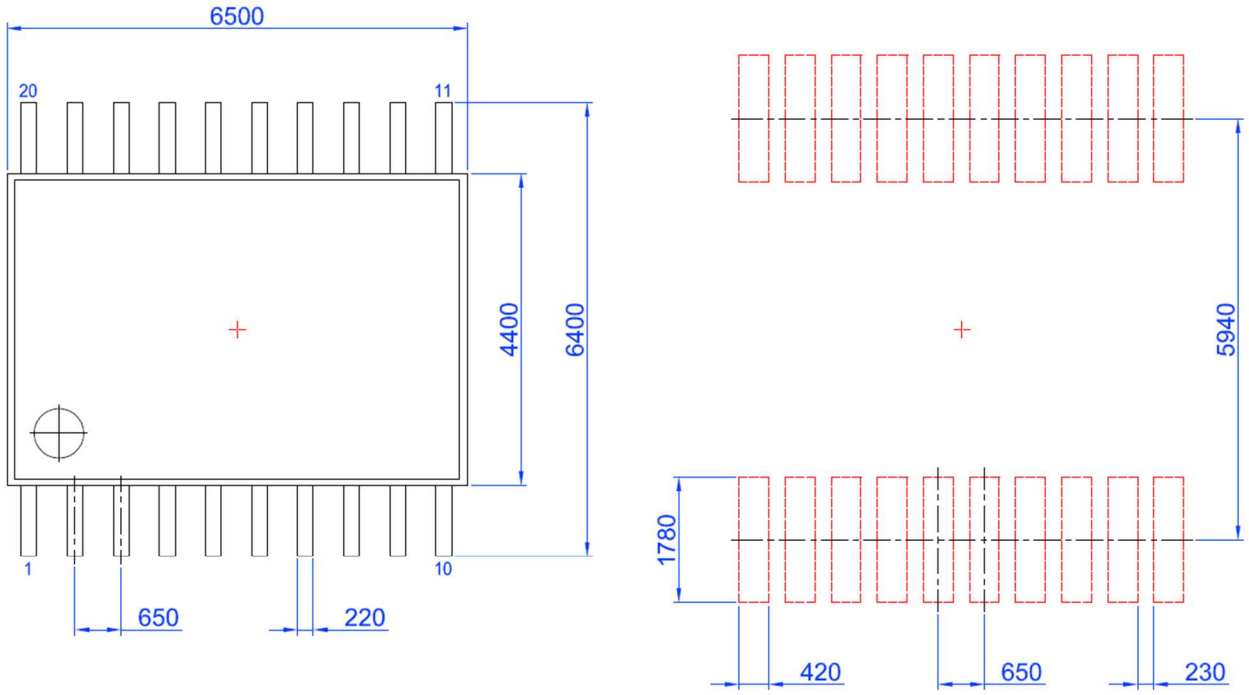
Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 25.74 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines

TSSOP-20



Unit: µm

Datasheet Revision History

Date	Version	Change
04/18/2023	0.10	New design for SLG46826G chip

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