SLG7RN46600

GreenPAK ™

SST: I2C Expander 13 Output, 2 Input

General Description

Renesas SLG7RN46600 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

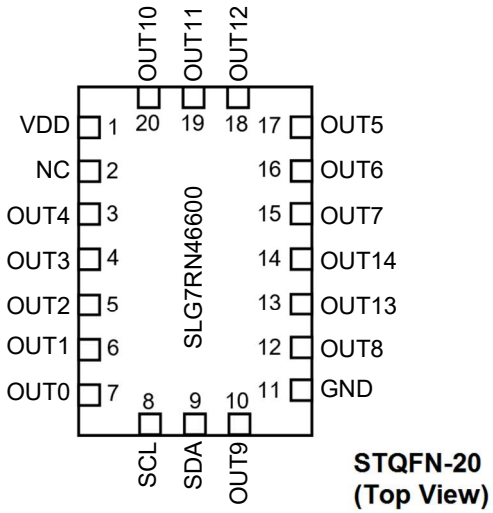
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

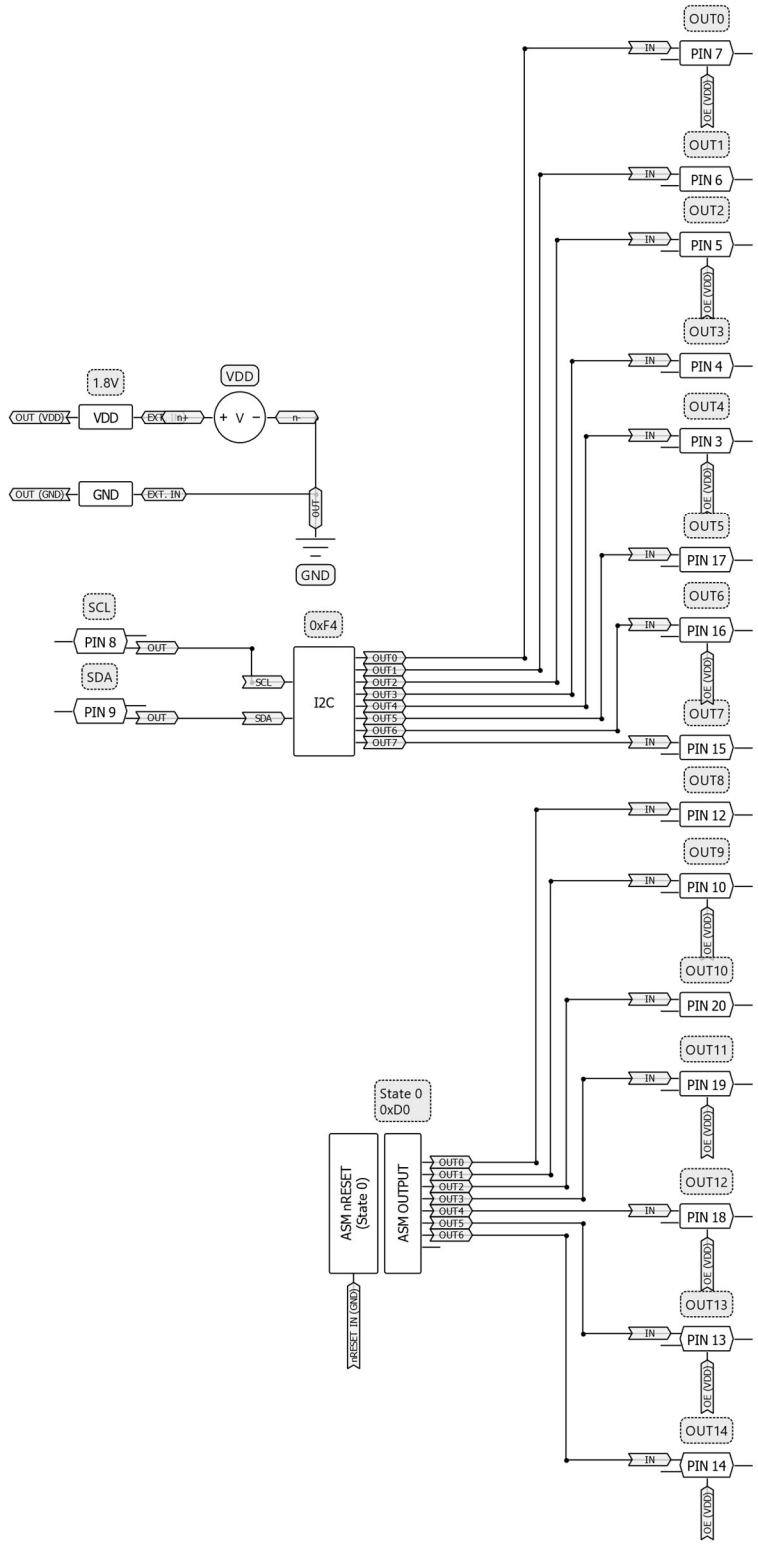
15 Outputs - Push Pull 1X

Pin Configuration



STQFN-20
(Top View)

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	OUT4	Digital Output	Push Pull 1X	floating
4	OUT3	Digital Output	Push Pull 1X	floating
5	OUT2	Digital Output	Push Pull 1X	floating
6	OUT1	Digital Output	Push Pull 1X	floating
7	OUT0	Digital Output	Push Pull 1X	floating
8	SCL	Digital Input	Digital Input without Schmitt trigger	floating
9	SDA	Digital Input	Digital Input without Schmitt trigger	floating
10	OUT9	Digital Output	Push Pull 1X	floating
11	GND	GND	Ground	--
12	OUT8	Digital Output	Push Pull 1X	floating
13	OUT13	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
14	OUT14	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
15	OUT7	Digital Output	Push Pull 1X	floating
16	OUT6	Digital Output	Push Pull 1X	floating
17	OUT5	Digital Output	Push Pull 1X	floating
18	OUT12	Digital Output	Push Pull 1X	floating
19	OUT11	Digital Output	Push Pull 1X	floating
20	OUT10	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN46600V	20-pin STQFN
SLG7RN46600V	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.8	1.89	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PIN8 and PIN9 are HIGH	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=1.8V	1.06	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=1.8V	0	--	0.76	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=100µA, at VDD=1.8V	1.69	1.79	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA, at VDD=1.8V	--	0.009	0.013	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, V_{OH}=VDD-0.2V, at VDD=1.8V	1.07	1.70	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=1.8V	0.92	1.69	--	mA
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.63	1.36	1.87	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 1, 2, 3, 4, 5, 6, 7, 8 and 19 are connected to one side, PINs 11, 12, 13, 14, 15, 17, 18, 21 and 22 to another.
3. Guaranteed by Design.

I2C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (1.71...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	VDD = 1.8V ± 5%	--	--	168	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (1.71...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (1.71...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (1.71...5.5) V	50	--	--	ns

Asynchronous State Machine (ASM) Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
$t_{st\_out\_delay}$	Asynchronous State Machine Output Delay Time	VDD = 1.8V ± 5%	225	--	275	ns
t_{st_out}	Asynchronous State Machine Output Transition Time	VDD = 1.8V ± 5%	--	--	165	ns
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	VDD = 1.8V ± 5%	29	--	--	ns
t_{st_comp}	Asynchronous State Machine Input Compete Time	VDD = 1.8V ± 5%	--	--	29	ns

Chip address

HEX	BIN	DEC
0x08	0001000	8

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

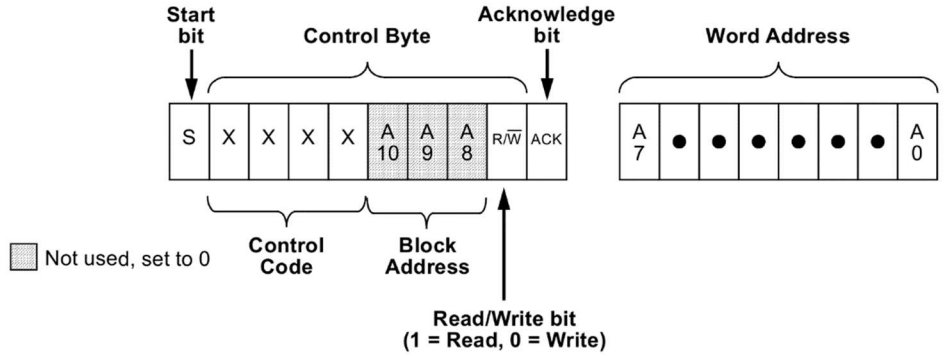


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

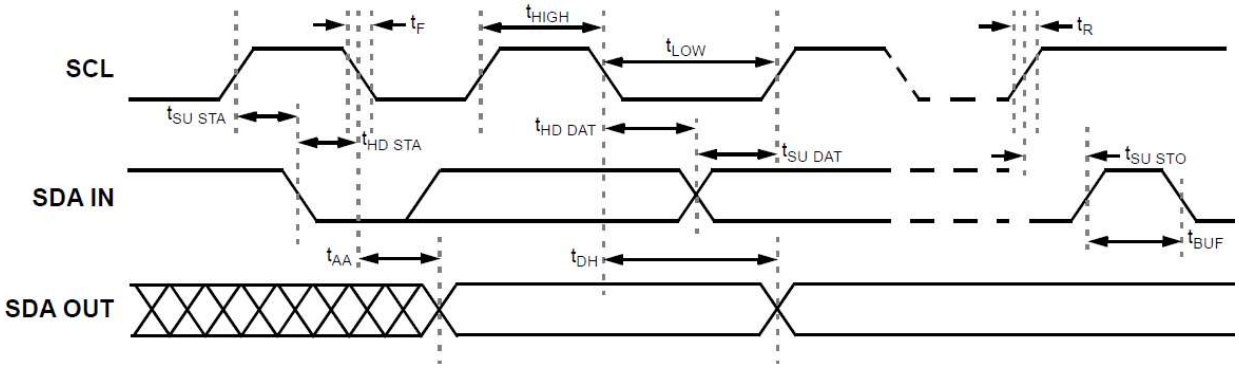


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLGRN46600 to the correct data byte to be written. After the SLGRN46600 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLGRN46600 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLGRN46600 generates the Acknowledge bit.

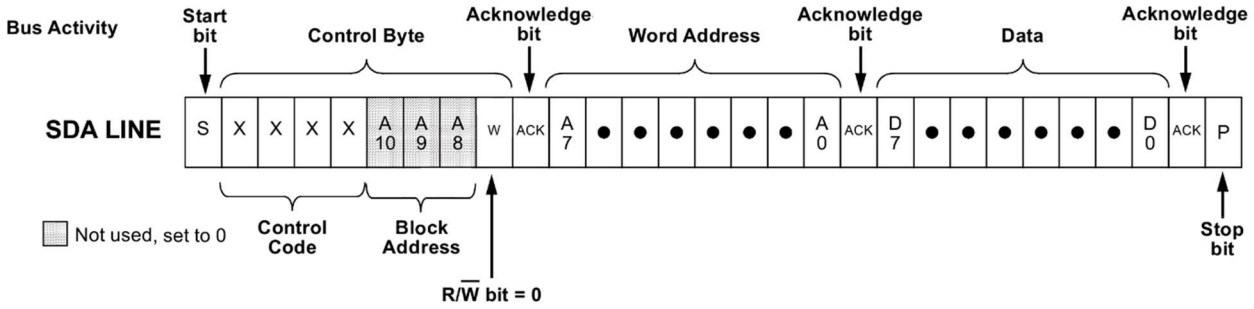


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLGRN46600 issues an Acknowledge bit, followed by the requested eight data bits.

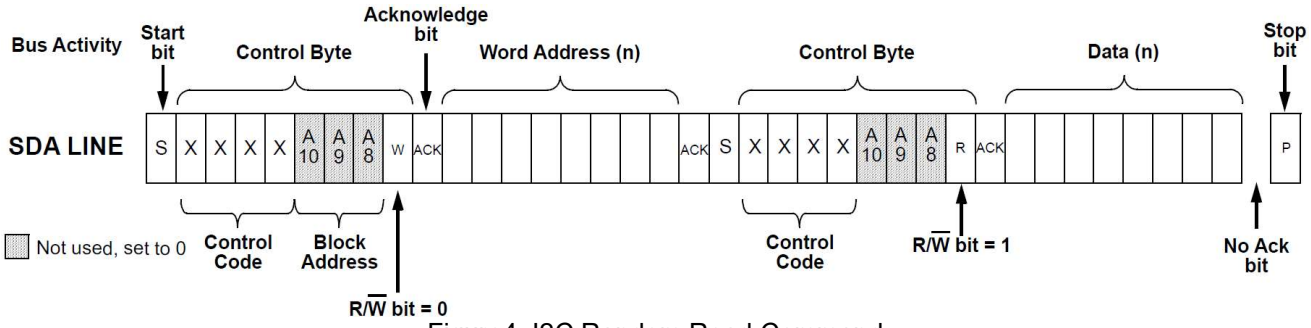


Figure4. I2C Random Read Command

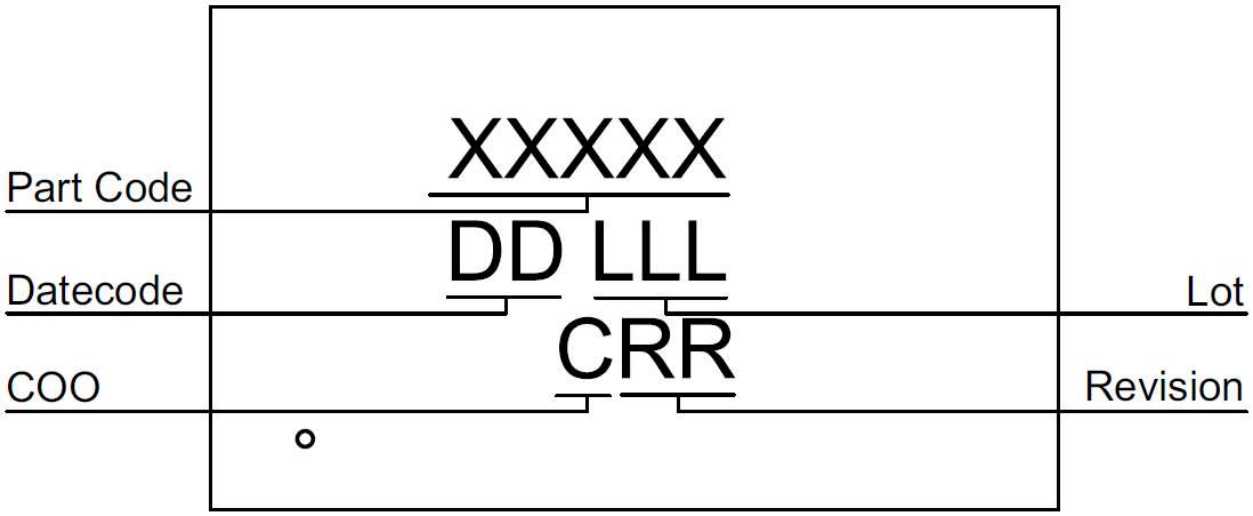
4. I2C register control data

Address Byte	Register Bit	Block	Function
0x27	reg<319:312>	IO10 Output Enable	Change PIN13 direction, 0x00 for input, 0x3F for output
0x29	reg<335:328>	IO11 Output Enable	Change PIN14 direction, 0x00 for input, 0x3F for output
0xD0	reg<1664>	ASM-state0 OUT0	Enable (0) and disable (1) OUT8 Default is 0.
	reg<1665>	ASM-state0 OUT1	Enable (0) and disable (1) OUT9 Default is 0.
	reg<1666>	ASM-state0 OUT2	Enable (0) and disable (1) OUT10 Default is 0.
	reg<1667>	ASM-state0 OUT3	Enable (0) and disable (1) OUT11 Default is 0.
	reg<1668>	ASM-state0 OUT4	Enable (0) and disable (1) OUT12 Default is 0.
	reg<1669>	ASM-state0 OUT5	Enable (0) and disable (1) OUT13 Default is 0.
	reg<1670>	ASM-state0 OUT6	Enable (0) and disable (1) OUT14 Default is 0.
0xF4	reg<1952>	Virtual Input <0>	Enable (0) and disable (1) OUT0 Default is 0.
	reg<1953>	Virtual Input <1>	Enable (0) and disable (1) OUT1 Default is 0.
	reg<1954>	Virtual Input <2>	Enable (0) and disable (1) OUT2 Default is 0.
	reg<1955>	Virtual Input <3>	Enable (0) and disable (1) OUT3 Default is 0.
	reg<1956>	Virtual Input <4>	Enable (0) and disable (1) OUT4 Default is 0.
	reg<1957>	Virtual Input <5>	Enable (0) and disable (1) OUT5 Default is 0.
	reg<1958>	Virtual Input <6>	Enable (0) and disable (1) OUT6 Default is 0.
	reg<1959>	Virtual Input <7>	Enable (0) and disable (1) OUT7 Default is 0.
0xF6	reg<1968>	Don't care	Don't care
	reg<1969>	IO10 Digital Input	State of PIN13, when it works as input
	reg<1970>	IO11 Digital Input	State of PIN14, when it works as input
	reg<1975:1971>	Don't care	Don't care

5. I2C Commands:

1. [start] [0x08] [w] [0xD0] [xxxxxxx(OUT8)] [stop] // enable (OUT8 = 0) or disable (OUT8 = 1)
2. [start] [0x08] [w] [0xD0] [xxxxxx(OUT9)x] [stop] // enable (OUT9 = 0) or disable (OUT9 = 1)
3. [start] [0x08] [w] [0xF4] [xxxxxxx(OUT0)] [stop] // enable (OUT0 = 0) or disable (OUT0 = 1)
4. [start] [0x08] [w] [0xF4] [xxxxxx(OUT1)x] [stop] // enable (OUT1 = 0) or disable (OUT1 = 1)
5. [start] [0x08] [w] [0x27] [0x3F] [stop] // Change PIN13 to input mode
6. [start] [0x08] [w] [0x29] [0x3F] [stop] // Change PIN14 to input mode
7. [start] [0x08] [w] [0xF6] [start] [0x08] [R] [xxxxx(OUT14)(OUT13)x][stop] // read PIN13 and PIN14 state, is valid when PINs work as input

Package Top Marking



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	U	0x50E208D5			05/29/2023

Lock coverage for this part is indicated by √, from one of the following options:

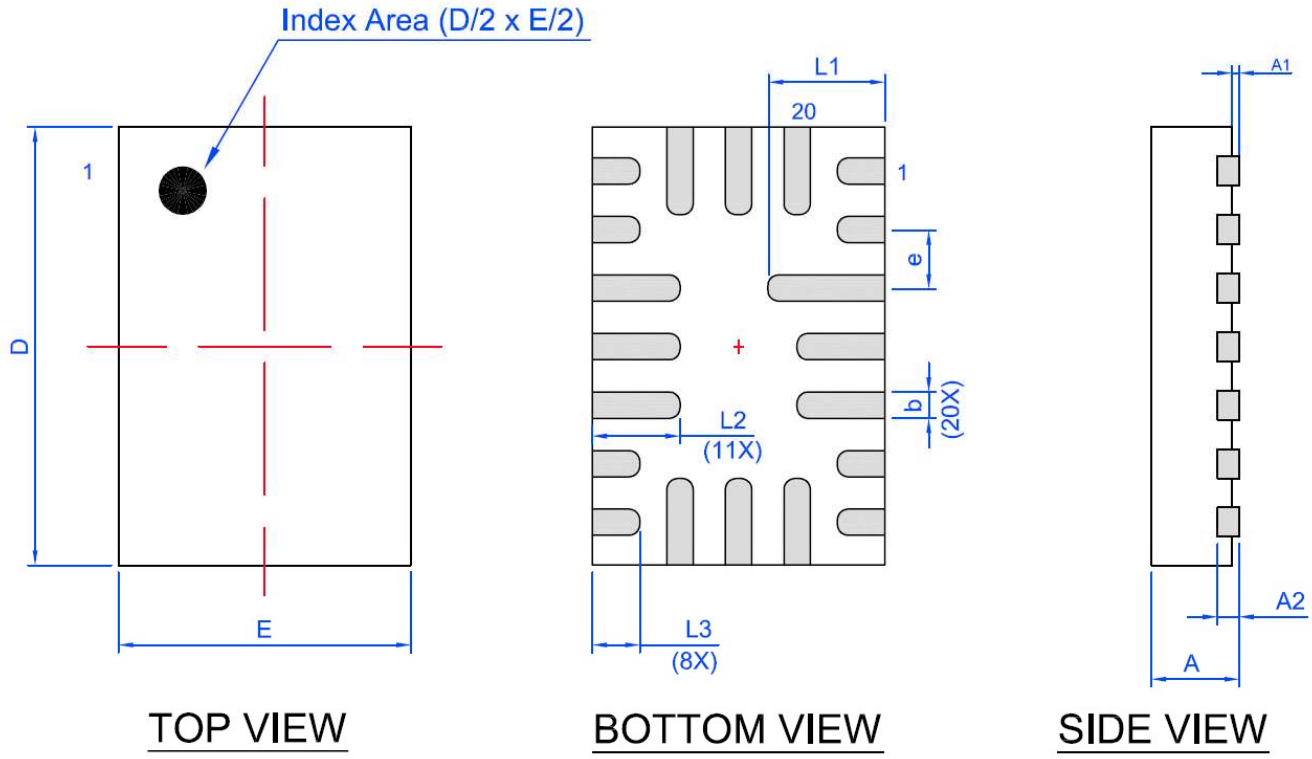
√	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package

JEDEC MO-220



TOP VIEW BOTTOM VIEW SIDE VIEW

Unit: mm

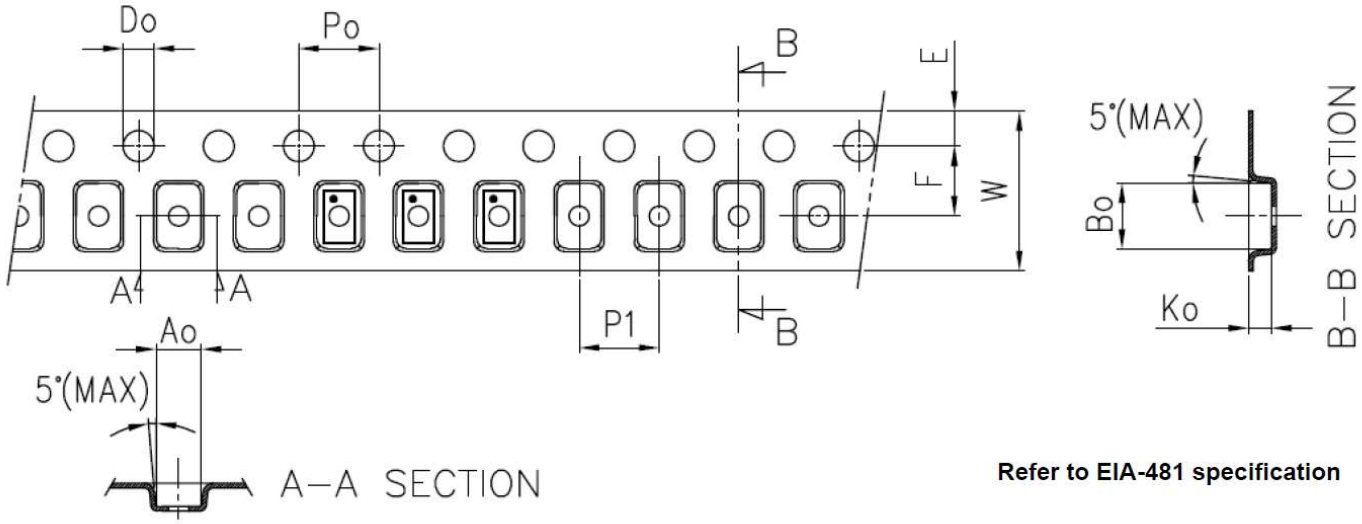
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3 mm 0.4P COL	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

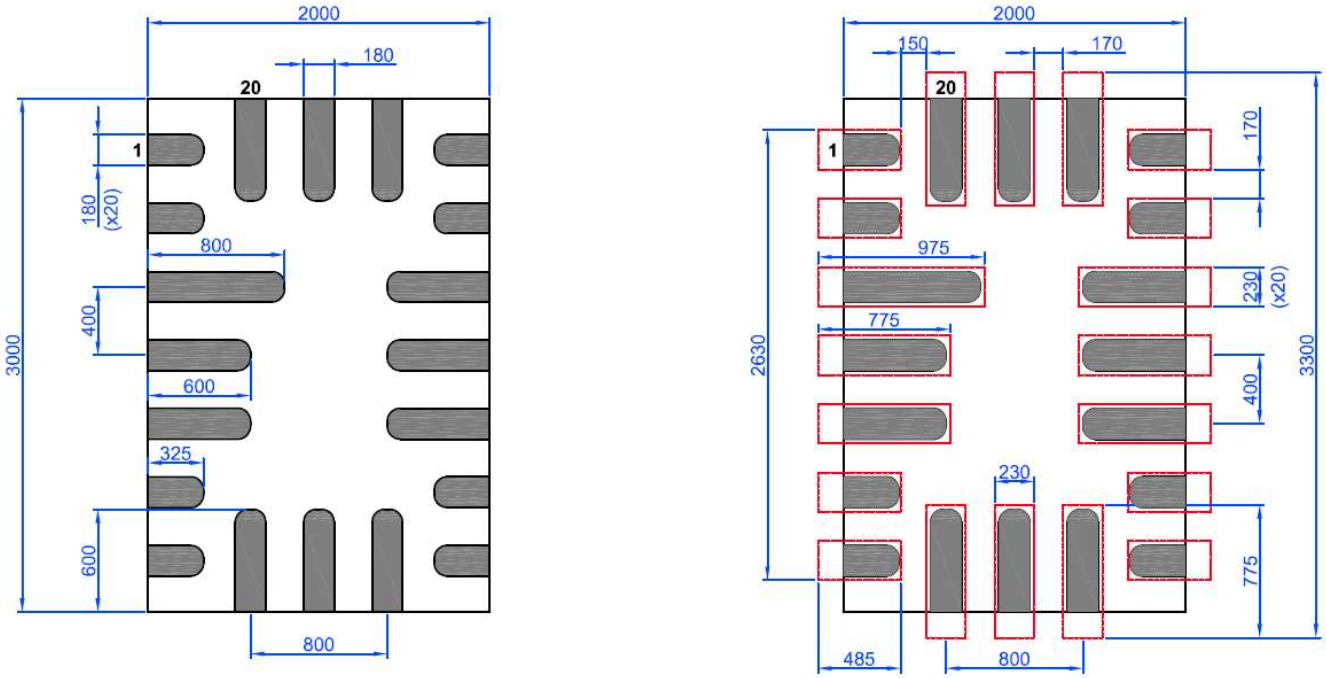
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm



Datasheet Revision History

Date	Version	Change
05/29/2023	0.10	New design for SLG46537V chip

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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