SLG7RN47748

DC-DC Boost Converter & Buzzer Driver

Description

The SLG7RN47748 provides a small, low power component for commonly used Mixed-Signal and H-Bridge functions. The mixed-signal IC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices. Configurable PWM macrocells in combination with Special High Voltage outputs will be useful for a motor drive or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations visit the HVPAK™ website.

Email GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Output Summary

- 3 Outputs - High and Low MOSFET on
- 1 Output - Low MOSFET on

Features

- Low Power Consumption
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 mm x 3 mm x 0.55 mm,
- 0.4 mm Pitch
- Four High Voltage High Current Drive GPOs
- Programmable Pattern
- Easily Adjustable Piezo Frequency

Applications

- Smart Locks
- Electric Toothbrushes
- Smart Blinds
- Smart Fans
- Air Fresheners
- Humidifiers
- Keychains
- Trackers
- E-Cigarettes
- POS Terminals
- Smart Speakers
- Kitchen Electronics
- Smoke Alarms
- Gas Alarms
- Water Alarms
- Medical Devices
- Security Systems
- Wearables
- Fitness Trackers
- Remote Controls
- Battery-Powered Toys
- IoT Sensors
- Industrial Control Panels
- Home Automation Hubs
- Environmental Monitors

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1. Overview

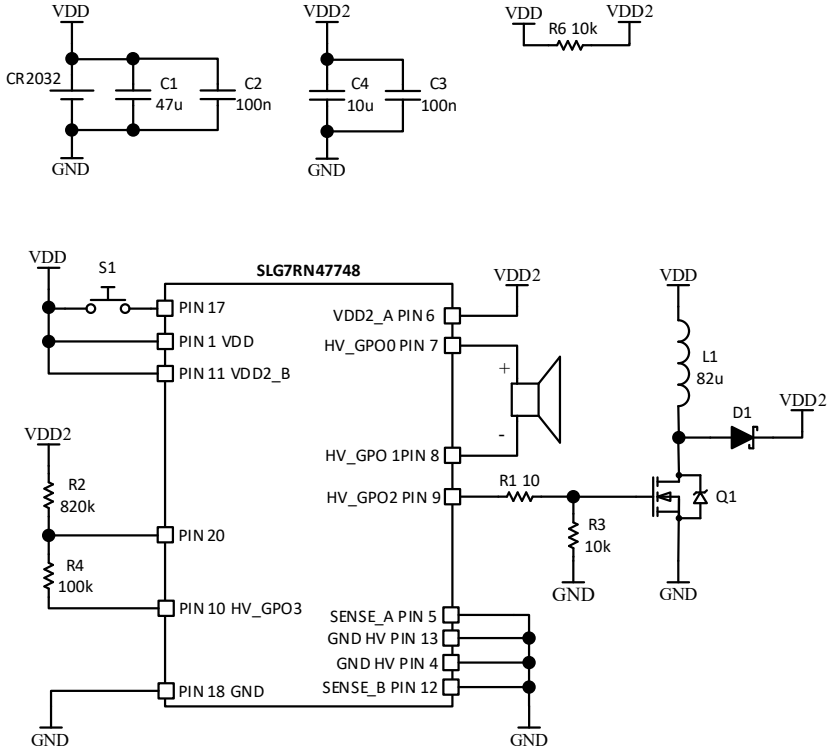
The SLG7RN47748 is a flexible, configurable mixed-signal IC that combines a DC-DC boost converter and a piezo driver in a single package, requiring a small number of external components.

Such a schematic can be used in devices that require short-term notifications (keychains for finding things, and others). When the push button S1 is pressed, the DC-DC converter boosts the voltage from 3 V to 9.5 V, which powers the piezo driver. Then the short pattern is played with a resonant piezo frequency of 1 kHz. Then the circuit goes to sleep mode until the button S1 is pressed again.

If the battery voltage (VDD) drops to less than 2.5 V, the system powers down.

When the circuit is ON, it consumes nearly 8.5 mA RMS, and in sleep mode, the current consumption is less than 1 uA.

1.1 Typical Application Circuit

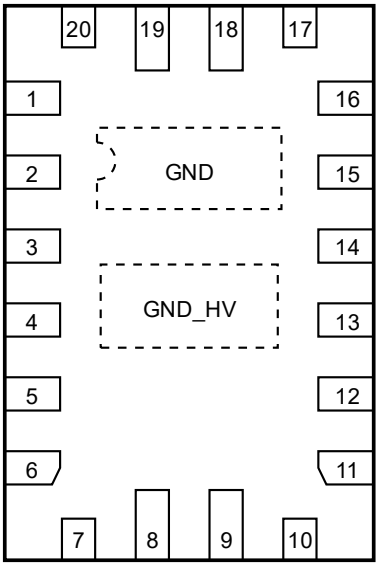


1.2 Ordering Information

Part number	Package type
SLG7RN47748V	20-pin STQFN - Tape and Reel (3k units)

2. Pin Information

2.1 Pin Assignments



STQFN-20L
(Top View)

2.2 Pin Name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	VDD2_B
2	NC	12	SENSE B
3	NC	13	GND HV
4	GND HV	14	NC
5	SENSE A	15	NC
6	VDD2_A	16	NC
7	AOUT1	17	Boost&Buzzer_EN
8	AOUT2	18	GND
9	BOUT1	19	NC
10	BOUT2	20	FB

2.3 Pin Configuration

Pin	Pin Name	Type	Pin Description	Internal Resistors
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or connect to GND	--
3	NC	--	Keep Floating or connect to GND	--
4	GND HV	GND HV	High Voltage Ground	--
5	SENSE A	--	Connect to GND	--
6	VDD2_A	PWR	Supply Voltage	--
7	AOUT1	Digital Output	HIGH and LOW MOSFET on	--
8	AOUT2	Digital Output	HIGH and LOW MOSFET on	--
9	BOUT1	Digital Output	HIGH and LOW MOSFET on	--
10	BOUT2	Digital Output	LOW MOSFET on	--
11	VDD2_B	PWR	Supply Voltage	--
12	SENSE B	--	Connect to GND	--
13	GND HV	GND HV	High Voltage Ground	--
14	NC	--	Keep Floating or connect to GND	--
15	NC	--	Keep Floating or connect to GND	--
16	NC	--	Keep Floating or connect to GND	--
17	Boost&Buzzer_EN	Digital Input	Digital Input with Schmitt trigger	100 kΩ pull-down
18	GND	GND	Ground	--
19	NC	--	Keep Floating or connect to GND	--
20	FB	Analog Input/Output	Analog Input/Output	floating

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter		Description	Condition	Min	Max	Unit
Supply Voltage on V_{DD} relative to GND				-0.3	7.0	V
Supply Voltage on V_{DD2} relative to GND				-0.3	18.0	V
DC Input Voltage				GND-0.5	V_{DD}+0.5	V
Maximum V_{DD} Average or DC Current		(Through V_{DD} or GND pin) for V_{DD} Group		--	120	mA
Maximum V_{DD2} or Sense Average or DC Current		(Through each V_{DD2_A}, V_{DD2_B}, SENSE_A or SENSE_B pin)		--	2000	mA
Maximum Average or DC Current (V_{DD2} power supply)	Push-Pull/Half Bridge	Through V_{DD2} High Current Group pins		--	1500	mA
Current at Input Pin		Through V_{DD} Group pin		-0.1	1.0	mA
Input Leakage Current (Absolute Value)				--	1000	nA
Storage Temperature Range				-65	150	℃
Junction Temperature				--	150	℃
ESD Protection (Human Body Model)				4000	--	V
ESD Protection (Charged Device Model)				1300	--	V
Moisture Sensitivity Level				1		

3.2 Thermal Information

Parameter	Description	Condition	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance	4L JEDEC PCB	--	--	65	℃/W
		4L JEDEC PCB with a thermal vias that connect thermal pad through all layers of the PCB	--	--	46	℃/W
$\theta_{JC(top)}$	Junction-to-case (top) Thermal Resistance		--	23.50	--	℃/W
θ_{JB}	Junction-to-board Thermal Resistance		--	25.51	--	℃/W
$\psi_{JC(top)}$	Junction-to-case (top) Characterization Parameter		--	6.80	--	℃/W
ψ_{JB}	Junction-to-board Characterization Parameter		--	24.44	--	℃/W

3.3 Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (Note 3)		2.70	3.20	3.30	V
V_{DD2_A}	High Supply Voltage (Note 3)		3.00	9.50	13.20	V
V_{DD2_B}	High Supply Voltage (Note 3)		3.00	3.20	3.30	V
T_A	Operating Ambient Temperature		-40	25	85	℃
C_{VDD}	Capacitor Value at V_{DD}		--	0.1	--	µF
C_{IN}	Input Capacitance		--	2.5	--	pF
I_{Q_VDD}	Quiescent Current	Static inputs and floating outputs	--	1.0	--	µA
$I_{Q\_VVD2\_A}$	Quiescent Current	Static inputs and floating outputs	--	0.5	--	µA
$I_{Q\_VDD2\_B}$	Quiescent Current	Static inputs and floating outputs	--	0.5	--	µA
V_O	Maximal Voltage Applied to any PIN in High Impedance State	for V_{DD} Group	--	--	V_{DD}+0.3	V

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{O2}	Maximal Voltage Applied to any PIN in High Impedance State	for V_{DD2} Group	--	--	V_{DD}+0.3	V
V_{IH}	HIGH-Level Input Voltage for V_{DD} group (Note 1)	Logic Input with Schmitt Trigger	0.8xV_{DD}	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage for V_{DD} group (Note 1)	Logic Input with Schmitt Trigger	GND-0.3	--	0.2xV_{DD}	V
V_{OH2}	HIGH-Level Output Voltage for V_{DD2} High Current Group	Push-Pull, V_{DD2} = 5 V ± 10 %, I_{OH2} = 10 mA	4.496	--	--	V
		Push-Pull, V_{DD2} = 9 V ± 10 %, I_{OH2} = 10 mA	8.097	--	--	V
		Push-Pull, V_{DD2} = 12 V ± 10 %, I_{OH2} = 10 mA	10.797	--	--	V
V_{OL2}	LOW-Level Output Voltage for V_{DD2} High Current Group	Push-Pull, V_{DD2} = 5 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 9 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		Push-Pull, V_{DD2} = 12 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
R_{PULL_DOWN}	Internal Pull-Down Resistance	Pull-down on PIN 17	--	100	--	kΩ
T_{OSH1}	Pulse Width	At temperature +25 ℃	440	540	720	ns
		At temperature -40 +85 ℃ (Note 2)	380	540	740	ns
T_{DLY2}	Delay Time	At temperature +25 ℃	49.04	50.53	52.25	ms
		At temperature -40 +85 ℃ (Note 2)	47.78	50.53	55.02	ms
T_{OSH3}	Pulse Width	At temperature +25 ℃	853.24	876.95	893.06	ms
		At temperature -40 +85 ℃ (Note 2)	831.40	876.95	939.68	ms
T_{OSH4}	Pulse Width	At temperature +25 ℃	2.20	2.34	2.55	us
		At temperature -40 +85 ℃ (Note 2)	2.12	2.34	2.61	us
$T_{PipeDelay}$	Delay Time	At temperature +25 ℃	280	340	520	ns
		At temperature -40 +85 ℃ (Note 2)	240	340	540	ns
T_{PWM0}	Period	At temperature +25 ℃	4.90	5.08	5.32	us
		At temperature -40 +85 ℃ (Note 2)	4.78	5.08	5.44	us
V_{ACMP0H}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 ℃	2583	--	2651	mV
		Low to High transition, at temperature -40 +85 ℃ (Note 2)	2574	--	2659	mV
		High to Low transition, at temperature +25 ℃	2456	--	2523	mV
		High to Low transition, at temperature -40 +85 ℃ (Note 2)	2448	--	2531	mV
V_{ACMP1H}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 ℃	1009	--	1033	mV
		Low to High transition, at temperature -40 +85 ℃ (Note 2)	1005	--	1036	mV
		High to Low transition, at temperature +25 ℃	1009	--	1033	mV
		High to Low transition, at temperature -40 +85 ℃ (Note 2)	1005	--	1036	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 2)	ACMP 0 at temperature +25 ℃	--	32	--	mV
		ACMP 0 at temperature -40 +85 ℃	--	32	--	mV

Parameter	Description	Condition	Min	Typ	Max	Unit
T_{SU}	Chip Startup Time	From V_{DD} rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip, T_J = -40 °C to 150 °C	1.80	1.98	2.16	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip, T_J = -40 °C to 150 °C	1.33	1.55	1.83	V

Note 1 ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect VIH and VIL.
Note 2 Guaranteed by Design.

Note 3 VDD2_A and VDD2_B are physically connected to VDD on the demo board. Therefore, the minimum possible voltage on VDD2_A and VDD2_B is 2.7V. The 2.7 V - 3.0 V range for VDD2_A and VDD2_B is not guaranteed by the specification.

3.4 HV Output Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
t_R	Rise time HV OUT in Pre-Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to 150 °C	10	13	22	ns
	Rise time HV OUT in Driver Mode	VDD2 = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to 150 °C	80	116	200	ns
t_F	Fall time HV OUT in Pre-Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 85 °C	8	11	23	ns
		V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 150 °C	8	11	25	ns
	Fall time HV OUT in Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 85 °C	80	115	200	ns
		V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 150 °C	80	115	225	ns
t_{DEAD}	Dead band time of HV_GPOx_HD in Pre-Driver Mode (For Full Bridge and Half Bridge HV OUT modes)	V_{DD2} = 3 V, T_J = -40 °C to 150 °C	--	55	--	ns
		V_{DD2} = 5 V, T_J = -40 °C to 150 °C	--	23	--	ns
		V_{DD2} = 13.2 V, T_J = -40 °C to 150 °C	--	22	--	ns
	Dead band time of HV_GPOx_HD in Driver Mode (For Full Bridge and Half Bridge HV OUT modes	V_{DD2} = 3 V, T_J = -40 °C to 150 °C	--	337	--	ns
		V_{DD2} = 5 V, T_J = -40 °C to 150 °C	--	75	--	ns
		V_{DD2} = 13.2 V, T_J = -40 °C to 150 °C	--	91	--	ns
PWM_t_{DEAD}	Dead Band Time, Generated by PWM Block	Configured in PWM Block	0; $1 \cdot T_{clk}$	$2 \cdot T_{clk}$	$3 \cdot T_{clk}$	CLK time
$R_{DS(ON)}$	HS FET on resistance (SENSE_A, SENSE_B, GND_HV and GND Pins are connected together)	V_{DD2} = 13.2 V, I_O = 500 mA, T_J = 25 °C	--	171	--	mΩ
		V_{DD2} = 13.2 V, I_O = 500 mA, T_J = 150 °C	--	--	295	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = 25 °C	--	171	--	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = 150 °C	--	--	295	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = 25 °C	--	177	--	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = 150 °C	--	--	305	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = 25 °C	--	256	--	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = 150 °C	--	--	426	mΩ
	LS FET on resistance (SENSE_A, SENSE_B, GND_HV and GND Pins are connected together)	V_{DD2} = 13.2 V, I_O = 500 mA, T_J = 25 °C	--	182	--	mΩ
		V_{DD2} = 13.2 V, I_O = 500 mA, T_J = 150 °C	--	--	332	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = 25 °C	--	182	--	mΩ
		V_{DD2} = 9.0 V, I_O = 500 mA, T_J = 150 °C	--	--	331	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = 25 °C	--	185	--	mΩ
		V_{DD2} = 5.0 V, I_O = 500 mA, T_J = 150 °C	--	--	338	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = 25 °C	--	232	--	mΩ
		V_{DD2} = 3.0 V, I_O = 500 mA, T_J = 150 °C	--	--	414	mΩ

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OFF}	Off-state leakage current	GPO0_HD, GPO1_HD (Note 1), V_{DD2} = 5.0 V, T_J = -40 ℃ to 85 ℃, Sleep Mode	23.2	--	32.9	µA
		GPO0_HD, GPO1_HD (Note 1), V_{DD2} = 5.0 V, T_J = -40 ℃ to 150 ℃, Sleep Mode	23.2	--	35.2	µA
		GPO2_HD, GPO3_HD, V_{DD2} = 5.0 V, T_J = -40 ℃ to 85 ℃, Sleep Mode	--	--	0.2	µA
		GPO2_HD, GPO3_HD, V_{DD2} = 5.0 V, T_J = -40 ℃ to 150 ℃, Sleep Mode	--	--	1.5	µA
I_{DD2}	Single HV Driver Current Consumption (including support circuits), without output load	V_{DD2} = 5.0 V, T_J = -40 ℃ to 150 ℃, Static (PWM is off), including the charge pump OSC	--	--	250	µA
		V_{DD2} = 5.0 V, T_J = -40 ℃ to 150 ℃, Switching (PWM = 250 kHz)	--	344	625	µA
	All HV Drivers On Current Consumption (including support circuits), without output load	V_{DD2} = 5.0 V, T_J = -40 ℃ to 150 ℃, Static (PWM is off), including the charge pump OSC	100	--	800	µA
	Charge Pump consumption current (from V_{DD1} Pin or V_{DD2} Pin)	V_{DD2} = 5.0 V, T_J = -40 ℃ to 150 ℃, PWM is off, including the charge pump OSC	--	--	200	µA
t_{WAKE}	Wake-up time	HV SLEEP OUT high to output transition, BG is always on, Another pins SLEEP - disable	--	82.3	134.0	µs
Note 1 There is a resistive voltage divider in front of Diff Amplifier that is connected to GPO0_HD and GPO1_HD.						

3.5 Protection Circuits

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{OCP}	Overcurrent Protection Threshold	Per any HS or LS FET	--	2.18	--	A
t_{OCP1}_0	HV OUT CTRL0 OCP deglitch time	V_{DD} = 5 V, V_{DD2} = 5 V, T = 25 ºC, Deglitch = Enable, High Side	--	2.497	--	µs
		V_{DD} = 5 V, V_{DD2} = 5 V, T = 25 ºC, Deglitch = Enable, Low Side	--	1.232	--	µs
t_{OCP1}_1	HV OUT CTRL1 OCP deglitch time	V_{DD} = 5 V, V_{DD2} = 5 V, T = 25 ºC, Deglitch = Enable, High Side	--	2.497	--	µs
		V_{DD} = 5 V, V_{DD2} = 5 V, T = 25 ºC, Deglitch = Enable, Low Side	--	1.232	--	µs
t_{OCP2}_0	HV GPO0 OCP Retry Time	Delay = 492 µs	--	491	--	µs
t_{OCP2}_1	HV GPO1 OCP Retry Time	Delay = 492 µs	--	491	--	µs
t_{OCP2}_2	HV GPO2 OCP Retry Time	Delay = 492 µs	--	491	--	µs
t_{OCP2}_3	HV GPO3 OCP Retry Time	Delay = 492 µs	--	491	--	µs
T_{TSD}	Thermal shutdown temperature	Junction temperature T_J	135	141	159	℃
T_{HYST}	Thermal shutdown hysteresis		--	16	--	℃

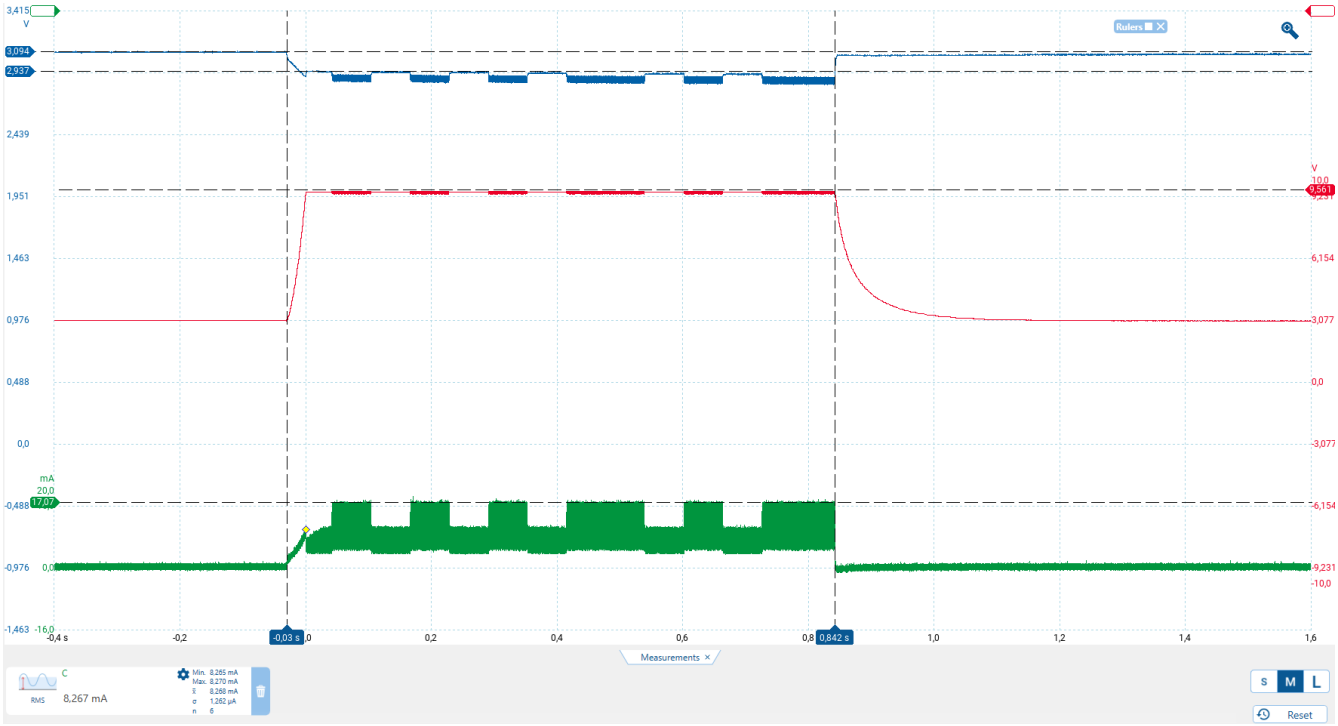
4. Functionality Waveforms

1. Whole trace operation

Channel 1 (blue/top line) – PIN# 1 (VDD)

Channel 2 (red/2nd line) – PIN# 6 (VDD2_A)

Channel 3 (green/3rd line) – current through PIN# 1 (VDD), Amperes



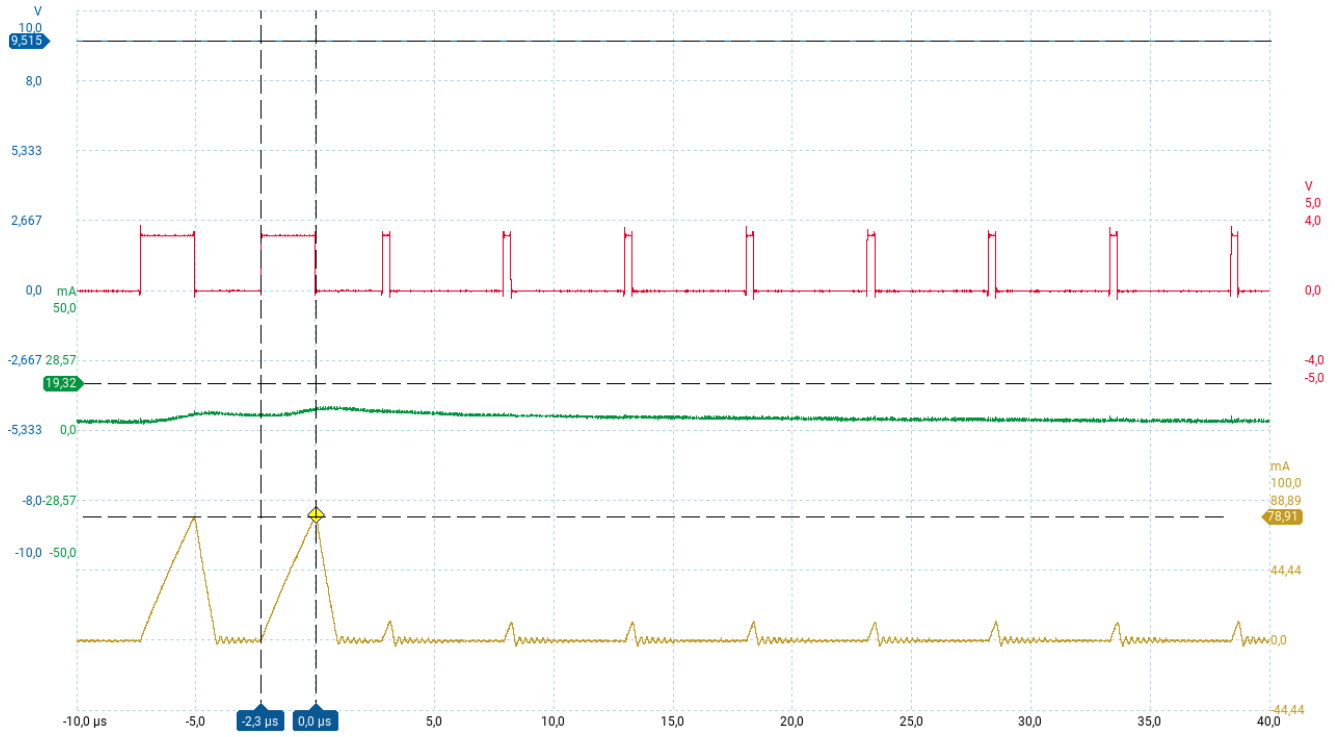
2. Maximum duty cycle

Channel 1 (blue/top line) – PIN# 6 (VDD2_A)

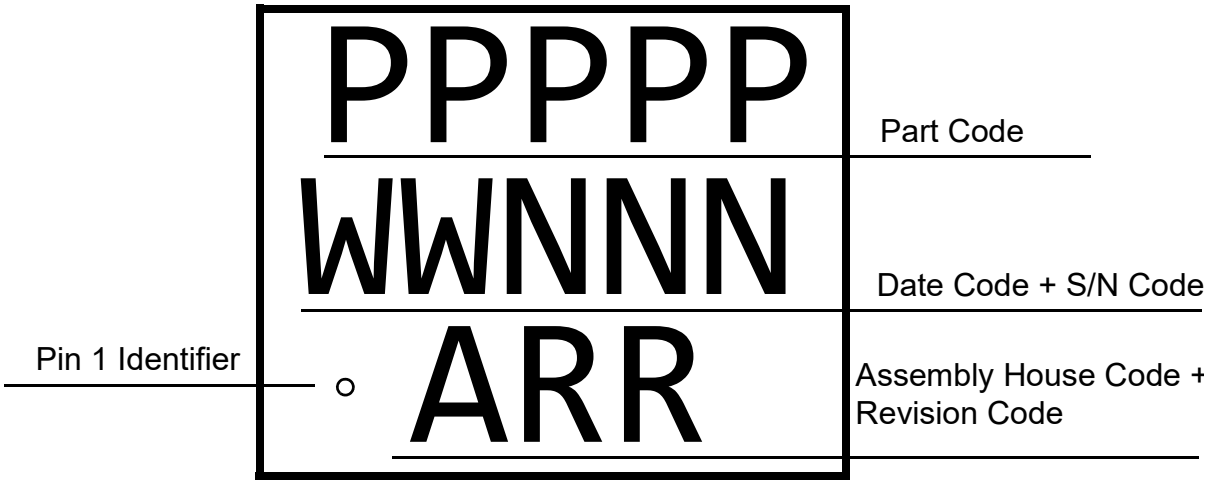
Channel 2 (red/2nd line) – PIN# 9 (BOUT1)

Channel 3 (green/3rd line) – current through PIN# 1 (VDD), Amperes

Channel 4 (yellow/4th line) – current through inductor L1, Amperes



5. Package Top Marking



Datasheet revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	002	L	0x975660ED	47748		11/13/2025

Memory Lock Options

Option	Status
Registers	All lock read/write (mode 6)

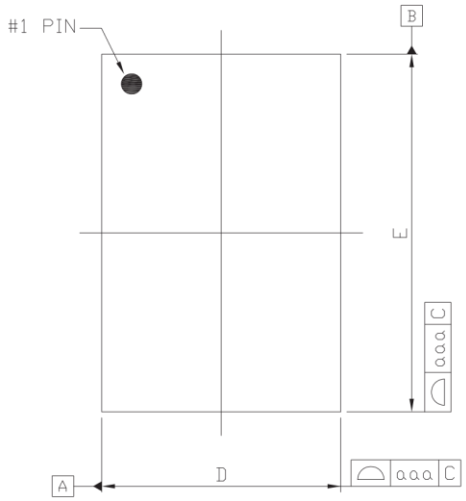
The IC security bit is locked/set for code security for production unless otherwise specified.
The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

6. Package Drawing and Dimensions

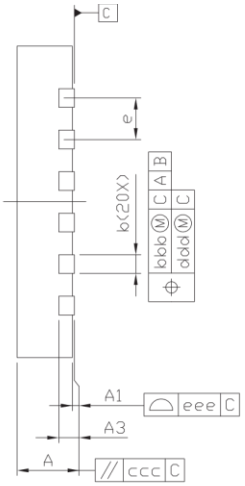
PACKAGE OUTLINES FOR STQFN 20L 2 MM X 3 MM 0.4P FCD GREEN PACKAGE

JEDEC MO-220

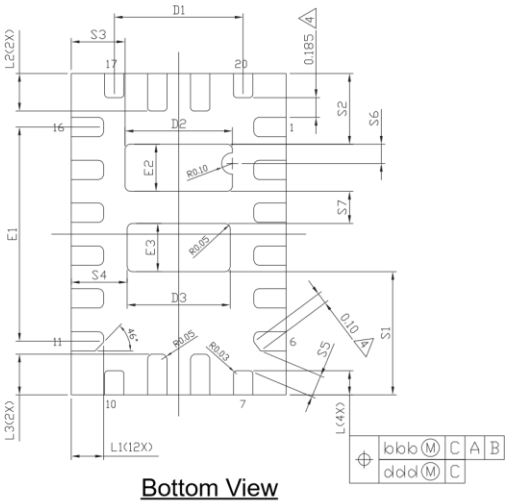
IC Net Weight: 0.008 g



Top View



Side View



Bottom View

Notes:

1. All dimensions are in millimeters.

2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

3. Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminal.

Controlling dimension: mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.95	2.00	2.05	0.077	0.079	0.081
E	2.95	3.00	3.05	0.116	0.118	0.120
D1	1.15	1.20	1.25	0.045	0.047	0.049
E1	1.95	2.00	2.05	0.077	0.079	0.081
D2	0.95	1.00	1.05	0.037	0.039	0.041
E2	0.39	0.44	0.49	0.015	0.017	0.019
D3	0.91	0.96	1.01	0.036	0.038	0.040
E3	0.40	0.45	0.50	0.016	0.018	0.020
S1	1.10	1.15	1.20	0.043	0.045	0.047
S2	0.61	0.66	0.71	0.024	0.026	0.028
S3	0.45	0.50	0.55	0.018	0.020	0.022
S4	0.47	0.52	0.57	0.018	0.020	0.022
S5	0.208 REF			0.008 REF		
S6	0.180 REF			0.007 REF		
S7	0.300 REF			0.012 REF		

“A1” max lead co-planarity 0.05 mm
Standard tolerance: ±0.05

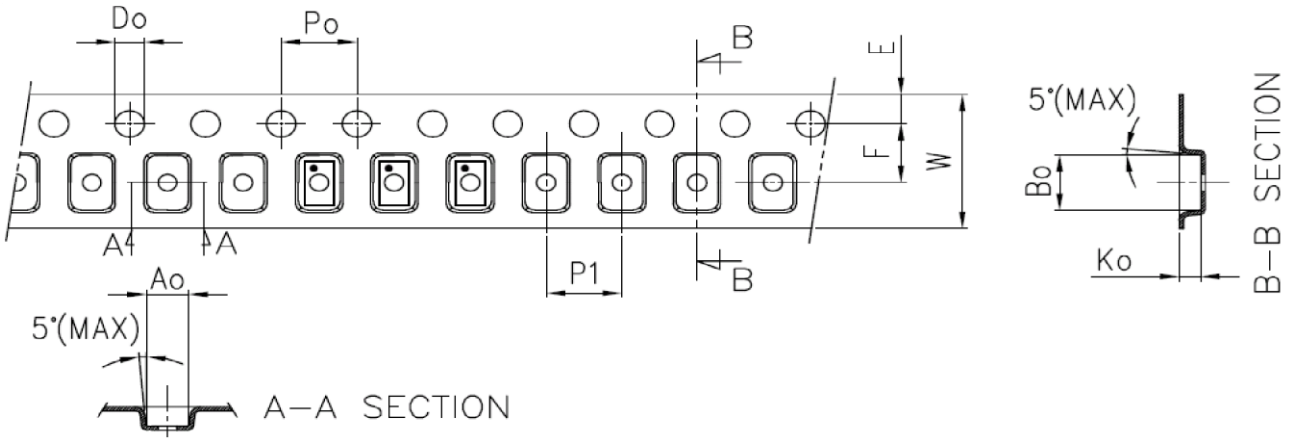
Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.250	0.300	0.350	0.010	0.012	0.014
L2	0.300	0.350	0.400	0.012	0.014	0.016
L3	0.330	0.380	0.430	0.013	0.015	0.017
b	0.130	0.180	0.230	0.005	0.007	0.009
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.1			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

7. Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 20L 2 mm x 3 mm 0.4P FCD Green	20	2.0x3.0x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2 mm x 3 mm 0.4P FCD Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

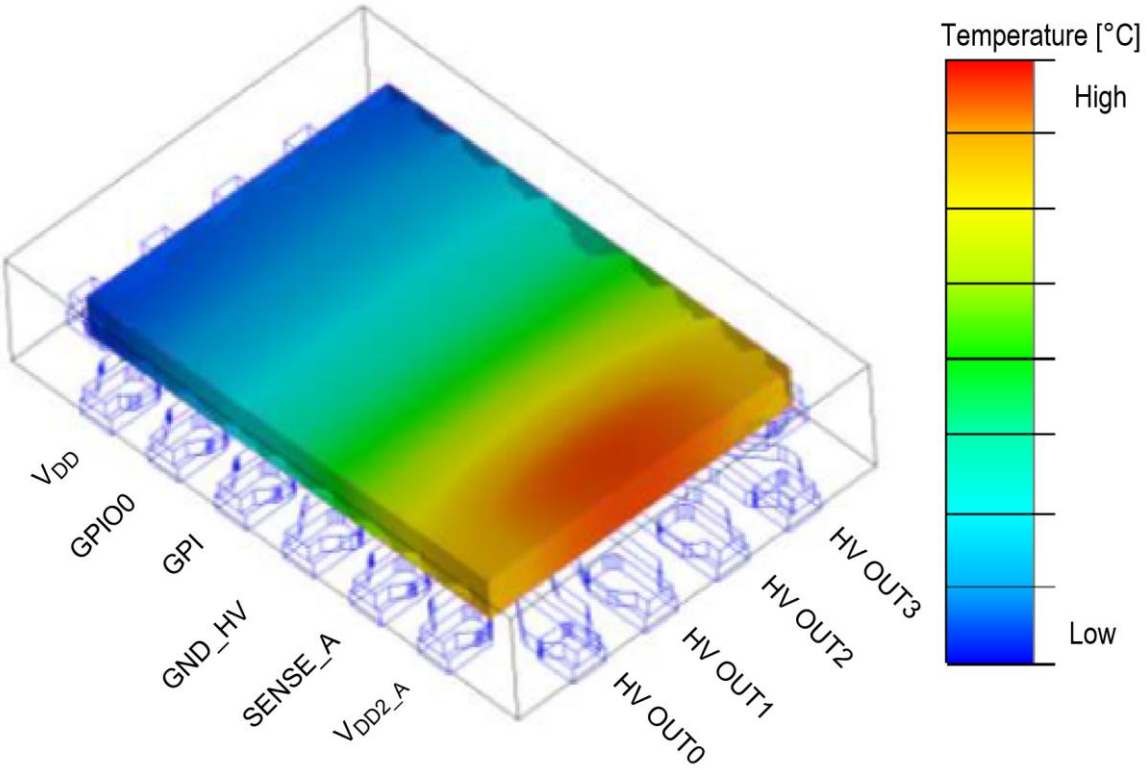
Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information.

This document can be downloaded from www.jedec.org.

8. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to 85 °C. To guarantee reliable operation, the junction temperature of the SLG7RN47748 must not exceed 150 °C.

To avoid overheating of the power MOSFETs (as shown in Figure), a good thermal design of the PCB layout must be implemented, especially when device operates near its maximum thermal limits. Refer to Section Thermal Specifications to find max value of Thermal Resistance.



Die Temperature when HV OUTs are Active

9. Layout Consideration Recommended Land Pattern

PCB should have enough ground plane to dissipate heat. SLG7RN47748 has two additional pads which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.

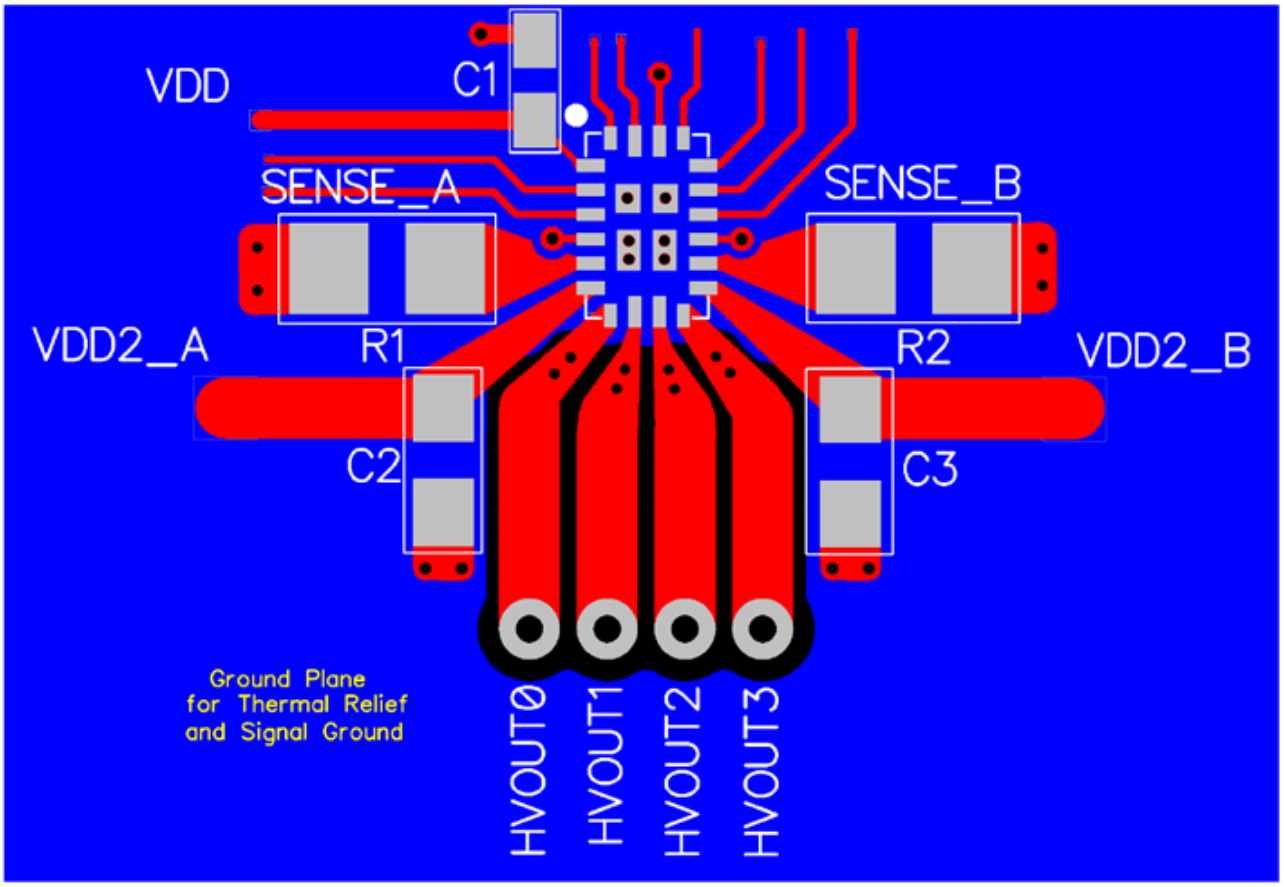
The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters.

STQFN 20L 2 MM X 3.0 MM X 0.55 MM 0.4P FCD PACKAGE

It's highly recommended to place low-ESR capacitor between VDD2_A, VDD2_B, and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it's highly recommended to place 0.1 µF ceramic capacitor between VDD and GND.

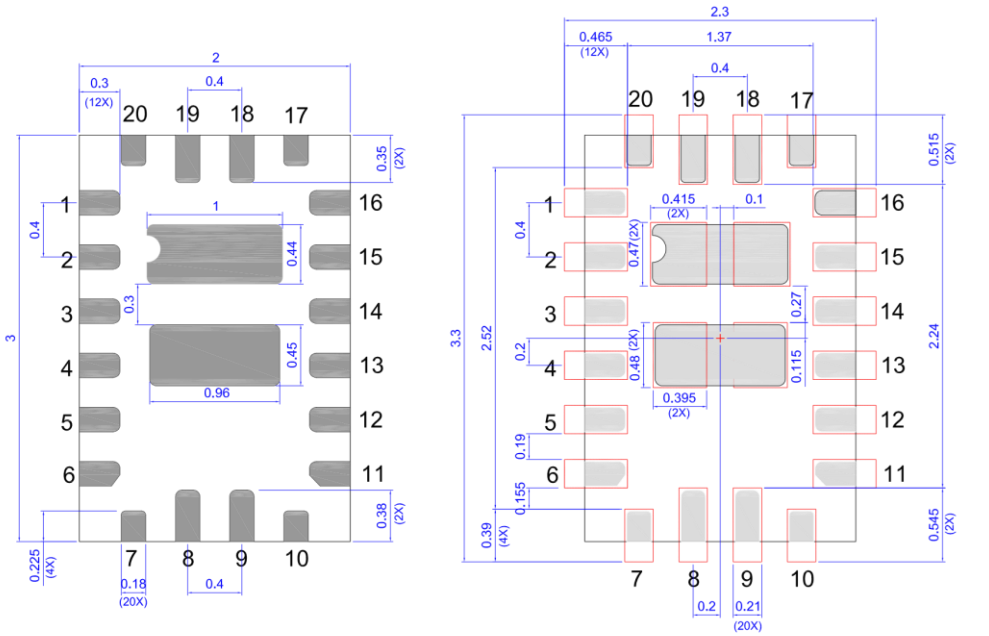
PCB Layout Example



10. Recommended Land Pattern

Expose Pad
(Package face down)

Recommended Landing Pattern
(Package face down)



Revision History

Revision	Date	Description
1.01	Nov 13, 2025	Added note in section Electrical Characteristics
1.00	Oct 17, 2025	Initial release Updated lock status Updated operating conditions Updated document template
0.13	May 20, 2025	Updated DRS Table
0.12	May 20, 2025	Design updated
0.11	Jun 12, 2024	Updated Device Revision Table
0.10	Jun 3, 2024	New design