SLG7RN47762

GreenPAK™ HART Modem Modulator/Demodulator

Description

Renesas SLG7RN47762V is HART modem. The device integrates modulation and demodulation of the HART FSK signal. The SoC is housed in a 2 mm x 2 mm STQFN package, which makes the device compact.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations visit the GreenPAK website.

Click here to download the GreenPAK file for the SLG7RN47762 design.

Email GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

- Low power consumption
- User-configurable logic
- Internal modulation/demodulation of 1200 Hz and 2200 Hz sine wave
- RoHS compliant/Halogen-free
- 16-pin STQFN: 2.0 mm x 2.0 mm x 0.55 mm, 0.4 mm pitch

Output Summary

- 2 Outputs – Open-Drain NMOS 1x
- 2 Outputs – Push-Pull 1x

1. Block Diagram

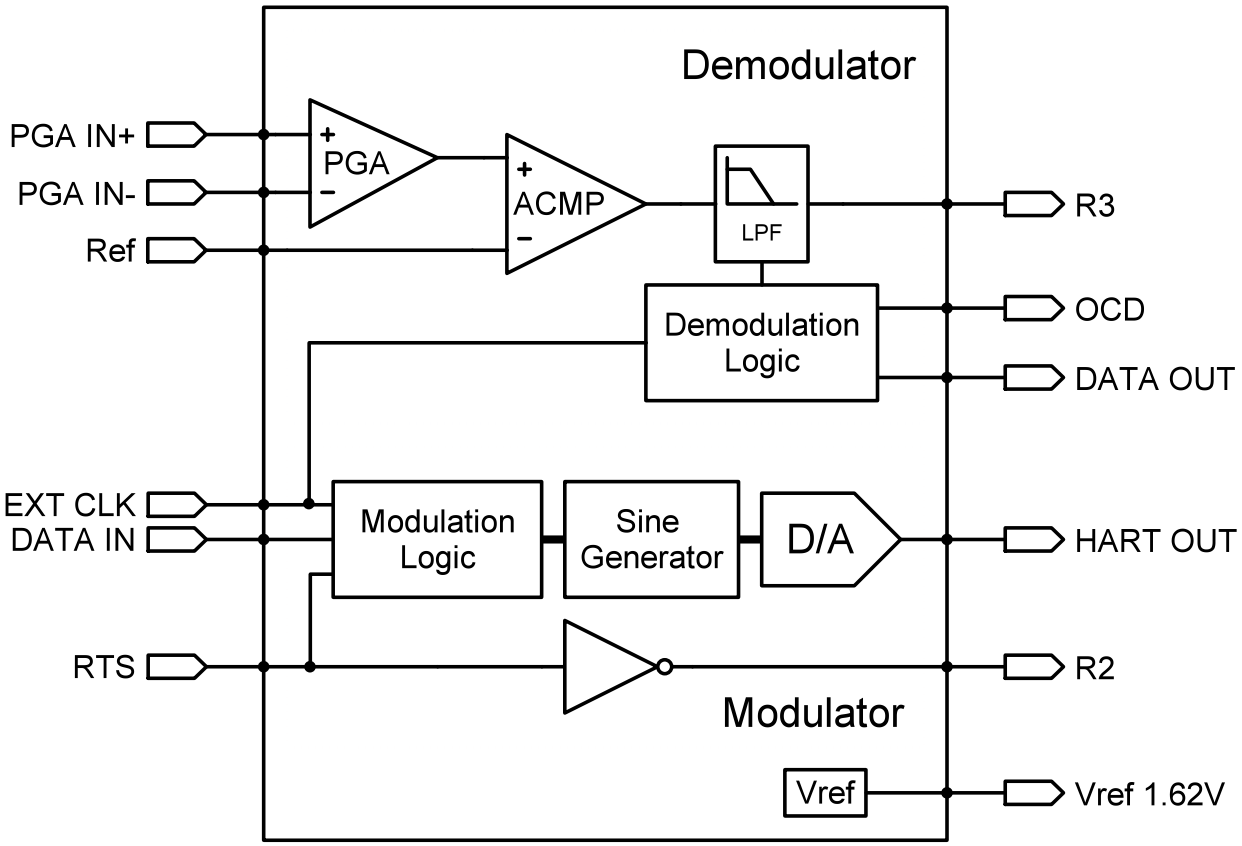
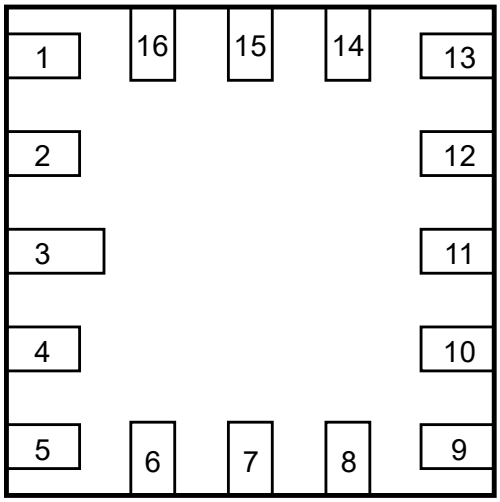


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments



STQFN-16 Pinout Diagram

(Top View)

Figure 2. Pin Assignments – Top View

2.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Number	Pin Name
1	VDD	9	NC
2	GND	10	NC
3	RTS	11	NC
4	DATA IN	12	HART OUT
5	NC	13	R3
6	OCD	14	Ref
7	EXT CLK	15	Vref 1.62V
8	DATA OUT	16	R2

Table 2. Functional Pin Description

Pin Number	Pin Name	Type	Pin Description	Internal Resistors
1	VDD	PWR	Supply Voltage	--
2	GND	GND	Ground	--
3	RTS	Digital Input	Digital Input with Schmitt trigger	floating
4	DATA IN	Digital Input	Digital Input with Schmitt trigger	floating
5	NC	--	Keep Floating or connect to GND	--
6	OCD	Digital Output	Push Pull 1X	floating
7	EXT CLK	Digital Input	Low Voltage Digital Input	floating
8	DATA OUT	Digital Output	Push Pull 1X	floating
9	NC	--	Keep Floating or connect to GND	--
10	NC	--	Keep Floating or connect to GND	--
11	NC	--	Keep Floating or connect to GND	--
12	HART OUT	Analog Input/Output	Analog Input/Output	floating
13	R3	Digital Output	Open Drain NMOS 1X	floating
14	Ref	Analog Input/Output	Analog Input/Output	floating
15	Vref 1.62V	Analog Input/Output	Analog Input/Output	floating
16	R2	Digital Output	Open Drain NMOS 1X	floating

3. Specifications

3.1 Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Supply Voltage on V_{DD} relative to GND		-0.3	4.5	V
DC Input Voltage (at any pins)		-0.3	V_{DD}+0.3, up to 4.5	V
V_{DD} DC Current		--	90	mA
GND DC Current		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	OD 1x	--	8	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value, Note 1)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitive Level		1		

Note 1: Guaranteed by design, not tested in production.

3.2 IO Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		1.71	3.30	3.60	V
Operating Temperature	T_A		-40	25	85	°C
Input Capacitor at V_{DD} pin	C_{VDD}		0.1	--	--	µF
Input Capacitance	C_{IN}	PIN 9, 12, 13, 14, 15, 16 Input Capacity on one PIN T_A = 25 °C	--	4.5	--	pF
		PIN 3, 4, 5, 6, 8, 10 Input Capacity on one PIN T_A = 25 °C	--	6.8	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs. PIN7, PIN4, PIN3 are Low	--	136	--	µA
HIGH-Level Input Voltage	V_{IH}	Logic Input with Schmitt Trigger	0.7xV_{DD}	--	--	V
		Low-Level Logic Input (Note 1)	0.9	--	--	V
LOW-Level Input Voltage	V_{IL}	Logic Input with Schmitt Trigger	--	--	0.3xV_{DD}	V
		Low-Level Logic Input (Note 1)	--	--	0.3	V
HIGH-Level Output Voltage	V_{OH}	Push-Pull 1X, V_{DD} = 1.8 V ± 5 %, I_{OH} = 100 µA	0.994xV_{DD}	--	--	V
		Push-Pull 1X, V_{DD} = 1.8 V ± 5 %, I_{OH} = 2 mA	0.895xV_{DD}	--	--	V
		Push-Pull 1X, V_{DD} = 2.5 V ± 10 %, I_{OH} = 100 µA	0.996xV_{DD}	--	--	V
		Push-Pull 1X, V_{DD} = 2.5 V ± 10 %, I_{OH} = 2 mA	0.940xV_{DD}	--	--	V
		Push-Pull 1X, V_{DD} = 3.3 V ± 10 %, I_{OH} = 100 µA	0.999xV_{DD}	--	--	V
		Push-Pull 1X, V_{DD} = 3.3 V ± 10 %, I_{OH} = 2 mA	0.983xV_{DD}	--	--	V
LOW-Level Output Voltage	V_{OL}	Push-Pull 1X, V_{DD} = 1.8 V ± 5 %, I_{OL} = 100 µA	--	--	0.002xV_{DD}	V
		Push-Pull 1X, V_{DD} = 1.8 V ± 5 %, I_{OL} = 2 mA	--	--	0.047xV_{DD}	V
		Push-Pull 1X, V_{DD} = 2.5 V ± 10 %, I_{OL} = 100 µA	--	--	0.002xV_{DD}	V
		Push-Pull 1X, V_{DD} = 2.5 V ± 10 %, I_{OL} = 2 mA	--	--	0.028xV_{DD}	V
		Push-Pull 1X, V_{DD} = 3.3 V ± 10 %, I_{OL} = 100 µA	--	--	0.001xV_{DD}	V
		Push-Pull 1X, V_{DD} = 3.3 V ± 10 %, I_{OL} = 2 mA	--	--	0.019xV_{DD}	V
		Open Drain NMOS 1X, V_{DD} = 1.8 V ± 5 %, I_{OL} = 100 µA	--	--	0.004xV_{DD}	V
		Open Drain NMOS 1X, V_{DD} = 1.8 V ± 5 %, I_{OL} = 2 mA	--	--	0.077xV_{DD}	V
		Open Drain NMOS 1X, V_{DD} = 2.5 V ± 10 %, I_{OL} = 100 µA	--	--	0.002xV_{DD}	V
		Open Drain NMOS 1X, V_{DD} = 2.5 V ± 10 %, I_{OL} = 2 mA	--	--	0.045xV_{DD}	V
		Open Drain NMOS 1X, V_{DD} = 3.3 V ± 10 %, I_{OL} = 100 µA	--	--	0.002xV_{DD}	V
		Open Drain NMOS 1X, V_{DD} = 3.3 V ± 10 %, I_{OL} = 2 mA	--	--	0.029xV_{DD}	V
HIGH-Level Output Pulse Current (Note 2)	I_{OH}	Push-Pull 1X, V_{DD} = 1.8 V ± 5 %, V_{OH} = V_{DD} x 0.8	2.96	--	--	mA
		Push-Pull 1X, V_{DD} = 2.5 V ± 10 %, V_{OH} = V_{DD} x 0.8	5.13	--	--	mA
		Push-Pull 1X, V_{DD} = 3.3 V ± 10 %, V_{OH} = V_{DD} x 0.8	8.41	--	--	mA
LOW-Level Output Pulse Current	I_{OL}	Push-Pull 1X, V_{DD} = 1.8 V ± 5 %, V_{OL} = V_{DD} x 0.2	5.27	--	--	mA
		Push-Pull 1X, V_{DD} = 2.5 V ± 10 %, V_{OL} = V_{DD} x 0.2	9.09	--	--	mA
		Push-Pull 1X, V_{DD} = 3.3 V ± 10 %, V_{OL} = V_{DD} x 0.2	14.48	--	--	mA
		Open Drain NMOS 1X, V_{DD} = 1.8 V ± 5 %, V_{OL} = V_{DD} x 0.1, PINs 13, 16	3.81	--	--	mA
		Open Drain NMOS 1X, V_{DD} = 2.5 V ± 10 %, V_{OL} = V_{DD} x 0.1, PINs 13, 16	6.50	--	--	mA
		Open Drain NMOS 1X, V_{DD} = 3.3 V ± 10 %,	10.28	--	--	mA

		V_{OL} = V_{DD} x 0.1, PINs 13, 16				
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR} OTP load including SRAM	--	4.2	--	ms
		From V_{DD} rising past PON_{THR} OTP load excluding SRAM	--	1.7	--	ms
		Transition from Sleep mode to All ON mode, OTP load including SRAM	--	3.8	--	ms
		Transition from Sleep mode to All ON mode, OTP load excluding SRAM	--	1.4	--	ms
		Transition from Retention mode to All ON mode	--	0.4	--	ms
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip	1.44	1.50	1.56	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip	0.66	0.70	0.72	V
External Clock Frequency (to PIN7)	FIN		-1%	4	+1%	MHz
Note 1: No hysteresis. **Note 2:** DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

4. Description

HART modem based on the SLG7RN47762V IC combines both current loop signal modulation and demodulation. The SLG7RN47762V can also act as both a host and a field device with minor circuit modifications.

The SLG7RN47762V includes a built-in DAC for generating sine waves on the current loop without phase shifts. Also, it contains all the necessary digital blocks for decoding the sine wave back into UART.

4.1 Modulation

Modulation begins when the RTS signal goes low and ends when RTS goes high. In the device receiving data, RTS should be high. After RTS goes low, the internal DAC starts modulating the HART OUT signal according to the DATA IN input.

4.2 Demodulation

Demodulation starts as soon as the SLG7RN47762V detects a 1200/2200 Hz signal with V_{IN} > 120 mV peak-to-peak on the line (in turn, sine signal with amplitude V_{IN} < 80 mV peak-to-peak will be ignored). The signal is fed to the PGA IN+ and PGA IN- pins and compared with the reference voltage on the Ref pin. Then, using the internal blocks, the frequency of the sine wave is determined and decoded into 1 and 0, where 1 is 1200 Hz and 0 is 2200 Hz. The start of data receiving is indicated by the OCD signal, which goes high at the beginning of data receiving and goes low at the end.

4.3 Application Description

For correct operation and compliance with HART specifications, the circuit includes an active filter that attenuates signals that do not correspond to 1200-2200 Hz. This allows to prevent noise in the current loop from affecting the correct demodulation of packets. The circuit features also hysteresis, to adjust the receive/reject threshold, which is controlled by resistors R3, R4, and R5.

Note: SLG7RN47762 goes in pair with SLG7RN48069, which is used for the analog front-end.

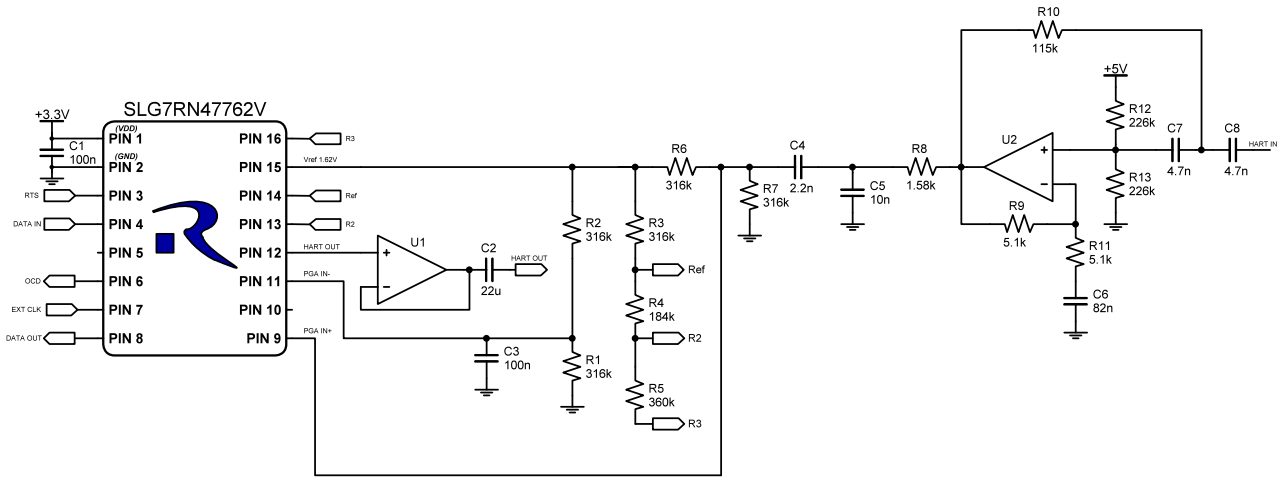


Figure 3. Typical Application Circuit

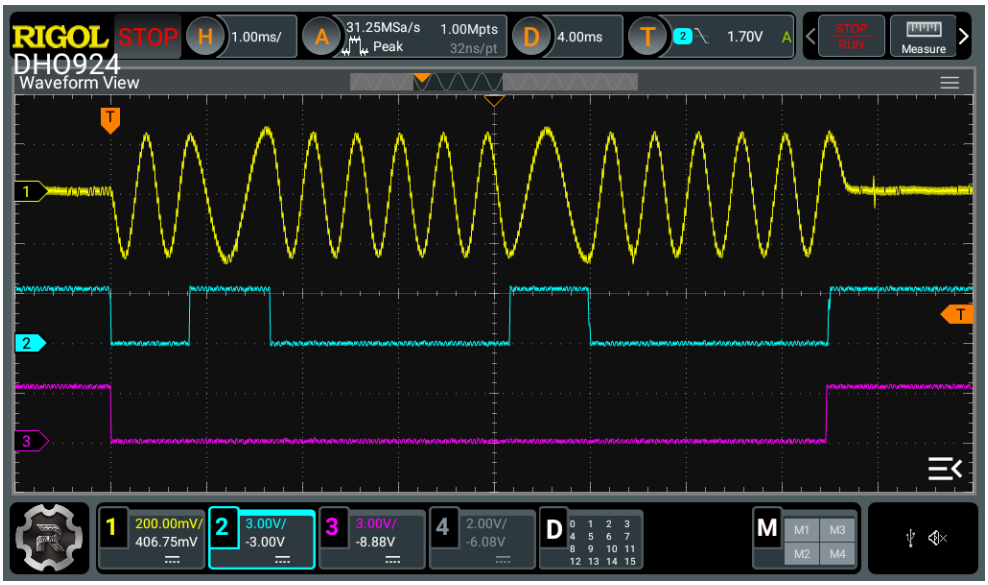
4.3.1 Functionality Waveforms

Channel 1 (yellow/top line) – HART IN.

Channel 2 (light blue/2nd line) – PIN 4 (DATA IN).

Channel 3 (magenta/3rd line) – PIN 3 (RTS).

1.Sending data to the current loop (Data is 0x11)

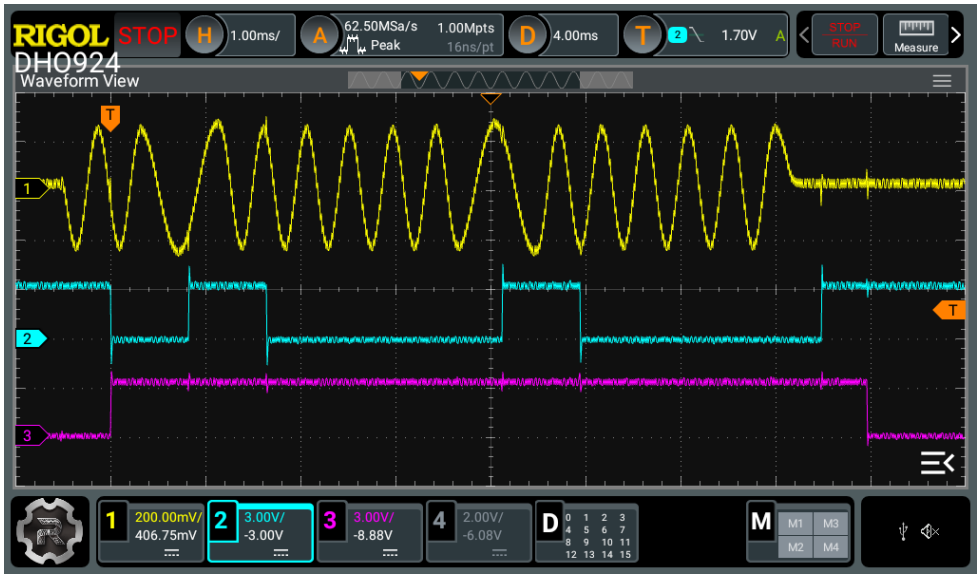


Channel 1 (yellow/top line) – HART IN.

Channel 2 (light blue/2nd line) – PIN 8 (DATA OUT).

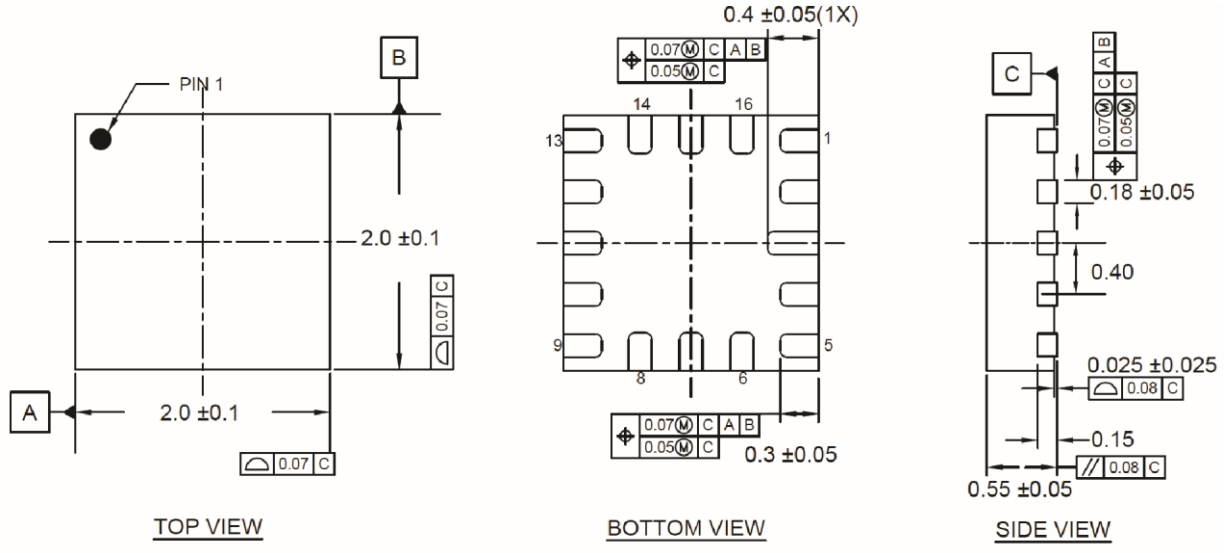
Channel 3 (magenta/3rd line) – PIN 6 (OCD).

2. Receiving data from the current loop


RIGOL
STOP
DHO924
Waveform View
1.00ms/
62.50MSa/s
Peak
1.00Mpts
16ns/pt
4.00ms
1.70V
STOP
RUN
Measure
200.00mV/
406.75mV
3.00V/
-3.00V
3.00V/
-8.88V
2.00V/
-6.08V
M1
M3
M2
M4

5. Package Information

5.1 Package Outline Drawing for STQFN-24 (3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) WB



Note 1: JEDEC compatible.

Note 2: All dimensions are in mm and angles are in degrees.

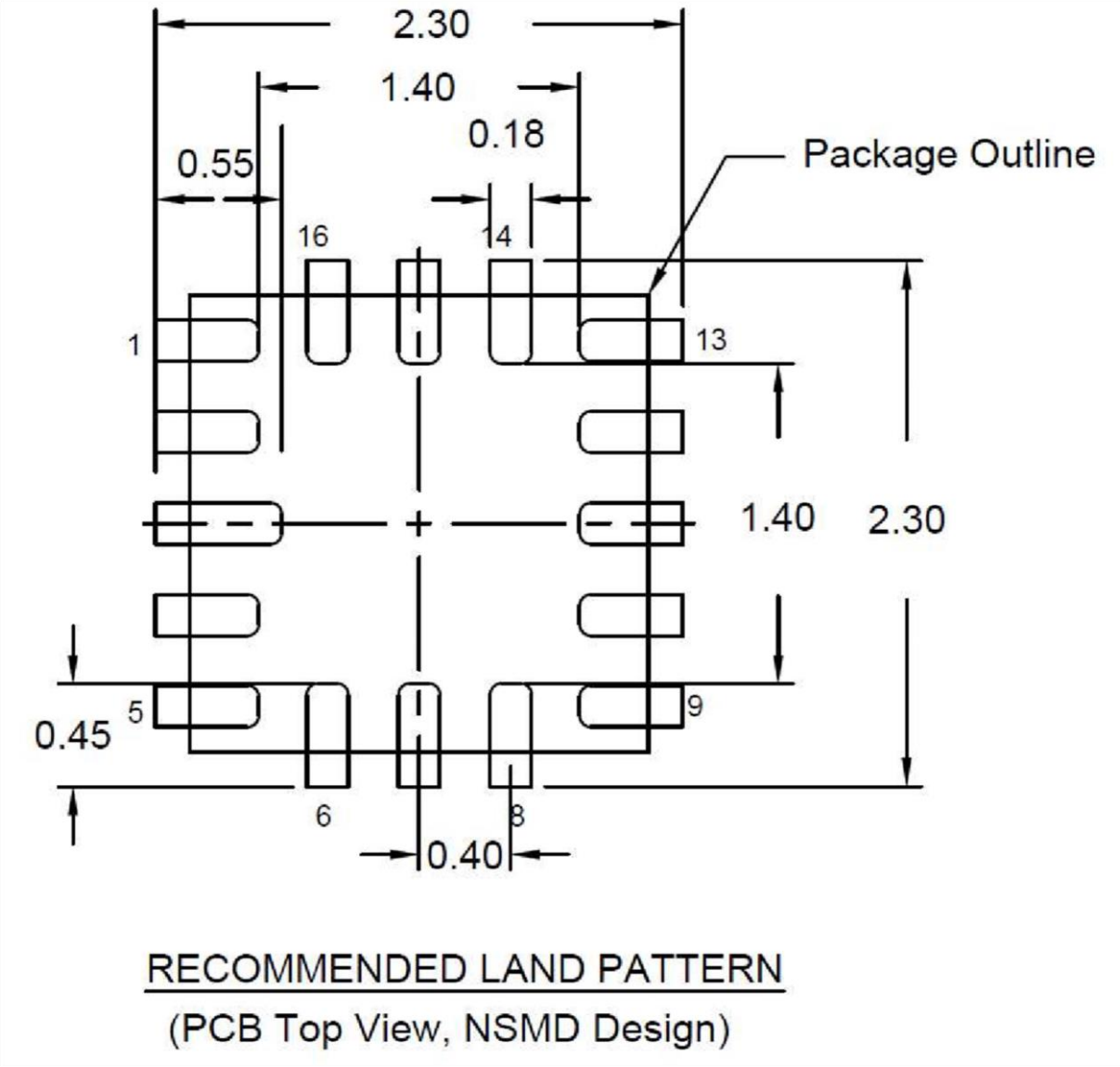
Note 3: Use ±0.05 mm for the non-tolerance dimensions.

Note 4: Numbers in ( ) are for reference only.

5.2 Recommended Reflow Soldering Profile

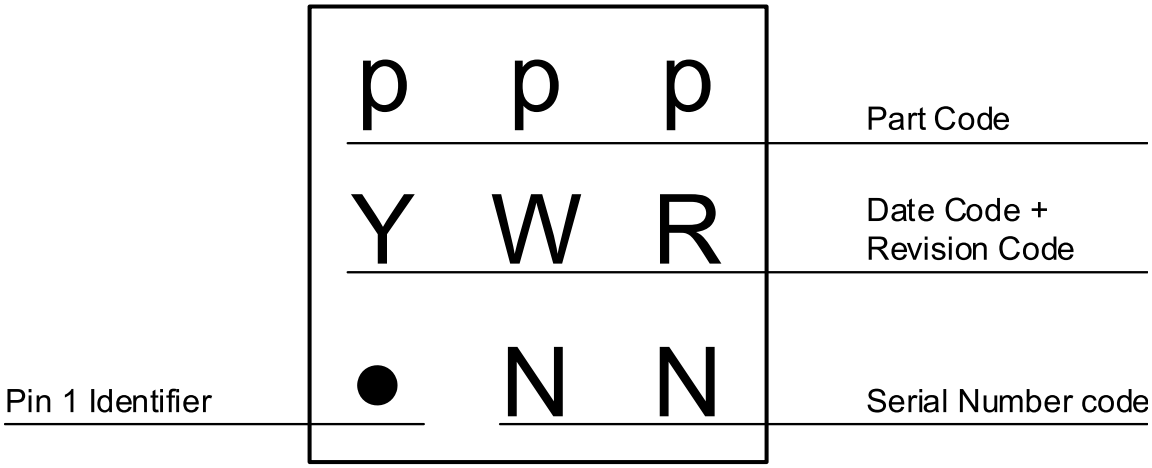
Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from www.jedec.org.

5.3 Layout Guidelines



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

6. Marking Diagram



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	002	L	0xC96D32E2	1LF	B	07/03/2025

Table 3. Memory Lock Options

Option	Status
Registers	Lock read and write
NVM	Lock read and write
Protect entire lock configuration	Disabled

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

7. Ordering Information

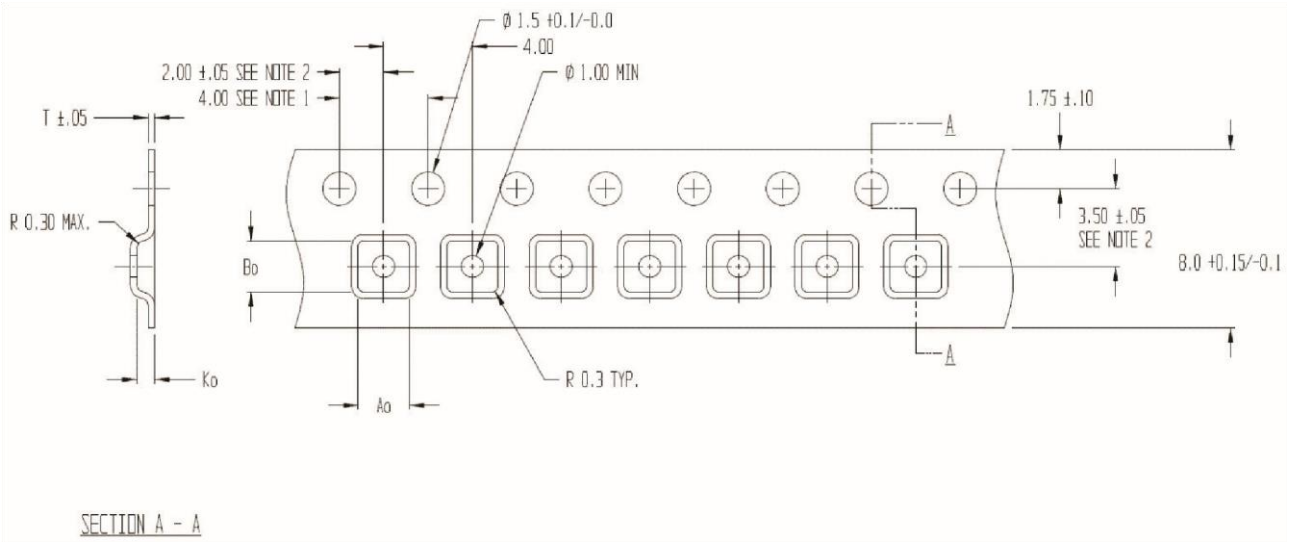
Part Number	Package Description
SLG7RN47762V	16-pin STQFN - Tape and Reel (3k units)

7.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units per Reel	Reel Diam. [mm]	Leader [min]		Trailer [min]		Tape Width [mm]	Part Pitch [mm]
					Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 2.0 mm x 2.0 mm 0.4P FC Green	16	2 x 2 x 0.6	3000	178	100	400	100	400	8	4

7.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 2.0 mm x 2.0 mm 0.4P FC Green	2.30	2.30	0.80	4.00	4.00	1.5	1.75	3.5	8



8. Revision History

Revision	Date	Description
1.02	Nov 5, 2025	Reformatted according to Renesas template
1.01	Jun 3, 2025	Updated name and description of the Datasheet
1.00	May 29, 2025	Production Release
0.15	May 28, 2025	Updated Device Revision Table
0.14	May 20, 2025	Locked design
0.13	May 7, 2025	Added the Block Diagram
0.12	Dec 11, 2024	Updated Device Revision Table
0.11	Dec 11, 2024	Changed PGA Gain
0.10	Jun 6, 2024	New Design