General Description

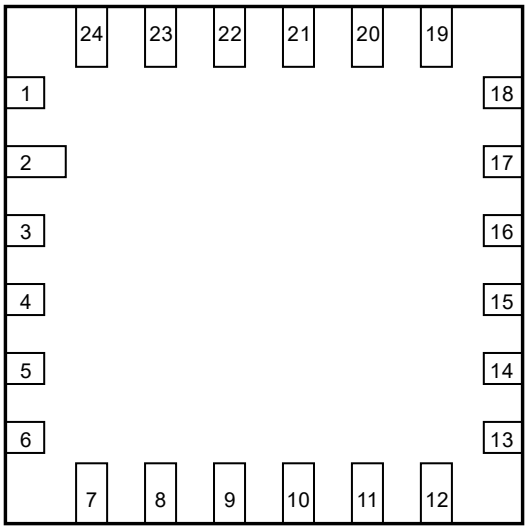
Overview

Renesas SLG7RN48069 is a low power and small form device. The SoC is housed in a 3mm x 3mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- RoHS Compliant / Halogen-Free
- 24-pin STQFN: 3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch
- SLG7RN48069 works in pair with HART Modem Modulator/Demodulator based on SLG7RN47762

Pin Configuration



STQFN-24

(Top View)

Pin Name

Pin #	Pin name	Pin #	Pin name
1	NC	13	NC
2	NC	14	NC
3	NC	15	GND
4	VDDA	16	VDD
5	NC	17	NC
6	NC	18	NC
7	FILTER IN+	19	RX_SIN_OUT_B(OUT)
8	FILTER IN-	20	NC
9	FILTER OUT	21	SDA
10	BUFFER OUT	22	SCL
11	BUFFER IN-	23	NC
12	BUFFER IN+	24	RX_SIN_OUT_B(IN)

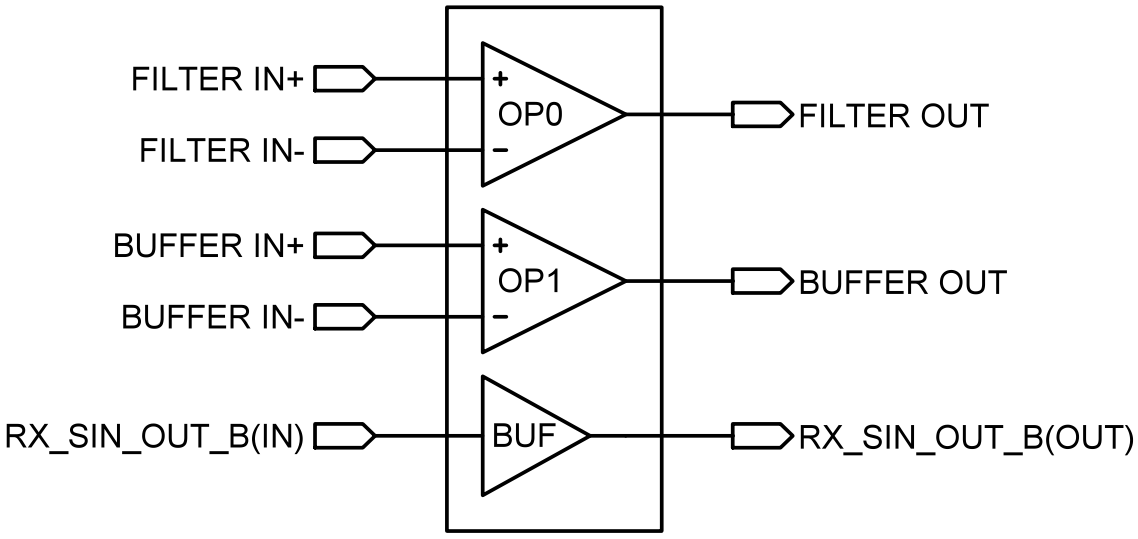
Pin Configuration

Pin	Pin Name	Type	Pin Description	Internal Resistors
1	NC	--	Keep Floating or connect to GND	--
2	NC	--	Keep Floating or connect to GND	--
3	NC	--	Keep Floating or connect to GND	--
4	VDDA	APWR	Analog Power Supply	--
5	NC	--	Keep Floating or connect to GND	--
6	NC	--	Keep Floating or connect to GND	--
7	FILTER IN+	Analog Input/Output	Analog Input/Output	floating
8	FILTER IN-	Analog Input/Output	Analog Input/Output	floating
9	FILTER OUT	Analog Input/Output	Analog Input/Output	floating
10	BUFFER OUT	Analog Input/Output	Analog Input/Output	floating
11	BUFFER IN-	Analog Input/Output	Analog Input/Output	floating
12	BUFFER IN+	Analog Input/Output	Analog Input/Output	floating
13	NC	--	Keep Floating or connect to GND	--
14	NC	--	Keep Floating or connect to GND	--
15	GND	GND	Ground	--
16	VDD	PWR	Supply Voltage	--
17	NC	--	Keep Floating or connect to GND	--
18	NC	--	Keep Floating or connect to GND	--
19	RX_SIN_OUT_B(OUT)	Analog Input/Output	Analog Input/Output	floating
20	NC	--	Keep Floating or connect to GND	--
21	SDA	Digital Input	Digital Input with Schmitt trigger	floating
22	SCL	Digital Input	Digital Input with Schmitt trigger	floating
23	NC	--	Keep Floating or connect to GND	--
24	RX_SIN_OUT_B(IN)	Analog Input/Output	Analog Input/Output	floating

Ordering Information

Part number	Package type
SLG7RN48069V	24-pin STQFN - Tape and Reel (TBD units)

Block Diagram



Absolute Maximum Conditions

Parameter		Min	Max	Unit
V_{DD} and V_{DDA} Voltage to GND		-0.5	7.0	V
DC Input Voltage	GPI0, GPIOs 0, 1, 2, 3, 6, 7, 8, 9	-0.5	V_{DD} + 0.5, up to 7.0	V
	GPIOs 4, 5	-0.5	7.0	
	OA0+, OA0-, OA0_OUT, OA1+, OA1-, OA1_OUT, RH0_A/GPI1, RH0_B/GPI2, RH1_A/GPI4, RH1_B/GPI3	-0.5	V_{DDA} + 0.5, up to 7.0	
V_{DD} DC Current (Note 1)		--	90	mA
V_{DDA} DC Current (Note 1)		--	180	mA
GND DC Current (Note 1)		--	145	mA
GPIO DC Current (Note 1)	Analog Switch Mode	--	130	mA
Logic Input Pin Current		--	1	mA
Input Leakage Current (Depends on the kind of GPIOs, Note 2)		10	30	nA
Storage Temperature Range		-65	+150	°C
Junction Temperature		--	+150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Thermal Resistance		--	79.7	°C/W
Moisture Sensitive Level		1		

Note 1: Continuous operation at T_J = +110 ºC
Note 2: For more details please see the official datasheet

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	V_{DD} Supply Voltage Range		2.4	3.4	5.5	V
V_{DDA}	V_{DDA} Supply Voltage Range		2.4	3.4	5.5	V
T_A	Operating Ambient Temperature Range		-40	25	85	°C
C_{VDD}	Input Capacitor at V_{DD} and V_{DDA} Pins		0.1	--	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PIN7, PIN12, PIN24 are Low; PIN21-22, PIN8, PIN11 are High	--	40	--	µA
V_{IH}	HIGH-level Input Voltage	Logic Input with Schmitt Trigger	0.7xV_{DD}	--	--	V
V_{IL}	LOW-level Input Voltage	Logic Input with Schmitt Trigger	--	--	0.3xV_{DD}	V
t_{SU}	Startup Time	From V_{DD} rising past V_{TH_PON}, V_{DD} Slew-rate < 1 V/ms	--	4.4	6.3	ms
		From V_{DD} rising past V_{TH_PON}, V_{DD} Slew-rate ≥ 1 V/ms	--	2.5	4.0	ms
V_{TH_PON}	Power-on Threshold	V_{DD} required to start up the device	1.62	1.84	2.05	V
V_{TH_POFF}	Power-off Threshold	V_{DD} to turn off the device	1.02	1.34	1.60	V

Operational Amplifier Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Input Voltage Range			2.3	--	5.5	V
GBP	Gain Bandwidth Product	f = 50 kHz, R_{LOAD} = 10 kΩ to V_{CM}		--	400	--	kHz
V_{OS}	Input Offset Voltage	T_A = +25 °C		-9	-3	9	µV
		T_A = -40 °C to +85 °C		-15	--	15	µV
V_{CMR}	Common-mode Input Voltage Range			-0.1	--	5.1	V
CMRR	Common-mode Rejection Ratio	V_{CM} = -0.1 V to 5.0 V	T_A = +25 °C	112	125	--	dB
			T_A = -40 °C to +85 °C	109	--	--	dB
PSRR	Power Supply Rejection Ratio	V_{DDA} = 2.3 V to 5.1 V	T_A = +25 °C	117	130	--	dB
			T_A = -40 °C to +85 °C	115	--	--	dB
I_B	Input Bias Current	T_A = +25 °C		-340	±30	440	pA
I_{OFFSET}	Input Offset Current	T_A = +25 °C		--	160	--	pA
R_{CM}	Common-mode Input Resistance			--	10	--	GΩ
R_{DIFF}	Differential-mode Input Resistance			--	10	--	GΩ
A_{OL}	Open Loop Gain	R_{LOAD} = 1 MΩ		--	152	--	dB
SR+	Positive Slew Rate	V_{OAx_OUT} = 1 V to 4 V, A_V = 1, R_{LOAD} = 10 kΩ		--	160	--	mV/µs
SR-	Negative Slew Rate	V_{OAx_OUT} = 1 V to 4 V, A_V = 1, R_{LOAD} = 10 kΩ		--	100	--	mV/µs

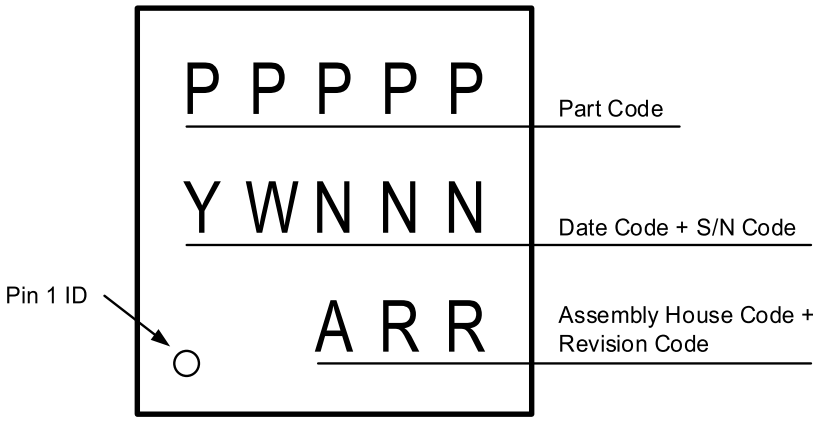
I²C Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	Clock Frequency, SCL		--	--	1000	kHz
t_{LOW}	Clock Pulse Width, LOW		500	--	--	ns
t_{HIGH}	Clock Pulse Width, HIGH		260	--	--	ns
t_{AA}	Clock LOW to Data Out Valid		--	--	450	ns
t_{BUF}	Bus Free Time between STOP and START		500	-	--	ns
t_{HD_STA}	Start Hold Time		260	--	--	ns
t_{SU_STA}	Start Set-up Time		260	--	--	ns
t_{HD_DAT}	Data Hold Time	Logic Input with Schmitt Trigger	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	Logic Input with Schmitt Trigger	100	--	--	ns
t_R	Inputs Rise Time		--	--	120	ns
t_F	Inputs Fall Time		--	--	120	ns
t_{SU_STO}	STOP Set-up Time		260	--	--	ns
t_{DH}	Data Out Hold Time		50	--	--	ns

Chip Address

HEX	BIN	DEC
0x08	0001000	8

Package Top Marking



Datasheet revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	001	L	0xFDB5E415	48069	AB	07/03/2025

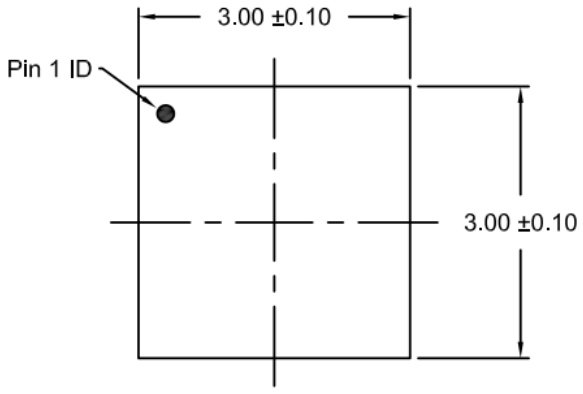
Memory Lock Options

Option	Status
Registers	All lock read/write (mode 6)

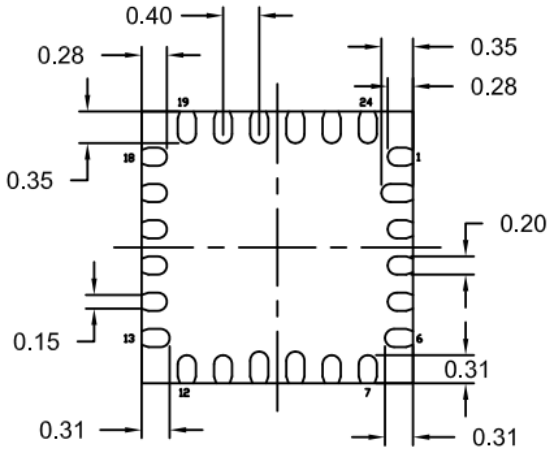
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

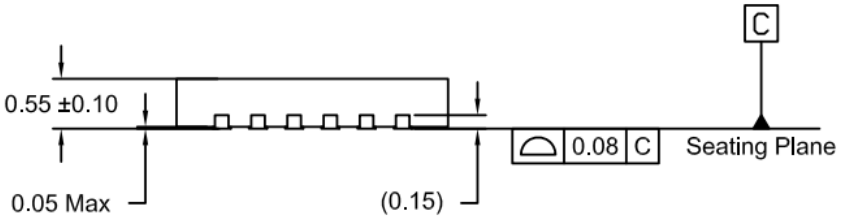
STQFN-24 (3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm Pitch) WB



TOP VIEW



BOTTOM VIEW



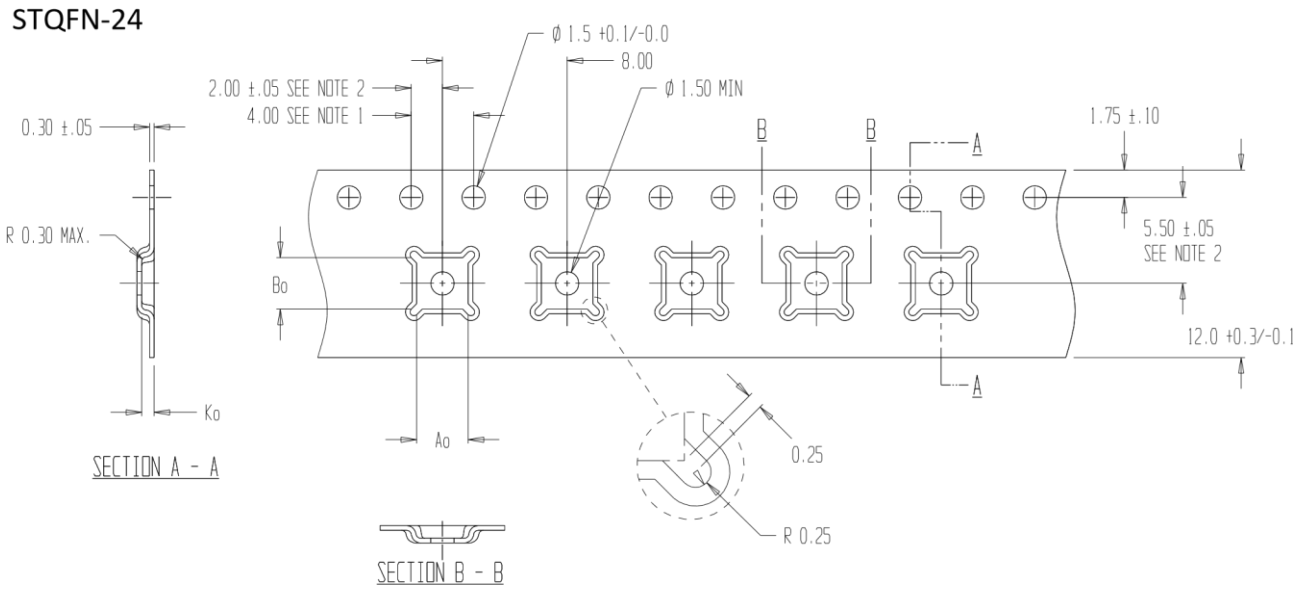
SIDE VIEW

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN-24	24	3.0 x 3.0 x 0.55	5,000	5,000	330/102	42	336	42	336	12.5	8.0

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN-24	3.3 ± 0.1	3.3 ± 0.1	0.75 ± 0.05	4.0 ± 0.1	4.0 ± 0.1	1.5 +0.1 / -0.0	1.75 ± 0.1	5.5 ± 0.05	12.15 ± 0.1



Recommended Reflow Soldering Profile

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from www.jedec.org.

Layout Consideration

The SLG7RN48069 has two supply input pins (V_{DD} and V_{DDA}) and one ground pin (GND) as analog and digital ground signals are internally connected. Separating the analog supply voltage (V_{DDA}) from the digital supply (V_{DD}) helps to minimize cross-coupling of noise generated by the digital part of the device.

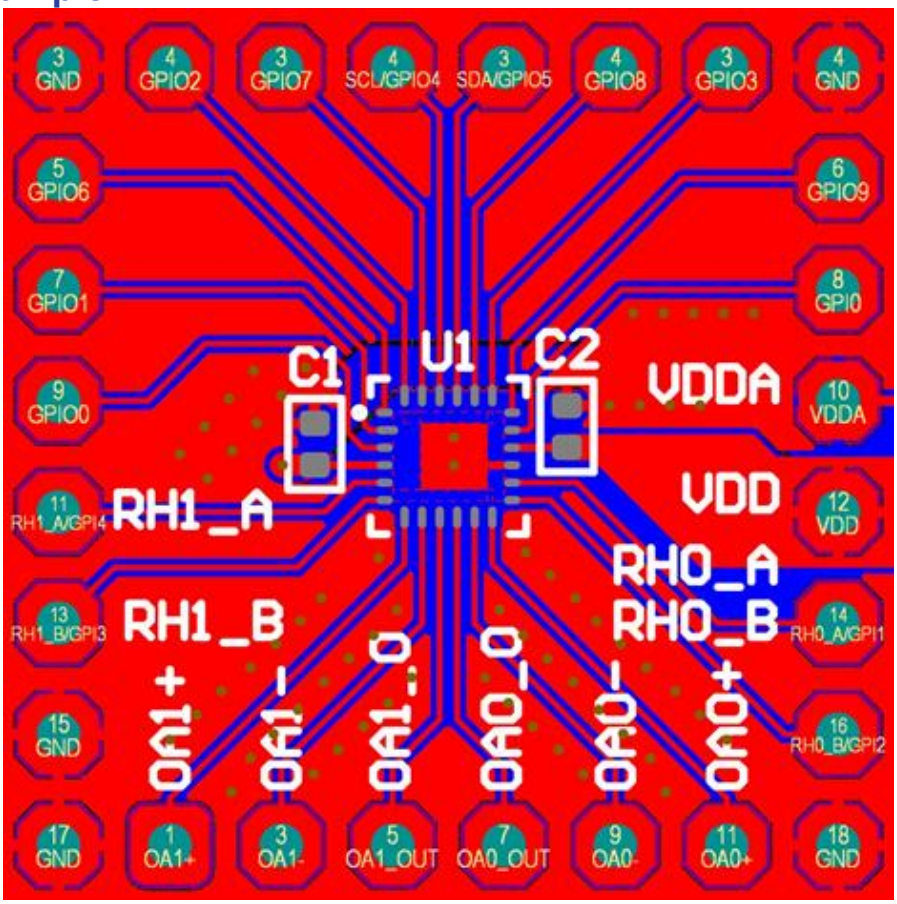
- Analog (V_{DDA}) Domain: Operational Amplifiers, bias generators (for V_{REF} of OpAmp and MS-ACMP), V_{REF} of OpAmp, digital rheostats, and low-power bandgap.
- Digital (V_{DD}) Domain: MS-ACMP (Chopper ACMP), V_{REF} of MS-ACMP, TS_OUT buffer, sink/source buffer, analog switch, OSC0 (2 kHz/10 kHz), OSC1 (25 MHz), I^2C macrocell, the NVM logic, multi-function macrocells, and combination-function macrocells.

It is strongly recommended to connect unused digital input pins to GND.

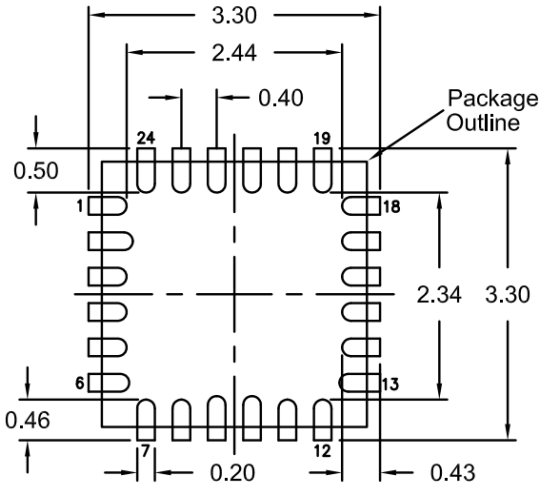
The following suggestions allow to minimize the impacts of the digital domain noise onto the analog domain:

- Decrease the slew-rate of digital input signals if possible.
- Use proper grounding scheme with bypass capacitors on V_{DDA} and V_{DD} pins.
- Assign GPIO0 – GPIO9 for digital signals first, then use other pins in case more digital IOs are needed.

PCB Layout Example



Recommended Land Pattern



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Datasheet Revision History

Date	Version	Change
12/11/2024	0.10	New Design
12/11/2024	0.11	Updated Device Revision Table
05/13/2025	0.12	Added the Block Diagram Updated Lock Status
05/15/2025	0.13	Updated Electrical Characteristics Table
05/22/2025	0.14	Updated Device Revision Table
05/23/2025	1.00	Production Release
07/03/2025	1.01	Updated name and description of the Datasheet