SLG7SQ47664

Low Power Compact Sequencer

The SLG7SQ47664 is a compact, single-channel low power simple sequencer IC. It features configurable time delays and trigger thresholds, ensuring accurate power-up sequencing across many applications.

PIN9 is an open-drain output stage, with active high (ENOUT) and PIN10 has an active low ($\overline{\text{ENOUT}}$) output. Both have open-drain output stages that can be pulled up to voltage levels as high as V_{DD} + 0.5 V through an external resistor, which increases compatibility with enable input logic levels of different regulators and converters. There is a dedicated enable pin allowing the outputs to be controlled externally.

Both delay time and trigger threshold can be configured via I^2C. The default delay time is configured to 10.25 ms but can be configured between 976.56 µs – 125 ms. The default threshold is set to 608 mV but can be configured between 32 mV and 2.016 V in 32 mV steps. The IC is housed in a 1.6 mm x 1.6 mm STQFN package for seamless integration into any board design.

Note: The device will reset to the default values on power-up and will need to be configured through I^2C to change V_{th} and delay time to the device RAM. After power cycle, it will reset to pre-programmed value.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations, visit the GreenPAK website.

Click here to download the GreenPAK file for the SLG7SQ47664 design.

E-mail GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

- Low power consumption
- Programmable time delays between enable signals, no need for external capacitor adjustable time delays
- Power supply monitoring from 0.05 V to V_{DD}, no need for an external resistor to adjust voltage monitoring threshold
- Output stages: inverting or non-inverting open-drain output
- Pb-free/RoHS compliant
- Halogen-free
- STQFN-12 package

Applications

- Desktop/notebook computers, servers
- Low power portable equipment
- Routers base stations
- Line cards
- Graphics cards

Output Summary

- Two outputs – open-drain NMOS 1x

Contents

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1. Block Diagram

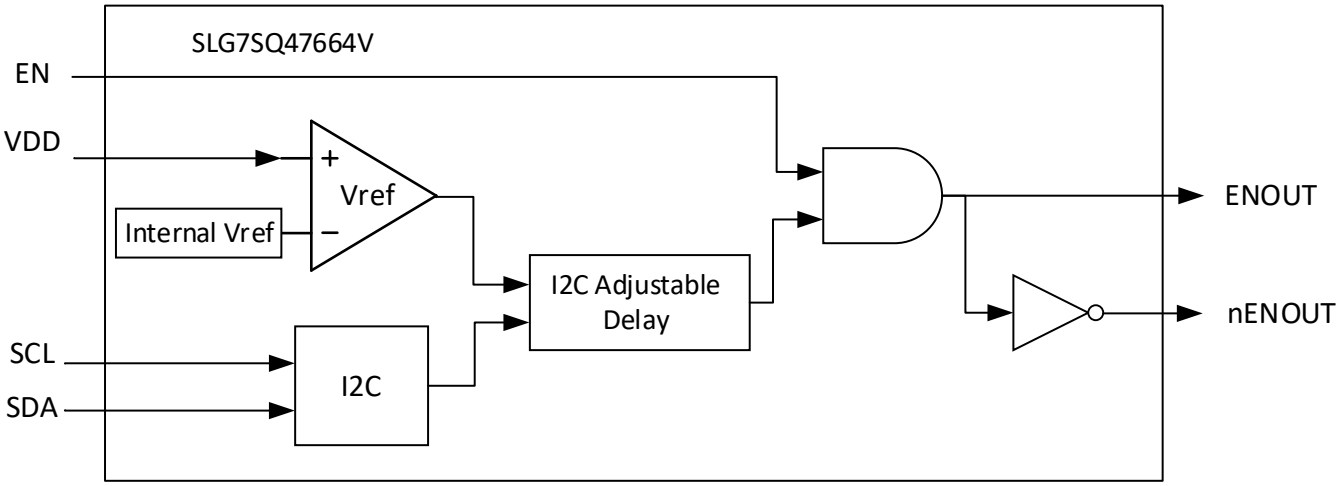


Figure 1. Functional Diagram

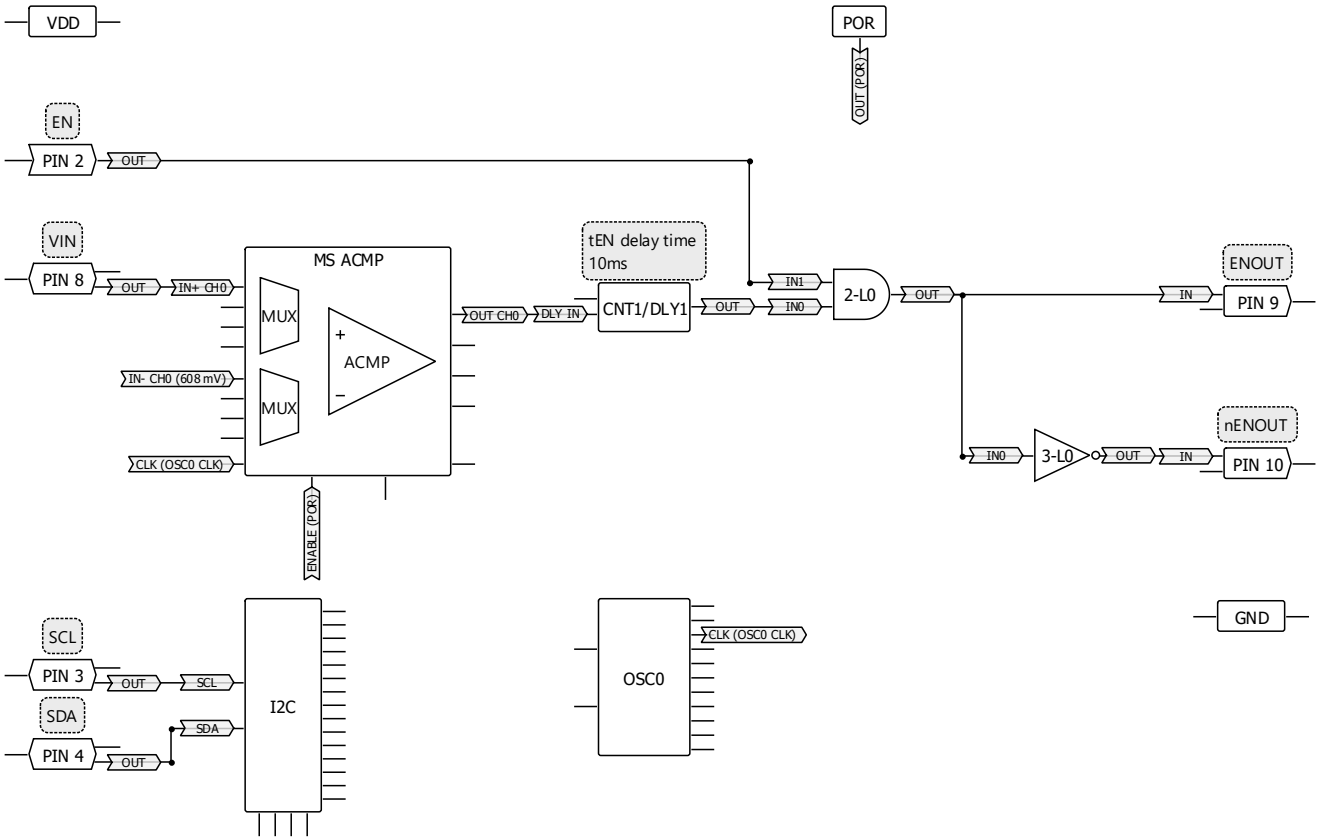
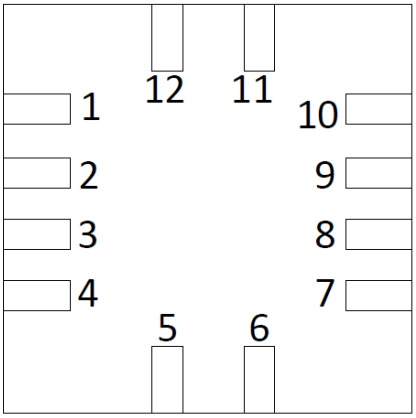


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



STQFN-12
(Top View)

Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin #	Pin Name	Type	Description	Internal Resistor
1	V_{DD}	PWR	Supply Voltage	--
2	EN	Digital Input	Digital Input without Schmitt Trigger	1 MΩ Pull-Down
3	SCL	Digital Input	Digital Input with Schmitt Trigger	Floating
4	SDA	Digital Input	Digital Input with Schmitt Trigger	Floating
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	GND	GND	Ground	--
8	VIN	Analog Input/Output	Analog Input/Output	Floating
9	ENOUT	Digital Output	Open-Drain NMOS 1x	Floating
10	nENOUT	Digital Output	Open-Drain NMOS 1x	Floating
11	NC	--	Keep Floating or Connect to GND	--
12	NC	--	Keep Floating or Connect to GND	--

3. Specifications

3.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{HIGH} to GND		-0.3	7.0	V
Voltage at Input Pin		GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current (Through V_{DD} or GND Pin)		--	90	mA
Maximum Average or DC Current (Through Pin)	OD 1x	--	11	mA
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	+150	°C
Junction Temperature		--	+150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

3.2 Electrical Specifications

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.3	3.3	5.5	V
Operating Temperature	T_A		-40	+25	+85	°C
Capacitor Value at V_{DD}	C_{VDD}		0.1	--	--	µF
Input Capacitance	C_{IN}		--	2.5	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs. PIN3 and PIN4 are HIGH, PIN2 and PIN8 are LOW	--	25	--	µA
Maximal Voltage Applied to any Pin in High-Impedance State	V_O		--	--	V_{DD} + 0.3	V
HIGH-Level Input Voltage	V_{IH}	Logic Input [1]	0.7 x V_{DD}	--	V_{DD} + 0.3	V
LOW-Level Input Voltage	V_{IL}	Logic Input [1]	GND - 0.3	--	0.3 x V_{DD}	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
LOW-Level Output Voltage	V_{OL}	Open-Drain NMOS 1x, I_{OL} = 1 mA, V_{DD} = 2.5 V	--	--	0.036	V
		Open-Drain NMOS 1x, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	--	0.089	V
		Open-Drain NMOS 1x, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	--	0.112	V
LOW-Level Output Current [2]	I_{OL}	Open-Drain NMOS 1x, V_{OL} = 0.15 V, V_{DD} = 2.5 V	3.676	--	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V, V_{DD} = 3.3 V	11.438	--	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V, V_{DD} = 5.0 V	15.397	--	--	mA
Internal Pull-Down Resistance	R_{PULL_DOWN}	Pull-down on PIN2	--	1	--	MΩ
Delay1 Time	T_{DLY1}	T_A = 25 °C	9.99	10.49	11.96	ms
		T_A = - 40 °C to +85 °C [3]	9.91	10.49	12.72	ms
MS ACMP Channel0 Threshold Voltage	V_{ACMP}	Low to High, T_A = 25°C	597	--	619	mV
		Low to High, T_A = -40 °C to +85 °C [3]	593	--	619	mV
		High to Low, T_A = 25°C	597	--	618	mV
		High to Low, T_A = -40 °C to +85 °C [3]	593	--	619	mV
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	1.85	3.42	ms
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip	1.55	1.86	2.17	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip	1.06	1.34	1.62	V

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
[3] Guaranteed by Design.

3.3 I²C Specifications

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Clock Frequency, SCL	F_{SCL}	V_{DD} = 2.3 to 5.5 V	--	--	1000	kHz
Clock Pulse Width Low	t_{LOW}	V_{DD} = 2.3 to 5.5 V	500	--	--	ns
Clock Pulse Width High	t_{HIGH}	V_{DD} = 2.3 to 5.5 V	260	--	--	ns
Bus Free Time between Stop and Start	t_{BUF}	V_{DD} = 2.3 to 5.5 V	500	--	--	ns
Start Hold Time	t_{HD_STA}	V_{DD} = 2.3 to 5.5 V	260	--	--	ns
Start Set-up Time	t_{SU_STA}	V_{DD} = 2.3 to 5.5 V	260	--	--	ns
Data Hold Time	t_{HD_DAT}	V_{DD} = 2.3 to 5.5 V	0	--	--	ns
Data Set-up Time	t_{SU_DAT}	V_{DD} = 2.3 to 5.5 V	50	--	--	ns
Inputs Rise Time	t_R	V_{DD} = 2.3 to 5.5 V	--	--	120	ns
Inputs Fall Time	t_F	V_{DD} = 2.3 to 5.5 V	--	--	120	ns
Stop Set-up Time	t_{SU_STO}	V_{DD} = 2.3 to 5.5 V	260	--	--	ns
Data Out Hold Time	t_{VD_ACK}	V_{DD} = 2.3 to 5.5 V	50	--	--	ns
Clock Low to Data Out Valid	t_{VD_DAT}	V_{DD} = 2.3 to 5.5 V	--	--	450	ns

3.4 Chip Address

HEX	BIN	DEC
0x08	0001000	8

4. I²C Description

4.1 I²C Basic Command Structure

Each command to the I²C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 4. After the Start bit, the first four bits are a control code, which can be set by the user in registers [1179:1176]. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 4 shows this basic command structure.

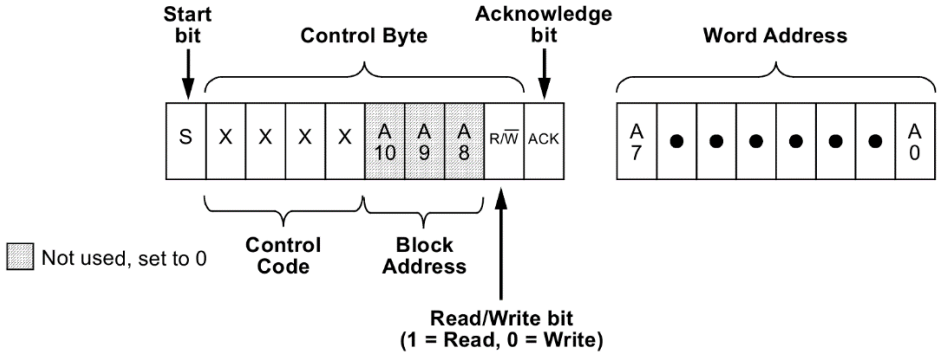


Figure 4. I²C Basic Command Structure

4.2 I²C Serial General Timing

Figure 5 shows the general timing characteristics for the I²C Serial Communications block.

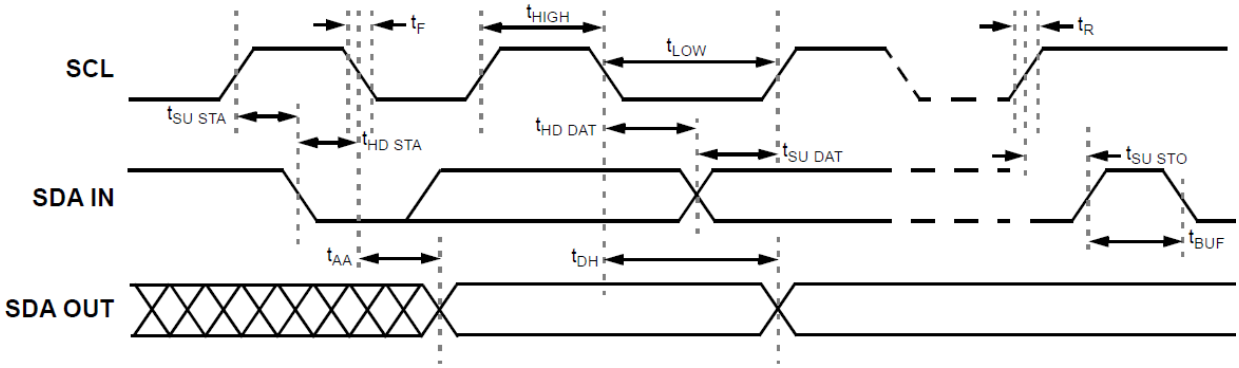


Figure 5. I²C Serial General Timing

4.3 I²C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits], and the R/W bit (set to “0”) are placed onto the bus by the Bus Master. After the I²C Serial Communications block has provided an Acknowledge bit (ACK), the next byte transmitted by the master is the Word Address. The Block Address is the next three bits and the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7SQ47664 for the correct data byte to be written. After the SLG7SQ47664 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7SQ47664 again provides an Acknowledge bit and then

the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7SQ47664 generates the Acknowledge bit.

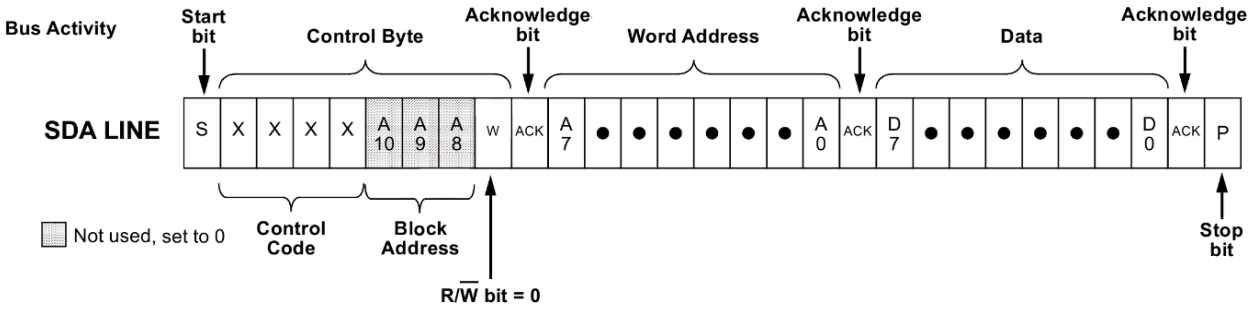


Figure 6. I²C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a Write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of the Write command but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7SQ47664 issues an Acknowledge bit, followed by the requested eight data bits.

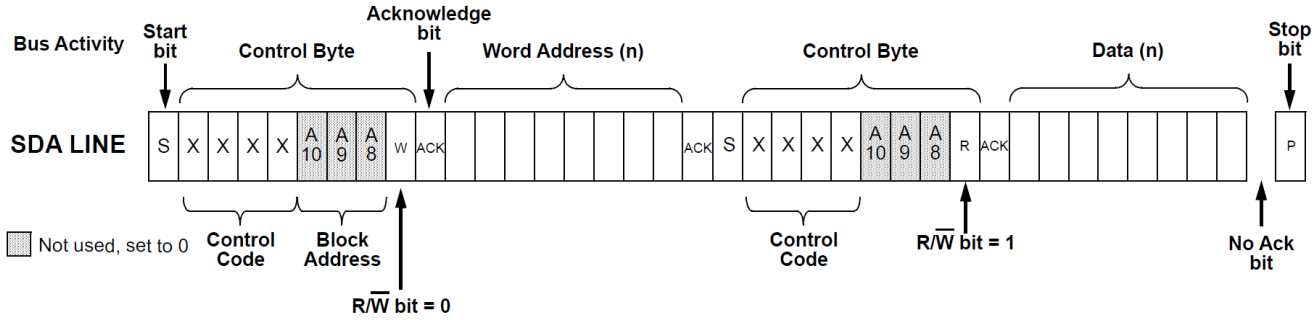


Figure 7. I²C Random Read Command

4.4 I²C Register Control Data

Address Byte	Register Bit	Block	Function
0x42	Registers [535:530]	ACMP0 Vref	ACMP0 Vref Select: 000000: 32 mV ~ 111110: 2.016 V/step = 32 mV

4.5 I²C Commands

1. [start] [0x08] [W] [0x42] [000000xx] [stop] // set ACMP0 Vref to 32 mV
2. [start] [0x08] [W] [0x42] [111111xx] [stop] // set ACMP0 Vref to 2016 mV

5. Timing Diagram

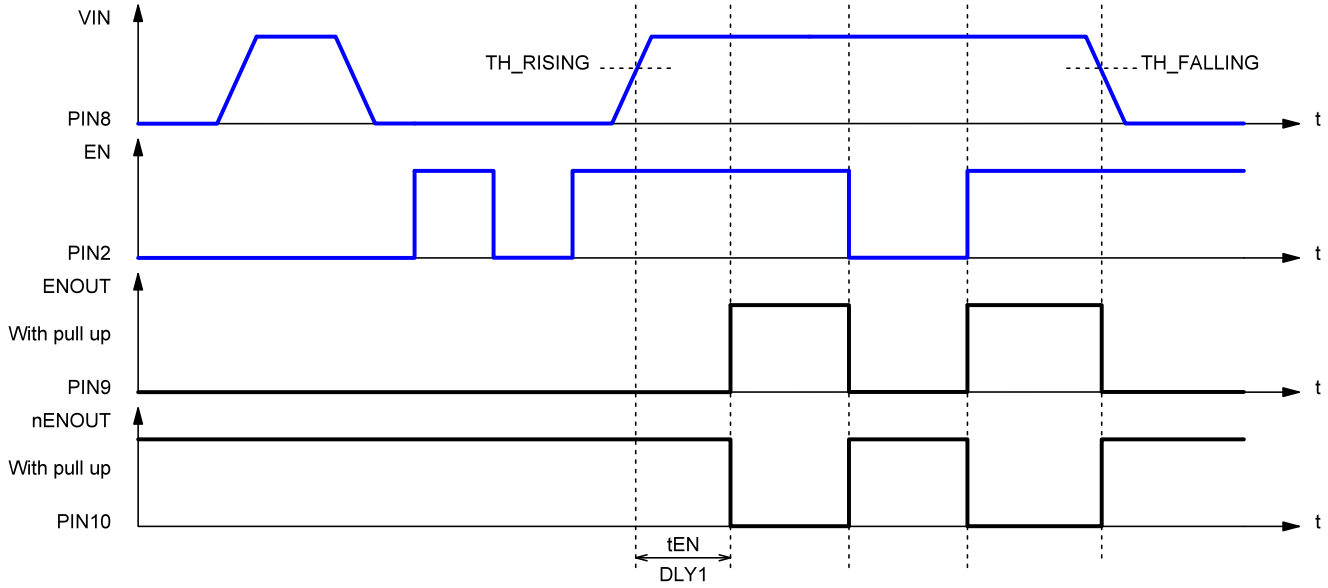


Figure 8. Timing Diagram

6. Typical Application Circuit

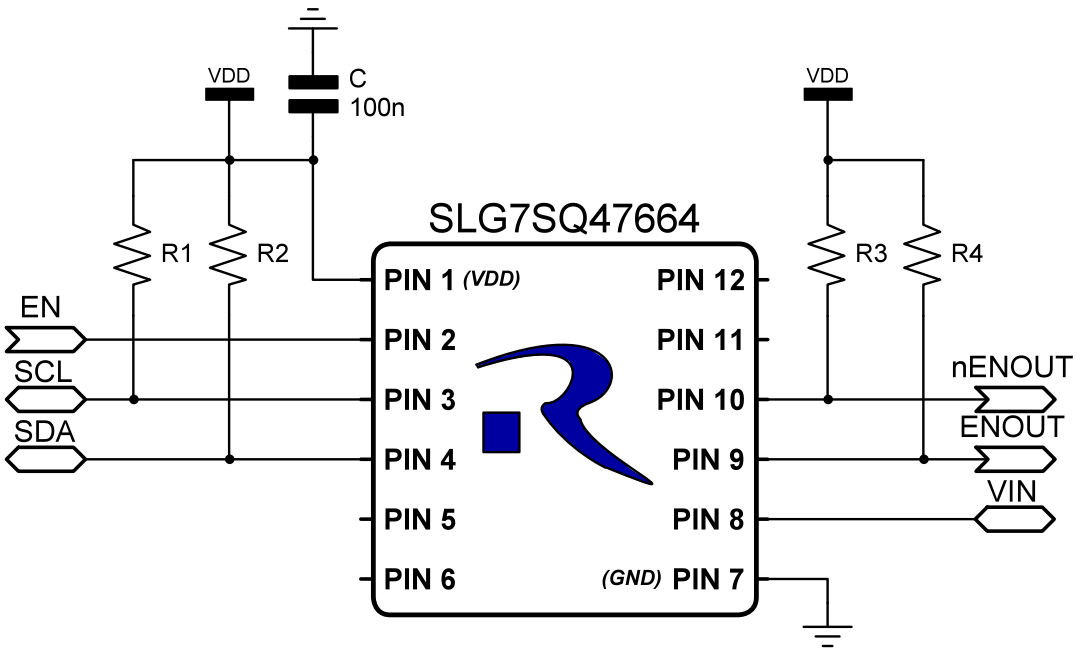
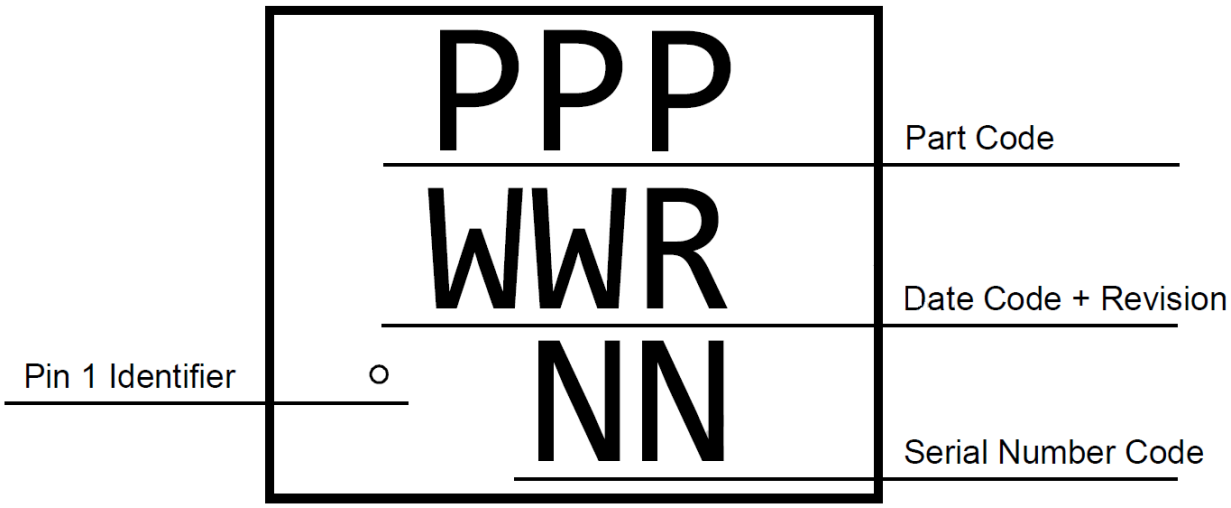


Figure 9. Typical Application Circuit

7. Package Top Marking Definitions



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0x2DA14C65			7/1/2024

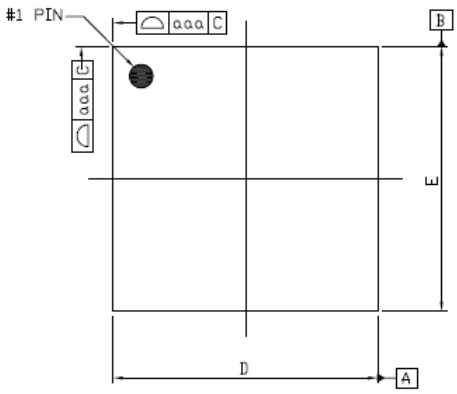
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

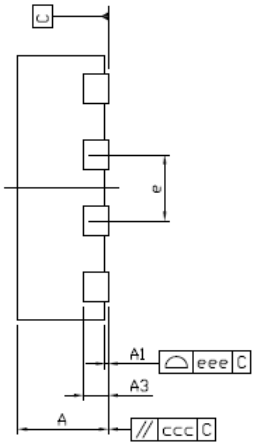
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

8. Package Outlines

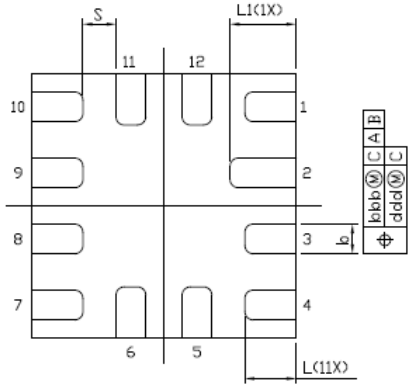
JEDEC MO-220IC Net Weight: 0.0035 g



Top View



Side View



Bottom View

Controlling dimensions: mm

Symbol	MILLIMETER			INCH		
	Min	Nom.	Max	Min	Nom.	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.55	1.60	1.65	0.061	0.063	0.065
e	0.40 BSC			0.016 BSC		
L	0.26	0.31	0.36	0.010	0.012	0.014
L1	0.35	0.40	0.45	0.014	0.016	0.018
b	0.13	0.18	0.23	0.005	0.007	0.009
S	0.200 REF			0.008 REF		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

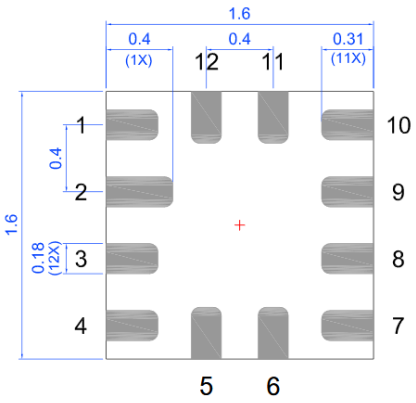
"A1" max lead coplanarity 0.05 mm
Standard tolerance: ±0.05

Notes:

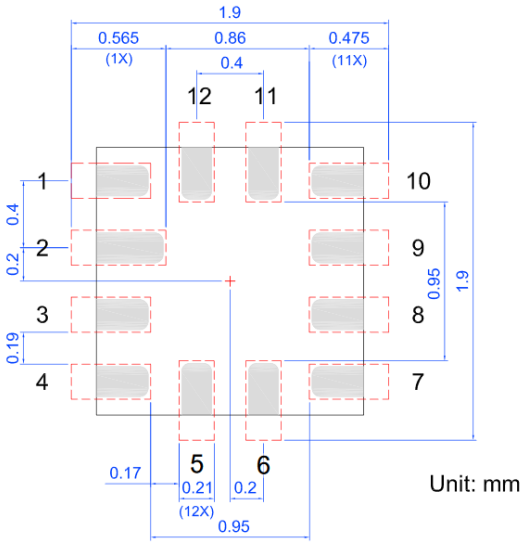
1. All dimensions are in millimeters.
2. Dimension "b" applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

9. Layout Guidelines

Expose Pad
(Package face down)



Recommended Landing Pattern
(Package face down)



9.1 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020. More information can be found at www.jedec.org.

10. Ordering Information

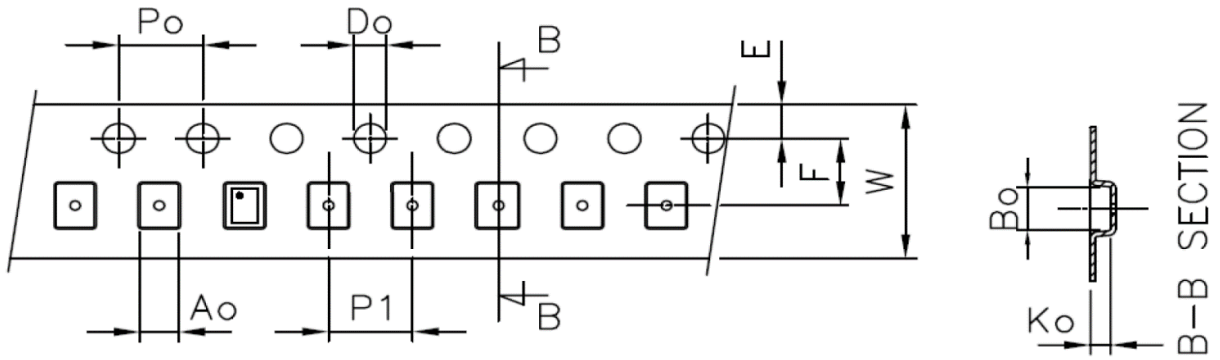
Part Number	Package Type
SLG7SQ47664V	12-pin STQFN - Tape and Reel (3k units)

10.1 Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L 1.6 mm x 1.6 mm x 0.55 mm 0.4P FC Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

10.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L 1.6 mm x 1.6 mm x 0.55 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



11. Revision History

Revision	Date	Description
1.00	Jul 1, 2024	Initial release