SLG7SV47663

Microprocessor Supervisor

The SLG7SV47663 was developed to monitor a 400 mV system voltage for microprocessor supervisory circuits. The main function asserts an open-drain RESET signal, which occurs in two cases: when the SENSE voltage drops below the threshold or when a logic low is asserted on the manual reset (MR) pin. When the SENSE voltage and manual reset (MR) return from their respective reset conditions, the RESET output remains low for 20 ms.

The SLG7SV47663 device provides a low typical quiescent current of 2 µA, so it fits well for battery-powered applications.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations, visit the GreenPAK website.

Click here to download the GreenPAK file for the SLG7SV47663 design.

E-mail GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

- Power-on reset generator with a delay time of 20 ms
- Real-time in-system configuration
- Open-drain watchdog output
- +2.3 V to +5.5 V operating voltage
- Low quiescent current: 2 µA typical
- Fixed threshold voltage for standard voltage rails 400 mV
- Manual reset (MR) input
- Open-drain RESET output
- Temperature range: -40 °C to 85 °C
- ESD performance HBM: 2000 V; CDM: 1000 V
- STQFN - 14 package 1.6 mm x 2.0 mm, IC net weight: 4.5 mg
- Low power consumption
- Pb-free/RoHS compliant
- Halogen-free
- Configurable without external components

Applications

- Desktop computers and notebooks
- Microcontroller applications or DSP
- PDAs and hand-held products
- FPGA and ASIC applications
- Portable and battery-powered products

Output Summary

- One output – open-drain NMOS 1x

Contents

Figures

1. Block Diagram

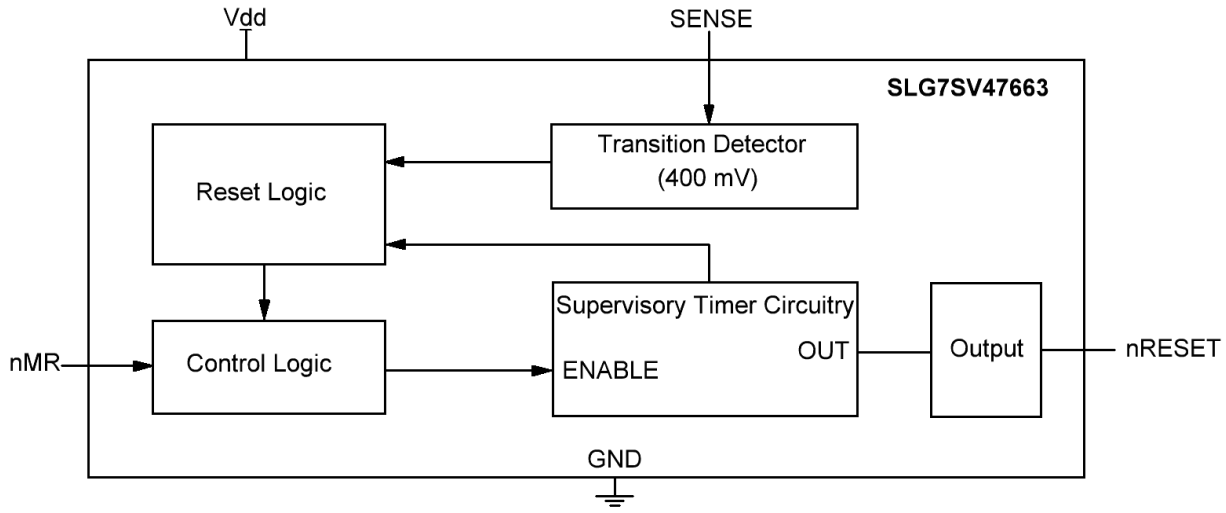


Figure 1. Functional Diagram

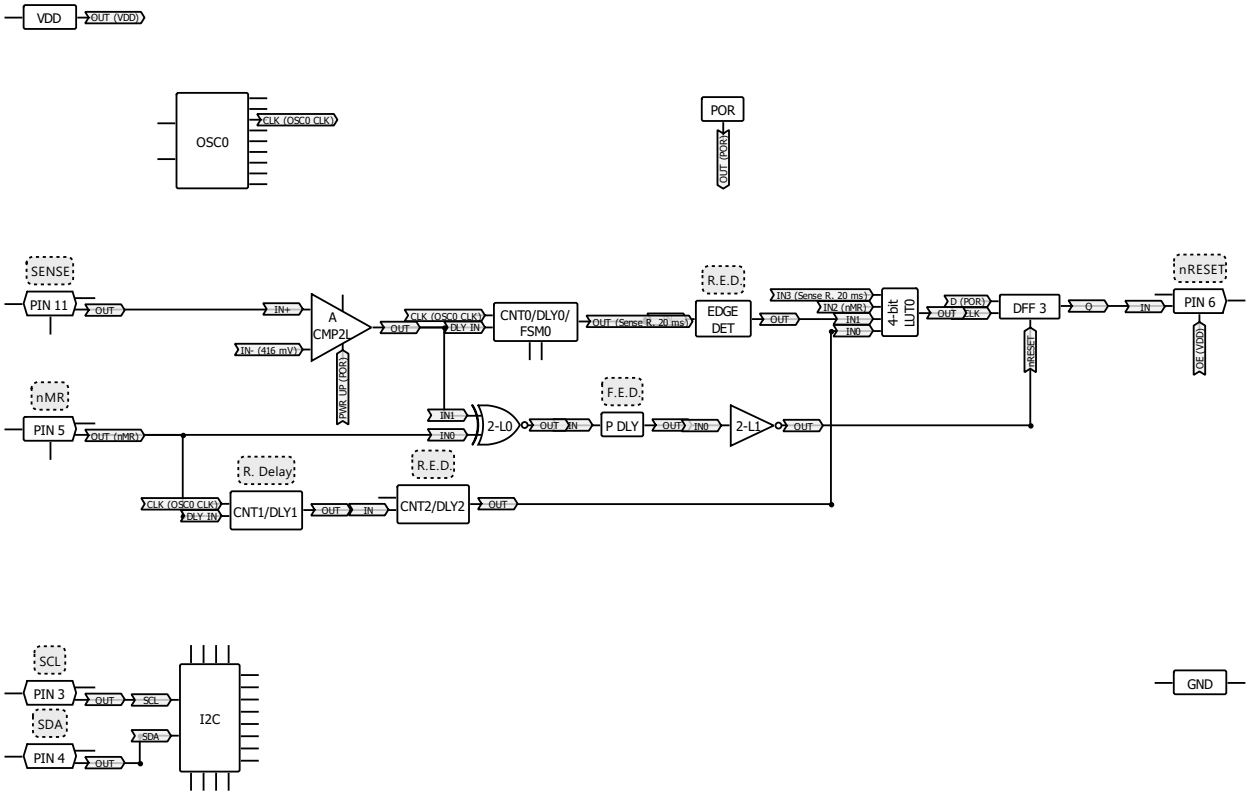


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

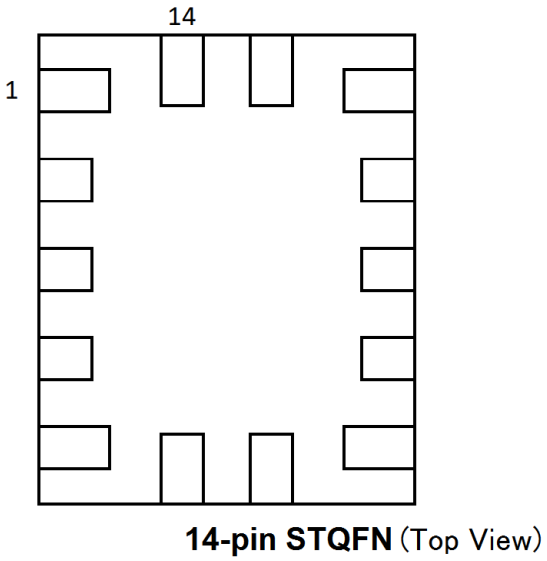


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin #	Pin Name	Type	Pin Description	Internal Resistors
1	V_{DD}	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	SCL	Digital Input	Digital Input without Schmitt Trigger	Floating
4	SDA	Digital Input	Digital Input without Schmitt Trigger	Floating
5	nMR	Digital Input	Digital Input without Schmitt Trigger	100 kΩ Pull-Up
6	nRESET	Digital Output	Open-Drain NMOS 1x	Floating
7	NC	--	Keep Floating or Connect to GND	--
8	GND	GND	Ground	--
9	NC	--	Keep Floating or Connect to GND	--
10	NC	--	Keep Floating or Connect to GND	--
11	SENSE	Analog Input/Output	Analog Input/Output	Floating
12	NC	--	Keep Floating or Connect to GND	--
13	NC	--	Keep Floating or Connect to GND	--
14	NC	--	Keep Floating or Connect to GND	--

3. Specifications

3.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current (Through V_{DD} or GND Pin)		--	90	mA
Maximum Average or DC Current (Through pin)	OD 1x	--	11	mA
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

3.2 Electrical Specifications

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.3	3.3	5.5	V
Operating Temperature	T_A		-40	25	85	°C
Capacitor Value at V_{DD}	C_{VDD}		0.1	--	--	µF
Input Capacitance	C_{IN}		--	4	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs. PIN 11 is LOW, PIN 3 and PIN 4 are HIGH	--	2	--	µA
Maximal Voltage Applied to any PIN in High-Impedance State	V_O		--	--	V_{DD} + 0.3	V
HIGH-Level Input Voltage	V_{IH}	Logic input [1]	0.7xV_{DD}	--	V_{DD} + 0.3	V
LOW-Level Input Voltage	V_{IL}	Logic input [1]	GND - 0.3	--	0.3xV_{DD}	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
LOW-Level Output Voltage	V_{OL}	Open-Drain NMOS 1x, I_{OL} = 1 mA, at V_{DD} = 2.5 V	--	--	0.043	V
		Open-Drain NMOS 1x, I_{OL} = 3 mA, at V_{DD} = 3.3 V	--	--	0.087	V
		Open-Drain NMOS 1x, I_{OL} = 5 mA, at V_{DD} = 5.0 V	--	--	0.107	V
LOW-Level Output Current [2]	I_{OL}	Open-Drain NMOS 1x, V_{OL} = 0.15 V, at V_{DD} = 2.5 V	4.11	--	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V, at V_{DD} = 3.3 V	13.35	--	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V, at V_{DD} = 5.0 V	17.90	--	--	mA
Internal Pull-Up Resistance	R_{PULL_UP}	Pull-up on PIN 5	--	100	--	kΩ
Delay0 Time	T_{DLY0}	At temperature 25 °C	19.71	20.26	21.92	ms
		At temperature -40 °C to +85 °C [3]	19.58	20.26	23.24	ms
Delay1 Time	T_{DLY1}	At temperature 25 °C	19.71	20.26	21.92	ms
		At temperature -40 °C to +85 °C [3]	19.58	20.26	23.24	ms
Analog Comparator2 Threshold Voltage	V_{ACMP2}	Low to High transition, at temperature 25 °C	402	--	429	mV
		Low to High transition, at temperature -40 °C to +85 °C [3]	397	--	432	mV
		High to Low transition, at temperature 25 °C	402	--	429	mV
		High to Low transition, at temperature -40 °C to +85 °C [3]	397	--	432	mV
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	1	2	ms
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
[3] Guaranteed by Design.

3.3 I²C Specifications

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Clock Frequency, SCL	F_{SCL}	V_{DD} = 2.3 V to 5.5 V	--	--	400	kHz
Clock Pulse Width Low	t_{LOW}	V_{DD} = 2.3 V to 5.5 V	1300	--	--	ns
Clock Pulse Width High	t_{HIGH}	V_{DD} = 2.3 V to 5.5 V	600	--	--	ns
Input Filter Spike Suppression (SCL, SDA)	t_I	V_{DD} = 2.5 V ± 8 %	--	--	95	ns
		V_{DD} = 3.3 V ± 10 %	--	--	95	ns
		V_{DD} = 5.0 V ± 10 %	--	--	111	ns
Clock Low to Data Out Valid	t_{AA}	V_{DD} = 2.3 V to 5.5 V	--	--	900	ns
Bus Free Time between Stop and Start	t_{BUF}	V_{DD} = 2.3 V to 5.5 V	1300	--	--	ns
Start Hold Time	t_{HD_STA}	V_{DD} = 2.3 V to 5.5 V	600	--	--	ns
Start Set-up Time	t_{SU_STA}	V_{DD} = 2.3 V to 5.5 V	600	--	--	ns
Data Hold Time	t_{HD_DAT}	V_{DD} = 2.3 V to 5.5 V	0	--	--	ns
Data Set-up Time	t_{SU_DAT}	V_{DD} = 2.3 V to 5.5 V	100	--	--	ns
Inputs Rise Time	t_R	V_{DD} = 2.3 V to 5.5 V	--	--	300	ns
Inputs Fall Time	t_F	V_{DD} = 2.3 V to 5.5 V	--	--	300	ns
Stop Set-up Time	t_{SU_STO}	V_{DD} = 2.3 V to 5.5 V	600	--	--	ns
Data Out Hold Time	t_{DH}	V_{DD} = 2.3 V to 5.5 V	50	--	--	ns

[1] Timing diagram can be found in the Figure 5.

3.4 Chip Address

HEX	BIN	DEC
0x08	0001000	8

4. I²C Description

4.1 I²C Basic Command Structure

Each command to the I²C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 4. After the Start bit, the first four bits are a control code, which can be set by the user in registers [2027:2024]. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 4 shows this basic command structure.

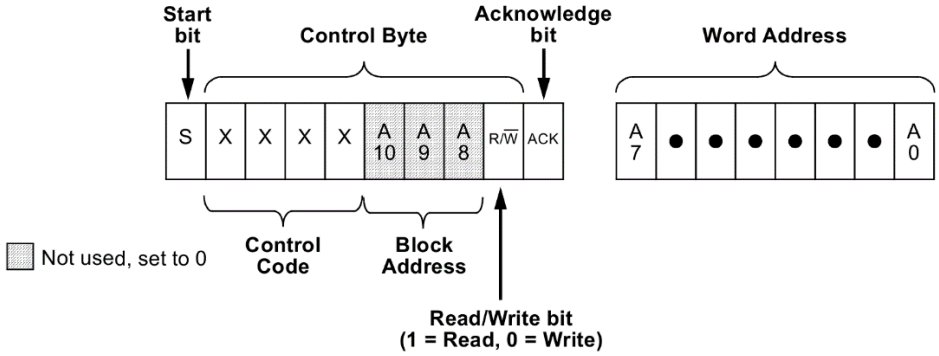


Figure 4. I²C Basic Command Structure

4.2 I²C Serial General Timing

Shown in Figure 5 is the general timing characteristics for the I²C Serial Communications block.

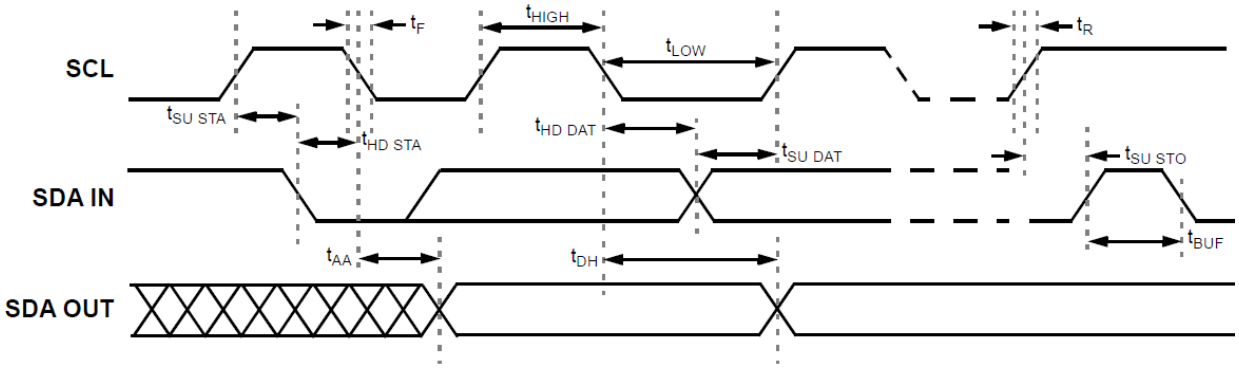


Figure 5. I²C Serial General Timing

4.3 I²C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits], and the R/W bit (set to “0”) are placed onto the bus by the Bus Master. After the I²C Serial Communications block has provided an Acknowledge bit, the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7SV47663 to the correct data byte to be written. After the SLG7SV47663 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7SV47663 again provides an Acknowledge bit and then the Bus

Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7SV47663 generates the Acknowledge bit.

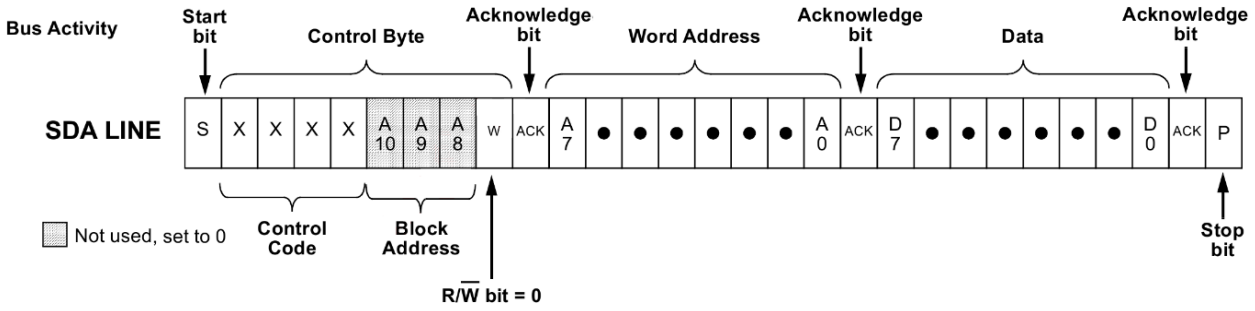


Figure 6. I²C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7SV47663 issues an Acknowledge bit, followed by the requested eight data bits.

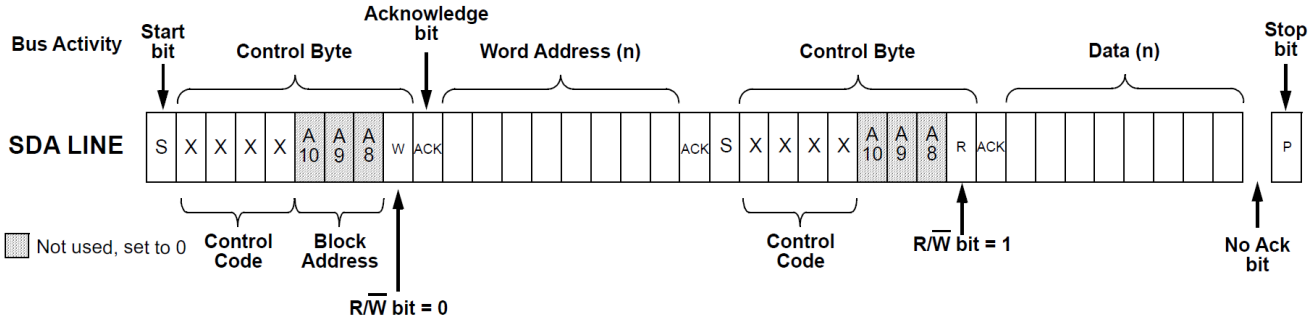


Figure 7. I²C Random Read Command

4.4 I²C Register Control Data

Address Byte	Register Bit	Block	Function
0x95	Registers [1199:1192]	DLY0	DLY0 Counter Data
0x96	Registers [1207:1200]		
0x98	Registers [1223:1216]	DLY1	DLY1 Counter Data

4.5 I²C Commands

1. [start] [0x08] [w] [0x95] [xxxxxxxx] [xxxxxxxx] [stop] // set DLY0 Counter Data
2. [start] [0x08] [w] [0x98] [xxxxxxxx] [stop] // set DLY1 Counter Data
3. [start] [0x08] [w] [0x95] [start] [0x08] [R] [xxxxxxxx] [xxxxxxxx] [stop] // read DLY0 Counter Data
4. [start] [0x08] [w] [0x98] [start] [0x08] [R] [xxxxxxxx] [stop] // read DLY1 Counter Data

5. Typical Application Circuit

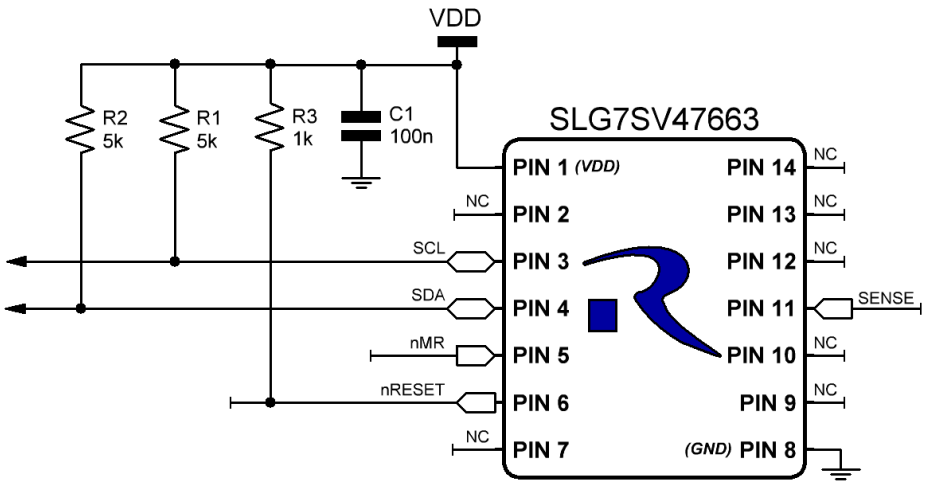


Figure 8. Typical Application Circuit

6. Functionality Waveforms

Channel 1 (yellow/top line) – PIN 11 (SENSE).

Channel 2 (light blue/2nd line) – PIN 5 (nMR).

Channel 3 (magenta/3rd line) – PIN 6 (nRESET) with external 5 kΩ pull-up resistor.

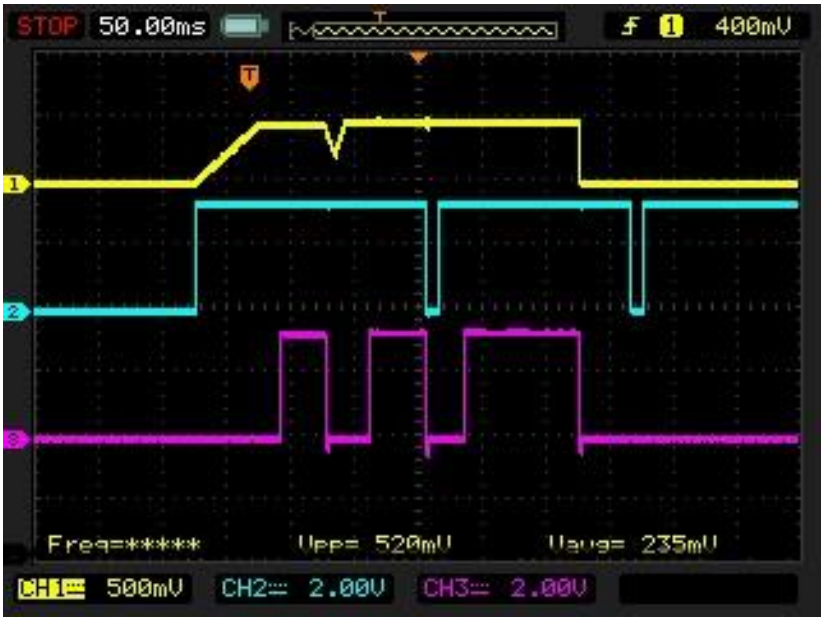


Figure 9. General Functionality for PIN 11 (SENSE), PIN 5 (nMR), and PIN 6 (nRESET)

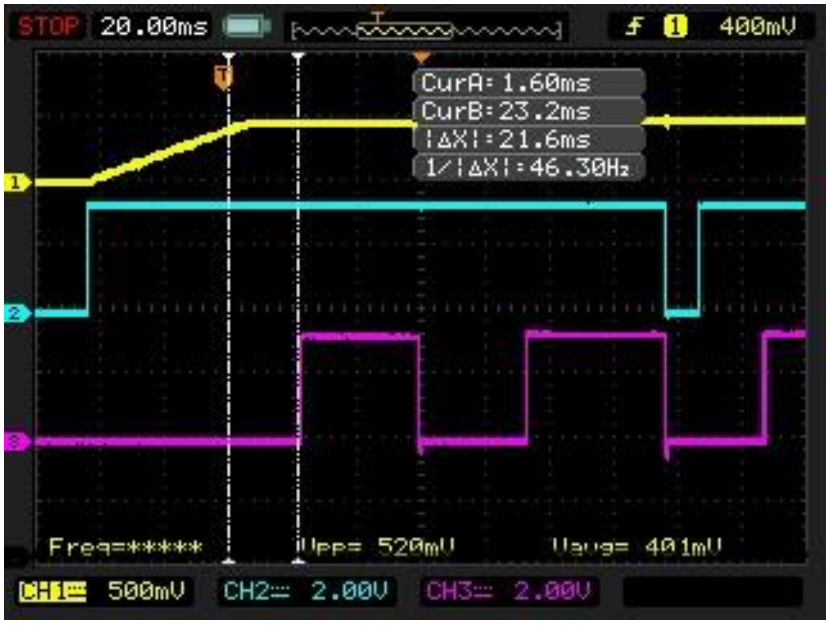


Figure 10. Reset Functionality as PIN 11 (SENSE) First Rises Above 400 mV

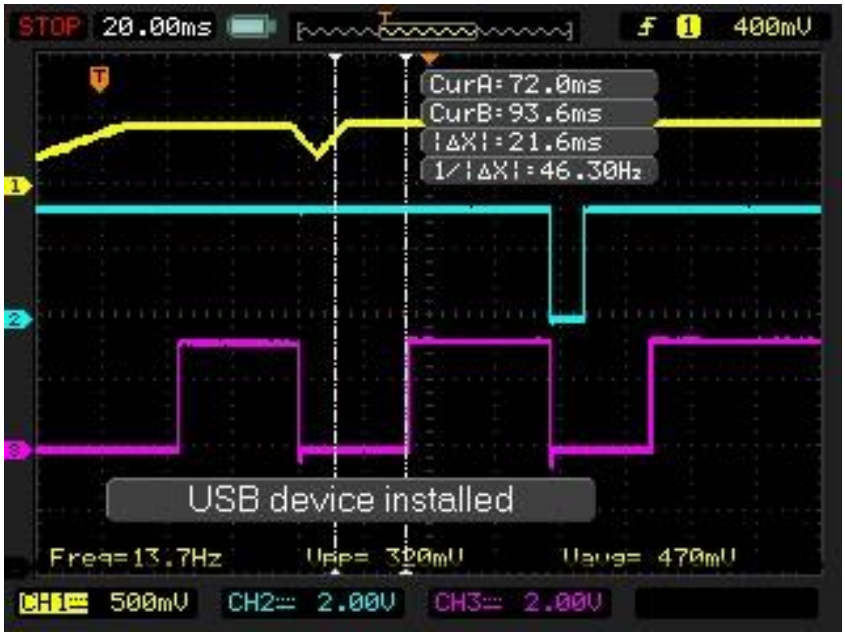
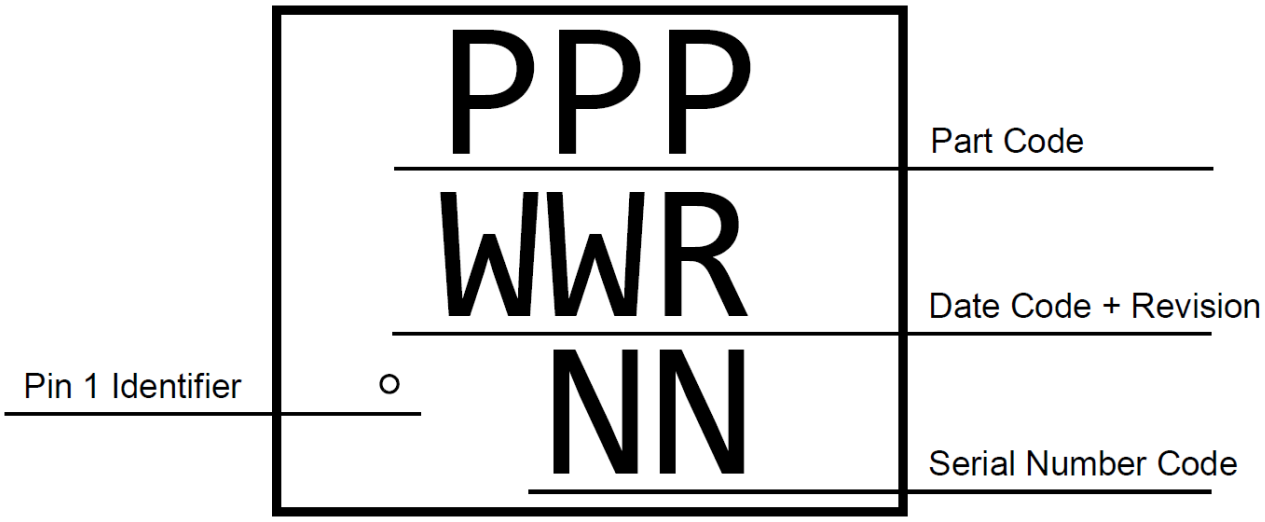


Figure 11. Reset Functionality when PIN 11 (SENSE) Drops Below 400 mV and Returns Above 400 mV

Figure 12. Reset Functionality when PIN 5 (nMR) Is Pulsed Low

7. Package Top Marking Definitions



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0xF2C4CAE5			7/1/2024

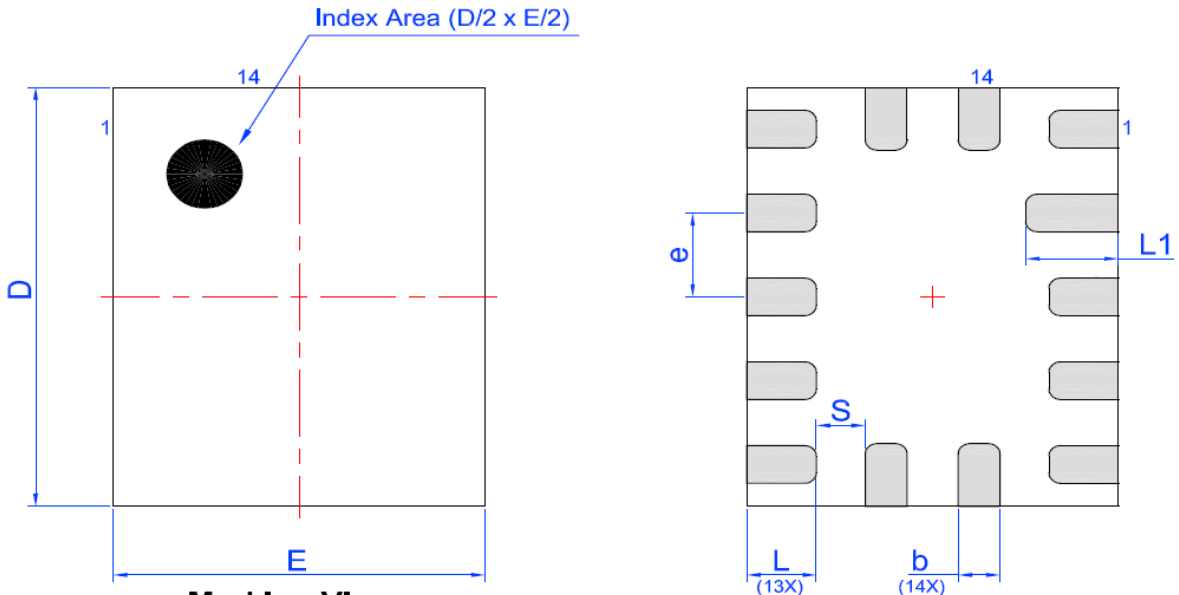
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

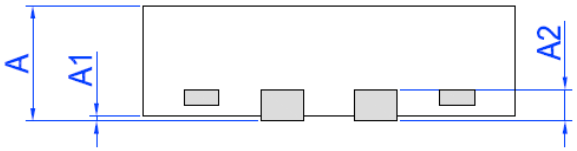
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

8. Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Marking View

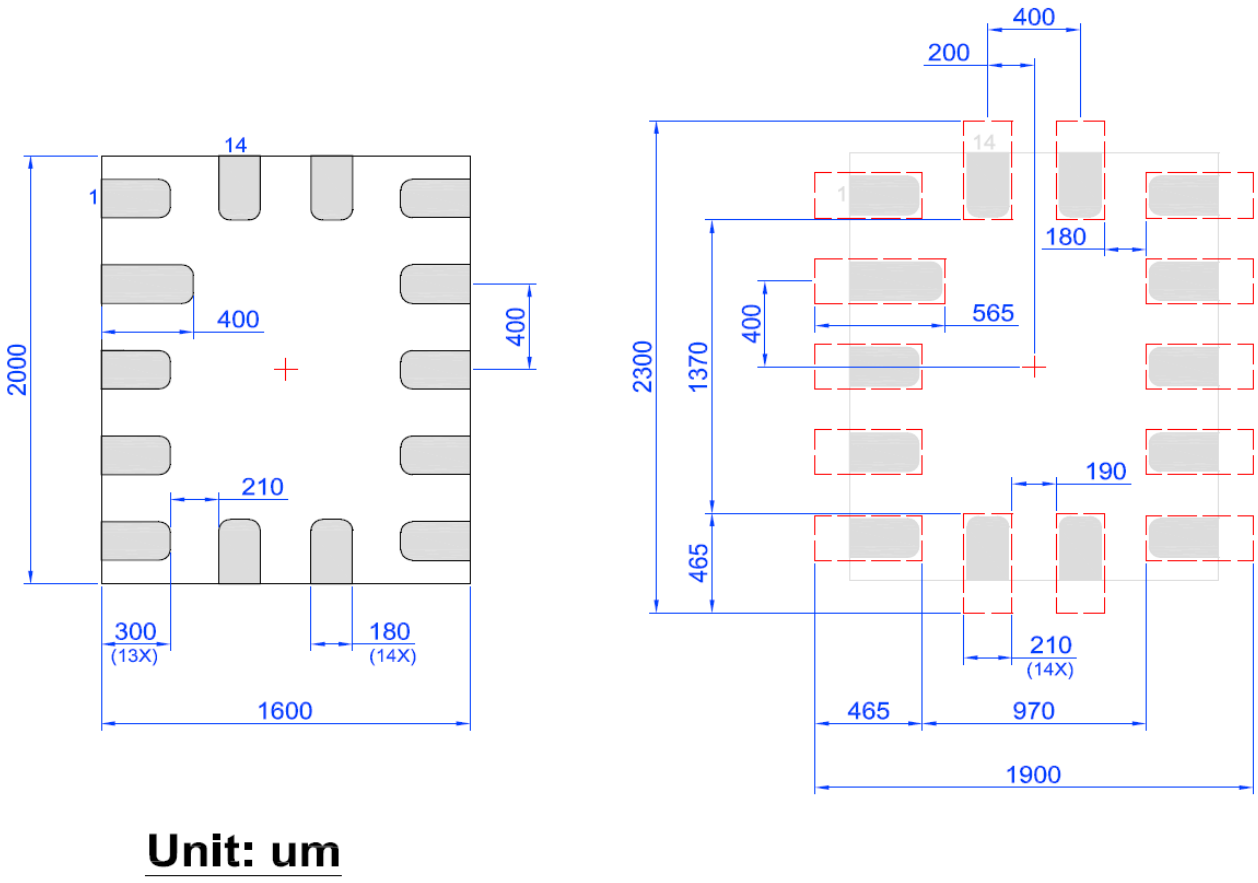


Marking View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

9. Layout Guidelines



Unit: um

9.1 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L package. More information can be found at www.jedec.org.

10. Ordering Information

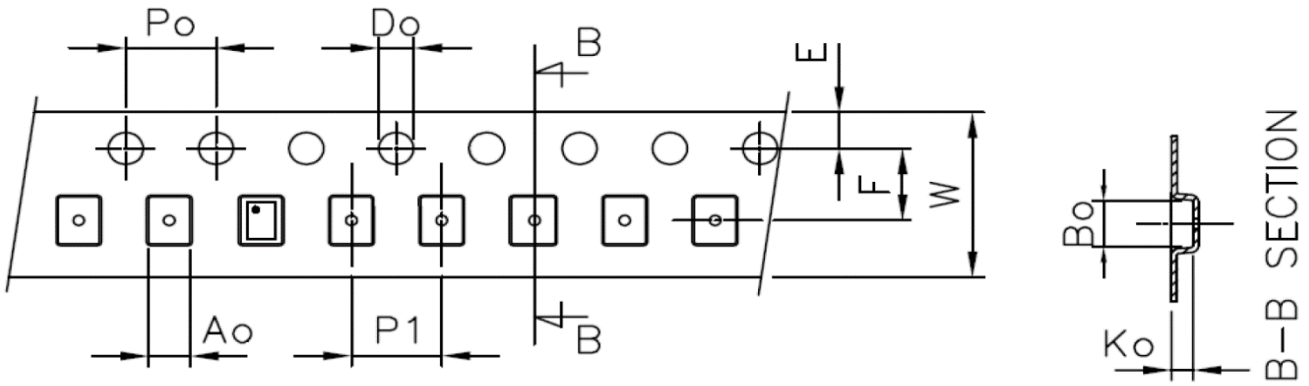
Part Number	Package Type
SLG7SV47663V	14-pin STQFN – Tape and Reel (3k units)

10.1 Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	Per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6 mm x 2.0 mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178/60	100	400	100	400	8	4

10.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6 mm x 2.0 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



11. Revision History

Revision	Date	Description
1.00	Jul 1, 2024	Initial release