SLG7WD47666

Watchdog Timer

The SLG7WD47666 watchdog timer supervises microprocessor (µP) activities, identifying anomalies in system behavior. For proper code execution, the microprocessor must periodically toggle the watchdog input (WDI) before the selected timeout (twd) expires. During normal operation, WDI clears the internal watchdog timer at intervals within twd. If the watchdog timer is not cleared within twd, a watchdog output (nWDO) pulse is triggered, which indicates there was a failure to execute instructions in time. This pulse can prompt a microprocessor reset or system interrupt to address errors in operation, enhancing system reliability.

Additionally, an enable pin (nEN) allows toggling of the watchdog functionality. The device is enabled when the nEN pin is left floating, connected to the internal 100K pull-down resistor.

Renesas SLG7WD47666 is a low power and small form device. The SoC is housed in the 1.0 mm x 1.2 mm STQFN package, which is optimal for using with small devices.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations, visit the GreenPAK Website.

Click here to download the GreenPAK file for the SLG7WD47666 design.

E-mail GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

- Very low current consumption: 9 µA typical
- Watchdog timeout period 1.6 s
- Chip enable input
- +2.5 V to +5.5 V operating voltage
- Open-drain nWDO output
- Operating temperature range: -40 °C to 85 °C
- ESD performance HBM: 2000 V; CDM: 1300 V
- Low power consumption
- Pb-free/RoHS compliant
- Halogen-free
- Configurable without external components
- STQFN - 8 package 1.0 mm x 1.2 mm

Applications

- Alarm systems
- Telecommunications
- Networking
- Industrial equipment
- UPS (uninterruptible power supply)
- Medical equipment

Output Summary

- One output – open-drain NMOS 1x

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1. Block Diagram

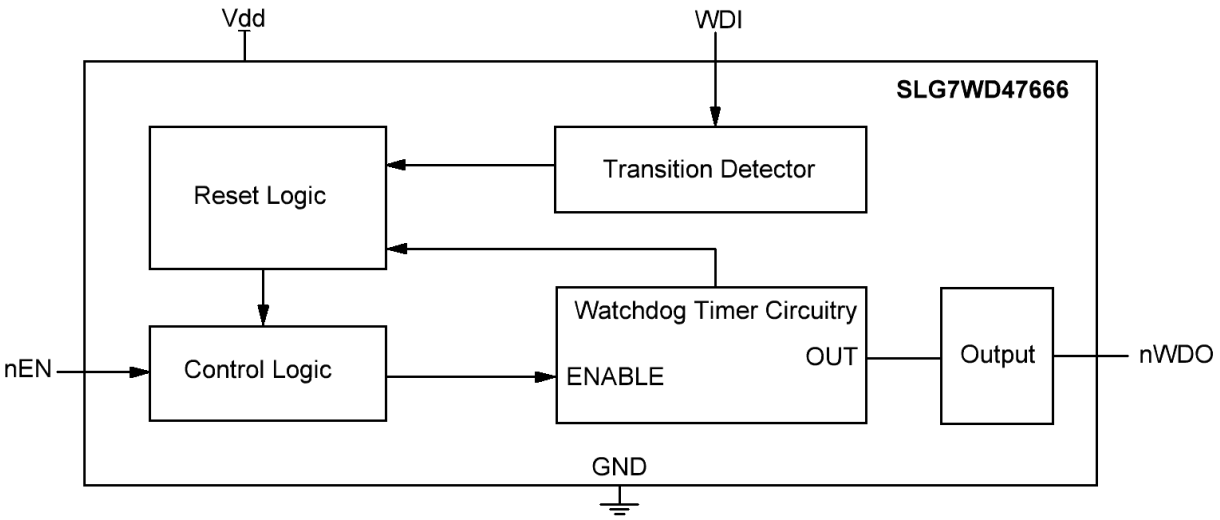


Figure 1. Functional Diagram

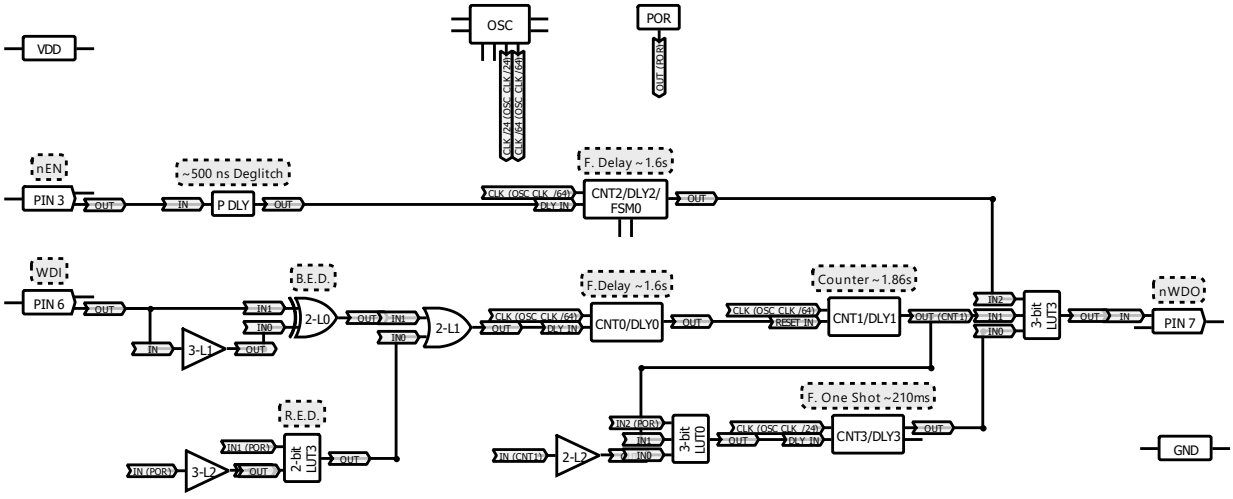
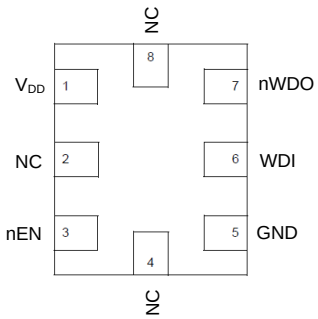


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



STQFN-8
(Top View)

Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin #	Pin Name	Type	Pin Description	Internal Resistors
1	V_{DD}	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	nEN	Digital Input	Digital Input without Schmitt Trigger	100 kΩ Pull-Down
4	NC	--	Keep Floating or Connect to GND	--
5	GND	GND	Ground	--
6	WDI	Digital Input	Digital Input without Schmitt Trigger	Floating
7	nWDO	Digital Output	Open-Drain NMOS 1x	Floating
8	NC	--	Keep Floating or Connect to GND	--

3. Specifications

3.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current (Through pin)	OD 1x	--	8	mA
Current at Input Pin		-1.0	1.0	mA
Input Leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

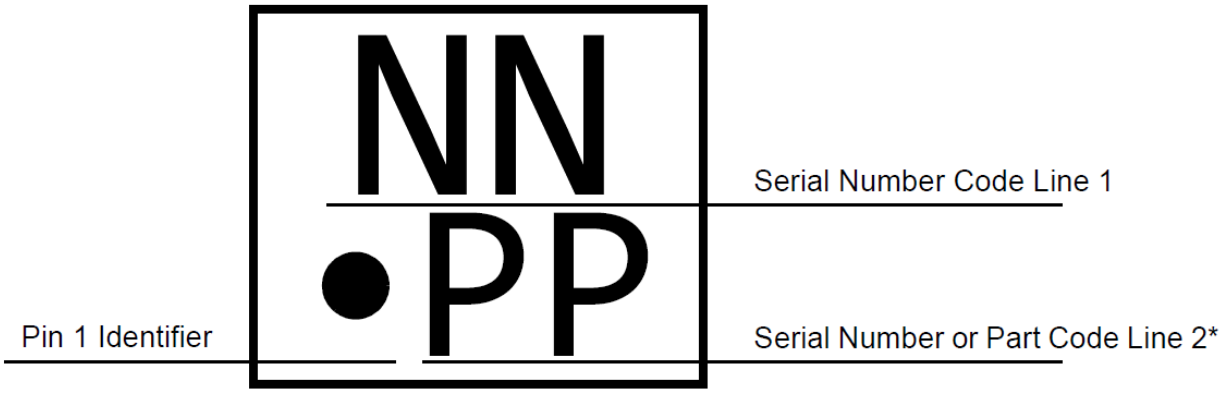
3.2 Electrical Specifications

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	3.3	5.5	V
Operating Temperature	T_A		-40	25	85	°C
Capacitor Value at V_{DD}	C_{VDD}		--	0.1	--	µF
Input Capacitance	C_{IN}		--	4	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs	--	9	--	µA
Maximal Voltage Applied to any Pin in High-Impedance State	V_O		--	--	V_{DD} + 0.3	V
Maximum Average or DC Current through V_{DD} Pin (Per Chip Side [2])	I_{VDD}	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
Maximum Average or DC Current through GND Pin (Per chip side [2])	I_{GND}	T_J = 85 °C	--	--	90	mA
		T_J = 110 °C	--	--	44	mA
HIGH-Level Input Voltage	V_{IH}	Logic Input at V_{DD} = 1.8 V	1.071	--	V_{DD}	V
		Logic Input at V_{DD} = 3.3 V	1.84	--	V_{DD}	V
		Logic Input at V_{DD} = 5.0 V	2.744	--	V_{DD}	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
LOW-Level Input Voltage	V_{IL}	Logic Input at V_{DD} = 1.8 V	--	--	0.73	V
		Logic Input at V_{DD} = 3.3 V	--	--	1.255	V
		Logic Input at V_{DD} = 5.0 V	--	--	1.877	V
LOW-Level Output Voltage	V_{OL}	Open-Drain NMOS 1x, I_{OL} = 100 µA, at V_{DD} = 1.8 V	--	0.005	0.006	V
		Open-Drain NMOS 1x, I_{OL} = 3 mA, at V_{DD} = 3.3 V	--	0.085	0.121	V
		Open-Drain NMOS 1x, I_{OL} = 5 mA, at V_{DD} = 5.0 V	--	0.11	0.155	V
LOW-Level Output Current [1]	I_{OL}	Open-Drain NMOS 1x, V_{OL} = 0.15 V, at V_{DD} = 1.8 V	2.029	2.763	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V, at V_{DD} = 3.3 V	9.227	12.995	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V, at V_{DD} = 5.0 V	12.444	17.282	--	mA
Internal Pull-Down Resistance	R_{PULL_DOWN}	Pull-down on Pin 3	--	100	--	kΩ
Delay0 Time	T_{DLY0}	At temperature 25 °C	1.52	1.61	1.68	s
		At temperature -40 °C to +85 °C [3]	1.48	1.61	1.75	s
Delay2 Time	T_{DLY2}	At temperature 25 °C	1.52	1.61	1.68	s
		At temperature -40 °C to +85 °C [3]	1.48	1.61	1.75	s
Delay3 Time	T_{DLY3}	At temperature 25 °C	200.48	213.11	222.91	ms
		At temperature -40 °C to +85 °C [3]	194.92	213.11	232.26	ms
Output Period	T_{CNT1}	At temperature 25 °C	1.75	1.86	1.94	s
		At temperature -40 °C to +85 °C [3]	1.71	1.86	2.02	s
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	0.54	--	ms
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip	0.675	0.901	1.174	V

[1] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
[2] The GreenPAK's power rails are divided in two sides. Pins 2, 3, and 4 are connected to one side, pins 6, 7, and 8 to another.
[3] Guaranteed by Design.

4. Package Top Marking Definitions



* PP may consist of the special characters +, -, and = for a total of 9 different combinations, or may consist of two character alphanumeric Part Code (A-Z and 0-9), depending on time of marking.

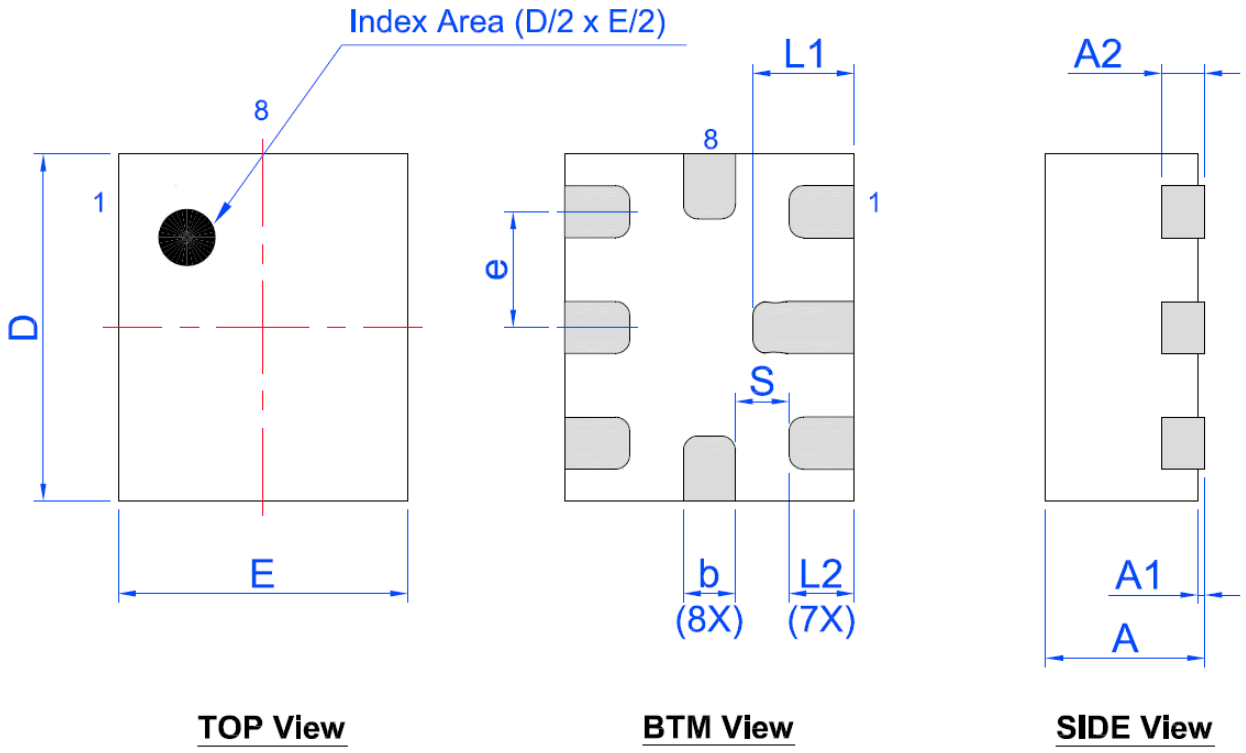
Note: The SN Code (Line 1 and Line 2) is generated during production, and encodes information including part number, programming code number, date code and lot code. This same information is provided in plain text form on a label placed on the reel. If you need assistance in decoding the SN Code, please contact Renesas Electronics Corporation.

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0x8C08D6DE			7/1/2024

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

5. Package Outlines

8 Lead STQFN Package 1.0 x 1.2 mm

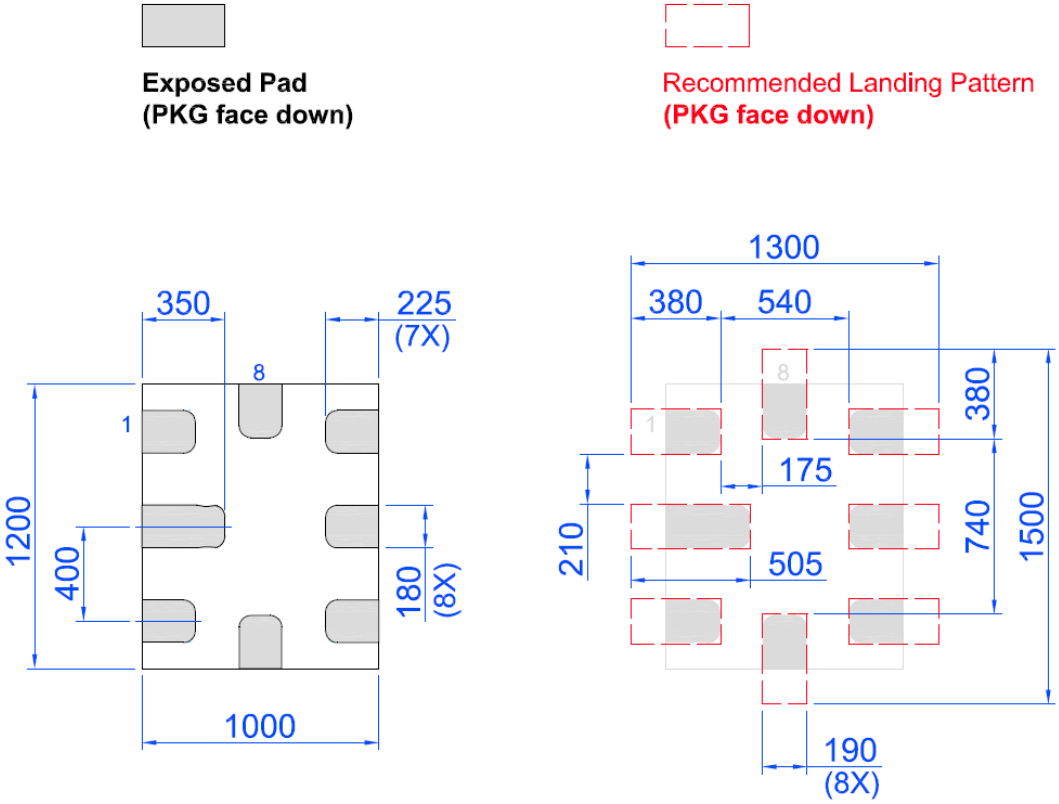


TOP View **BTM View** **SIDE View**

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.15	1.20	1.25
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L1	0.30	0.35	0.40
b	0.13	0.18	0.23	L2	0.175	0.225	0.275
e	0.40 BSC			S	0.185 REF		

6. Layout Guidelines



6.1 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm^3 (nominal). More information can be found at www.jedec.org.

7. Ordering Information

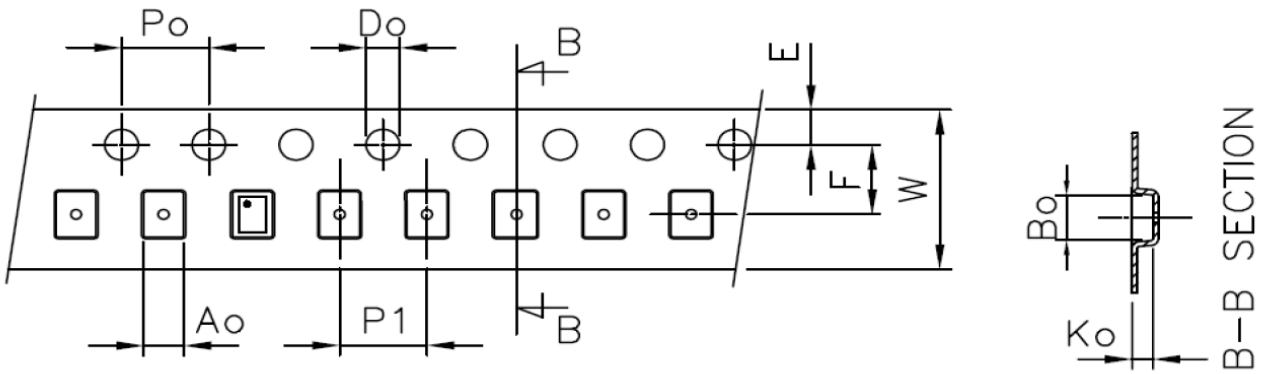
Part Number	Package Type
SLG7WD47666V	8-pin STQFN – Tape and Reel (3k units)

7.1 Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	Per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 8L 0.4P FC Green	8	1.0x1.2x0.55	3000	3000	178/60	100	400	100	400	8	4

7.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 8L 0.4P FC Green	1.16	1.38	0.71	4	4	1.5	1.75	3.5	8



8. Revision History

Revision	Date	Description
1.00	Jan 20, 2025	Initial release

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