SLG7WD47674

Pin-Selectable Watchdog Timer

The SLG7WD47674 watchdog timer with pin-selectable features is designed to monitor microprocessor (µP) activities and identify abnormal system behavior. To confirm that the code is being processed appropriately, the microprocessor should routinely toggle the watchdog input (WDI) before the selected watchdog timeout length expires. The supervisor initiates a watchdog (WDO) output signal to indicate that the system is not executing the intended instruction within the allotted time if the µP does not provide a valid watchdog input transition before the timeout period ends. When there are processing issues, this watchdog output pulse can be used to either reset the µP or cause a system interrupt to notify of errors.

By identifying mistakes in code execution, the SLG7WD47674 provides flexible watchdog timer supervision, improving system reliability. This IC meets a variety of system timing needs by offering numerous pin-selectable watchdog timing options:

- Watchdog startup delay: before the watchdog timer starts, there is a little delay.
- Watchdog timeout period: specifies how long the watchdog timeout usually lasts after the first startup delay.
- Watchdog output/timing options: open-drain (200 ms).

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations, visit the GreenPAK website.

Click here to download the GreenPAK file for the SLG7WD47674 design.

E-mail GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

- Pin-selectable watchdog timeout periods
- Real-time In-system configuration
- Watchdog timer disable feature
- Open-drain watchdog output
- +2.5 V to +5.5 V operating voltage
- 1 µA quiescent current
- 10 µA max supply current
- Configurable without external components
- Low power consumption
- Pb-free/RoHS compliant
- Halogen-free
- 14-pin STQFN: 2.0 mm x 2.2 mm x 0.55 mm, 0.4 mm pitch

Applications

- Microcontroller (µC) and microprocessor (µP) monitoring
- Industrial controllers
- Telecommunications
- Networking
- Embedded control systems
- Data communications equipment
- Handheld and portable electronics
- Personal computers and servers

Output Summary

- One output – open-drain NMOS 1x

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1. Block Diagram

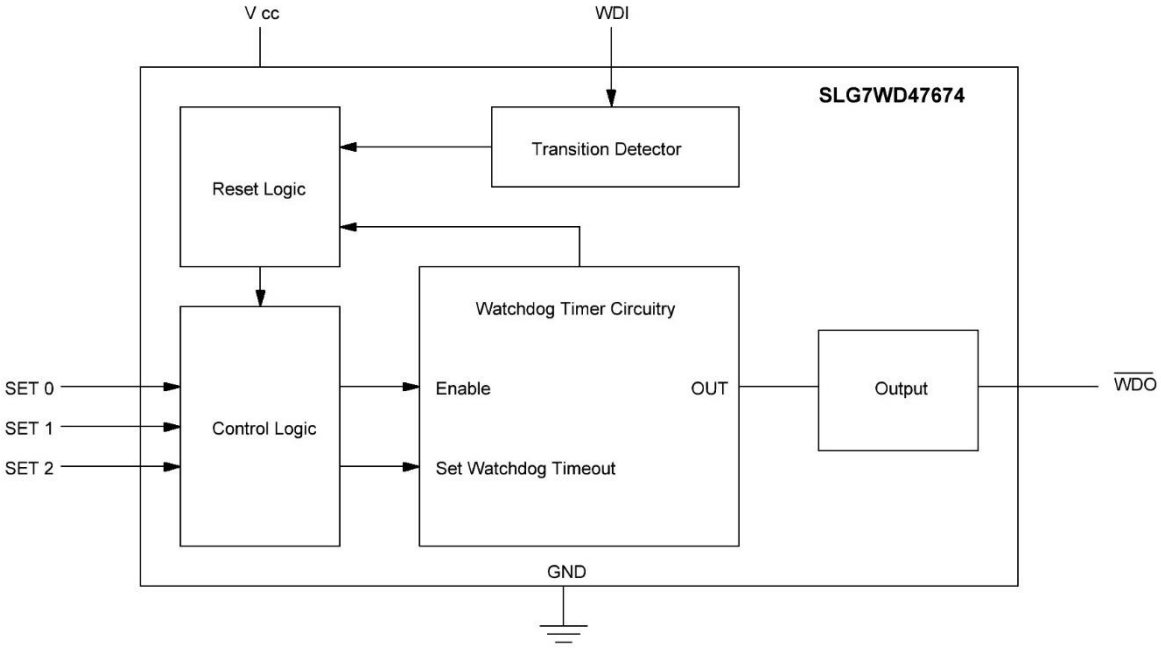


Figure 1. Functional Diagram

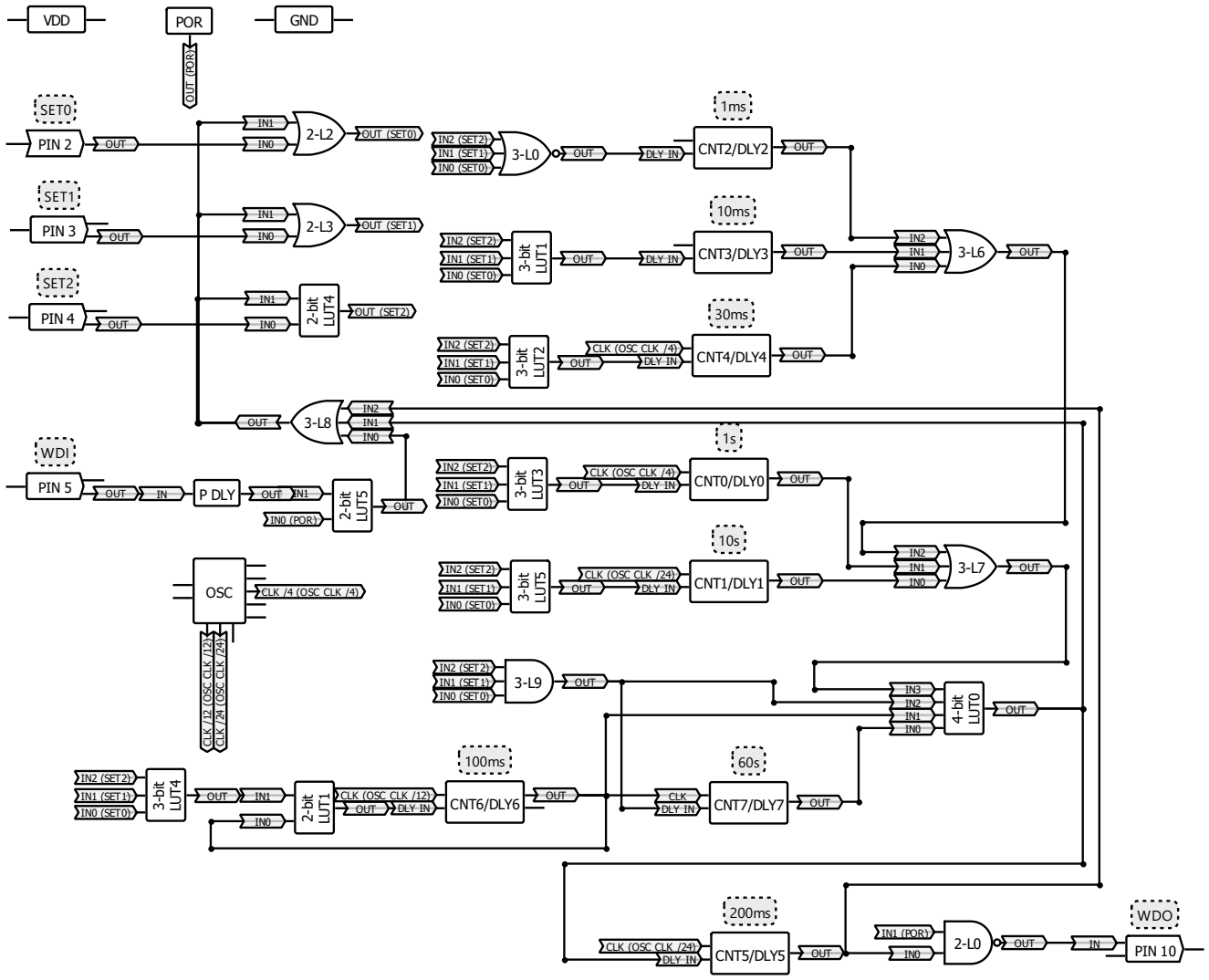


Figure 2. Block Diagram

Table 1. Timeout Settings

Logic Inputs			SLG7WD47674
SET2	**SET1**	**SET0**	t_{WD}
0	0	0	1 ms
0	0	1	10 ms
0	1	0	30 ms
0	1	1	Disabled
1	0	0	100 ms
1	0	1	1 s
1	1	0	10 s
1	1	1	60 s

2. Pin Information

2.1 Pin Assignments

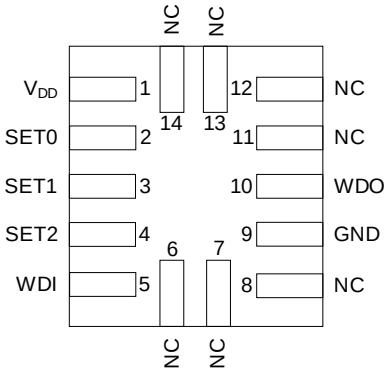


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin #	Pin Name	Type	Description	Internal Resistor
1	V_{DD}	PWR	Supply Voltage	--
2	SET0	Digital Input	Digital Input without Schmitt Trigger	Floating
3	SET1	Digital Input	Digital Input without Schmitt Trigger	Floating
4	SET2	Digital Input	Digital Input without Schmitt Trigger	Floating
5	WDI	Digital Input	Digital Input without Schmitt Trigger	Floating
6	NC	--	Keep Floating or Connect to GND	--
7	NC	--	Keep Floating or Connect to GND	--
8	NC	--	Keep Floating or Connect to GND	--
9	GND	GND	Ground	--
10	WDO	Digital Output	Open-Drain NMOS 1x	Floating
11	NC	--	Keep Floating or Connect to GND	--
12	NC	--	Keep Floating or Connect to GND	--
13	NC	--	Keep Floating or Connect to GND	--
14	NC	--	Keep Floating or Connect to GND	--

3. Specifications

3.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.5	7.0	V
DC Input Voltage		GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current (Through Pin)	OD 1x	--	8	mA
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	+150	°C
Junction Temperature		--	+150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

3.2 Electrical Specifications

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	3.3	5.5	V
Operating Temperature	T_A		-40	+25	+85	°C
Capacitor Value at V_{DD}	C_{VDD}		--	0.1	--	µF
Input Capacitance	C_{IN}		--	4.0	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs. PIN 2 and PIN 3 are HIGH, PIN 4 and PIN 5 are LOW	--	1	--	µA
Maximal Voltage Applied to any Pin in High-Impedance State	V_O		--	--	V_{DD}	V
Maximum Average or DC Current Through V_{DD} Pin (Per Chip Side [2])	I_{VDD}	T_J = +85 °C	--	--	45	mA
		T_J = +110 °C	--	--	22	mA
Maximum Average or DC Current Through GND Pin (Per Chip Side [2])	I_{GND}	T_J = +85 °C	--	--	84	mA
		T_J = +110 °C	--	--	40	mA
HIGH-Level Input Voltage	V_{IH}	Logic input at V_{DD} = 1.8 V	1.10	--	--	V
		Logic input at V_{DD} = 3.3 V	1.78	--	--	V
		Logic input at V_{DD} = 5.0 V	2.64	--	--	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
LOW-Level Input Voltage	V_{IL}	Logic input at V_{DD} = 1.8 V	0	--	0.69	V
		Logic input at V_{DD} = 3.3 V	0	--	1.21	V
		Logic input at V_{DD} = 5.0 V	0	--	1.84	V
LOW-Level Output Voltage	V_{OL}	Open-drain NMOS 1x, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.005	0.020	V
		Open-drain NMOS 1x, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.080	0.147	V
		Open-drain NMOS 1x, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	0.102	0.180	V
LOW-Level Output Current [1]	I_{OL}	Open-drain NMOS 1x, V_{OL} = 0.15 V, V_{DD} = 1.8 V	1.375	2.534	--	mA
		Open-drain NMOS 1x, V_{OL} = 0.4 V, V_{DD} = 3.3 V	7.313	12.370	--	mA
		Open-drain NMOS 1x, V_{OL} = 0.4 V, V_{DD} = 5.0 V	10.820	17.380	--	mA
Delay0 Time	T_{DLY0}	T_A = 25 °C	0.92	1	1.07	s
		T_A = - 40 °C to +85 °C [3]	0.87	1	1.27	s
Delay1 Time	T_{DLY1}	T_A = 25 °C	9.24	10	10.62	s
		T_A = - 40 °C to +85 °C [3]	8.75	10	12.70	s
Delay2 Time	T_{DLY2}	T_A = 25 °C	0.87	1	1.13	ms
		T_A = - 40 °C to +85 °C [3]	0.83	1	1.34	ms
Delay3 Time	T_{DLY3}	T_A = 25 °C	9.19	10	10.68	ms
		T_A = - 40 °C to +85 °C [3]	8.72	10	12.76	ms
Delay4 Time	T_{DLY4}	T_A = 25 °C	27.50	29.92	31.94	ms
		T_A = - 40 °C to +85 °C [3]	26.06	29.92	38.19	ms
Delay5 Time	T_{DLY5}	T_A = 25 °C	183.71	199.68	212.89	ms
		T_A = - 40 °C to +85 °C [3]	174.08	199.68	254.61	ms
Delay6 Time	T_{DLY6}	T_A = 25 °C	91.85	99.84	106.46	ms
		T_A = - 40 °C to +85 °C [3]	87.04	99.84	127.31	ms
Delay7 Time	T_{DLY7}	T_A = 25 °C	57.2	59.7	62.6	s
		T_A = - 40 °C to +85 °C [3]	52.4	59.7	73.6	s
Startup Time	T_{SU}	From V_{DD} rising past 1.35 V	--	0.3	--	ms

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Power-On Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.096	1.353	1.528	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.759	0.933	1.125	V

[1] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
[2] The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, and 8 are connected to one side, pins 10, 11, 12, 13, and 14 to another.
[3] Guaranteed by Design.

4. Typical Application Circuit

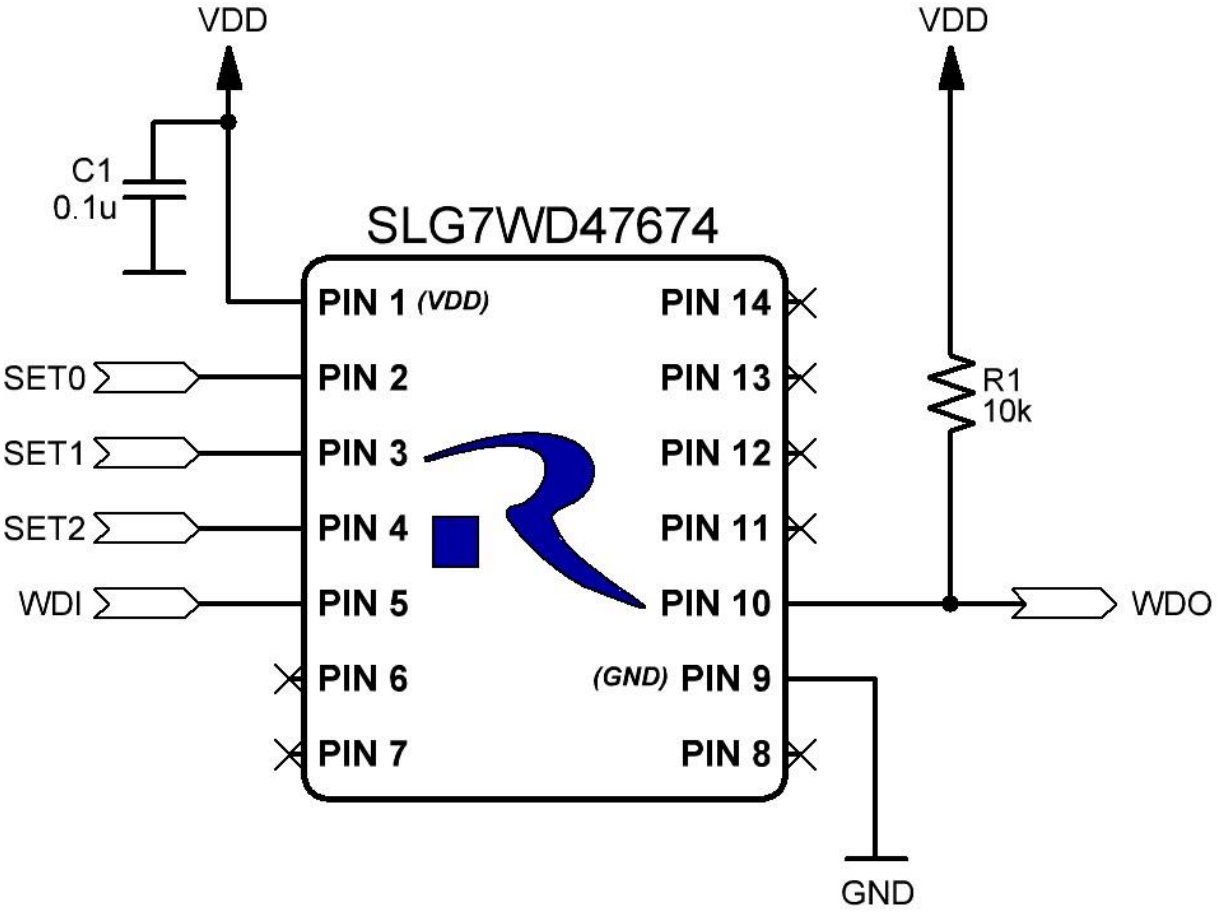
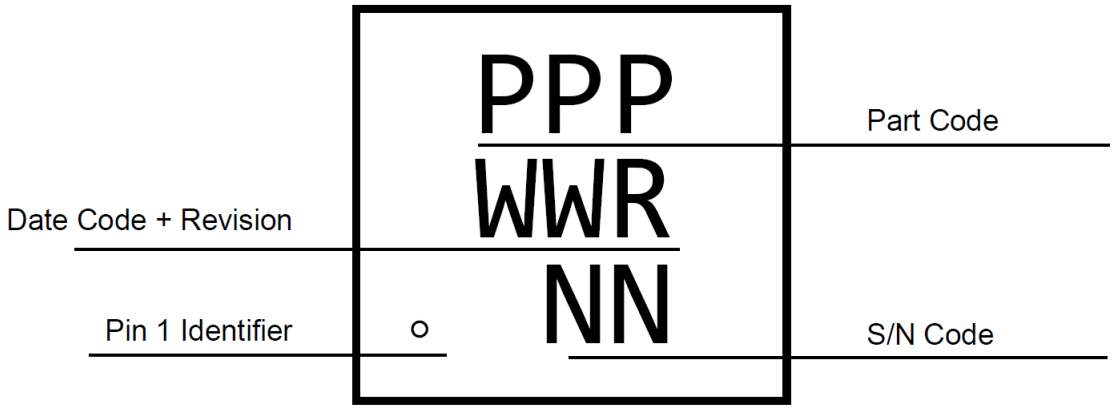


Figure 4. Typical Application Circuit

5. Package Top Marking Definitions

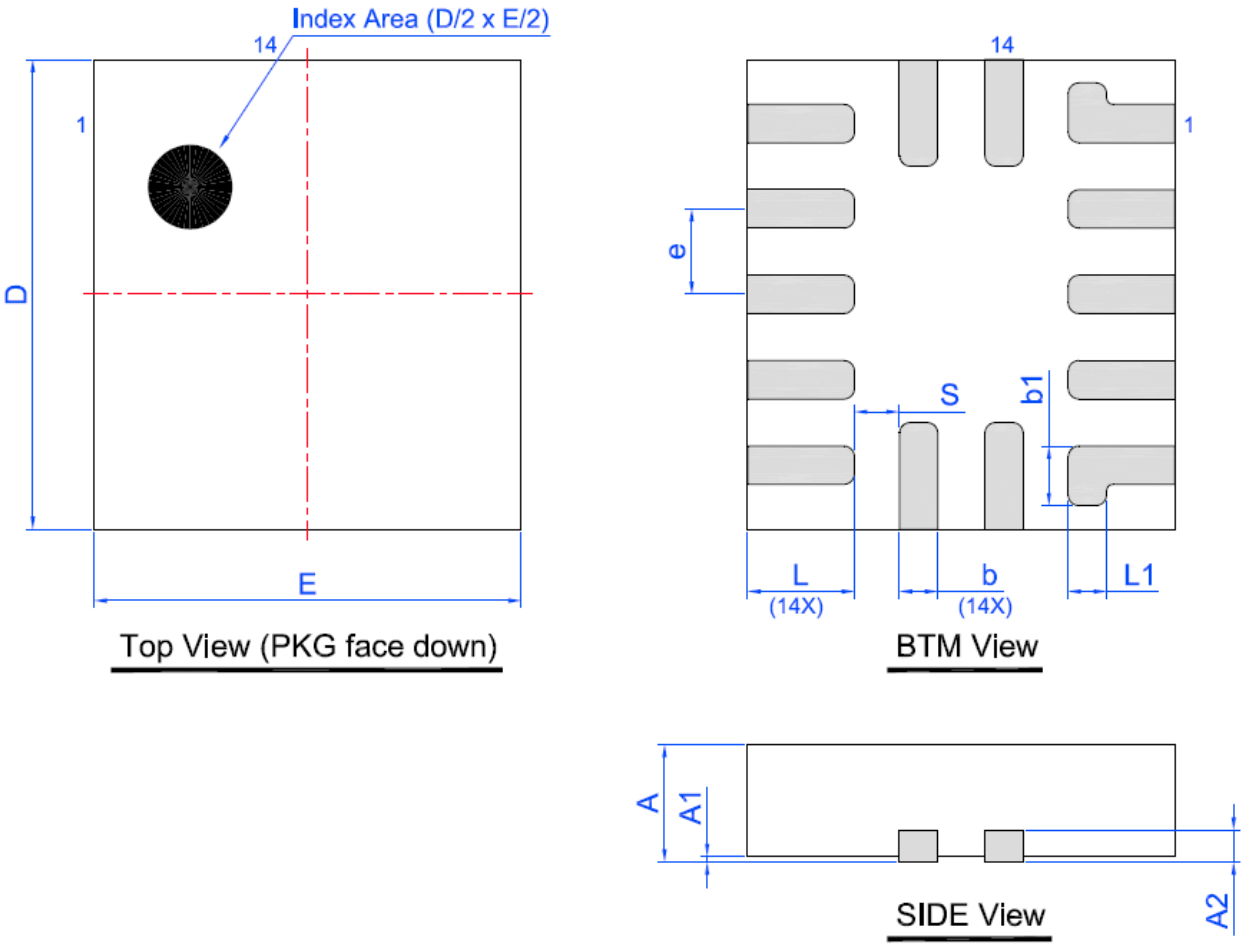


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0xBC00DD44			7/1/2024

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

6. Package Outlines

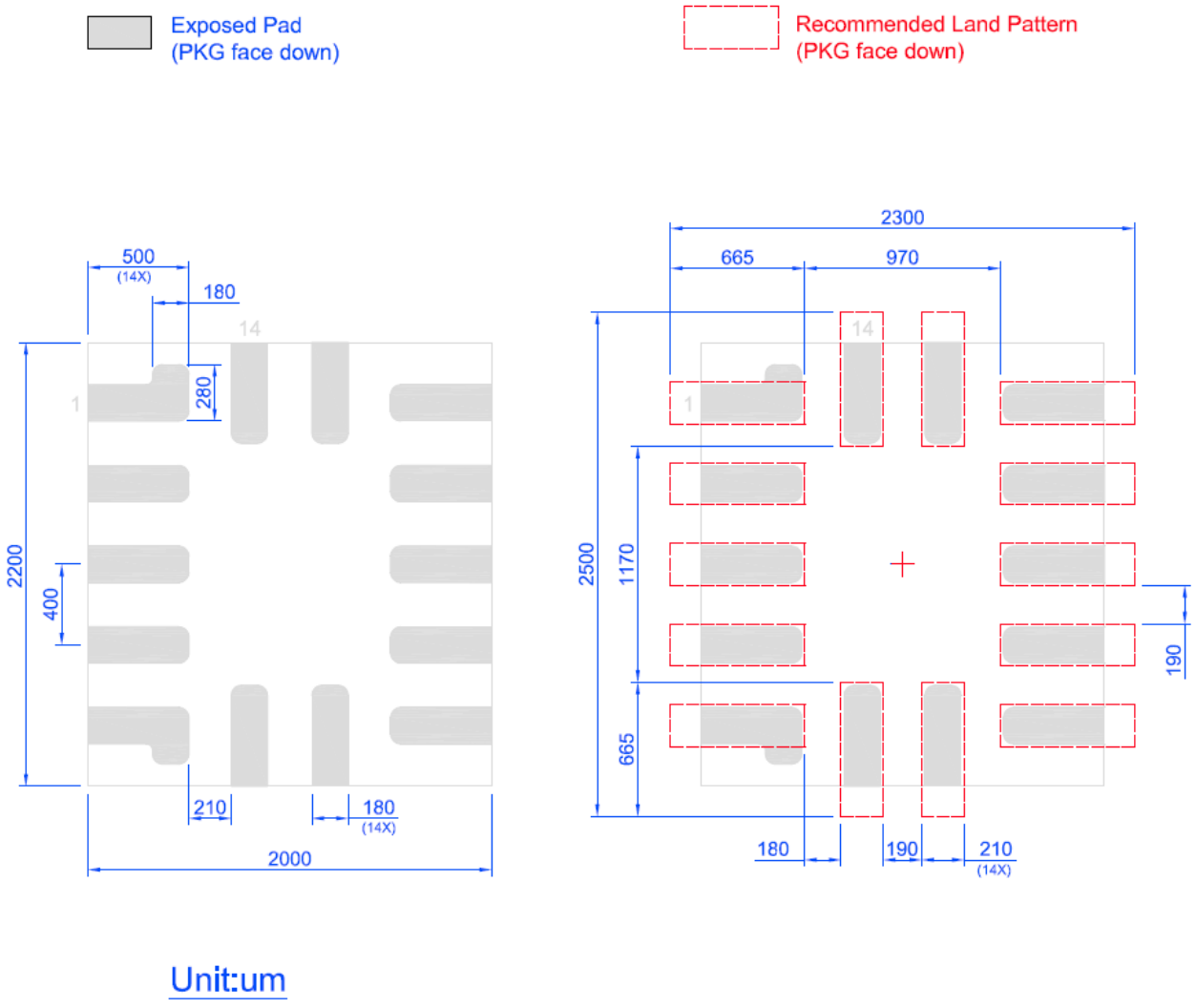
STQFN 14L 2 x 2.2mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.15	2.20	2.25
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.45	0.50	0.55
b	0.13	0.18	0.23	S		0.21 TYP	
e		0.40 BSC		b1		0.28 TYP	
				L1		0.18 TYP	

7. Layout Guidelines



7.1 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.42 mm^3 (nominal). More information can be found at www.jedec.org.

8. Ordering Information

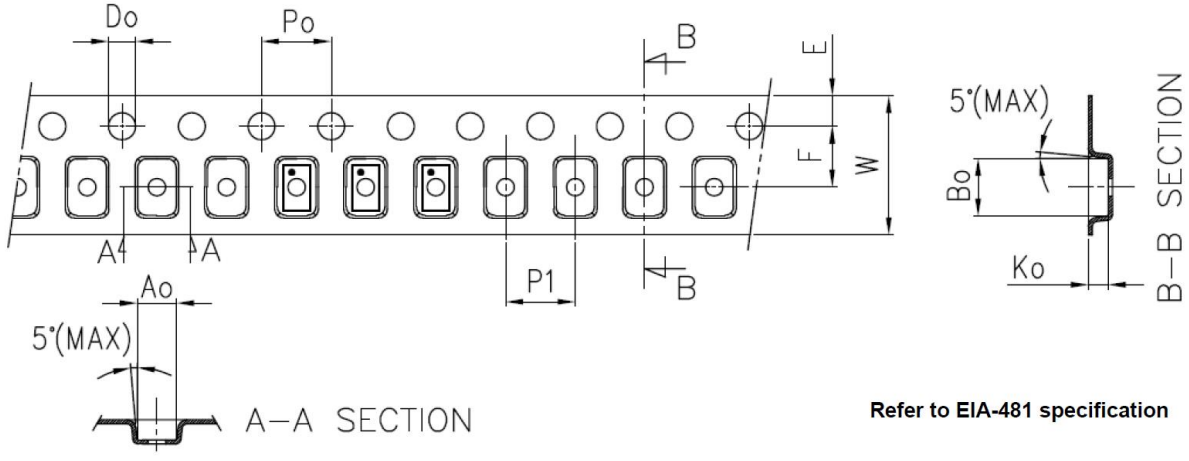
Part Number	Package Type
SLG7WD47674V	14-pin STQFN - Tape and Reel (3k units)

8.1 Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 2.0 mm x 2.2 mm x 0.4P COL	14	2.0x2.2x0.55	3000	3000	178 / 60	100	400	100	400	8	4

8.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 2.0 mm x 2.2 mm x 0.4P COL	2.20	2.35	0.8	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

9. Revision History

Revision	Date	Description
1.00	Dec 20, 2024	Initial release