TP65H035G4WSQA

650V SuperGaN® FET in TO-247 (source tab)

Description

The TP65H035G4WSQA 650V, 35 mΩ gallium nitride (GaN) FET is a normally-off device using Renesas's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

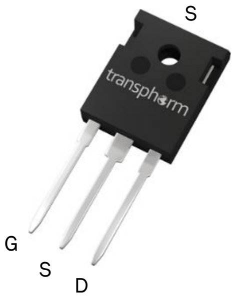
Related Literature

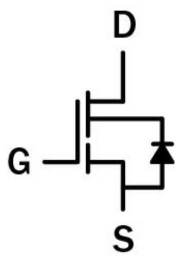
- Recommended External Circuitry for GaN FETs
- Printed Circuit Board Layout and Probing
- Paralleling GaN FETs

Ordering Information

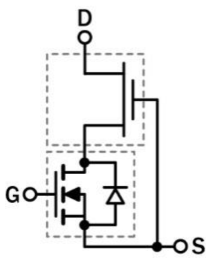
Part Number	Package	Package Configuration
TP65H035G4WSQA	3 lead TO-247	Source

TP65H035G4WSQA
TO-247
(top view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- AEC-Q101 qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - — Wide gate safety margin
  - — Transient over-voltage capability
- Enhanced inrush current capability
- Very low Q_{RR}
- Reduced crossover loss

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - — Increased power density
  - — Reduced system size and weight
  - — Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Automotive
- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications	
V_{DSS} (V)	650
$V_{DSS(TR)}$(V)*	800
$R_{DS(on)eff}$ (mΩ) max**	41
Q_{RR} (nC) typ	150
Q_G (nC) typ	22

*Pulse condition, see note on Page2
* *Dynamic on-resistance; see Figures 19 and 20

Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 175°C)		650	V
$V_{DSS(TR)}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±20	
P_D	Maximum power dissipation @T_C=25°C		187	W
I_D	Continuous drain current @T_C=25°C [b]		47.2	A
	Continuous drain current @T_C=100°C [b]		33.4	A
I_{DM}	Pulsed drain current (pulse width: 10μs)		240	A
T_C	Operating temperature	Case	-55 to +175	°C
T_J		Junction	-55 to +175	°C
T_S	Storage temperature		-55 to +175	°C
T_{SOLD}	Soldering peak temperature [c]		260	°C

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <1μs, spike duration <30μs, nonrepetitive.

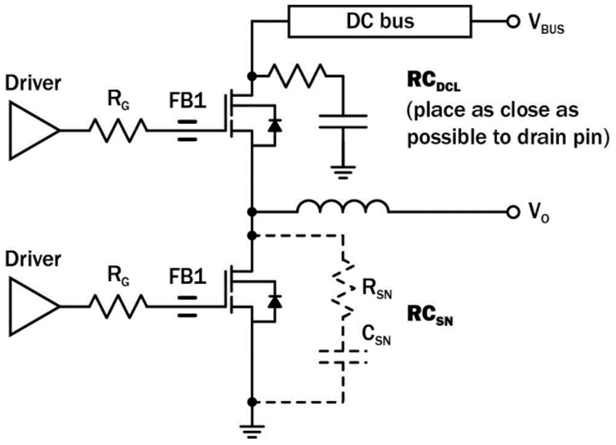
b. For increased stability at high current operation, see Circuit Implementation on page 3

c. For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	0.8	°C/W
$R_{\Theta JA}$	Junction-to-ambient	40	°C/W

Circuit Implementation



Simplified Half-bridge Schematic (See also on Figure 15)

For additional gate driver options/configurations, please see Application Note Recommended External Circuitry for GaN FETs

Layout Recommendations

Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

Power loop: (For reference see page 13)

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Recommended gate drive: (0V, 12V) with R_G= 30Ω

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) [a]	Recommended Switching Node RC Snubber (RC_{SN}) [b]
200 – 270Ω at 100MHz	[4.7nF + 5Ω] x 2	Not necessary [b]

Notes:

a. RC_{DCL} should be placed as close as possible to the drain pin

b. RC_{SN} (100pF + 10Ω) is needed only if R_G is smaller than recommendations

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS(BL)}$	Drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	3.3	4	4.8	V	V_{DS}=V_{GS}, I_D=1mA
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	—	-6.5	—	mV/°C	
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	35	41	mΩ	V_{GS}=10V, I_D=30A
		—	84	—		V_{GS}=10V, I_D=30A, T_J=175°C
I_{DSS}	Drain-to-source leakage current	—	3	30	μA	V_{DS}=650V, V_{GS}=0V
		—	30	—		V_{DS}=650V, V_{GS}=0V, T_J=175°C
I_{GSS}	Gate-to-source forward leakage current	—	—	400	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	—	—	-400		V_{GS}=-20V
C_{ISS}	Input capacitance	—	1500	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	147	—		
C_{RSS}	Reverse transfer capacitance	—	5	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	220	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	380	—		
Q_G	Total gate charge	—	22	—	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=32A
Q_{GS}	Gate-source charge	—	8.4	—		
Q_{GD}	Gate-drain charge	—	6.6	—		
Q_{OSS}	Output charge	—	150	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	60	—	ns	V_{DS}=400V, V_{GS}=0V to 12V, R_G=30Ω, I_D=32A, Z_{FB}=240Ω at 100MHz (See Figure 15)
t_R	Rise time	—	10	—		
$t_{D(off)}$	Turn-off delay	—	94	—		
t_F	Fall time	—	10	—		
E_{off}	Turn off Energy	—	82	—	μJ	V_{DS}=400V, V_{GS}=0V to 12V, R_G=30Ω, I_D=32A, Z_{FB}=180Ω at 100MHz
E_{on}	Turn on Energy	—	206	—	μJ	

Notes:

a. Dynamic on-resistance; see Figures 19 and 20 for test circuit and conditions

b. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V

c. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	33.4	A	V_{GS}=0V, T_C=100°C ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	1.8	—	V	V_{GS}=0V, I_S=32A
		—	1.3	—		V_{GS}=0V, I_S=16A
t_{RR}	Reverse recovery time	—	59	—	ns	I_S=32A, V_{DD}=400V, di/dt=1000A/ms
Q_{RR}	Reverse recovery charge	—	150	—	nC	
$(di/dt)_{RM}$	Reverse diode di/dt [b]	—	—	3200	A/µs	Circuit implementation and parameters on page 3

Notes:

a. Includes dynamic $R_{DS(on)}$ effect

b. Reverse conduction di/dt will not exceed this max value with recommended R_G.

Typical Characteristics (T_c=25°C unless otherwise stated)

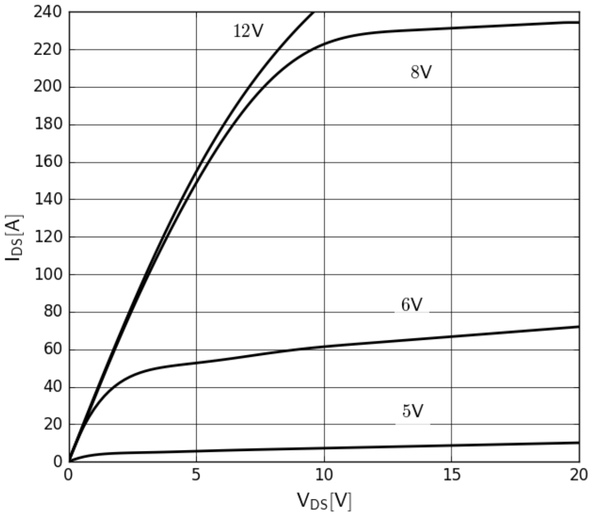


Figure 1. Typical Output Characteristics T_J=25°C

Parameter: V_{GS}

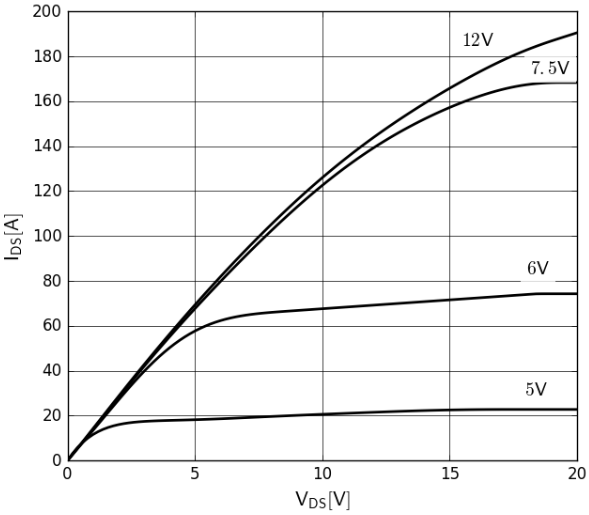


Figure 2. Typical Output Characteristics T_J=175°C

Parameter: V_{GS}

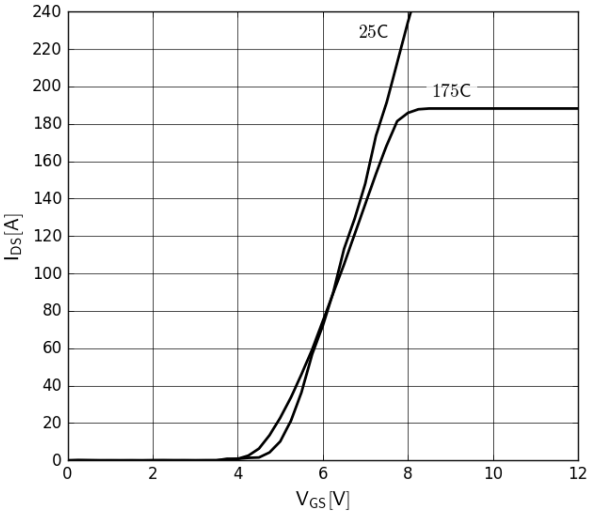


Figure 3. Typical Transfer Characteristics

V_{DS}=20V, parameter: T_J

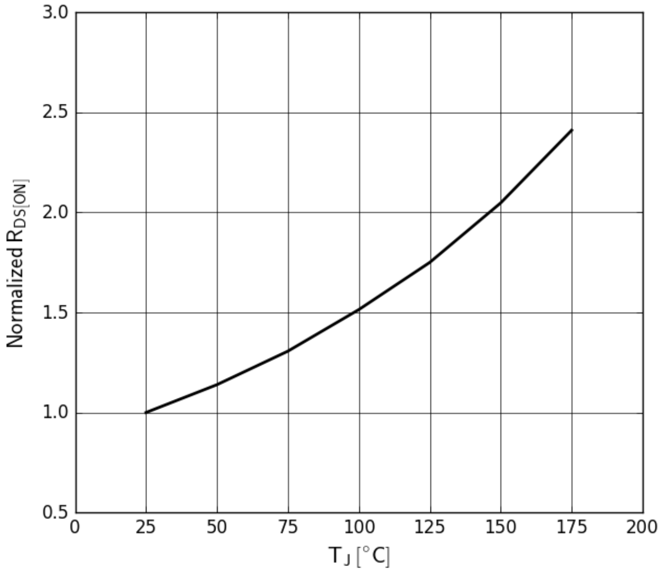
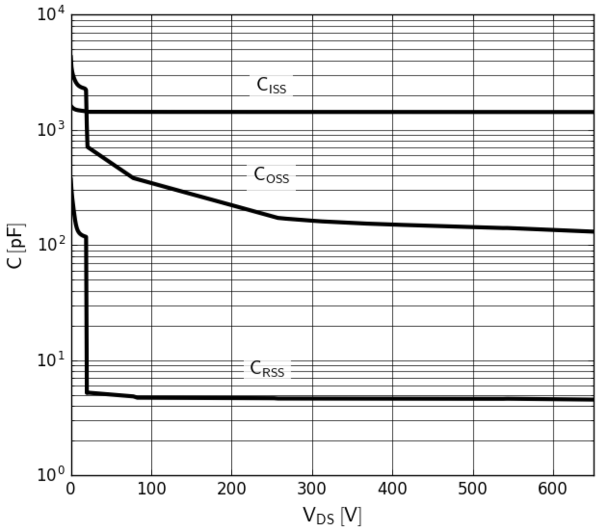


Figure 4. Normalized On-resistance

I_D=30A, V_{GS}=10V

Typical Characteristics (T_c=25 ° C unless otherwise stated)



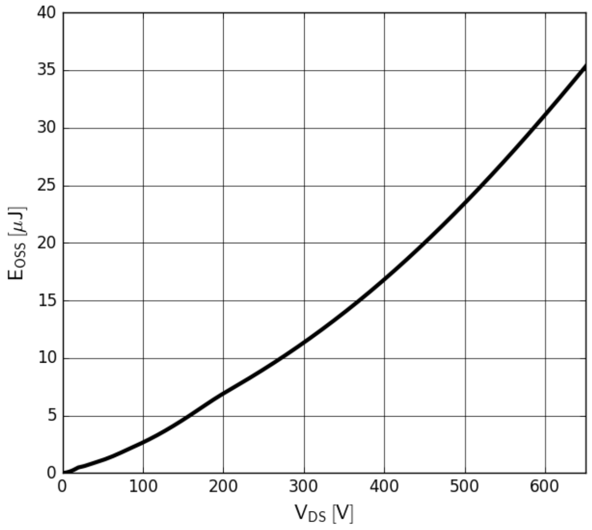
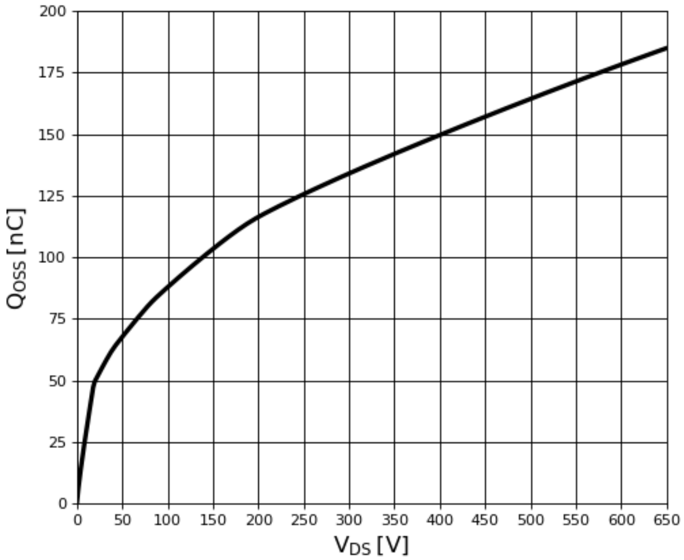


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHz

Figure 6. Typical C_{OSS} Stored Energy



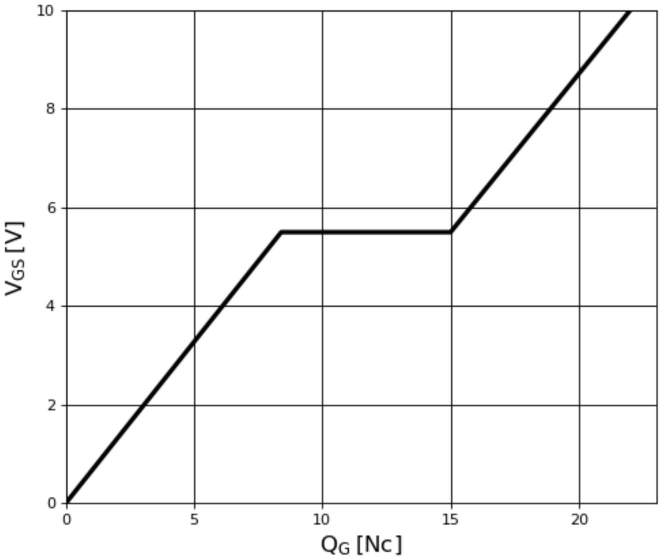
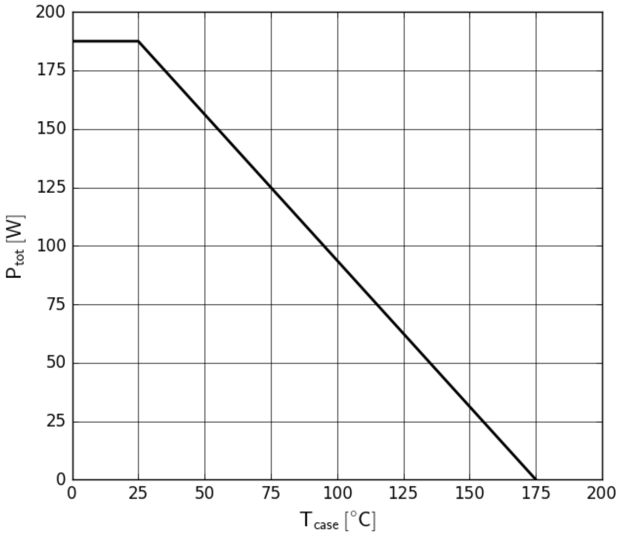


Figure 7. Typical Q_{OSS}

Figure 8. Typical Gate Charge

I_{DS}=32A, V_{DS}=400V

Typical Characteristics (T_c=25 °C unless otherwise stated)



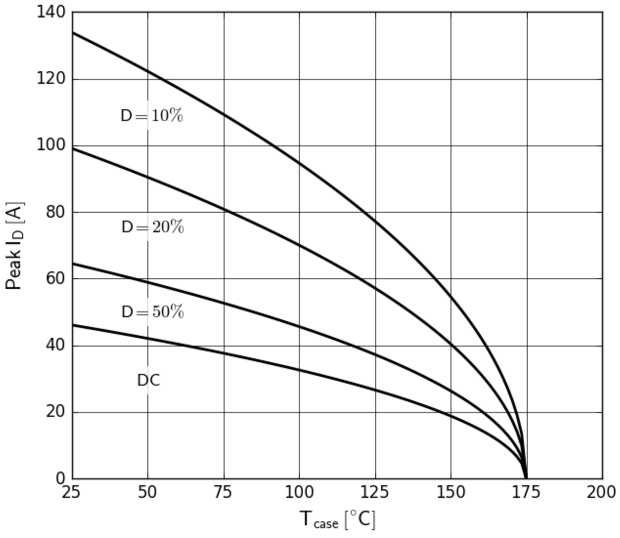
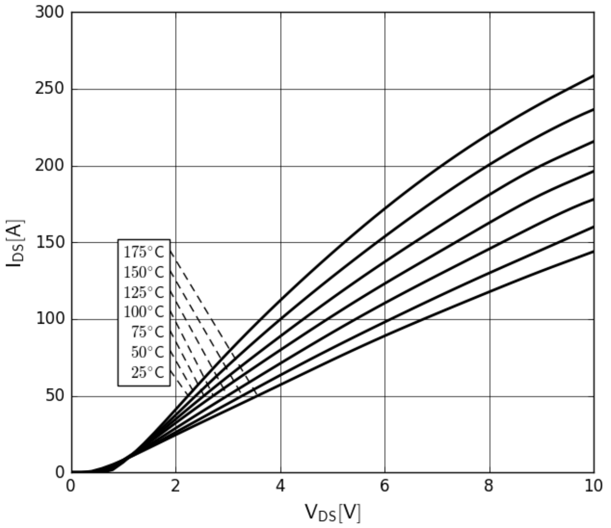


Figure 9. Power Dissipation

Figure 10. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 10V



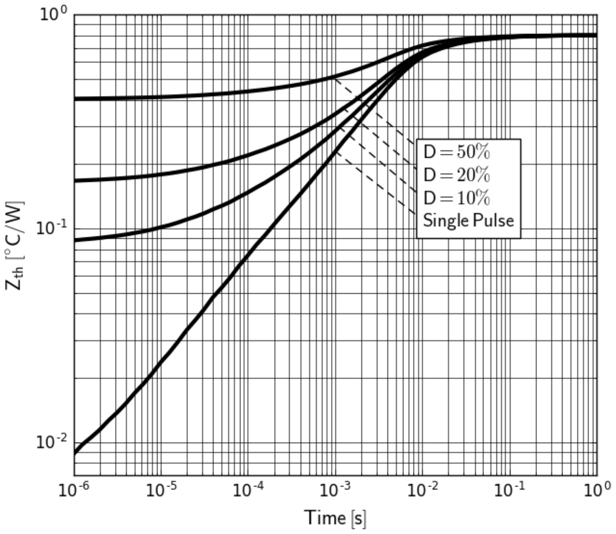


Figure 11. Forward Characteristics of Rev. Diode

I_S=f(V_{SD}), parameter: T_J

Figure 12. Transient Thermal Resistance

Typical Characteristics (T_c=25 °C unless otherwise stated)

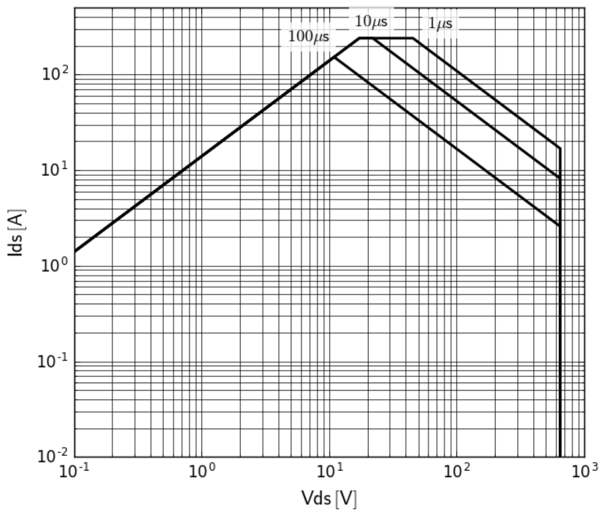


Figure 13. Safe Operating Area T_C=25 °C

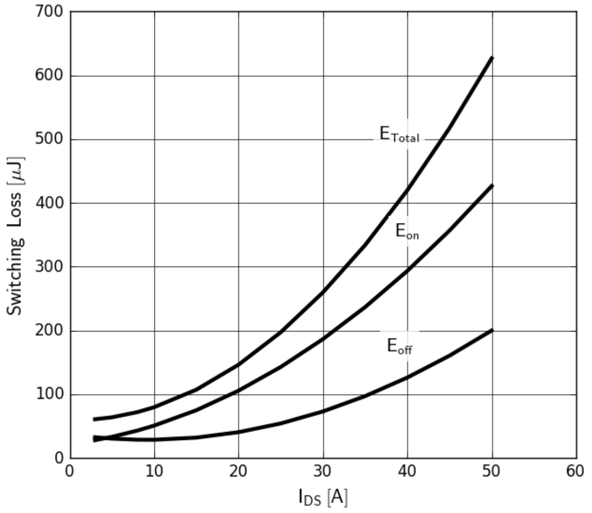


Figure 14. Inductive Switching Loss

Rg=30Ω, V_{DS}=400V

Test Circuits and Waveforms

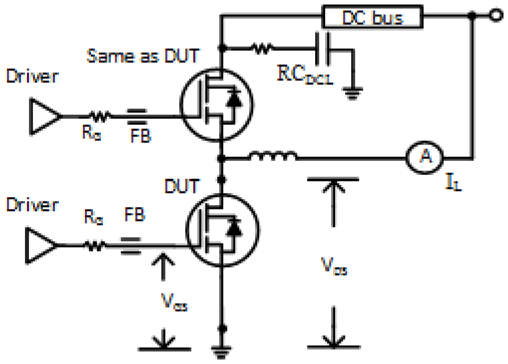


Figure 15. Switching Time Test Circuit

(see circuit implementation on page 3 for methods to ensure clean switching)

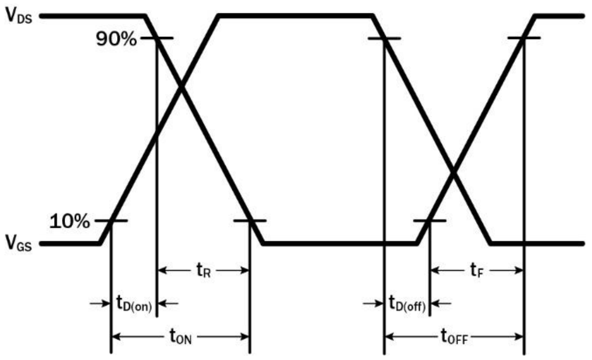


Figure 16. Switching Time Waveform

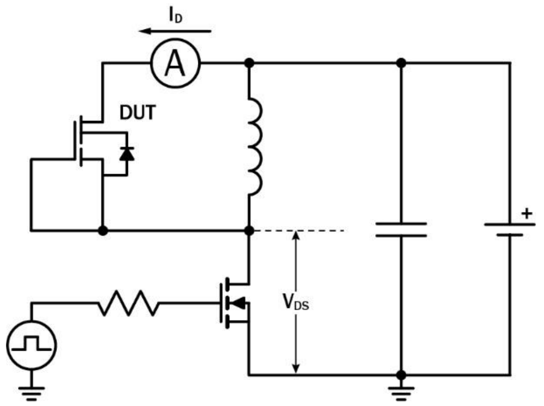


Figure 17. Diode Characteristics Test Circuit

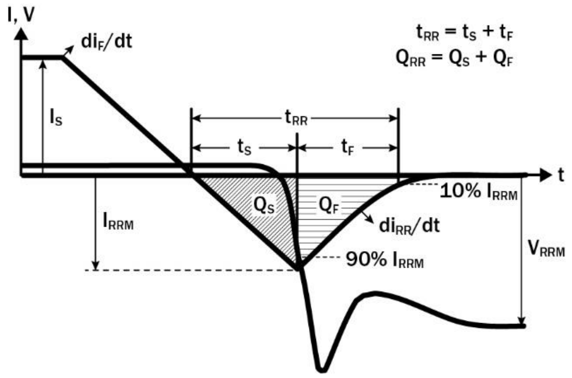


Figure 18. Diode Recovery Waveform

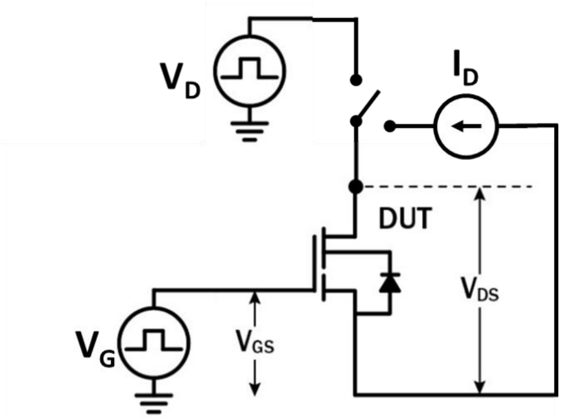


Figure 19. Dynamic $R_{DS(on)eff}$ Test Circuit

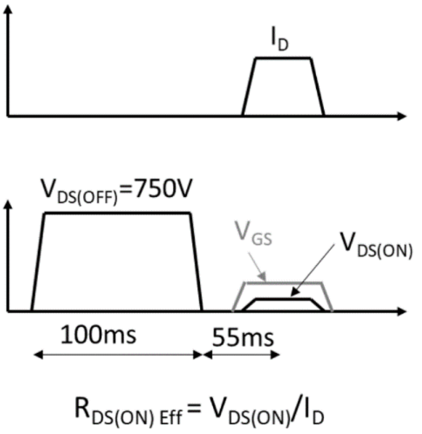


Figure 20. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See Printed Circuit Board Layout and Probing	

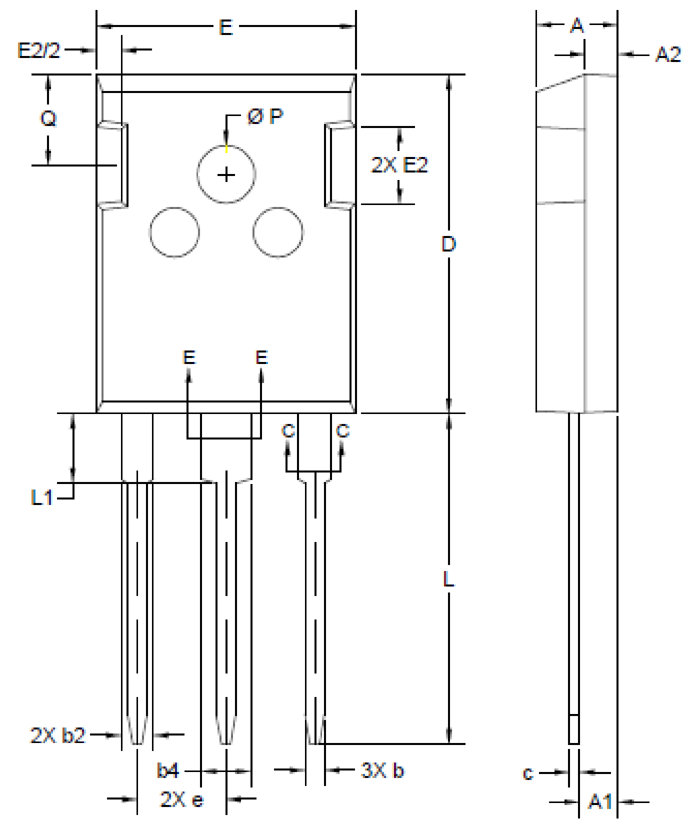
GaN Design Resources

The complete technical library of GaN design tools can be found at Renesasusa.com/design:

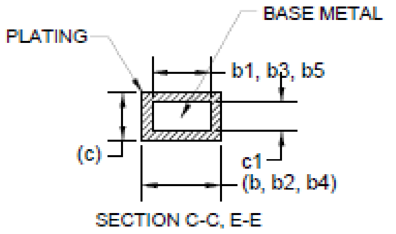
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical

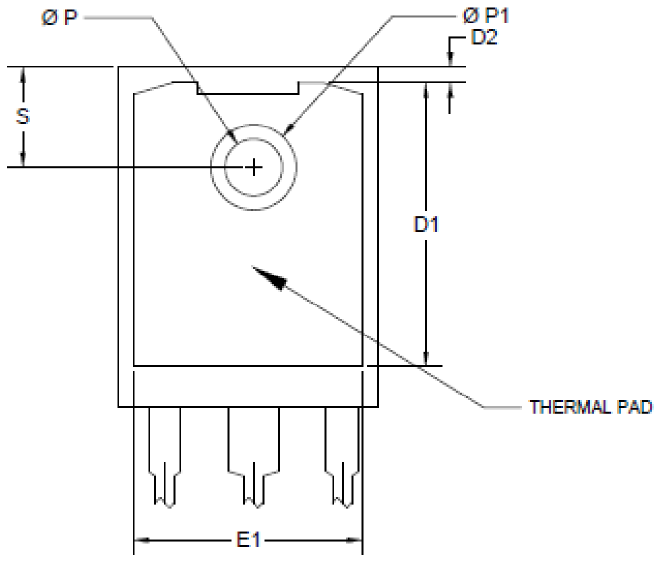
3 Lead TO-247 Package



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.82	5.00	5.19	0.190	0.197	0.204
A1	2.20	2.39	2.57	0.087	0.094	0.101
A2	1.82	2.01	2.18	0.072	0.079	0.086
b	1.09	1.19	1.35	0.043	0.047	0.053
b1	1.09	-	1.30	0.043	-	0.051
b2	1.87	2.03	2.31	0.074	0.080	0.091
b3	1.87	-	2.27	0.074	-	0.089
b4	2.94	3.05	3.22	0.116	0.120	0.127
b5	2.94	-	3.18	0.116	-	0.125
c	0.50	0.58	0.68	0.020	0.023	0.027
c1	0.50	-	0.64	0.020	-	0.025
D	20.67	20.85	21.11	0.814	0.821	0.831
D1	17.20	-	17.63	0.677	-	0.694
D2	0.81	-	1.20	0.032	-	0.048
E	15.72	15.90	16.15	0.619	0.626	0.636
E1	13.79	-	14.25	0.543	-	0.561
E2	4.30	-	4.86	0.169	-	0.191
e	5.46 BSC			0.215 BSC		
L	19.55	19.94	20.38	0.770	0.785	0.802
L1	3.93	4.11	4.48	0.155	0.162	0.176
ØP	3.50	3.61	3.69	0.138	0.142	0.145
ØP1	7.08	7.19	7.32	0.279	0.283	0.288
Q	5.41	-	5.85	0.213	-	0.230
S	6.15 BSC			0.242 BSC		



SECTION C-C, E-E



NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.

2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.

3. LEAD FINISH UNCONTROLLED IN L1.

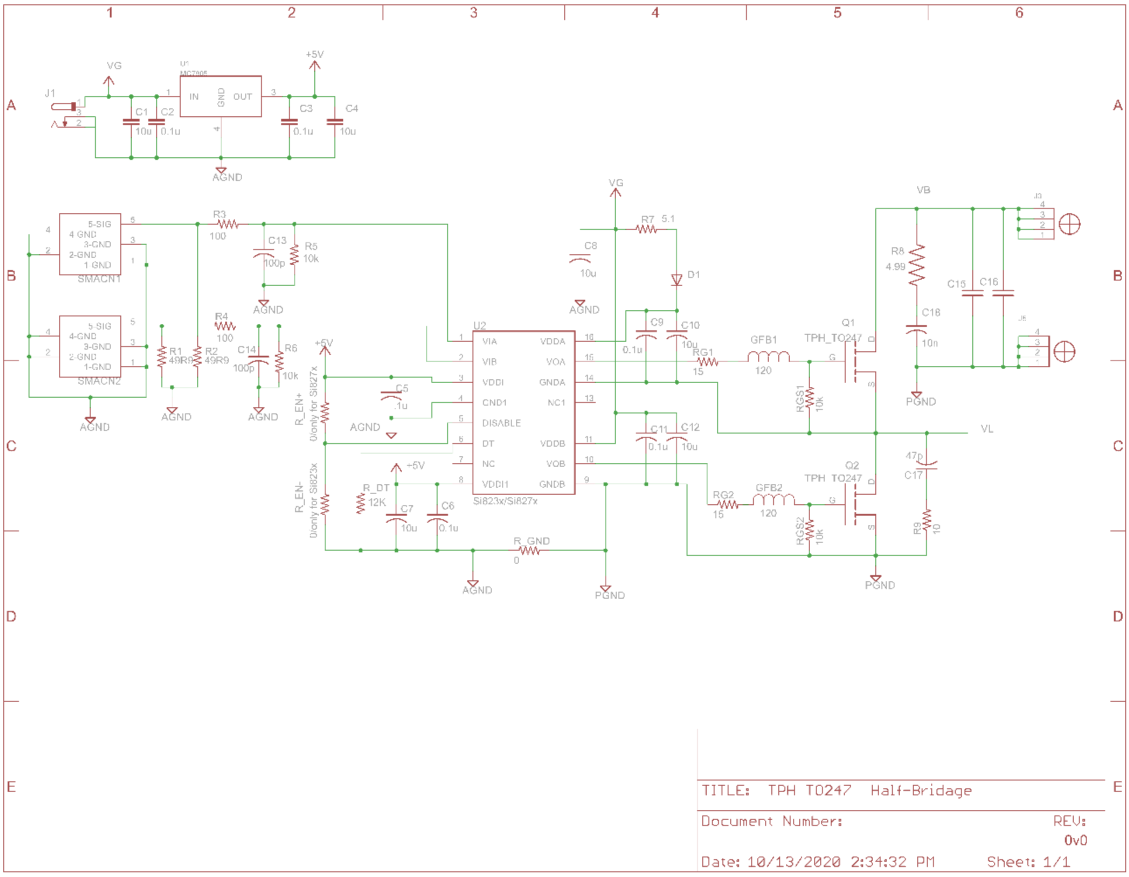
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

TO-247 3L

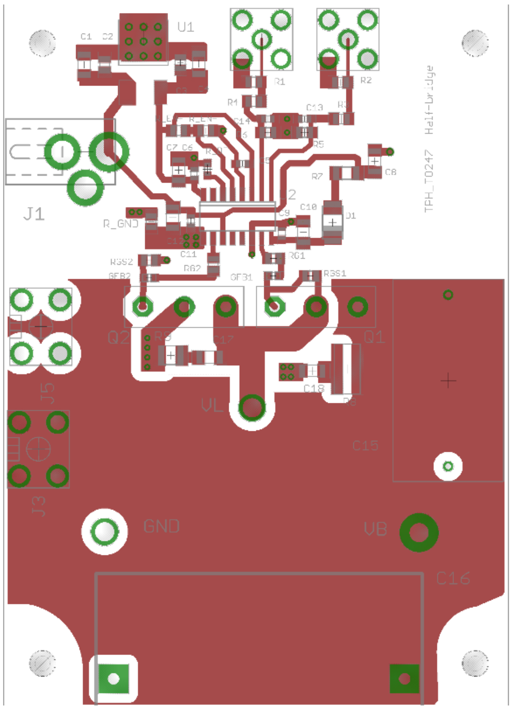
transphorm

SCALE: 1:1	SHEET 1/1	DRAWING NO. 200019	VER. 3

Half-bridge Reference Schematic and PCB Layout



Half-bridge layout Sample (Top Layer)



Half-bridge layout Sample (Bottom Layer)