TP65H070G4LSGBEA

650V SuperGaN® GaN FET in PQFN 8 × 8 Industry Standard Package (source tab)

Description

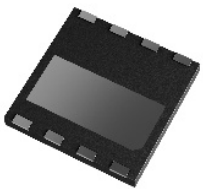
The TP65H070G4LSGBEA 650V, 72mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a high-voltage GaN HEMT with a low-voltage silicon MOSFET to offer superior reliability and performance while enabling reduced system size and cost.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

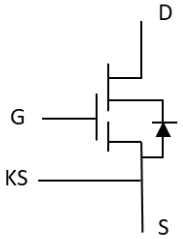
Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with Si gate drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required

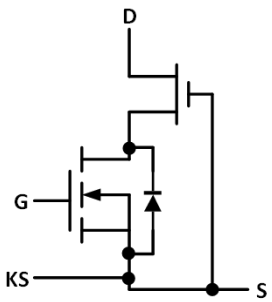
Product and Schematic Diagrams



TP65H070G4LSGBEA PQFN 8 × 8 IP



Cascode Schematic Symbol



Cascode Device Structure

(MOSFET has integrated ESD Protection Circuit)

Features

- Ultra-fast switching Gen IV GaN technology
- JEDEC-qualified GaN technology
- Dynamic R_{DS}(on)eff production tested
- Robust design, defined by:
  - Transient over-voltage capability
  - Operation with E-mode gate drivers without need for Zener protection
- Reduced crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- Consumer and industrial power supply
- Power adapters
- PV Inverter
- Lighting
- UPS
- BESS

Key Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V)	800
$R_{DS(on)}$ (mΩ) maximum [1]	85
Q_{OSS} (nC) typical	64
Q_G (nC) typical	11.9

1. Dynamic RDS(on); see Figure 18 and Figure 19.

Contents

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1. Pin Information

1.1 Pin Assignments

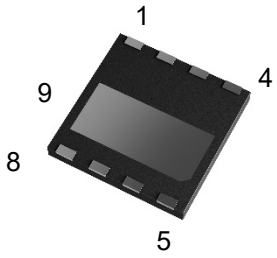


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4	D	Drain.
5, 6	S	Source.
7	KS	Kelvin source.
8	G	Gate.
9	S	Source.

2. Specifications

2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	-	650	V
$V_{DSS(TR)\ ,\ non\text{-}repetitive}$	Transient drain to source voltage, non-repetitive [1]	-	800	
$V_{DSS(TR)\ ,\ repetitive}$	Transient drain to source voltage, repetitive [2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at T_C = 25°C	-	125	W
I_D	Continuous drain current at T_C = 25°C	-	29	A
	Continuous drain current at T_C = 100°C	-	18.4	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	-	120	A
T_J	Junction operating temperature	-55	+150	°C
T_S	Storage temperature	-55	+150	°C
T_{SOLD}	Reflow soldering temperature [3]	-	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. Off-state, spike duration < 5µs, repetitive.
3. Reflow MSL3.

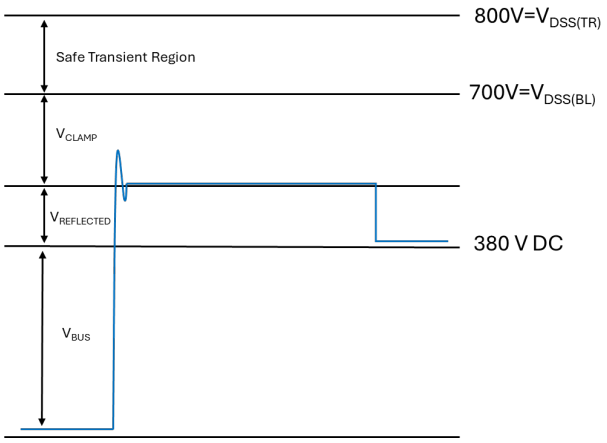


Figure 2. Transient Behavior at Turn-off

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	1	°C/W
$R_{\Theta JA}$	Junction-to-ambient [1]	62	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm^2 copper area and 70µm thickness).

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.5mA	3.2	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-	-5.8	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 12V, I_D = 18A	-	72	85	mΩ
		V_{GS} = 12V, I_D = 18A, T_J = 150°C	-	148	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V	-	3	30	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	12	-	
I_{GSS}	Gate-to-source forward leakage current [2]	V_{GS} = 20V	-	-	10	μA
	Gate-to-source reverse leakage current [2]	V_{GS} = -20V	-	-	-10	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	588	-	pF
C_{OSS}	Output capacitance		-	64	-	
C_{RSS}	Reverse transfer capacitance		-	4	-	
$C_{O(er)}$	Output capacitance, energy related [3]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	91	-	pF
$C_{O(tr)}$	Output capacitance, time related [4]		-	159	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 18A	-	11.9	-	nC
Q_{GS}	Gate-source charge		-	3.5	-	
Q_{GD}	Gate-drain charge		-	4.7	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	64	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 18A, R_G = 20Ω, ZFB = 120Ω at 100MHz (see Figure 16)	-	26	-	ns
t_R	Rise time		-	4	-	
$t_{D(off)}$	Turn-off delay		-	51	-	
t_F	Fall time		-	6	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 18 and Figure 19 for conditions.
2. Including leakage current of the integrated ESD protection circuit.
3. Equivalent capacitance to give same stored energy from 0V to 400V.
4. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	18	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 9A	-	1.5	-	V
		V_{GS} = 0V, I_S = 18A	-	2.1	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible enabled by the LV Si FET technology.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

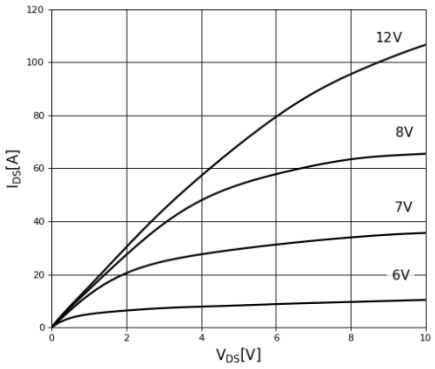


Figure 3. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

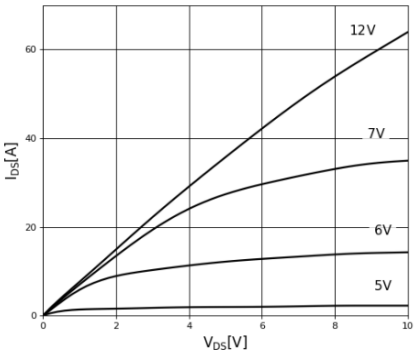


Figure 4. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

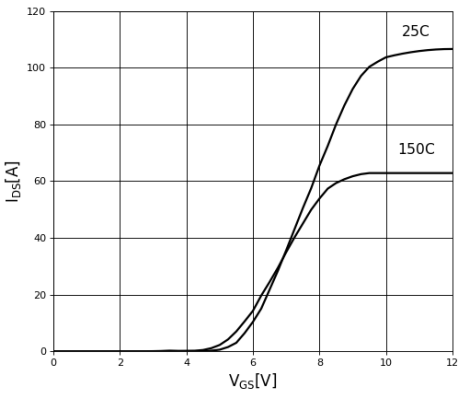


Figure 5. Typical Transfer Characteristics

V_{DS} = 10V, Parameter: T_J

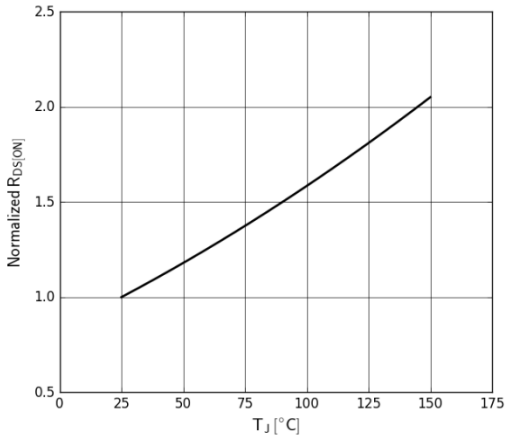


Figure 6. Normalized On-resistance

I_D = 18A, V_{GS} = 12V

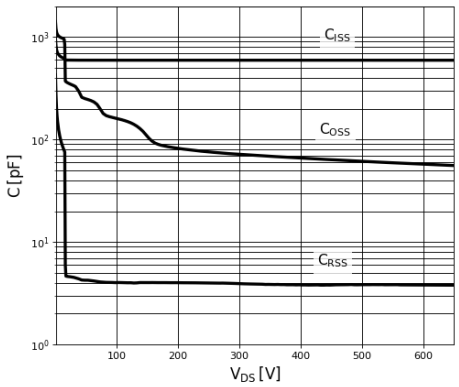


Figure 7. Typical Capacitance

V_{GS} = 0V, f = 1MHz

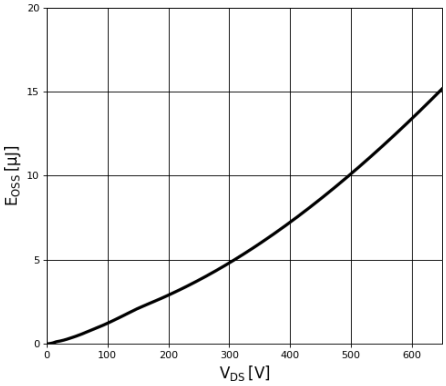


Figure 8. Typical C_{OSS} Stored Energy

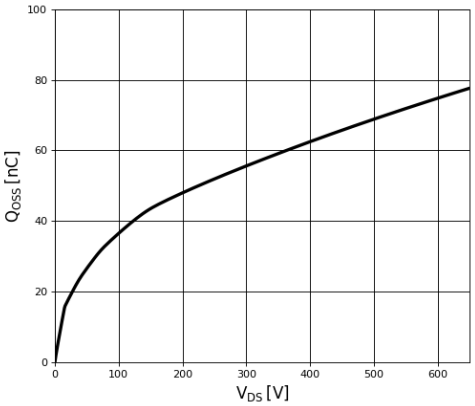


Figure 9. Typical Q_{OSS}

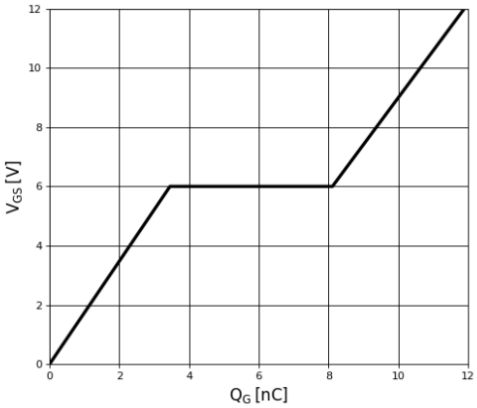


Figure 10. Typical Gate Charge

I_{DS} = 18A, V_{DS} = 400V

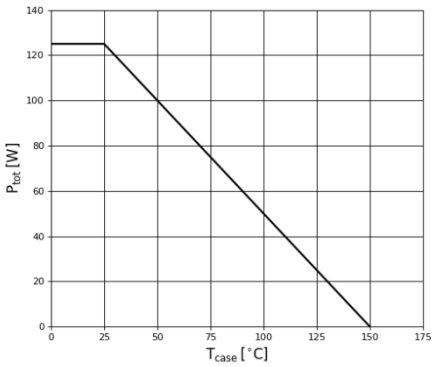


Figure 11. Power Dissipation

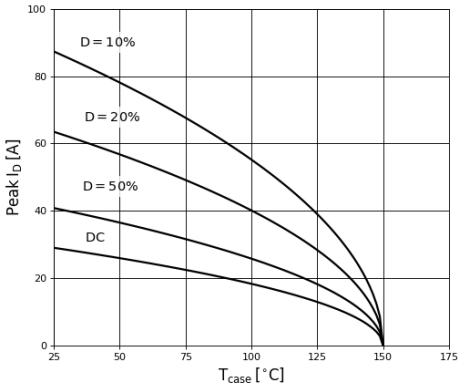


Figure 12. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 10V

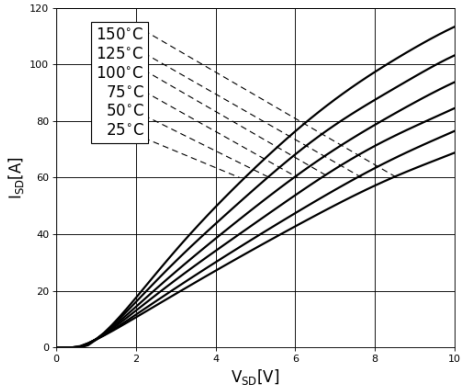


Figure 13. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

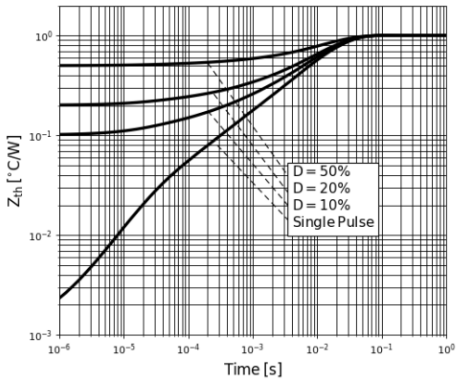


Figure 14. Transient Thermal Resistance

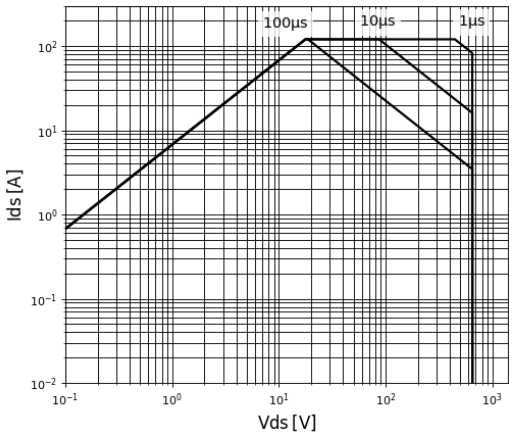


Figure 15. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

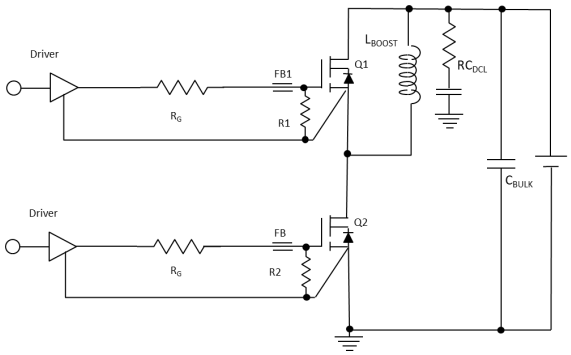


Figure 16. Switching Time Test Circuit

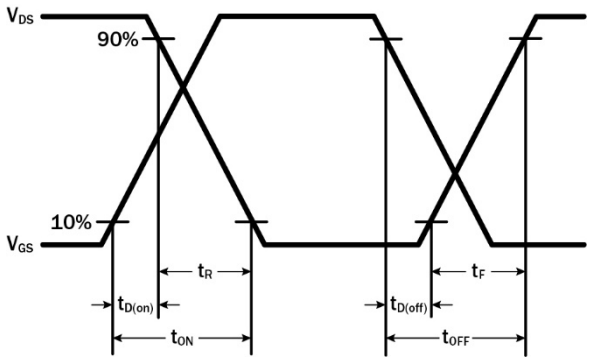


Figure 17. Switching Time Waveform

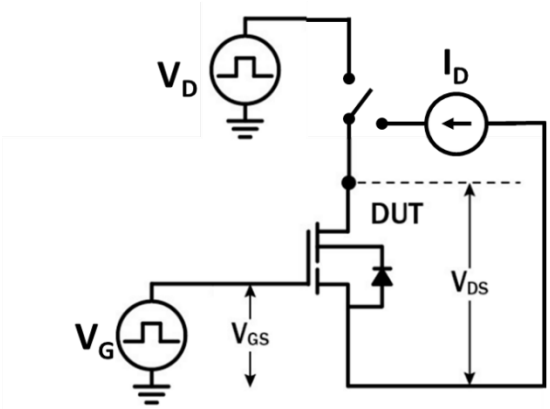


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

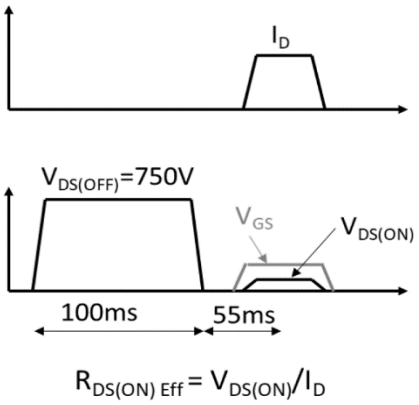
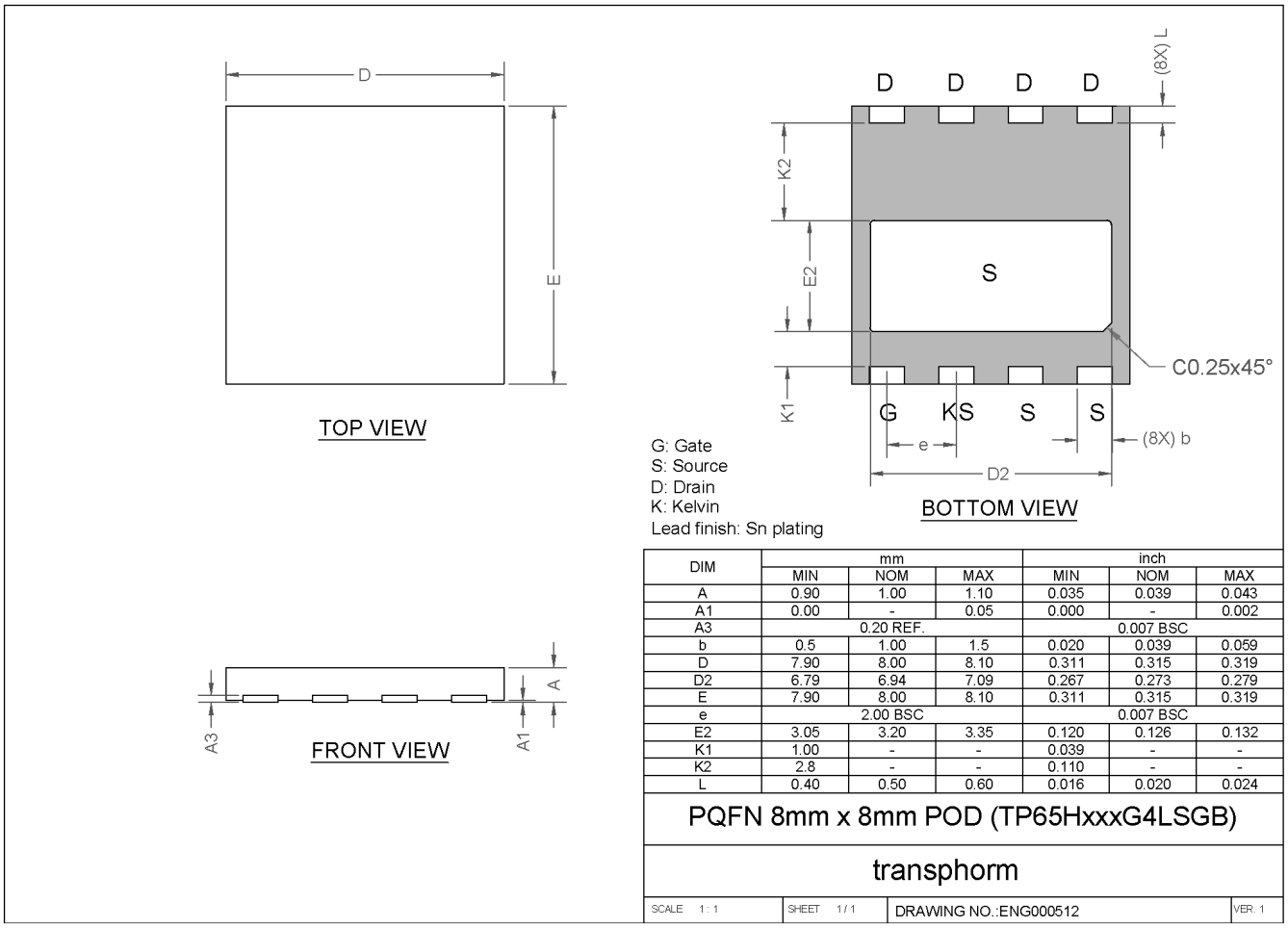


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 REF.			0.007 BSC	
b	0.5	1.00	1.5	0.020	0.039	0.059
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.79	6.94	7.09	0.267	0.273	0.279
E	7.90	8.00	8.10	0.311	0.315	0.319
e		2.00 BSC			0.007 BSC	
E2	3.05	3.20	3.35	0.120	0.126	0.132
K1	1.00	-	-	0.039	-	-
K2	2.8	-	-	0.110	-	-
L	0.40	0.50	0.60	0.016	0.020	0.024

PQFN 8mm x 8mm POD (TP65HxxxG4LSGB)

transphorm

SCALE 1 : 1 | SHEET 1 / 1 | DRAWING NO.:ENG000512 | VER. 1

Figure 20. 8 × 8 mm PQFN Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H070G4LSGBEA-TR [1]	8 × 8 mm PQFN IP	Source tab

1. "-TR" suffix refers to tape and reel.

8. Revision History

Revision	Date	Description
2.00	Nov 25, 2025	Updated the document's formatting; no technical changes were completed
1.00	Jul 25, 2025	Initial release.

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