TP65H070G4PS

650V SuperGaN® GaN FET in TO-220 (source tab)

Description

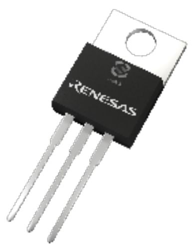
The TP65H070G4PS 650V, 72mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines a state-of-the-art high-voltage GaN HEMT with a low-voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

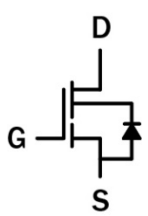
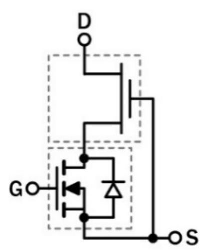
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

Product and Schematic Diagrams



TP65H070G4PS TO-220

	
Cascode Schematic Symbol	**Cascode Device Structure**

Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Reduced crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	85
Q_{OSS} (nC) typical	78
Q_G (nC) typical	9

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

Contents

Figures

1. Pin Information

1.1 Pin Assignments

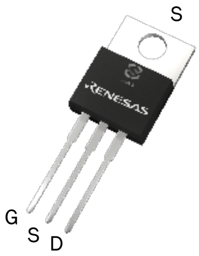


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Name	Description
D	Drain.
S	Source.
G	Gate.

2. Specifications

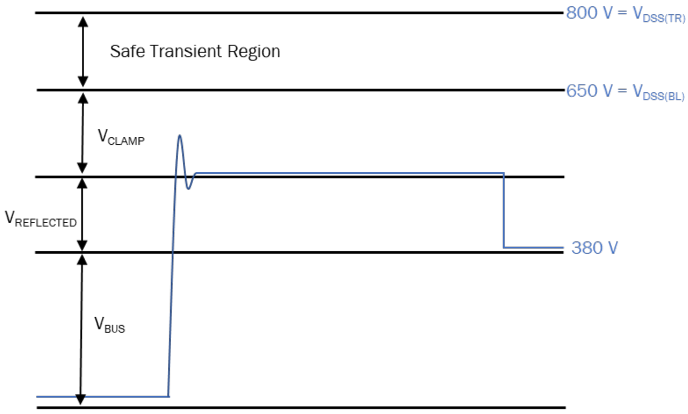
2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	650	V
$V_{DSS(TR)}$	Transient drain to source voltage [1]	800	
V_{GSS}	Gate to source voltage	+20	
P_D	Maximum power dissipation at T_C = 25°C	96	W
I_D	Continuous drain current at T_C = 25°C	29	A
	Continuous drain current at T_C = 100°C	18.4	A
I_{DM}	Pulsed drain current (pulse width: 10μs)	120	A
T_J	Junction operating temperature	-55 to +150	°C
T_S	Storage temperature	-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [2]	260	°C

1. In off-state, spike duration < 30μs, non-repetitive.
2. Reflow MSL3.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	1	°C/W
$R_{\Theta JA}$	Junction-to-ambient [1]	62	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V, I_D = 1mA	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.7mA	3.3	4	4.8	V
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 10V, I_D = 18A, T_J = 25°C	-	72	85	mΩ
		V_{GS} = 10V, I_D = 18A, T_J = 150°C	-	148	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	1.2	12	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	8	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz	-	638	-	pF
C_{OSS}	Output capacitance		-	72	-	
C_{RSS}	Reverse transfer capacitance		-	2	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	105	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	194	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 18A	-	9	-	nC
Q_{GS}	Gate-source charge		-	3.7	-	
Q_{GD}	Gate-drain charge		-	2.4	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	78	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 18A, R_G = 50Ω (see Figure 15)	-	43.4	-	ns
t_R	Rise time		-	6.2	-	
$t_{D(off)}$	Turn-off delay		-	56	-	
t_F	Fall time		-	7.2	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	18	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 18A	-	2.4	-	V
		V_{GS} = 0V, I_S = 9A	-	1.7	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

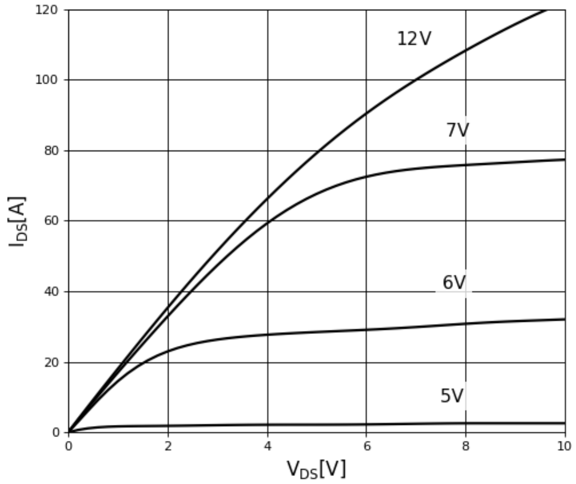


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

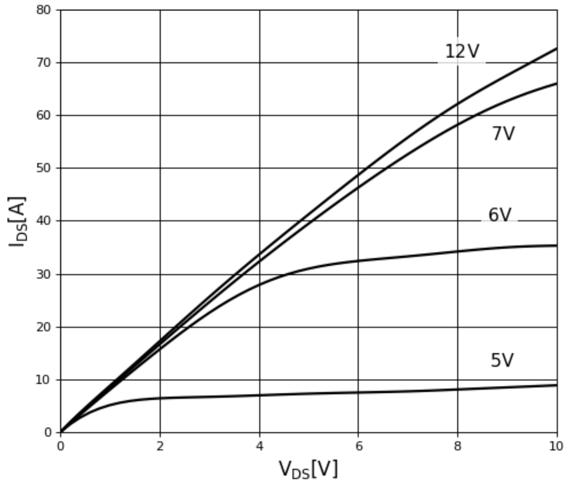


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

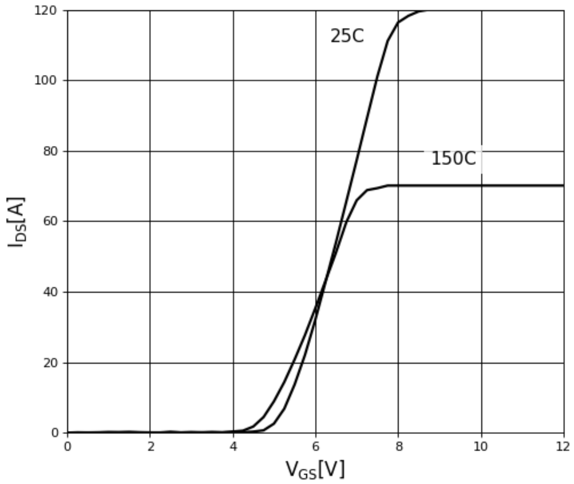


Figure 4. Typical Transfer Characteristics

V_{DS} = 10V, Parameter: T_J

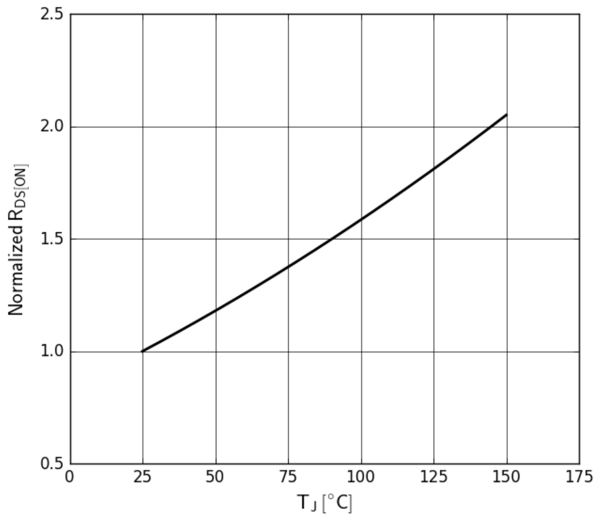


Figure 5. Normalized On-resistance

I_D = 18A, V_{GS} = 10V

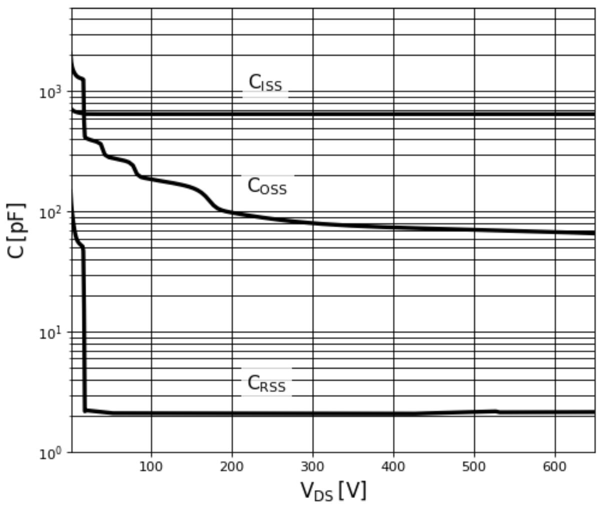


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 1MHz

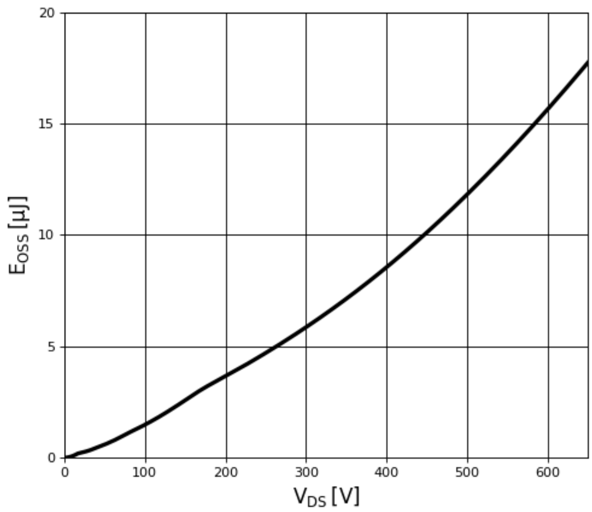


Figure 7. Typical C_{OSS} Stored Energy

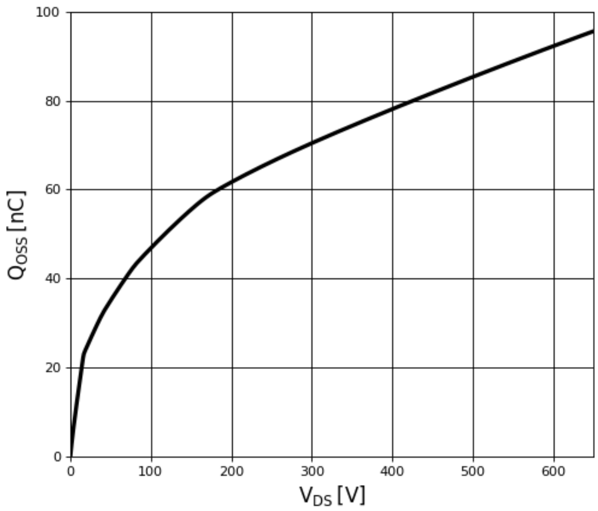


Figure 8. Typical Q_{OSS}

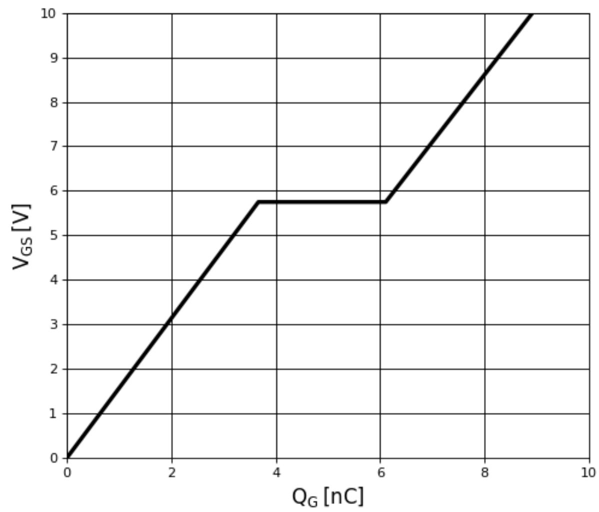


Figure 9. Typical Gate Charge

I_{DS} = 18A, V_{DS} = 400V

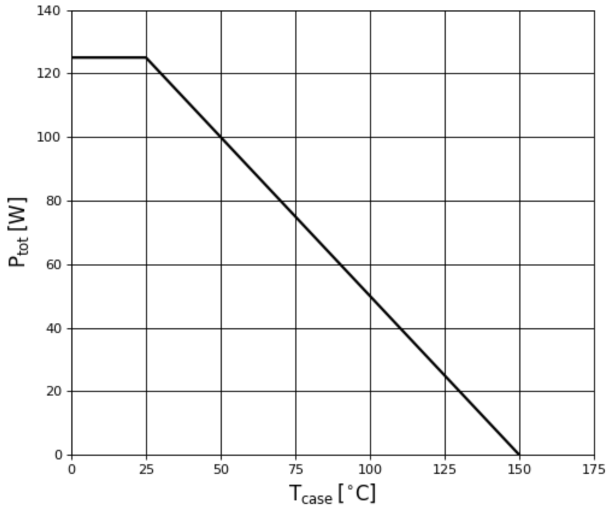


Figure 10. Power Dissipation

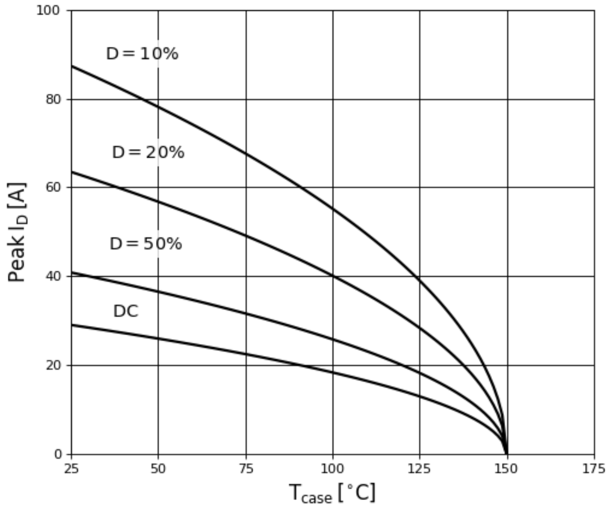


Figure 11. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 10V

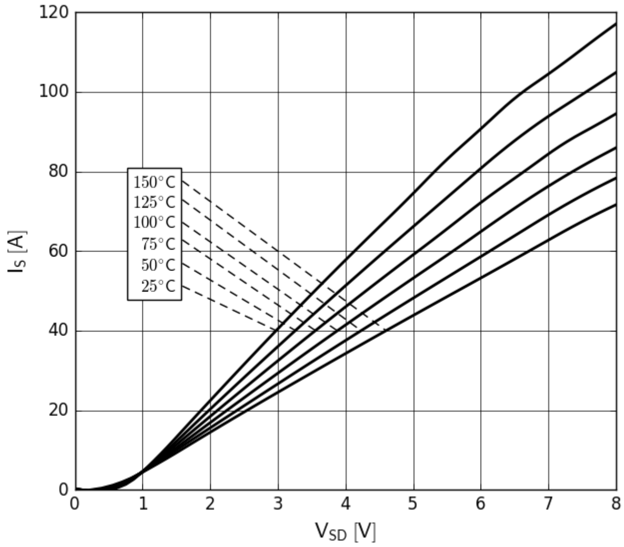


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

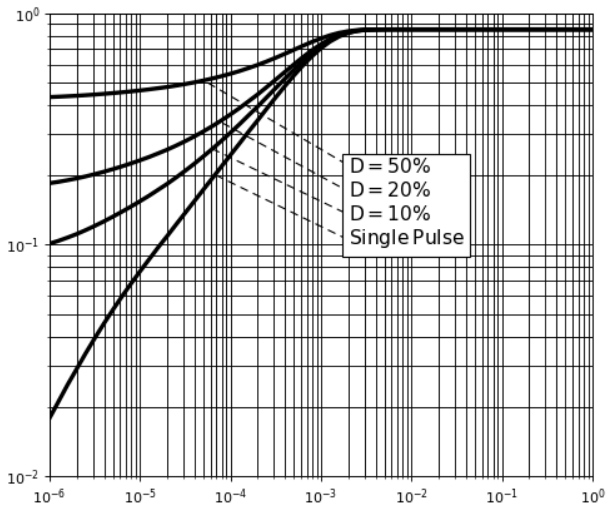


Figure 13. Transient Thermal Resistance

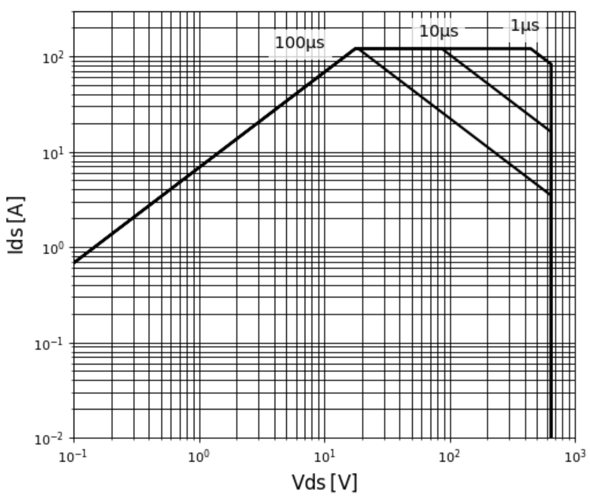


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

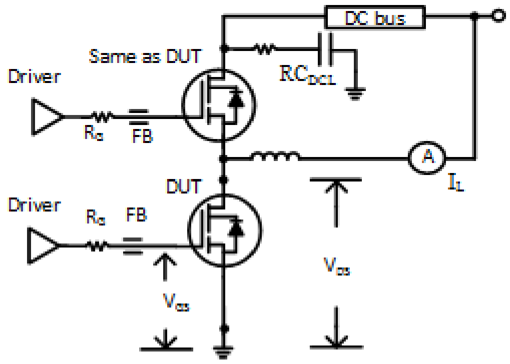


Figure 15. Switching Time Test Circuit

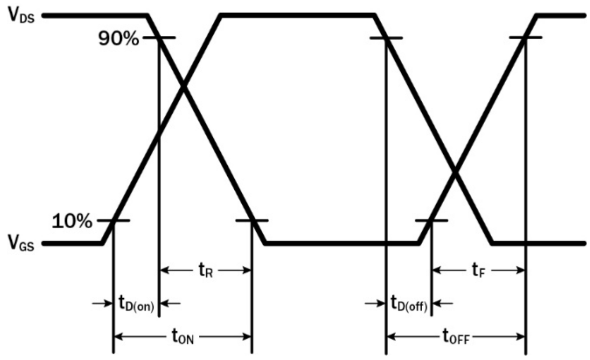


Figure 16. Switching Time Waveform

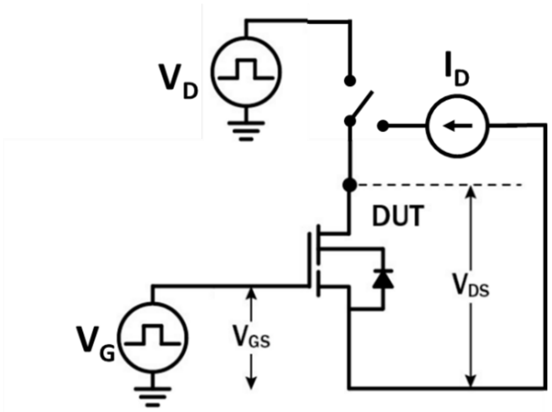


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

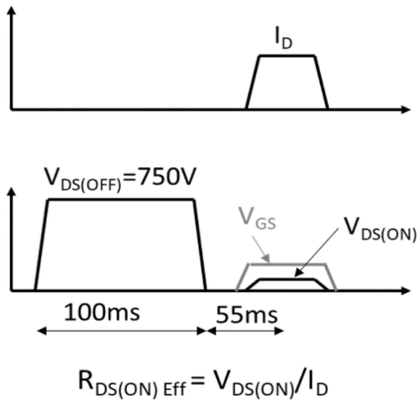
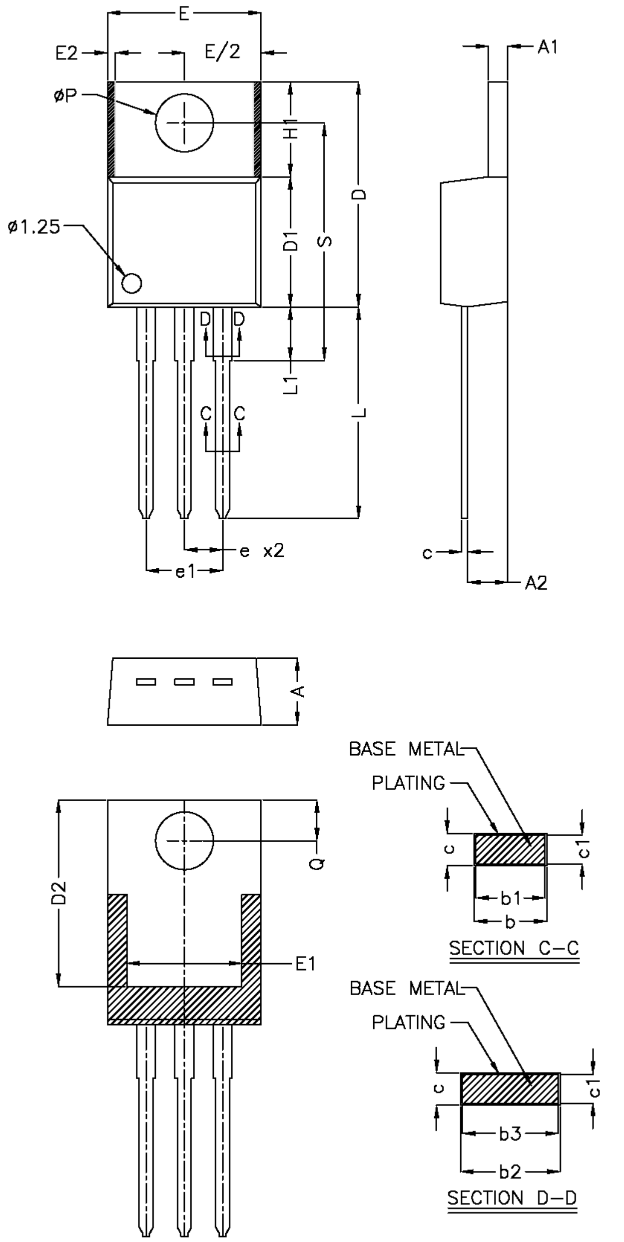


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.29	4.45	4.73	0.169	0.175	0.186
A1	1.09	1.31	1.40	0.043	0.052	0.055
A2	2.48	2.64	2.93	0.098	0.104	0.115
b	0.77	0.86	1.02	0.031	0.034	0.040
b1	0.70	–	0.86	0.027	–	0.034
b2	1.23	1.33	1.43	0.048	0.052	0.057
b3	1.20	–	1.37	0.047	–	0.054
c	0.35	0.40	0.47	0.014	0.016	0.019
c1	0.35	–	0.43	0.014	–	0.017
D	14.78	14.95	15.75	0.581	0.589	0.620
D1	8.38	–	9.01	0.330	–	0.355
D2	12.19	–	12.88	0.480	–	0.507
E	9.96	10.25	10.36	0.392	0.404	0.408
E1	6.86	–	8.89	0.271	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	6.10	6.37	6.60	0.241	0.251	0.260
L	12.70	13.84	14.27	0.500	0.545	0.562
L1	3.40	3.55	3.90	0.133	0.140	0.154
øP	3.72	3.80	3.88	0.146	0.150	0.153
Q	2.60	2.80	3.00	0.102	0.110	0.119
S	15.42	15.80	16.51	0.607	0.622	0.650

Notes:

1. Dimensions D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extreme of the plastic body.
2. Dimensions E2 and H1 define a zone where stamping and singulation irregularities are allowed.
3. Outline conforms to JEDEC TO–220AB.

TO–220AB			
transphorm			
SCALE 1:1	SHEET 1/1	DRAWING NO. 200014	VER. 3

Figure 19. TO-220 Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H070G4PS	TO-220	Source tab

8. Revision History

Revision	Date	Description
2.00	Nov 25, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Dec 4, 2023	Initial release.

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