TP65H070G4RS

650V SuperGaN® GaN FET in TOLT (source tab)

Description

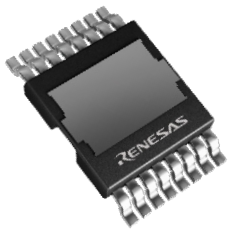
The TP65H070G4RS 650V, 72mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines a state-of-the-art high-voltage GaN HEMT with a low-voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

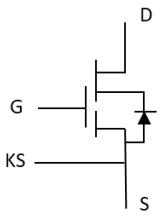
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

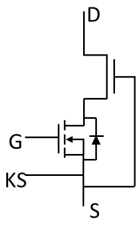
Product and Schematic Diagrams



TP65H070G4RS TOLT (top view)



Cascode Schematic Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV GaN technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Reduced crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor
- Computing

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)eff}$ (mΩ) maximum [1]	85
Q_{OSS} (nC) typical	78
Q_G (nC) typical	9

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

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1. Pin Information

1.1 Pin Assignments

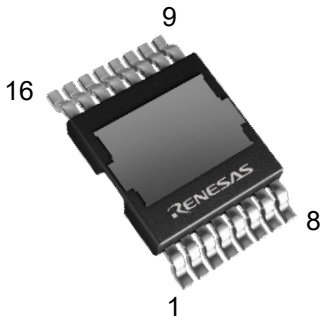


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8	D	Drain.
9	G	Gate.
10	KS	Kelvin Source.
11, 12, 13, 14, 15, 16	S	Source.
Exposed heat slug	S	Source

2. Specifications

2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	-	650	V
$V_{DSS(TR)}$	Transient drain to source voltage [1]	-	800	
V_{GSS}	Gate to source voltage	-	±20	
P_D	Maximum power dissipation at T_C = 25°C	-	96	W
I_D	Continuous drain current at T_C = 25°C	-	29	A
	Continuous drain current at T_C = 100°C	-	18.4	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	-	120	A
T_J	Operating temperature, junction	-55	+150	°C
T_S	Storage temperature	-55	+150	°C
T_{SOLD}	Soldering peak temperature [2]	-	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. For 10 seconds, 1.6mm from the case.

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	1	°C/W
$R_{\Theta JA}$	Junction-to-ambient	62	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.7mA	3.3	4	4.8	V
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 10V, I_D = 18A, T_J = 25°C	-	72	85	mΩ
		V_{GS} = 10V, I_D = 18A, T_J = 150°C	-	148	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	1.2	12	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	8	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-		100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	638	-	pF
C_{OSS}	Output capacitance		-	72	-	
C_{RSS}	Reverse transfer capacitance		-	2	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	105	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	194	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 18A	-	9	-	nC
Q_{GS}	Gate-source charge		-	3.7	-	
Q_{GD}	Gate-drain charge		-	2.4	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	78	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 18A, R_G = 50Ω (See Figure 15)	-	43.4	-	ns
t_R	Rise time		-	6.2	-	
$t_{D(off)}$	Turn-off delay		-	56	-	
t_F	Fall time		-	7.2	-	

1. Dynamic on-resistance; see Figure 17 and Figure 18 for test circuit and conditions.
2. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V.
3. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	18	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 18A	-	2.4	-	V
		V_{GS} = 0V, I_S = 9A	-	1.7	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible enabled by the LV Si FET technology.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

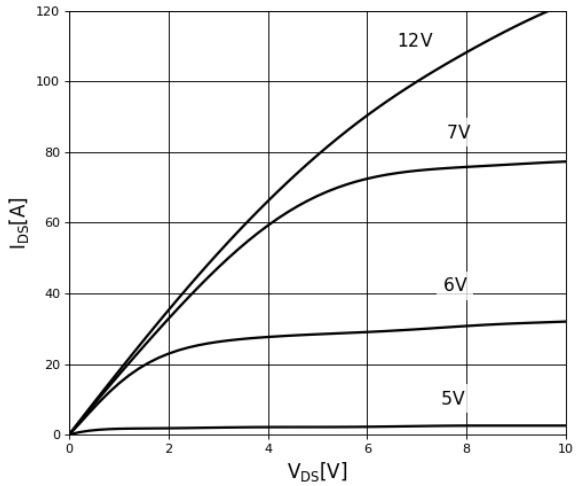


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

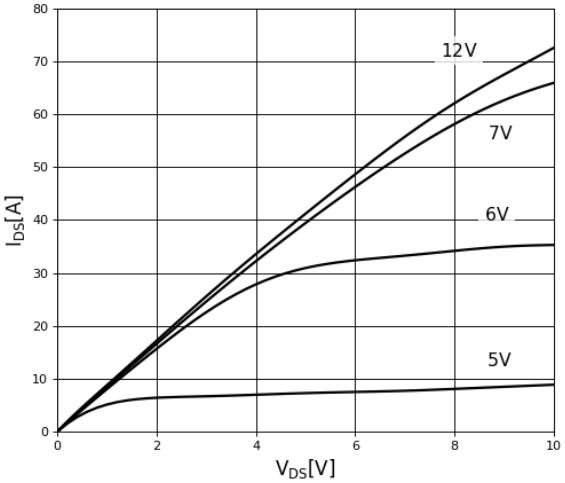


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

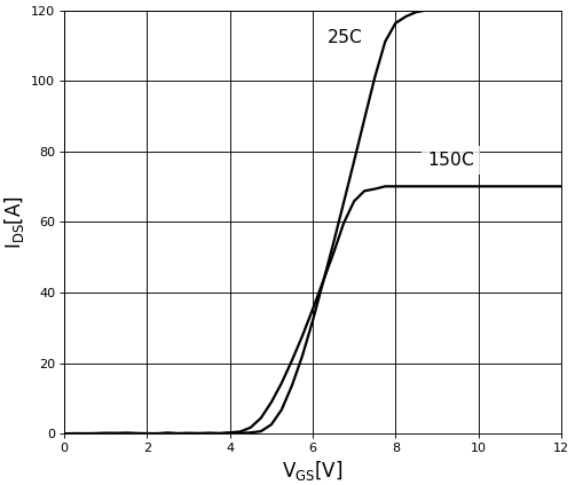


Figure 4. Typical Transfer Characteristics

V_{DS} = 10V, Parameter: T_J

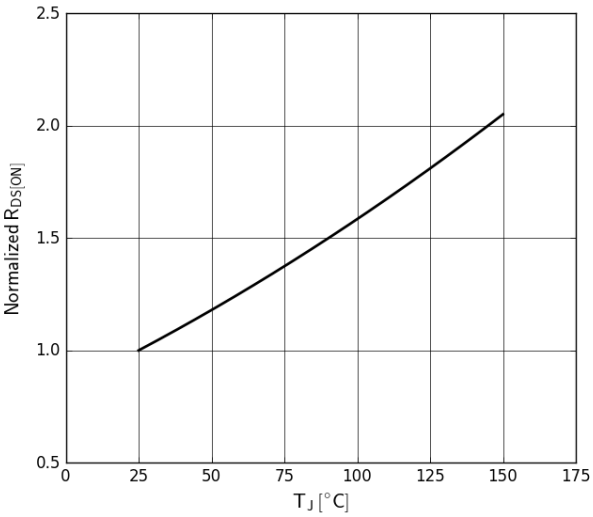


Figure 5. Normalized On-resistance

I_D = 18A, V_{GS} = 10V

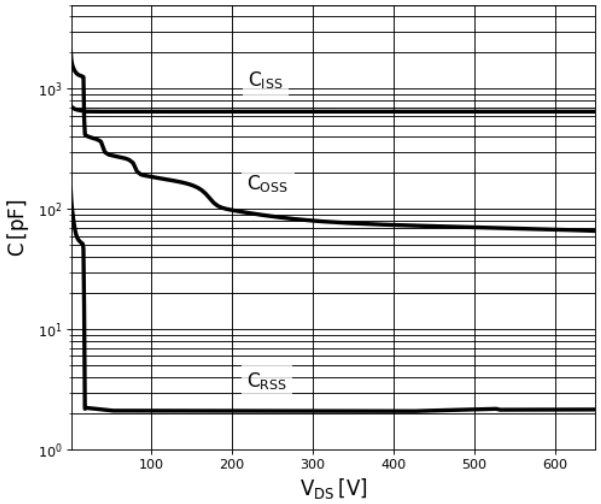


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 1MHz

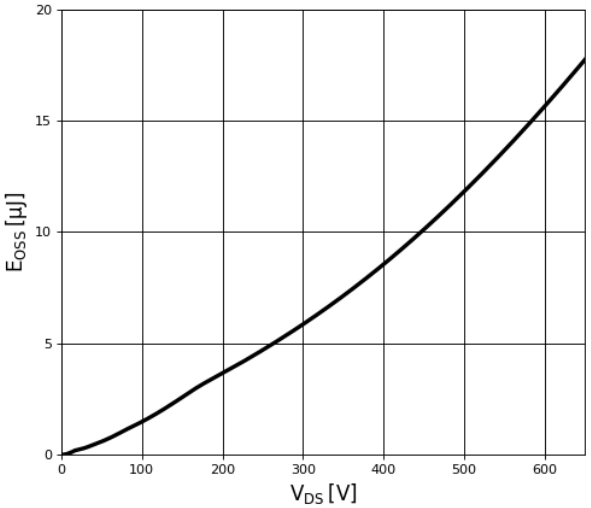


Figure 7. Typical C_{OSS} Stored Energy

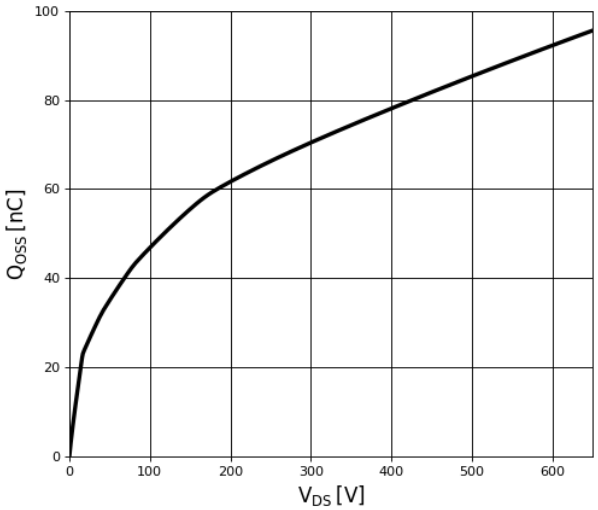


Figure 8. Typical Q_{OSS}

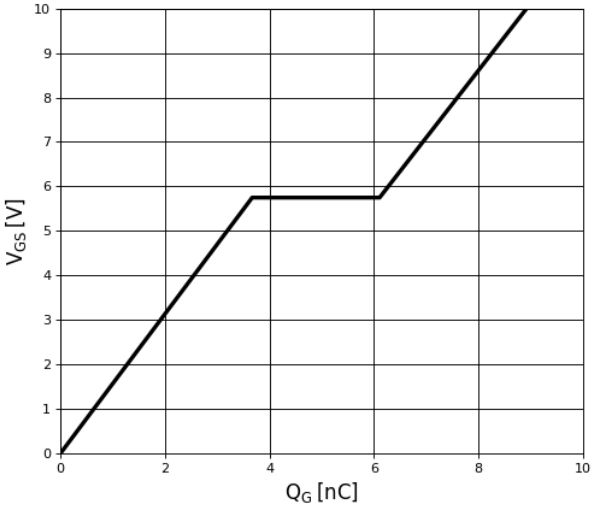


Figure 9. Typical Gate Charge

I_{DS} = 18A, V_{DS} = 400V

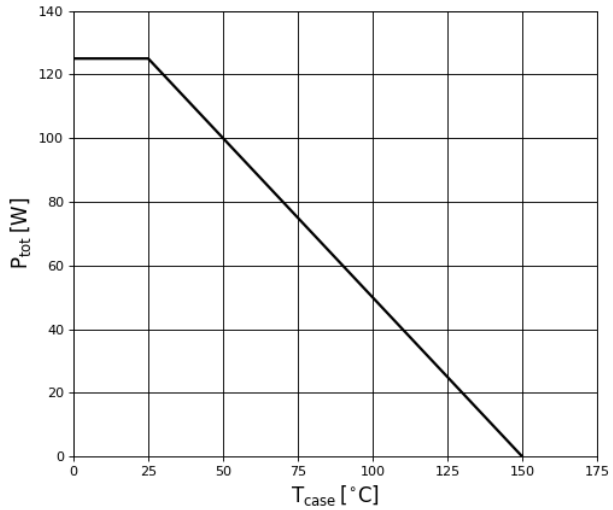


Figure 10. Power Dissipation

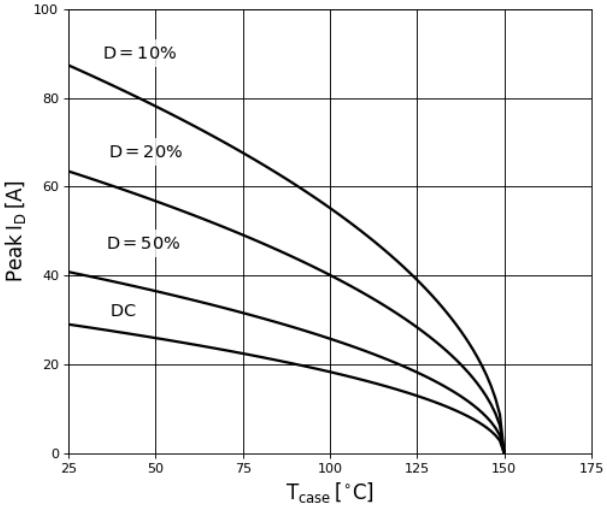


Figure 11. Current Derating

Pulse width ⩽ 10µs, V_{GS} ⩾ 10V

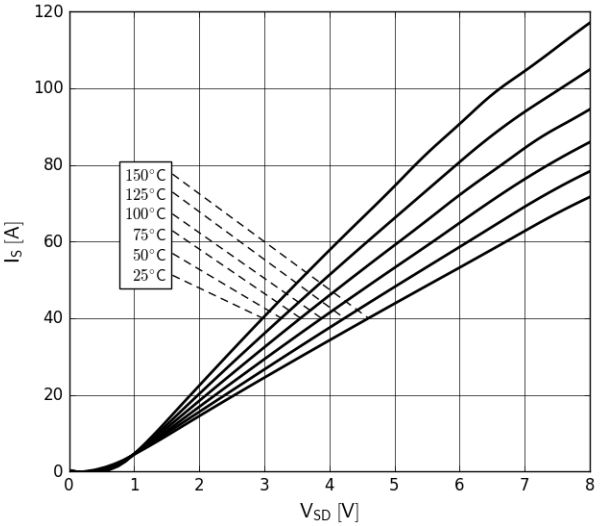


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

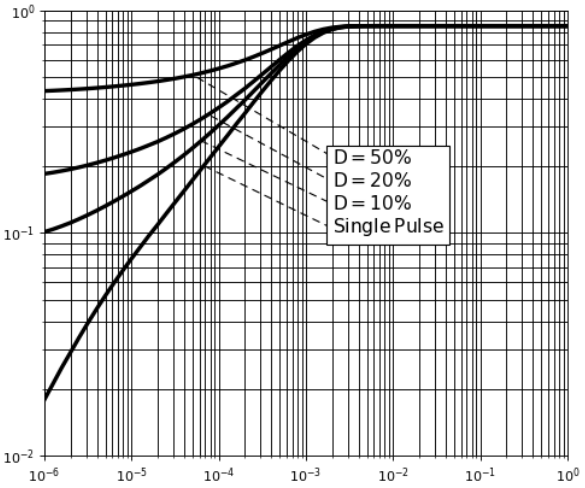


Figure 13. Transient Thermal Resistance

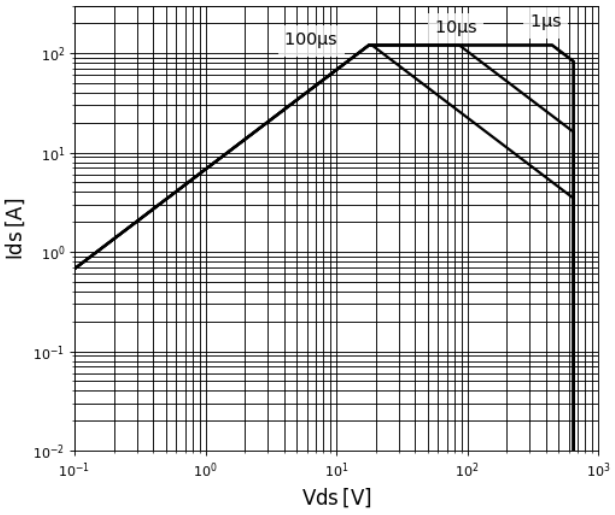


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

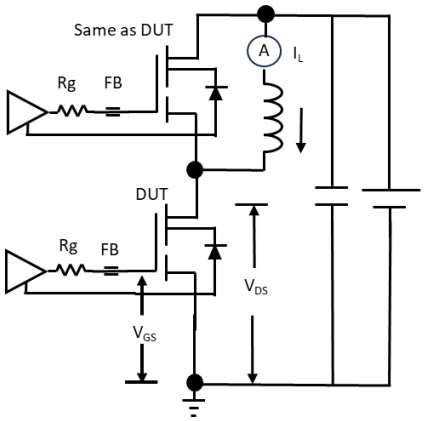


Figure 15. Switching Time Test Circuit

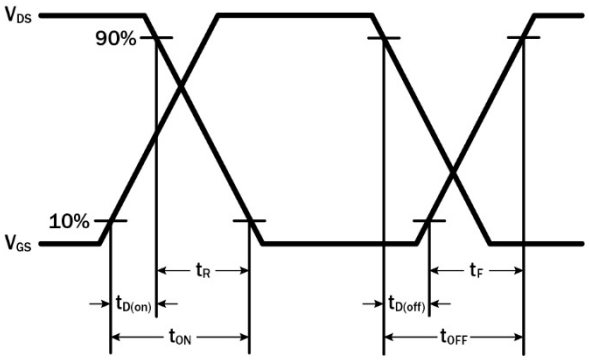


Figure 16. Switching Time Waveform

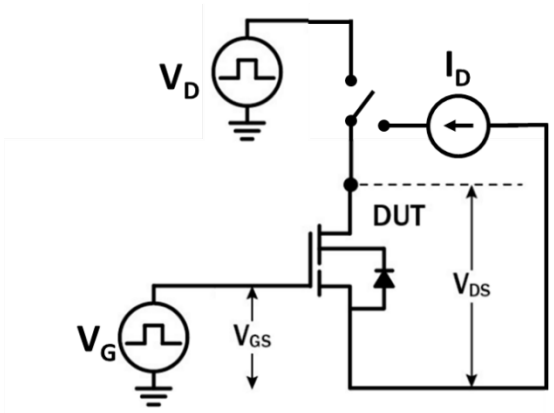


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

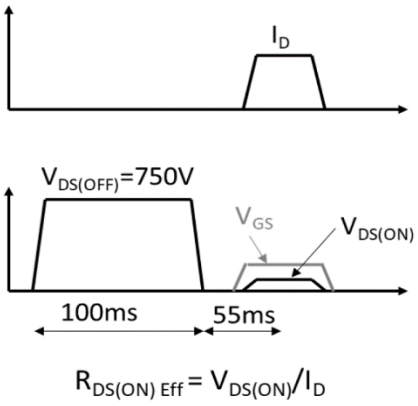
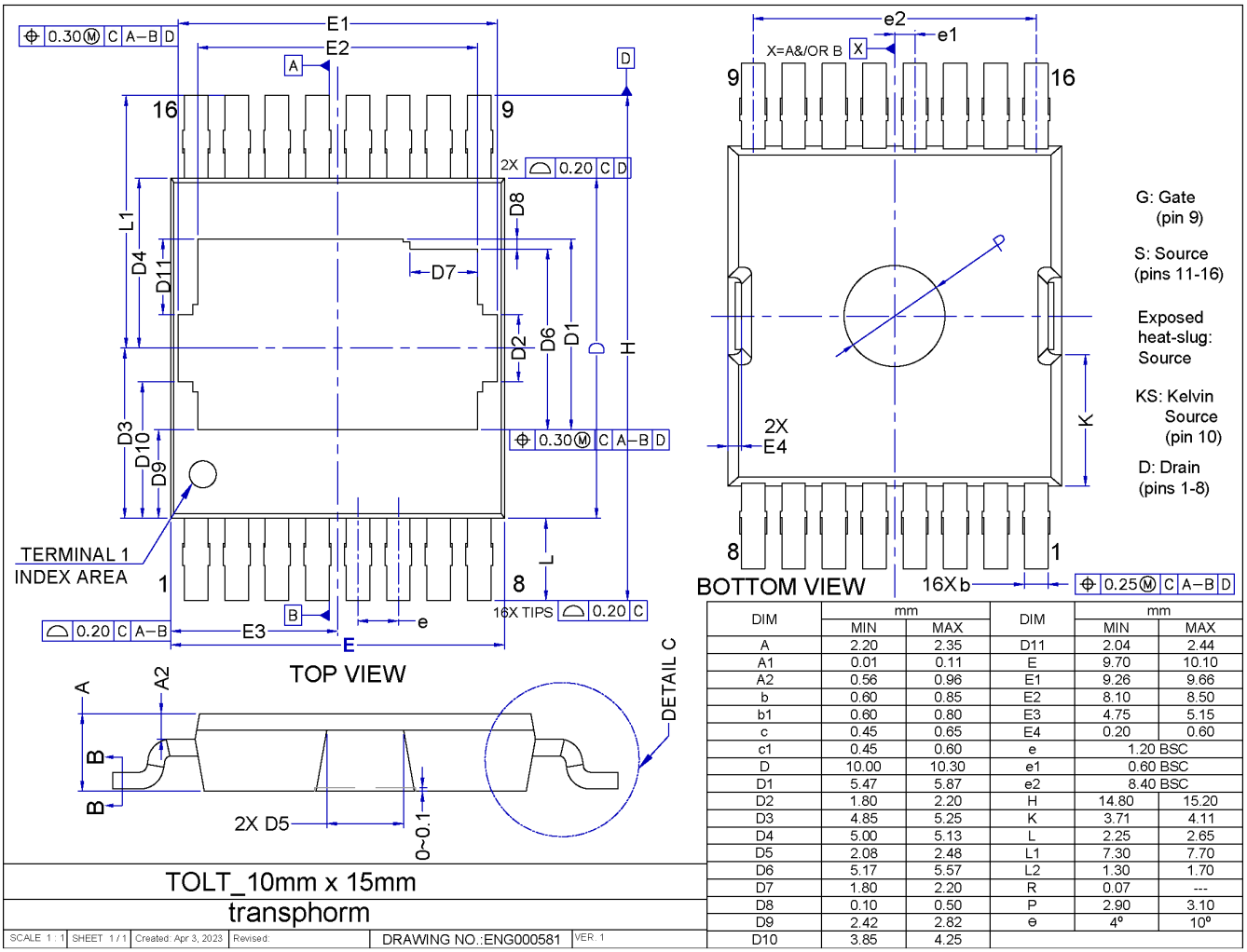


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



DIM	mm MIN	mm MAX	DIM	mm MIN	mm MAX
A	2.20	2.35	D11	2.04	2.44
A1	0.01	0.11	E	9.70	10.10
A2	0.56	0.96	E1	9.26	9.66
b	0.60	0.85	E2	8.10	8.50
b1	0.60	0.80	E3	4.75	5.15
c	0.45	0.65	E4	0.20	0.60
c1	0.45	0.60	e	1.20 BSC	
D	10.00	10.30	e1	0.60 BSC	
D1	5.47	5.87	e2	8.40 BSC	
D2	1.80	2.20	H	14.80	15.20
D3	4.85	5.25	K	3.71	4.11
D4	5.00	5.13	L	2.25	2.65
D5	2.08	2.48	L1	7.30	7.70
D6	5.17	5.57	L2	1.30	1.70
D7	1.80	2.20	R	0.07	---
D8	0.10	0.50	P	2.90	3.10
D9	2.42	2.82	θ	4°	10°
D10	3.85	4.25			

Figure 19. 10 × 15 mm TOLT Page Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description
TP65H070G4RS-TR	TOLT (source tab)

1. "-TR" designated tape and reel.

8. Revision History

Revision	Date	Description
2.00	Nov 25, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Jul 10, 2025	Initial release.

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