# TP65H100G4PS

650V SuperGaN® GaN FET in TO-220 (source tab)

## Description

The TP65H100G4PS 650V, 85mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance while enabling reduced system size and cost.

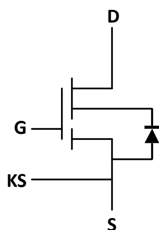
The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

## Benefits

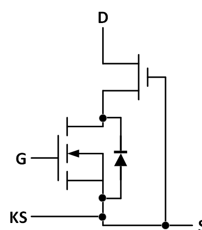
- Achieves increased efficiency in both hard-switched and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly used gate drivers
- GSD pin layout improves high speed design

## Product and Schematic Diagrams

**TP65H100G4P TO-220**




**Cascode Schematic Symbol**




**Cascode Device Structure**

(MOSFET has integrated ESD Protection Circuit)

## Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Robust design, defined by
  - Wide gate safety margin
  - Transient over-voltage capability
- Negligible reverse recovery charge (QRR)
- RoHS compliant and Halogen-free packaging

## Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

## Specifications

| | |
|---|---|
| $V_{DS}$ (V) | 650 |
| $V_{DSS(TR)}$(V) maximum | 800 |
| $R_{DS(on)}$ (mΩ) maximum [1] | 110 |
| $Q_{OSS}$ (nC) typical | 56 |
| $Q_G$ (nC) typical | 14.4 |

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)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# 1. Pin Information

## 1.1 Pin Assignments

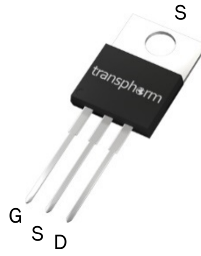



**Figure 1. Pin Assignments**

## 1.2 Pin Descriptions

| Pin Name | Description |
|---|---|
| D | Drain. |
| S | Source. |
| G | Gate. |

# 2. Specifications

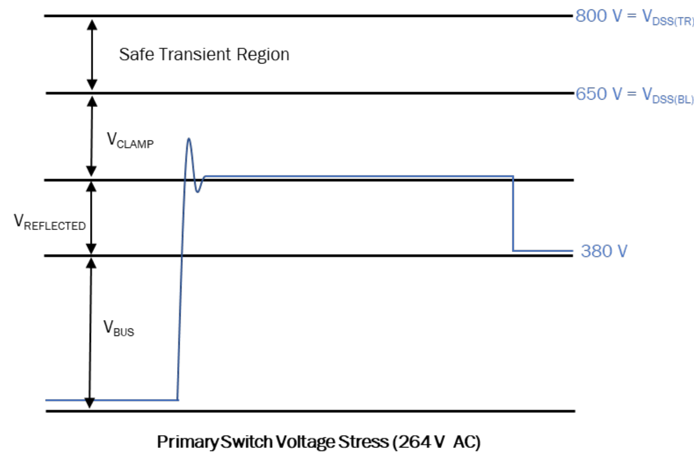
## 2.1 Absolute Maximum Ratings

$T_c$ = 25°C unless otherwise stated.

***Caution***: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Symbol | Parameter | Limit Value | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain to source voltage ($T_J$ = -55°C to 150°C) | 650 | V |
| $V_{DSS(TR)}$ | Transient drain to source voltage [1] | 800 | |
| $V_{GSS}$ | Gate to source voltage | +20 | |
| $P_D$ | Maximum power dissipation at $T_C$ = 25°C | 65.8 | W |
| $I_D$ | Continuous drain current at $T_C$ = 25°C | 18.9 | A |
| | Continuous drain current at $T_C$ = 100°C | 12 | A |
| $I_{DM}$ | Pulsed drain current (pulse width: 10µs) | 95 | A |
| $T_J$ | Junction operating temperature | -55 to +150 | °C |
| $T_S$ | Storage temperature | -55 to +150 | °C |
| $T_{SOLD}$ | Reflow soldering temperature [2] | 260 | °C |

1. In off-state, spike duration < 30µs, non-repetitive.
2. For 10 seconds,1.6mm from the case.




Primary Switch Voltage Stress (264 V AC)

## 2.2 Thermal Specifications

| Symbol | Condition | Typical Value | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Junction-to-case | 1.9 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient [1] | 50 | |

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm$^2$ copper area and 70µm thickness).

## 2.3 ESD Rating

| Symbol | Condition | Maximum | Unit |
|---|---|---|---|
| HDM | Human-body model | 750 | V |
| CDM | Charged-device model | 2000 | V |

## 2.4 Electrical Specifications – Forward Device

$T_J$ = 25°C unless otherwise stated.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{DSS(BL)}$ | Maximum drain-source voltage | $V_{GS}$ = 0V | 650 | - | - | V |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.8mA | 3.2 | 3.65 | 4.1 | V |
| $\Delta V_{GS(th)}/T_J$ | Gate threshold voltage temperature coefficient | | - | -5.8 | - | mV/°C |
| $R_{DS(on)eff}$ | Drain-source on-resistance [1] | $V_{GS}$ = 10V, $I_D$ = 12A, $T_J$ = 25°C | - | 92 | 110 | mΩ |
| | | $V_{GS}$ = 10V, $I_D$ = 12A, $T_J$ = 150°C | - | 184 | - | |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{DS}$ = 650V, $V_{GS}$ = 0V, $T_J$ = 25°C | - | 2.5 | 25 | µA |
| | | $V_{DS}$ = 650V, $V_{GS}$ = 0V, $T_J$ = 150°C | - | 5 | - | |
| $I_{GSS}$ | Gate-to-source forward leakage current | $V_{GS}$ = 20V | - | - | 100 | nA |
| | Gate-to-source reverse leakage current | $V_{GS}$ = -20V | - | - | -100 | |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 400V, *f* = 500kHz | - | 818 | - | pF |
| $C_{OSS}$ | Output capacitance | | - | 53 | - | |
| $C_{RSS}$ | Reverse transfer capacitance | | - | 3.6 | - | |
| $C_{O(er)}$ | Output capacitance, energy related [2] | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 400V | - | 78 | - | pF |
| $C_{O(tr)}$ | Output capacitance, time related [3] | | - | 139 | - | |
| $Q_G$ | Total gate charge | $V_{DS}$ = 400V, $V_{GS}$ = 0V to 10V, $I_D$ = 12A | - | 14.4 | - | nC |
| $Q_{GS}$ | Gate-source charge | | - | 4.7 | - | |
| $Q_{GD}$ | Gate-drain charge | | - | 5.2 | - | |
| $Q_{OSS}$ | Output charge | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 400V | - | 56 | - | nC |
| $t_{D(on)}$ | Turn-on delay | $V_{DS}$ = 400V, $V_{GS}$ = 0V to 12V, $I_D$ = 13A, $R_{G_on}$ = 36Ω, $Z_{FB}$ = 120Ω at 100MHz (see Figure 15) | - | 23 | - | ns |
| $t_R$ | Rise time | | - | 7.1 | - | |
| $t_{D(off)}$ | Turn-off delay | | - | 58 | - | |
| $t_F$ | Fall time | | - | 7.5 | - | |

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

## 2.5 Electrical Specifications – Reverse Device

$T_J$ = 25°C unless otherwise stated.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_S$ | Reverse current | $V_{GS}$ = 0V, $T_C$ = 100°C, ≤ 20% duty cycle | - | - | 12 | A |
| $V_{SD}$ | Reverse voltage [1] | $V_{GS}$ = 0V, $I_S$ = 12A | - | 1.7 | - | V |
| | | $V_{GS}$ = 0V, $I_S$ = 8A | - | 1.4 | - | |

1. Includes dynamic $R_{DS(on)}$ effect.

*Note*: Reverse recovery charge is negligible, enabled by the LV Si FET technology

# 3. Typical Performance Graphs

$T_C$ = 25°C unless otherwise stated.

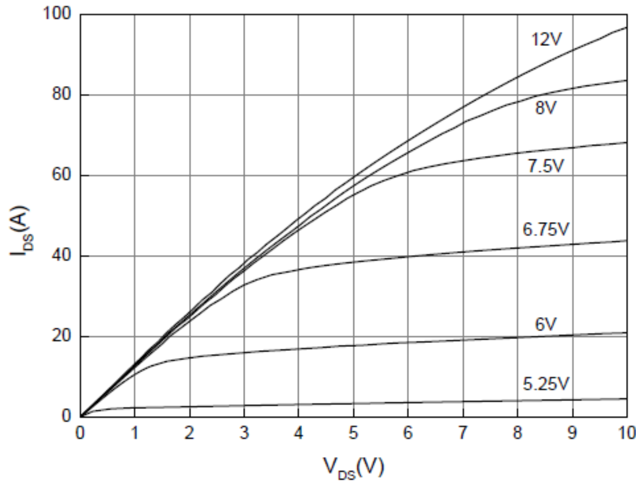



**Figure 2. Typical Output Characteristics, $T_J$ = 25°C**

Parameter: $V_{GS}$

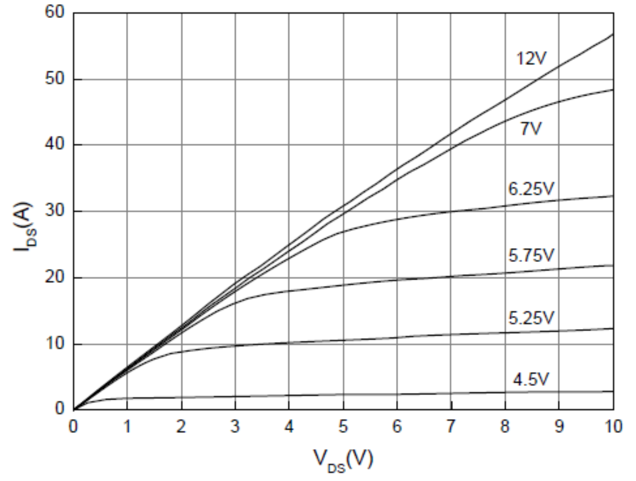



**Figure 3. Typical Output Characteristics, $T_J$ = 150°C**

Parameter: $V_{GS}$

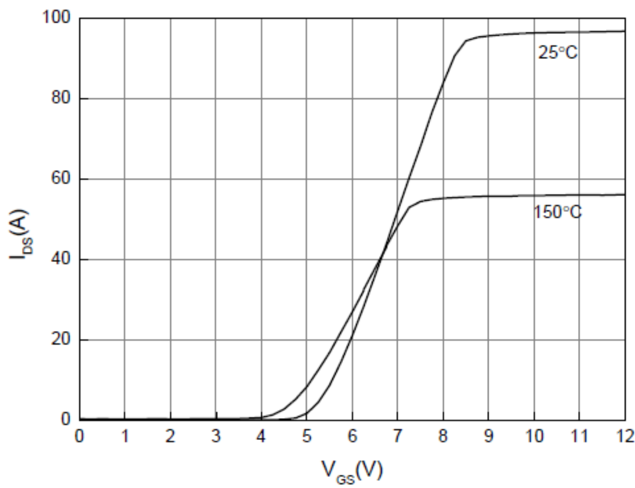



**Figure 4. Typical Transfer Characteristics**

$V_{DS}$ = 20V, Parameter: $T_J$

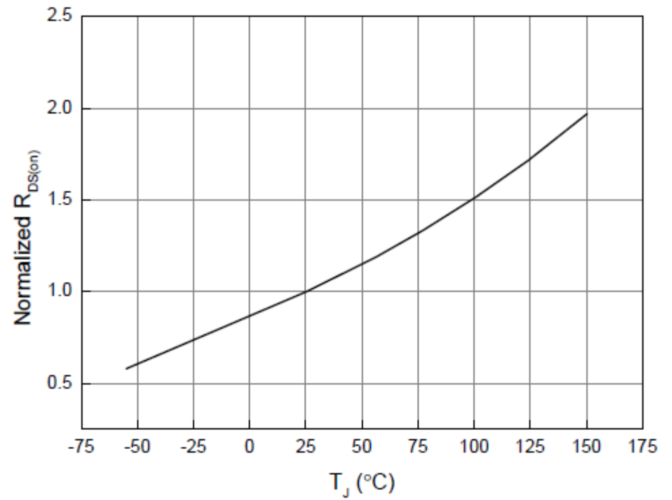



**Figure 5. Normalized On-resistance**

$I_D$ = 12A, $V_{GS}$ = 10V

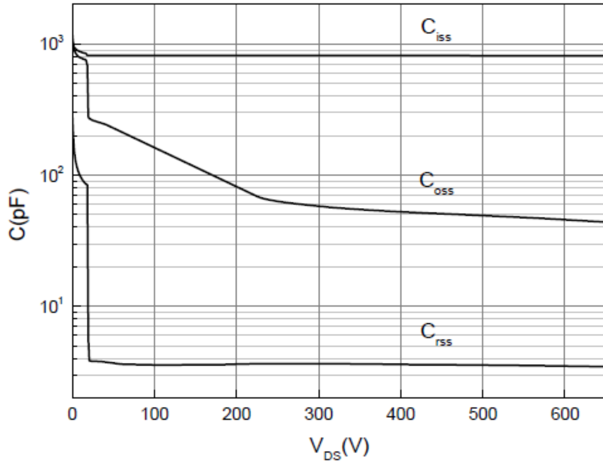



**Figure 6. Typical Capacitance**

$V_{GS}$ = 0V, f = 1MHz

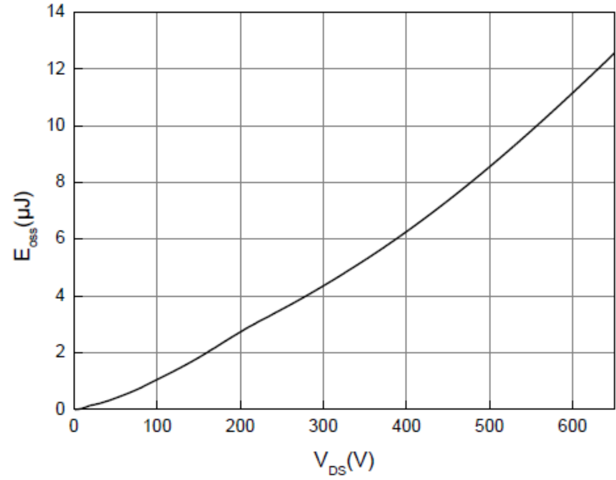



**Figure 7. Typical $C_{OSS}$ Stored Energy**

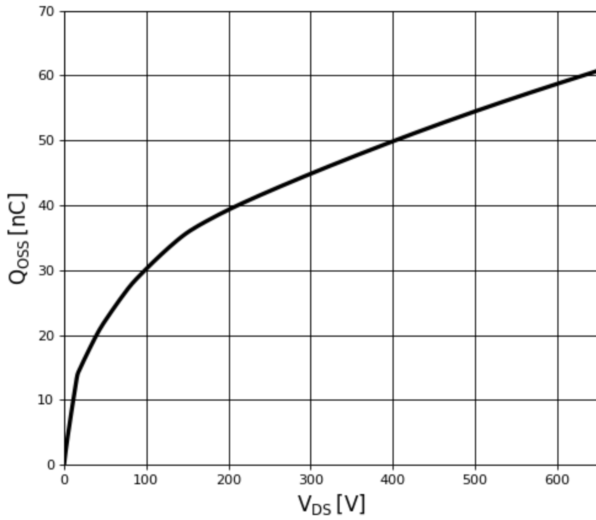



**Figure 8. Typical $Q_{OSS}$**

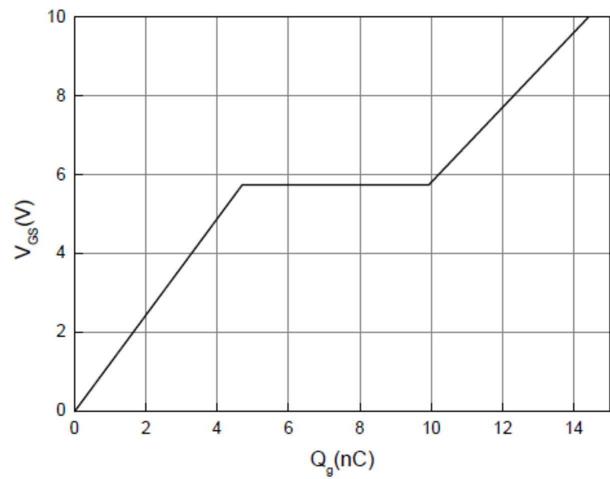



**Figure 9. Typical Gate Charge**

$I_{DS}$ = 12A, $V_{DS}$ = 400V

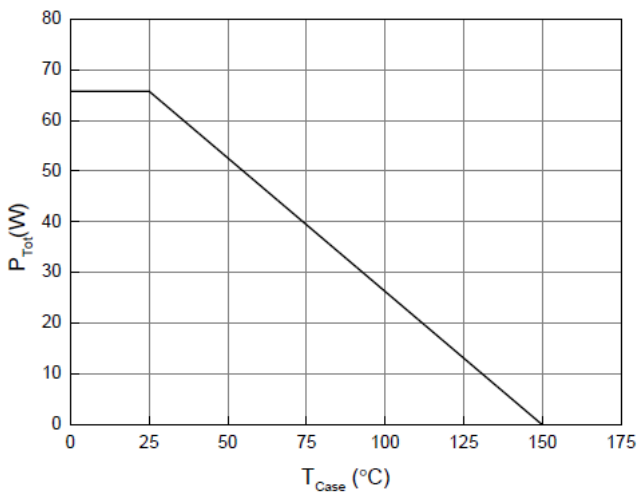



**Figure 10. Power Dissipation**

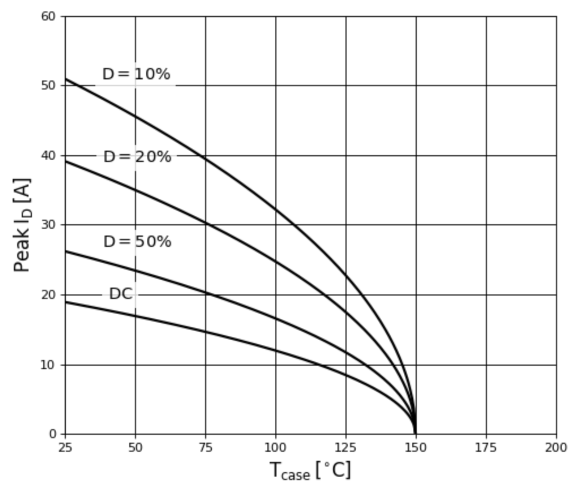



**Figure 11. Current Derating**

Pulse width ≤ 10μs, $V_{GS}$ ≥ 10V

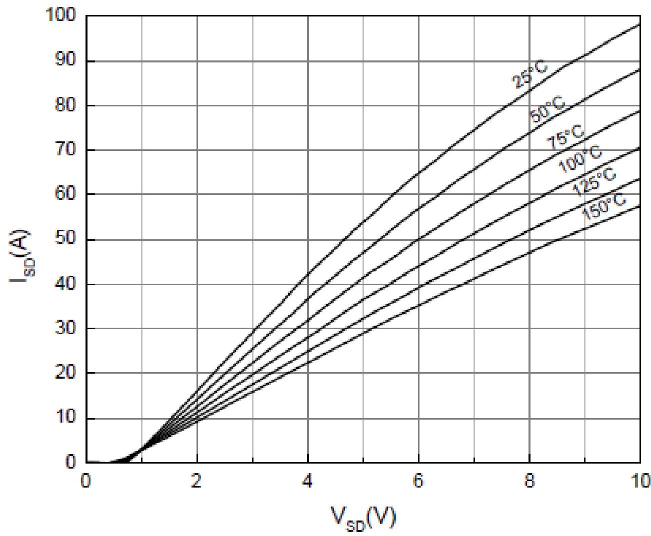



**Figure 12. Forward Characteristics of Rev. Diode**

$I_S = f(V_{SD})$, Parameter: $T_J$

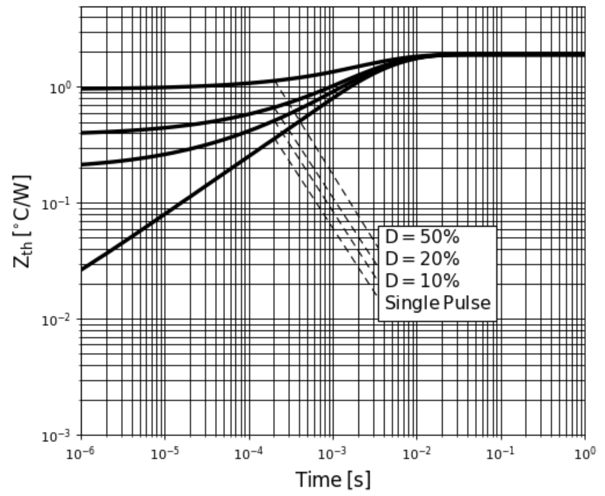



**Figure 13. Transient Thermal Resistance**

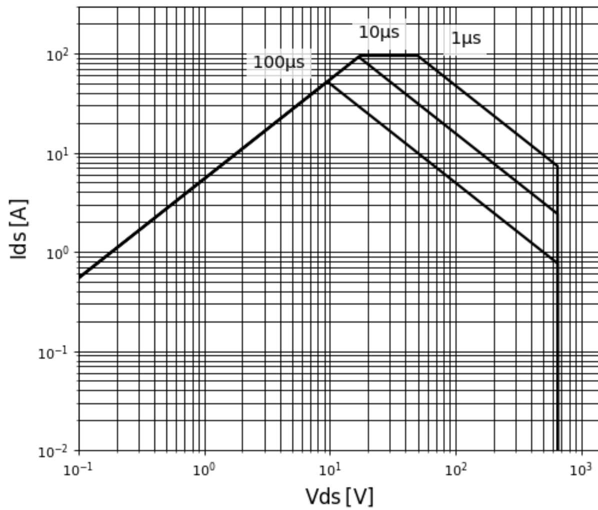



**Figure 14. Safe Operating Area $T_C$ = 25°C**

# 4. Test Circuits and Waveforms

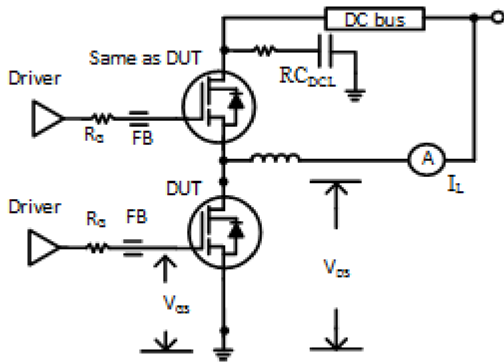



Figure 15. Switching Time Test Circuit

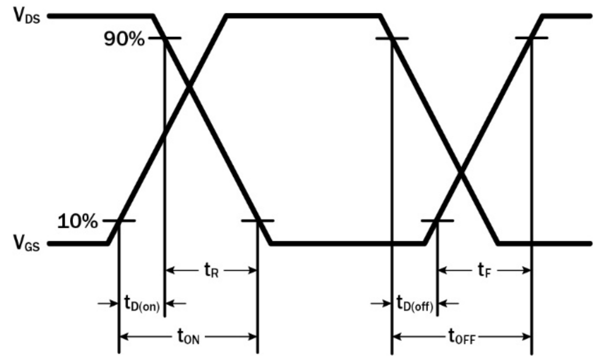



Figure 16. Switching Time Waveform

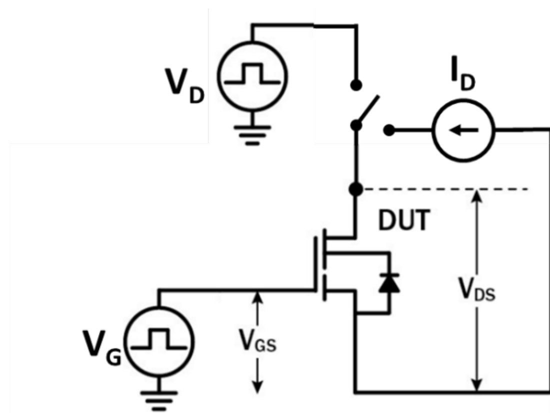



Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

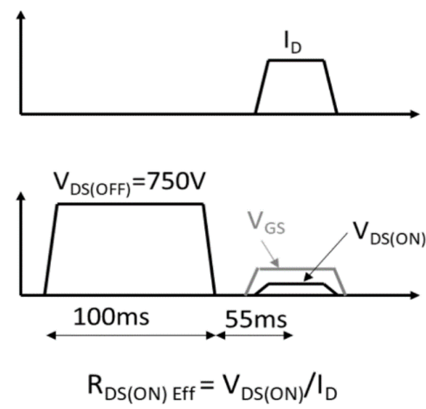
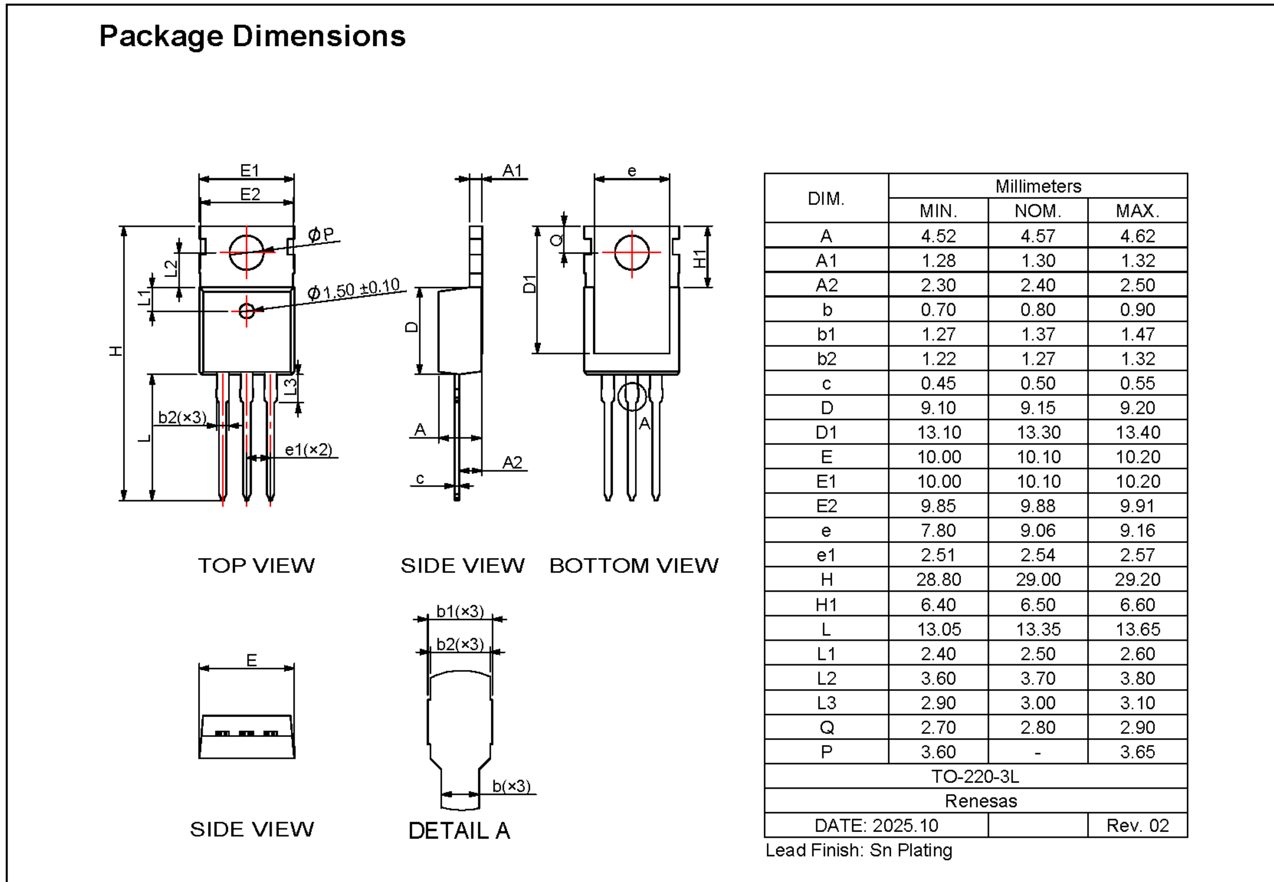



Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

# 5. Package Outline Drawings




| DIM. | Millimeters | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 4.52 | 4.57 | 4.62 |
| A1 | 1.28 | 1.30 | 1.32 |
| A2 | 2.30 | 2.40 | 2.50 |
| b | 0.70 | 0.80 | 0.90 |
| b1 | 1.27 | 1.37 | 1.47 |
| b2 | 1.22 | 1.27 | 1.32 |
| c | 0.45 | 0.50 | 0.55 |
| D | 9.10 | 9.15 | 9.20 |
| D1 | 13.10 | 13.30 | 13.40 |
| E | 10.00 | 10.10 | 10.20 |
| E1 | 10.00 | 10.10 | 10.20 |
| E2 | 9.85 | 9.88 | 9.91 |
| e | 7.80 | 9.06 | 9.16 |
| e1 | 2.51 | 2.54 | 2.57 |
| H | 28.80 | 29.00 | 29.20 |
| H1 | 6.40 | 6.50 | 6.60 |
| L | 13.05 | 13.35 | 13.65 |
| L1 | 2.40 | 2.50 | 2.60 |
| L2 | 3.60 | 3.70 | 3.80 |
| L3 | 2.90 | 3.00 | 3.10 |
| Q | 2.70 | 2.80 | 2.90 |
| P | 3.60 | - | 3.65 |
| TO-220-3L | | | |
| Renesas | | | |
| DATE: 2025.10 | | | Rev. 02 |

**Figure 19. TO-220 Package Outline Drawing**

# 6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

# 7. Ordering Information

| Part Number | Package Description | Package Configuration |
|---|---|---|
| TP65H100G4PS | TO220 | Source |

# 8. Revision History

| Revision | Date | Description |
|---|---|---|
| 2.00 | Nov 25, 2025 | Updated the document's formatting; no technical changes were completed. |
| 1.03 | Oct 27, 2025 | Updated POD. |
| 1.02 | Aug 22, 2024 | Fixed typo on page 1 above the device image. |
| 1.01 | Mar 19, 2024 | Added ESD rating. |
| 1.00 | Mar 18, 2024 | Initial release. |

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