TP65H150G4PS

650V SuperGaN® GaN FET in TO-220 (source tab)

Description

The TP65H150G4PS 650V, 150mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

Related Literature

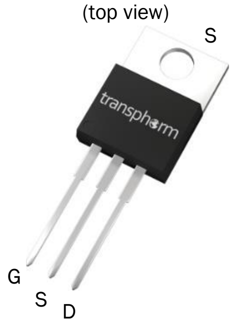
- Printed Circuit Board Layout and Probing
- Recommendations for Vapor Phase Reflow
- Recommended External Circuitry for GaN FETs
- Low cost driver solution

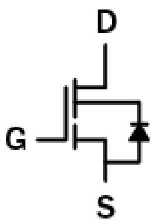
Product Series and Ordering Information

Part Number	Package	Package Configuration
TP65H150G4PS	3 lead TO-220	Source

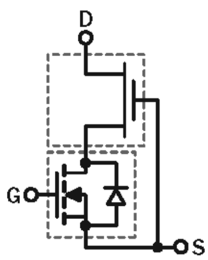
TP65H150G4PS
TO-220

(top view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - — Wide gate safety margin
  - — Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - — Increased power density
  - — Reduced system size and weight
  - — Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Key Specifications	
V_{DS} (V) min	650
$V_{DSS(TR)}$ (V) max	800
$R_{DS(on)}$ (mΩ) max*	180
Q_{oss} (nC) typ	34
Q_G (nC) typ	8

* Dynamic $R_{DS(on)}$; see Figures 18 and 19

Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

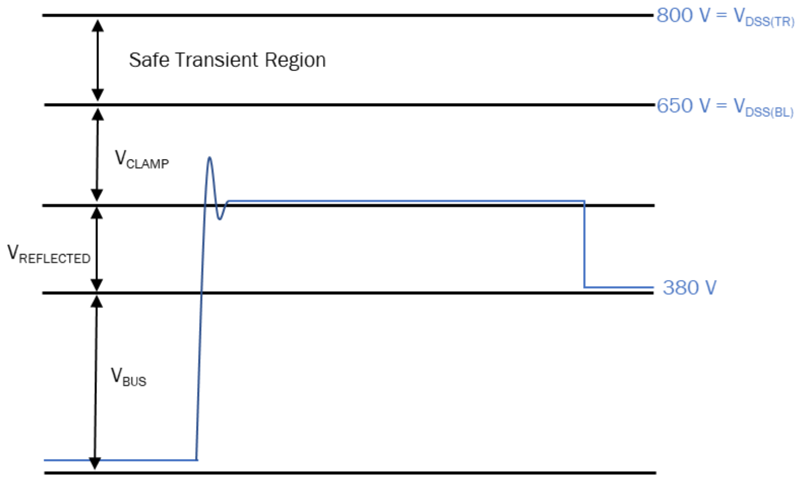
Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{DSS(TR)}$	Transient drain to source voltage [(a)]		800	
V_{GSS}	Gate to source voltage		±20	
P_D	Maximum power dissipation @T_C=25°C		83	W
I_D	Continuous drain current @T_C=25°C [(b)]		16	A
	Continuous drain current @T_C=100°C [(b)]		10	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		60	A
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature [(c)]		260	°C

Notes:

a. In off-state, spike duration < 30µs, non-repetitive.

b. For increased stability at high current operation, see Circuit Implementation on page 3

c. For 10 seconds, 1.6mm from the case



Primary Switch Voltage Stress (264 V AC)

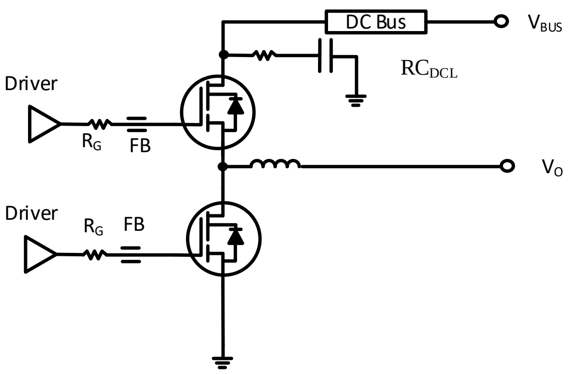
Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.5	°C/W
$R_{\Theta JA}$	Junction-to-ambient [d]	50	°C/W

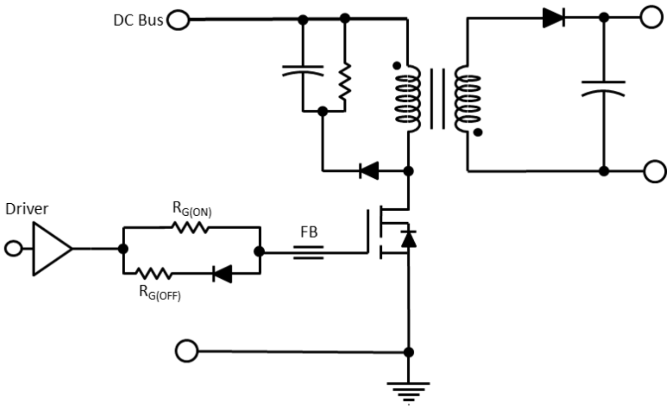
Notes:

d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70µm thickness)

Circuit Implementation



Simplified Half-bridge Schematic



Simplified Single Ended Schematic

Recommended gate drive: (0V, 10V) with $R_{G(tot)} = 70\ \Omega^{(d)}$

Recommended gate drive: (0V, 12V) with $R_{G(ON)} = 100$ to $300\ \Omega$

$R_{G(OFF)} = 0$ to $15\ \Omega$

Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) [e]
240Ω @ 100MHz	4.7nF + 2.5Ω

Notes:

d. For bridge topologies only. R_G could be much smaller in single ended topologies.

e. RC_{DCL} should be placed as close as possible to the drain pin.

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS(BL)}$	Maximum drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	3.3	4	4.8	V	V_{DS}=V_{GS}, I_D=0.5mA
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	—	-5.8	—	mV/°C	
$R_{DS(on)eff}$	Drain-source on-resistance [f]	—	150	180	mΩ	V_{GS}=10V, I_D=8.5A, T_J=25°C
		—	307	—		V_{GS}=10V, I_D=8.5A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	2.5	25	μA	V_{DS}=650V, V_{GS}=0V, T_J=25°C
		—	10	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-20V
C_{ISS}	Input capacitance	—	598	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	30	—		
C_{RSS}	Reverse transfer capacitance	—	1	—		
$C_{O(er)}$	Output capacitance, energy related [g]	—	43	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [h]	—	85	—		
Q_G	Total gate charge	—	8	—	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=8.5A
Q_{GS}	Gate-source charge	—	3.3	—		
Q_{GD}	Gate-drain charge	—	2	—		
Q_{OSS}	Output charge	—	34	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	37.8	—	ns	V_{DS}=400V, V_{GS}=0V to 12V, I_D=8.5A, R_G=70Ω, Z_{FB}=240Ω at 100MHz (See Figure 14)
t_R	Rise time	—	5.2	—		
$t_{D(off)}$	Turn-off delay	—	48	—		
t_F	Fall time	—	8	—		

Notes:

f. Dynamic $R_{DS(on)}$ value; see Figures 18 and 19 for conditions

g. Equivalent capacitance to give same stored energy from 0V to 400V

h. Equivalent capacitance to give same charging time from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	8.3	A	V_{GS}=0V, T_C=100°C, ≤20% duty cycle
V_{SD}	Reverse voltage (i)	—	2.4	—	V	V_{GS}=0V, I_S=10A
		—	1.6	—		V_{GS}=0V, I_S=5A
t_{RR}	Reverse recovery time	—	31	—	ns	I_S=10A, V_{DD}=400V, di/dt=1000A/ms
Q_{RR}	Reverse recovery charge(j)	—	0	—	nC	

Notes:

i. Includes dynamic $R_{DS(on)}$ effect

j. Excludes Q_{oss}

Typical Characteristics (T_c=25°C unless otherwise stated)

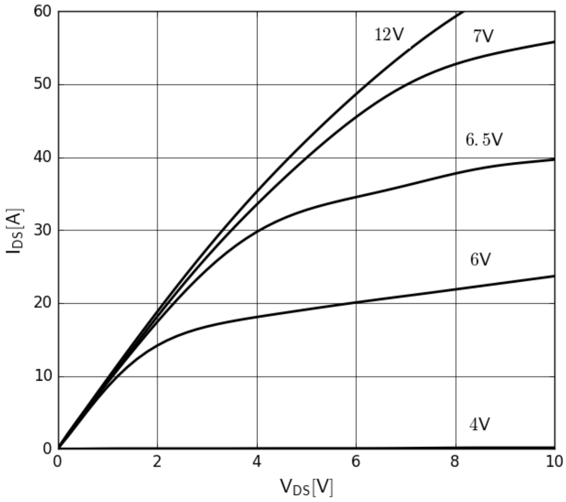


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

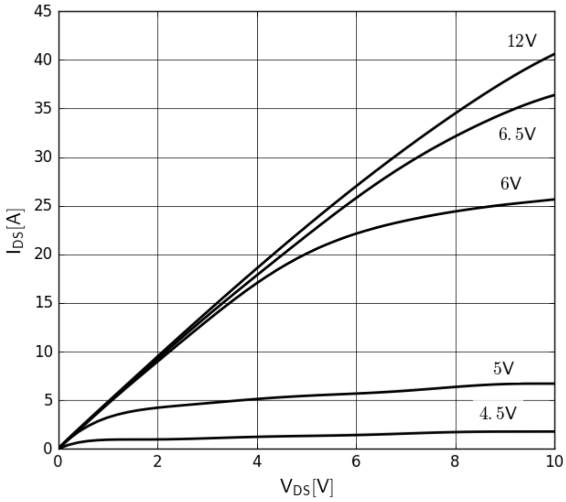


Figure 2. Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

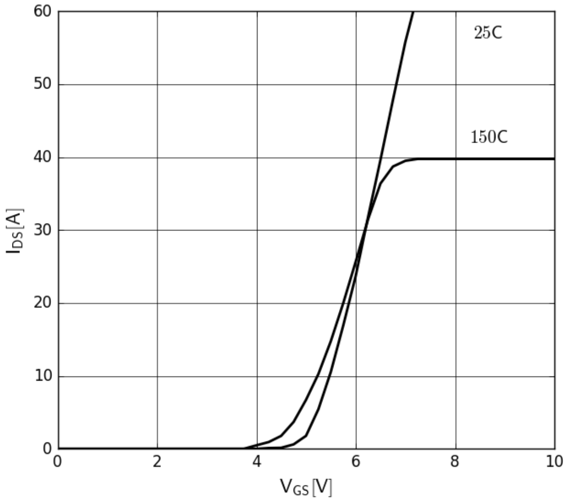


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

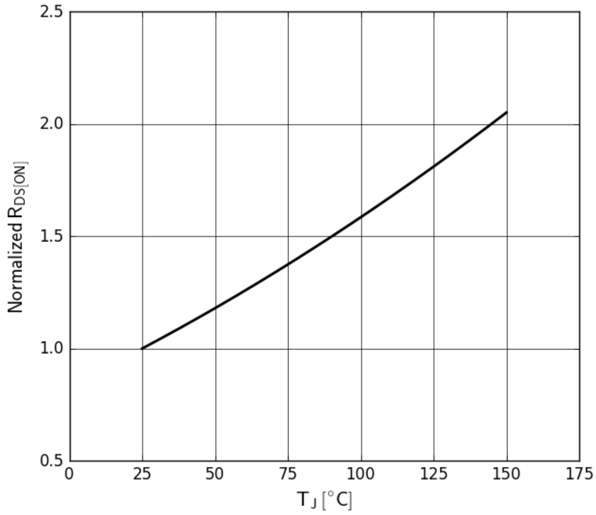


Figure 4. Normalized On-resistance
I_D=8.5A, V_{GS}=10V

Typical Characteristics (T_c=25°C unless otherwise stated)

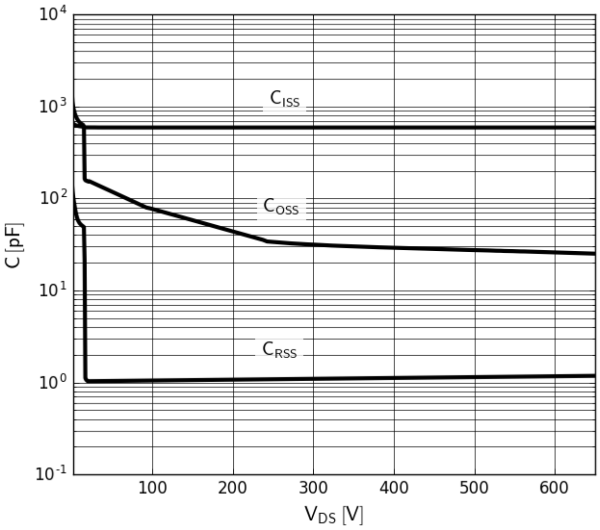


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHz

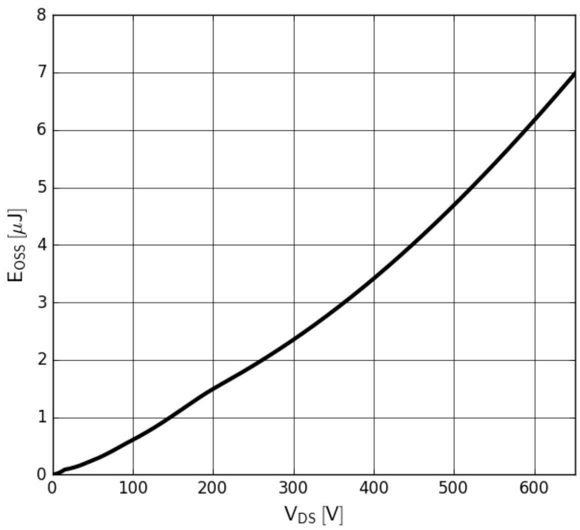


Figure 6. Typical C_{OSS} Stored Energy

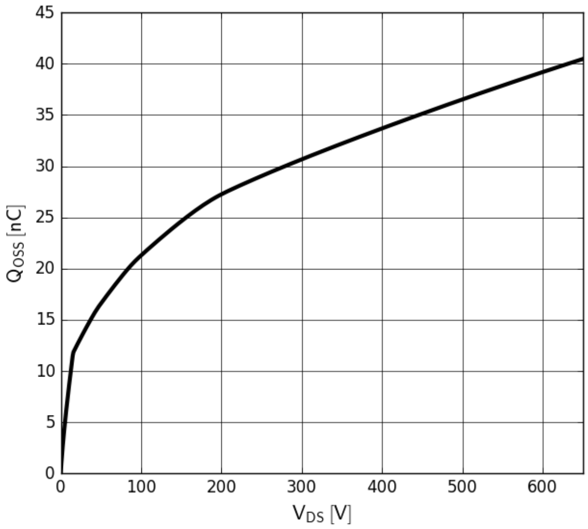


Figure 7. Typical Q_{OSS}

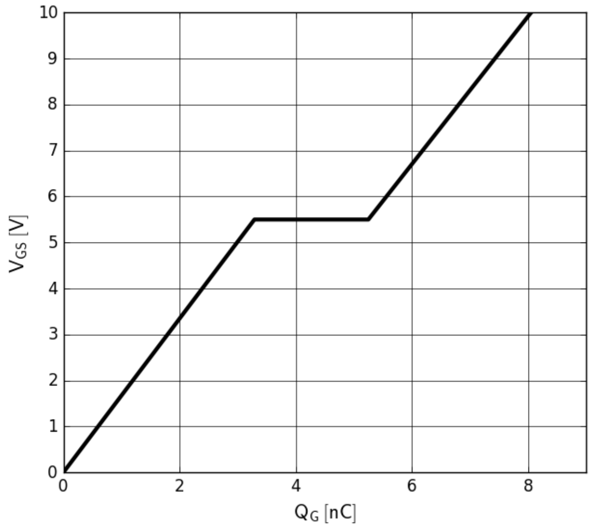


Figure 8. Typical Gate Charge

I_{DS}=8.5A, V_{DS}=400V

Typical Characteristics (T_c=25 °C unless otherwise stated)

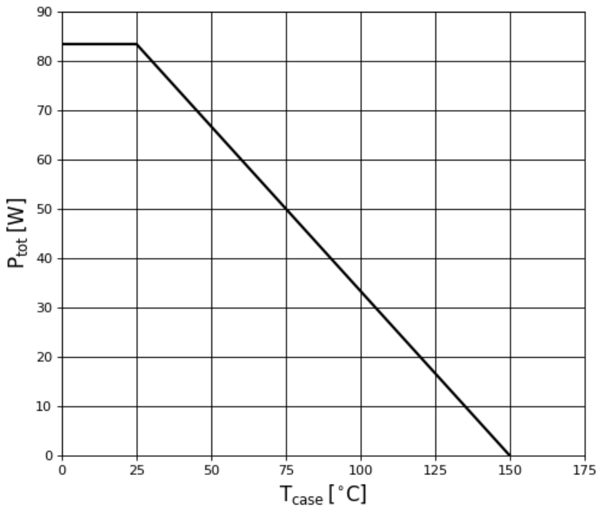


Figure 9. Power Dissipation

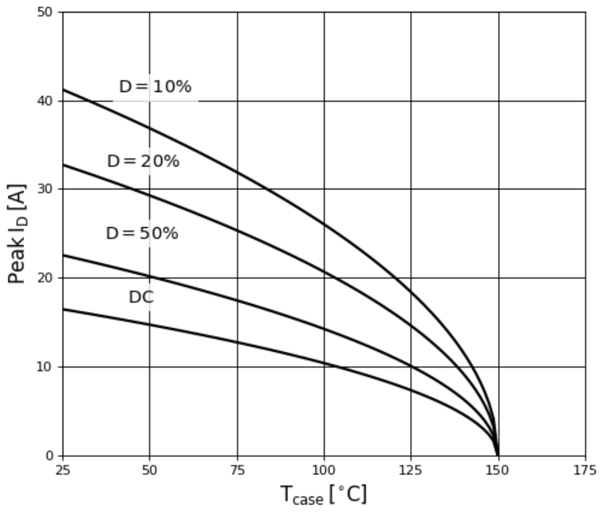


Figure 10. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 10V

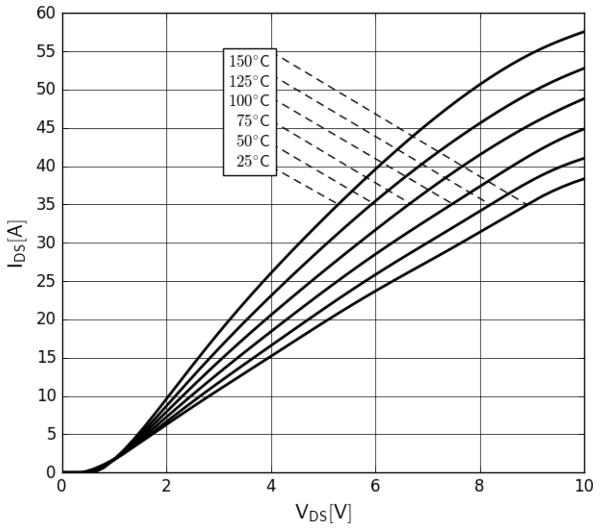


Figure 11. Forward Characteristics of Rev. Diode

I_S=f(V_{SD}), parameter: T_J

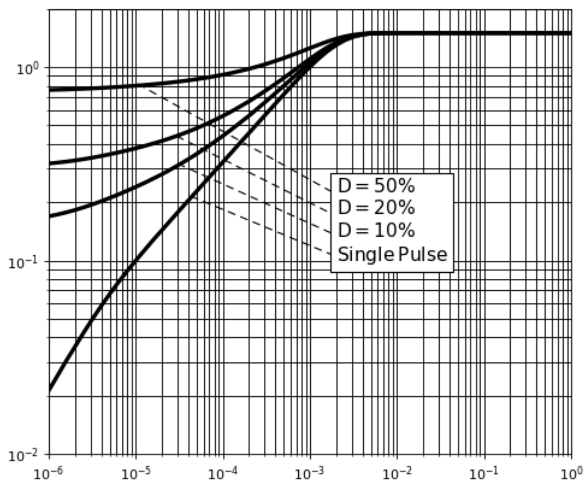


Figure 12. Transient Thermal Resistance

Typical Characteristics (T_c=25°C unless otherwise stated)

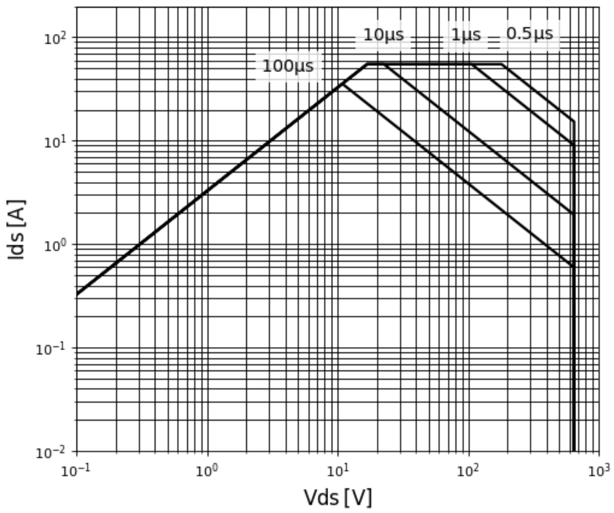


Figure 13. Safe Operating Area T_C=25°C

Test Circuits and Waveforms

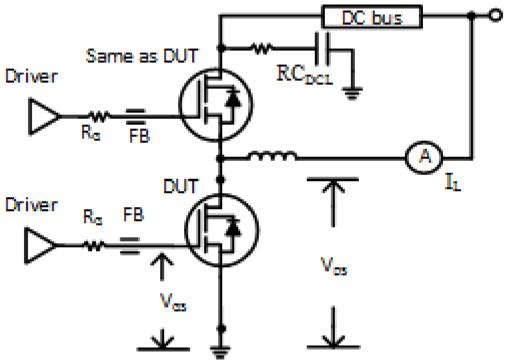


Figure 14. Switching Time Test Circuit

(see circuit implementation on page 3
for methods to ensure clean switching)

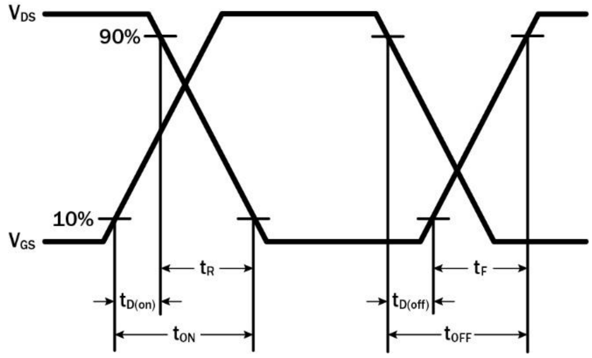


Figure 15. Switching Time Waveform

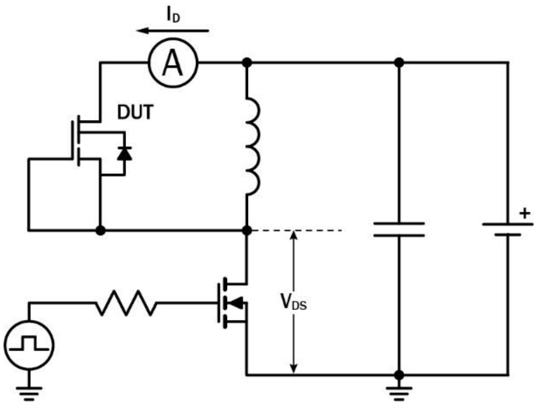


Figure 16. Diode Characteristics Test Circuit

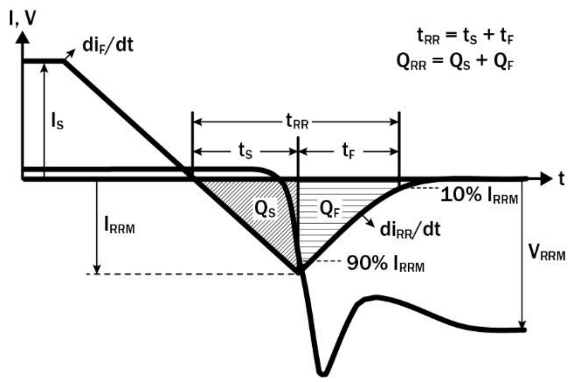


Figure 17. Diode Recovery Waveform

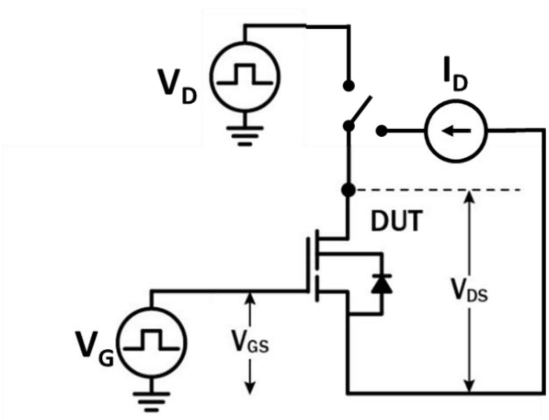


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

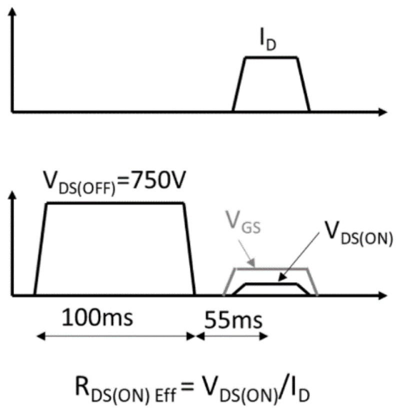


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See Printed Circuit Board Layout and Probing	

GaN Design Resources

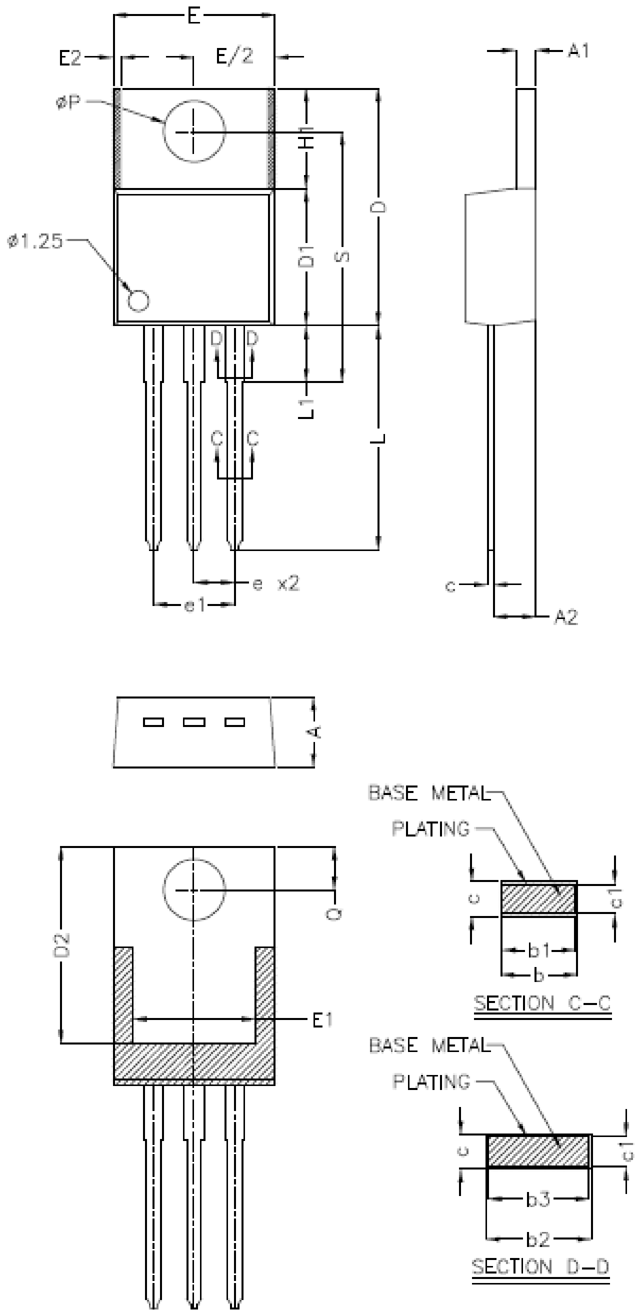
The complete technical library of GaN design tools can be found at Renesasusa.com/design:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical

3 Lead TO-220 (PS) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Source



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.29	4.45	4.73	0.169	0.175	0.186
A1	1.09	1.31	1.40	0.043	0.052	0.055
A2	2.48	2.64	2.93	0.098	0.104	0.115
b	0.77	0.86	1.02	0.031	0.034	0.040
b1	0.70	–	0.86	0.027	–	0.034
b2	1.23	1.33	1.43	0.048	0.052	0.057
b3	1.20	–	1.37	0.047	–	0.054
c	0.35	0.40	0.47	0.014	0.016	0.019
c1	0.35	–	0.43	0.014	–	0.017
D	14.78	14.95	15.75	0.581	0.589	0.620
D1	8.38	–	9.01	0.330	–	0.355
D2	12.19	–	12.88	0.480	–	0.507
E	9.96	10.25	10.36	0.392	0.404	0.408
E1	6.86	–	8.89	0.271	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	6.10	6.37	6.60	0.241	0.251	0.260
L	12.70	13.84	14.27	0.500	0.545	0.562
L1	3.40	3.55	3.90	0.133	0.140	0.154
øP	3.72	3.80	3.88	0.146	0.150	0.153
Q	2.60	2.80	3.00	0.102	0.110	0.119
S	15.42	15.80	16.51	0.607	0.622	0.650

Notes:

1. Dimensions D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extreme of the plastic body.
2. Dimensions E2 and H1 define a zone where stamping and singulation irregularities are allowed.
3. Outline conforms to JEDEC TO–220AB.

TO–220AB			
transphorm			
SCALE 1:1	SHEET 1/1	DRAWING NO. 200014	VER. 3

Mechanical