TP70H130G4PLSG

700V SuperGaN® GaN FET in PQFN 8 × 8 mm Performance Package (source tab)

Description

The TP70H130G4PLSG 700V, 130mΩ Gallium Nitride (GaN) FET is a normally-off switch that uses Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

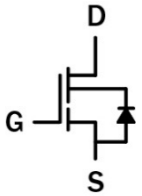
The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

Benefits

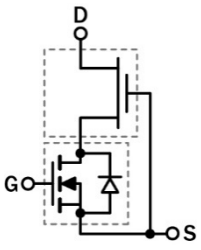
- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with high threshold voltage and no negative gate drive requirement
- Enables high-efficiency, high power density, and reliable power conversion in hard- and soft-switching circuits.
- Facilitates cost-effective GaN adoption, reducing system size, weight, and costs

Product Diagrams

TP70H130G4PLSG PQFN 8 × 8 mm



Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Robust design, defined by
  - Transient over-voltage capability
  - Operation with E-mode gate drivers without need for Zener protection.
- Extremely low crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging
- Low reverse conduction drop V_{SD}

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Specifications

V_{DS} (V)	700
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum	163
Q_{OSS} (nC) typical	29.2
Q_G (nC) typical	10.7

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1. Pin Information

1.1 Pin Assignments

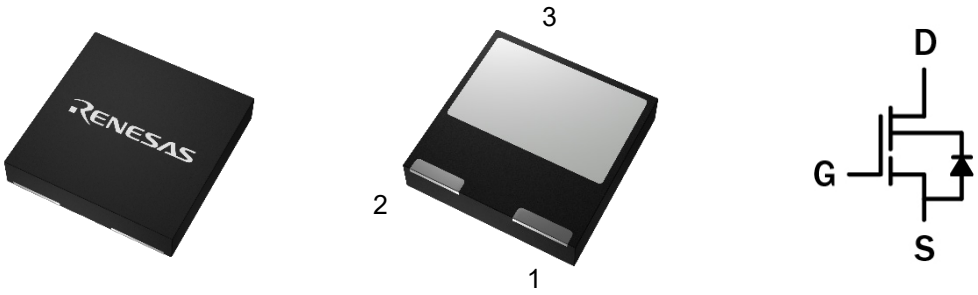


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1	G	Gate.
2	D	Drain.
3	S	Source.

2. Specifications

2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Test Condition	Unit
V_{DSS}	Drain to source voltage	-	700	V_{GS} = 0V,Test as per JEDEC	V
$V_{DSS(TR)\ ,\ non\text{-}repetitive}$	Transient drain to source voltage, non-repetitive	-	800	V_{GS} = 0V, spike duration < 30µs	
$V_{DSS(TR)\ ,\ pulsed}$	Drain to source voltage, pulsed	-	750	V_{GS} = 0V, spike duration < 5µs	
V_{GSS}	Gate to source voltage	-20	+20	-	
P_D	Maximum power dissipation	-	69.4	T_C = 25°C	W
I_D	Continuous drain current at T_C = 25°C	-	16	V_{GS} = 9V, V_{DS} can be positive and negative	A
	Continuous drain current at T_C = 100°C	-	10		
$I_{D(PULSE)}$	Pulsed drain current at T_C = 25°C	-	54	V_{GS} = 9V, pulse width=10µs V_{DS} can be positive and negative	
	Pulsed drain current at T_C = 100°C	-	47		
$I_{SD(PULSE)}$	Pulsed reverse drain current at T_C = 25°C	-	54	V_{GS} = 0V, pulse width = 10µs, V_{DS} <0	
	Pulsed reverse drain current at T_C = 100°C	-	47		
T_J	Operating temperature junction	-55	+150	-	°C
T_S	Storage temperature	-55	+150	Max shelf life depends on storage conditions	°C
T_{SOLD}	Reflow soldering temperature [1]	-	260	-	°C

1. Reflow MSL3.

2.2 Thermal Specifications

Symbol	Parameter	Typical Value	Test Condition	Unit
$R_{\Theta JC}$	Junction-to-case	1.8	-	°C/W
$R_{\Theta JA}$	Junction-to-ambient	52	Device on 40 × 40 mm × 1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70µm thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling.	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	700	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.5 mA	3.2	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-7.6	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance	V_{GS} = 9V, I_D = 4A, T_J = 25°C	-	130	163	mΩ
		V_{GS} = 9V, I_D = 4A, T_J = 150°C	-	267	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 700V, V_{GS} = 0V, T_J = 25°C	-	0.7	10	μA
		V_{DS} = 700V, V_{GS} = 0V, T_J = 150°C	-	5	-	
I_{GSS}	Gate-to-source forward leakage current [1]	V_{GS} = 20V	-	-	10	μA
	Gate-to-source reverse leakage current [1]	V_{GS} = -20V	-	-	-10	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	567	-	pF
C_{OSS}	Output capacitance		-	28	-	
C_{RSS}	Reverse transfer capacitance		-	3.9	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	40.2	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	73	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 9V, I_D = 4A	-	10.7	-	nC
Q_{GS}	Gate-source charge		-	3.2	-	
Q_{GD}	Gate-drain charge		-	4.6	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	29.2	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0 to 9V, R_G= 30Ω, I_D = 4A, at 100MHz (see Figure 15)	-	36.2	-	ns
t_R	Rise time		-	4.3	-	
$t_{D(off)}$	Turn-off delay		-	46	-	
t_F	Fall time		-	14.7	-	

1. MOSFET has integrated ESD Protection Circuit
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{SD}	Reverse voltage	V_{GS} = 0V, I_S = 4A	-	1.3	-	V
		V_{GS} = 0V, I_S = 2A	-	1.1	-	

Note: Reverse recovery charge is negligible enabled by the LV Si FET technology.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

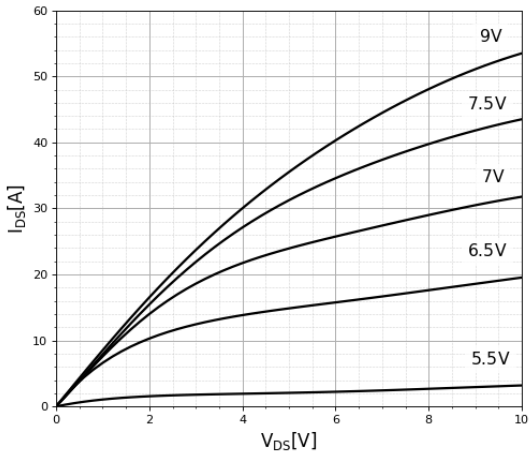


Figure 2. Typical Output Characteristics, T_J = 25°C
Parameter: V_{GS}

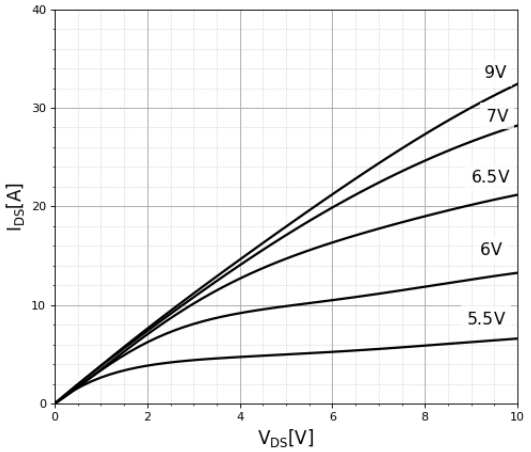


Figure 3. Typical Output Characteristics, T_J = 150°C
Parameter: V_{GS}

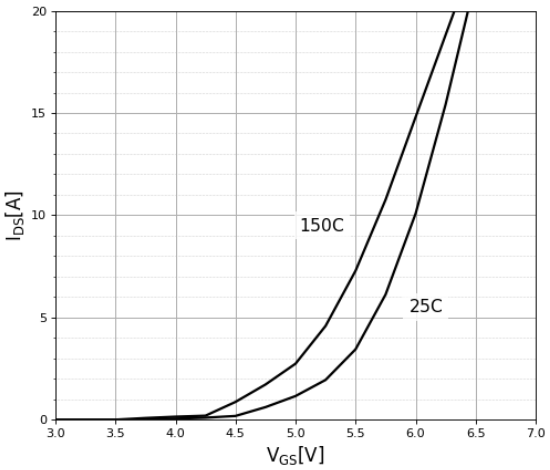


Figure 4. Typical Transfer Characteristics,
V_{DS} = 10V, Parameter: T_J

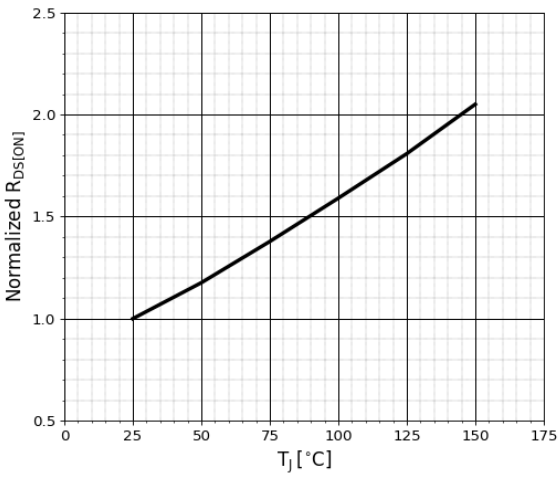


Figure 5. Normalized On-Resistance,
I_D = 4A, V_{GS} = 9V

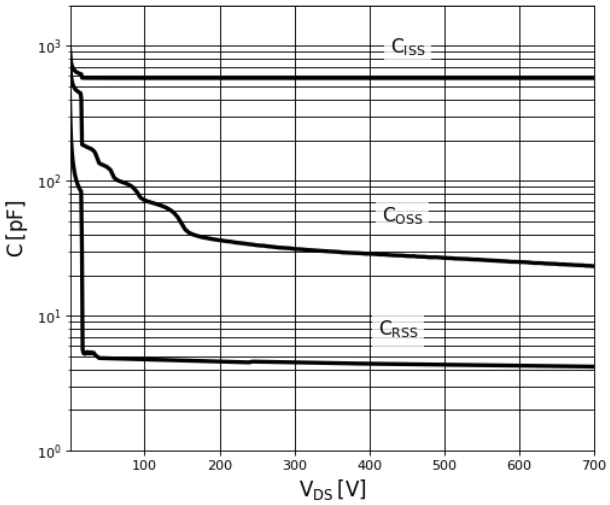


Figure 6. Typical Capacitance,
V_{GS} = 0V, f = 1MHz

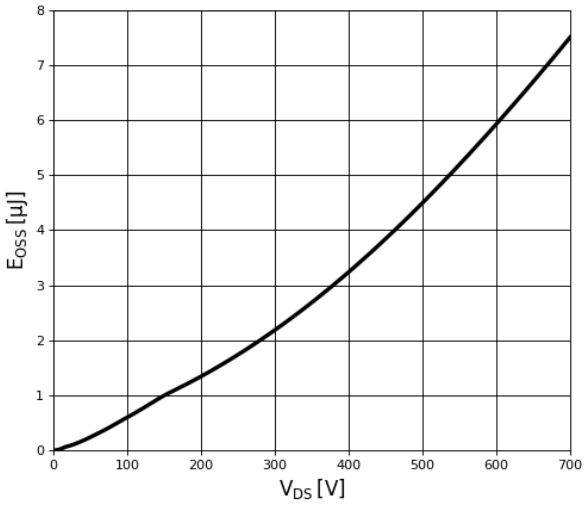


Figure 7. Typical C_{OSS} Stored Energy

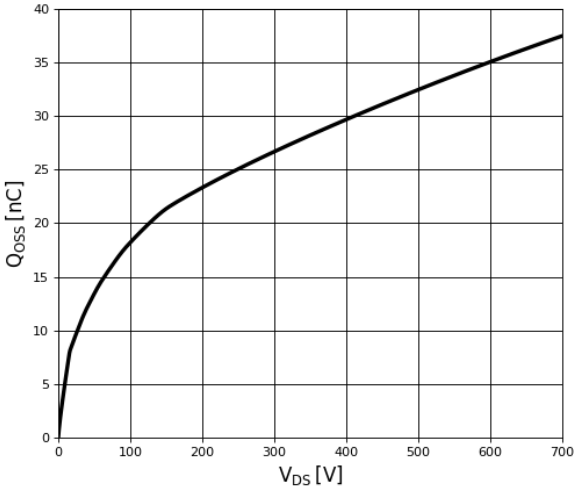


Figure 8. Typical Q_{OSS}

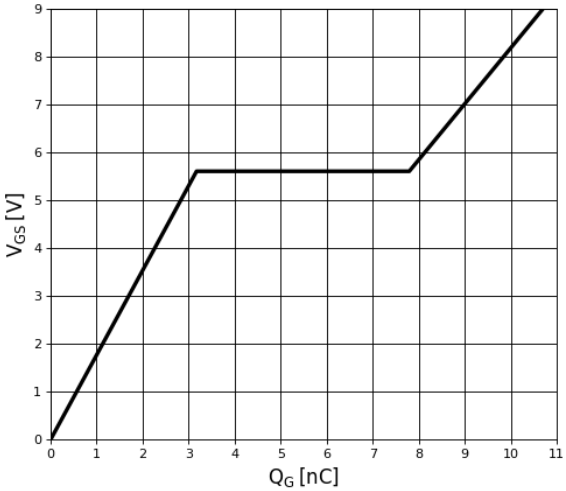


Figure 9. Typical Gate Charge,
I_{DS} = 4A, V_{DS} = 400V

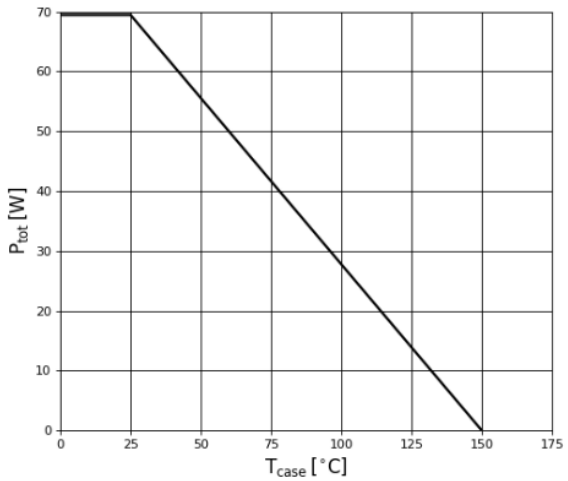


Figure 10. Power Dissipation

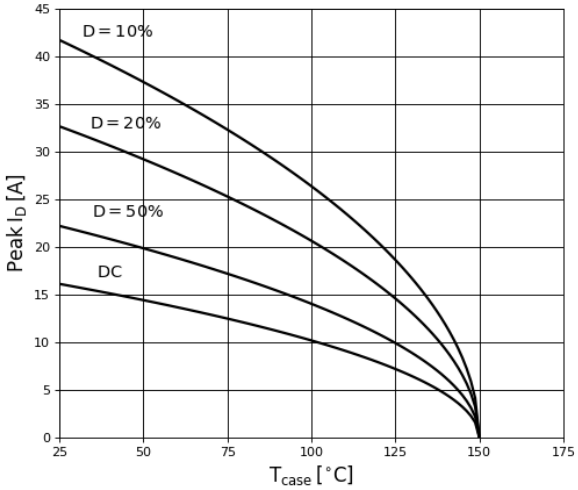


Figure 11. Current Derating,

Pulse width ≤ 10µs, V_{GS} ≥ 9V

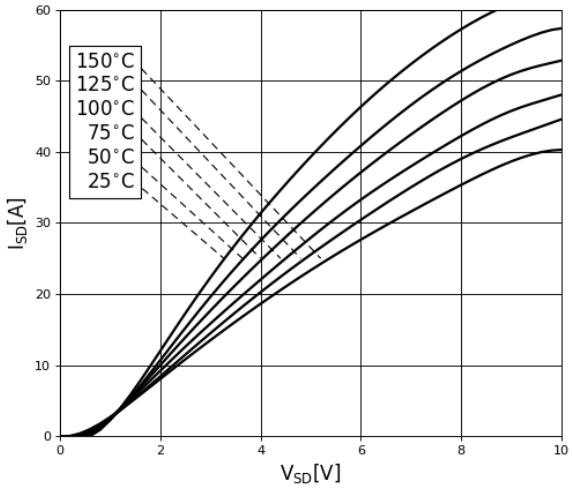


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

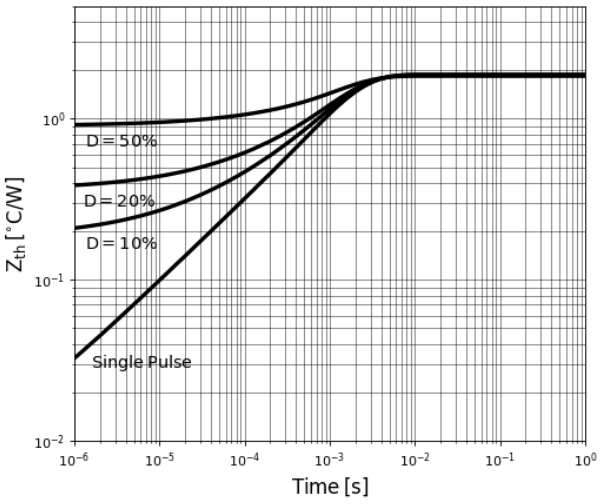


Figure 13. Transient Thermal Resistance

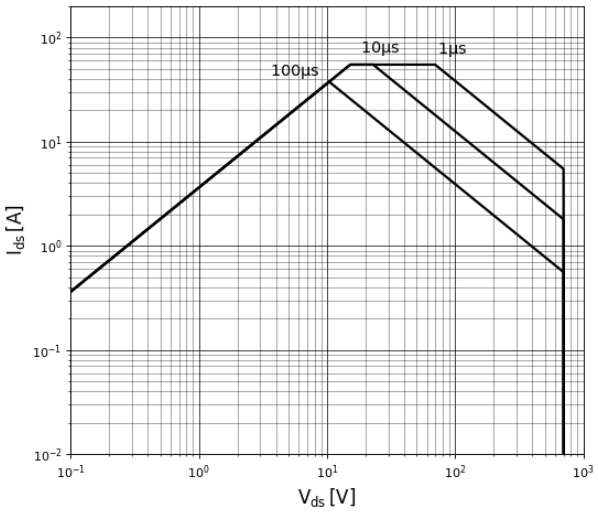


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

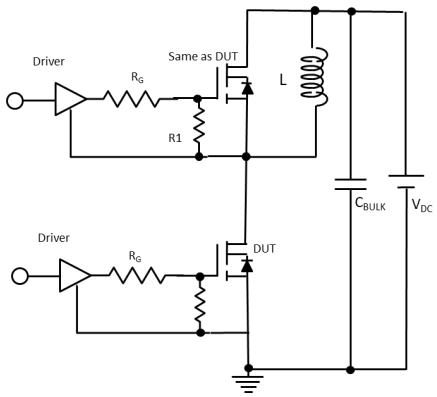


Figure 15. Switching Time Test Circuit

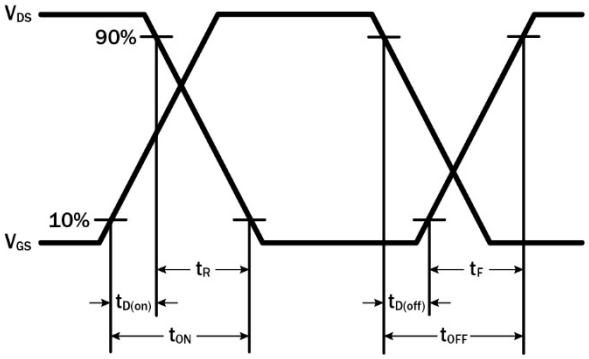
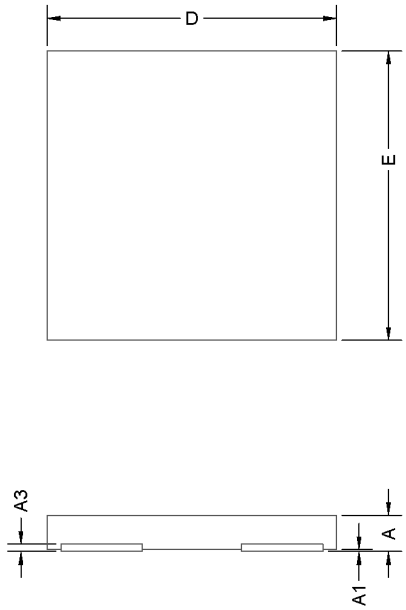
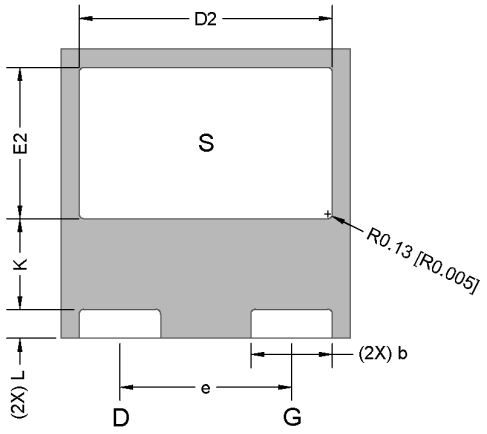


Figure 16. Switching Time Waveform

5. Package Outline Drawings





G: Gate
S: Source
D: Drain
Lead finish: Sn plating

DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 REF.			0.007 BSC	
b	2.20	2.25	2.30	0.087	0.089	0.091
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.85	7.00	7.15	0.270	0.276	0.281
E	7.90	8.00	8.10	0.311	0.315	0.319
e		4.75 BSC			0.187 BSC	
E2	4.03	4.18	4.33	0.159	0.165	0.170
K	2.50	-	-	0.098	-	-
L	0.70	0.80	0.90	0.028	0.031	0.035

QFN 8mm x 8mm POD

transphorm

SCALE 1 : 1 | SHEET 1 / 1 | DRAWING NO.:200119 | VER. 2

Figure 17. Package Outline Drawing – 8 × 8 mm PQFN

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP70H130G4PLSG-TR [1]	PQFN 8 × 8 mm Industry Performance Package	Source tab

1. "-TR" suffix refers to tape and reel.

8. Revision History

Revision	Date	Description
1.00	Feb 20, 2026	Initial release.

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